

MASTER

digital

PDP 12
STUDENT HANDOUTS



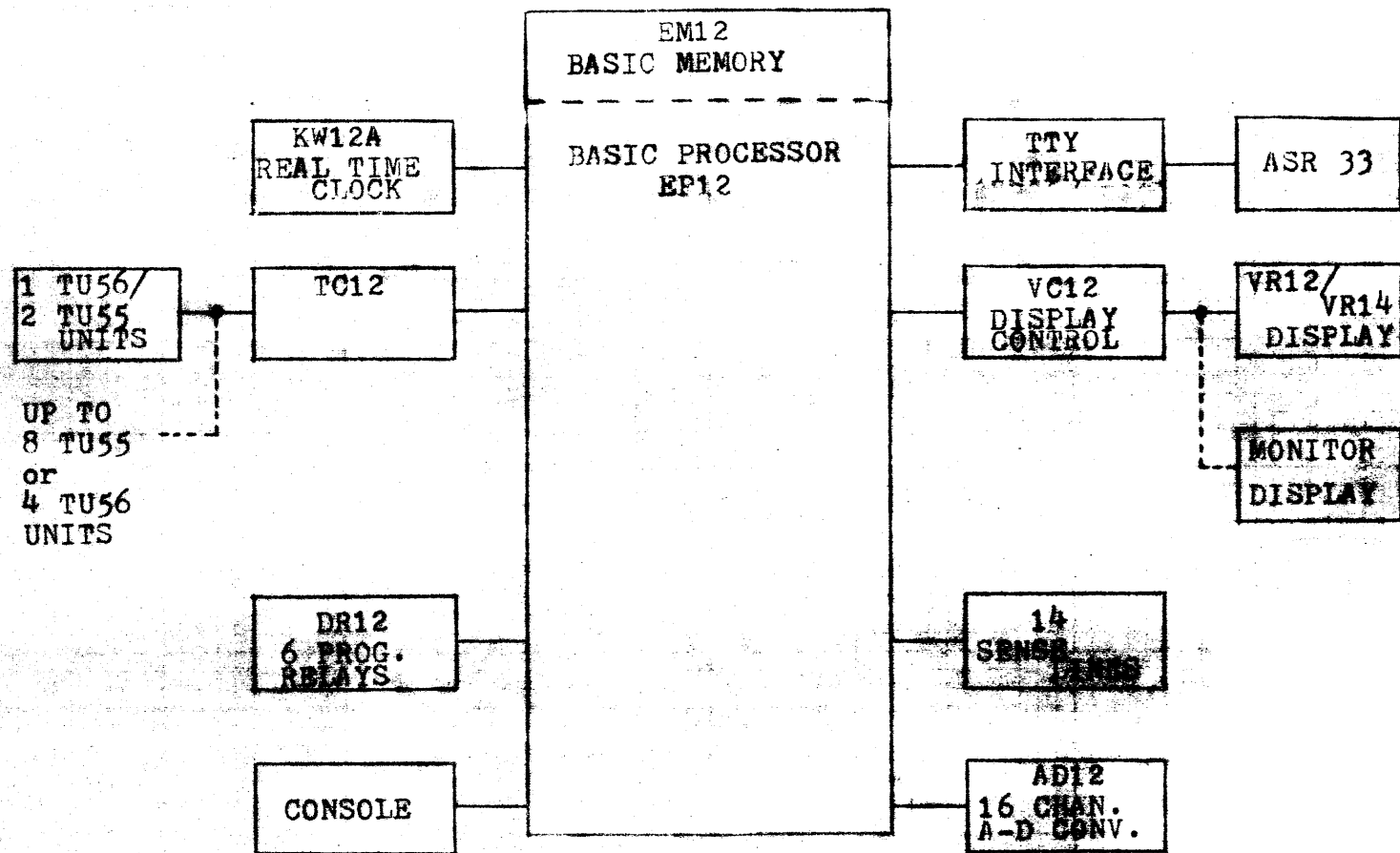
PDP 12
STUDENT HANDOUTS

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PDP-12A SYSTEM BLOCK DIAGRAM

PDP-12 KEY IO PRESET

Key IO Preset kicks off manual timing if run = 0

1.

<u>CST</u>	<u>IO</u>	<u>PRESET</u>	
a.	0	→ IOT PAUSE	CPT
b.	0	→ INTERNAL PAUSE	CPT
c.	-	CPT IO PRESET	CPT
d.	0	→ DO F/F	CST
e.	1	ENABLE MEM	CST
f.	0	→ FILL STEP	CST
g.	0	→ AUTO	CST
h.	0	→ MFTS1.MFTS2	CST
i.	0	→ STEP EX	
j.	0	→ FLOW	
k.	0	→ LINK	FLK
l.	-	LOAD AC	RCL
m.	-	IO PRESET L	IOC
n.	-	IO PRESET	MPG
o.	-	MEM EXT N PRESET	MPG
p.	0	→ RELAY	
2.

a.	CPT SET TS1	→ 1	→ CYCLE DONE (CPT)
b.	1	→ TS1	(CPT)
c.	0	→ TS2	— 5 (CPT)
d.	0	→ RECYCLE SYNC	(CPT)
e.	0	→ T5 RECYCLE	(CPT)
f.	1	→ MEM IDLE	(CPT)
3. CST KEY CONT . MFTP1
 - a. 0 → H (SKH)
 - b. 0 → SKIP (SKH)
4. IOC TO PRESET
 - c. 0 → ADDRESS ACCEPTED (IOC)
 - d. 0 → WC OVERFLOW (IOC)
 - e. 0 → INT ENABLE (IOC)
 - f. 0 → IOP FF 1-2-4 (IOC)

0 → INT DLY (IOC)
5. MPG IO PRESET
 - a. 0 → SF 9 (MPG)
 - b. SET IF to 2(8)
 - c. 0 → INT INHIBIT (MPG)
 - d. SET DF to 3(8)
 - e. SET IB to 2(8)

EIGHT BASIC INSTRUCTIONS

0 → 5 MEMORY REFERENCE INSTRUCTIONS MRT's

AND TAD ISZ DCA JMP JMS
0XXX 1XXX 2XXX 3XXX 4XXX 5XXX

IS MB 3 = 1 OR 0 } 2ND OCTAL
IS MB 4 = 1 OR 0 } DIGIT
IS MB 5 = 1 OR 0 } ANALOGY
0-7

MB 3(0) = DIRECT
MB 3(1) = INDIRECT
MB 4(0) = PAGE ZERO
MB 4(1) = CURRENT PAGE
MB 5(0) = < 100 LOCATIONS
MB 5(1) = ≥ 100 LOCATIONS

TRUTH TABLE

OCTAL	BINARY	ANALOGY
0	000	DIR, P ₃ Z, <100
1	001	DIR, P ₃ Z, ≥100
2	010	DIR, CUR. P ₃ , <100
3	011	DIR, CUR. P ₃ , ≥100
4	100	IND, P ₃ Z, <100
5	101	IND, P ₃ Z, ≥100
6	110	IND, CUR. P ₃ , <100
7	111	IND, CUR. P ₃ , ≥100

6 IN/OUT TRANSFER IOT's

IOT's
FOR TRANS-
FER OF DATA
INTO OR OUT
OF COMPUTER

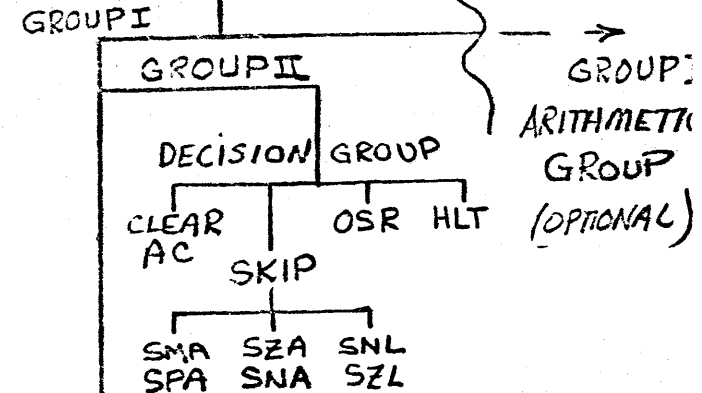
→ IN → OUT
K_{SF} K_{CC} K_{RS} K_{RB} T_{SF} T_{CF} T_{PC} T_{LS}

IS MB 9(1) = IOP 4
IS MB 10(1) = IOP 2
IS MB 11(1) = IOP 1

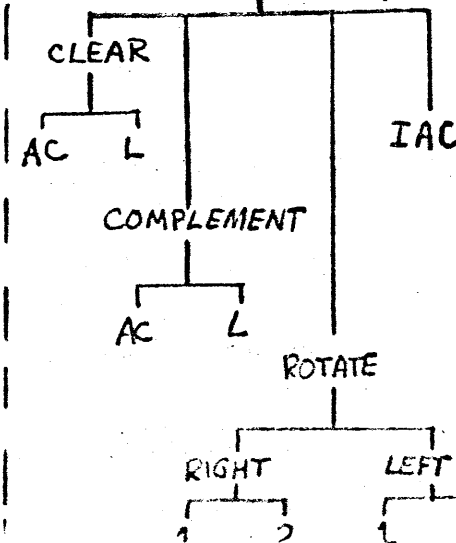
GENERAL IOP USES

IOP 1 - SKIP
IOP 2 - CLEAR
IOP 4 - READ OR LOAD

7 OPERATE GROUPS CPR

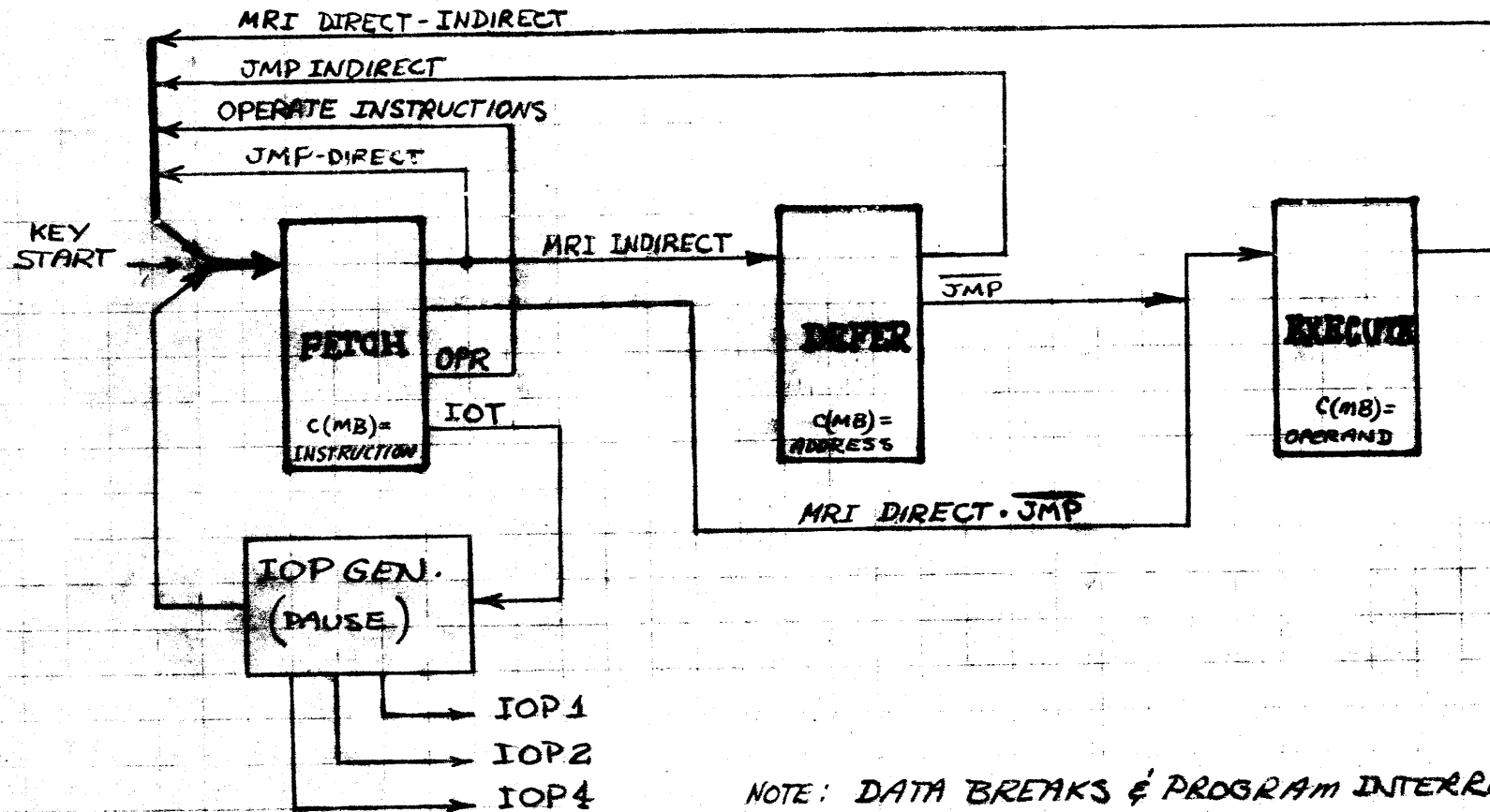


EFFECT IS ON THE AC & L



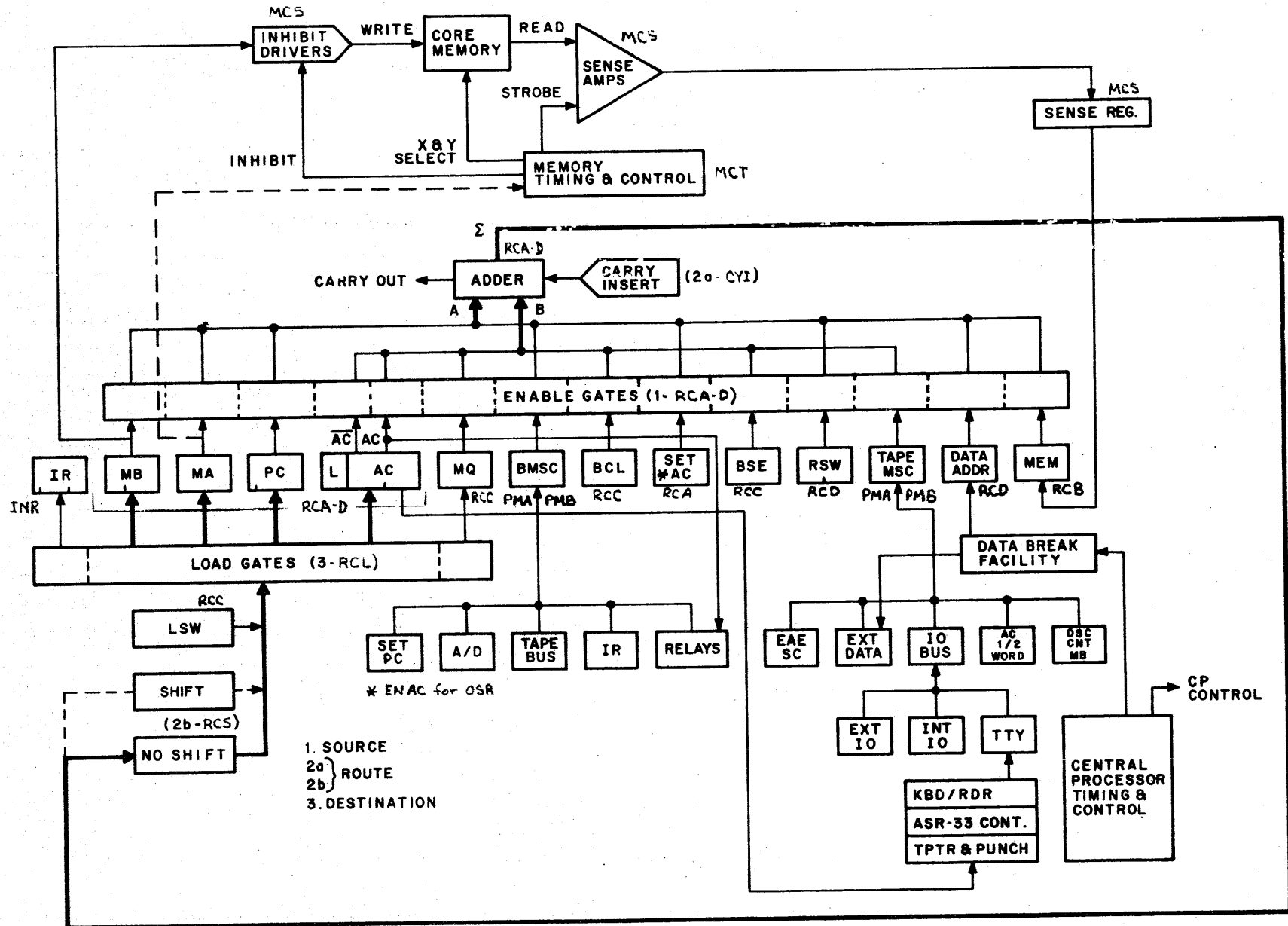
MEMORY BUFFER
0 1 2 3 4 5 6 7 8 9 10 11
↓
0 GPI
1 GP II
1 GP III
C

MAJOR STATE FLOW DIAGRAM



NOTE: DATA BREAKS & PROGRAM INTERRUPTS
HAVE BEEN EXCLUDED FOR SIMPLICITY

PDP-12 DATA FLOW



IS IT A LOGIC ONE OR ZERO ?

EXAMPLES OF LOGIC ONE CONDITIONS

KEY FUNCTIONS: FILL STEP
SEE EXAM
START 400 etc.

TIMING :

1. MANUAL - MFTS1
MFTP2 etc
2. PROCESSOR - TS 1
TF4 etc.
3. MEMORY - READ.
WRITE etc.
4. MAJOR STATES - FETCH
EXECUTE etc.
5. IO - IOP 1
IOP 2 etc.

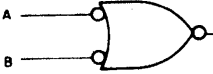
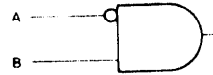
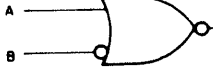
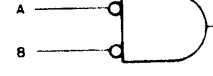
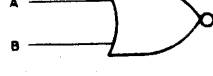
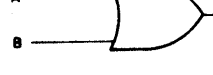
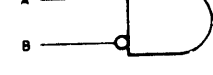
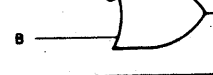
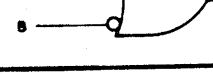
REGISTERS: RC, MA, MB, L, AC, IR, CORE (binary bits) etc.

SIGNALS: EN MB5-11, AC ADDS, 8 JUMP ADDRESS etc.

FUNCTION MODIFIERS: AUTO, RECYCLE etc.

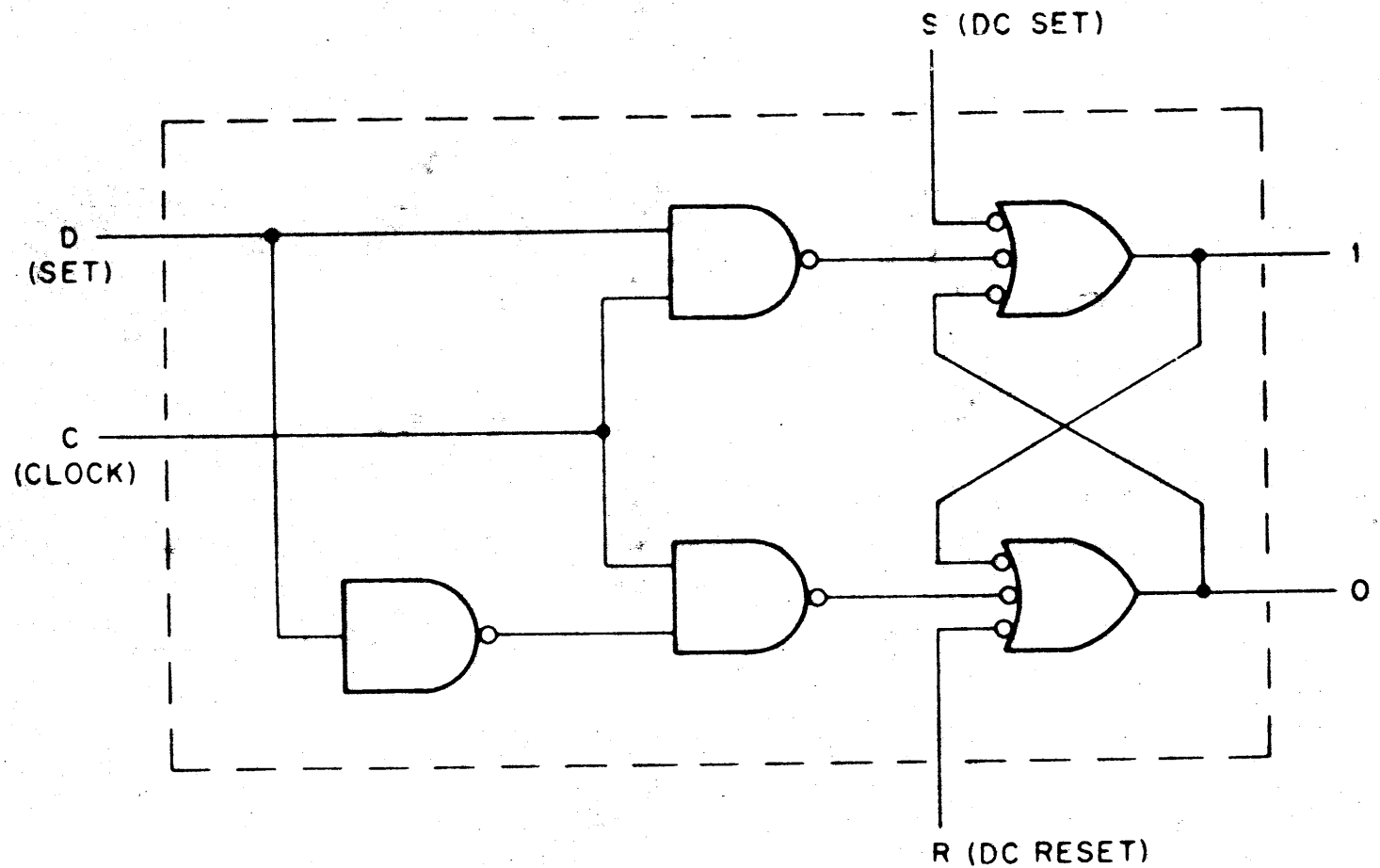
A LOGIC ONE IS A CONDITION THAT IS ACTIVE, TRUE, HAPPENING AND IS NOT NECESSARILY ANY PARTICULAR LOGIC LEVEL i.e., DEC USES DUAL POLARITY DUAL DEFINED LOGIC. THEREFORE, A POLARITY INDICATOR IS REQUIRED IN ADDITION TO THE LOGIC CONDITION NAMED. CONVERSELY, A LOGIC ZERO WOULD BE AN INACTIVE, FALSE OR NEGATED CONDITION AND THE POLARITY INDICATED WOULD BE INCORRECT UNLESS INDICATED TO BE A NOT CONDITION.

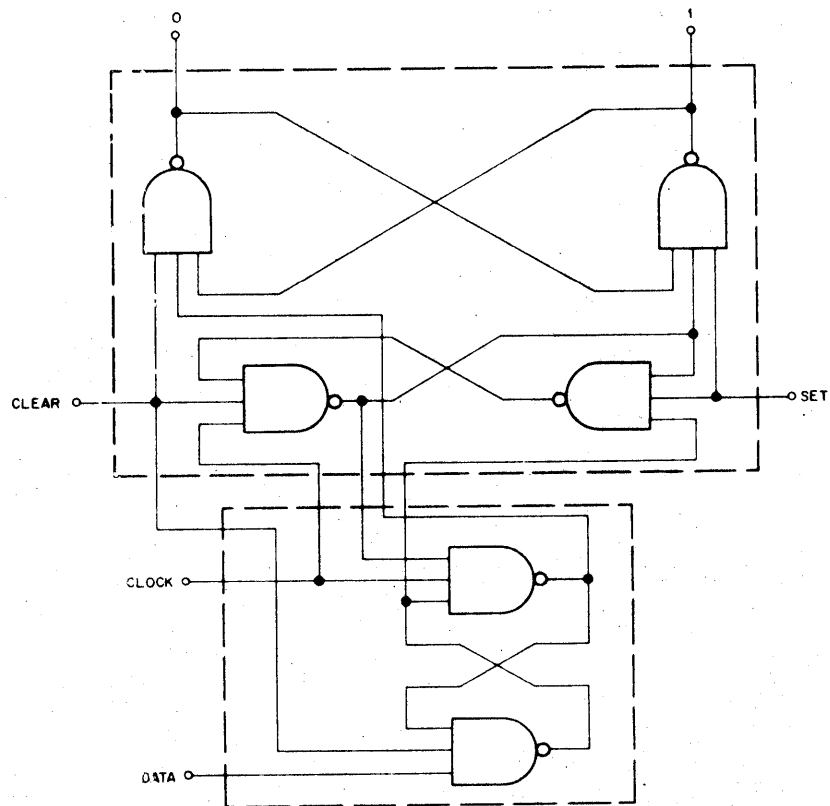
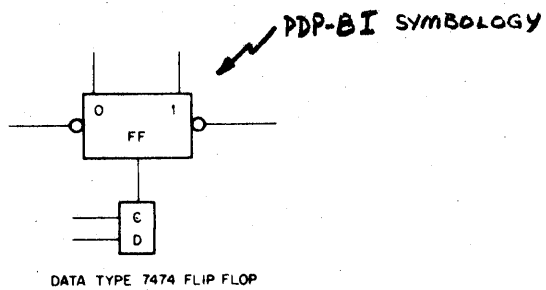
The following table of combinations illustrates the applications and functions of two variables and equivalents.

		TABLE OF COMBINATIONS		
AND	OR	A	B	X
		H	H	H
		H	L	L
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	H
		L	L	L
		H	H	L
		H	L	H
		L	H	L
		L	L	L
		H	H	L
		H	L	L
		L	H	L
		L	L	H
		H	H	H
		H	L	H
		L	H	H
		L	L	L
		H	H	H
		H	L	L
		L	H	H
		L	L	H
		H	H	H
		H	L	H
		L	H	H
		L	L	H

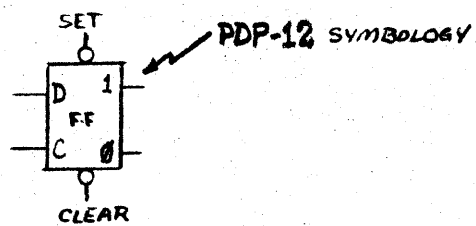
Logic Functions

SIMPLIFIED D-TYPE FLIP-FLOP

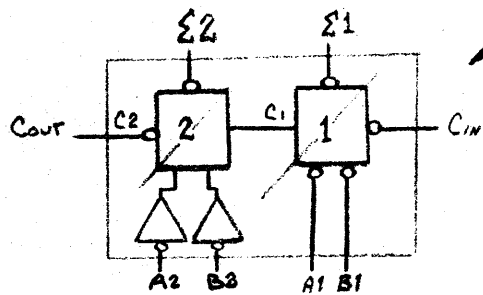




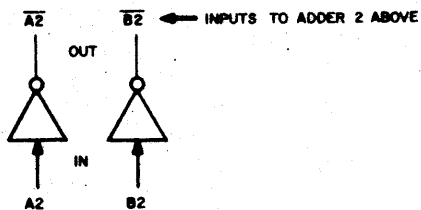
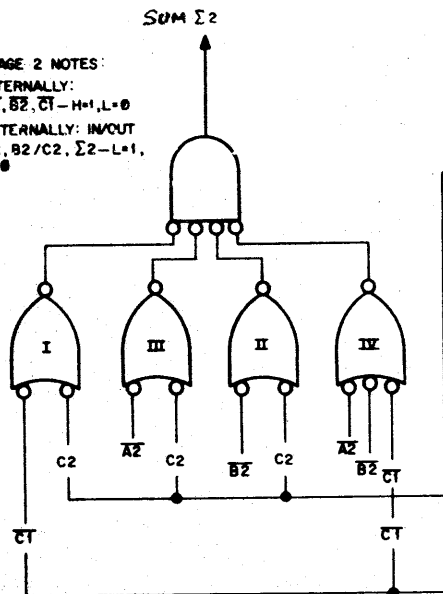
Data Type 7474 Flip-flop



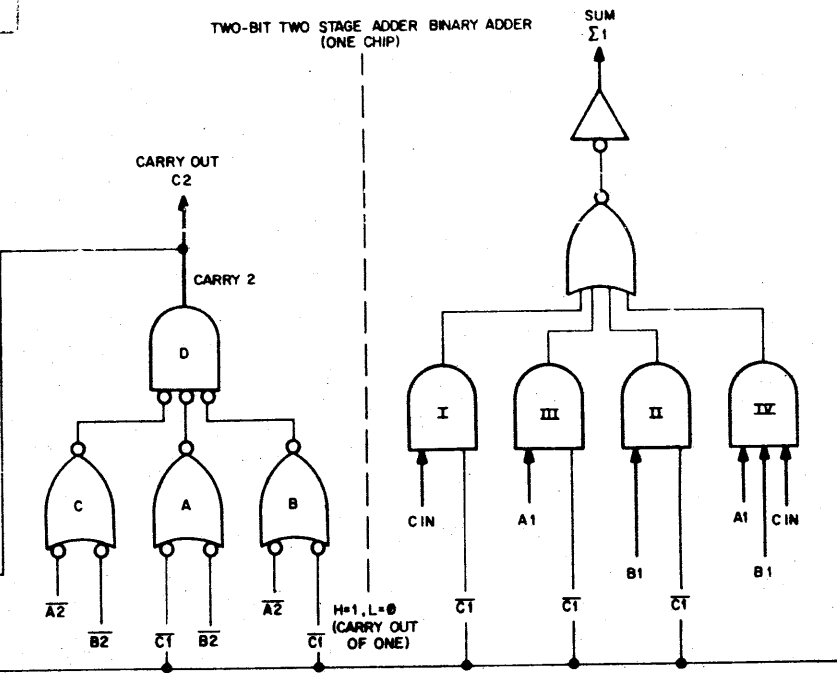
SYMBOLIC REPRESENTATION



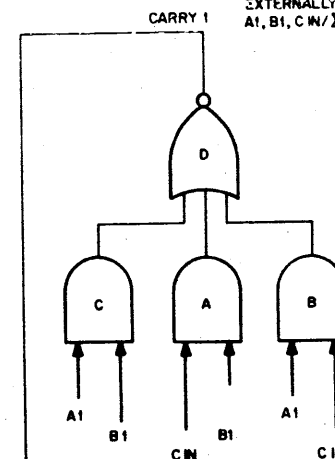
STAGE 2 NOTES:
INTERNALLY:
 $\overline{A2}, \overline{B2}, C1 - H=1, L=0$
EXTERNALLY: IN/OUT
 $A2, B2 / C2, \Sigma2 - L=1, H=0$



TWO-BIT TWO STAGE ADDER BINARY ADDER (ONE CHIP)



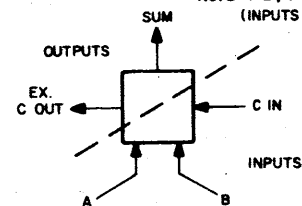
STAGE 1 NOTES:
INTERNALLY:
 $C1 - H=1, L=0$
EXTERNALLY: (IN/OUT)
 $A1, B1, C IN / \Sigma1 - L=1, H=0$



ADDER TRUTH TABLE

	A	B	C IN	Σ	C OUT	
	0	0	0	0	0	NO QUALIFIED GATE
I	0	0	1	1	0	
II	0	1	0	1	0	
	0	1	1	0	1	A
III	1	0	0	1	0	
	1	0	1	0	1	B
IV	1	1	0	0	1	C
	1	1	1	1	1	D

NOTE: 1=L, 0=H
(INPUTS AND OUTPUTS ONLY)



Two-Bit Two Stage Adder-Binary
(One Chip)

Title	Page	Drawing Page Number	Title
PDP-12 System (2 sheets)	7	39 -CPR	Central Processor Run
PDP-12 System (2 sheets)	8	40 -CPS	Central Processor States
PDP-12 System (Parts List) (3 sheets)	10	41 -CPT	CP Time States
Drawing Index (4 sheets)	13	42 -CTPT	Central Processor Time Pulses
PDP-12 Configuration (5 sheets)	17	43 -CSI	Console Switch Inputs
Power Wiring & Signal Cables	22	44 -CST	Console Starts
Manual Timing Function Part 1	23	45 -CYI	Carry Inserts
Manual Timing Function Part 2	24	46 -FLE	Flow & End Shift
Linc Fetch 1A	25	47 -FLK	Link Logic
Linc Fetch 1B	26	48 -ICB	IO & EXT Mem Cables
Linc Fetch 2	27	49 -INR	Instruction Register
Linc Defer	28	50 -INS	Instructions
Linc Execute	29	51 -IOA	IO Input Part A
Linc Execute	30	52 -IOB	IO Input Part B
Linc Execute	31	53 -IOC	IO Control & Timing
Linc Execute	32	54 -IOO	IO Output Buffers
Execute 2 & Interrupt	33	55 -IOR	Relay Buffer
PDP-8 Mode Fetch	34	56 -IPC	Inter Proc Cables
PDP-8 Mode Defer & Execute	35	57 -MEA	Mem Extn AC Inputs
Break	36	58 -MPG	Mem Page Extn Controls
PDP-12 Processor (2 sheets)	37	59 -MQR	Mul Quotient
Console Indicators	38	60 -PMA	Processor Miscellaneous A
		61 -PMB	Processor Miscellaneous B
		62 -PRA	PRA Processor Bits 0 & 1
		63 -PRB	PRB Processor Bits 2 & 3
		64 -PRC	PRC Processor Bits 4 & 5
		65 -PRD	PRD Processor Bits 6 & 7
		66 -PRE	PRE Processor Bits 8 & 9
		67 -PRF	PRF Processor Bits 10 & 11
		68 -RCA	Register Control A
		69 -RCB	Register Control B
		70 -RCC	Register Control C
		71 -RCD	Register Control D
		72 -RCL	Processor Register Load Control
		73 -RCS	Reg Shift & Mo Inputs
		74 -SKH	Skip FF & H Bits
		75 -SKL	EP12 Skips
		76 -SLA	Special Levels
Tape Processor MJR. St. Flow	111		
Tape Inst Setup Timing	112		
Search Timing	113		
Block Mode Reading	114		
Block Mode Write	115		
Block Mode Checking	116		
Mark Timing	117		
LINC-8 Scope Display	142		

98 -PCM	Inter Proc Cables
99 -MCS	MCS Sense Amps & Inhibit Drivers
100 -MCT	Memory Control
101 -MCX	X-Axis Selection
102 -MCY	Y-Axis Selection

118 -LCS	Tape Control States
119 -LCX	Tape Extended Operations
120 -LCXF	Tape Extended Fields
121 -LGP	Tape Group Counter
122 -LIN	Tape Instruction
123 -LIP	Interprocessor Signals
124 -LMU	Tape Unit and Motion
125 -LRE	Tape Reg Enable Control
126 -LRL	Tape Reg Load Control
127 -LTC	Transport Control
128 -LTD	Tape Delays
129 -LTM	Tape Maint
130 -LTMR	Tape Maint Reg
131 -LTR	Tape Readers-Writers
132 -LTRA	LTRA Bits 0 & 1
133 -LTRB	LTRB Bits 2 & 3
134 -LTRC	LTRC Bits 4 & 5
135 -LTRD	LTRD Bits 6 & 7
136 -LTRE	LTRE Bits 8 & 9
137 -LTRF	LTRF Bits 10 & 11
138 -LTS	Tape States
139 -LTT	Tape Time Pulse
140 -LWN	Tape Mark Window

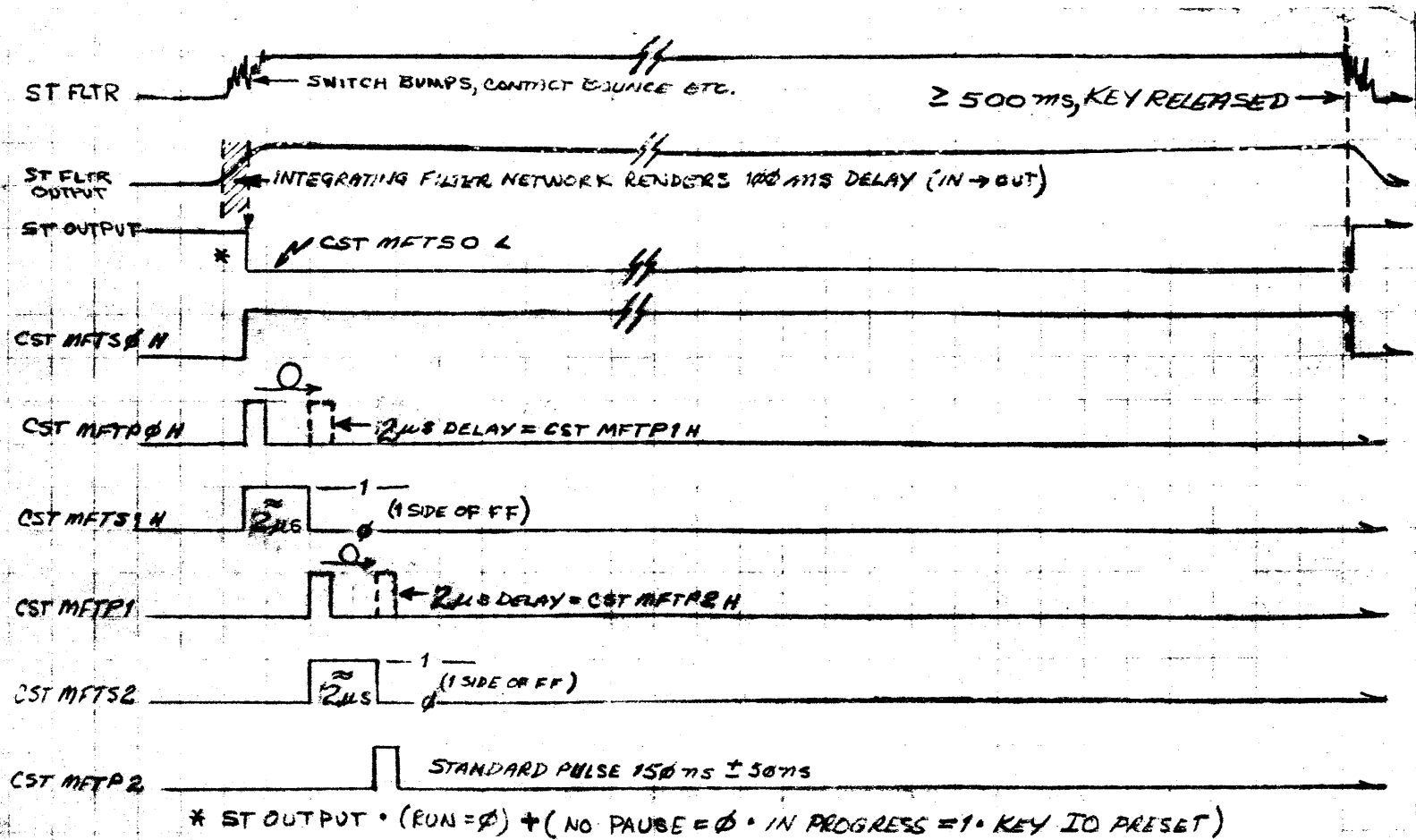
197 -YAD	A-D Converter
198 -YADA	YADA Chan 10-17
199 -YADB	YADB Chan 20-37
200 -YADC	YADC A-D Control

143 -DSC	DSC Display Control
144 -DSX	DSX Horizontal D-A

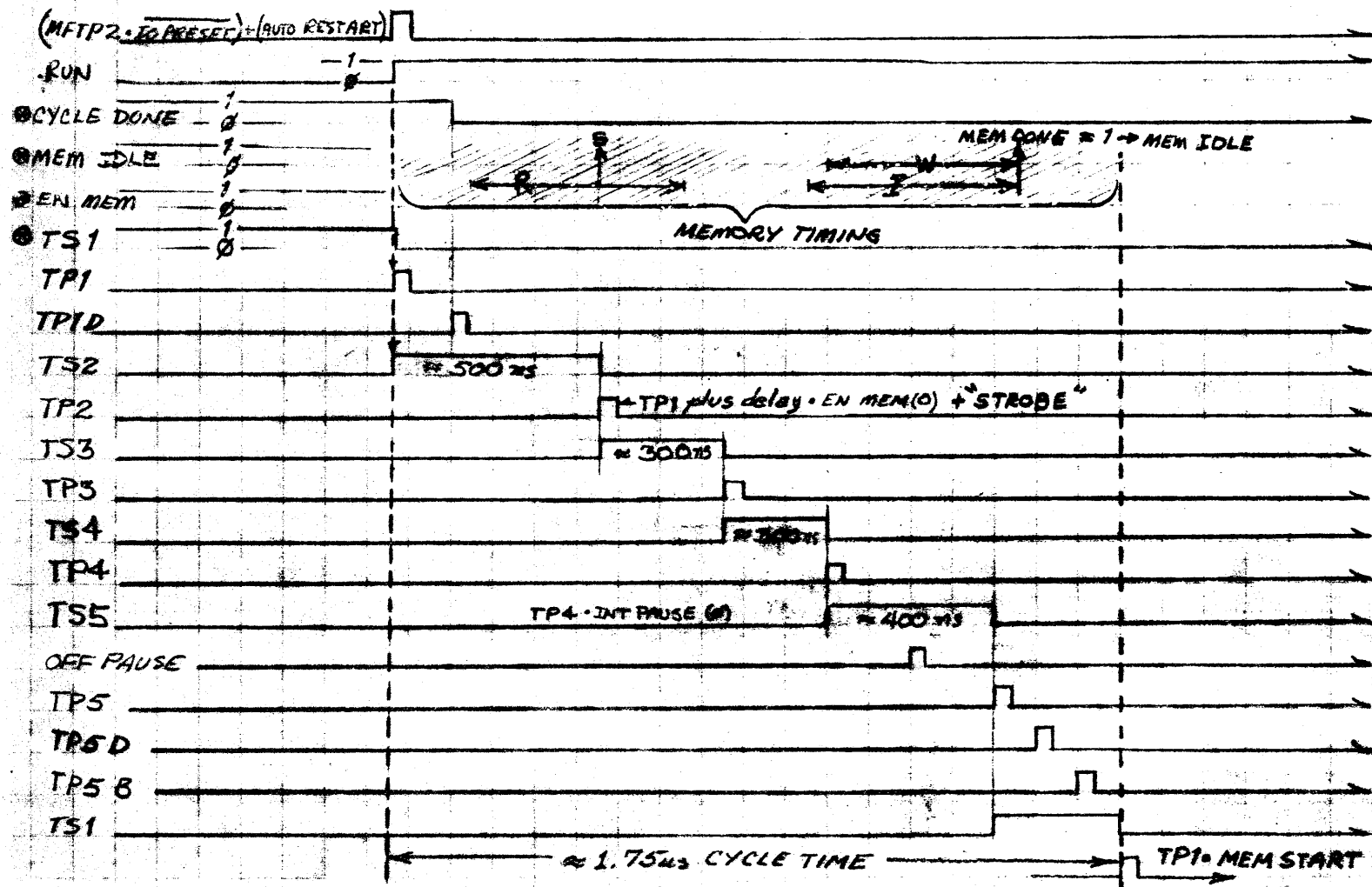
77 -TTI	TTI Teletype Receiver
78 -TTO	TTO Teletype Transmitter

81	Module Utilization Proc
82	Module Utilization Proc
90	Module Utilization Rack A-D
91	Module Utilization Rack E-F

KEY OPERATIONS TIMING



CENTRAL PROCESSOR-TIMING & RUN

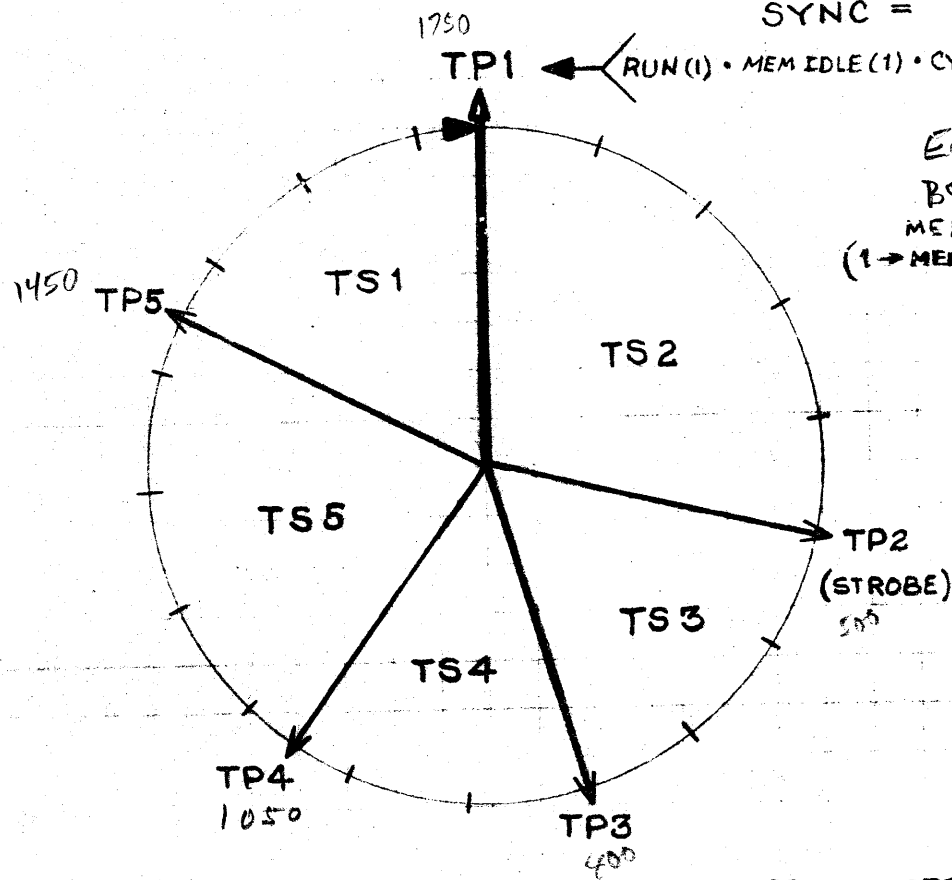


IO PRESET OCCURS WHEN POWER IS APPLIED & WILL 1 → CYCLE DONE, MEM IDLE, EN MEM & TS1

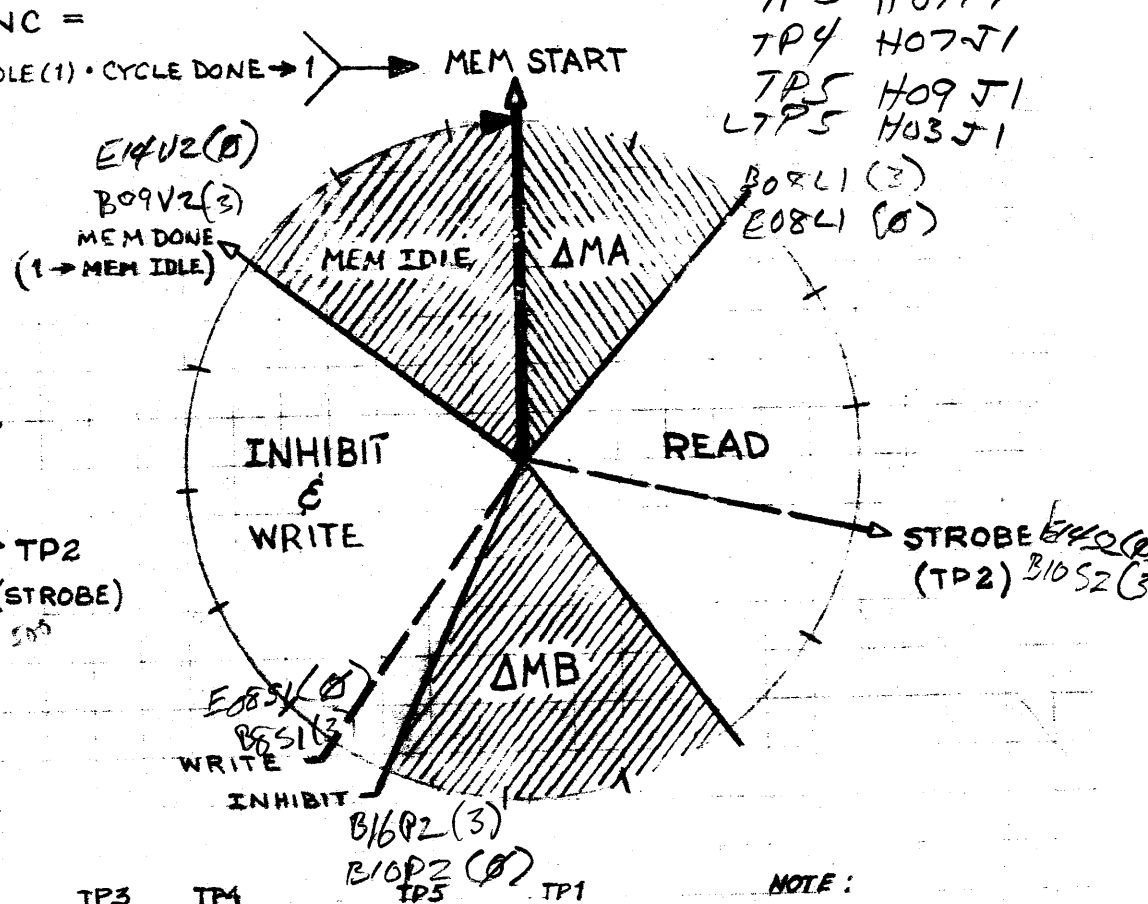
R. Towne

CYCLE TIME

PROCESSOR CYCLE



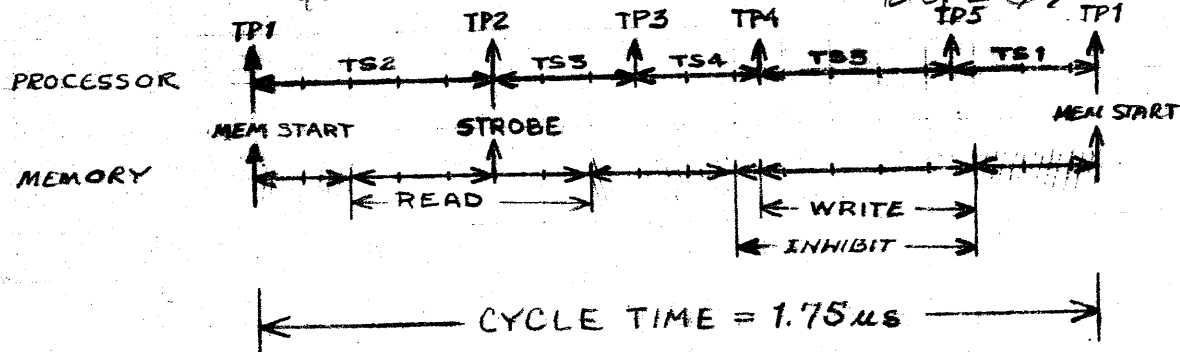
MEMORY CYCLE



TP1 L05J2
 TP2 J07E1
 TP3 H07F1
 TP4 H07J1
 TP5 H09J1
 LTP5 H03J1

B08L1 (3)
 E08L1 (0)

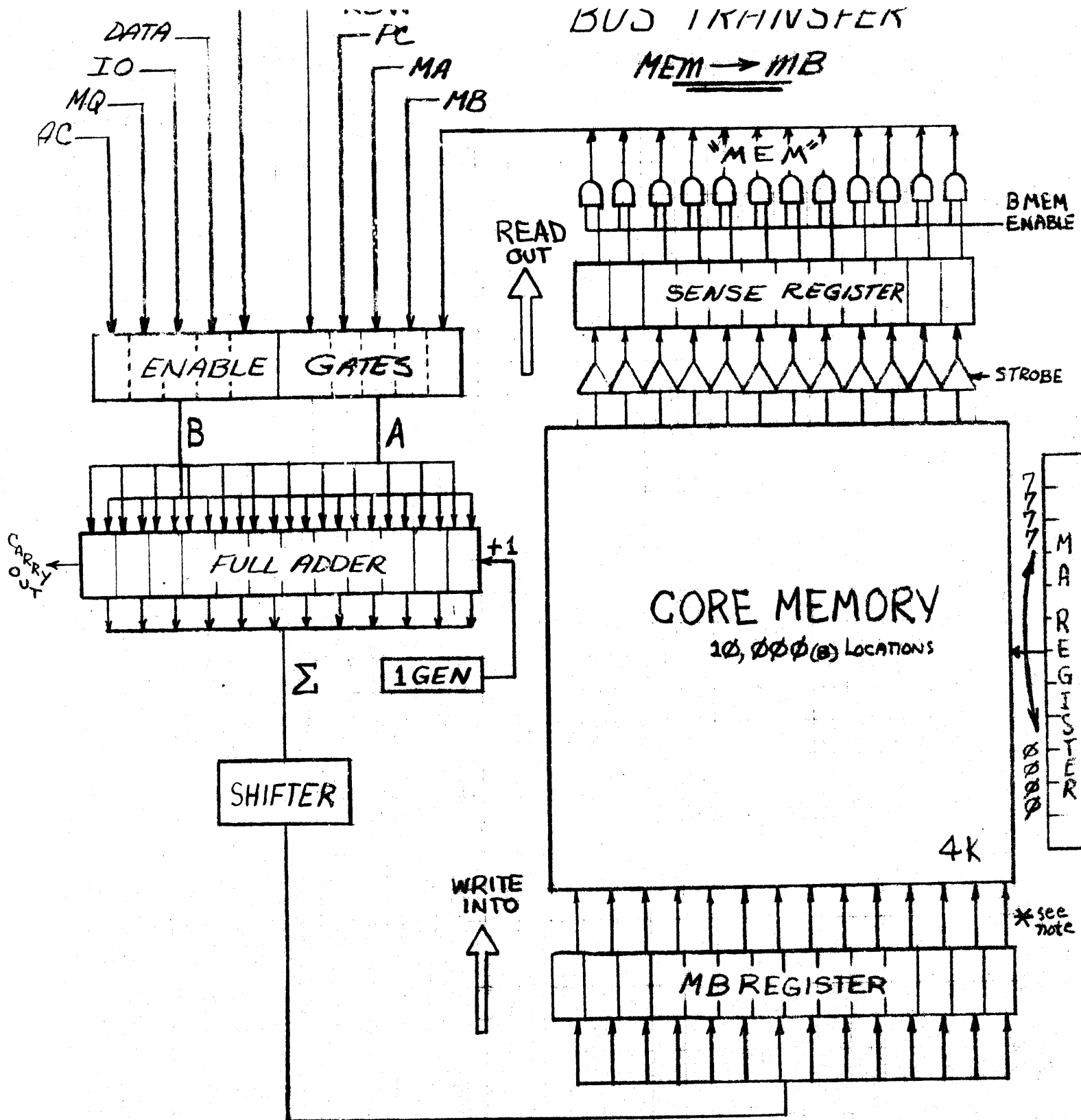
E14V2 (0)
 B10S2 (3)



NOTE:

1. GRADIENT MARKS REPRESENT 100 NS
2. TIMES ARE ACADEMIC

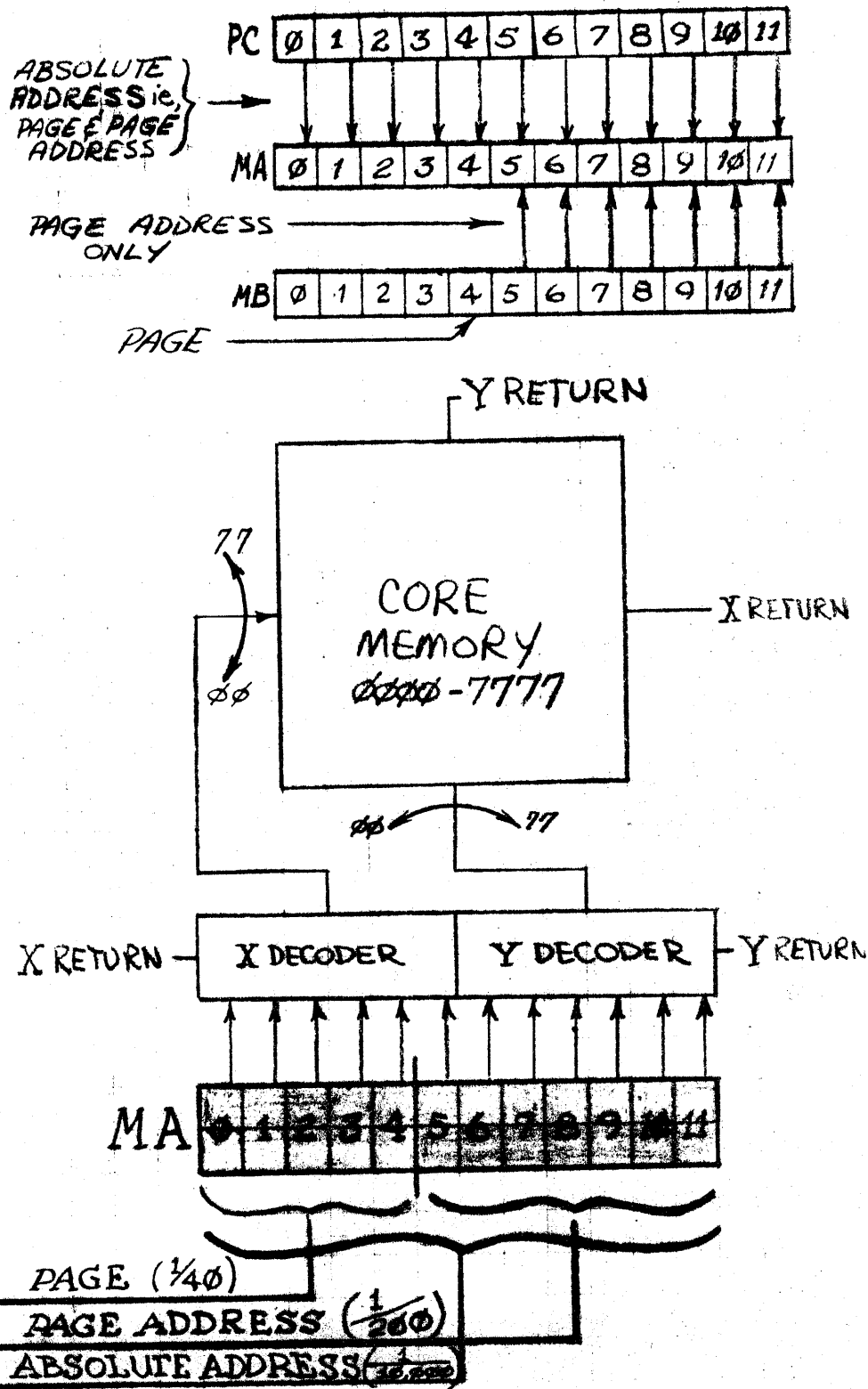
1.75



* NOTE: INHIBIT DRIVERS ARE NOT SHOWN

R. D. Lane

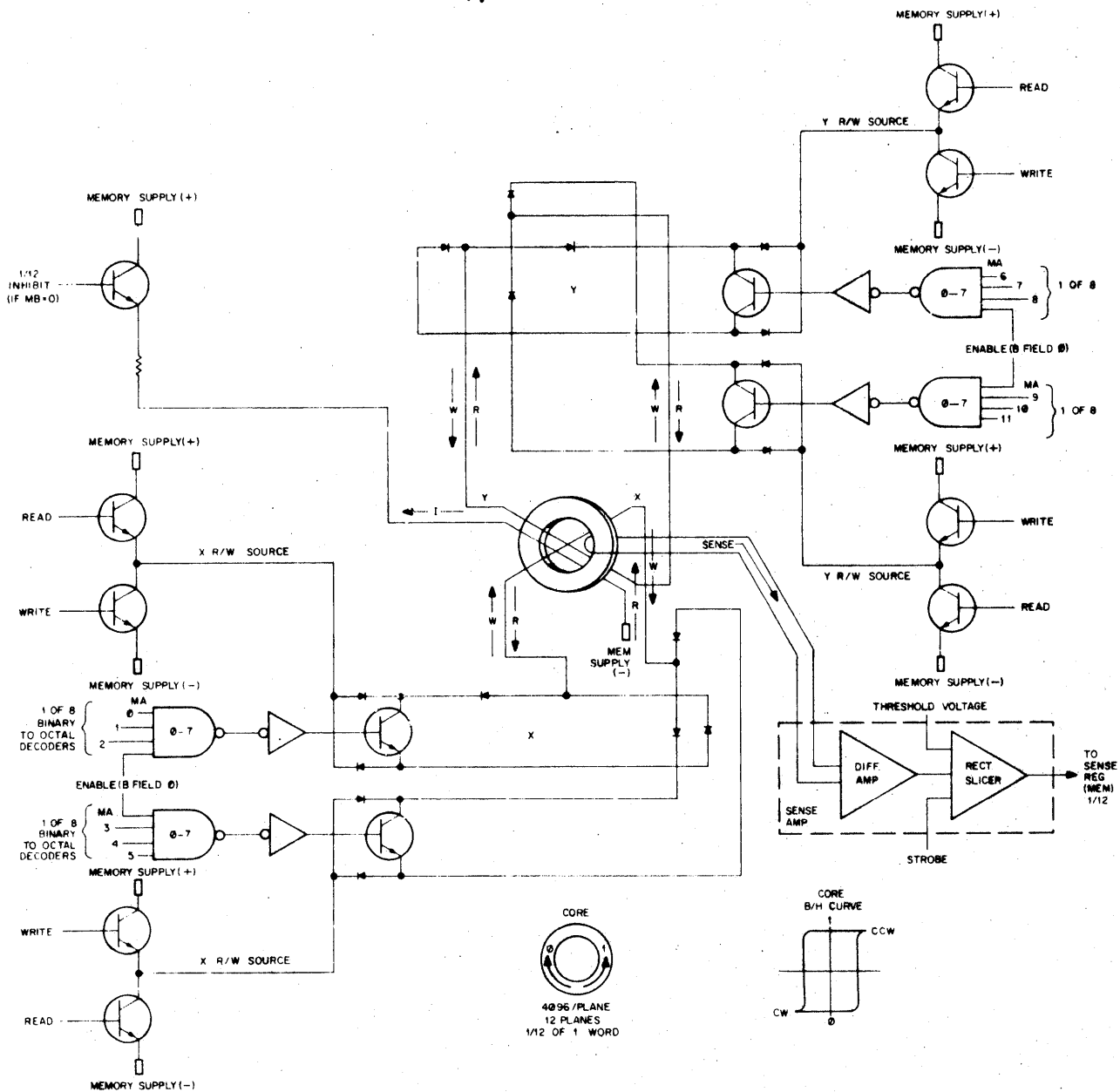
ADDRESS		ADDRESS
7600 - 7799	37	000 - 177
7400 - 7599	36	000 - 177
7200 - 7399	35	000 - 177
7000 - 7199	34	000 - 177
6600 - 6799	33	000 - 177
6400 - 6599	32	000 - 177
6200 - 6399	31	000 - 177
6000 - 6199	30	000 - 177
5600 - 5799	27	000 - 177
5400 - 5599	26	000 - 177
5200 - 5399	25	000 - 177
5000 - 5199	24	000 - 177
4600 - 4799	23	000 - 177
4400 - 4599	22	000 - 177
4200 - 4399	21	000 - 177
4000 - 4199	20	000 - 177
3600 - 3799	17	000 - 177
3400 - 3599	16	000 - 177
3200 - 3399	15	000 - 177
3000 - 3199	14	000 - 177
2600 - 2799	13	000 - 177
2400 - 2599	12	000 - 177
2200 - 2399	11	000 - 177
2000 - 2199	10	000 - 177
1600 - 1799	7	000 - 177
1400 - 1599	6	000 - 177
1200 - 1399	5	000 - 177
1000 - 1199	4	000 - 177
0600 - 0799	3	000 - 177
0400 - 0599	2	000 - 177
0200 - 0399	1	000 - 177
0000 - 0199	0	000 - 177



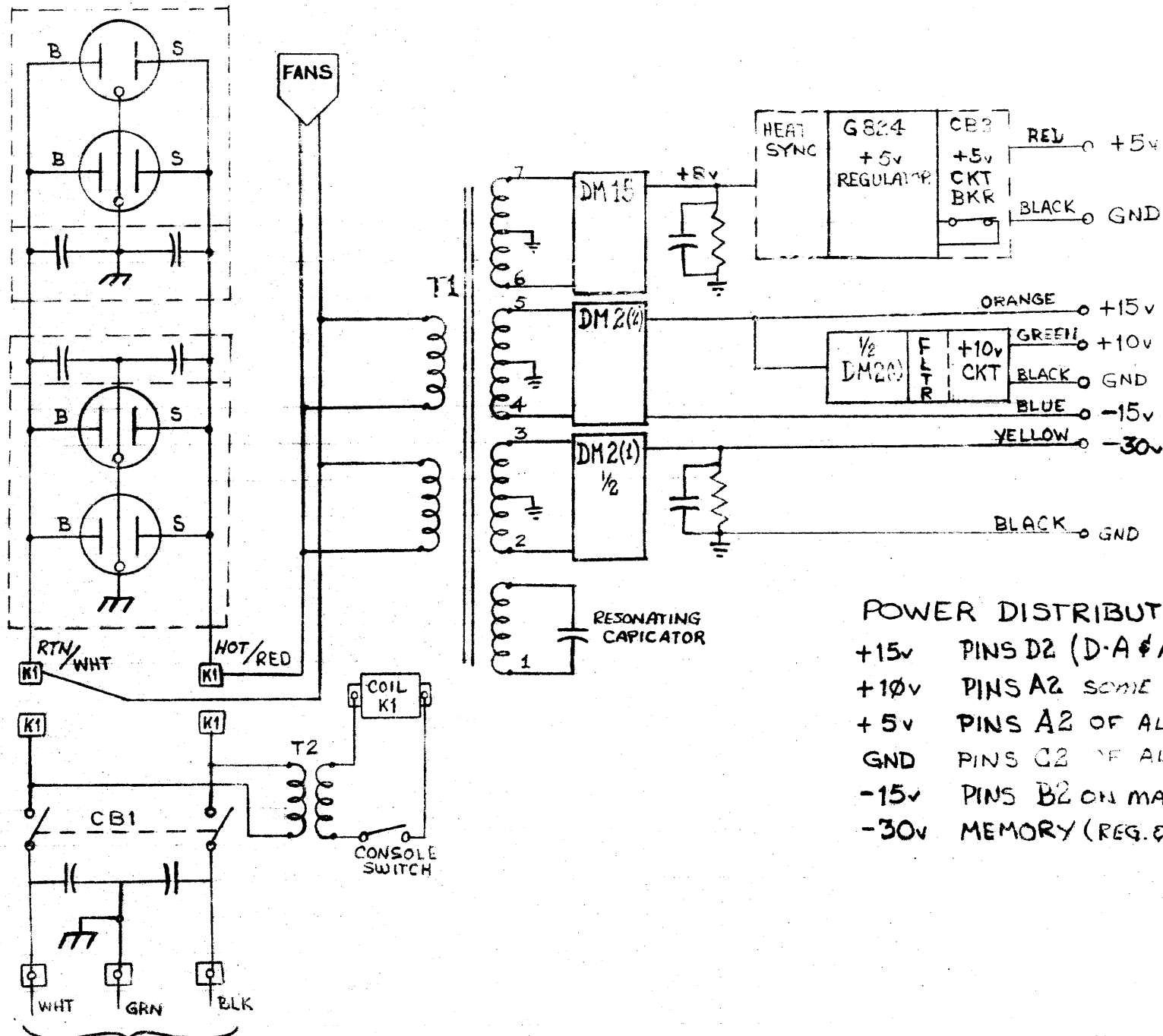
- 14 -

Female care and...

ADDRESS SELECTION



POWER SUPPLY 724 (60 HZ)



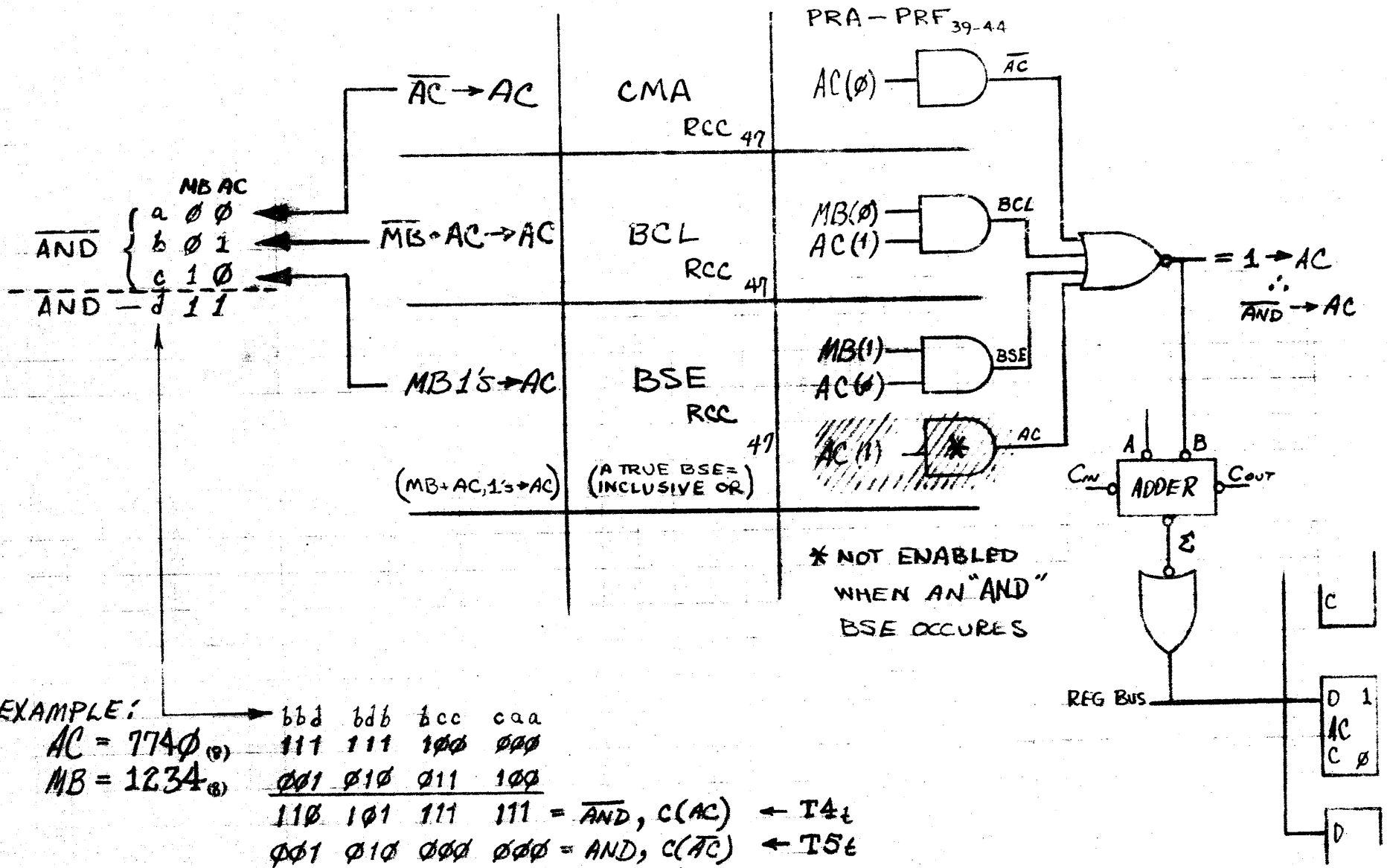
NOTE: see diagram
1. POWER WIRING
& SIGNAL CABLES
PDP12-0-3
2. POWER SUPPLY 724
724-0-1

POWER DISTRIBUTION:

- +15V PINS D2 (D-A & A-D, SCHMITT TRIG., PANEL LIGHTS)
- +10V PINS A2 SOME PAGES (R SERIES LOGIC & TUS)
- +5V PINS A2 OF ALL LOGIC ROWS
- GND PINS C2 OF ALL LOGIC ROWS (F2, HQ GND)
- 15V PINS B2 ON MANY MODULES (TU53)
- 30V MEMORY (REG. & CONT., G-826) & TTY

117V $\pm$ 10V, 60 $\pm$ 1 cps, 30 AMP. HUBBEL CONNECTOR, TEMP. 40°-105°F, REL. HUMIDITY 20%-80%

"AND" INSTRUCTION LOGIC



LINC MODE INSTRUCTIONS

SUBGROUP

<u>FULL ADDRESS</u>	<u>INDEX (BETA)</u>	<u>NON-INDEX</u>	
ADD 2000	LDA 100C	SHD 1400	MSC 00XX
STC 4000	STA 1040	SAE 1440	
JMP 6000	ADA 110C	SRO 1500	HLT 0000
	ADM 1140	BCL 1540	AXO 0001
	LAM 1200	BSE 1600	PDP 0002
	MUL 124C	BCO 1640	TAC 0003
	LDH 1300	NO INST 2 1700	ESF 0004
		1737} T(32)	QAC 0005
	STH 1300	DSC 1740	DJR 0006
			CLR 0011
			ATR 0014
			RTA 0015
			NOP 0016
			COM 0017
			XOA 0021
			TMA 0023
			SFA 0024
			SET 0040
			SAM 0100
			DIS 0140
			XSK 0200
			ROL 0240
			ROR 0300
			SCR 0340
			SXLn040n {Ø-13s}
			SNS 044n {Ø-5}
			AZE 0450
			AP0 0451
			LZE 0452
			KST 0415
			FLO 0454
			QLZ 0455
			IBZ 0453
			SKP 0456
			STD 0416
			TWC 0417
			LOPR 05XX
			0501} T(15)
			0515}
			IOB 0500
			RSW 0516
			0521} T(15)
			0535}
			LSW 0517
			NO INST 1 0540
			0540} T(32)
			0571}
			LMB (LIF) 0600
			UMB (LDF) 0640
			MTP 07XX
			RDE 0702
			RDC 0700
			RCG 0701
			WRI 0706
			WRC 0704
			WRG 0705
			CHK 0707
			MTB 0703
			EXC 0740} T(32)
			0777}

NOTE: T = Trap Codes

LINC 8 "CODE" ORIENTED FORMAT

LINC MODE

Mnemonic	Code	Operation	Direct	Indirect
<u>Miscellaneous</u>				
HLT	0000	halt	3	
ZTA†	0005	Z to A: (11 bits) i equals 1 to 11	3	
ENI†	0010	enable interrupt	N/A	
CLR	0011	clear accumulator, link, and Z register	3	
ATR	0014	(Ac-Ait) → R register	3	
RTA	0015	R register → (Ac- Ait)	3	
NOP	0016	no operation	3	
COM	0017	C(A) → C(A)	3	
SET	0040	C(p+1) → R regis- ter (or indirect)	4.5	6
SAM	0100	sample analog	19.5	
DIS	0140	display (dot)	18	
XSK	0200	skip on 1777	4.5	
<u>Shift</u>				
		if i = 1 include LINK bit		
ROL	0240	rotate left	3-13.5	
ROR	0300	rotate right also shift right into Z register	3-13.5	
SCR	0340	scale right also shift right into Z register	3-13.5	
<u>Skip</u>				
SXL	0400	skip if external level is -3	3	
KST	0415	skip if key has been struck	3	
SNS	0440	skip if sense switch is up	3	
PIN†	0446	pause interrupt	N/A	
SKP	0440	skip unconditionally	3	
AZE	0450	skip if accumulator zero	3	
APO	0451	skip if accumulator positive	3	
LZE	0452	skip if link zero	3	
IBZ	0453	skip if between tape blocks	3	
FLO†	0454	skip if add overflow flag is set	3	
ZZZ†	0455	skip if bit 11 of Z register is 0	3	
		i=0 skip if condition met i=1 skip if condition not met		
<u>Operate</u>				
PDP†	0513	transfer to PDP-8 programming at location contained in LINC A register		
TYPT	0514	TYPE the ASC ii character in the LINC A register on the teletypewriter		
KBD	0515	read keyboard into ac- cumulator	<200	
RSW	0516	read right switch register into accumu- lator	<200	
LSW	0517	read left switch regis- ter into accumulator	<200	

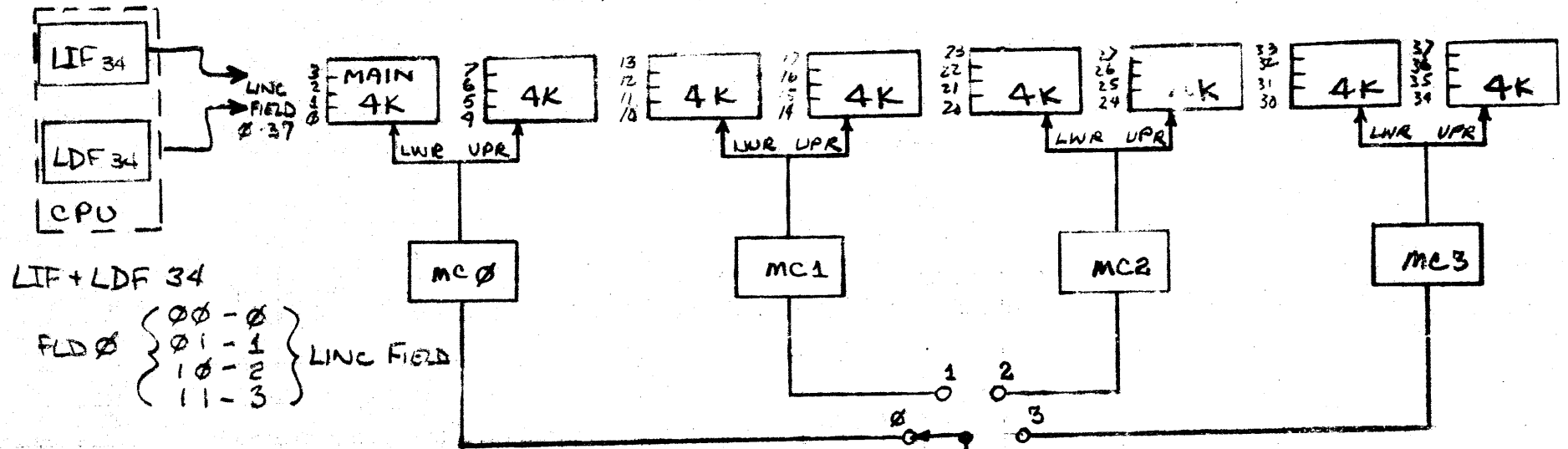
* Classic LINC only † Not defined in LAP 4

Mnemonic	Code	Operation	Direct	Indirect
<u>Memory Bank</u>				
LMB†	0600	change contents of lower memory bank selector	3	
UMB†	0640	change contents of upper memory bank selector	3	
<u>Magnetic Tape (MTP)</u>				
RDC	0700	read and check one block		
RCG	0701	read and check n con- secutive blocks		
RDE	0702	read one block into memory		
MTB	0703	move tape toward des- ignated block	(times depend on tape position)	
WRC	0704	write and check one block		
WCG	0705	write and check n consecutive blocks		
WRI	0706	write one block		
CHK	0707	check one block		
		i=0 stop tape after instruction i=1 leave tape in motion after instruction		
<u>Mode Change</u>				
EXC†	0740	transfer to PDP-8 pro- gram control	<120 depends on PROGOFOP	
<u>Arithmetic</u>				
LDA	1000	load accumulator	3	4.5
STA	1040	store contents of ac- cumulator	4.5	6
ADA	1100	add to contents of ac- cumulator	3	4.5
ADM	1140	add to contents of memory register	6	7.5
LAM	1200	add contents of link and accumulator to contents of memory register	6	7.5
MUL	1240	multiply	33	34.5
<u>Half Word Operations</u>				
LDH	1300	transfer half word from memory into the right half of accumu- lator	3	4.5
STH	1340	transfer the half word from the right side of accumulator register into the designated half of a memory register	4.5	6
SHD	1400	skip if the half word in accumulator regis- ter and the memory register differ	4.5	6

† Not defined in LAP 4

Mnemonic	Code	Operation	Direct	Indirect
<u>Memory Reference Operations</u>				
SAE	1440	skip if the contents of the accumulator equal the contents of the designated memory register	4.5	6
SRO	1500	skip if the right-most bit in the designated memory register is 0; after testing, rotate the contents one place to the right	4.5	6
BCL	1540	for each bit position of memory register Y that contains a 1, clear the correspond- ing bit position of the accumulator (logical AND)	3	4.5
BSE	1600	for each bit position of memory register Y that contains a 1, set the corresponding bit position of the accu- mulator (inclusive OR)	4.5	6
BCO	1640	for each bit position of memory register Y that contains a 1, complement the cor- responding bit posi- tion of the accumu- lator (exclusive OR)	3	4.5
<u>Character Display</u>				
DSC	1740	display the character stored in the desig- nated memory register	75-140	
<u>Full Address</u>				
ADD	2000	add the contents of the designated mem- ory register to accu- mulator	3	
STC	4000	store the contents of accumulator in the designated memory register then clear ac- cumulator	3	
JMP	6000	jump to another desig- nated memory register for the next instruc- tion	3 (1.5 if to location 0)	
<u>Index Class Addressing</u>				
		i=0, R=0 operand address is in p+1		
		i=0, R≠0 operand address is in R register		
		i=1, R=0 operand is in next location		
		i=1, R≠0 operand address (less 1) in R register when execution starts (auto indexing)		

EA - EXTENDED ADDRESS CONTROL



LIF + LDF 34

FLD 0 { 00 - 0
01 - 1
10 - 2
11 - 3 } LINC FIELD

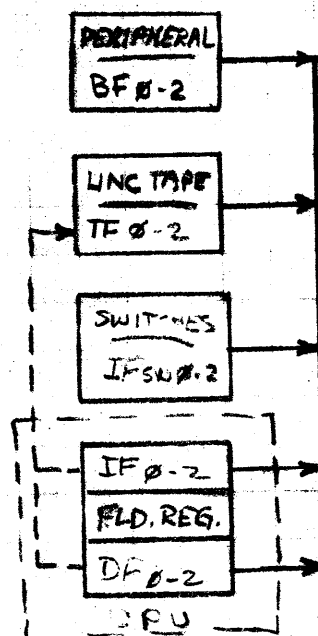
EA 012 LF 34

000	00
000	01
000	10
000	11
001	00
001	01
001	10
001	11
010	00
010	01
010	10
010	11
011	00
011	01

etc,

EXAMPLE

MC 01 ← 01 1 01
 ↓ ↓
(1 of 4) UPPER 4K 1 of 4
 (1 of 2)



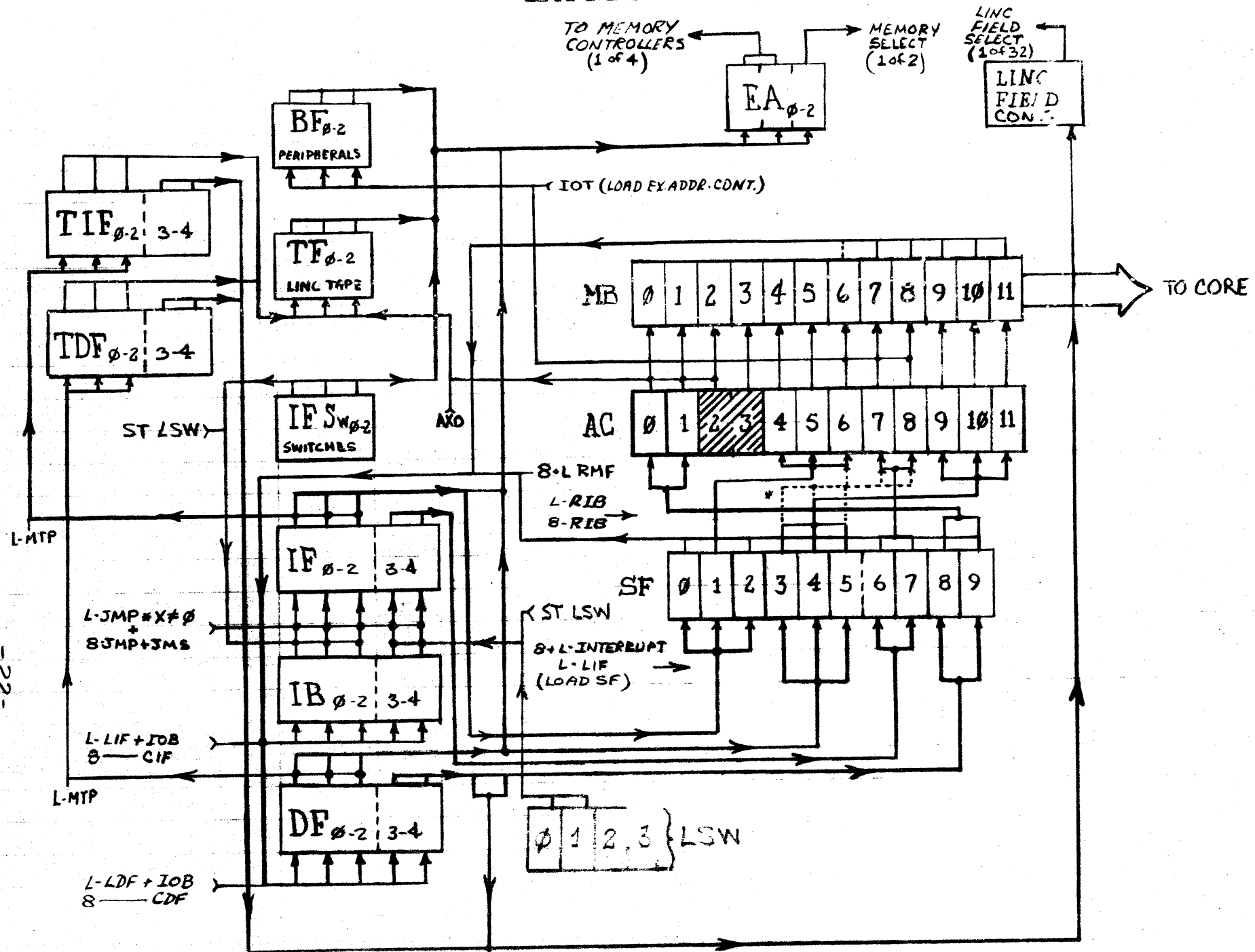
EA 012

MEM CONT

0	(00)	0-LWR
0	(00)	1-UPR
1	(01)	0-LWR
1	(01)	1-UPR
2	(10)	0-LWR
2	(10)	1-UPR
3	(11)	0-LWR
3	(11)	1-UPR

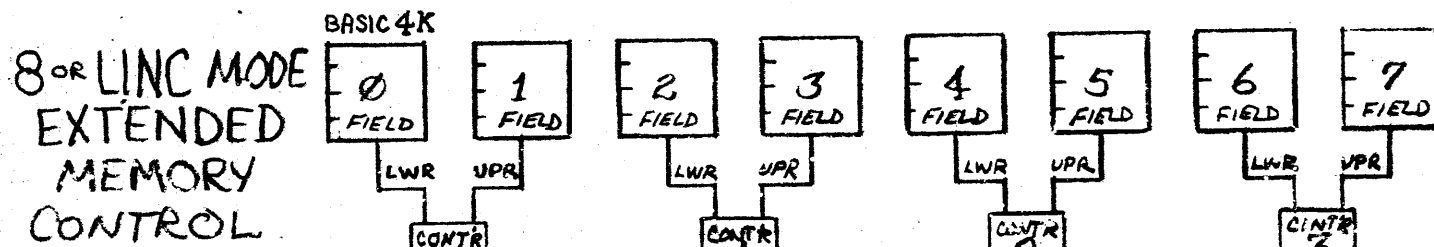
1 of 8 = 4K MEM

EXTENDED MEMORY BLOCK DIAGRAM



* NOTE: DOTTED LINE REPRESENTS AN 8-MODE DEVIATION

EXTENDED MEMORY CONTROL



CONTROLLER	FIELD
0	00 0 LWR
	00 1 UPR
1	01 0 LWR
	01 1 UPR
2	10 0 LWR
	10 1 UPR
3	11 0 LWR
	11 1 UPR

EAIF=DF 0 1 2"

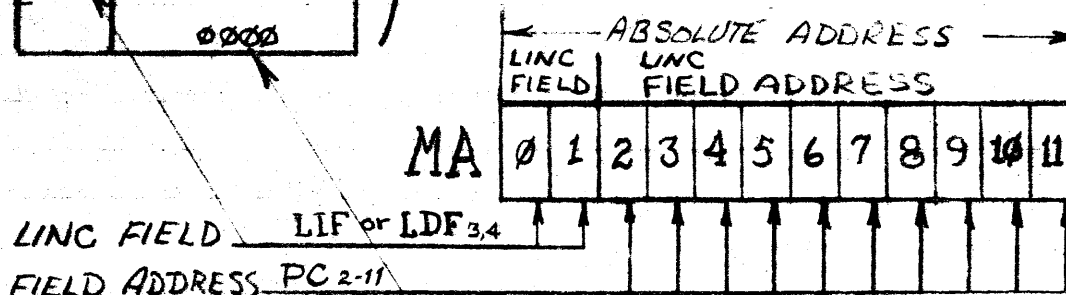
-24-

LINC FIELDS PDP-12

ABSOLUTE ADDRESS ↓	LINC FIELD	LINC FIELD ADDRESS
7777	3	1777
6000 5777	2	0000 1777
4000 3777	1	0000 1777
2000 1777	0	0000 1777
0000		0000

= 4 K MEMORY = 1 of 1 to 8 FIELDS

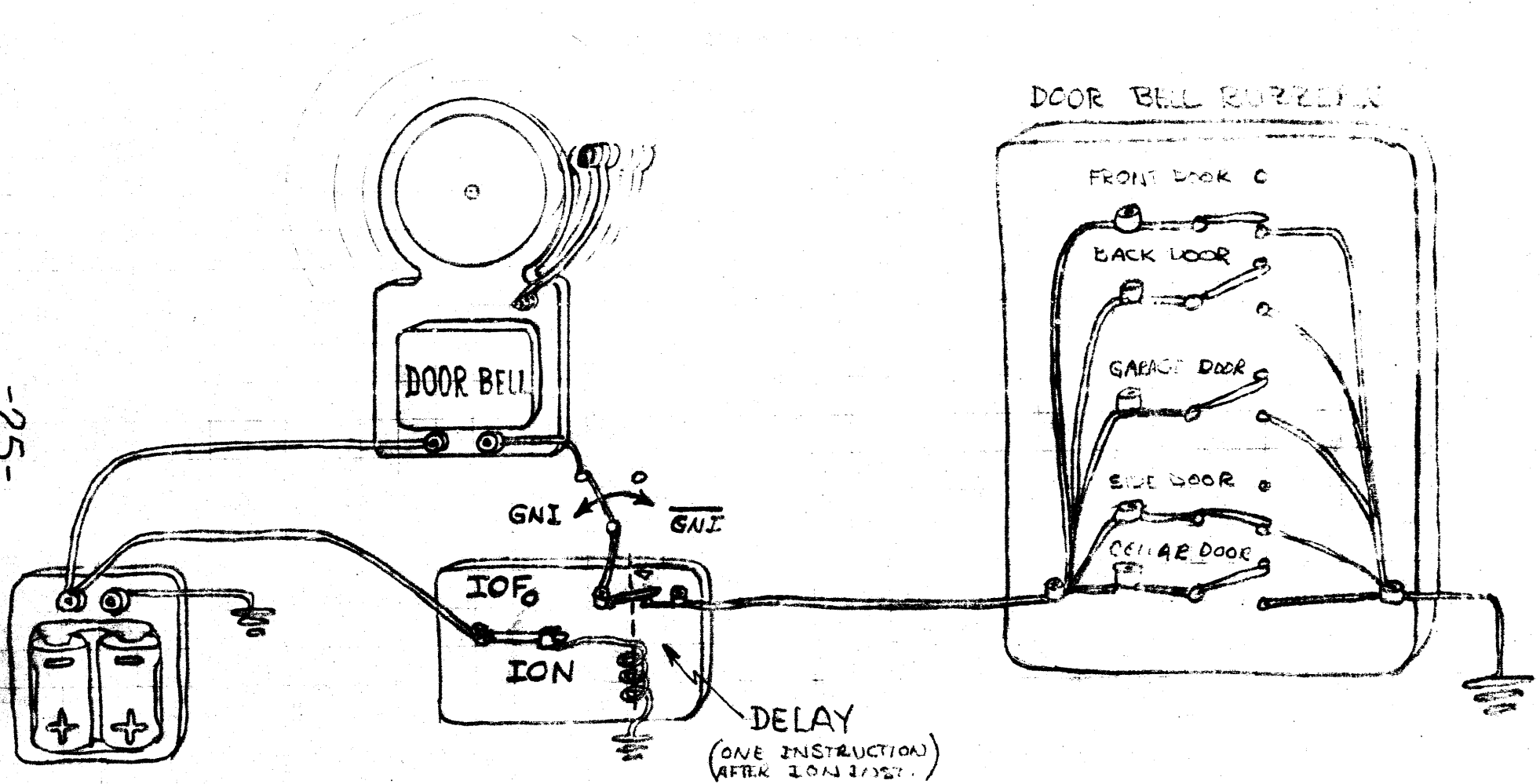
FIELDS	LINC FIELDS
7	37 34
6	33 30
5	27 24
4	23 20
3	17 14
2	13 10
1	7 4
BASIC 4K 0	3 0
IF 0 1 2	34
DF 0 1 2	34



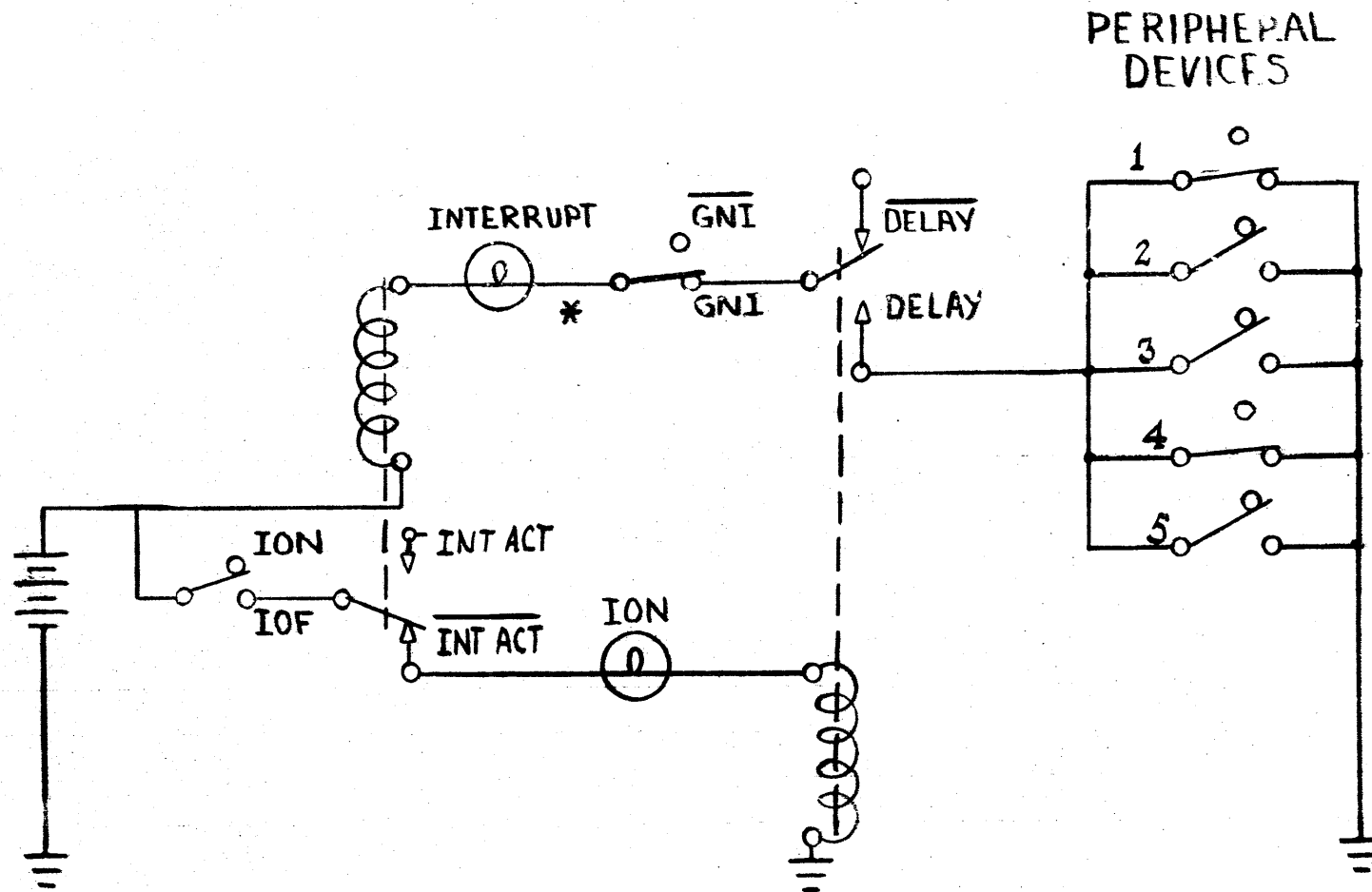
AD

INTERRUPT CONCEPT

-25-



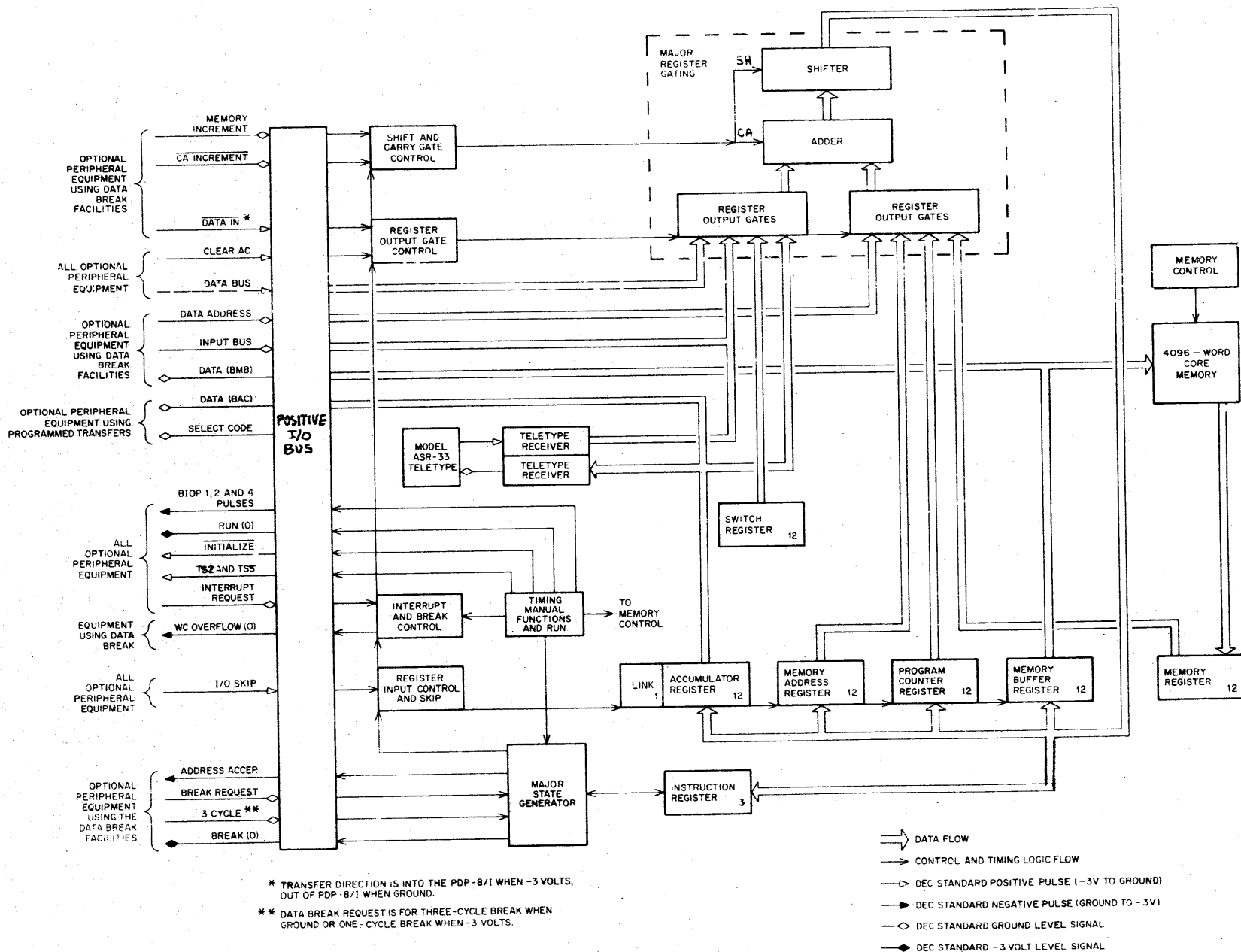
INTERRUPT CHAIN



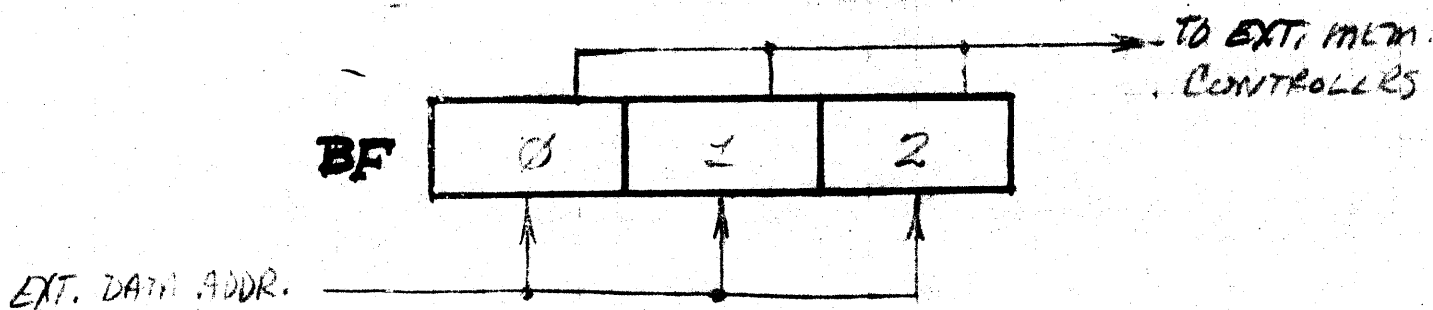
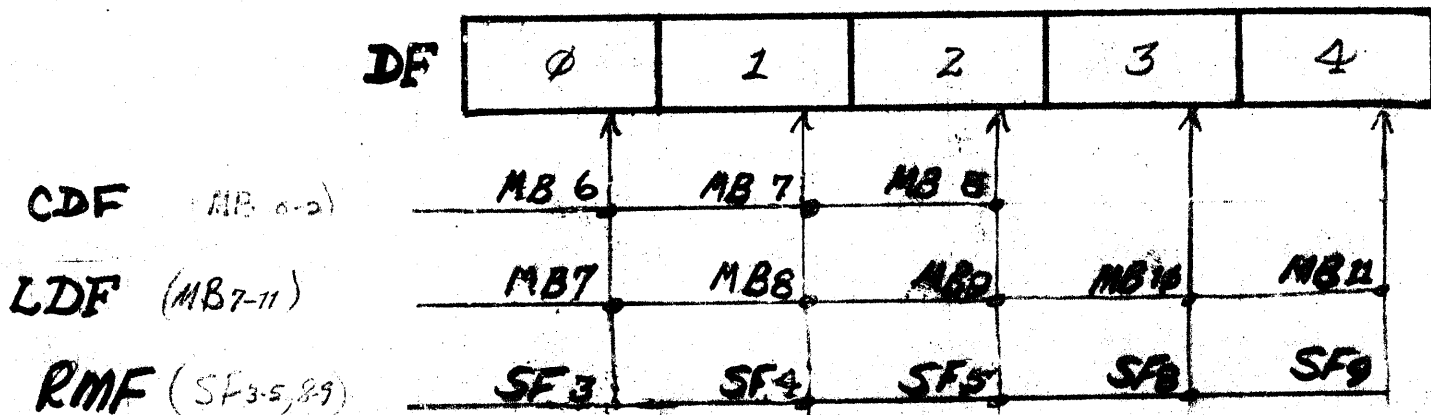
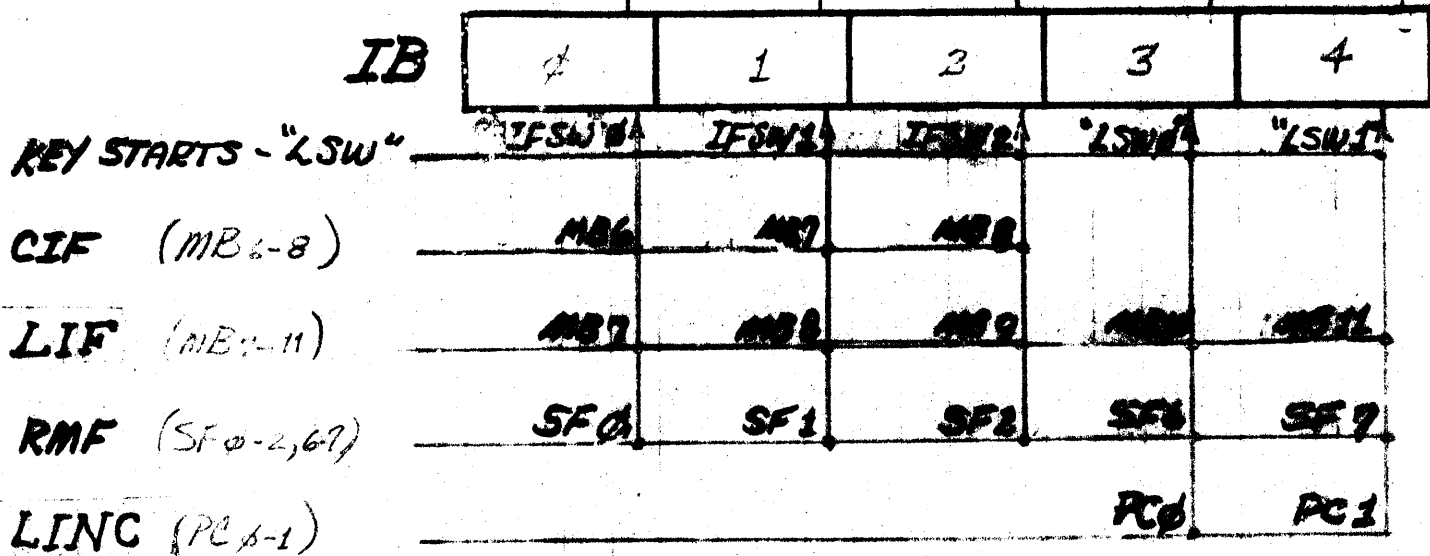
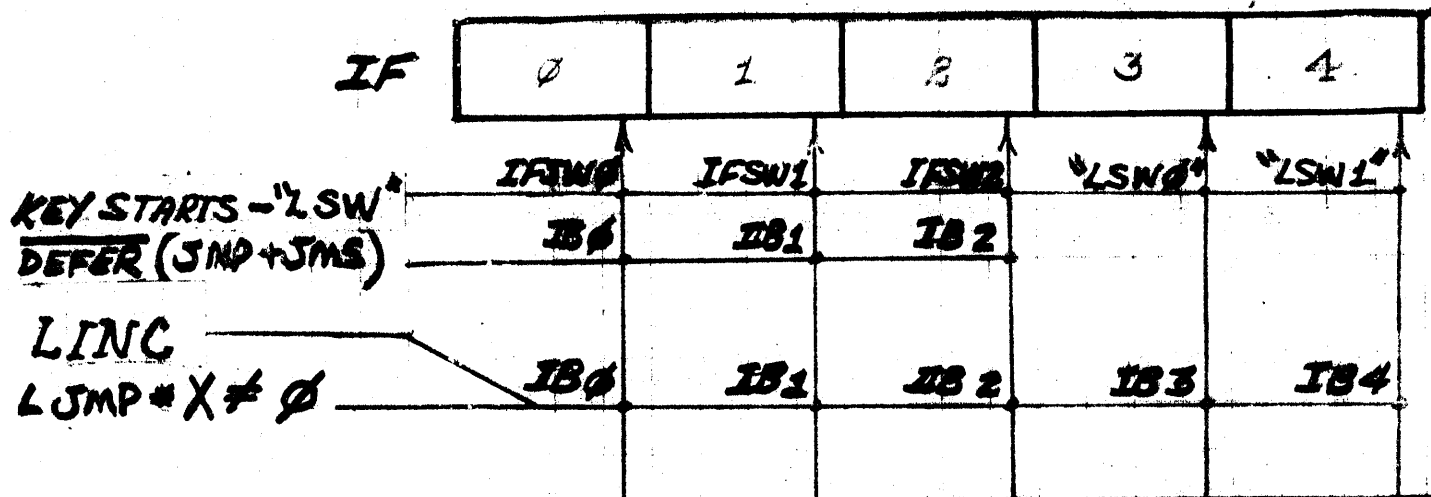
* MODE CHANGE (PDP + LINC) OR INTERRUPT INHIBIT WILL INHIBIT INTERRUPT ACKNOWLEDGE

Handwritten signature

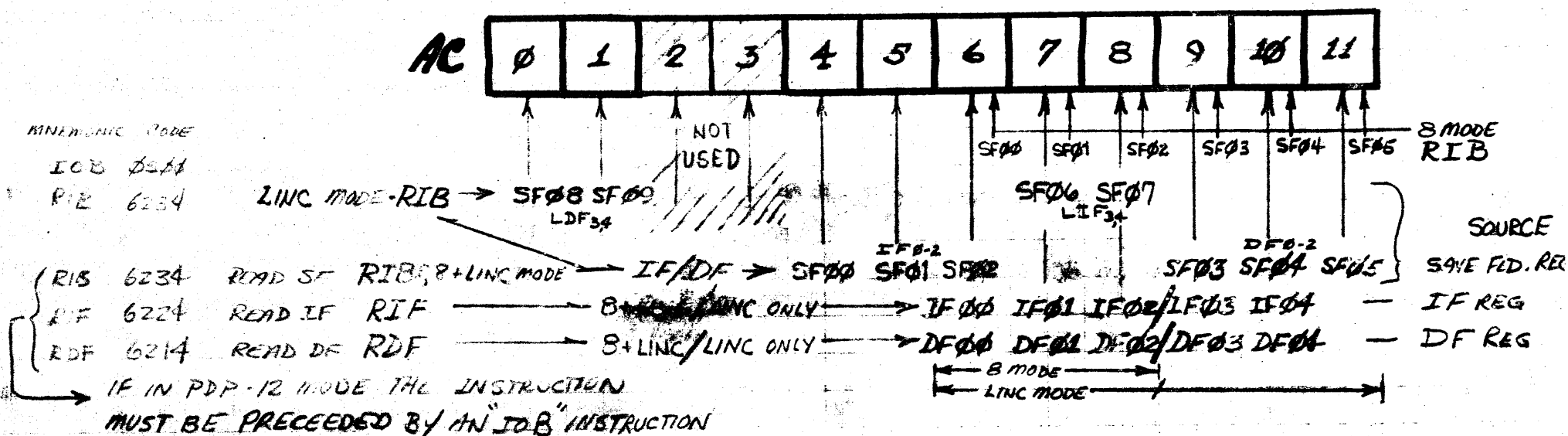
-27-



INTERFACE DIAGRAM

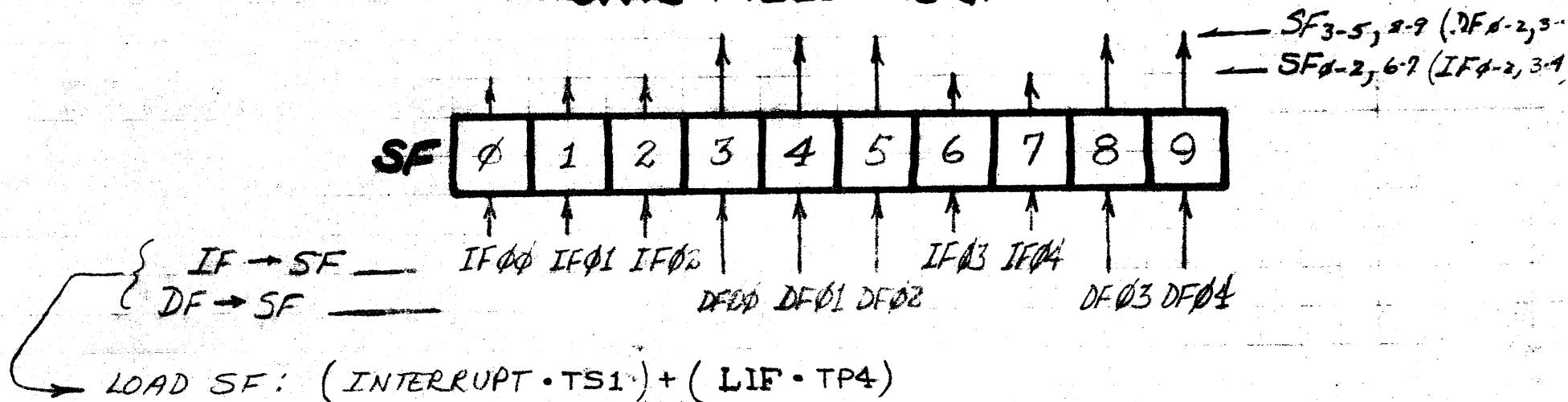


ACCUMULATOR REG.

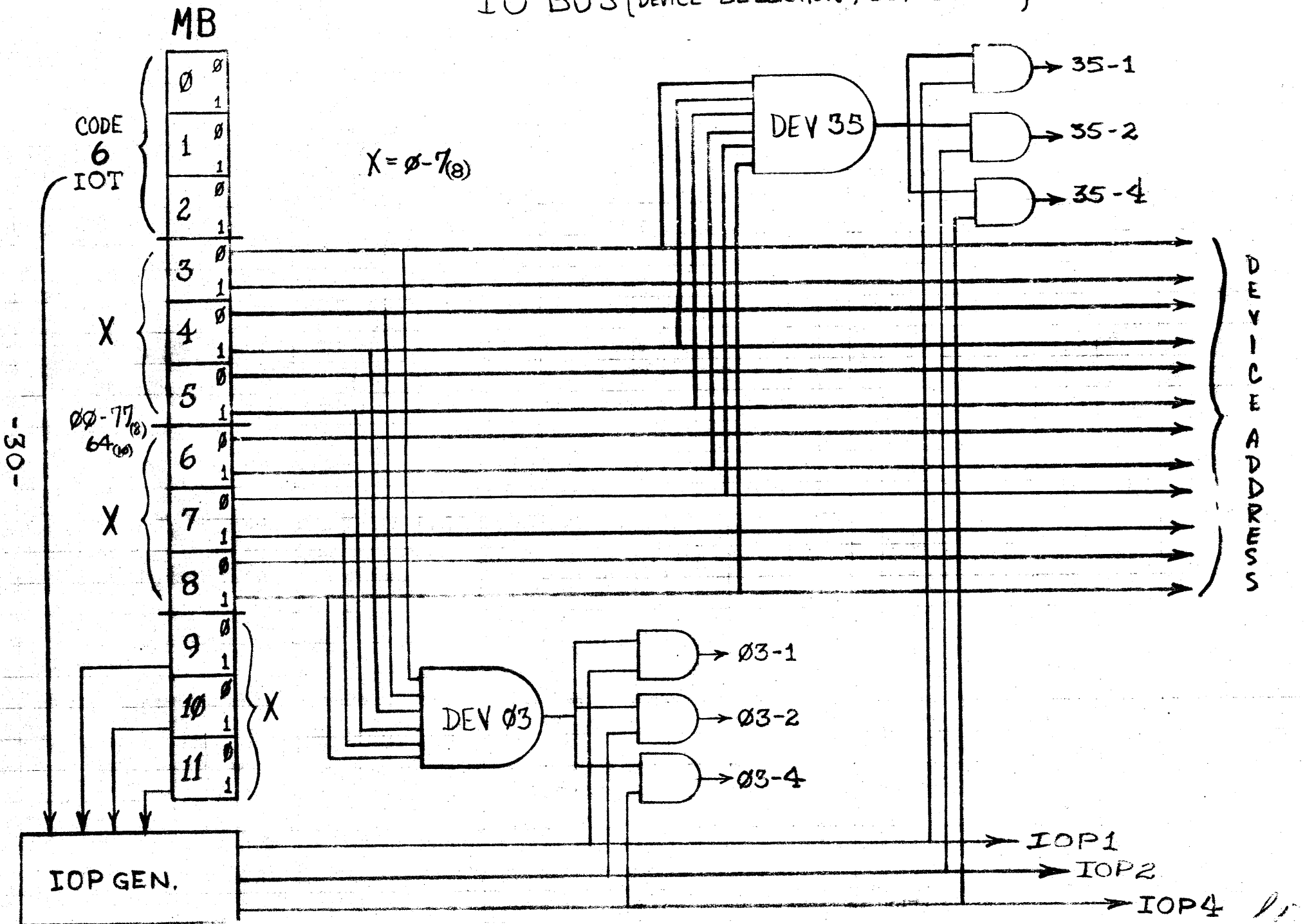


DRAWING SEQUENCE = MEA (INT IO BUS) $\rightarrow$ IOA (IO BUS) $\rightarrow$ PMA (B MSC) $\rightarrow$ PRA (PROC. REGS)

SAVE FIELD REG.

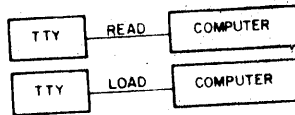


IO BUS (DEVICE SELECTION & IOP GATING)



TTY DISTRIBUTOR

603X = KEYBOARD READER



604X = TELEPRINTER PUNCH

CHARACTERISTICS:
 603X } X-IOP 1 (SKIP) + IOP 2 (CLEAR) + IOP 4 (TRANSFER to READ/LOAD)
 604X }

DISTRIBUTOR REVOLUTION = 100ms

1 CHARACTER / 100ms

10 CHARACTERS / SECOND

600 CHARACTERS / MINUTE ~ 5 CHAR / WORD = 120 WORDS / MIN

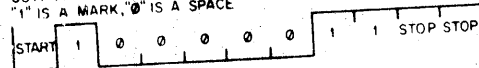
OUTPUT: (ASCII CODE)

1 START BIT - 8 CHARACTER BITS - 2 STOP BITS

@ 909ms / BIT = 99.99ms

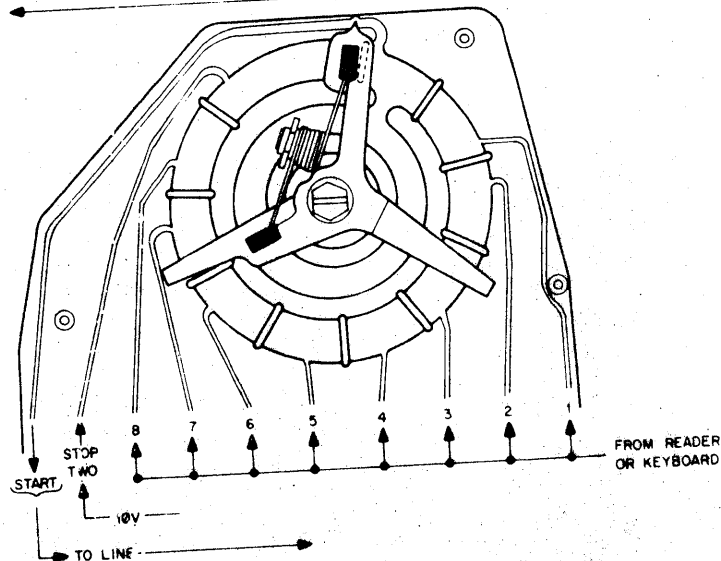
OUTPUT IS TO "LINE" & THE 1st BIT TRANSMITTED IS "START"

"1" IS A MARK, "0" IS A SPACE

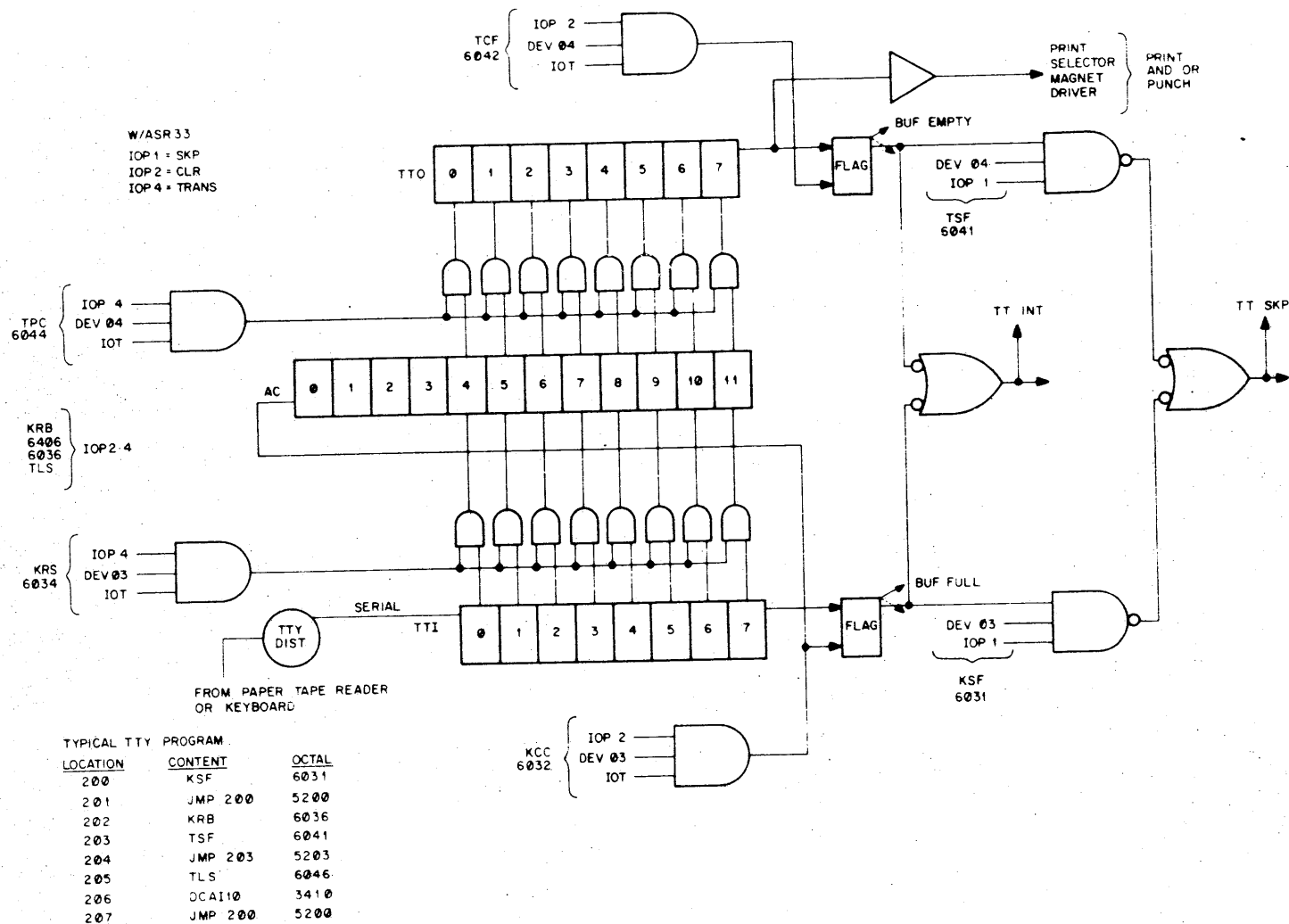


A = 301 (ASCII CHARACTER)

SERIAL INPUT
TO BUFFER TTI

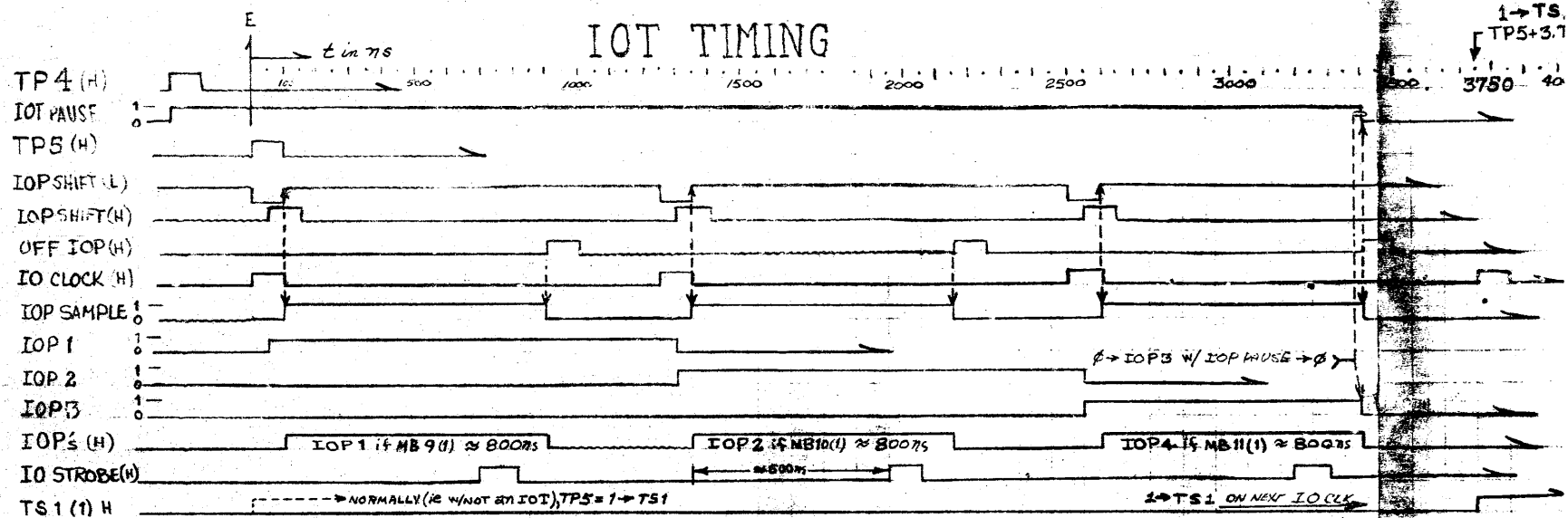


TTY BLOCK DIAGRAM



-32-

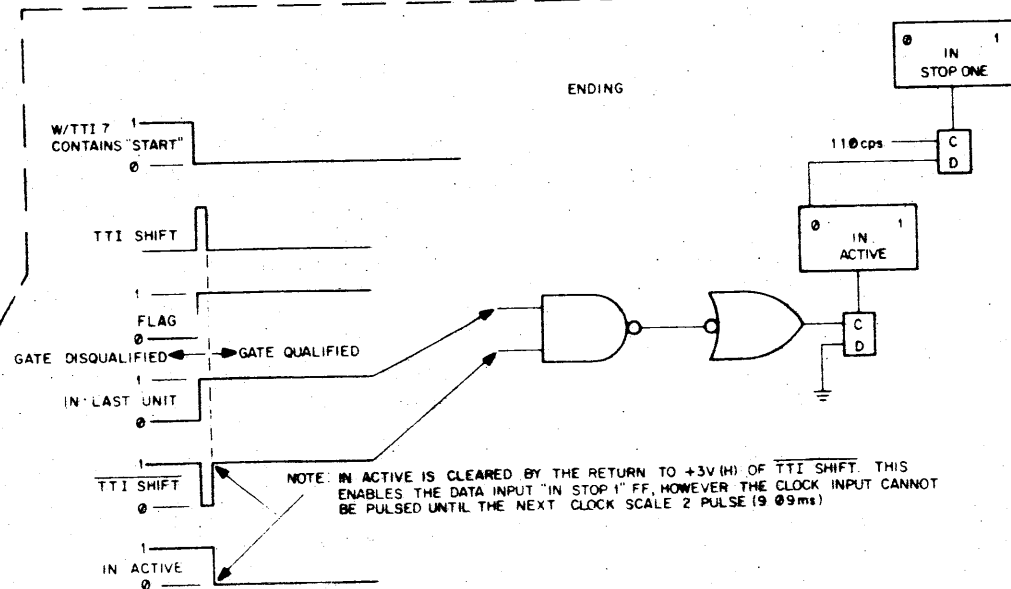
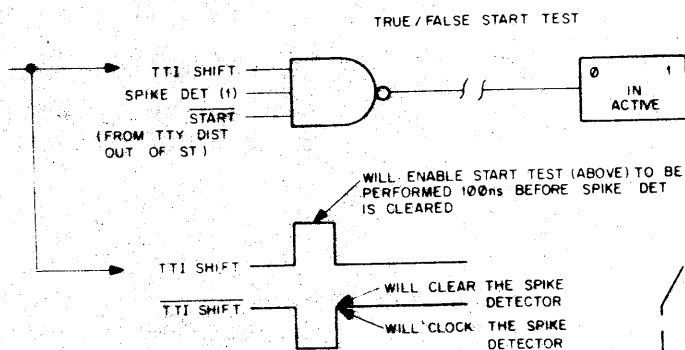
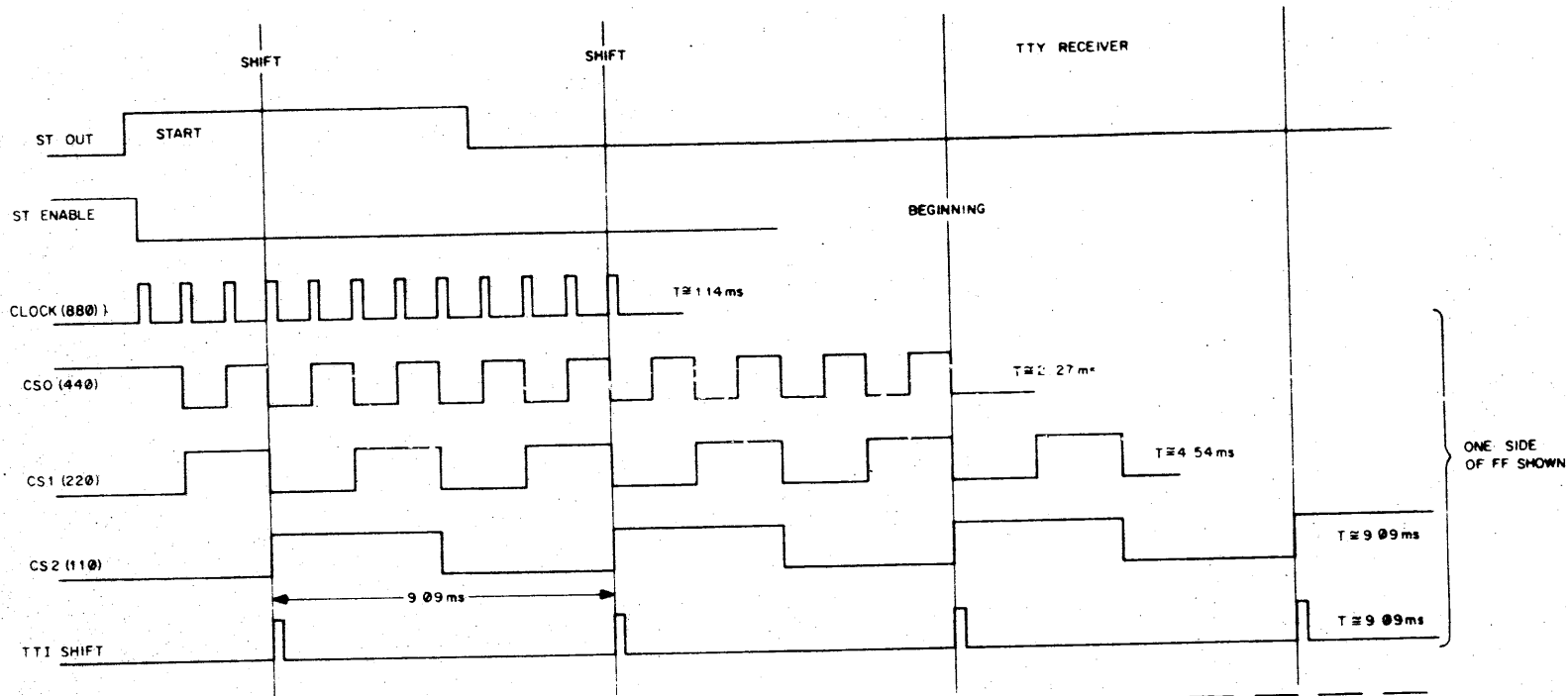
112



33-

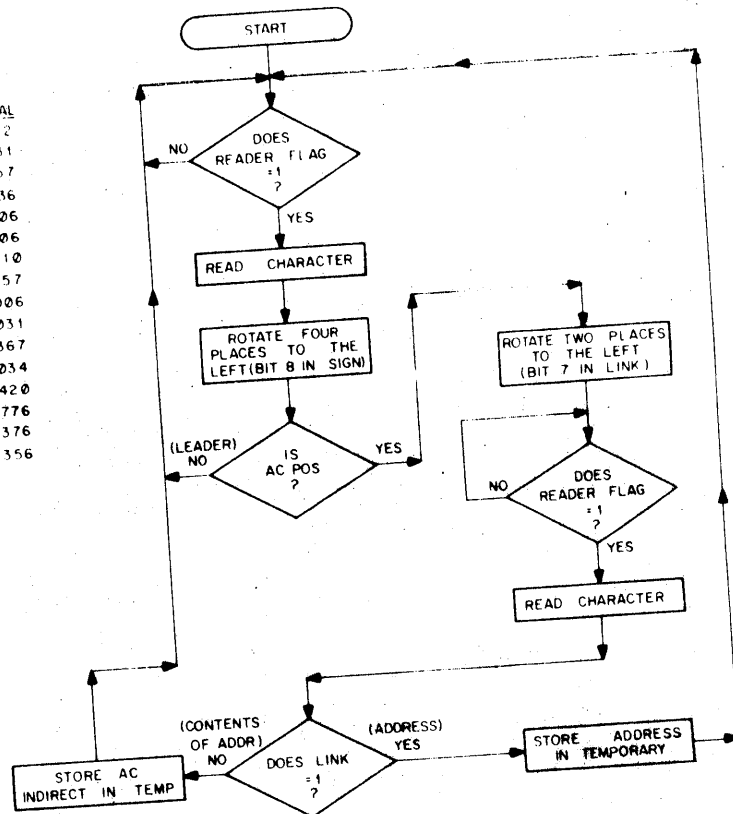
L. L. L.

TTY CONTROL LOGIC

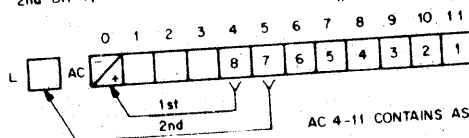


RIM

LOCATION	CONTENT	OCTAL
7756	KCC	6032
7757	KSF	6031
7760	JMP 7757	5357
7761	KRB	6036
7762	CLL, RTL	7106
7763	RTL	7006
7764	SPA	7510
7765	JMP 7757	5357
7766	RTL	7006
7767	KSF	6031
7770	JMP 7767	5367
7771	KRS	6034
7772	SNL	7420
7773	DCAI7776	3776
7774	DCA 7776	3376
7775	JMP 7756	5356
7776	0000	



1st BIT 8, SIGN BIT CHECK IS FOR LEADER - TRAILER
 2nd BIT 7, IN LINK CHECK DETERMINE: IF A ONE - ADDRESS
 IF A ZERO - DATA



AC 4-11 CONTAINS ASC II CODED CHARACTER

DATA BREAK

STOP TRANS.

12

12

12

12

1 GEN.

NOT USED FOR 3 CYCLE DATA BREAK

IOPs {

TIMING PULSES {

B

77778

12

12

12

12

RUN

DND-8/T

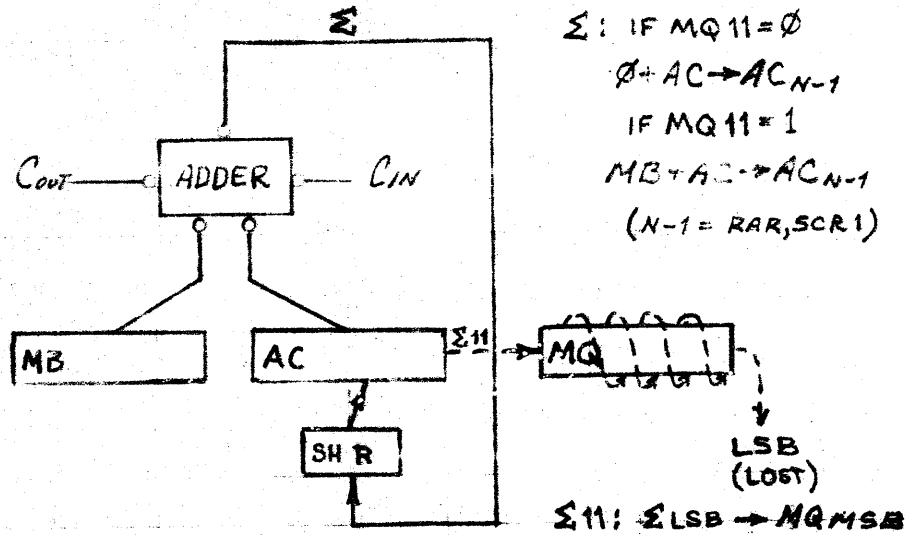
NOTES:

RECEIVED
JAN 10 1968

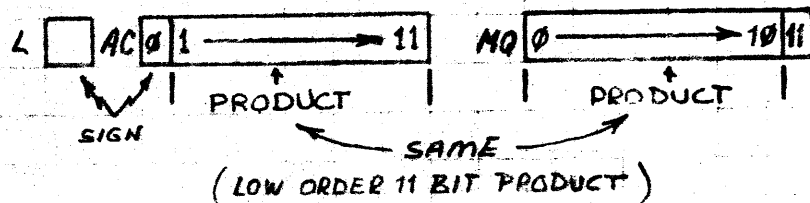
1

MULTIPLY FLOW

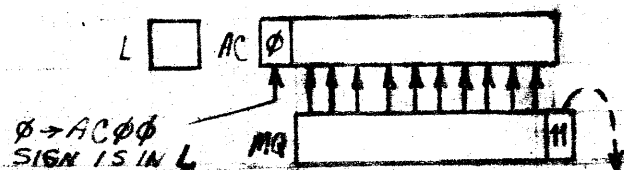
MULTIPLY



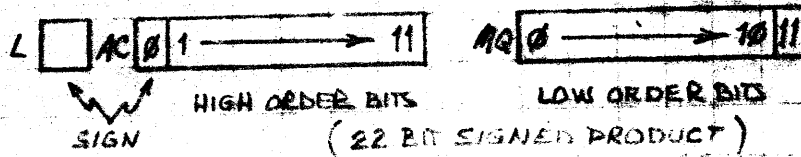
2a

INTEGER MULTIPLY $H=0$ 

MQ → AC, LSB TRANSFER



2b

FRACTIONAL MULTIPLY $H=1$ 

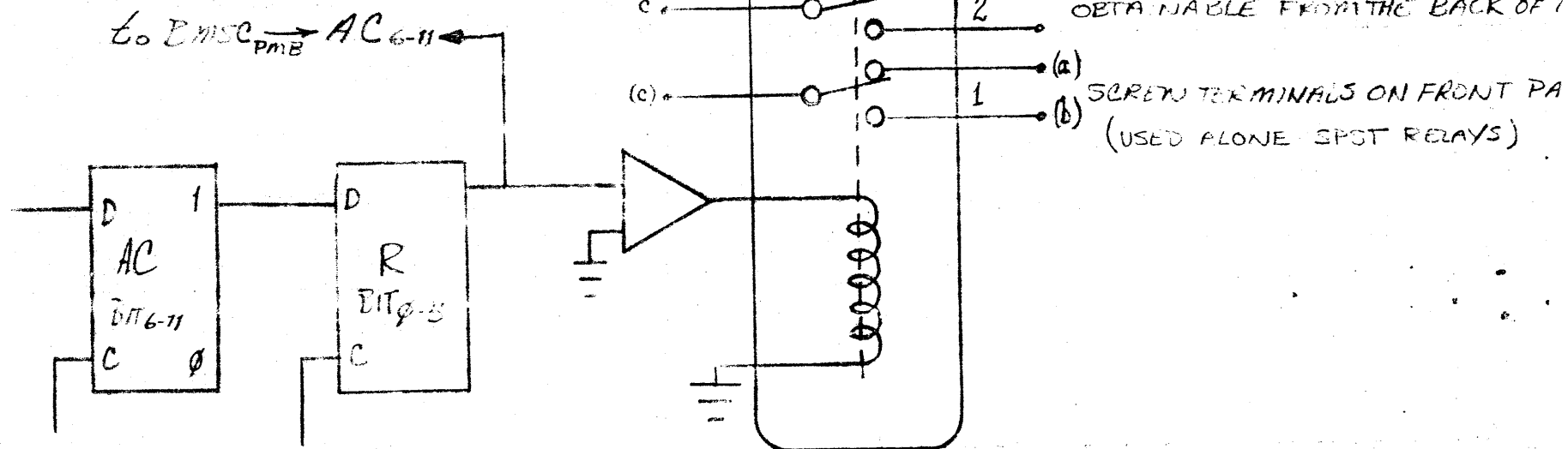
3.

PROBLEM: $23 \times 15_{(8)} = 0367_{(8)}$

MULTIPLICAND MB	AC	MULTIPLIER MQ	TESTED BIT TO DETERMINE NEXT TYPE OF ADD-SEE ①
001 101	000 000	010 01 1	
	001 101		ADD - MB+AC→AC
	000 110	101 00 1	SHIFT
	010 011		ADD - MB+AC→AC
	001 001	110 10 0	SHIFT
	001 001		ADD - 0+AC→AC
	000 100	111 01 0	SHIFT
	000 100		ADD - 0+AC→AC
	000 010	011 10 1	SHIFT
	001 111		ADD - MB+AC→AC
	000 111	101 11 0	SHIFT
	000 111		ADD - 0+AC→AC
001 101	000 011	110 11 1	SHIFT
	0 3	6 7 (8)	
	MSH	LSH	

R. J. Jones

RELAYS



AC bit	RELAY
6	0
7	1
8	2
9	3
10	4
11	5
RIA	ATR

(a)	(c) COMMON	(b)
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○
○	○	○

SCREEN TERMINALS

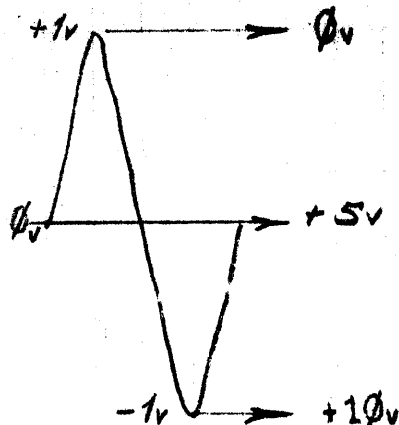
A 214
PRE AMP
INPUT

A 404
SAMPLE & HOLD
OUTPUT

A-D CONVERTER

CONVERTER

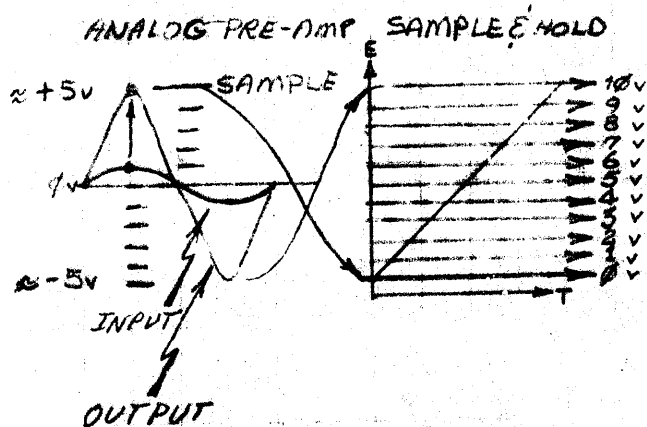
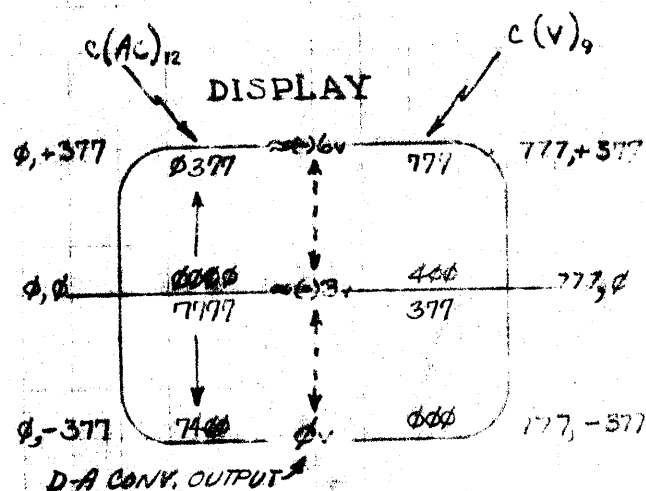
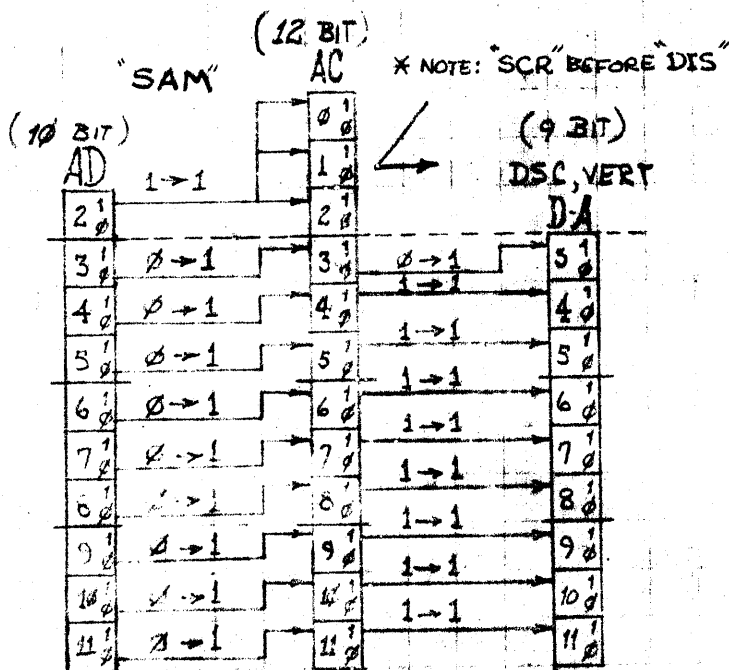
TRANSFER



2^9	5v
2^8	2.5v
2^7	1.25v
2^6	0.625v
2^5	0.3125v
2^4	0.15625v
2^3	0.078125v
2^2	0.0390625v
2^1	0.01953125v
2^0	0.009765625v

YAD	AD2(1) H	=	1 → AC0	NOT COMPLEMENTS
"	AD3(1) H	=	1 → AC1	
"	AD4(1) H	=	1 → AC2	
"	AD5(1) H	=	0 → AC3	COMPLEMENTS
"	AD6(1) H	=	0 → AC4	
"	AD7(1) H	=	0 → AC5	
"	AD8(1) H	=	0 → AC6	
"	AD9(1) H	=	0 → AC7	
"	AD10(1) H	=	0 → AC8	
"	AD11(1) H	=	0 → AC9	
"	AD12(1) H	=	0 → AC10	
"	AD13(1) H	=	0 → AC11	

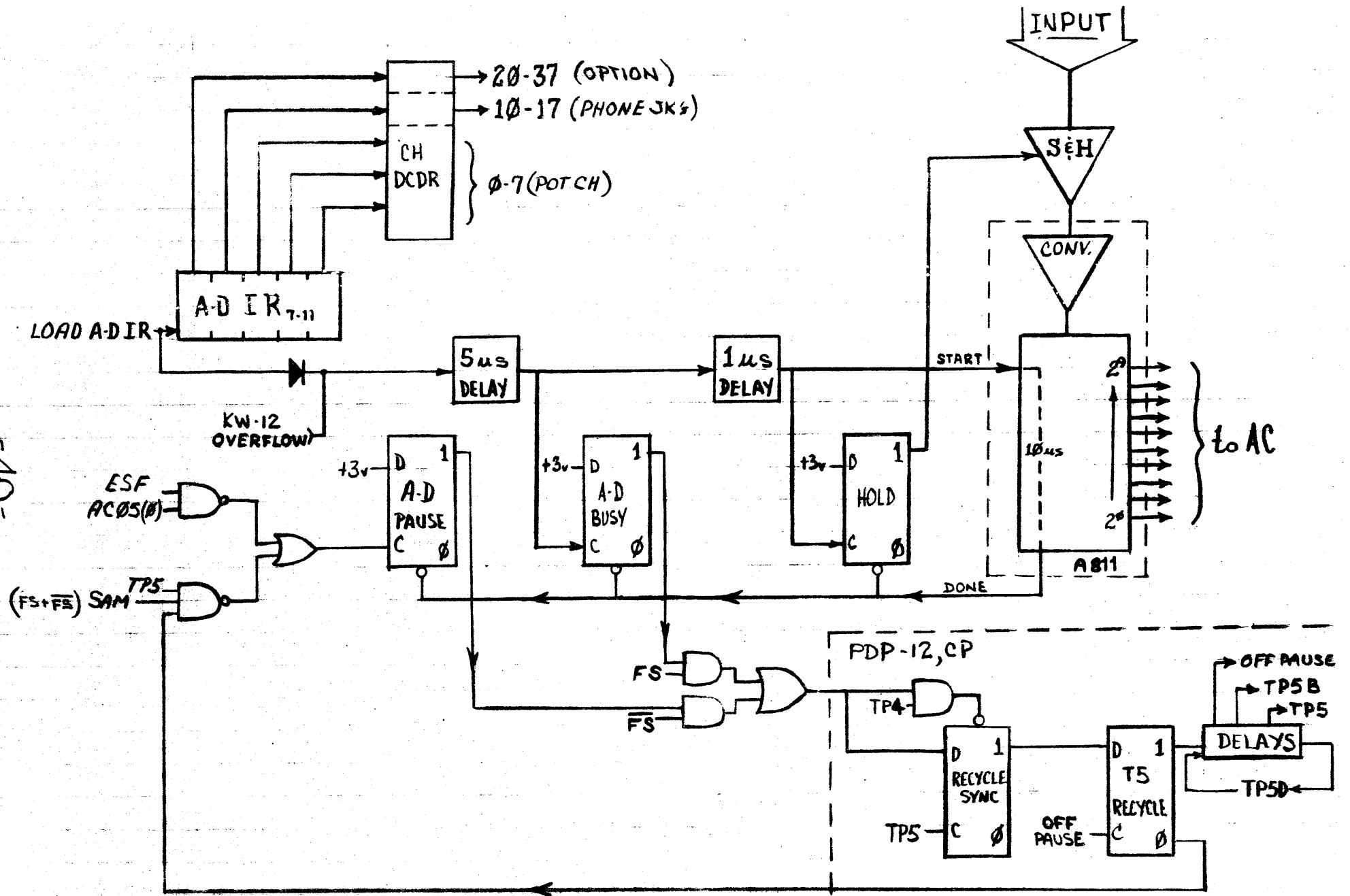
CONVERSION IS ACCOMPLISHED THROUGH SUCCESSIVE APPROXIMATIONS



A-D, DIGITIZING		AC	DSC VERT	D.A	D.A
YAD					
2	0	0	0	5 = 1 = (+)	} ≈ (-) 6v ∴ FULL SCALE DEFLECTION
3	0	0	0	4 = 1	
4	1	1	1	5 = 1	
5	1	1	1	6 = 1	
6	1	1	1	7 = 1	
7	1	1	1	8 = 1	
8	1	1	1	9 = 1	
9	1	1	1	10 = 1	
10	1	1	1	11 = 1	
11	0	0	0	12 = 0	

0777
0377 "SCR"

A-D BLOCK DIAGRAM



SAM

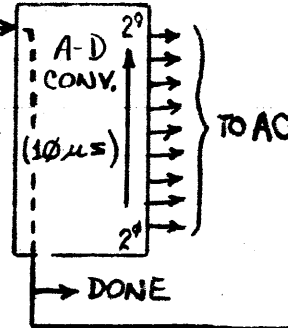
A-D CONTROL

T4

A-D RECYCLE
(FAST SAM-DONE)

A-D RECYCLE
(FAST SAM + DONE)
(BUSY)

START



A-D¹ HOLD 0

A-D¹ BUSY 0

A-D¹ PAUSE 0

FS

$\overline{FS}$

A-D RECYCLE

A-D LOGIC

OFF PAUSE

1 → TS RECYCLE

0 → TS RECYCLE

TS RECYCLE

(0) $\rightarrow$ ESF-ACS(0)

(1) $\rightarrow$ 1 → A-D PAUSE

RECYCLE TS UNTIL A-D CONVERSION IS "DONE"

0 → RECYCLE SYNC

1 → A-D PAUSE

TP5

A-D BUF → AC(XS0, MAX)

FS

$\overline{FS}$

TP5D

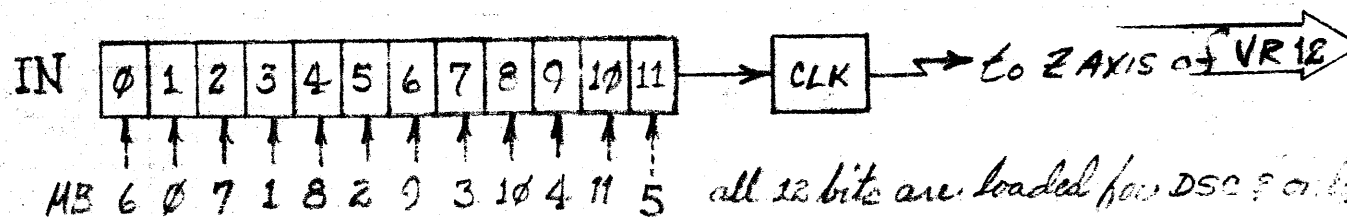
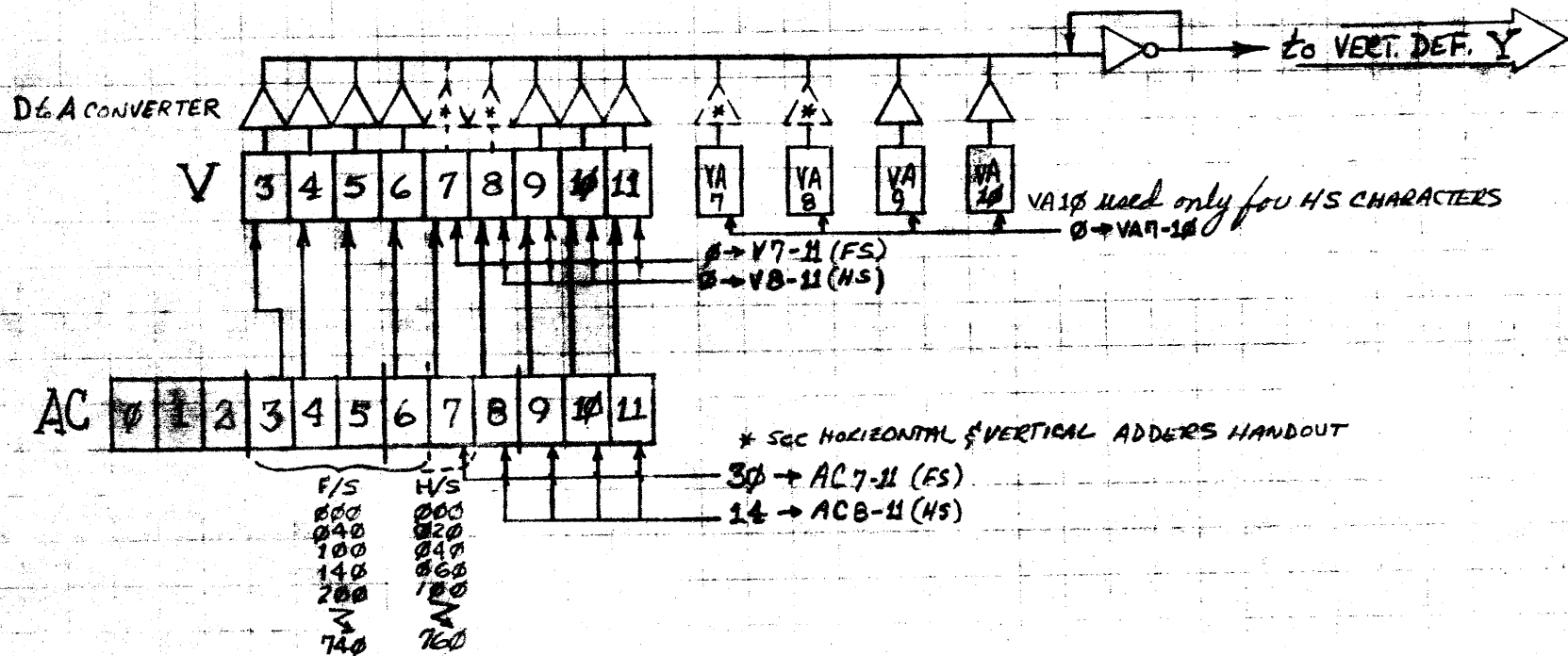
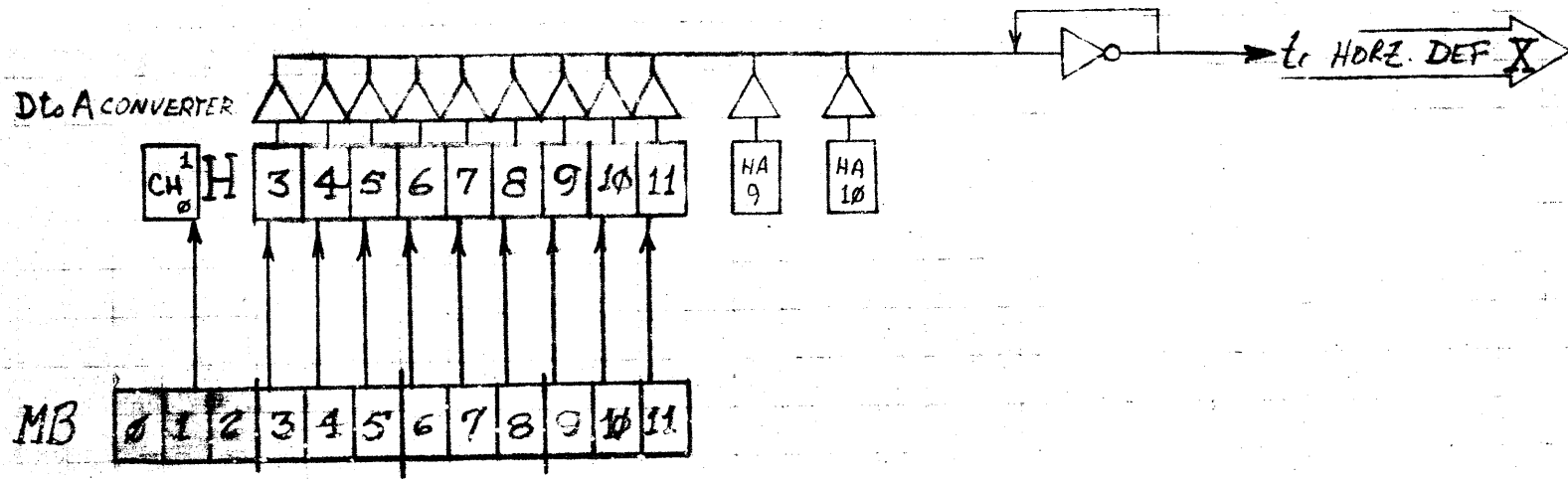
LOAD A-D IR

LOAD A-D IR

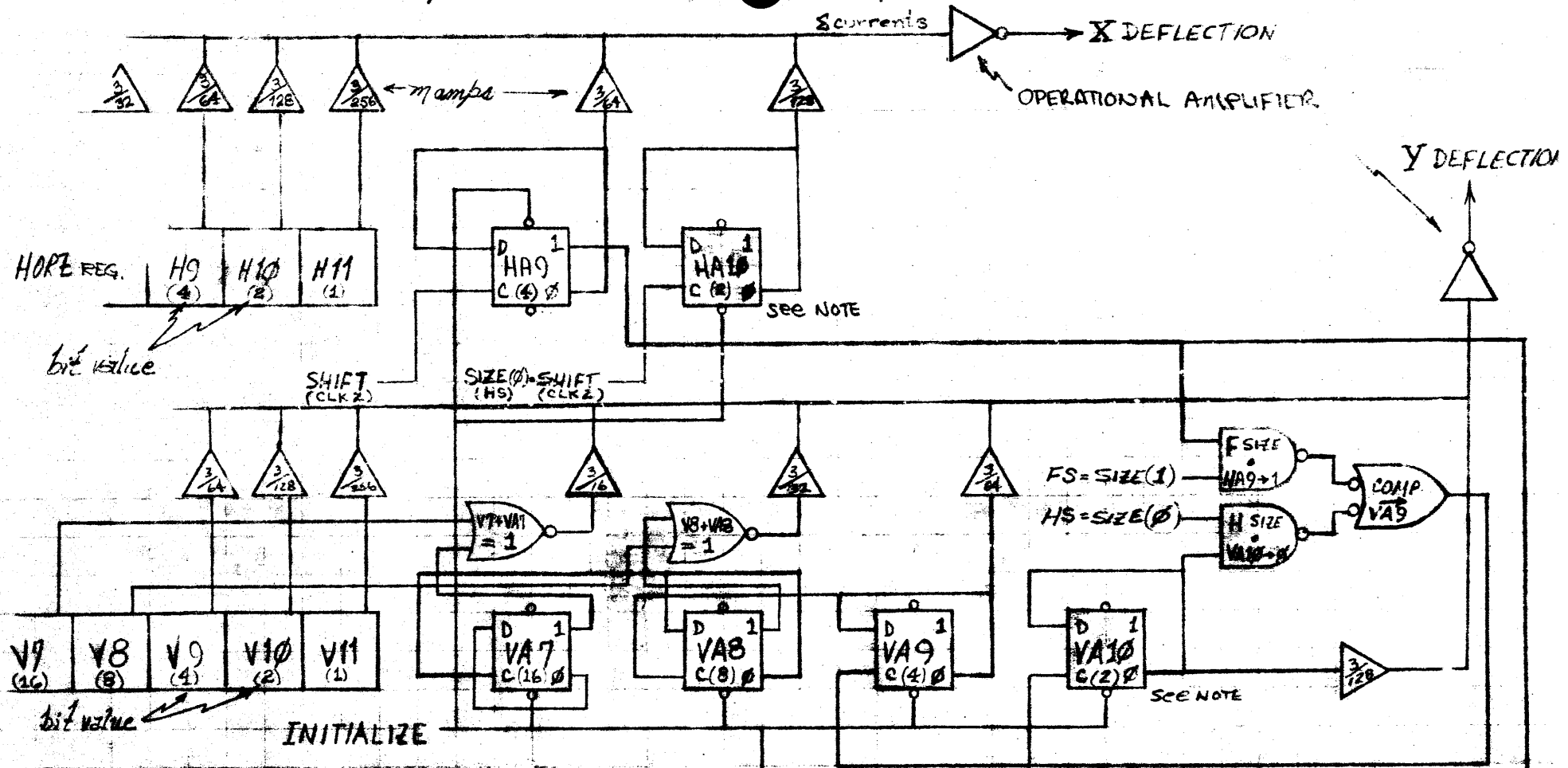
FETCH

ke

42.



D/A HORIZONTAL & VERTICAL ADDERS



FULL SIZE

HALF SIZE

VA	7 ₁₆	8 ₈	9 ₄	10 ₂	HA	9 ₄	10 ₂
(0)	0	0	0	0	1 ₄	0	
(0)	0	0	0	0	0	0	
(4)	0	0	1 ₄	0	1 ₄	0	
(4)	0	0	1 ₄	0	0	0	
(8)	0	1 ₈	0	0	1 ₄	0	
(8)	0	1 ₈	0	0	0	0	
(12)	0	1 ₈	1 ₄	0	1 ₄	0	
(12)	0	1 ₈	1 ₄	0	0	0	
(16)	1 ₁₆	0	0	0	1 ₄	0	

VA	7 ₁₆	8 ₈	9 ₄	10 ₂	HA	9 ₄	10 ₂
(0)	0	0	0	0	1 ₄	0	
(0)	0	0	0	0	0	1 ₂	
(2)	0	0	0	1 ₂	1 ₄	0	
(2)	0	0	0	1 ₂	0	1 ₂	
(4)	0	0	1 ₄	0	1 ₄	0	
(4)	0	0	1 ₄	0	0	1 ₂	
(6)	0	0	1 ₄	1 ₂	1 ₄	0	
(6)	0	0	1 ₄	1 ₂	0	1 ₂	
(8)	0	1 ₈	0	0	1 ₄	0	

COMPLEMENTS W/VA8 → 0

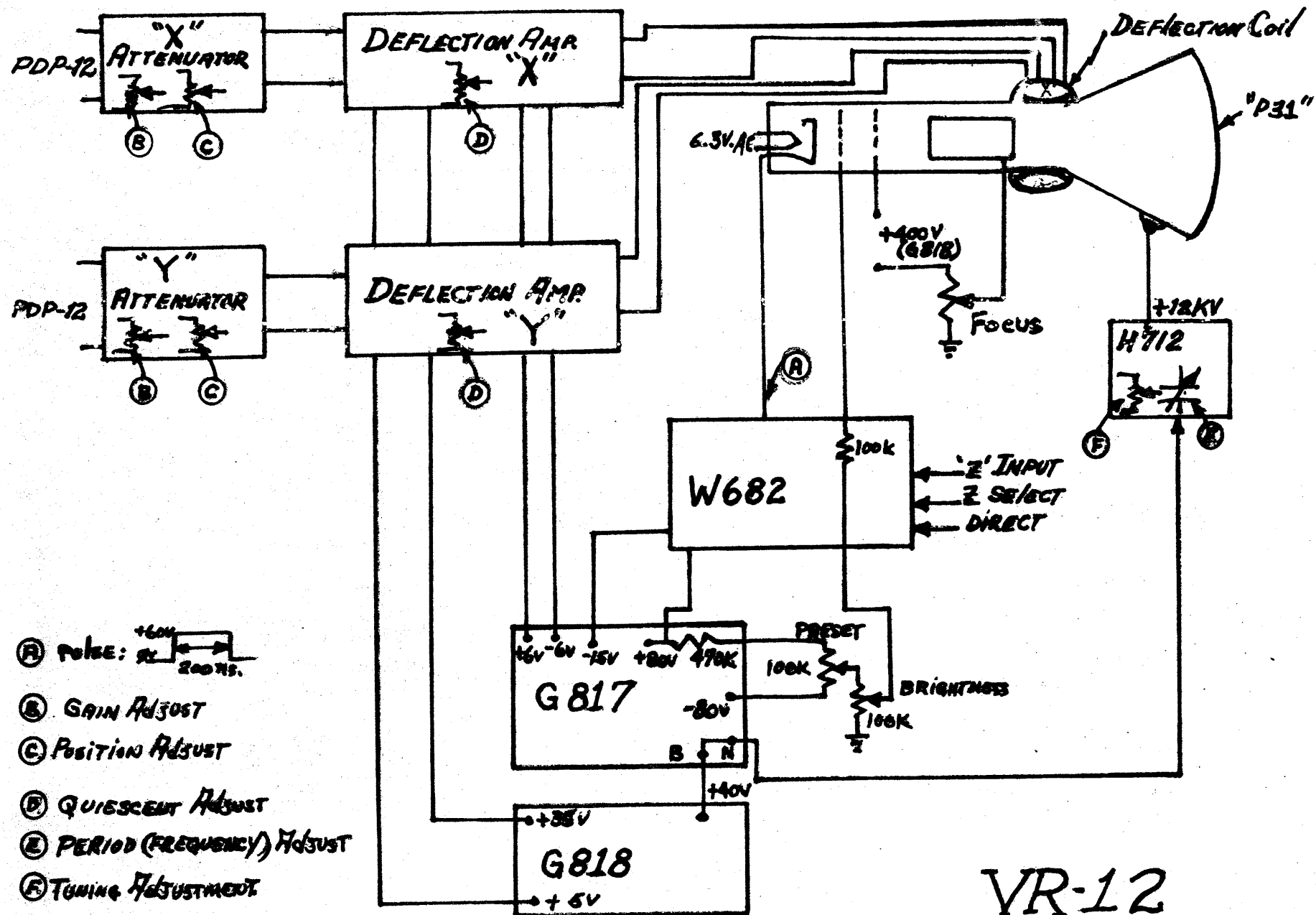
NOTE: VA & HA 10 are only used
(a) ON HALF SIZE character

(b) CLOCK 1 = INTENSIFY
2 = SHIFT

DISPLAY CHARACTER TABLE

0	4136	A	4477	U	0177
	3641		7744		7701
1	2101	B	5177	V	0176
	0177		2651		7402
2	4523	C	4136	W	0677
	2151		2241		7701
3	4122	D	4177	X	1463
	2651		3641		6314
4	2414	E	4577	Y	0770
	0477		4145		7007
5	5172	F	4477	Z	4543
	0651		4044		6151
6	1506	G	4136	=	1212
	4225		2645		1212
7	4443	H	1077	u	0107
	6050		7710		0107
8	5126	I	7741	,	0500
	2651		0041		0006
9	5120	J	4142	.	0001
	3651		4076		0000
EOL	0000	K	1077	≡	4577
	0000		4324		7745
del	0000	L	0177	[	4177
	0000		0301		0000
SPACE	0000	M	3077		
	0000		7730		
i	0101	N	3077		
	0126		7706		
p	3700	O	4177		
	3424		7741		
-	0404	P	4477		
	0404		3044		
+	0404	Q	4276		
	0437		0376		
	0000	R	4477		
	0077		3146		
#	3614	S	5121		
	1436		4651		
CASE	0000	T	4040		
	0000		4077		

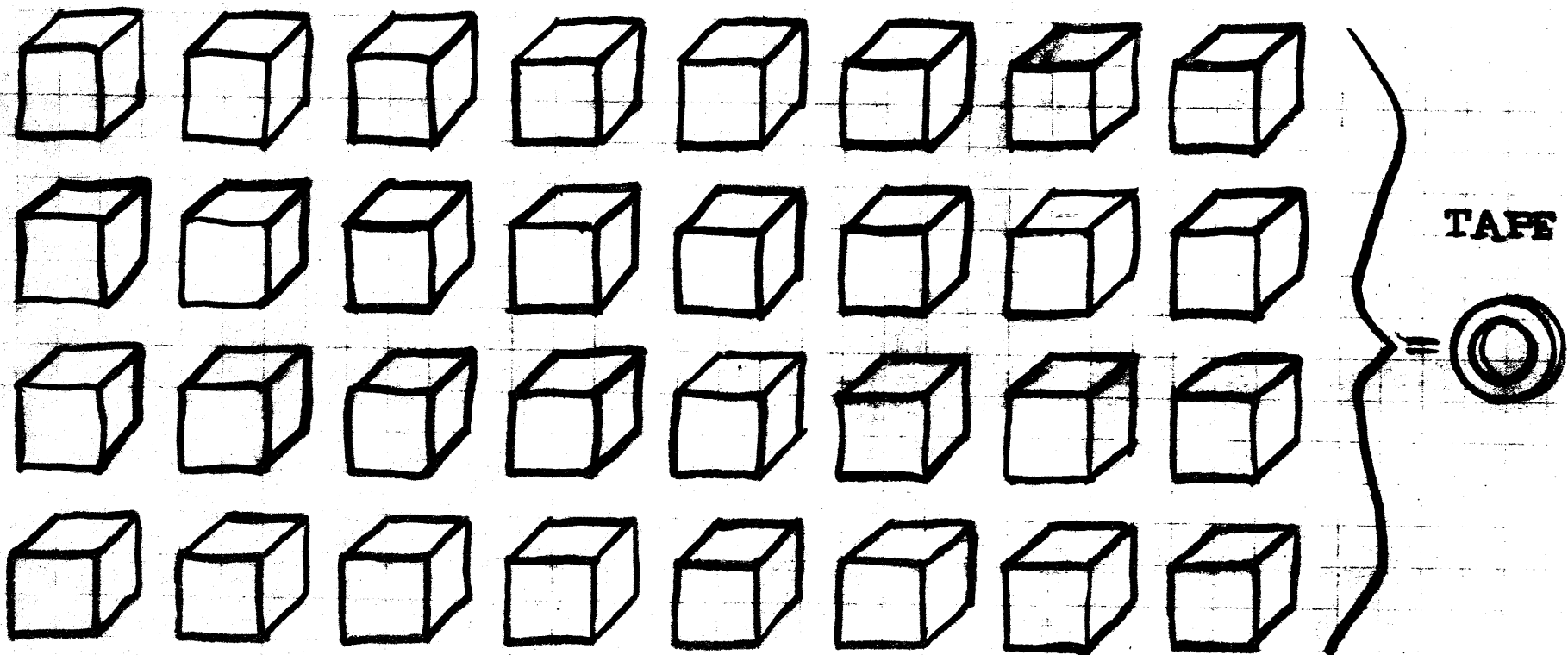
VR-12 BLOCK DIAGRAM



VR-12

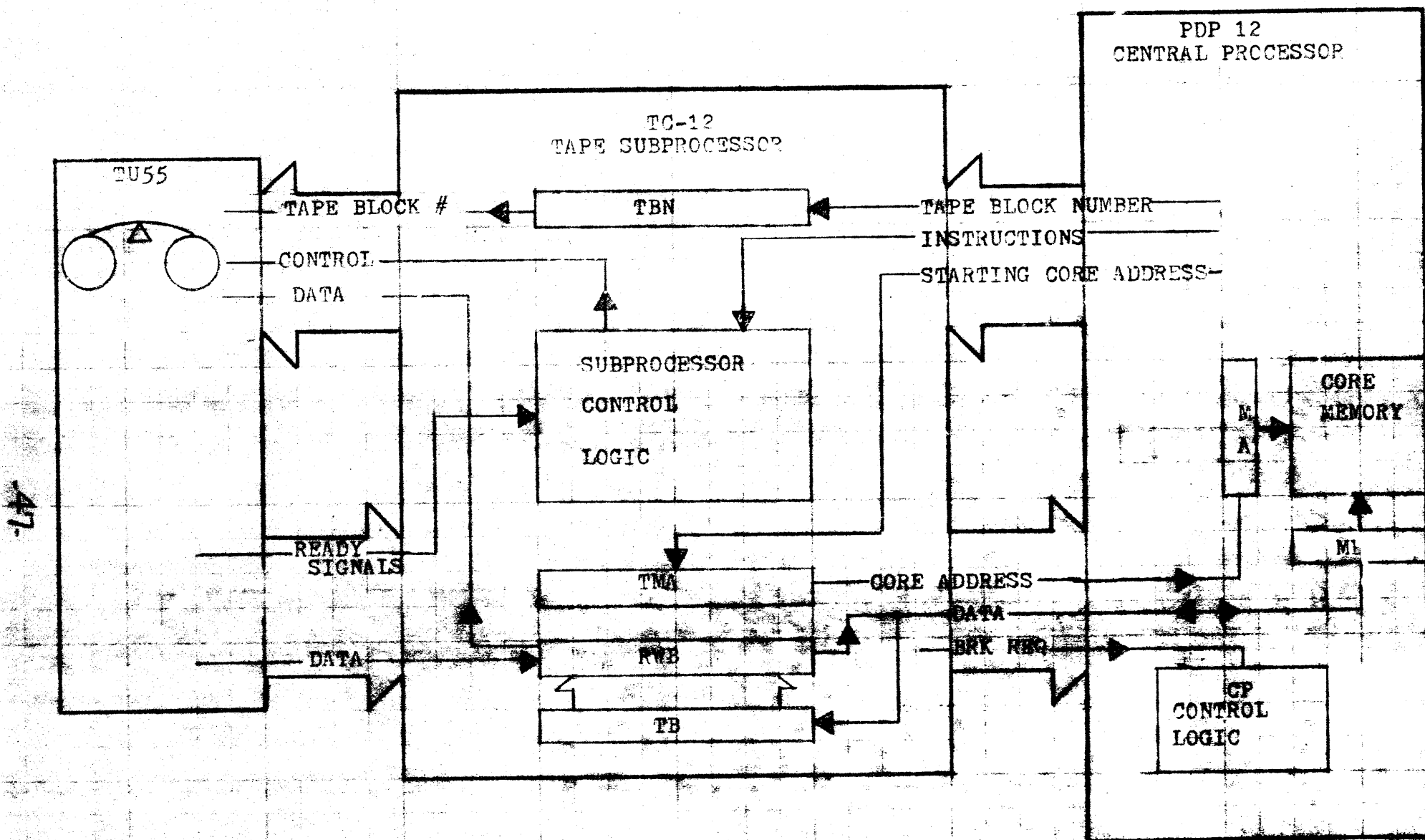
CORE MEMORY STORAGE VRS TAPE STORAGE

32 FOUR K's of MEMORY



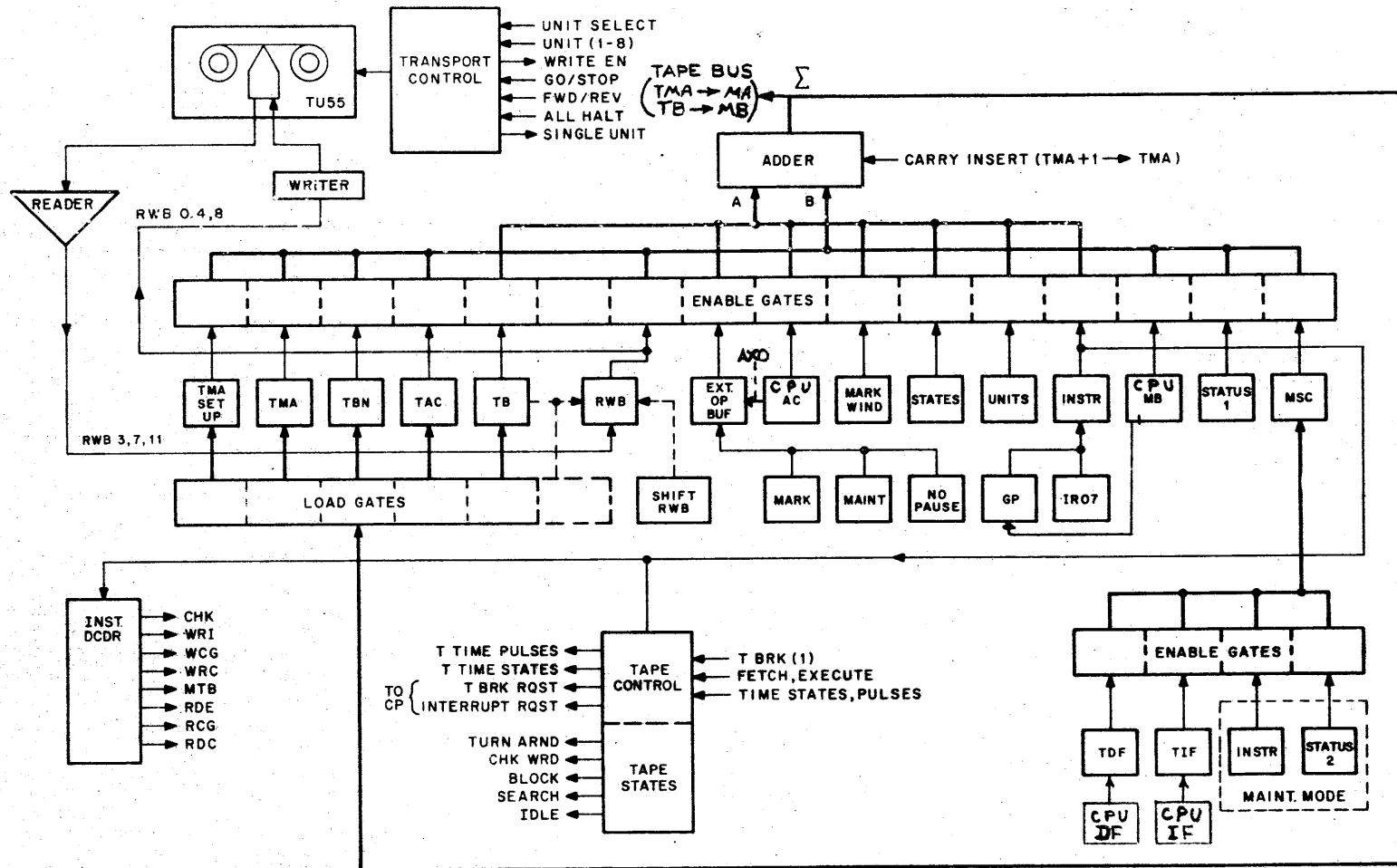
4096 WORDS ~
12 BIT WORDS

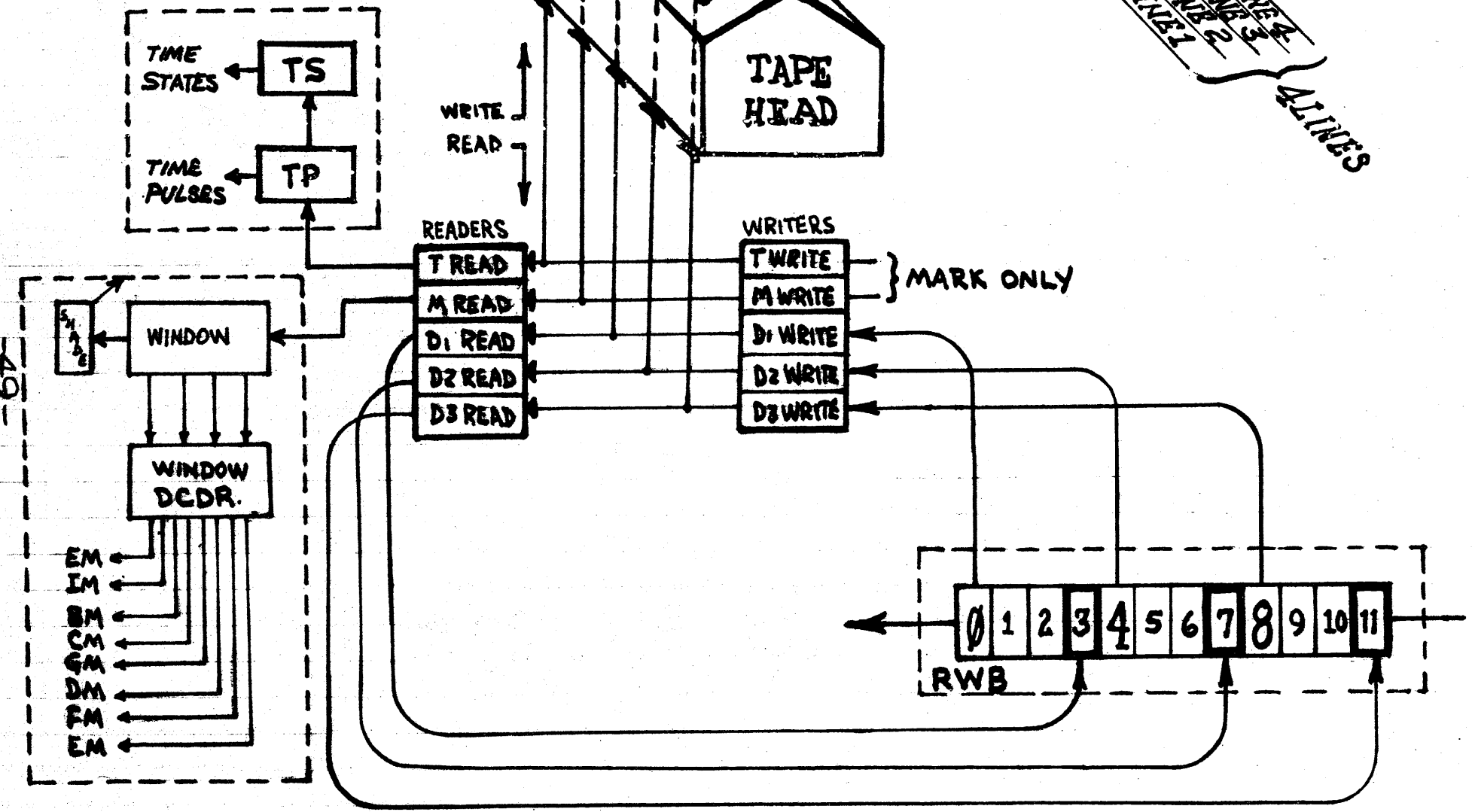
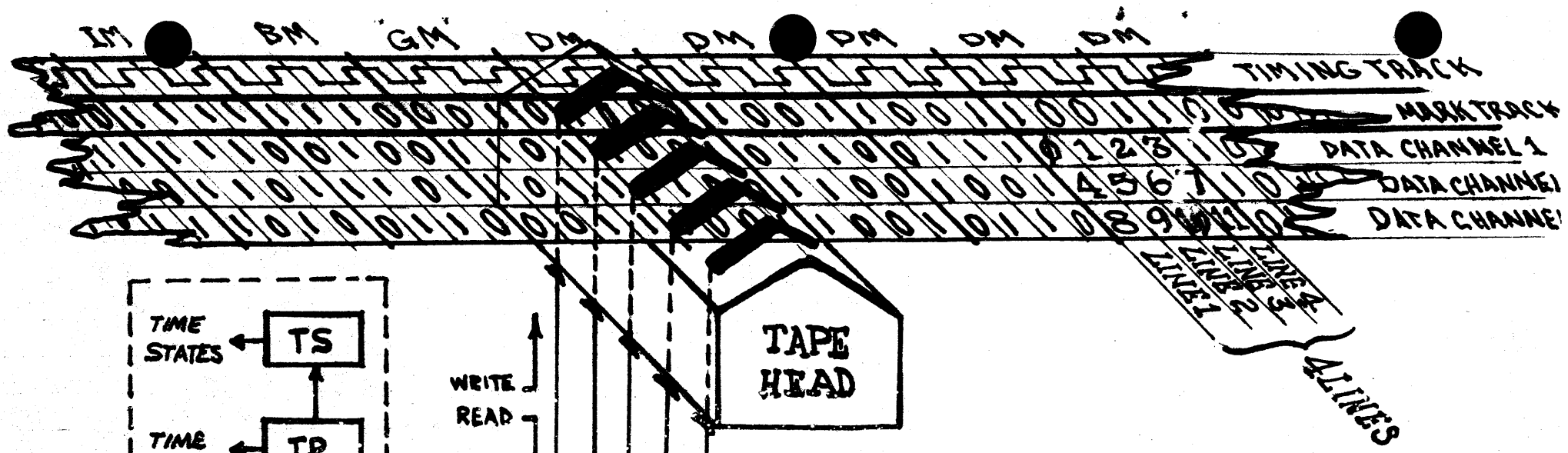
131,072 WORDS
512 BLOCKS
256 WORDS
12 BIT WORDS



LINCTAPE BLOCK DIAGRAM

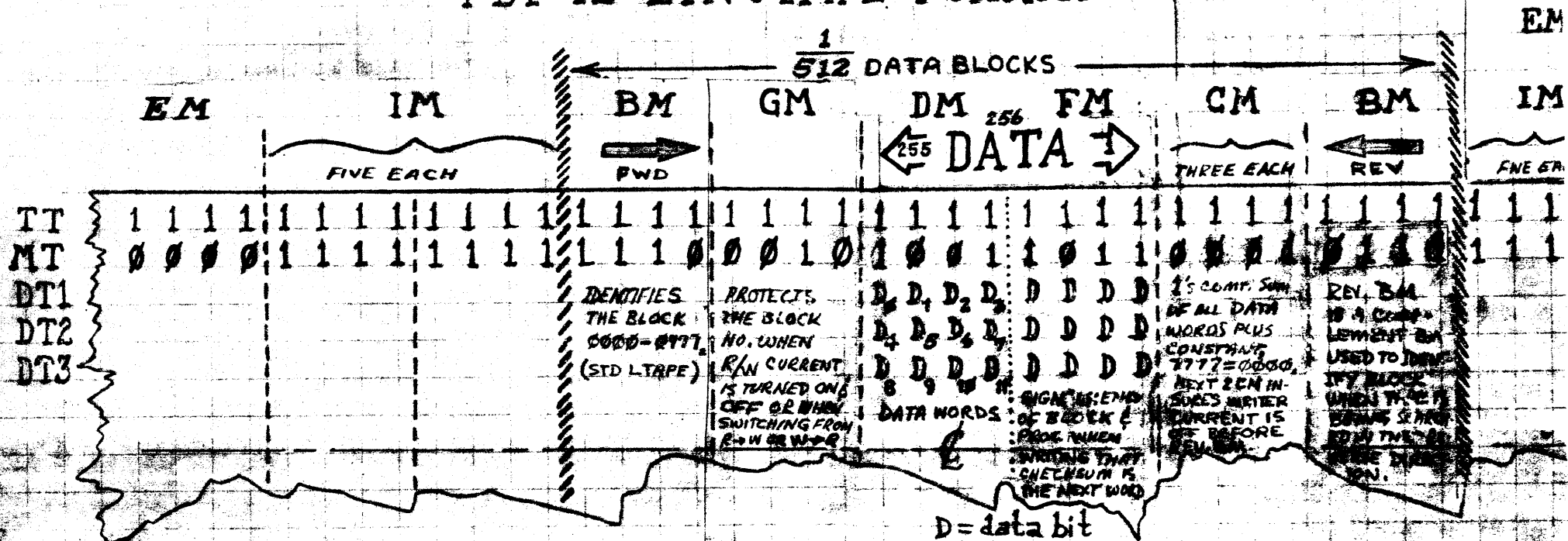
PDP-12 LINC TAPE FLOW DIAGRAM





LINC TAPE

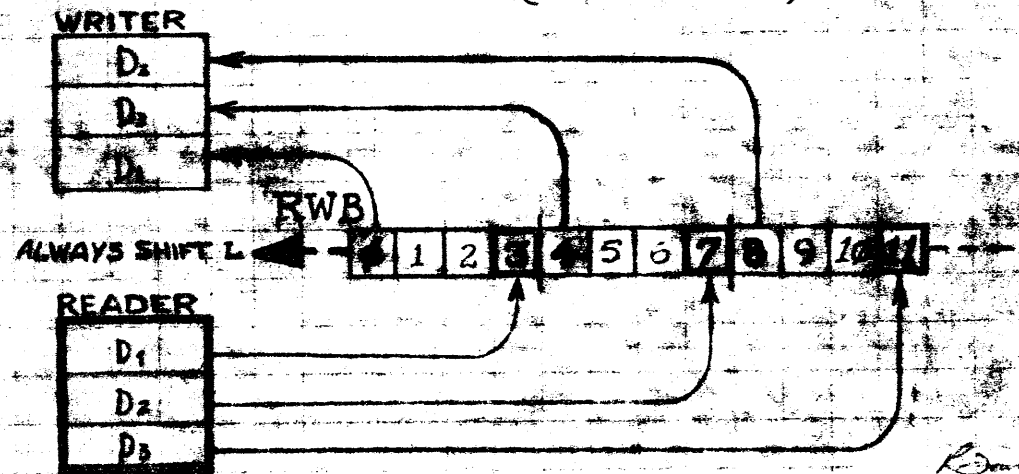
PDP 12 LINCTAPE FORMAT



NOTE:

1. ONLY READ AND WRITE DATA IN THE FOWARD DIRECTION
CAN READ BLOCK NUMBERS IN EITHER DIRECTION (FOWARD OR REVERSE).
2. MARK AND DATA TRACKS ARE WRITTEN AND ARE READ IN BINARY FORM (ie 1 = 0 & 0 = 1) BY PHASE.
THE CHECK SUM IS WRITTEN IN COMPLEMENT FORM (ie 1 = 0 & 0 = 1) BY PHASE.

- (1) BM = BLOCK MARK
- (3) CM = CHECK MARK
- (255) DM = DATA MARK
- EM = END MARK
- (1) FM = FINAL MARK
- (1) GM = GUARD MARK
- (5) IM = INTERBLOCK MARK
- MT = MARK TRACK
- TT = TIMING TRACK



BLOCK MARK

BM - BLOCK MARK = 1110

FORWARD BLOCK MARK

TAPE DIR. $\leftarrow 1, 1, 1, 0$

TAPE HEAD



HEAD DIRECTION

0_4
 1_3
 1_2
 1_1

MARK WINDOW

1_1
 1_2
 1_3
 0_4

HEAD DIRECTION

MARK DCDR

BM

$1, 1, 1, 0$

REVERSE BLOCK MARK

$0, 1, 1, 1 \rightarrow$ TAPE DIR.

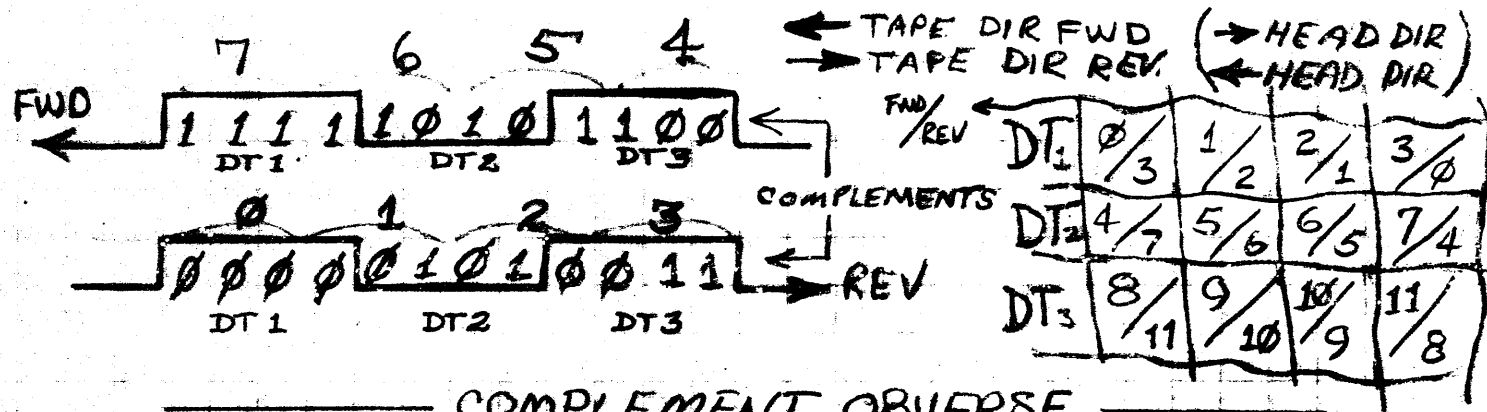
TAPE HEAD

1_4
 0_3
 0_2
 0_1

TO BE ABLE TO READ BM'S IN REV.
THE MARK CODE IS WRITTEN ON
TAPE IN OBLVERSE FORM

AN INVERTER IN THE LINC TAPE CONTROL
CIRCUITS IS USED TO COMPENSATE
FOR THE COMPLEMENTING OF THE
BINARY BITS DUE TO THE REVERSING
OF TAPE DIRECTION.

READING BLOCK MARKS (FWD - REV)



COMPLEMENT OBVERSE

HEAD DIR	BM	HEAD DIR	BM
TT	1 0 1 0 1 0	TT	1 0 1 0 1 0
MT	1 1 1 1 1 1	MT	1 0 0 0 0 0
DT1	0 1 2 3	DT1	3 2 1 0
DT2	1 0 1 0	DT2	0 0 0 0
DT3	1 1 0 0	DT3	1 0 1 0

OBVERSE { IS NOT A COMPLEMENT BUT IS A REVERSE ORDER

COMPLEMENT OBVERSE

NOTE: THE OBVERSE BLOCK NUMBER IS WRITTEN ON TAPE WHEN THE TAPE IS FORMATED

Done

WRITING ON TAPE

bit → 1 2 3



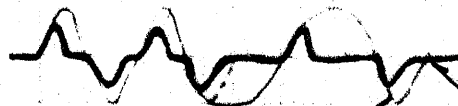
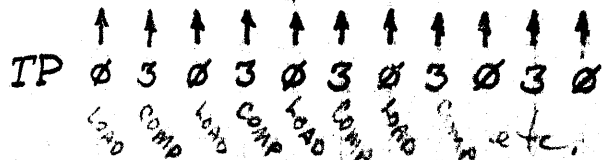
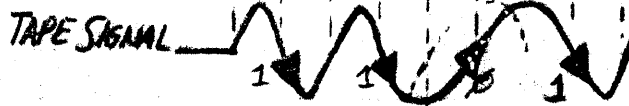
$$C(RWB_{out}) = 1101$$



R/L side of writer



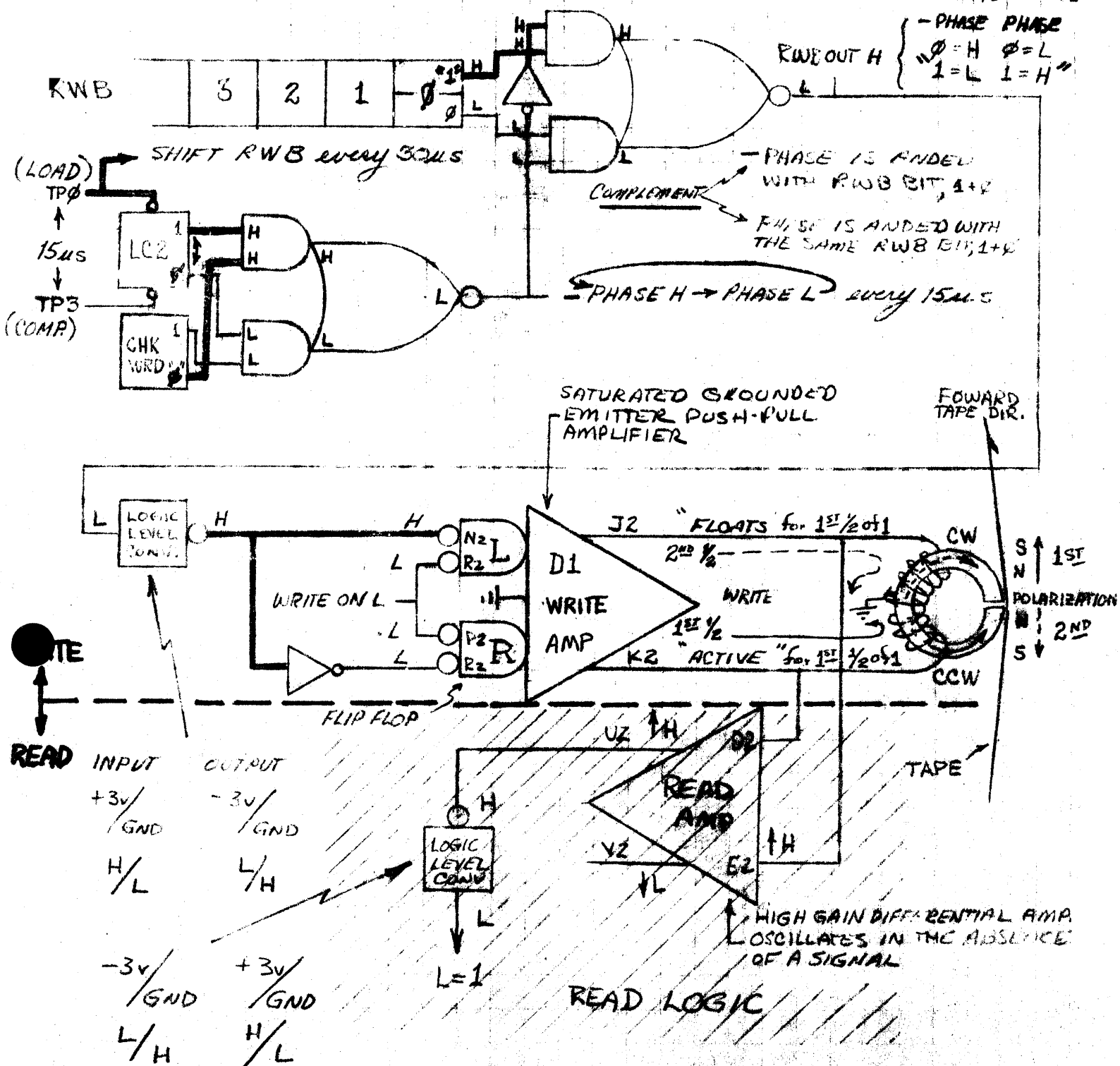
LC2(0) is TP3 } COMPLEMENTS PHASE
LC2(1) is TP0 }



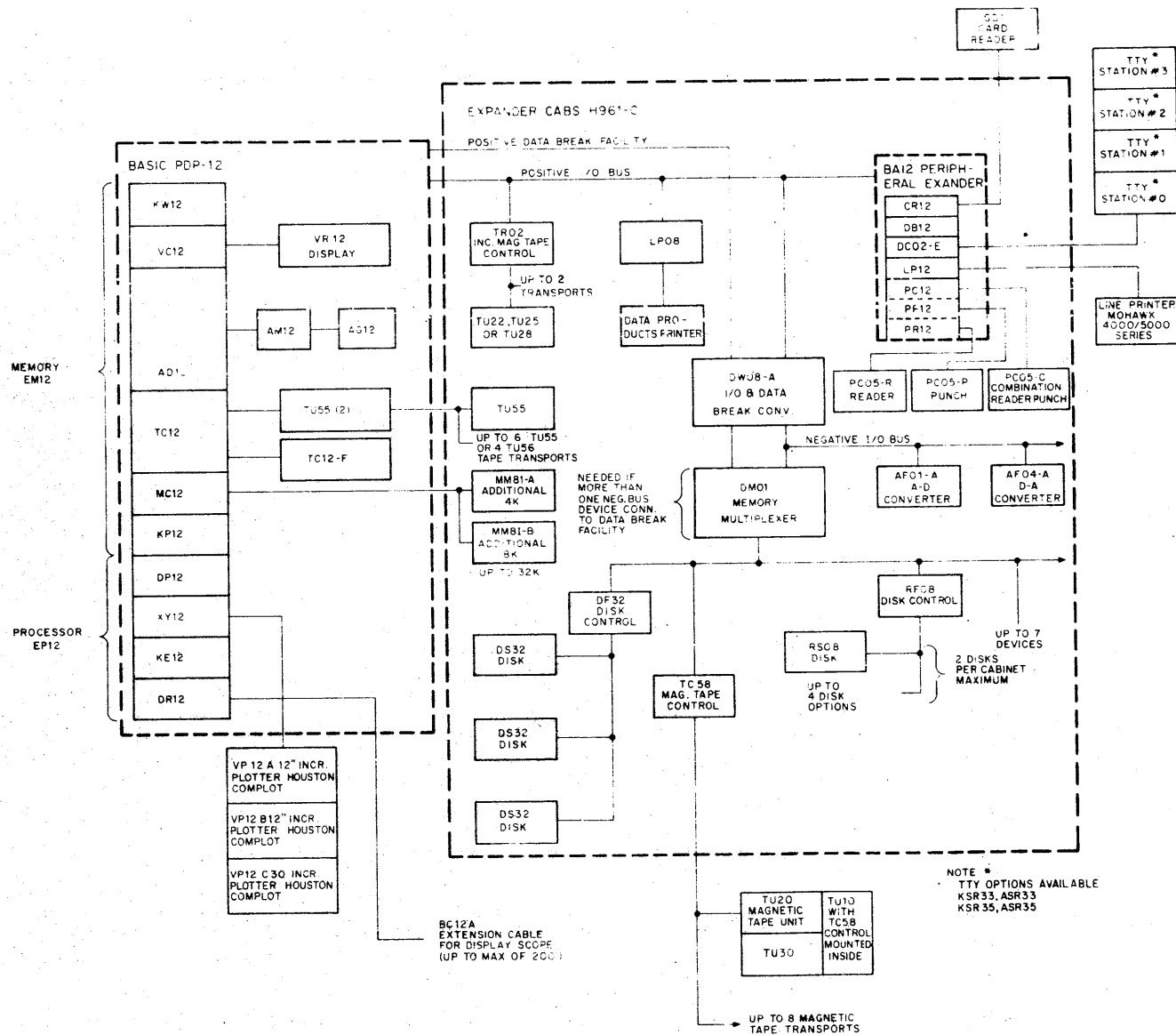
MORE LIKELY PATTERN

LINE TAPE READER-WRITER & CONTROL

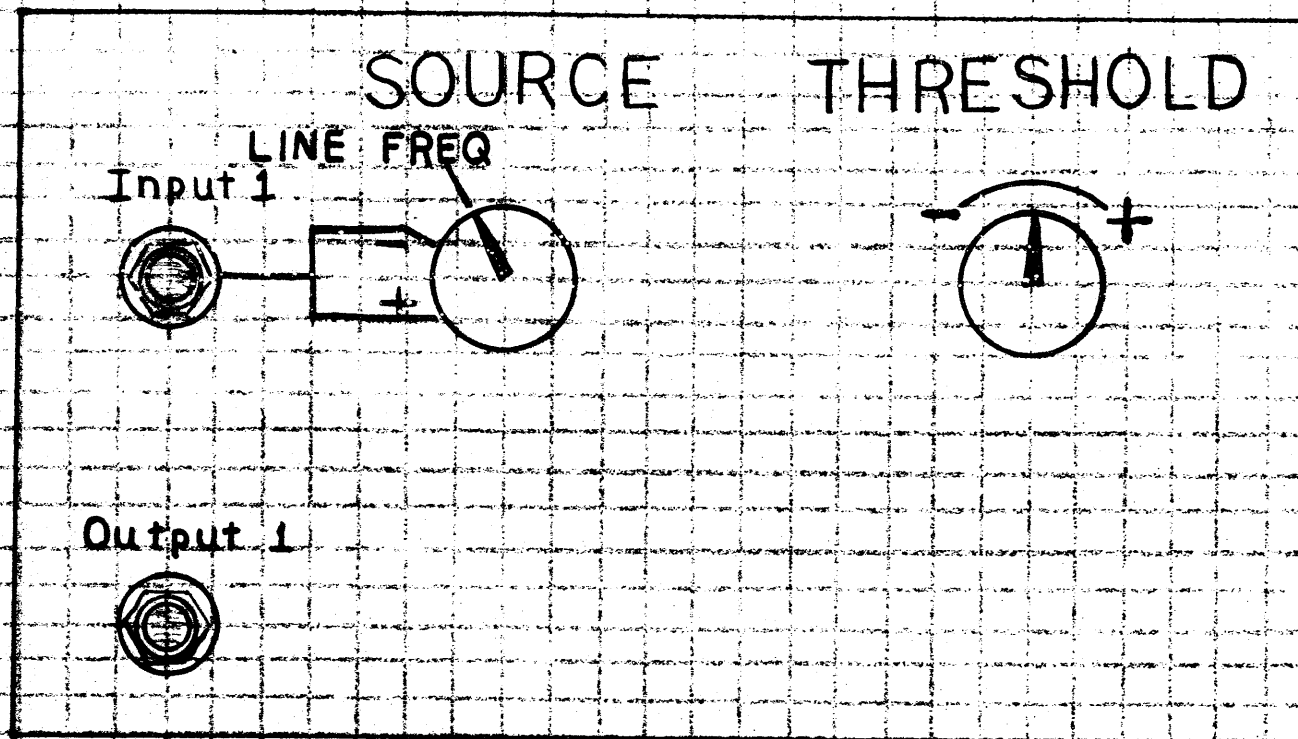
1ST 1/2 2ND 1/2



NOTE: POLARITIES SHOWN ON GATES ARE TRUE WHEN THE RWB IS LOADED & LC 2 (0) i.e., TP0 (ALSO, NOT IN THE CHECK WORD MAJOR STATE). THE RESULT IS AND'ED WITH (IN THE EXAMPLE) RWB 00 (CONSIDER A 1). AT TP3, LC 2 WILL COMPLEMENT ∴ LC 2 → 0, PHASE ∴ → H AND THE INPUT TO THE WRITER COMPLEMENTS, CHANGING POLARIZATION ON TAPE FROM S → N & N → S

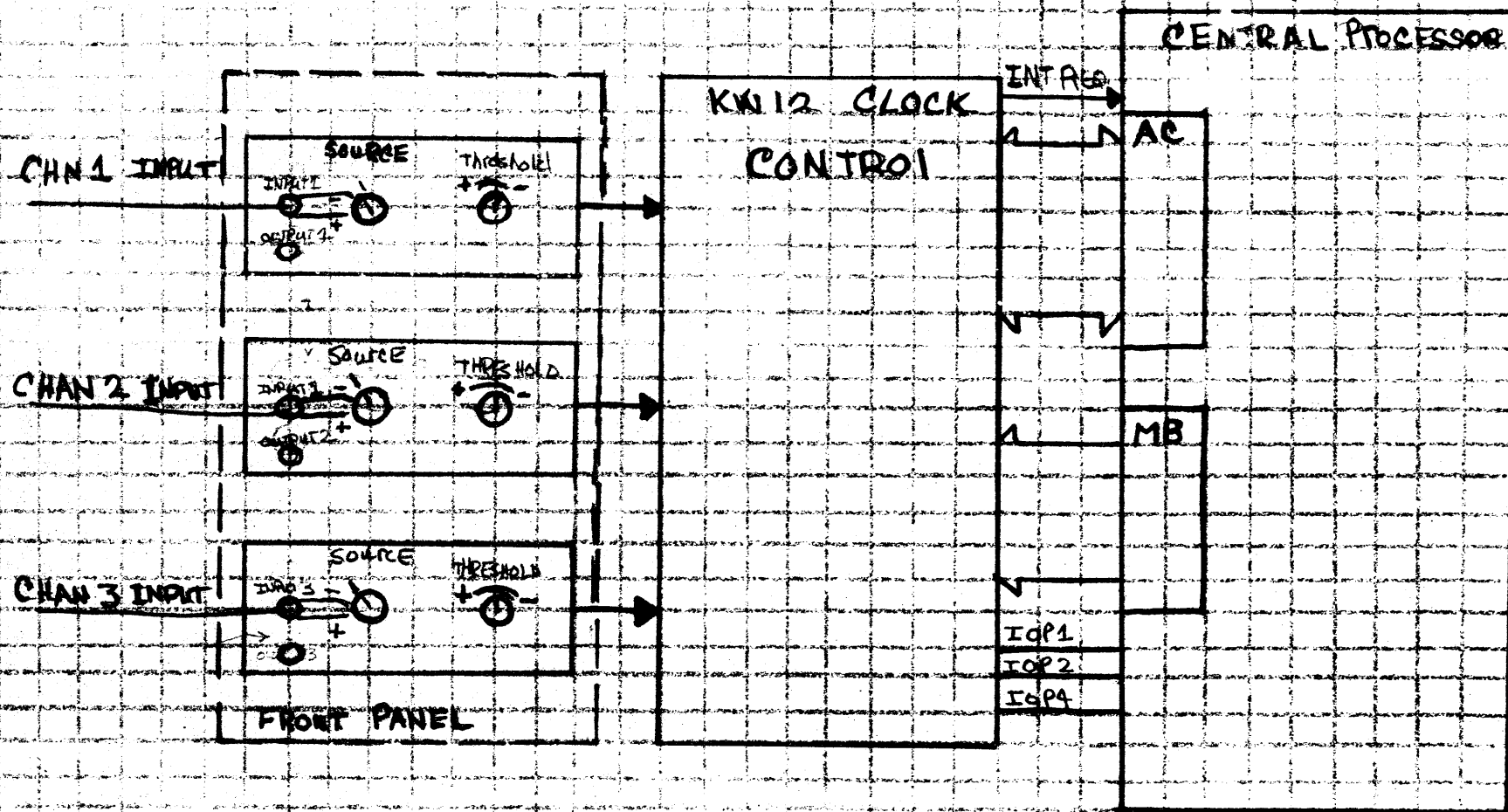


PDP-12 Functional Block Diagram

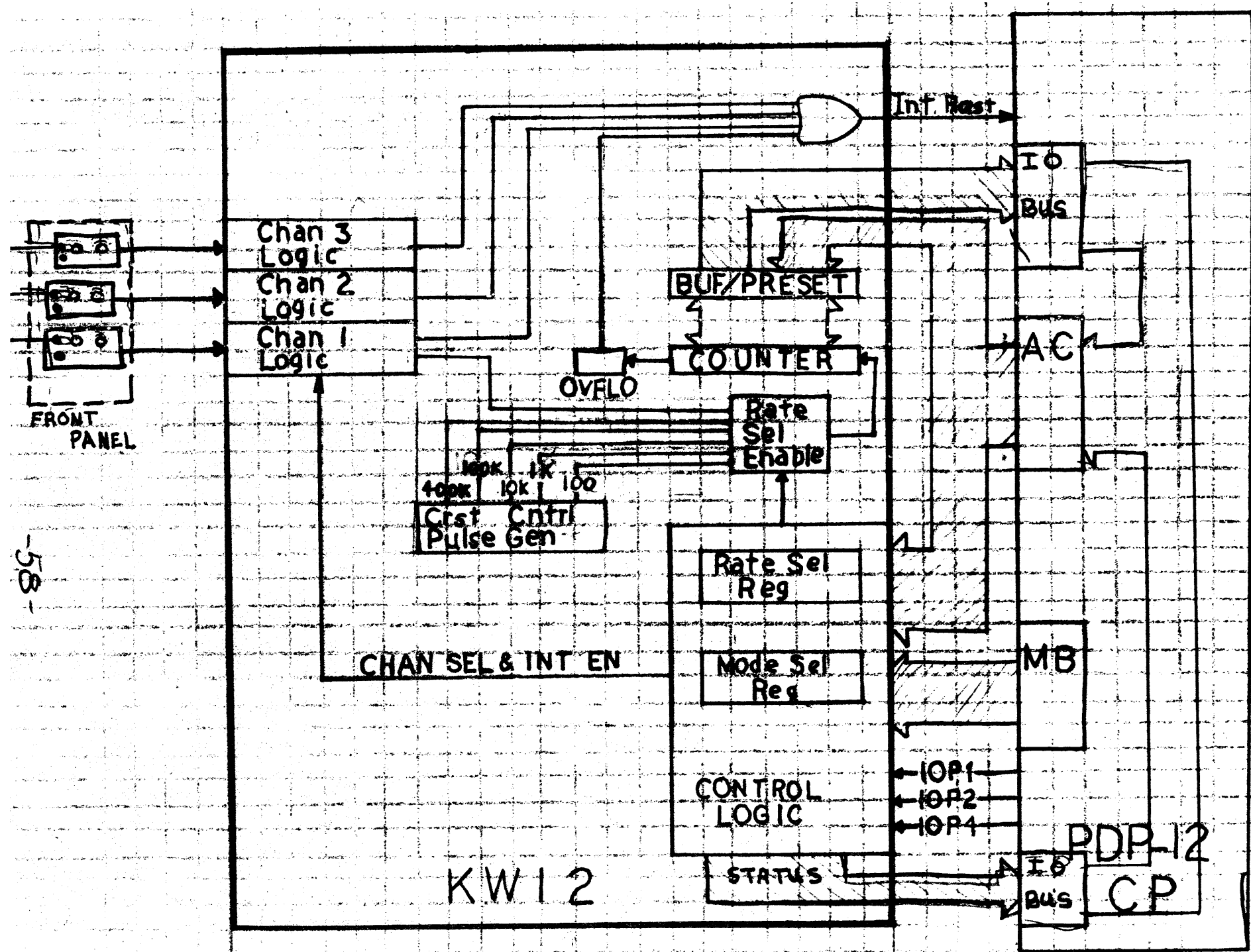


KW12
FRONT PANEL

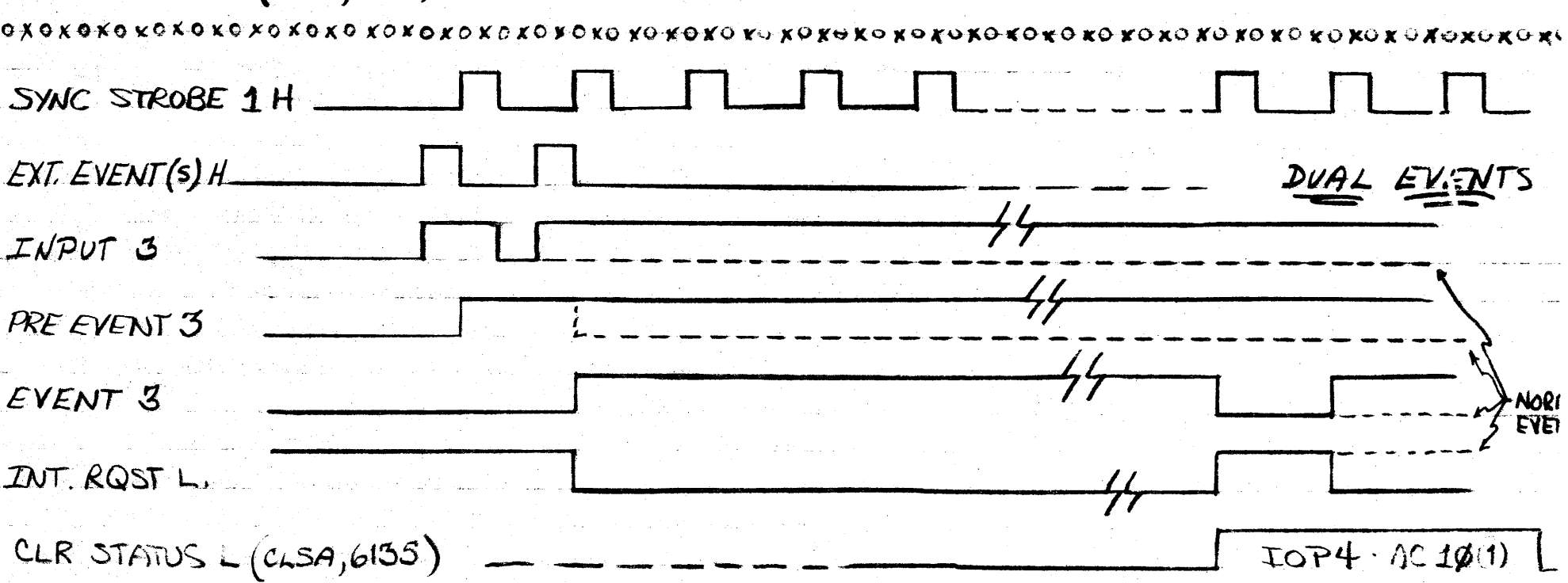
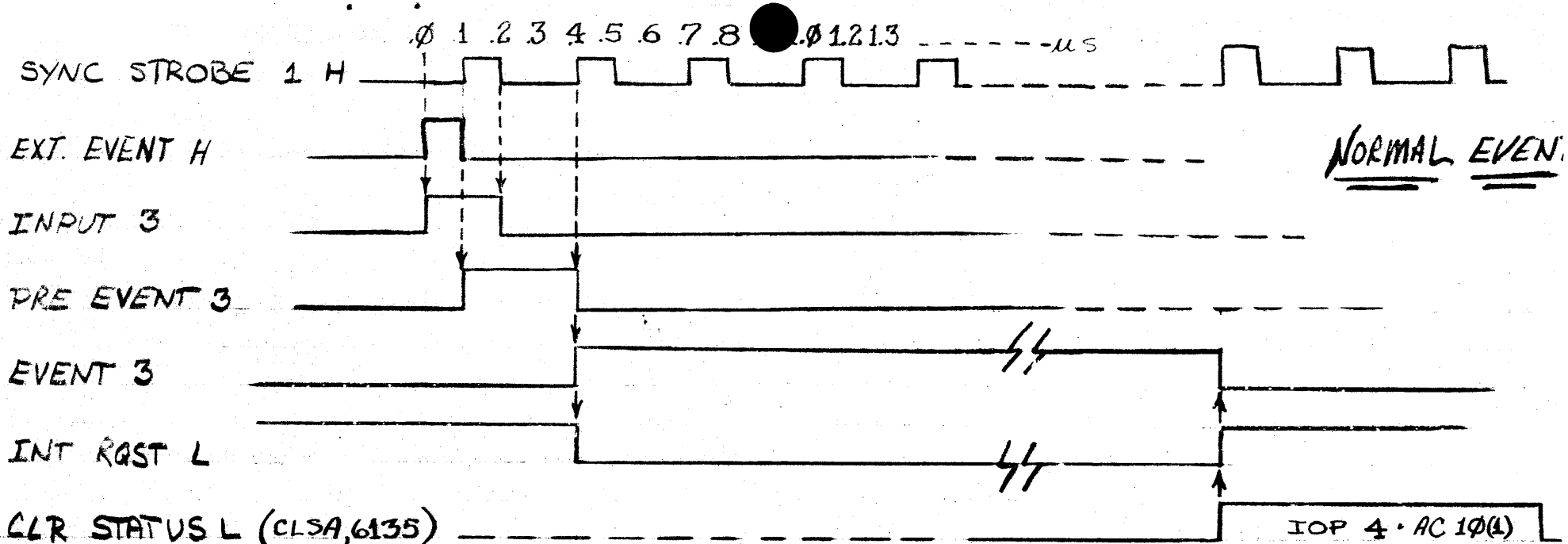
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KW 12 SYSTEM



KW12 BLOCK DIAGRAM



KW12-INPUT CHANNEL

TIMING FORMAT

[illegible]

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

DOCUMENTATION FORMAT

PC	MA	MEM	MB	IR	L	AC	CYCLE	INST	TIME
									T
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1
		0000							T2/S
									T3
									T4
									T5 W
									T1

MARK TAPE, COPY TAPE, PRINT DIAL INDEX EXERCISE

NOTE: See references to paragraphs
(ex. 5, 2) on pp. (ex. 1-5)
in the LA 6 DIAL Manual

Initial Starting Procedure

1. Place dial tape on top unit.
Select unit 0 (8) on T055 transport.
2. Mount another tape on the lower transport.
Select unit 1.

NOTE: A. This is only required for commands AS, LI, QL, and SB
(See 1.8 commands).
B. This is also required when using the Mark 12 program.
C. If this is a new DECTape rather than Linc tape, it must
be placed on the left hub and an empty spool on the
right hub. The left spool must now be wound on the
right using "LOCAL" and "→ (AW)".

3. Set switches on both tape units to "REMOTE" and set unit 0 (8) to
"Write Enable".
4. Set the Mode Switch to "LINC" mode and press "IO PRESET" to preset
Linc IF 2 and Linc DF to 3.
5. Set "LSW" to 0701 and "RSW" to 7300.

NOTE: Depressing switch on the panel side (of the switch) is a 0
and on the operator side equals a 1.

If tape comes off the spool, you didn't wind enough of it.
Turn "REMOTE" switch "OFF", rewind spool with leader and switch to
"REMOTE" again.

6. Press to "DO" switch (memory is initialized by tapes).
7. When tape motion stops, press "START 20" (starting address of Dial)

Dial Program Selection

1. Turn A-D knobs 3 (Cursor Control) and 7 (Line Control) fully CW (See 2.0)
2. Using the keyboard, type Linefeed (→, ) "cursor" appears at the
lower left of DISPLAY) DX RETURN () to obtain the Dial Index (See 5.4)

3. To view the entire index use the following keys:

<u>KEY</u>	<u>ACTION</u>
1	Forward one frame
2	Forward one line
Q	Backward one frame
W	Backward one line

4. When the MARK 12 program listing is found, perform the following steps using the keyboard.

A. Strike Key "RETURN and LINE FEED"

1. Return gets you back to DIAL
2. Line Feed stations the cursor in the lower left of Display

B. Type

1. "LO" (load)
2. "SPACE" ()
3. "MARK12" (w/no space)
4. "COMMA" (,)
5. "Ø"
6. "RETURN" (↵) MARK12 instructions should be seen on the display.

Refer to MARK 12 program listing (Program Library)

5. Follow the instructions on the Display.

Returning to DIAL

1. Using the keyboard, type:

- A. "2"
- B. "LINE FEED"

NOTE: Depending on programs used (other than MARK12) there are numerous ways to remove the current display, typing:

1. "RETURN" (clears the screen - back to DIAL)
2. "CONTROL D" (at the same time, gets DIAL back)
3. "CONTROL P" (together, gets you back to PIP)

Copy Tape

1. "LINE FEED" - cursor moves to lower left.
2. Type "DX & RETURN" (returns Index)
3. Locate PIP (peripheral interchange program) in the Index
4. "RETURN" back to DIAL

5. "LINEFEED" cursor lower left

NOTE: Do not use LO for PIP - has an auto loader type PIP & RETURN.

6. Select "A" (auxilliary options) and "RETURN"

NOTE: At this point tape to be duplicated should be to transport Ø (8)

7. Select "D" (duplicate) and "RETURN"

NOTE: Duplication begins

Observe tape instruction register on the PDP-12 Panel

Tape Inst Reg.

a. 000 702 RDE-Unit Ø (8)

b. 000 706 WRI

c. 000 707 CHK-Unit 1

8. "CONTROL D" together - back to DIAL

9. Linefeed - cursor lower left.

Print Index

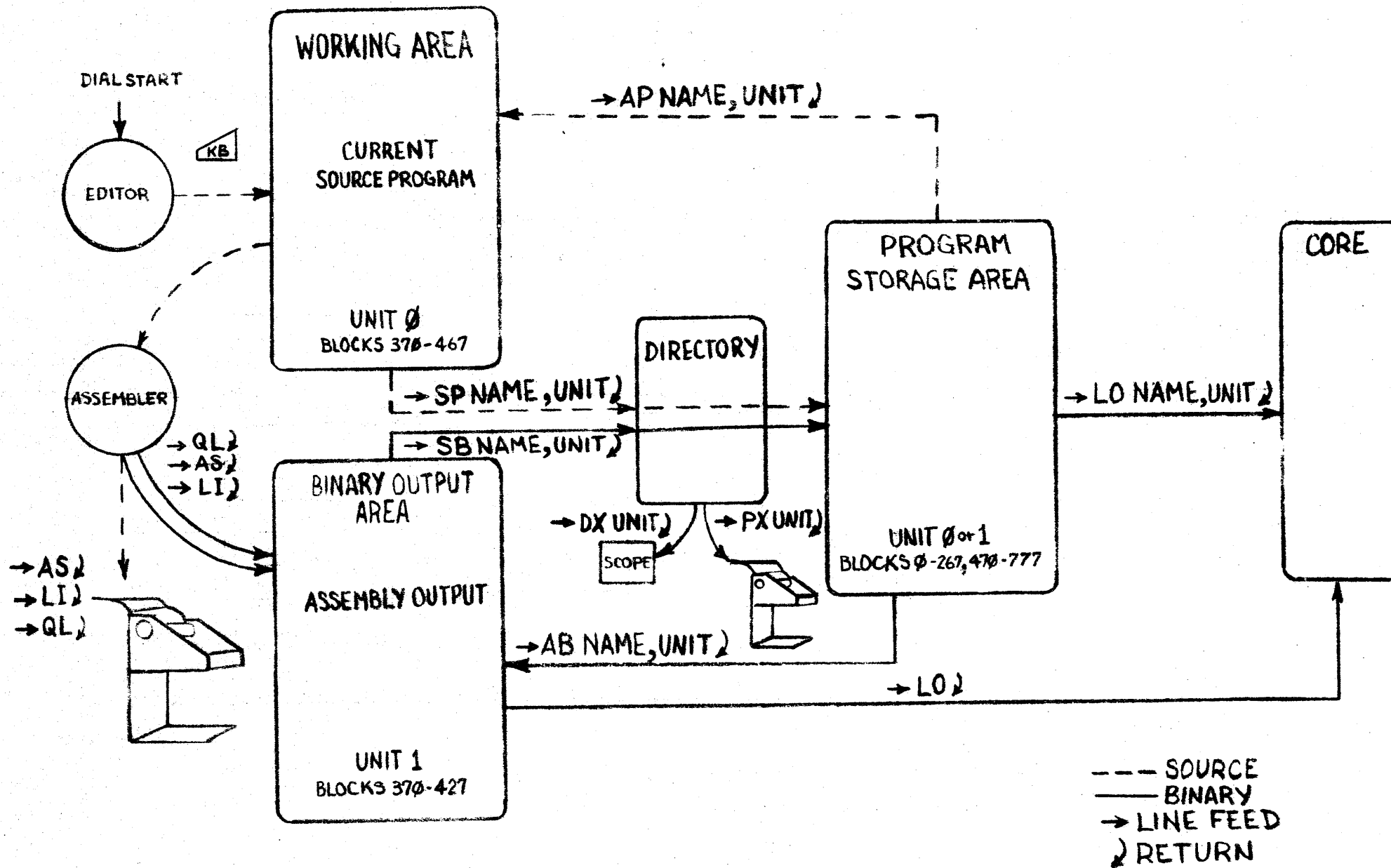
1. Linefeed print index unit return (See 5.5)

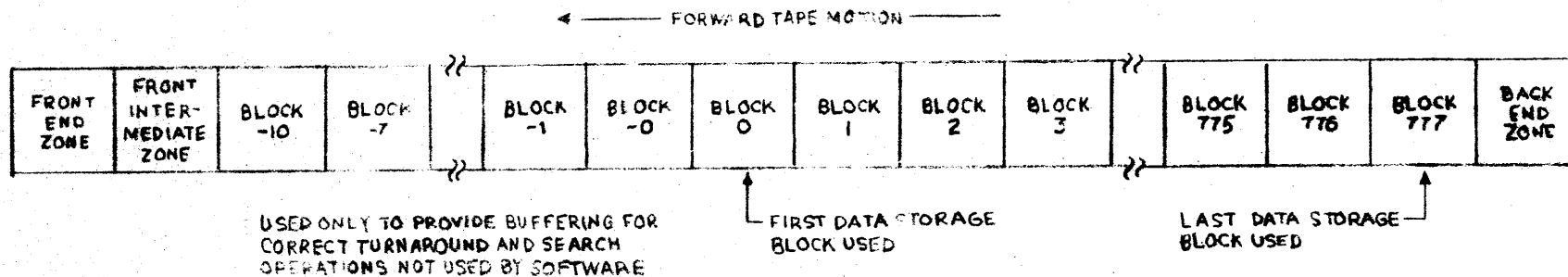
→ PX (,unit)
Printout occurs

↓

DIAL BLOCK DIAGRAM

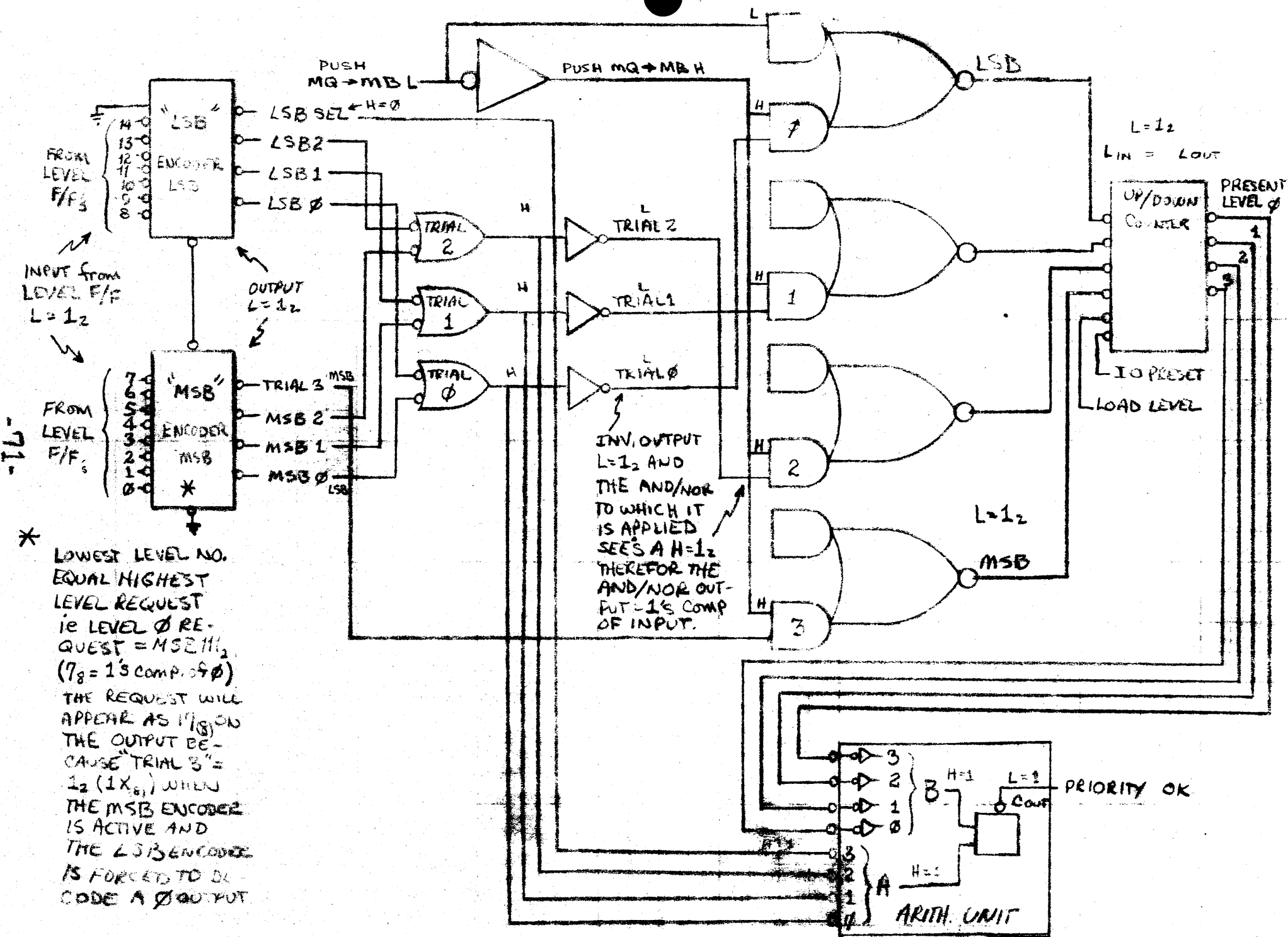
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LINCtape OVERALL FORMAT

INTERRUPT LEVEL PRIORITY



* LOWEST LEVEL NO. EQUAL HIGHEST LEVEL REQUEST ie LEVEL 0 REQUEST = MSE 11₂ (7₈ = 1's comp. of 0) THE REQUEST WILL APPEAR AS 17(8) ON THE OUTPUT BECAUSE "TRIAL 3" = 12 (1X₈) WHEN THE MSB ENCODER IS ACTIVE AND THE LSB ENCODER IS FORCED TO OUTPUT CODE A 0 OUTPUT