DEC-14-HGZA-D (II)

pdp14

MAINTENANCE MANUAL
VOLUME II

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CONTENTS

CONTENTS (Cont)

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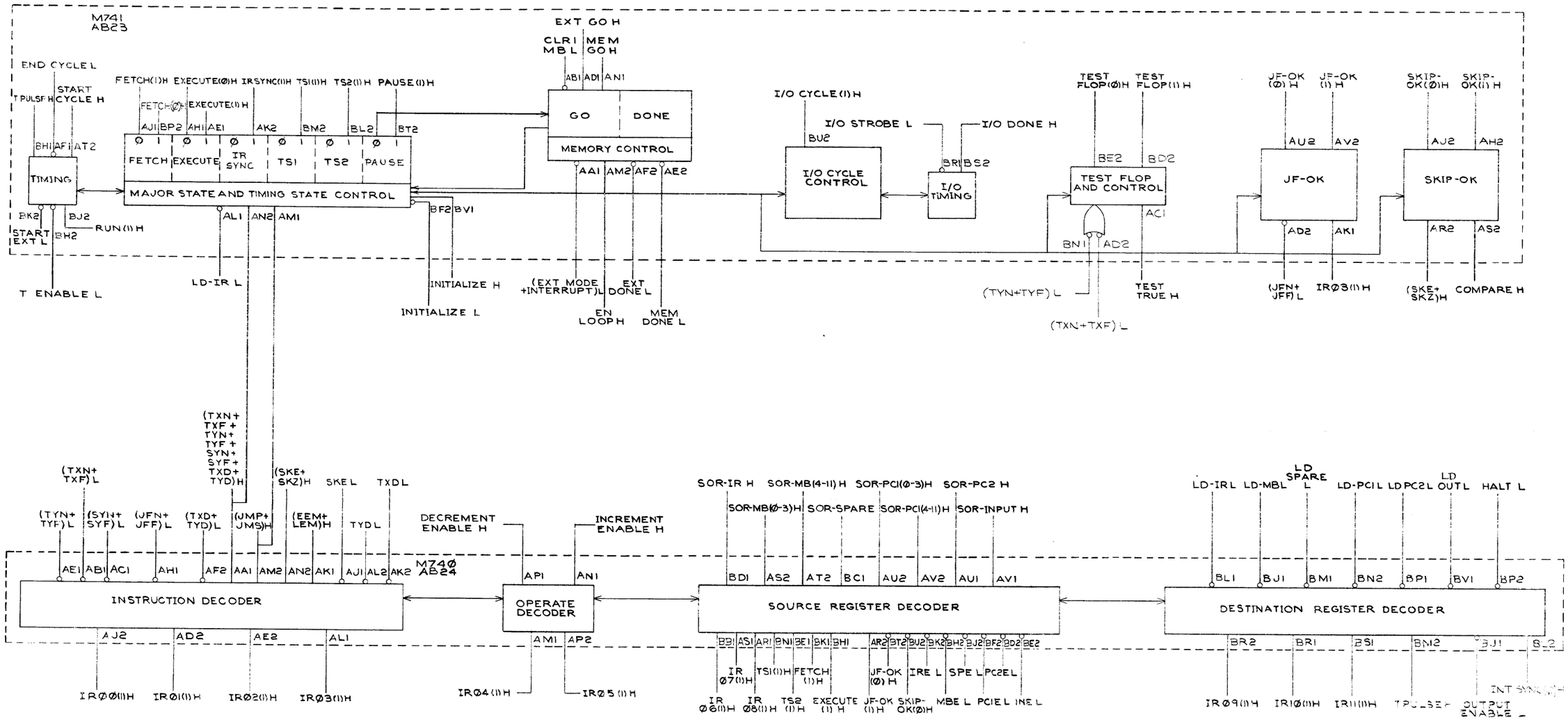


Figure II-1 PDP-14 Control Block Schematic (Sheet 1)

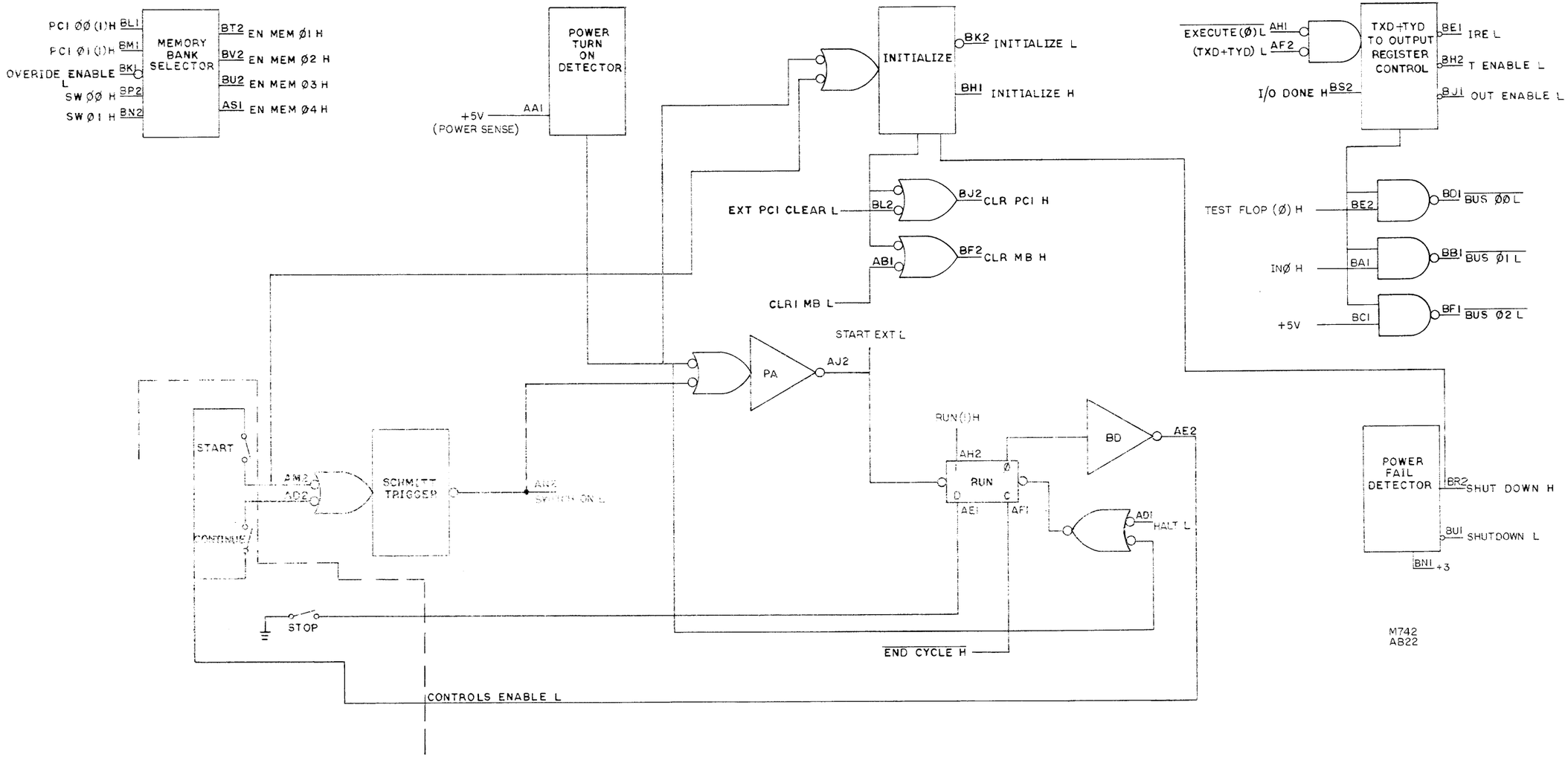


Figure II-2 PDP-14 Control Block Schematic (Sheet 2)

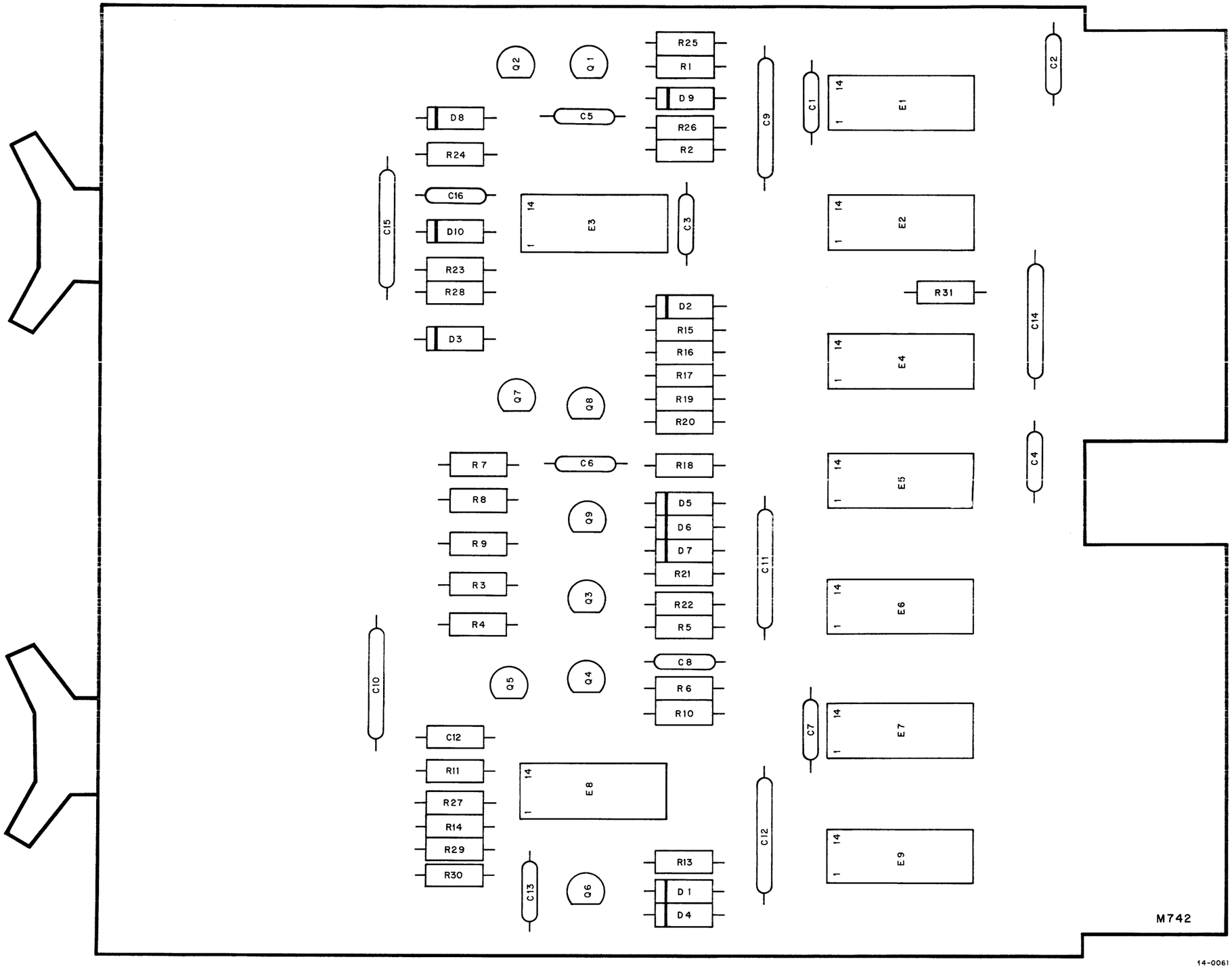
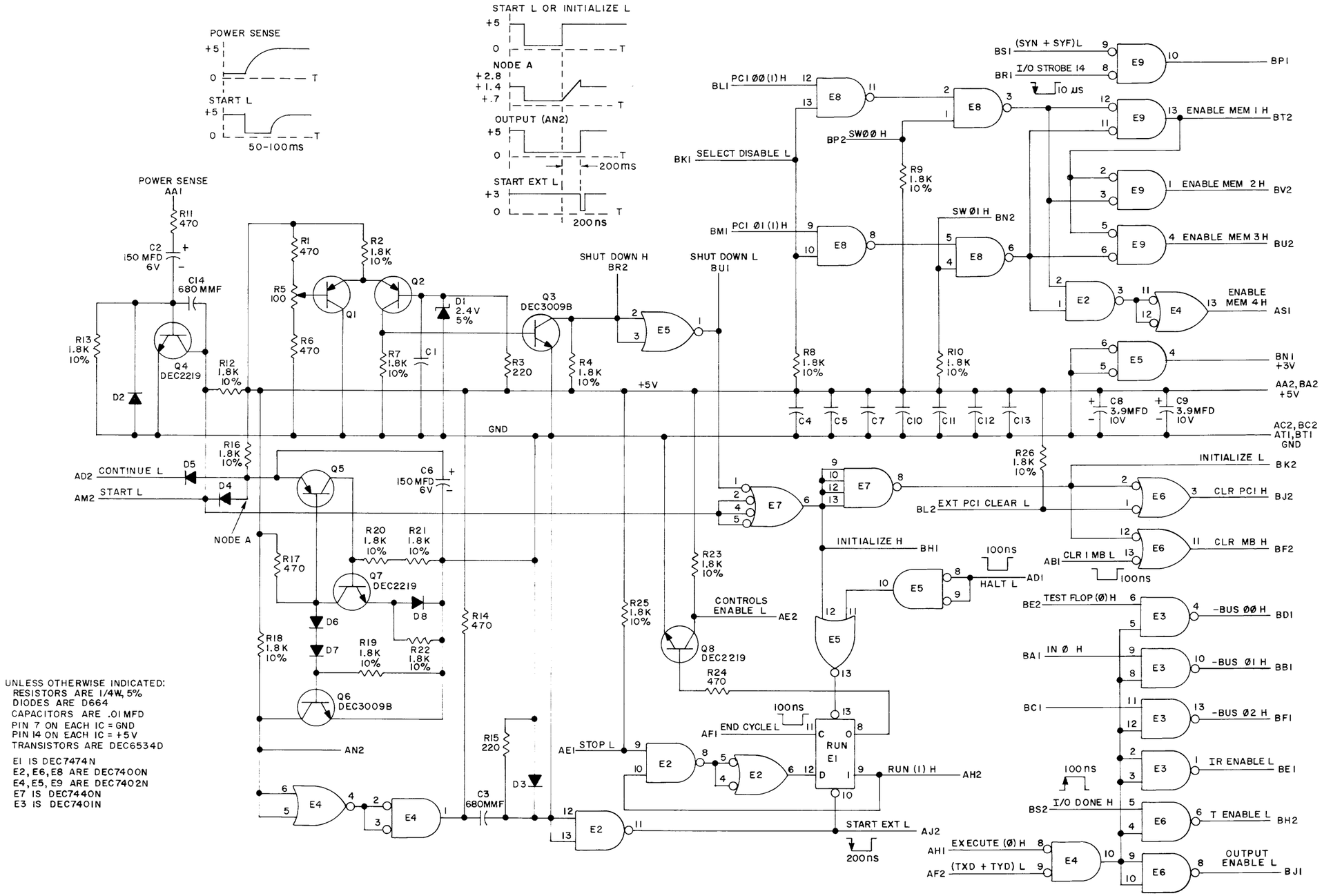


Figure II-3 PDP-14 Switch and Power Control M742 Component Locations



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D664
CAPACITORS ARE .01MFD
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
TRANSISTORS ARE DEC6534D

E1 IS DEC7474N
E2, E6, E8 ARE DEC7400N
E4, E5, E9 ARE DEC7402N
E7 IS DEC7440N
E3 IS DEC7401N

Figure II-4 PDP-14 Switch and Power Control M742 Circuit Schematic

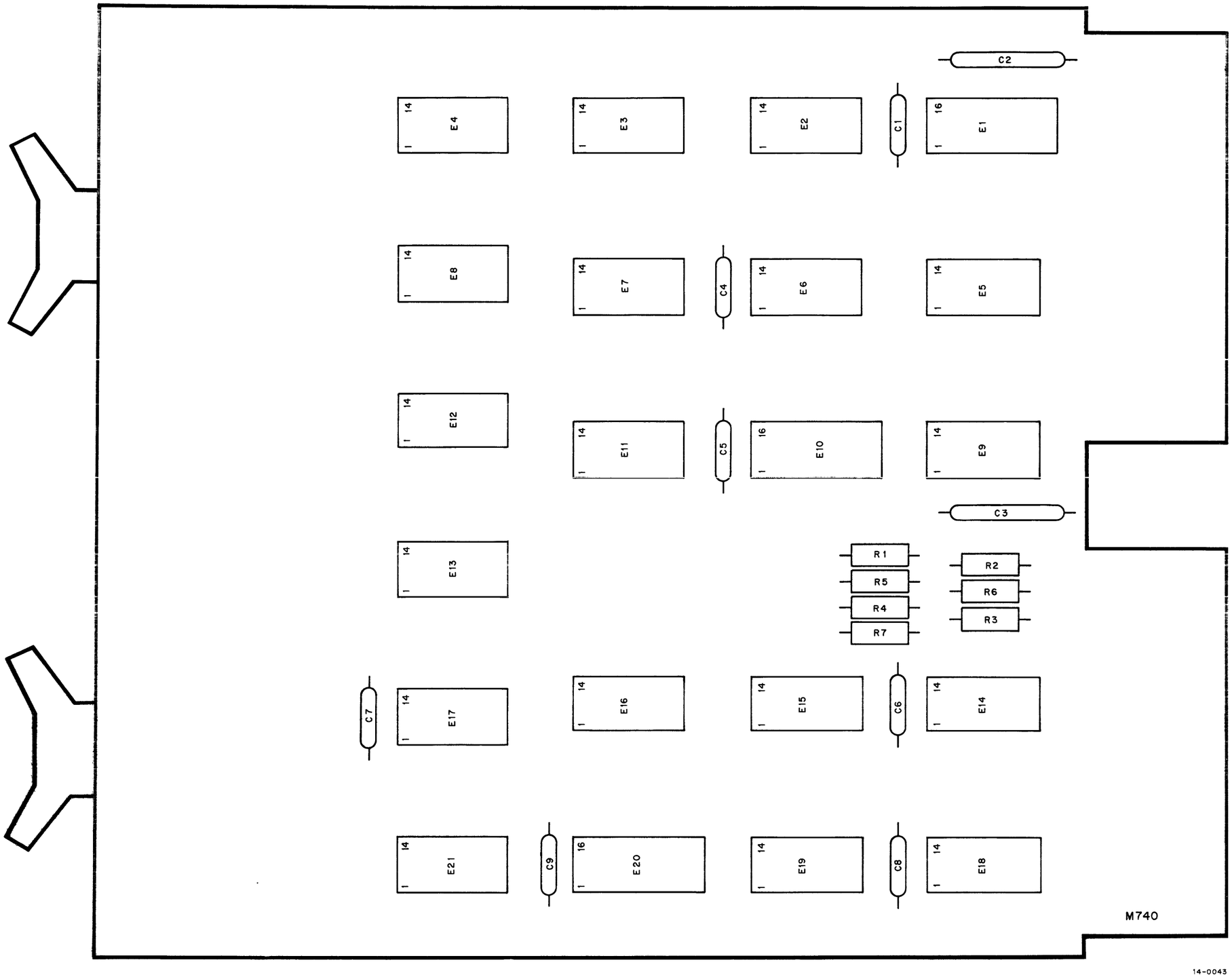
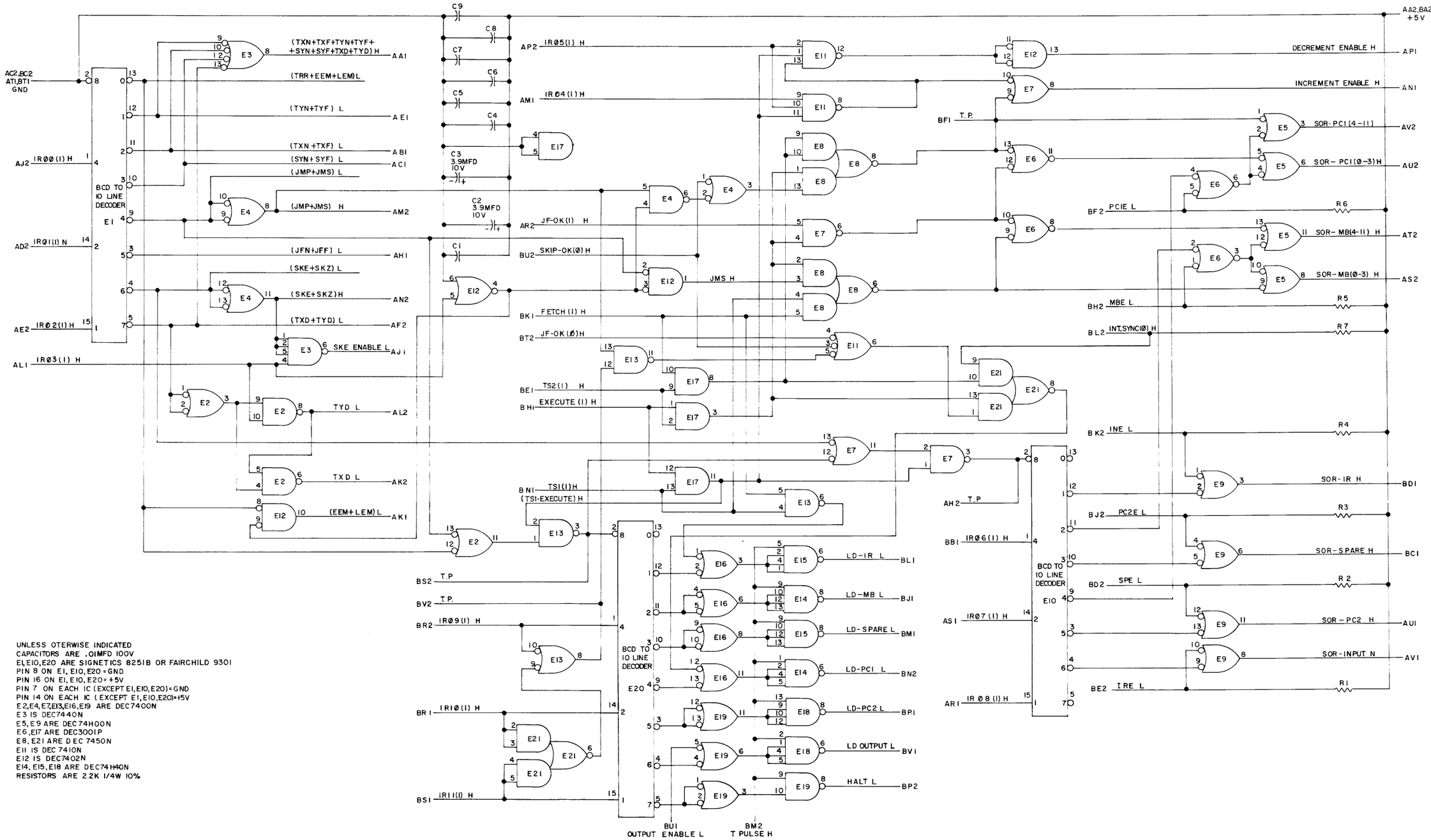


Figure II-5 Instruction Decoder and Register Control M740 Component Locations



UNLESS OTERWISE INDICATED
CAPACITORS ARE .OIMFD 100V
E1,E10,E20 ARE SIGNETICS 8251B OR FAIRCHILD 9301
PIN 8 ON E1, E10, E20 = GND
PIN 16 ON E1, E10, E20 = +5V
PIN 7 ON EACH IC (EXCEPT E1,E10,E20) = GND
PIN 14 ON EACH IC (EXCEPT E1,E10,E20) = +5V
E2,E4,E7,E13,E16,E19 ARE DEC7400N
E3 IS DEC7440N
E5,E9 ARE DEC74H00N
E6,E17 ARE DEC3001P
E8,E21 ARE DEC 7450N
E11 IS DEC7410N
E12 IS DEC7402N
E14,E15,E18 ARE DEC74H40N
RESISTORS ARE 2.2K 1/4W 10%

Figure II-6 Instruction Decoder and Register Control M740 Circuit Schematic

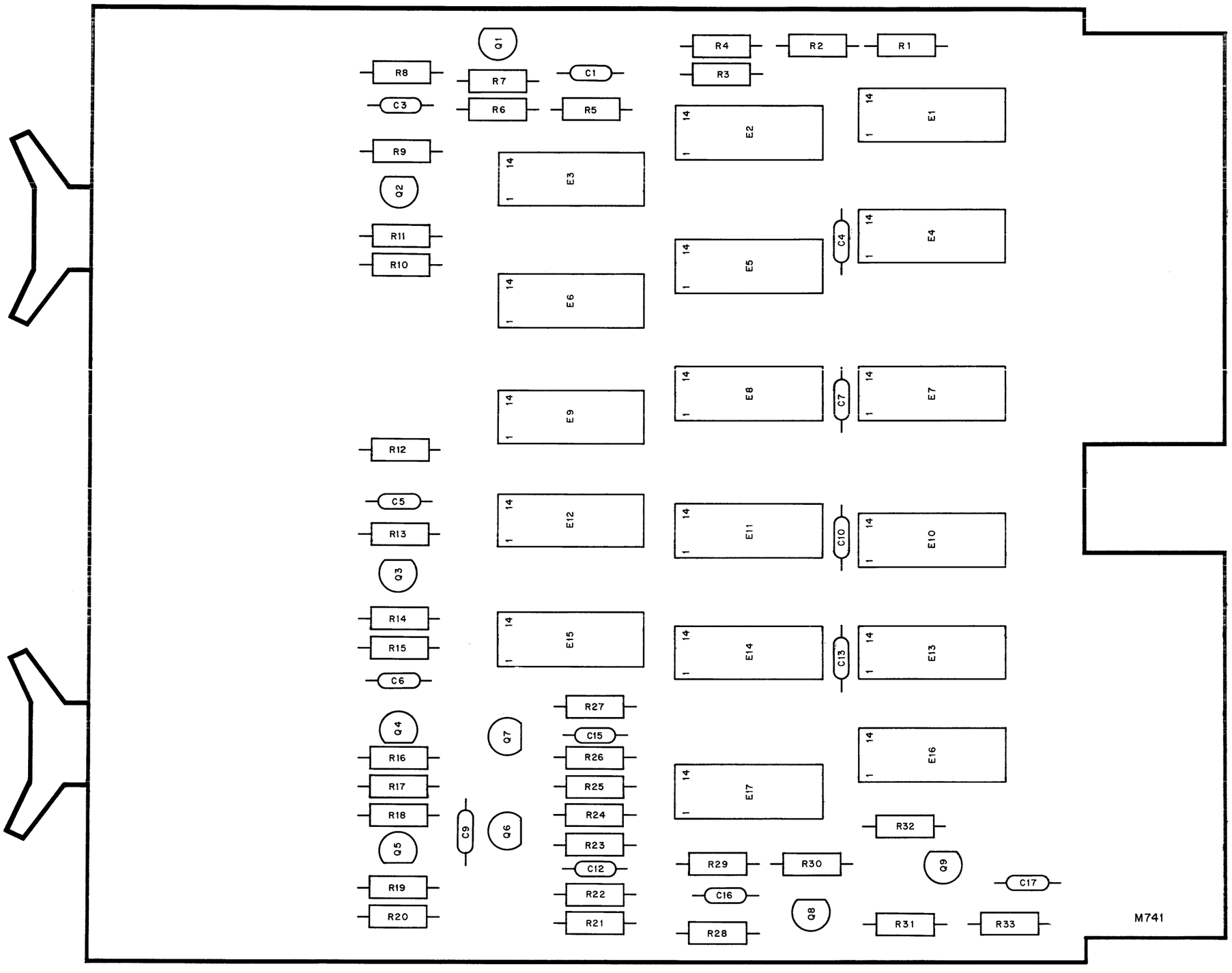
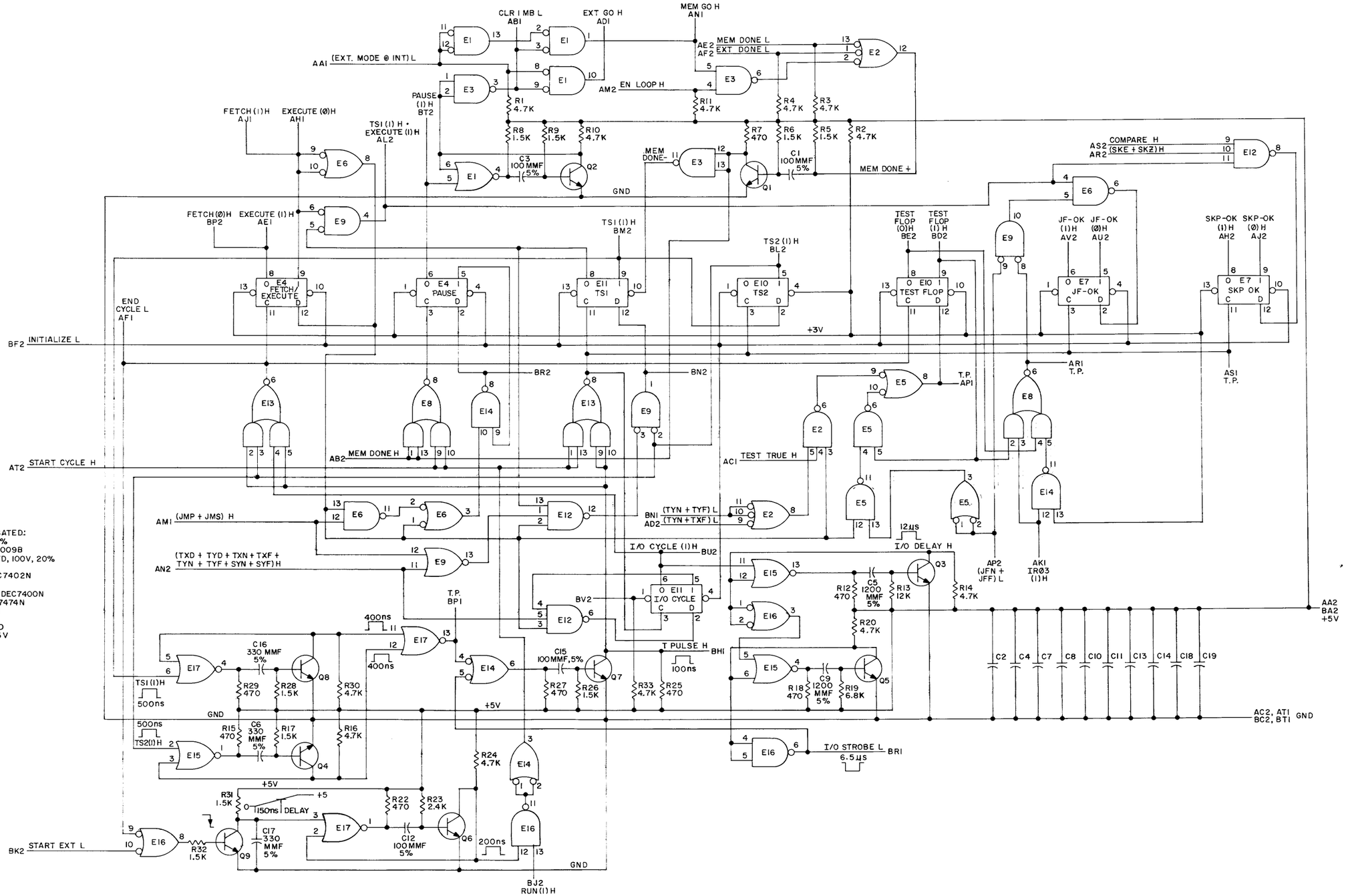


Figure II-7 PDP-14 Major States and Timing M741 Component Locations



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC30098
CAPACITORS ARE .01 MFD, 100V, 20%

E1, E9, E15, E17 ARE DEC7402N
E2, E12 ARE DEC7410N
E3, E5, E6, E14, E16 ARE DEC7400N
E4, E7, E10, E11 ARE DEC7474N
E8, E13 ARE DEC74H50N

PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

Figure II-8 PDP-14 Major States and Timing M741 Circuit Schematic

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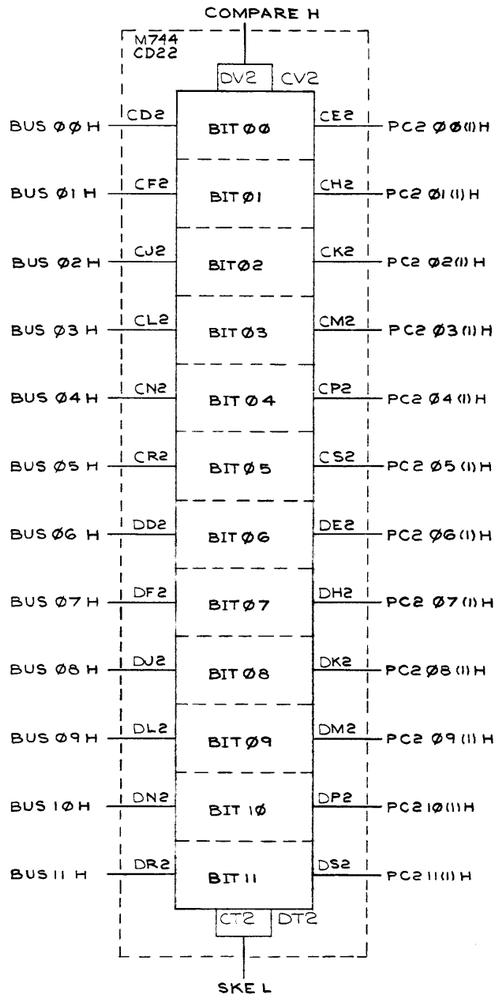


Figure II-9 Compare Control Block Schematic

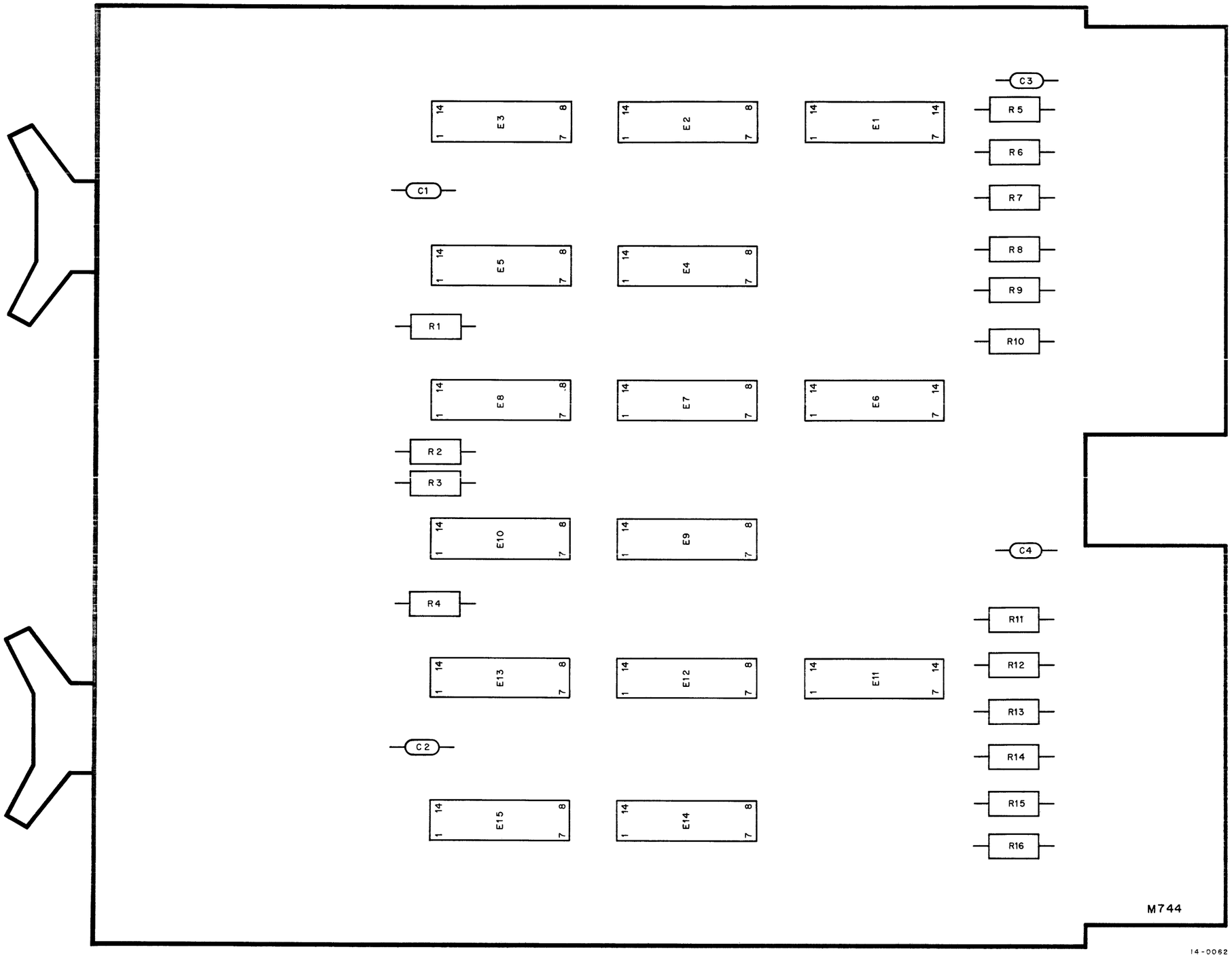
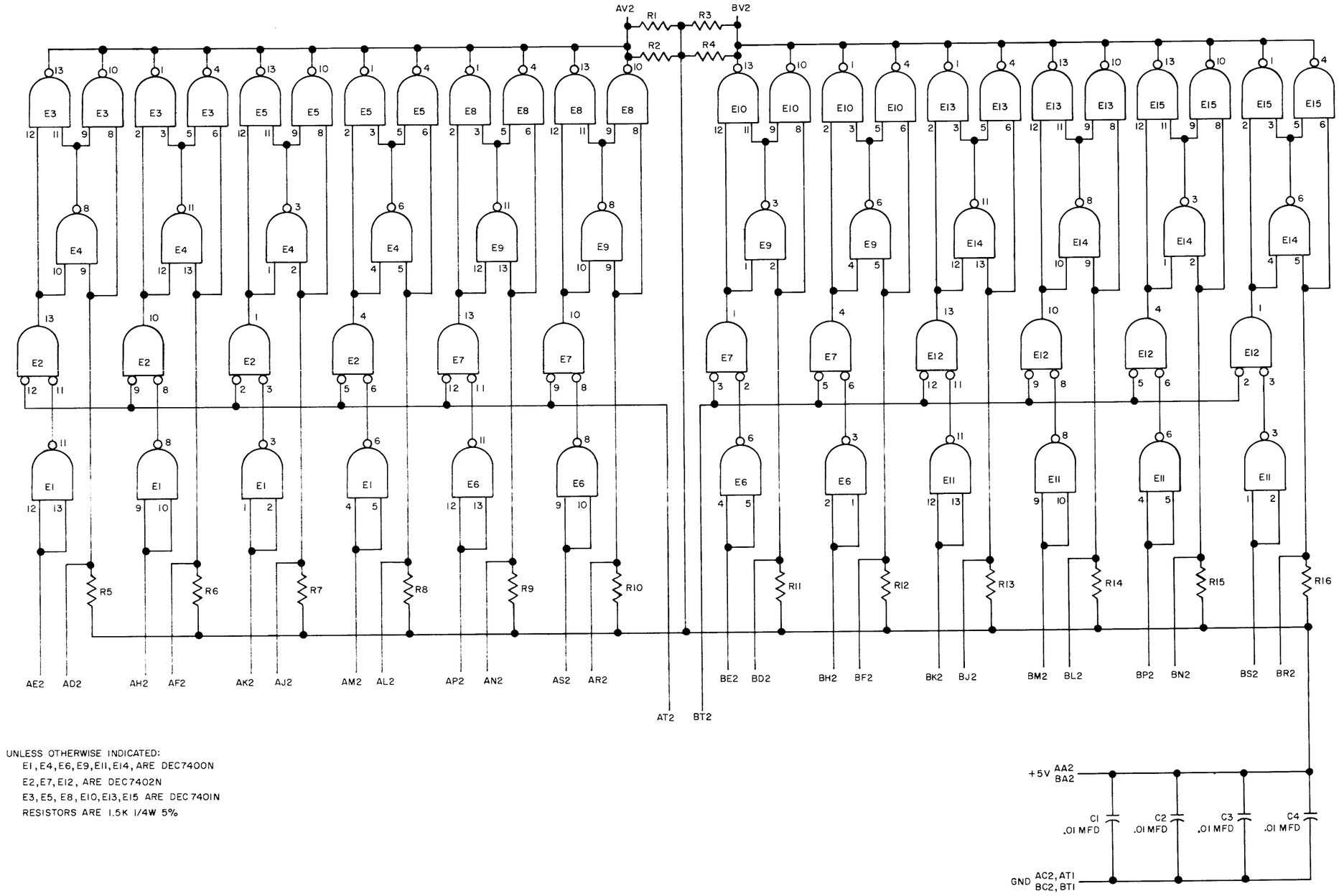


Figure II-10 Register Compare Circuit M744 Component Locations



UNLESS OTHERWISE INDICATED:
E1, E4, E6, E9, E11, E14, ARE DEC7400N
E2, E7, E12, ARE DEC7402N
E3, E5, E8, E10, E13, E15 ARE DEC7401N
RESISTORS ARE 1.5K 1/4W 5%

Figure II-11 Register Compare Circuit M744 Circuit Schematic

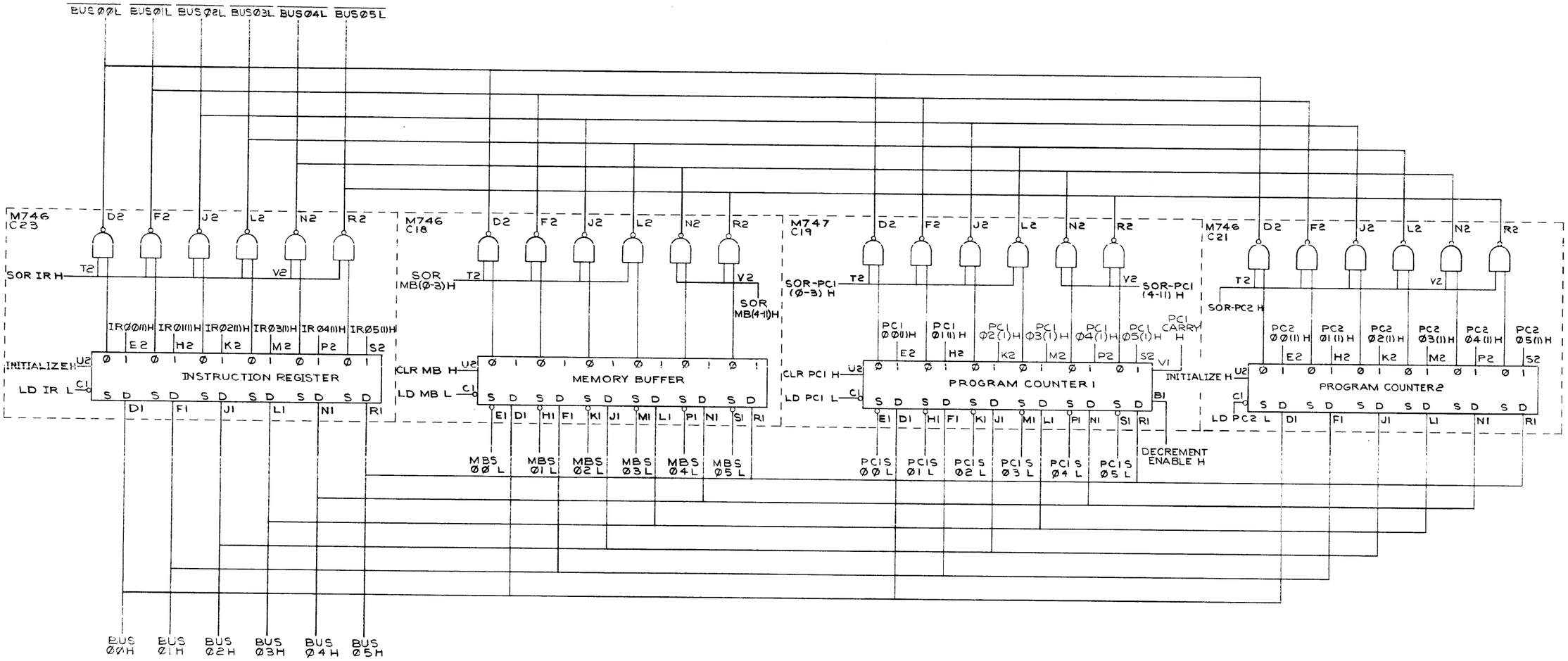


Figure II-12 Major Register (Bits 0-5) Block Schematic

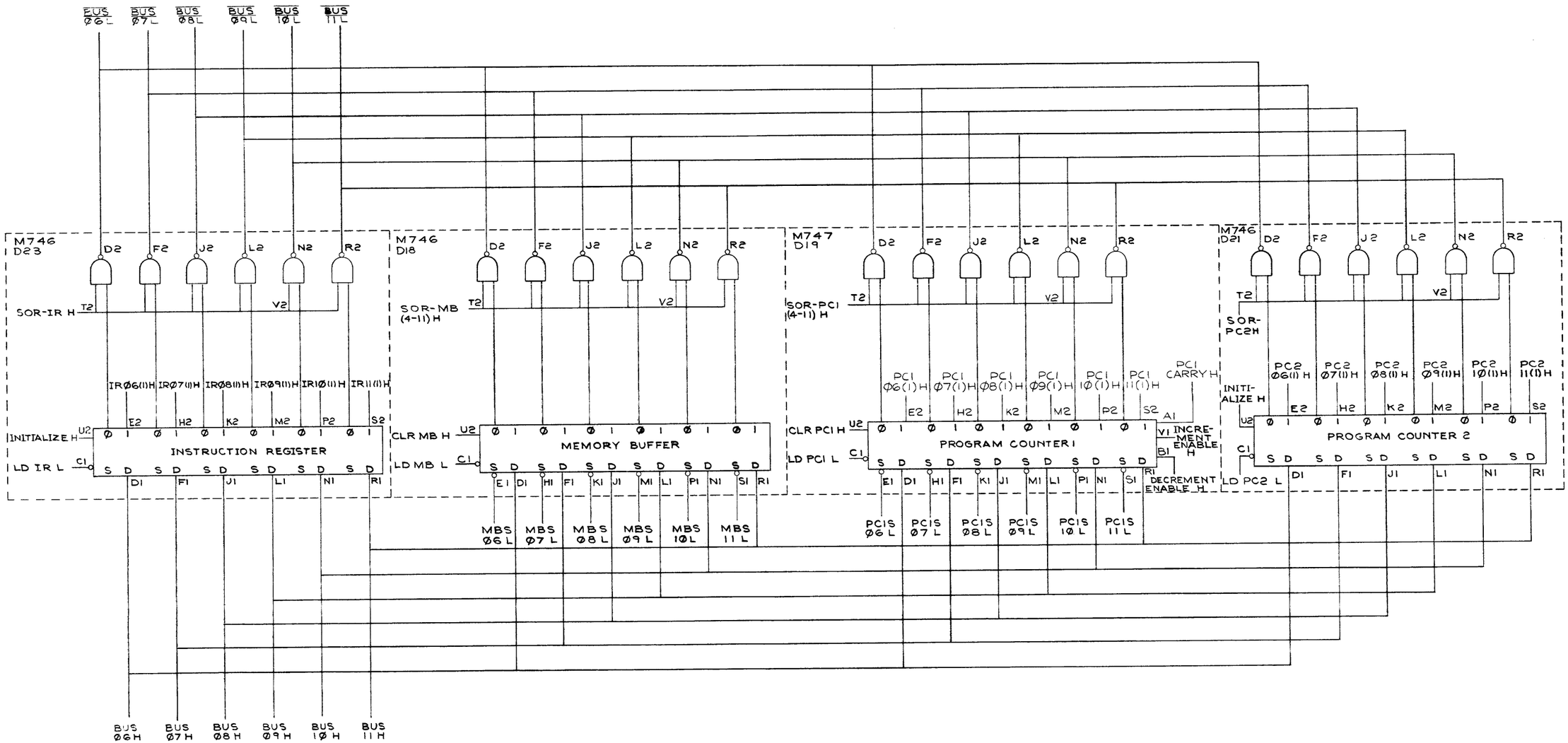


Figure II-13 Major Register (Bits 6-11) Block Schematic

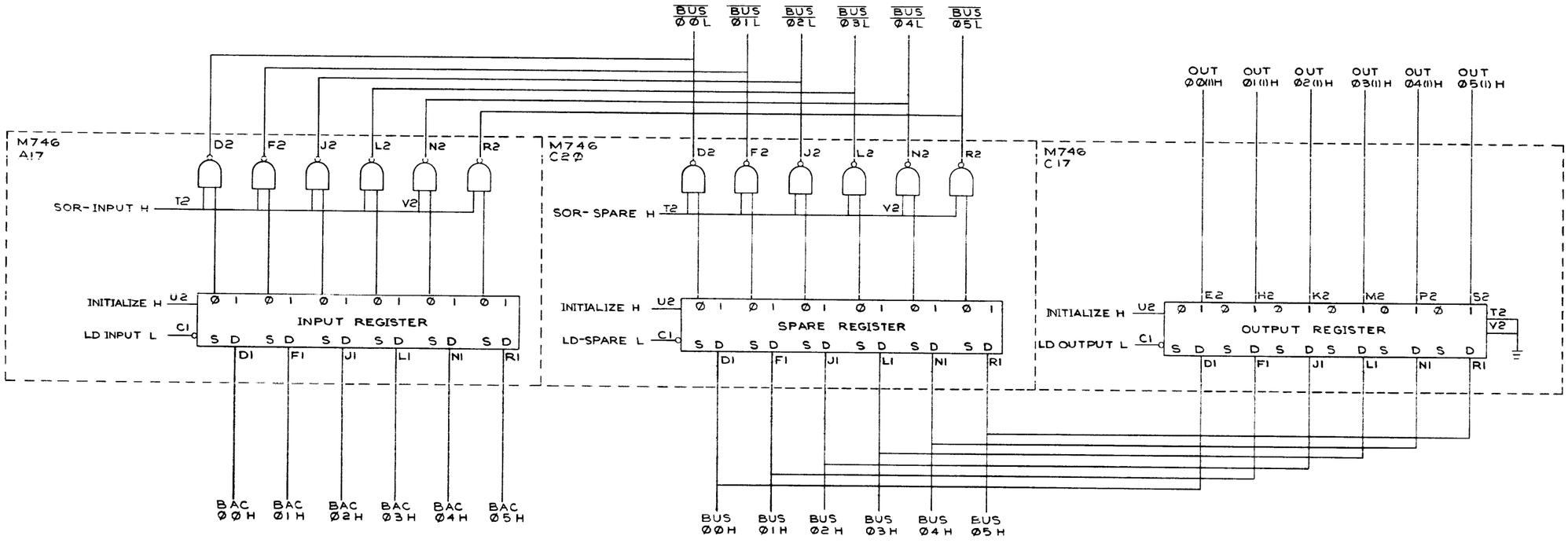


Figure II-14 Registers (Bits 0-5) Block Schematic

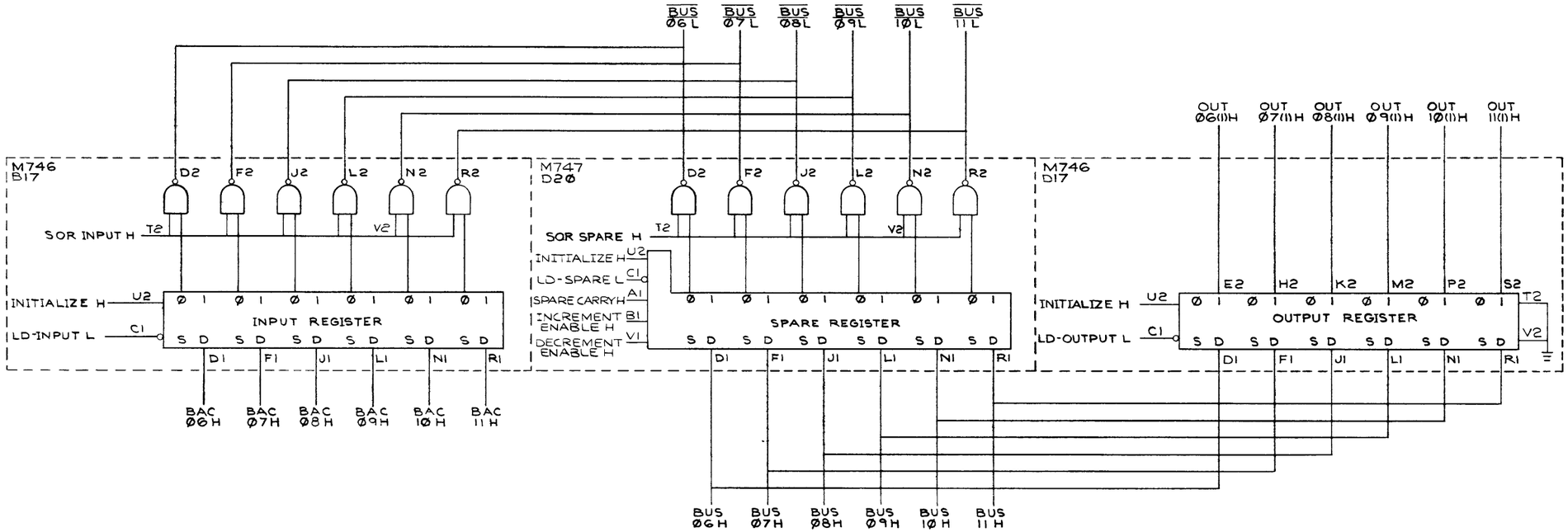


Figure II-15 Registers (Bits 6-11) Block Schematic

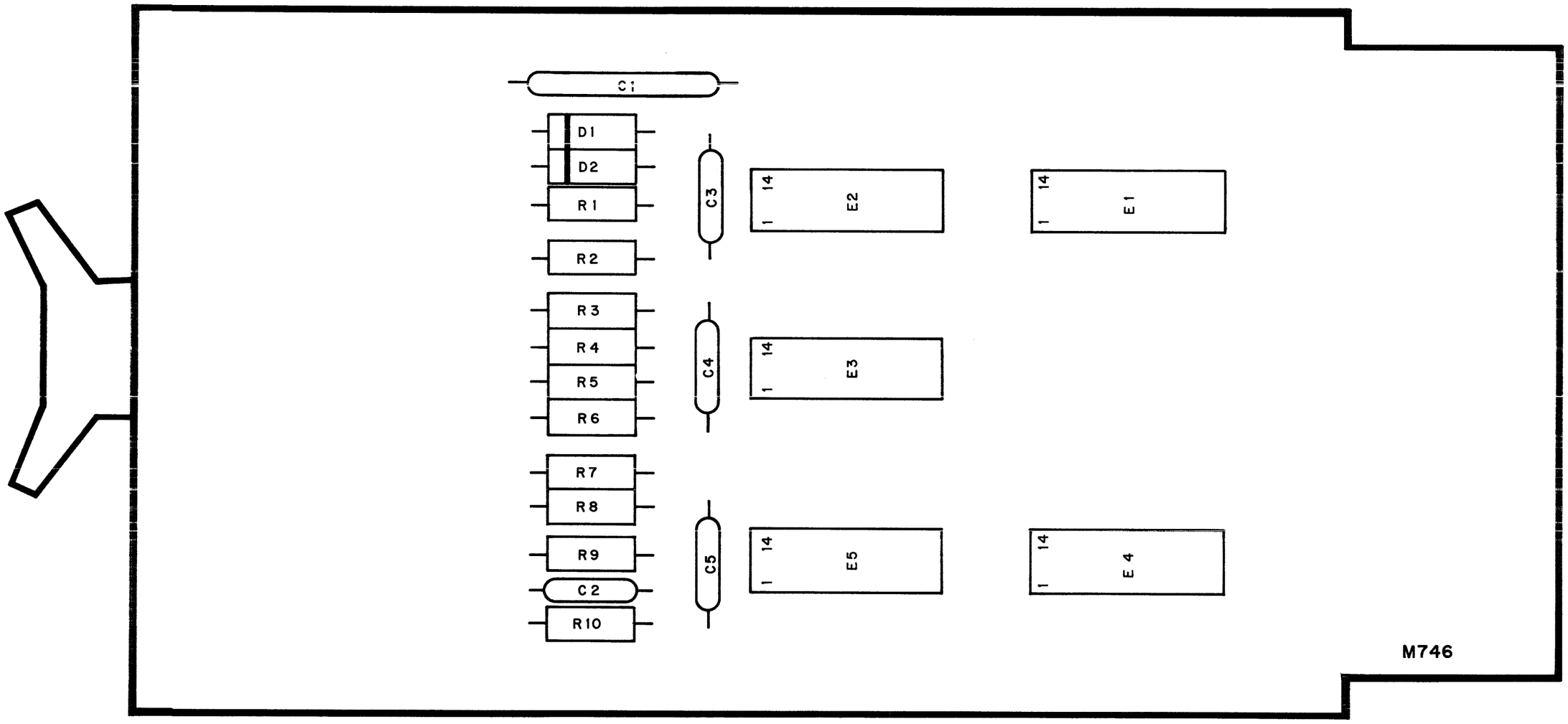
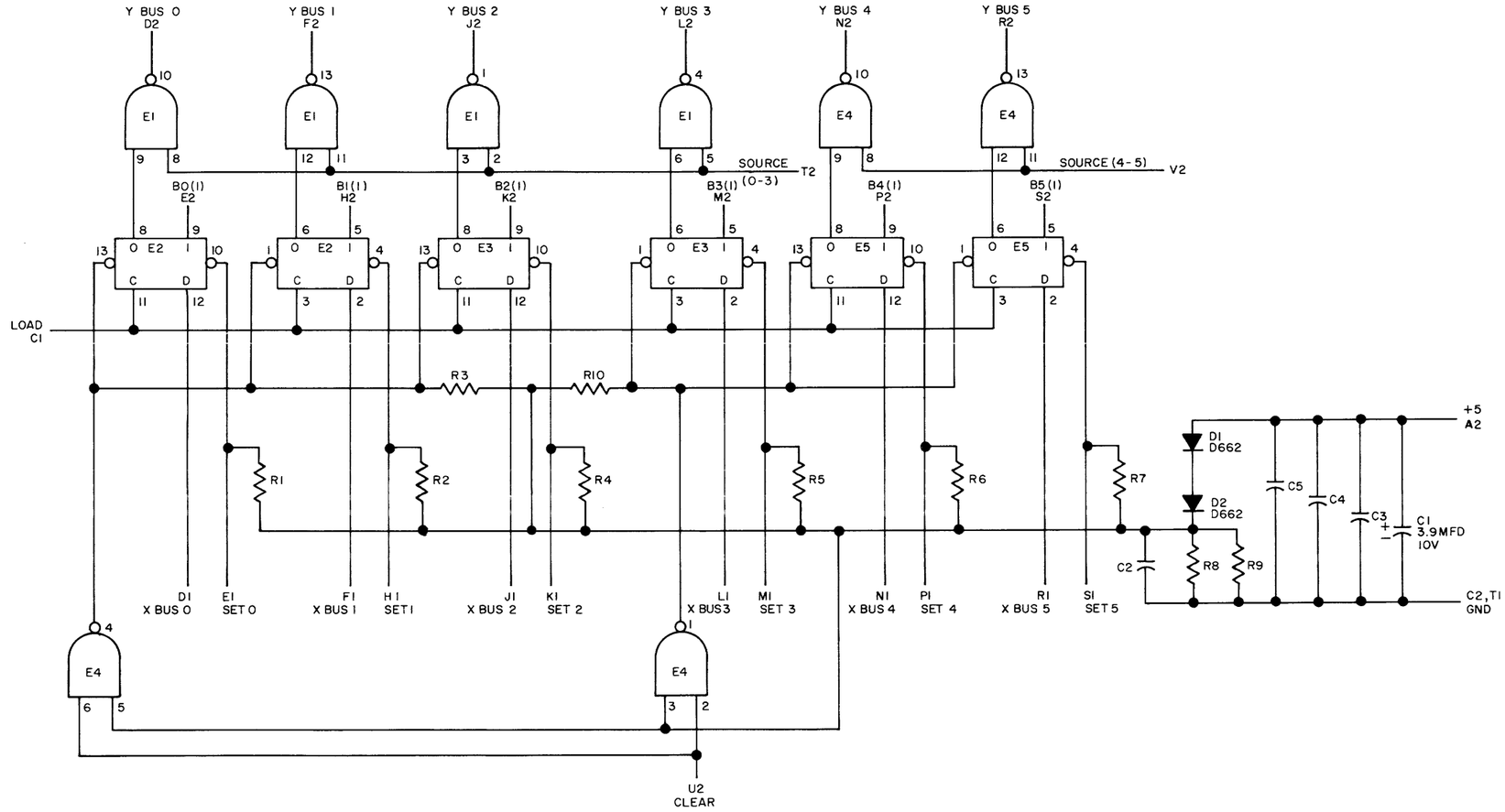


Figure II-16 Bus Register M746 Component Locations



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1/4W, 10%, 2.2K
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1 AND E4 ARE DEC 7401N
E2, E3 AND E5 ARE DEC7474N
CAPACITORS ARE .01 MFD, 100V, 20%, DISC

Figure II-17 Bus Register M746 Circuit Schematic

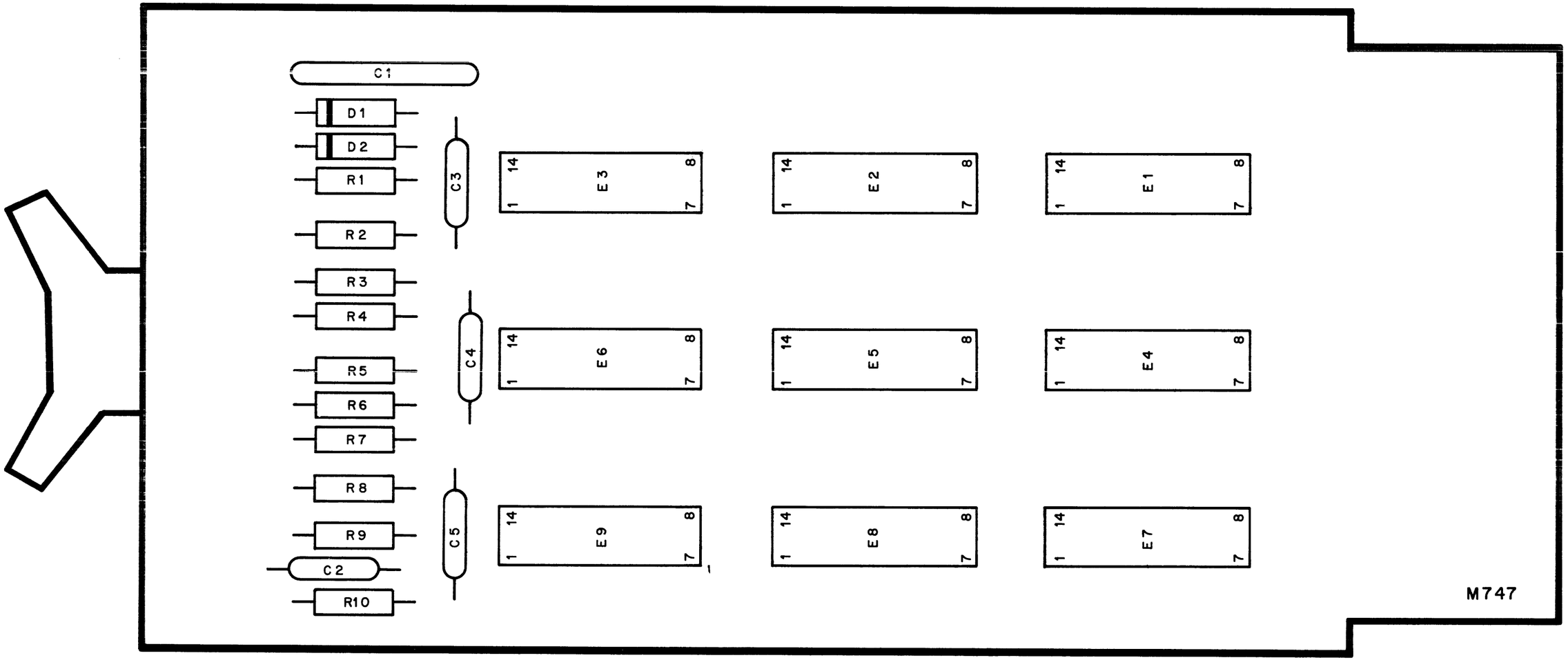
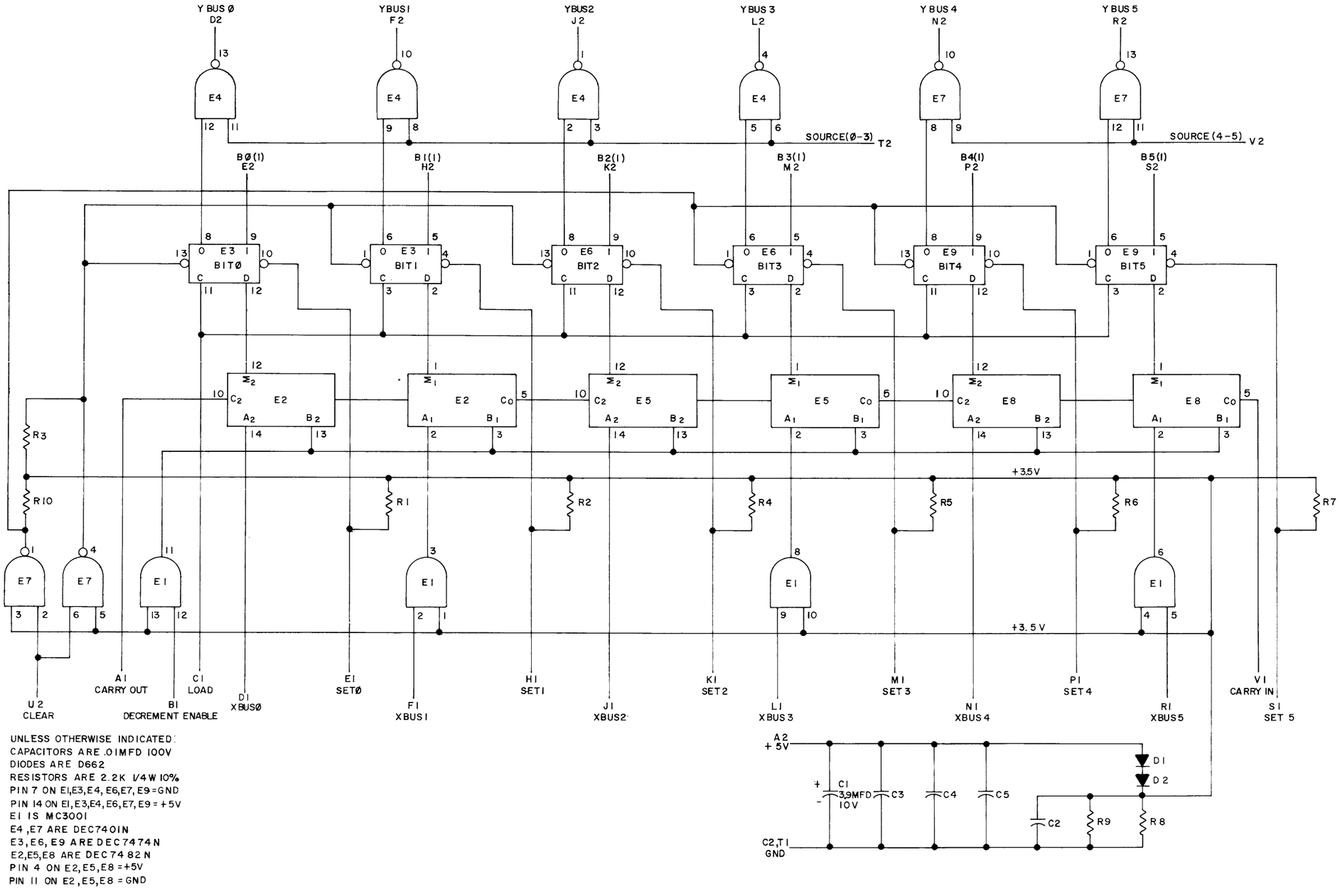
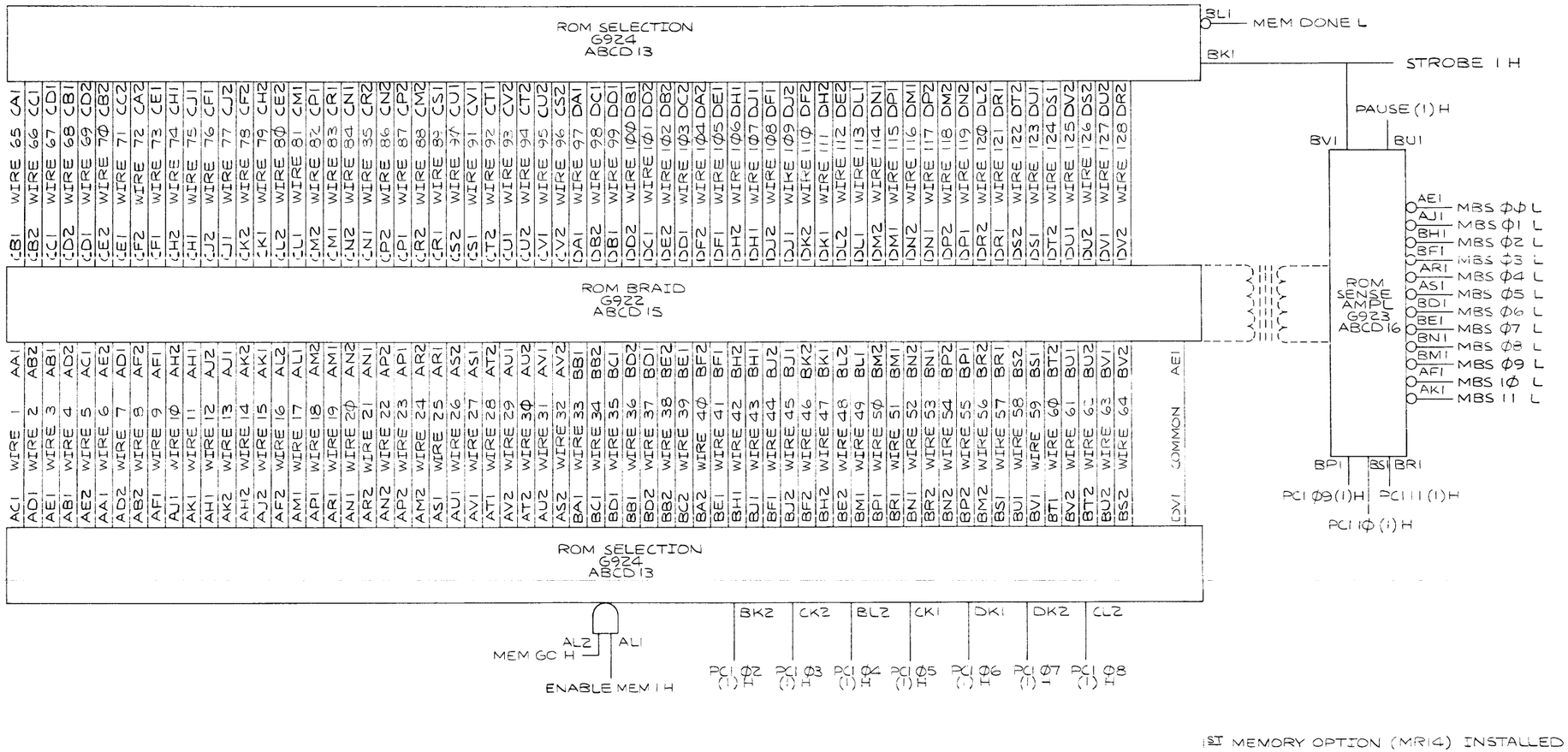


Figure II-18 Incrementing Bus Register M747 Component Location



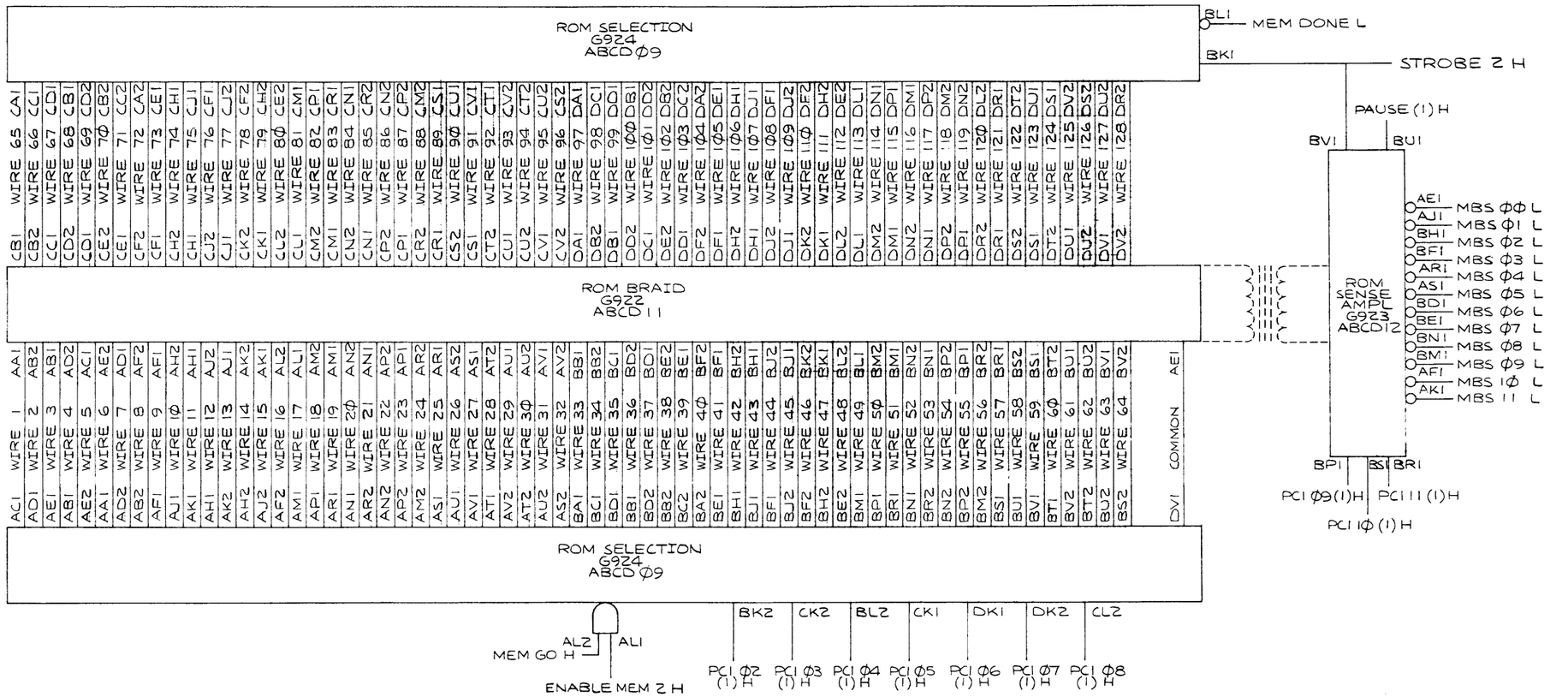
UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD 100V
DIODES ARE D662
RESISTORS ARE 2.2K 1/4W 10%
PIN 7 ON E1,E3,E4, E6,E7, E9=GND
PIN 14 ON E1, E3,E4, E6, E7, E9 = +5V
E1 IS MC3001
E4 ,E7 ARE DEC7401N
E3, E6, E9 ARE DEC7474N
E2,E5,E8 ARE DEC7482N
PIN 4 ON E2, E5, E8 =+5V
PIN 11 ON E2, E5, E8 = GND

Figure II-19 Incrementing Bus Register M747 Circuit Schematic



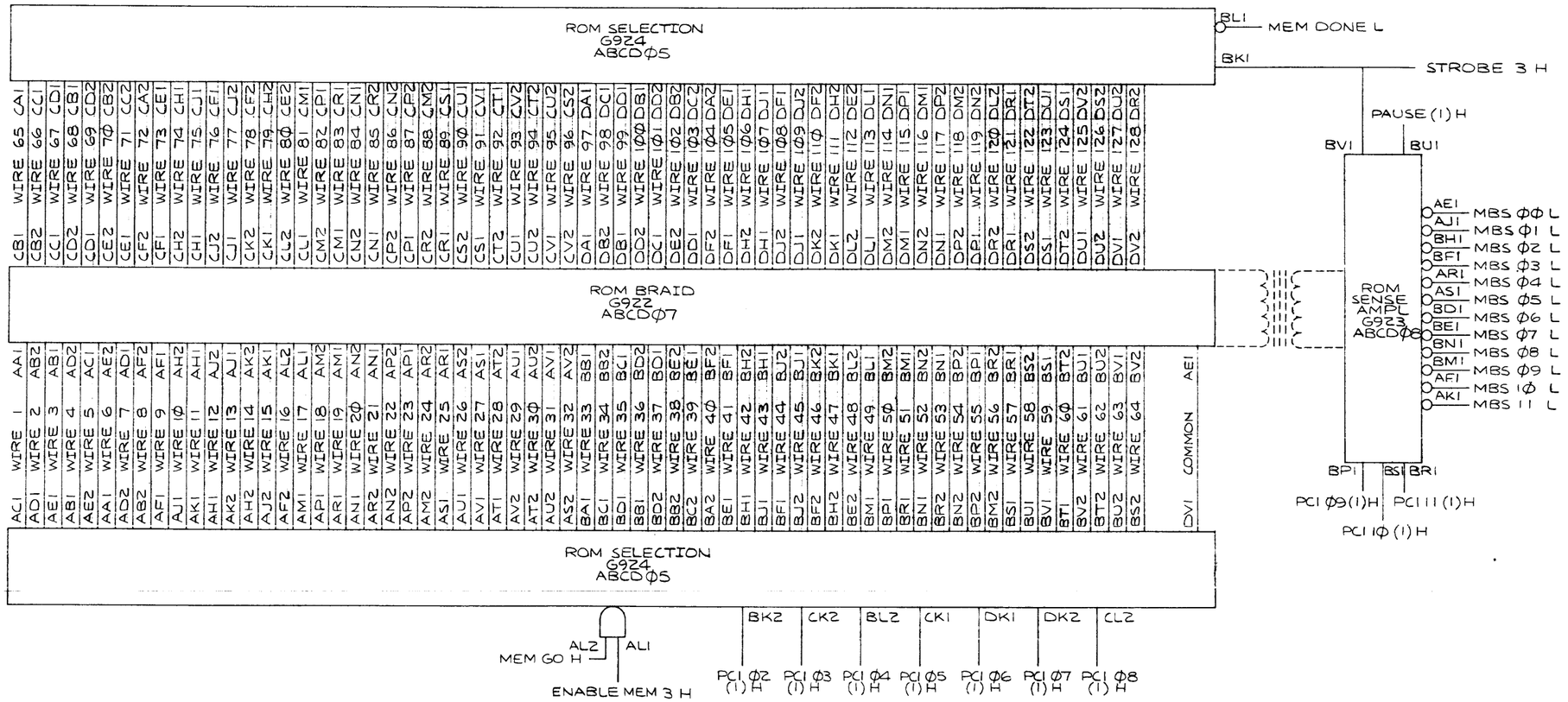
1ST MEMORY OPTION (MR14) INSTALLED

Figure II-20 Memory (1K) First Memory (MR14) Installed



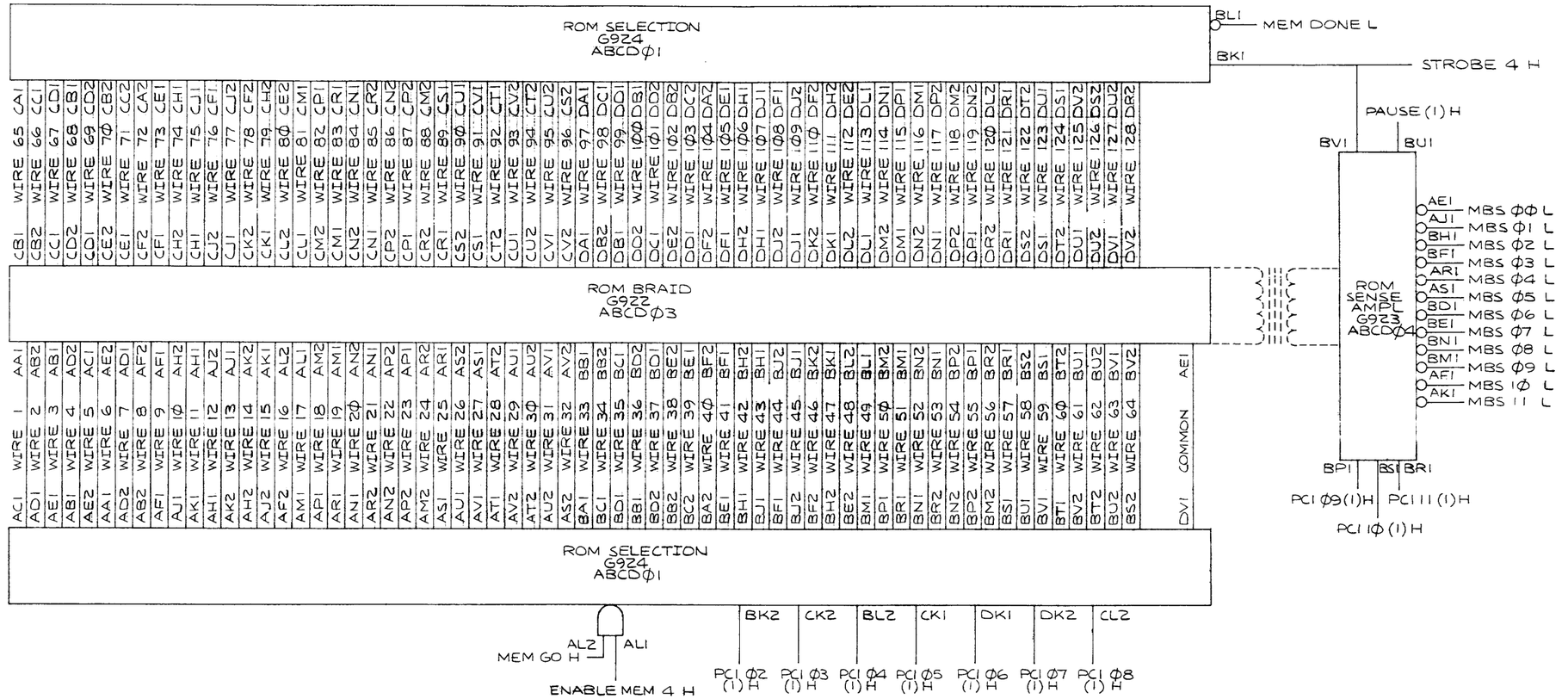
2ND MEMORY OPTION (MR14) INSTALLED

Figure II-21 Memory (1K) Second Memory (MR14) Option Installed Block Schematic



3RD MEMORY OPTION (MR14) INSTALLED

Figure II-22 Memory (1K) Third Memory (MR14) Option Installed Block Schematic



4TH MEMORY OPTION (MR14) INSTALLED

Figure II-23 Memory (1K) Fourth Memory (MR14) Option Installed Block Schematic

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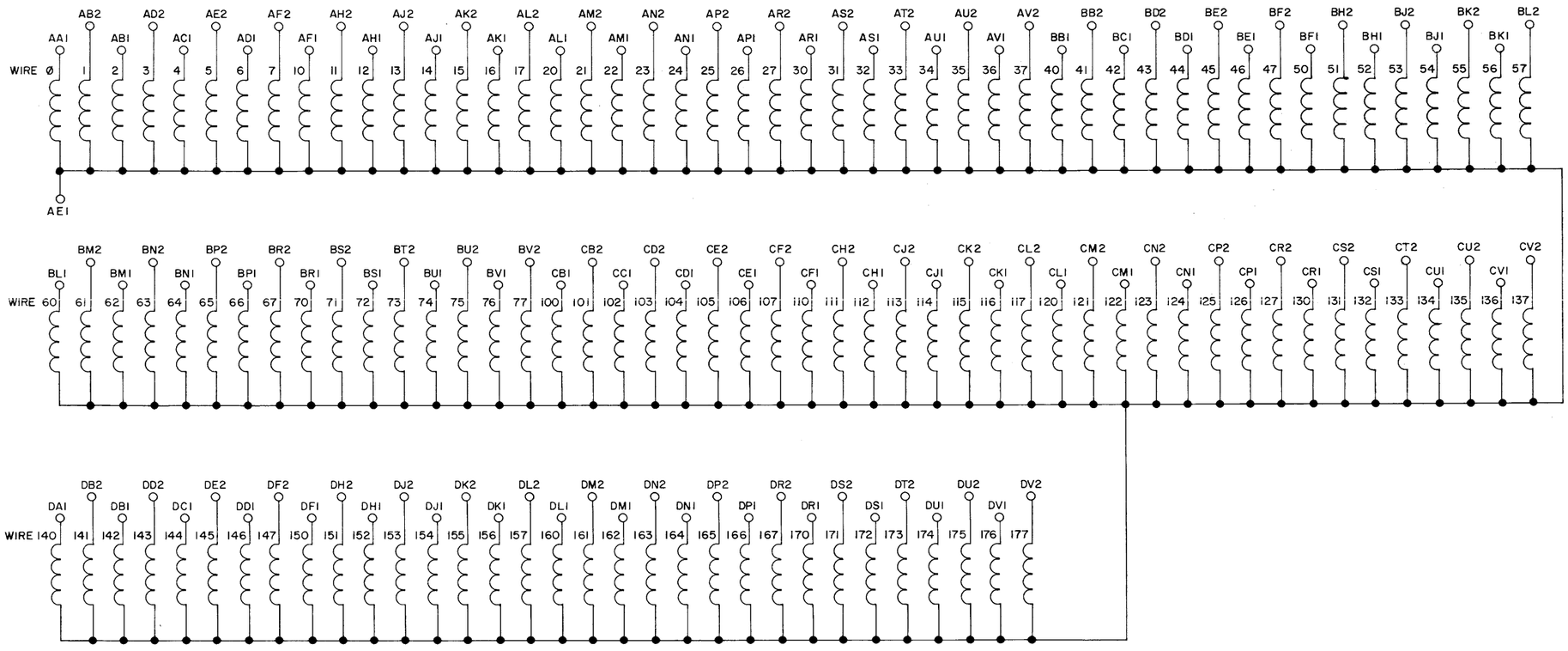
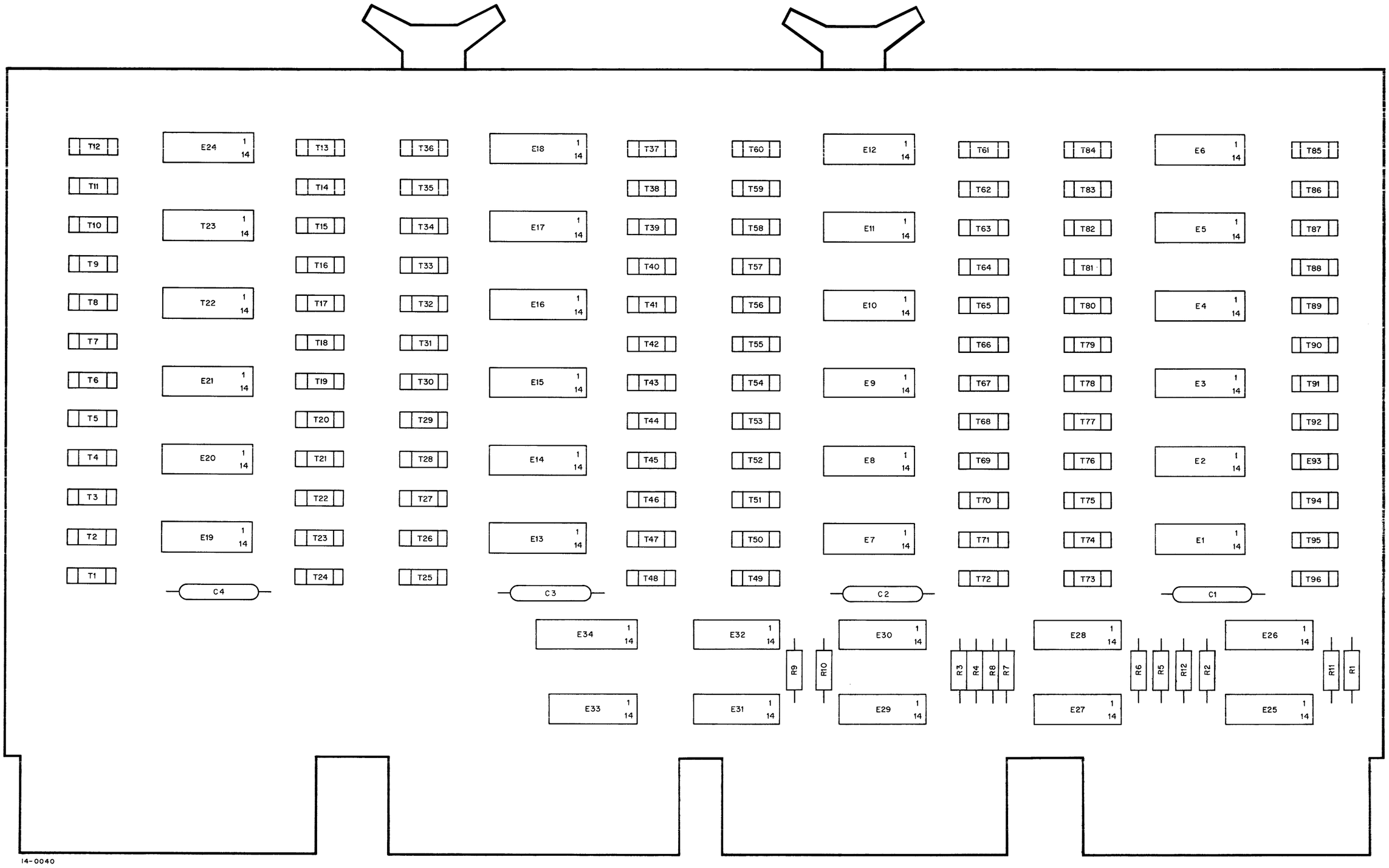


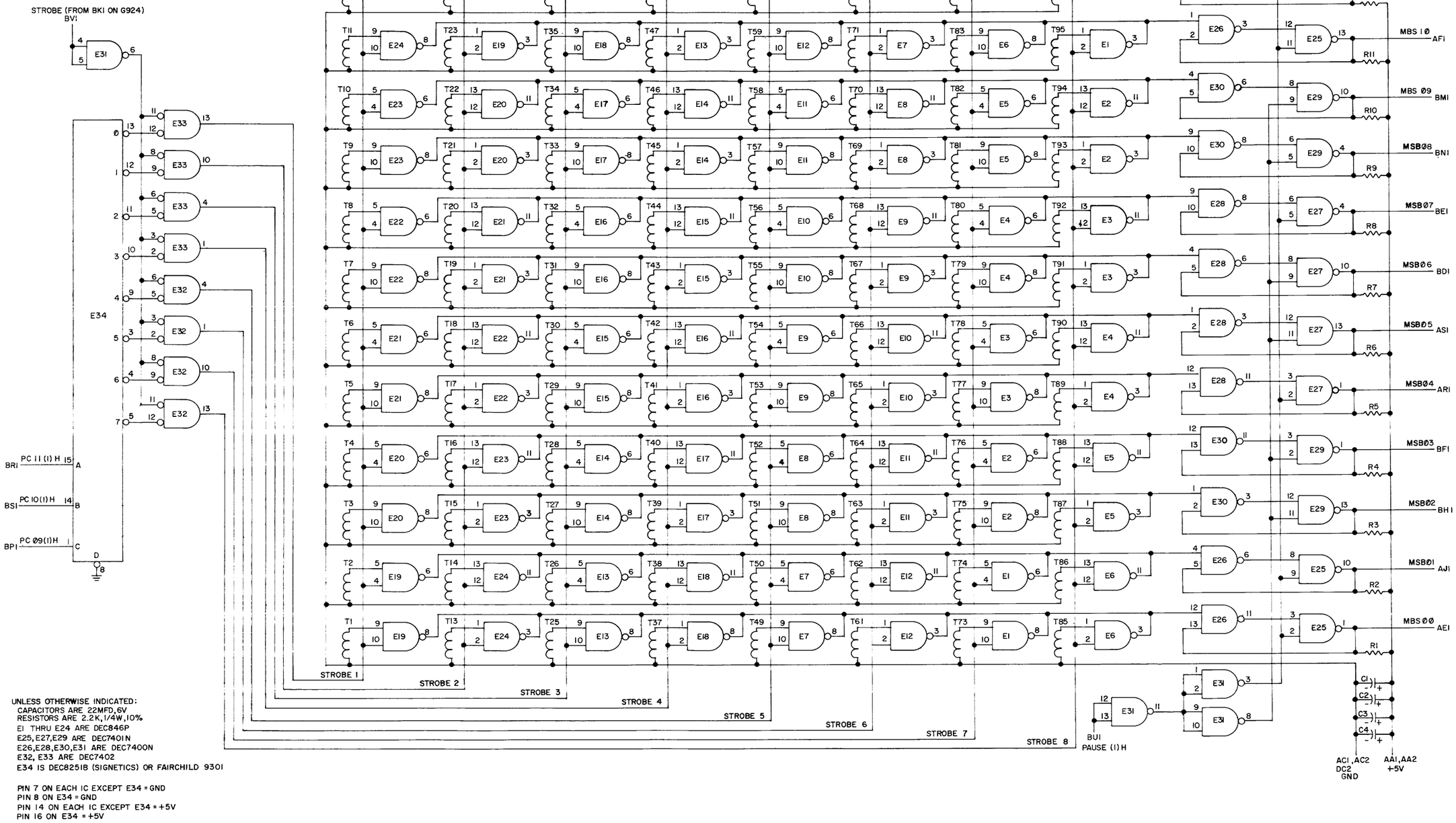
UNLESS OTHERWISE INDICATED:
COMPONENTS TO BE INSTALLED BY BRAID MANUFACTURERS

Figure II-24 ROM Braid Board G922 Circuit Schematic



14-0040

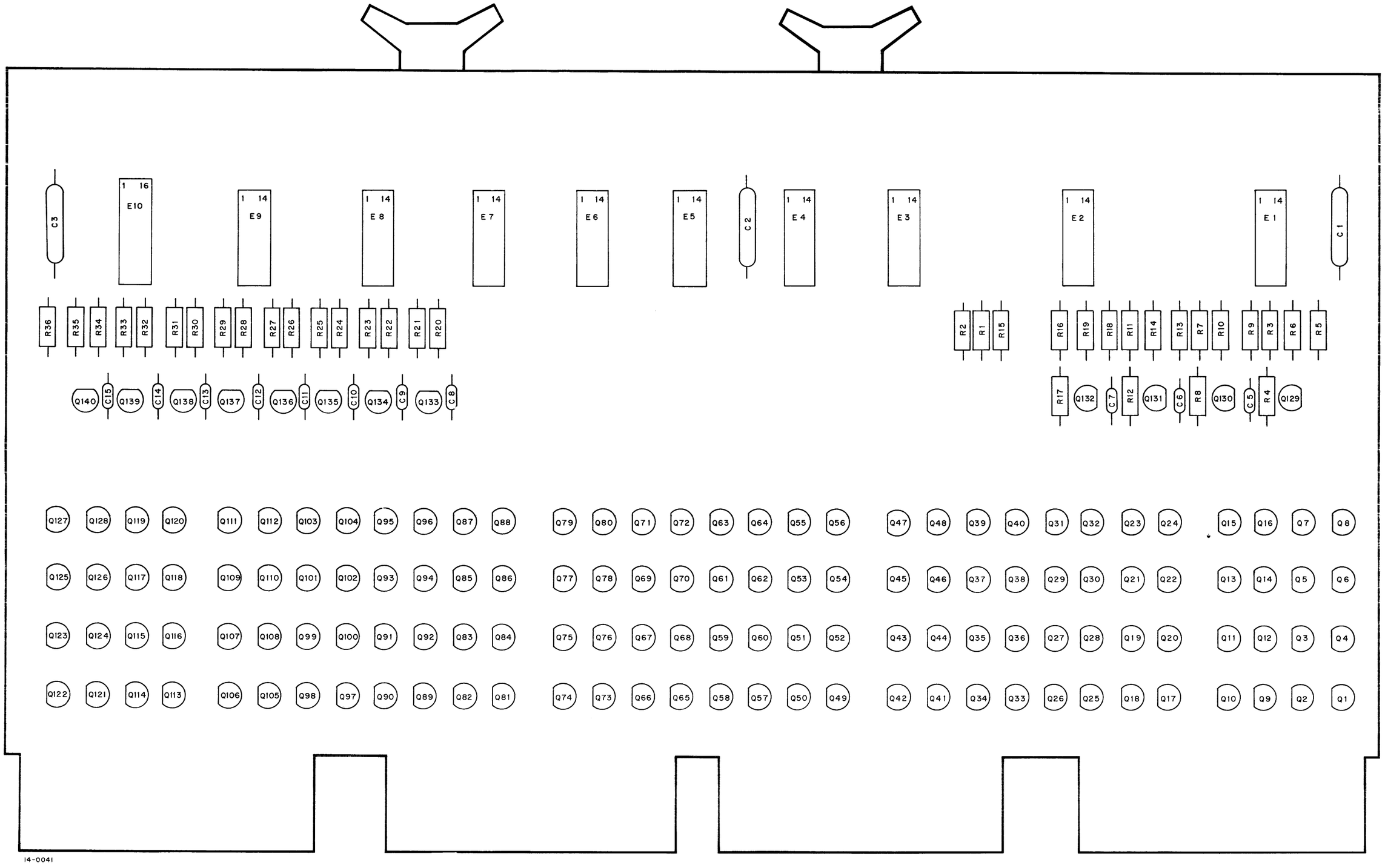
Figure II-25 ROM Sense Amplifier G923 Component Locations



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 22MFD, 6V
RESISTORS ARE 2.2K, 1/4W, 10%
E1 THRU E24 ARE DEC846P
E25, E27, E29 ARE DEC7401N
E26, E28, E30, E31 ARE DEC7400N
E32, E33 ARE DEC7402
E34 IS DEC8251B (SIGNETICS) OR FAIRCHILD 9301

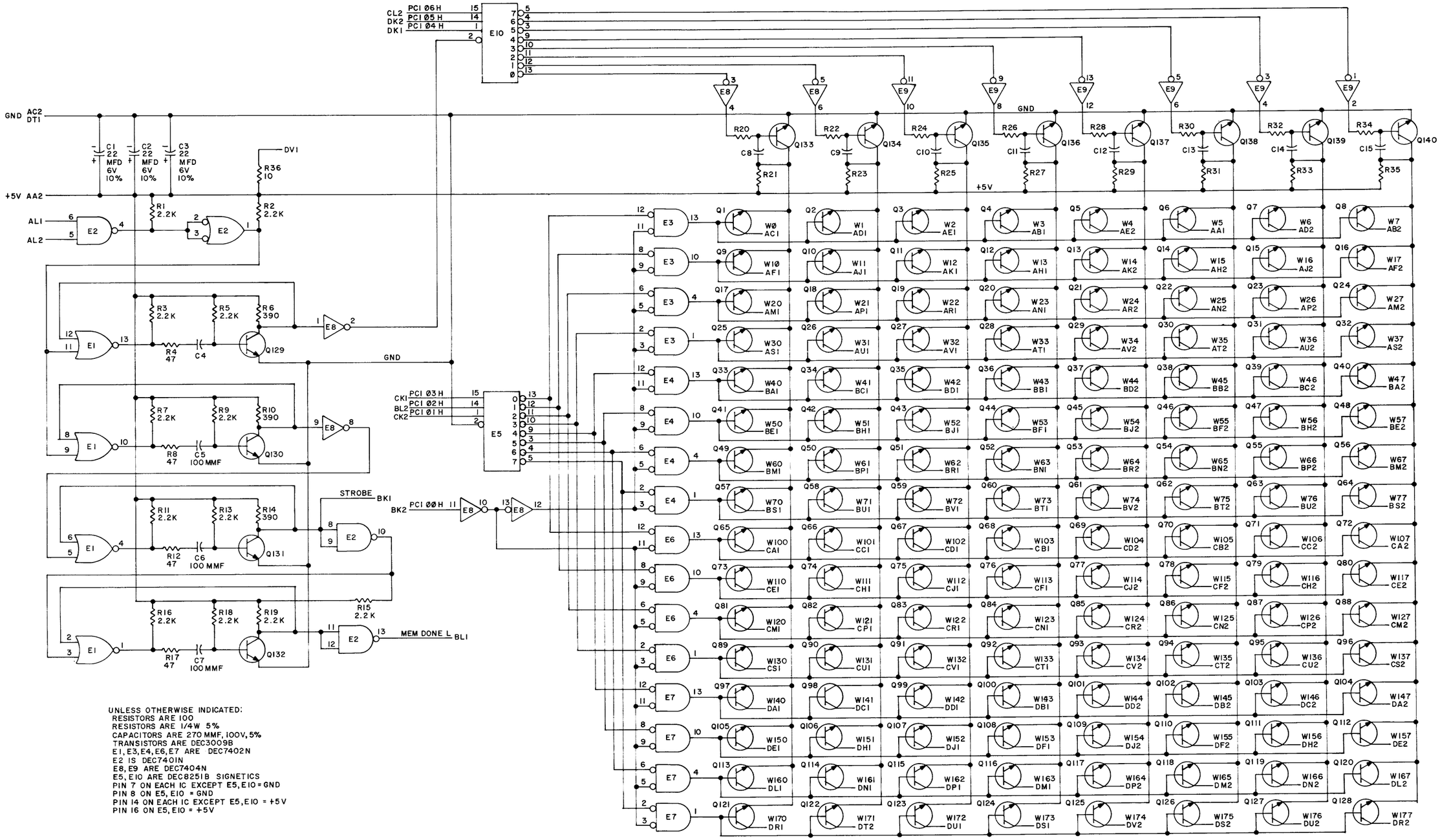
PIN 7 ON EACH IC EXCEPT E34 = GND
PIN 8 ON E34 = GND
PIN 14 ON EACH IC EXCEPT E34 = +5V
PIN 16 ON E34 = +5V

Figure II-26 ROM Sense Amplifier G923 Circuit Schematic



14-0041

Figure II-27 ROM Selection G924 Component Locations



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 10Ω
RESISTORS ARE 1/4W 5%
CAPACITORS ARE 270 MMF, 100V, 5%
TRANSISTORS ARE DEC3009B
E1, E3, E4, E6, E7 ARE DEC7402N
E2 IS DEC7401N
E8, E9 ARE DEC7404N
E5, E10 ARE DEC8251B SIGNETICS
PIN 7 ON EACH IC EXCEPT E5, E10 = GND
PIN 8 ON E5, E10 = GND
PIN 14 ON EACH IC EXCEPT E5, E10 = +5V
PIN 16 ON E5, E10 = +5V

Figure II-28 ROM Selection G924 Circuit Schematic

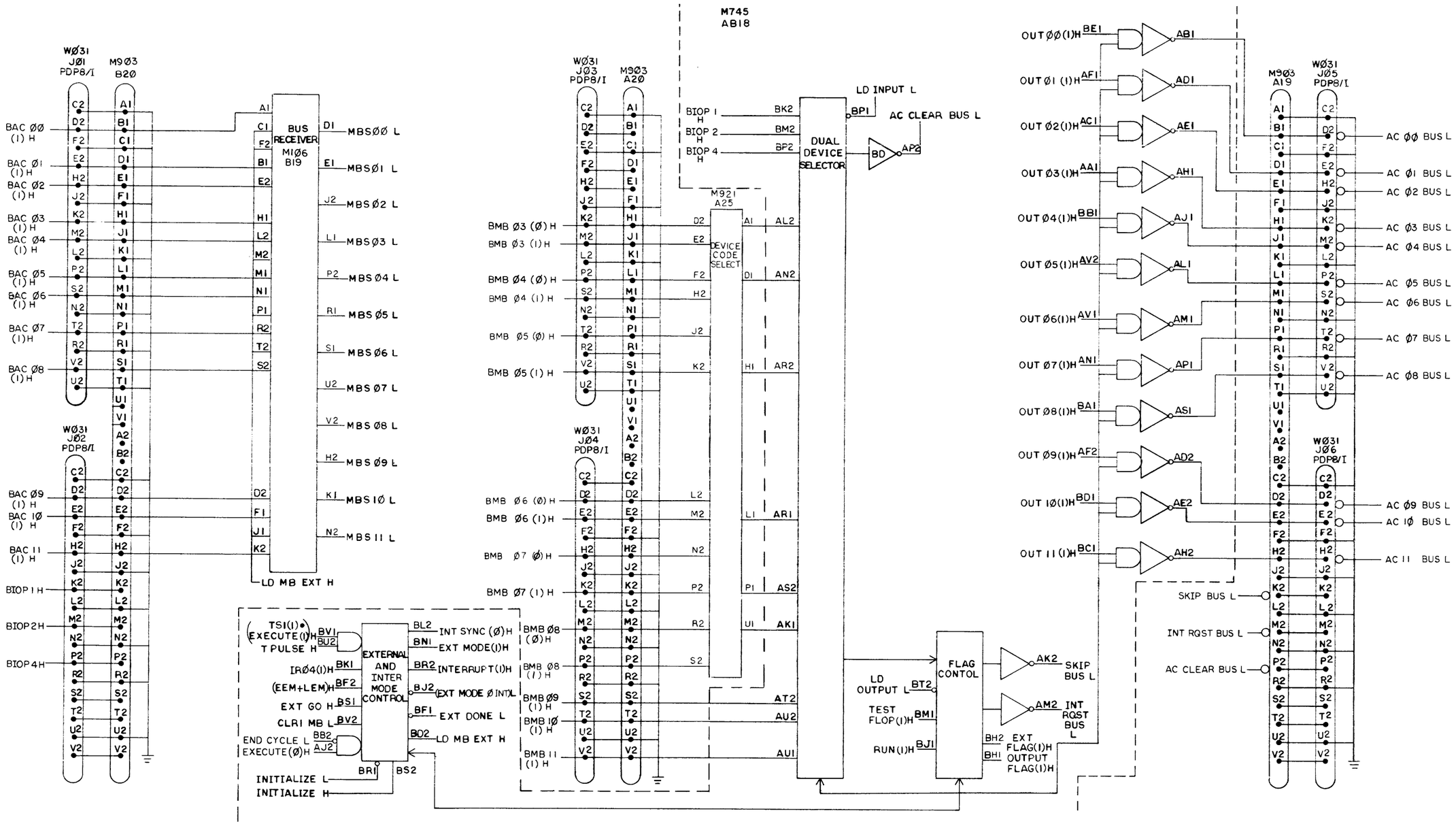


Figure II-29 PDP-8/I Interface to PDP-14 Block Schematic

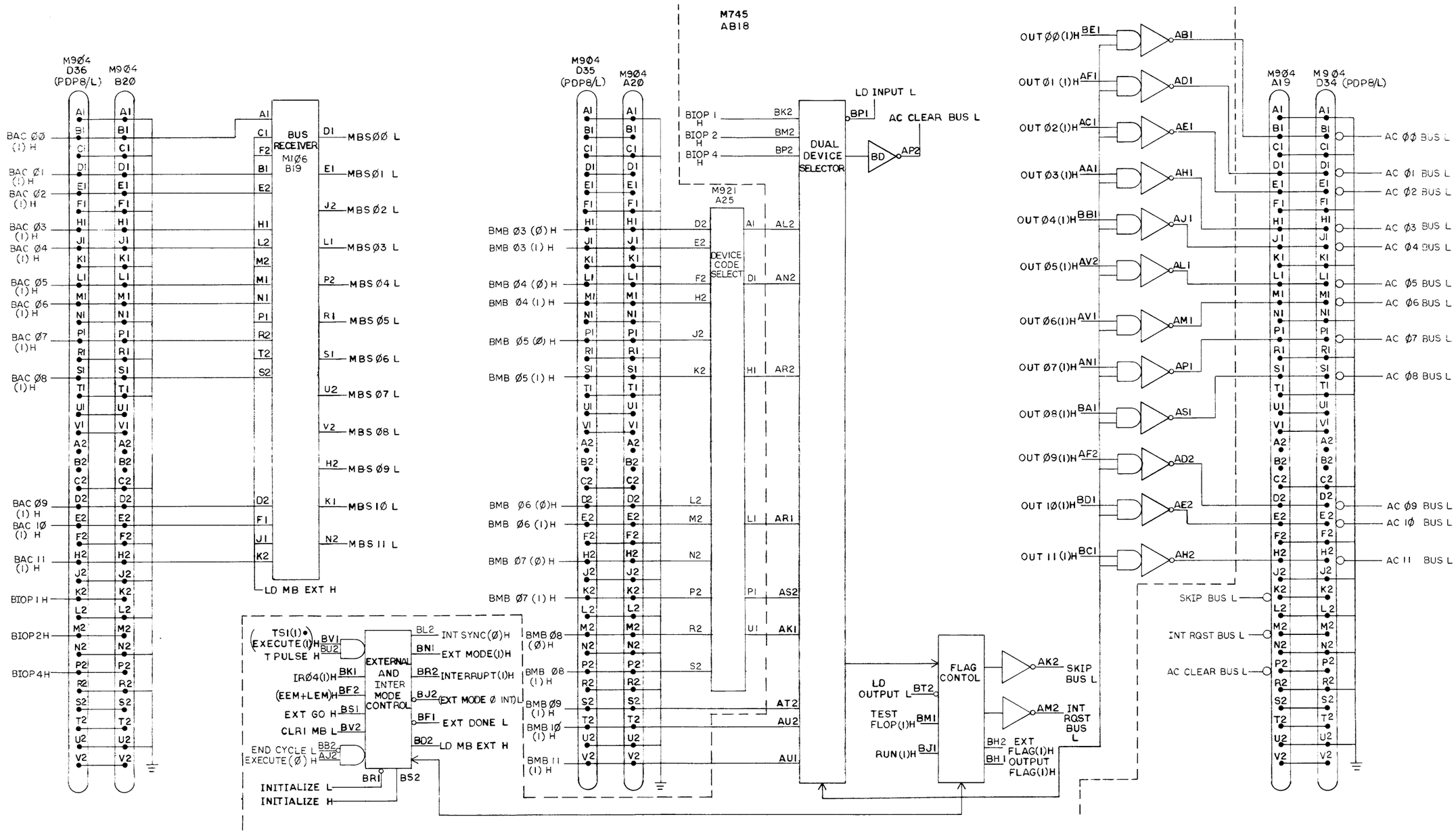


Figure II-30 PDP-8/L Interface to PDP-14 Block Schematic

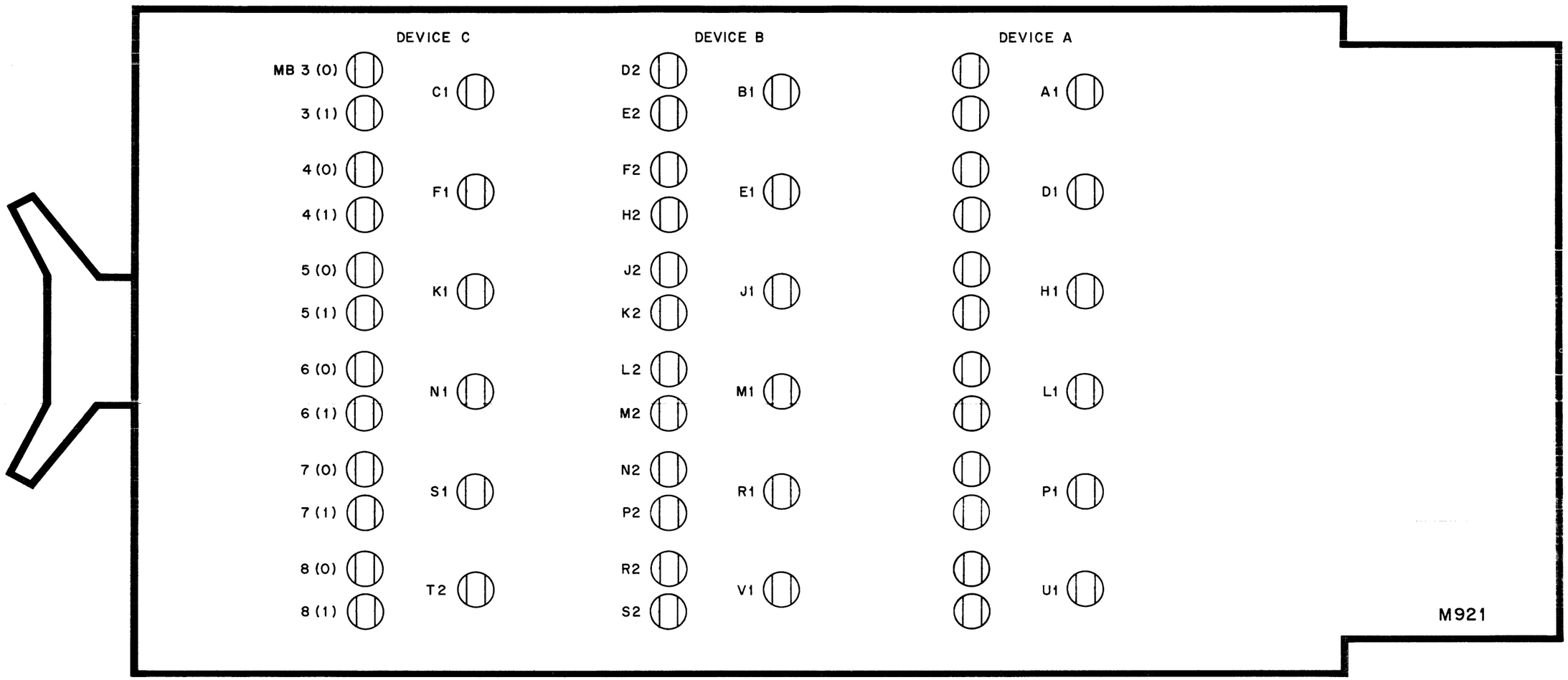


Figure II-31 Device Code Select Jumper Board Component Location

PIN SIGNAL ASSIGNMENTS

OUT			
DEVICE A	DEVICE B	DEVICE C	SIGNAL
AI	BI	CI	MB3
DI	EI	FI	MB4
HI	JI	KI	MB5
LI	MI	NI	MB6
PI	RI	SI	MB7
UI	VI	T2	MB8

IN	
D2	MB3(0)
E2	MB3(1)
F2	MB4(0)
H2	MB4(1)
J2	MB5(0)
K2	MB5(1)
L2	MB6(0)
M2	MB6(1)
N2	MB7(0)
P2	MB7(1)
R2	MB8(0)
S2	MB8(1)

UNLESS OTHERWISE INDICATED:
⊘ ARE SPLIT LUGS

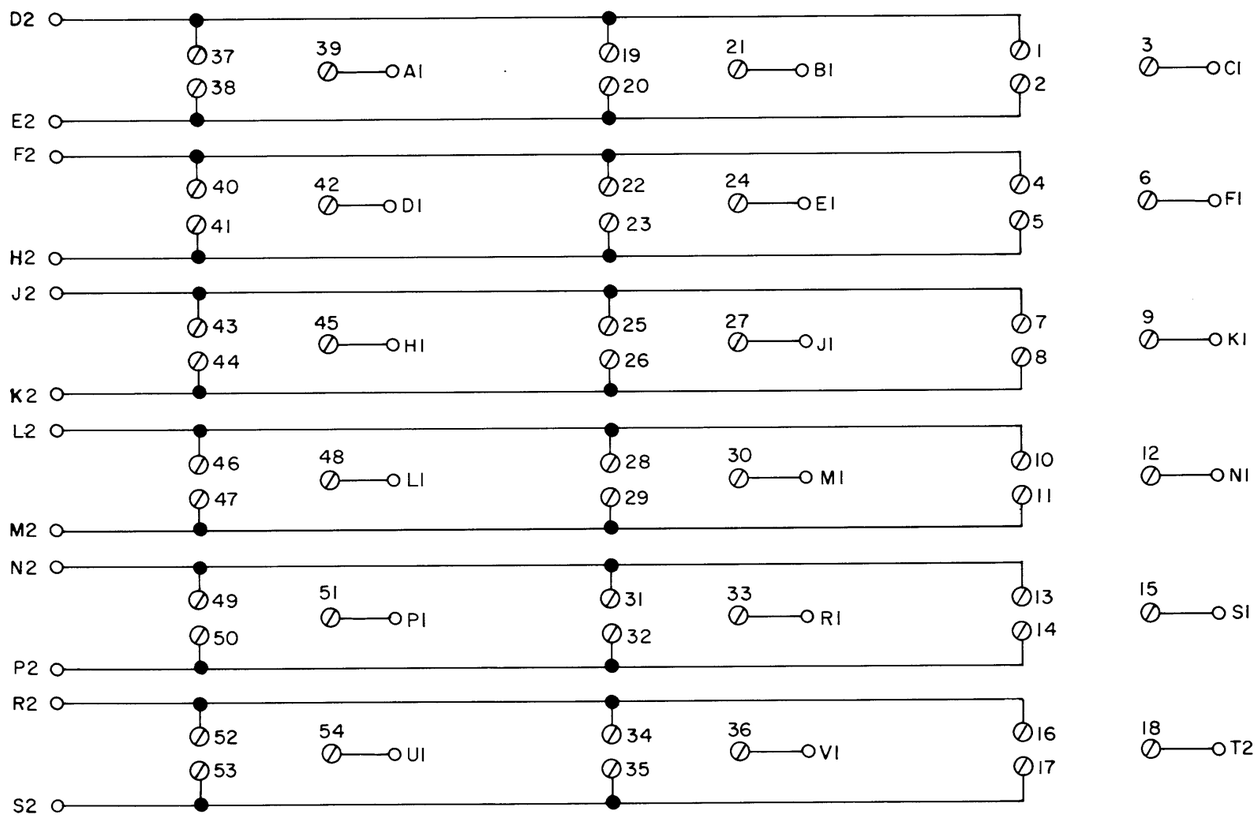


Figure II-32 Device Code Select Jumper Board Circuit Schematic

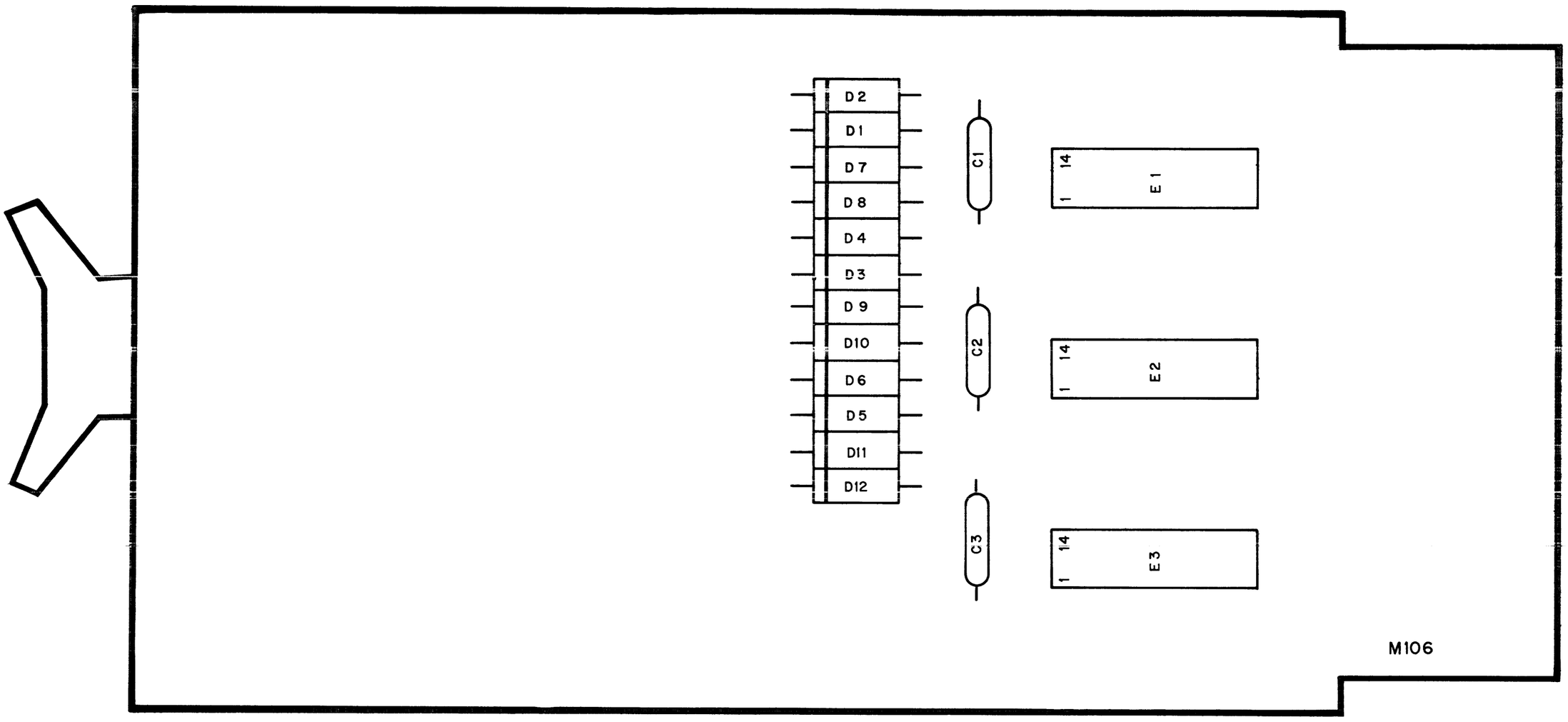


Figure II-33 Dot NOR Gates M106 Component Locations

UNLESS OTHERWISE INDICATED:
DIODES ARE D664
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
IC'S ARE DEC740IN

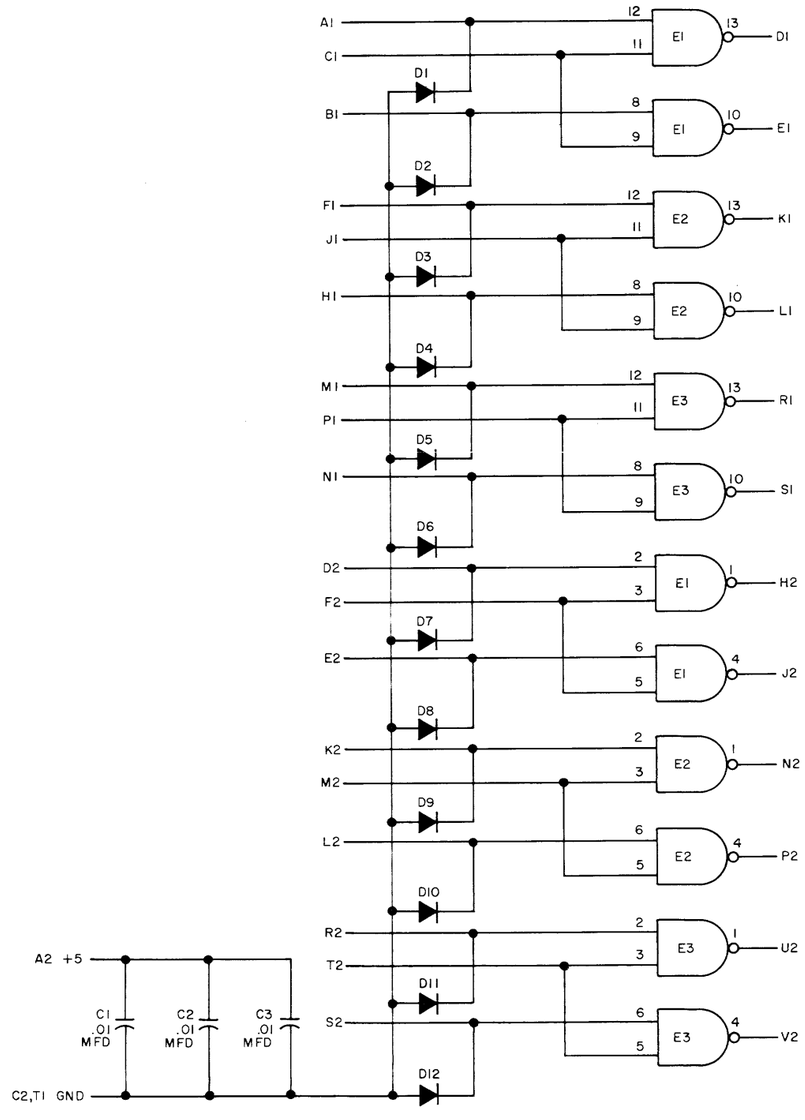


Figure II-34 Dot NOR Gates M106 Circuit Schematic

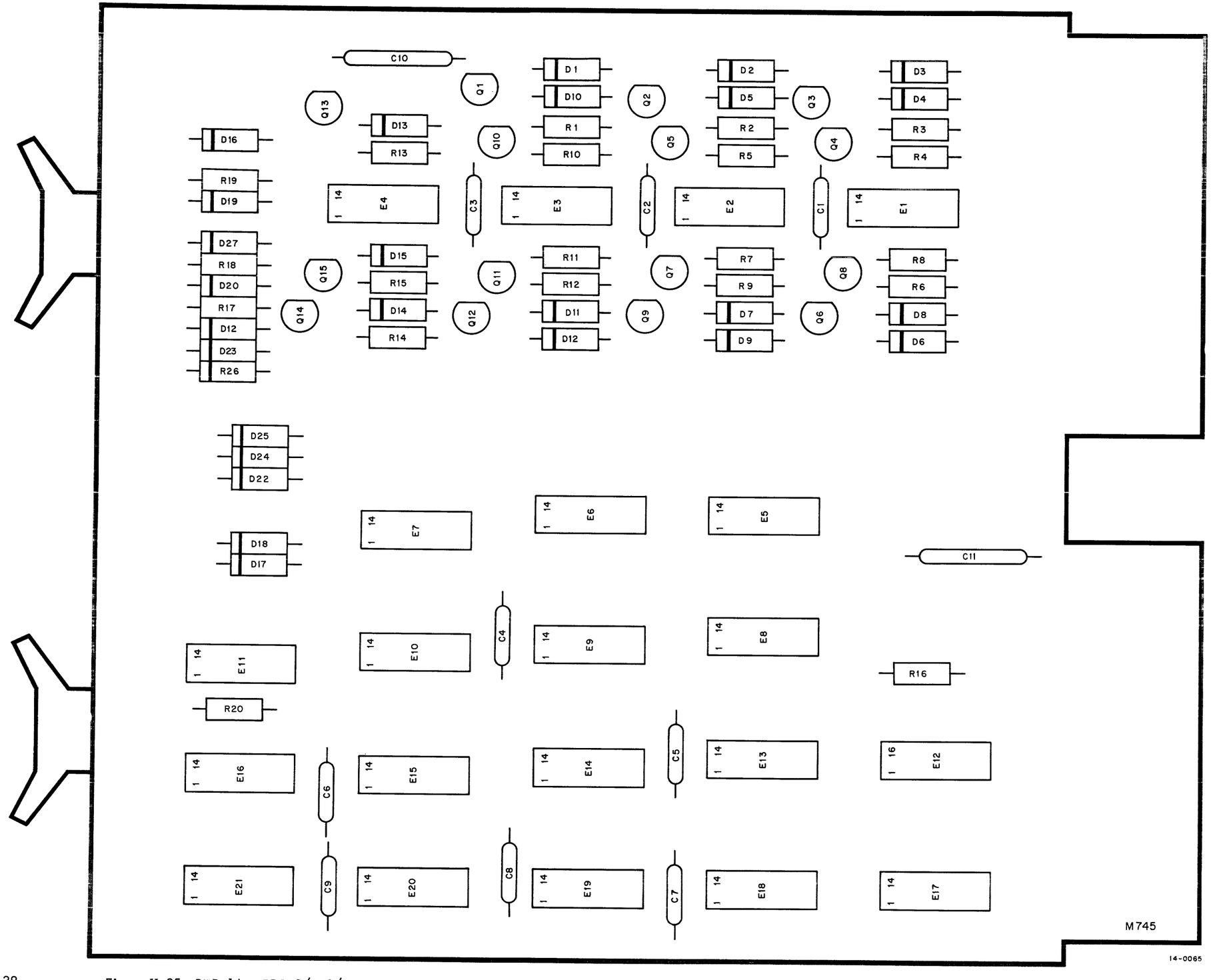


Figure II-35 PDP-14 to PDP-8/I, 8/L Interface M745 Component Location

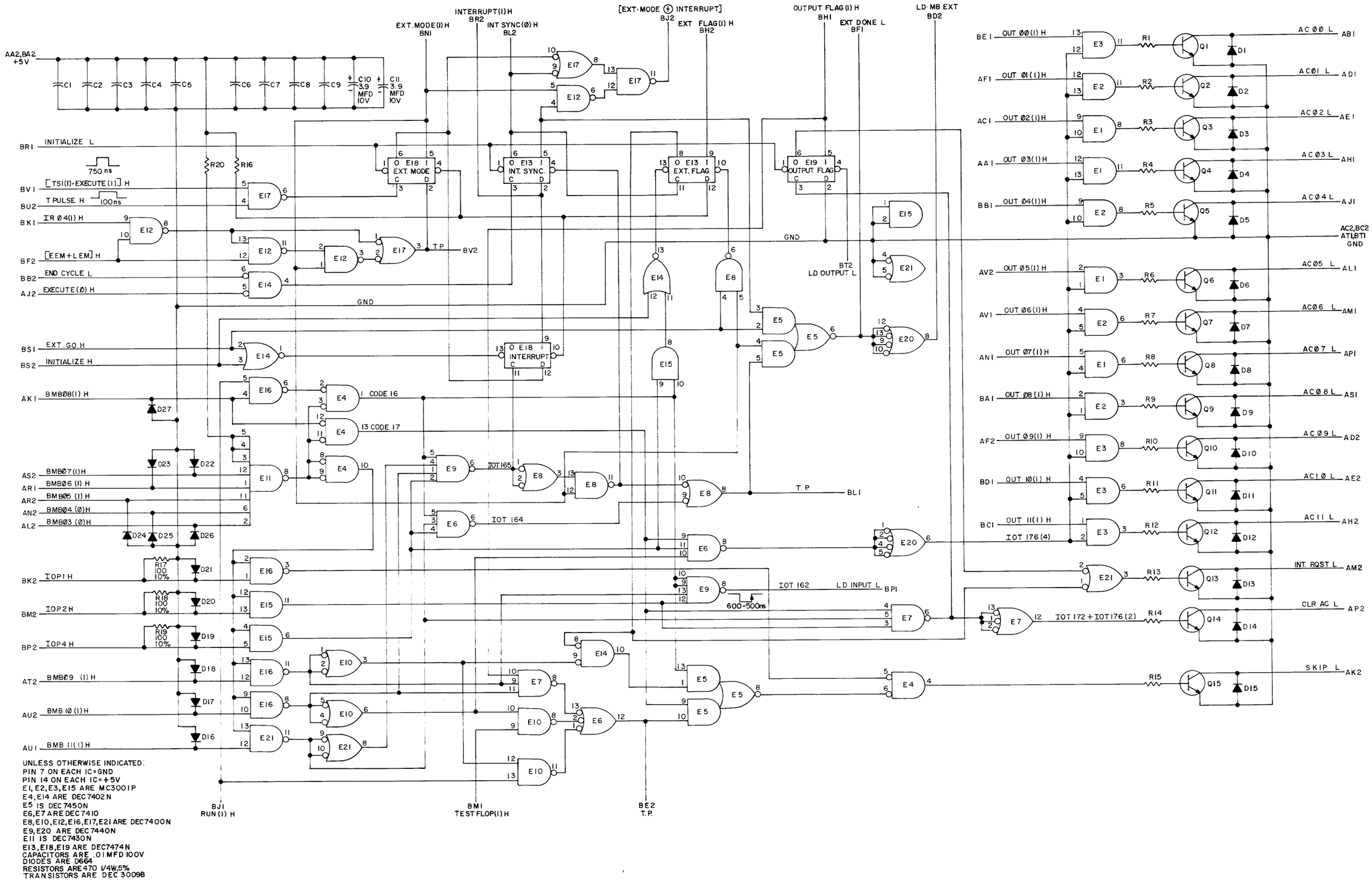


Figure II-36 PDP-14 to PDP-8/I, 8/L Interface Circuit Schematic

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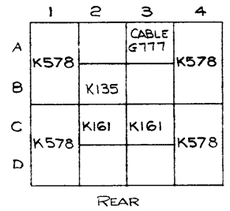


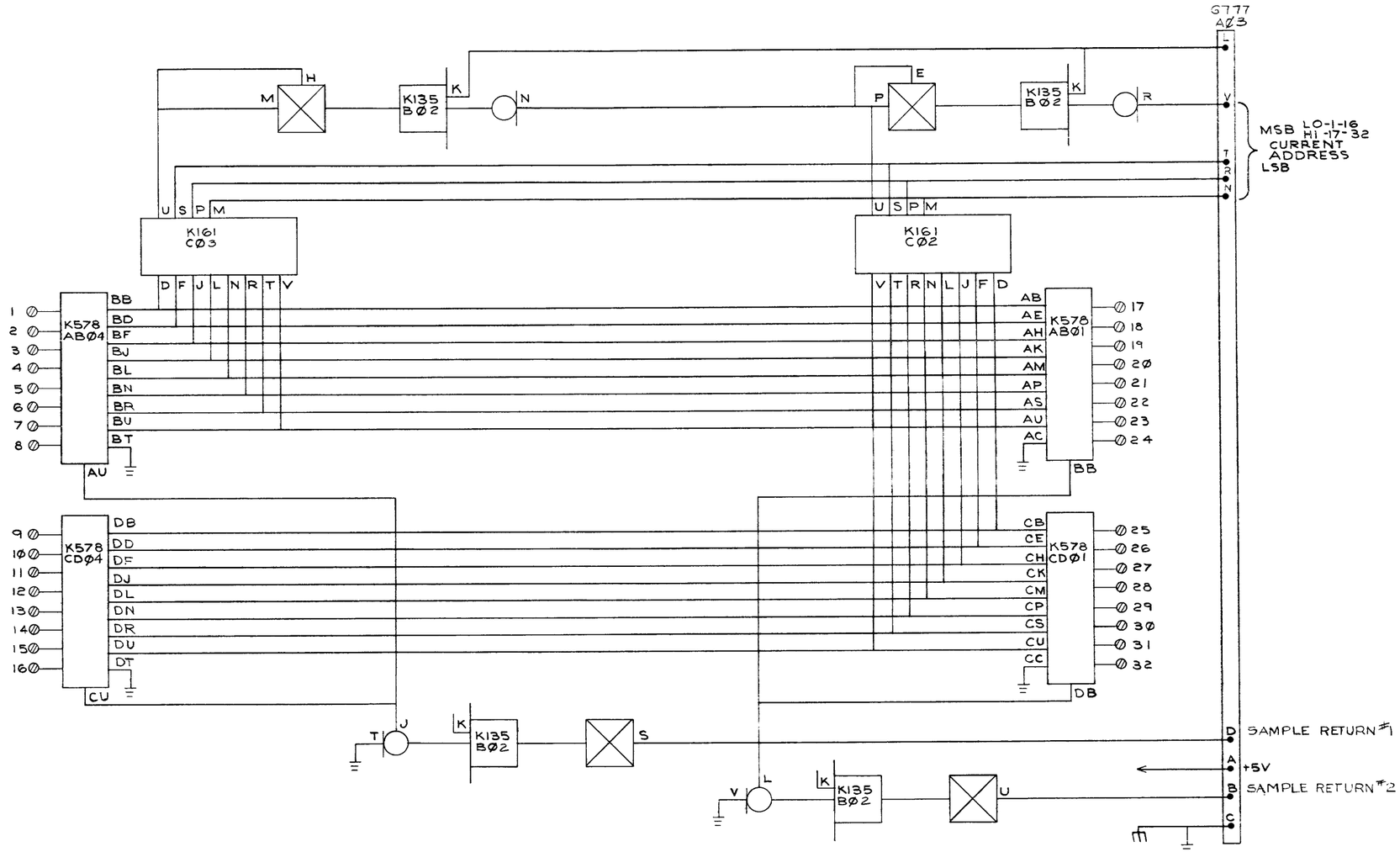
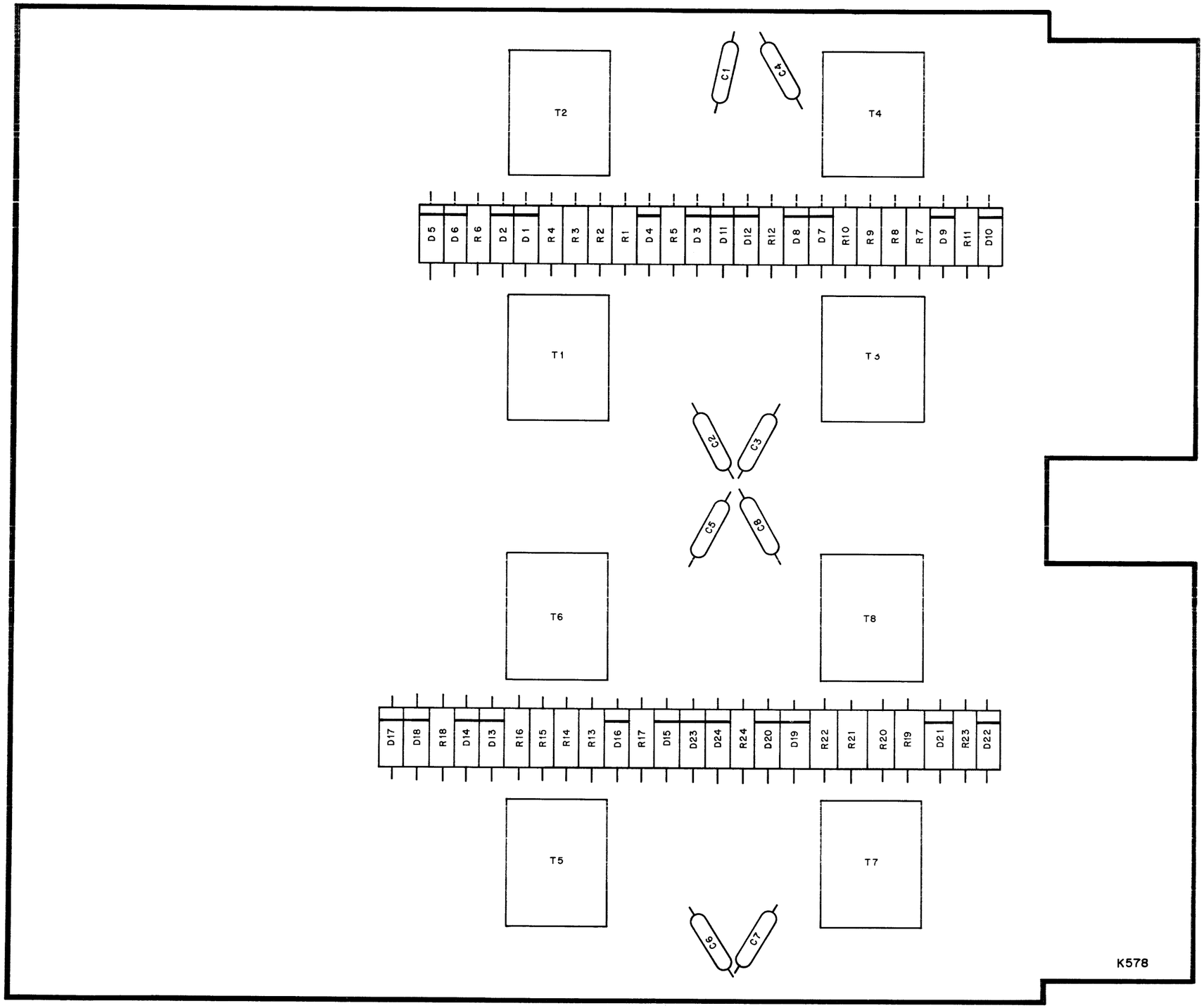
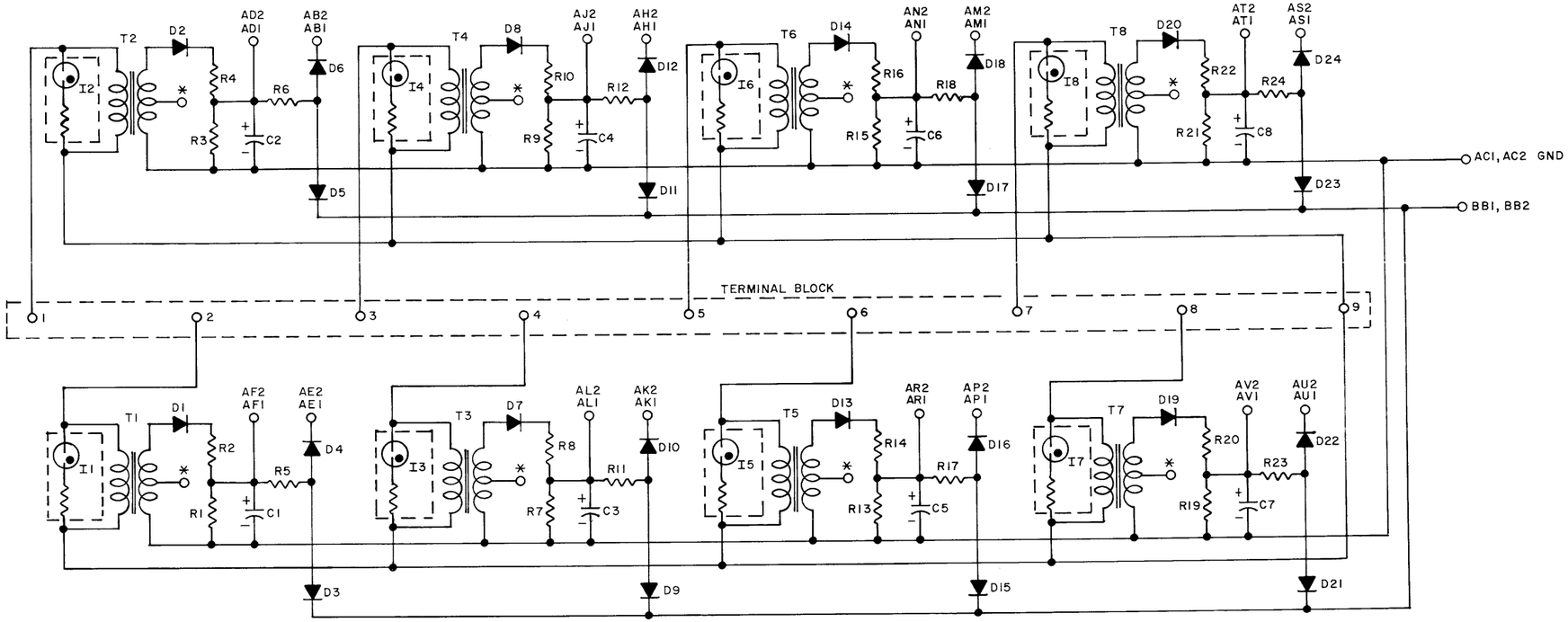


Figure II-37 Input Interface Box Block Schematic



14-0066

42 Figure II-38 AC Inputs K578 Component Locations



NOTE:
PINS WITH * ARE NOT USED

Figure II-39 AC Inputs K578 Circuit Schematic

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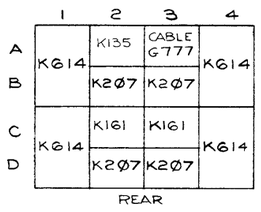
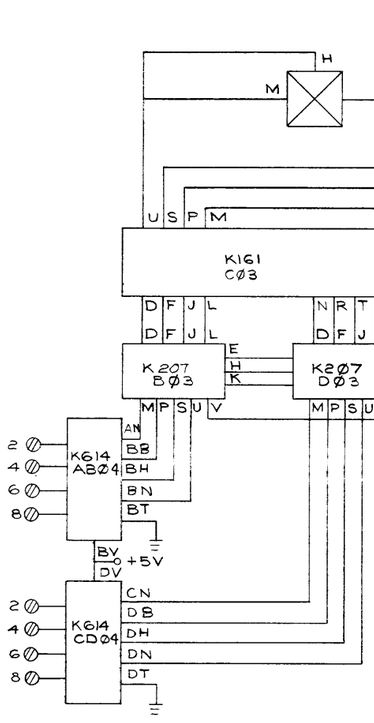




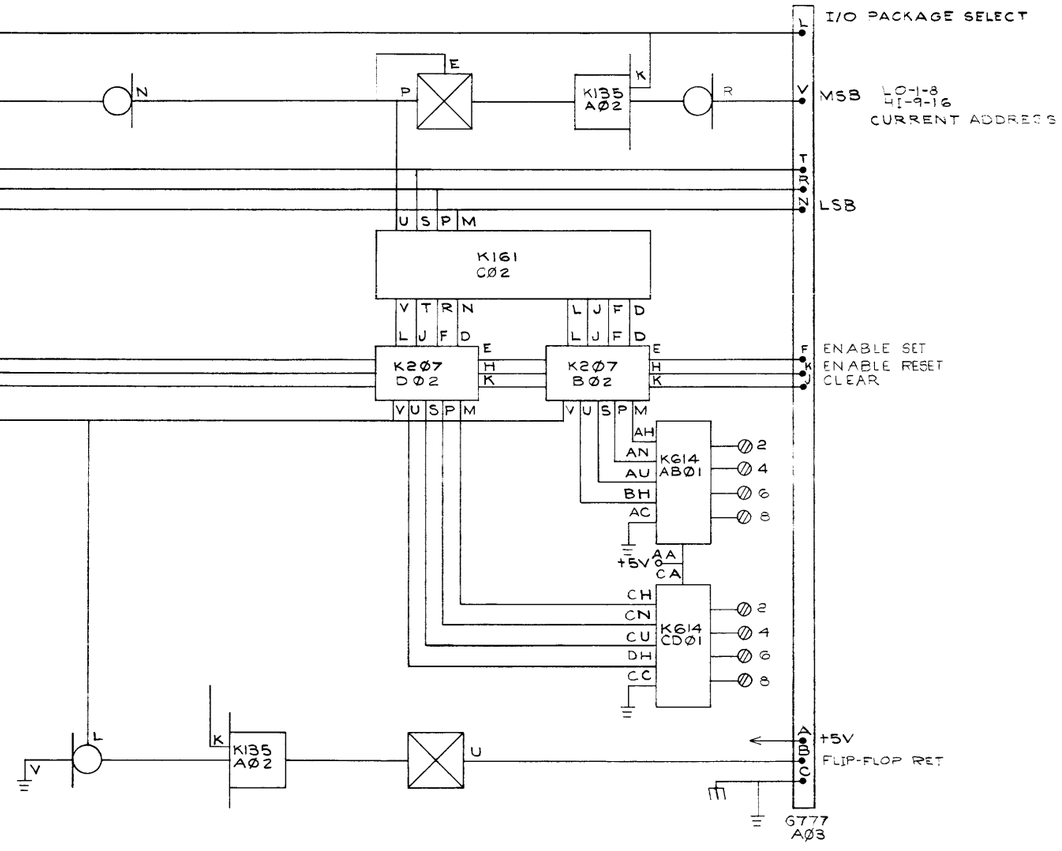
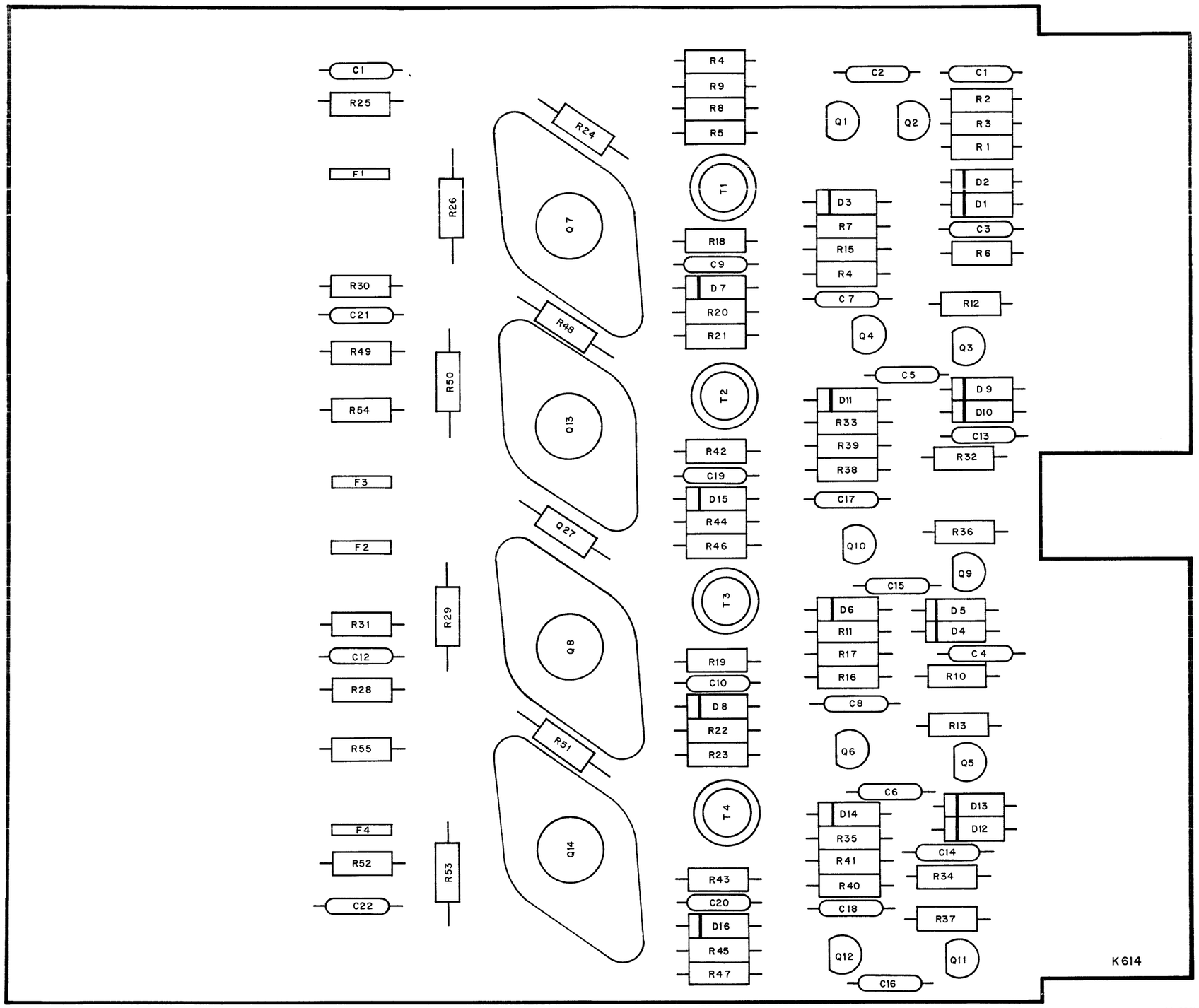


Figure II-40 Output Interface Box Block Schematic



14-0081

Figure II-41 Isolated AC Switch K614 Component Locations

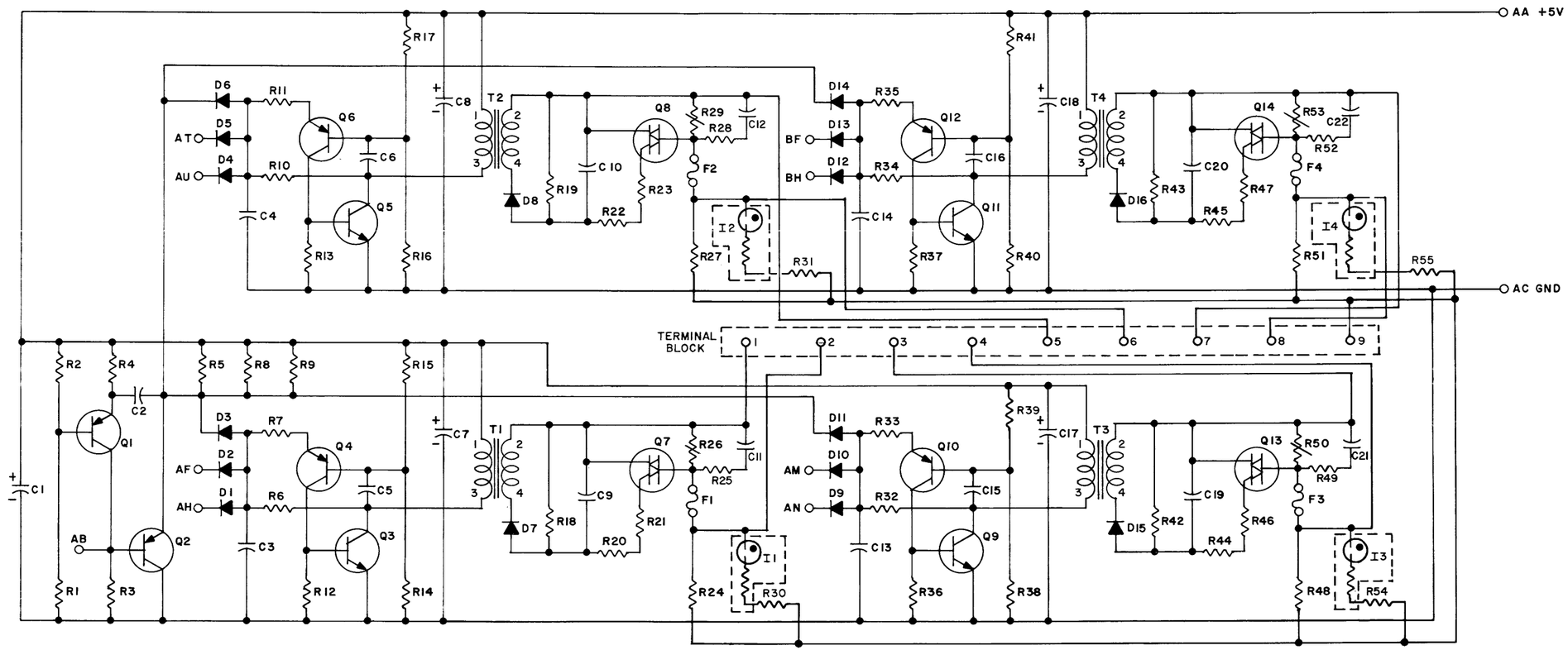


Figure II-42 Isolated AC Switch K614 Circuit Schematic

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	1	2	3	4
A	* *	K135	CABLE 6777	*
B	* *	K2Ø7	K2Ø7	*
C	* *	K161	K161	*
D	* *	K2Ø7	K2Ø7	*

REAR

NOTES:

1. SLOTS A,B,C,D-1 AND A,B,C,D-4 CAN ACCOMODATE EITHER K3Ø2 OR K272 MODULES AS NOTED IN 2,3 BELOW. THE NUMBER OF MODULES IS OPTIONAL.
2. IN SLOTS MARKED * ONLY K3Ø2 MODULES CAN BE USED.
3. IN SLOTS MARKED ** EITHER K3Ø2 OR K272 MODULES CAN BE USED.
4. WHEN RETENTIVE MEMORY MODULES (K272) ARE USED 'A' BOX MUST BE IN VERTICAL POSITION TO INSURE PROPER OPERATION.

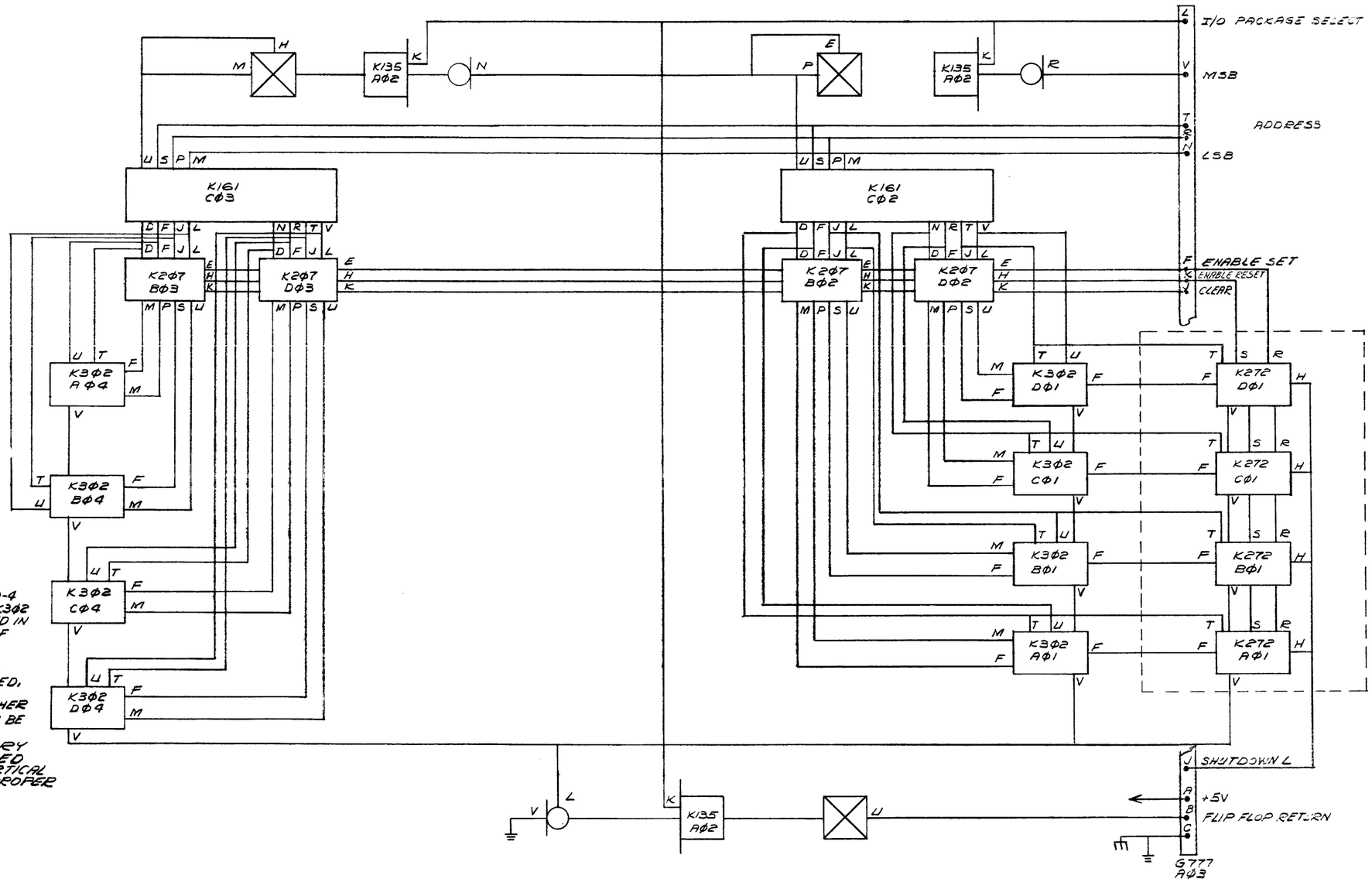


Figure II-43 Accessory Interface Box Block Schematic

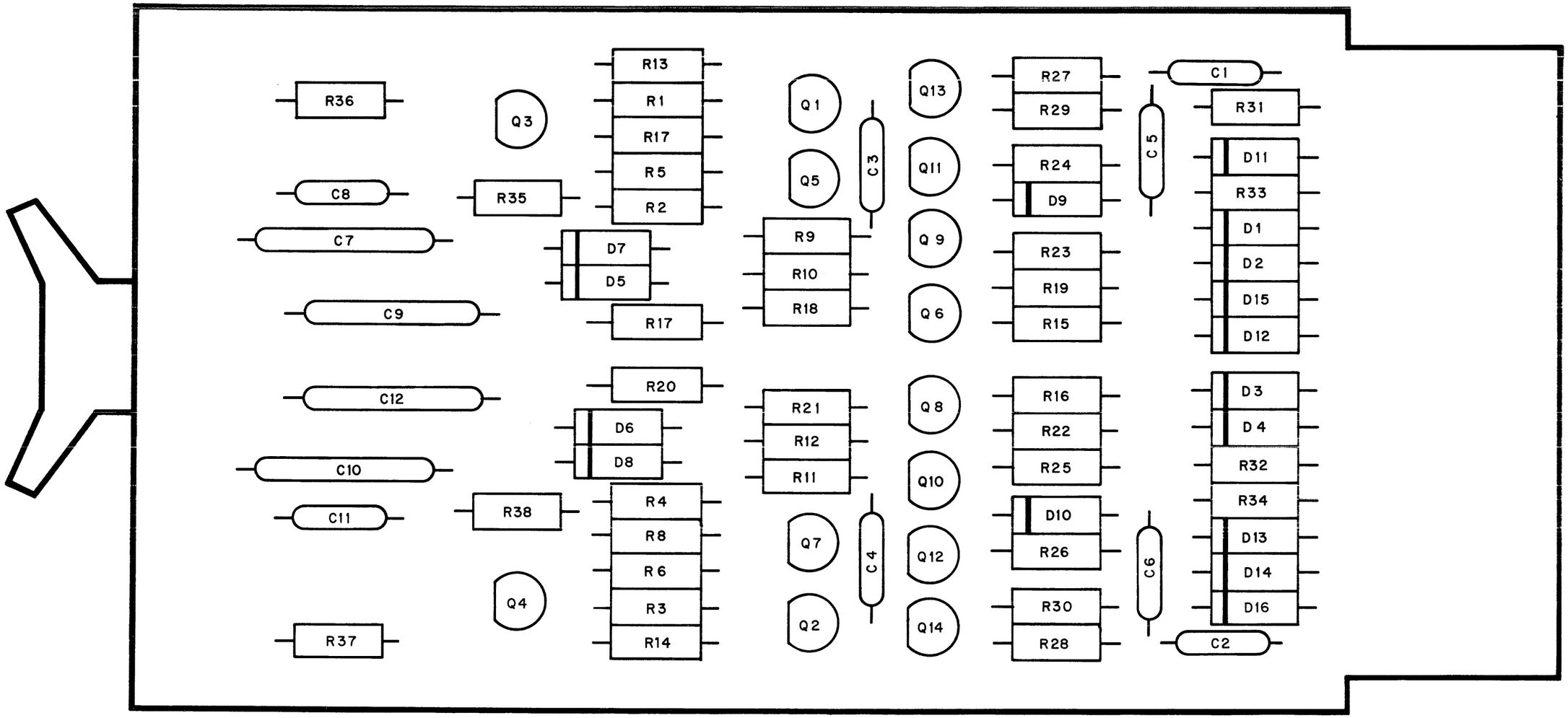
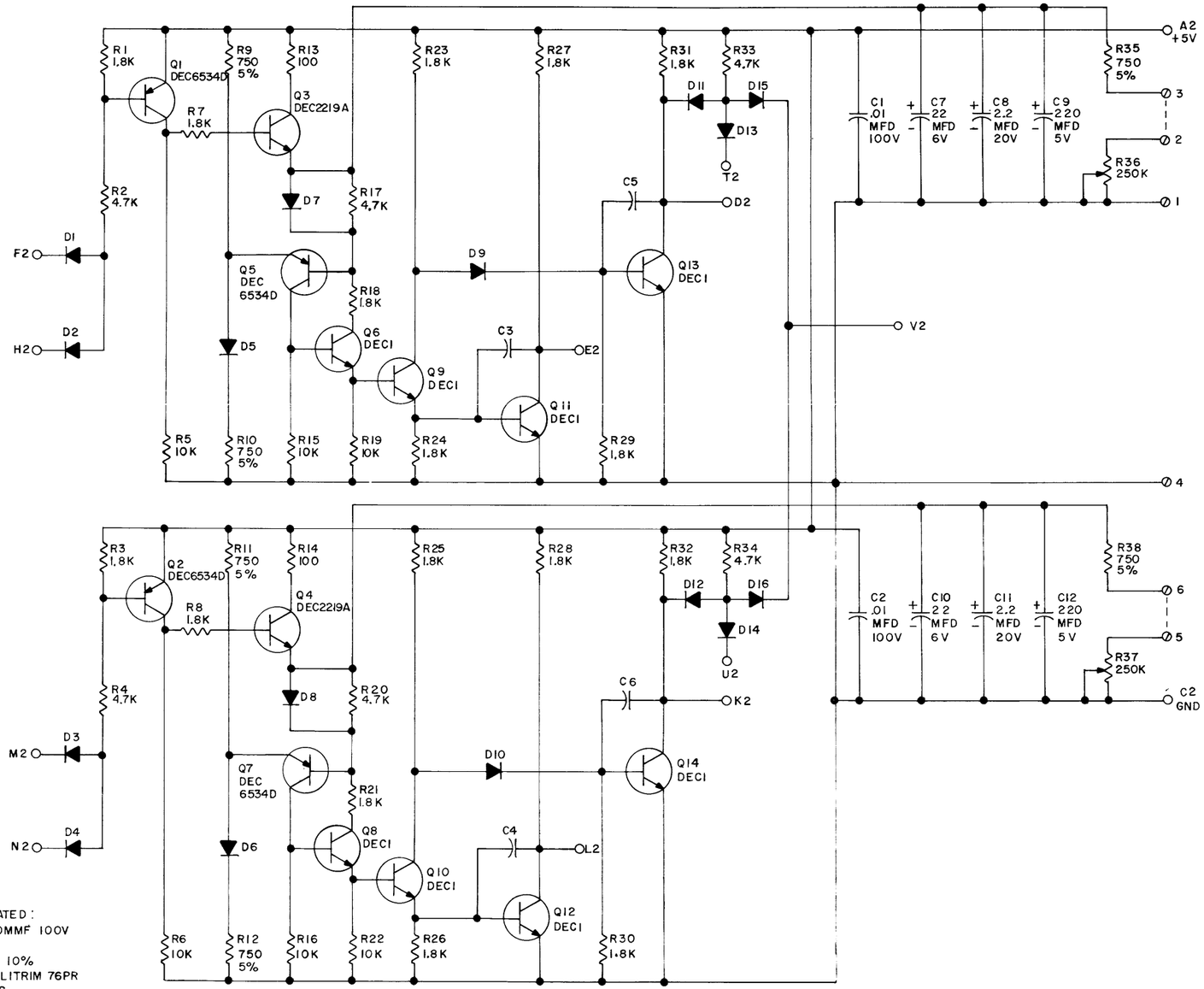


Figure II-44 Two Timers K302 Component Locations



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 680MMF 100V
DIODES ARE D600
RESISTORS ARE 1/4W 10%
R36,R37 ARE POTS HELITRIM 76PR
O---O ARE JUMPERS

Figure II-45 Two Timers K302 Circuit Schematic

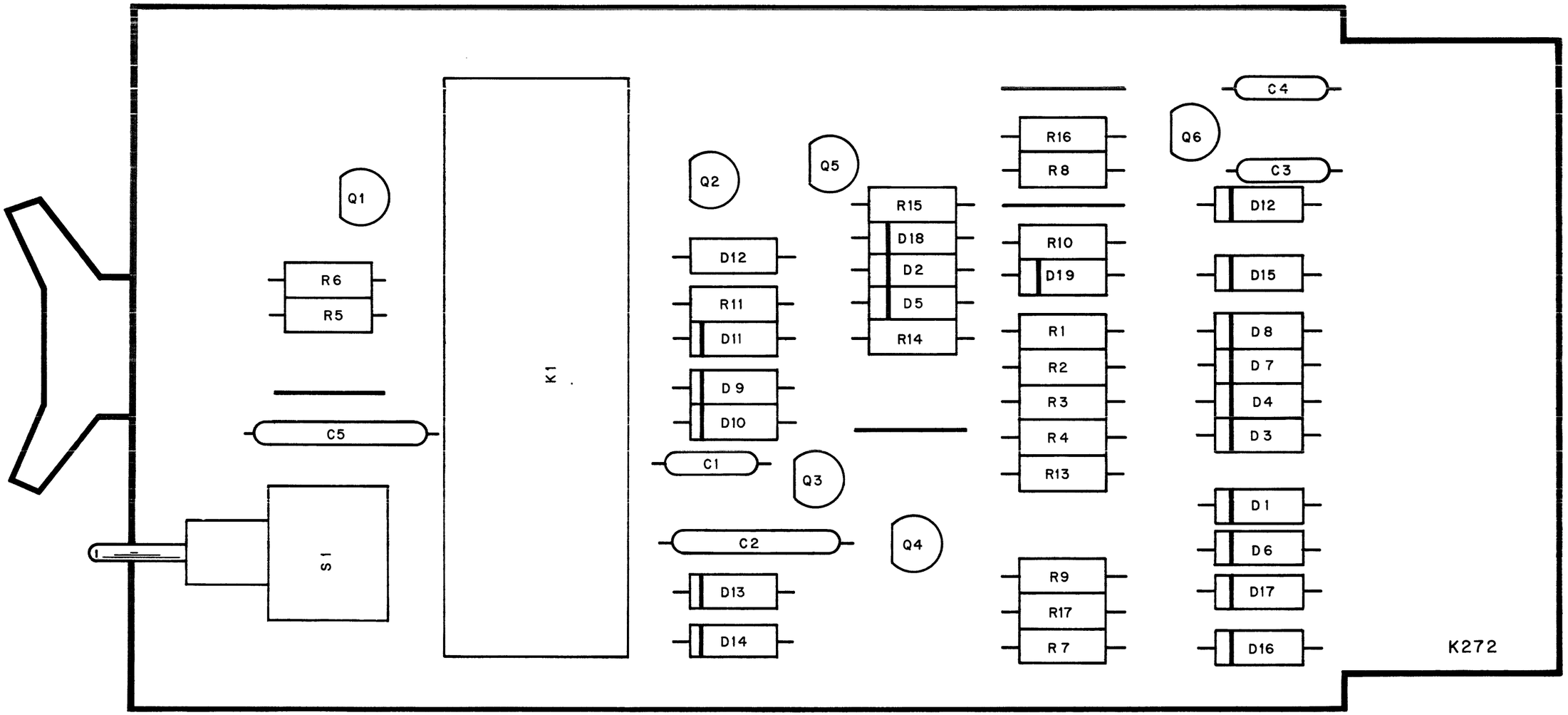
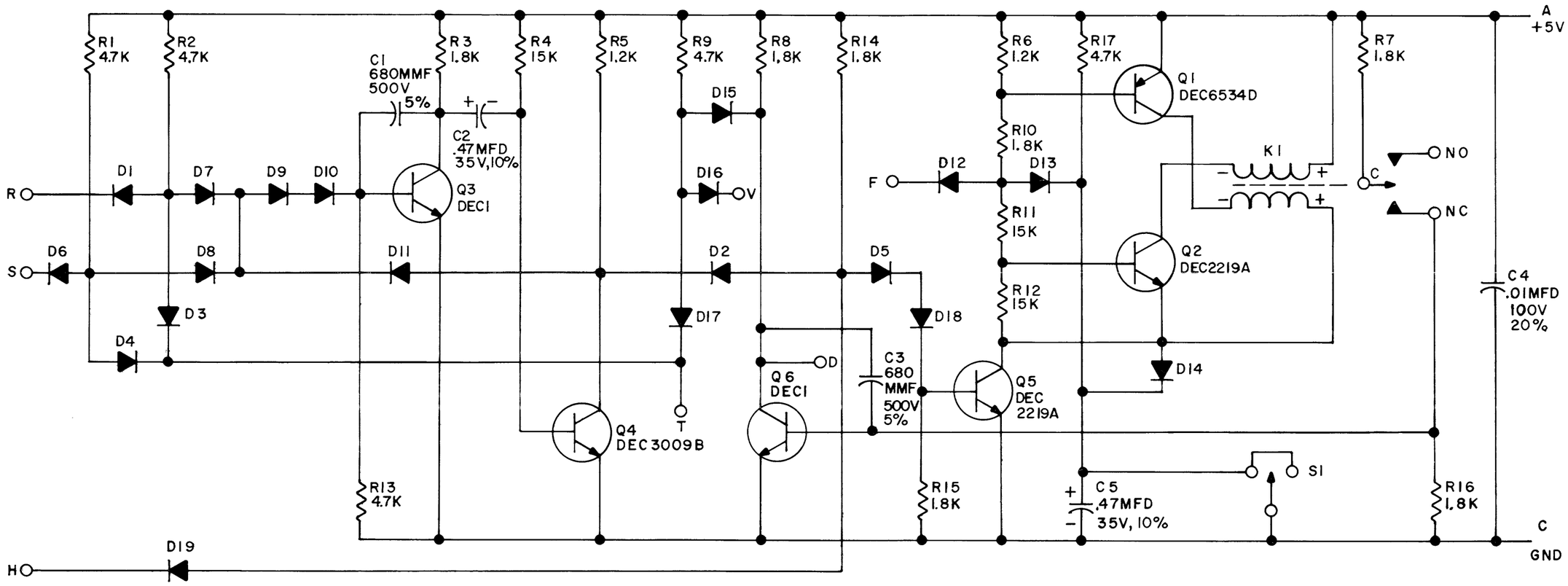


Figure II-46 Retentive Memory K272 Component Locations



UNLESS OTHERWISE INDICATED:
DIODES ARE D600
RESISTORS ARE 1/4W 10%
K1 IS HGSM 5020 RELAY
S1 IS SWITCH 7107

Figure II-47 Retentive Memory K272 Circuit Schematic

	1	2	3	4
A	K207	K135	CABLE G777	K207
B	K207	K161	K161	K207
C	K207	K161	K161	K207
D	K207	K135	CABLE G777	K207

REAR

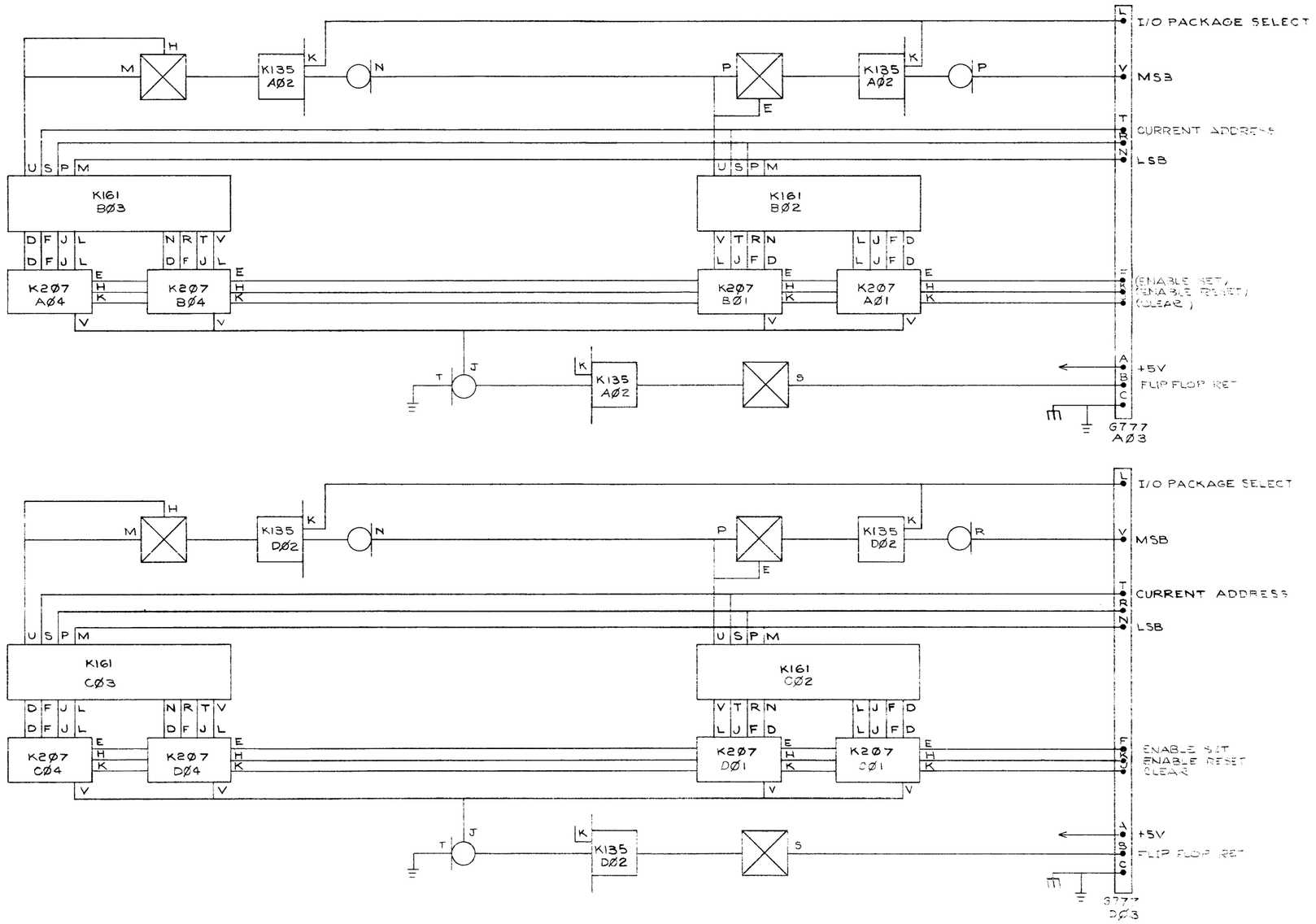
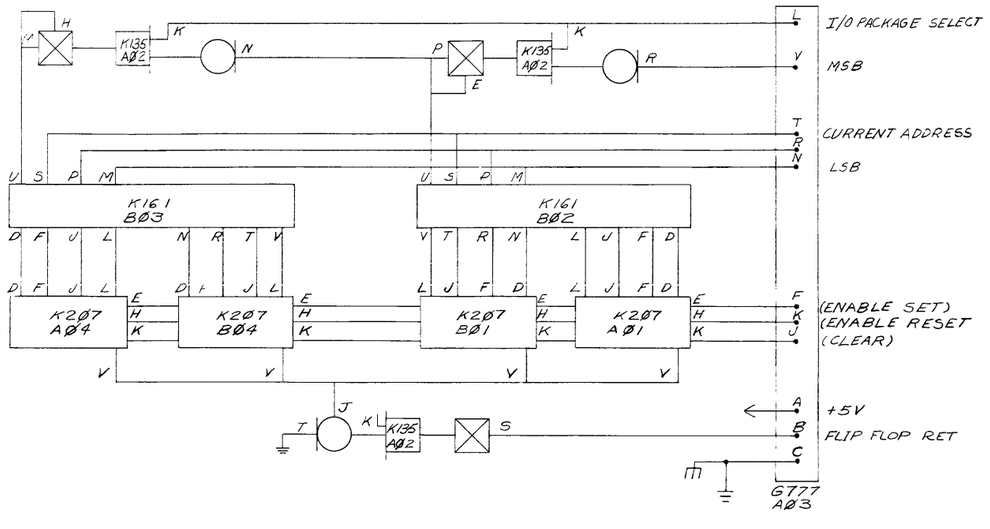


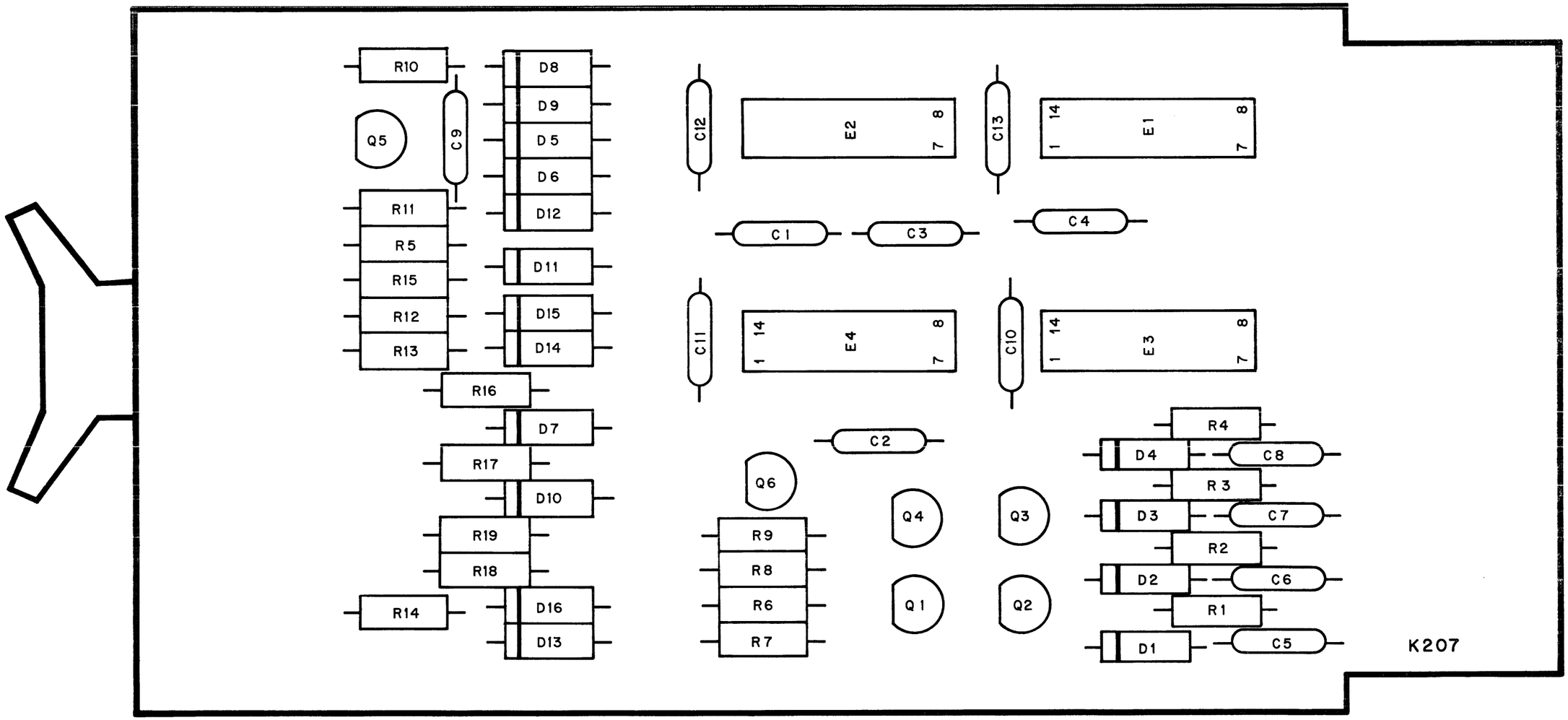
Figure II-48 Storage Interface Box Block Schematic



	1	2	3	4
A	K2Ø7	K135	G777 CABLE	K2Ø7
B	K2Ø7	K161	K161	K2Ø7

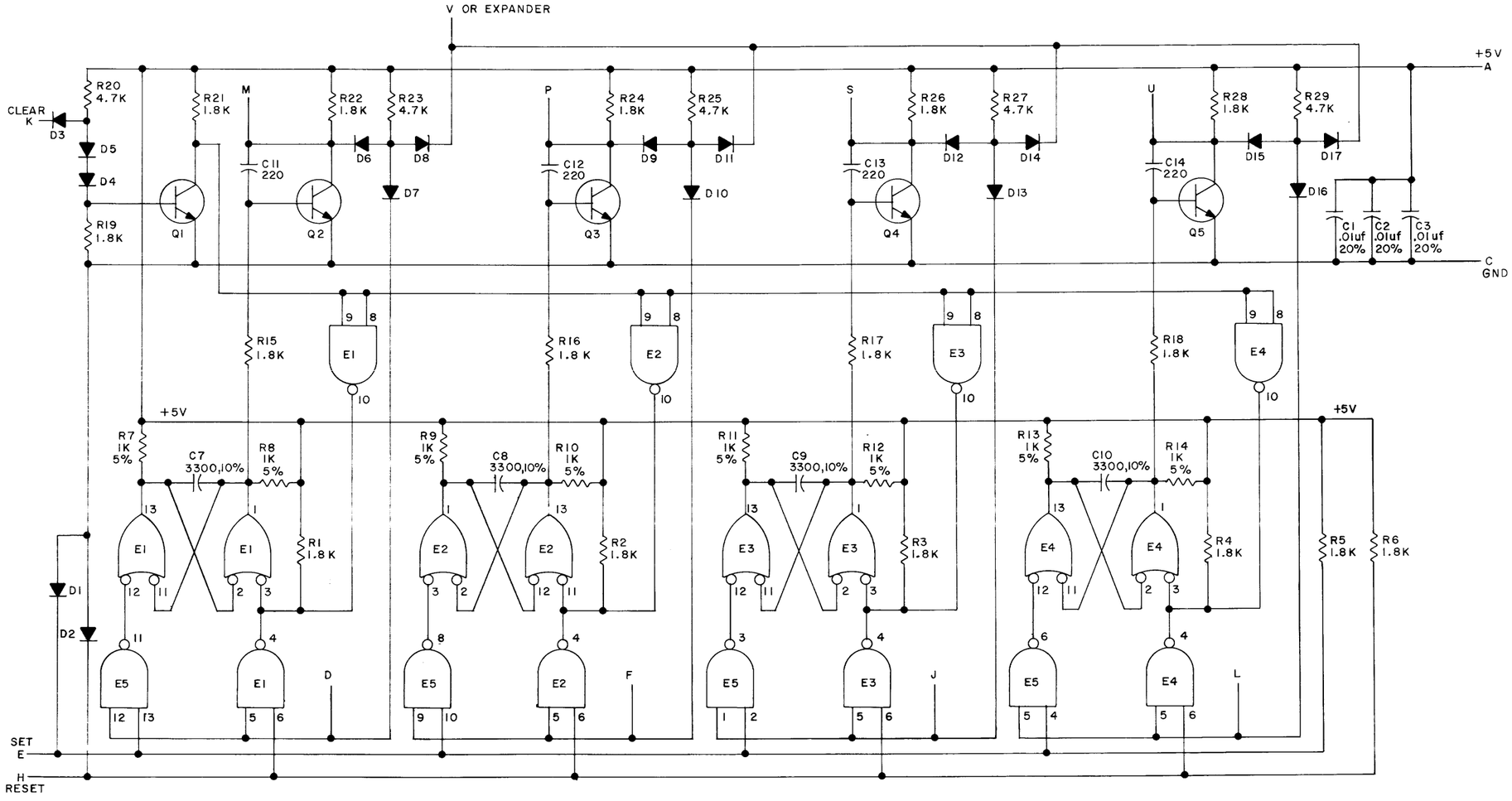
REAR

Figure II-49 Half Storage Interface Box Block Schematic



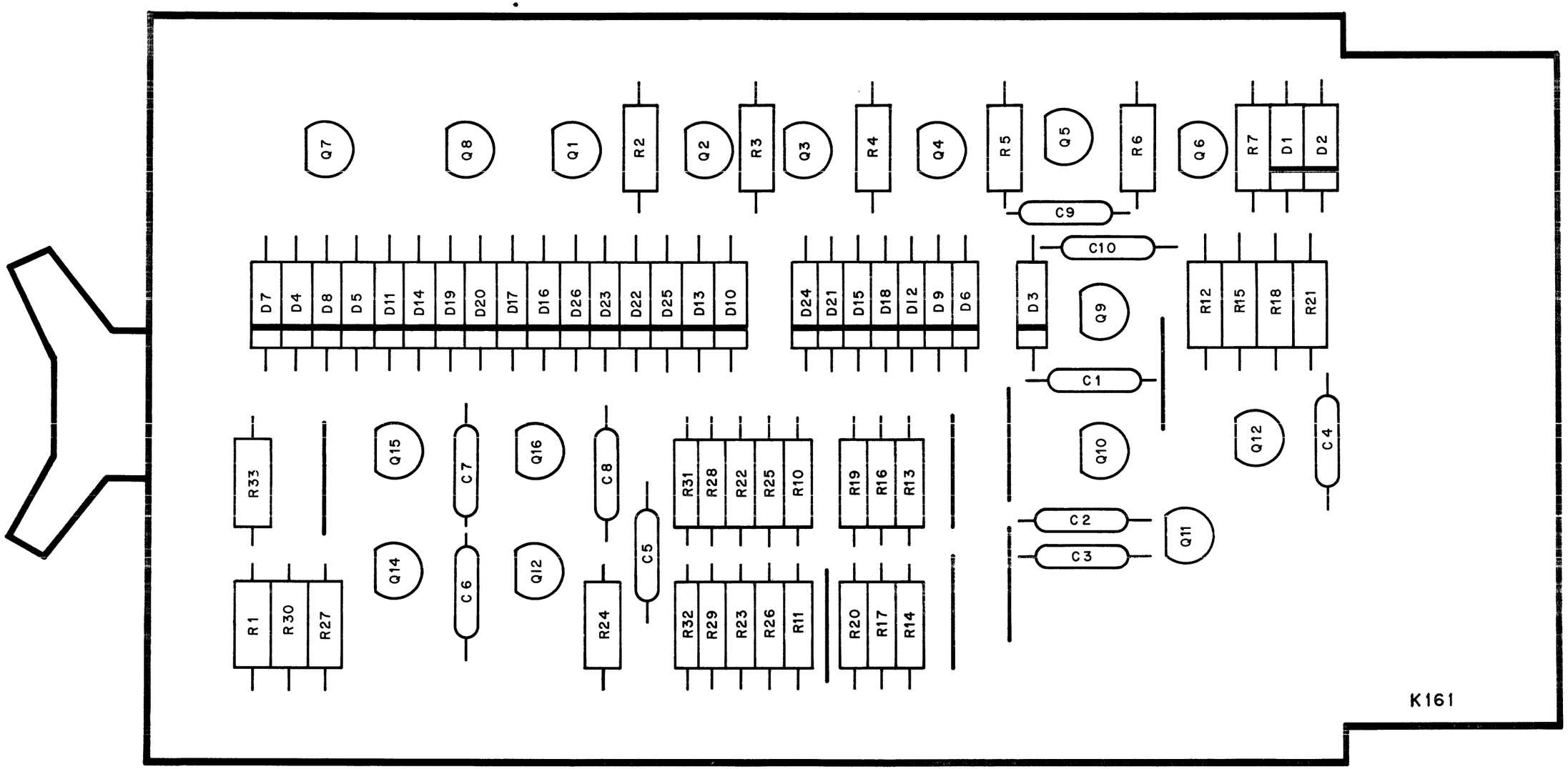
14-0070

Figure II-50 Flip-Flop K207 Component Locations



UNLESS OTHERWISE INDICATED:
DIODES ARE D600
TRANSISTORS ARE DEC I
CAPACITORS ARE pf, 100V, 5%
RESISTORS ARE 1/4W, 10%
E1, E2, E3, E4 ARE DEC7401
E5 IS DEC7400
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

Figure II-51 Flip-Flop K207 Circuit Schematic



14-0071

Figure II-52 Binary-to-Octal Decoder K161 Component Locations

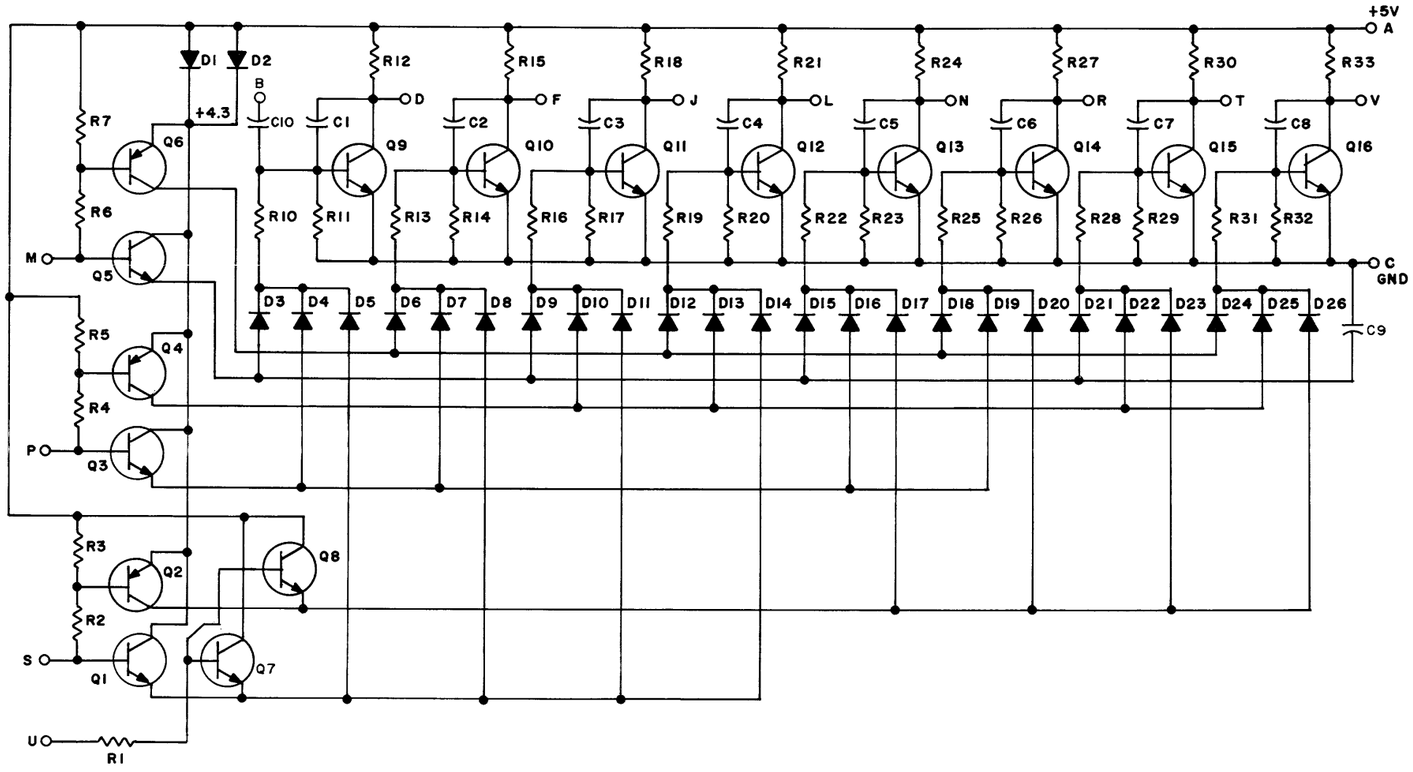


Figure II-53 Binary-to-Octal Decoder K161 Circuit Schematic

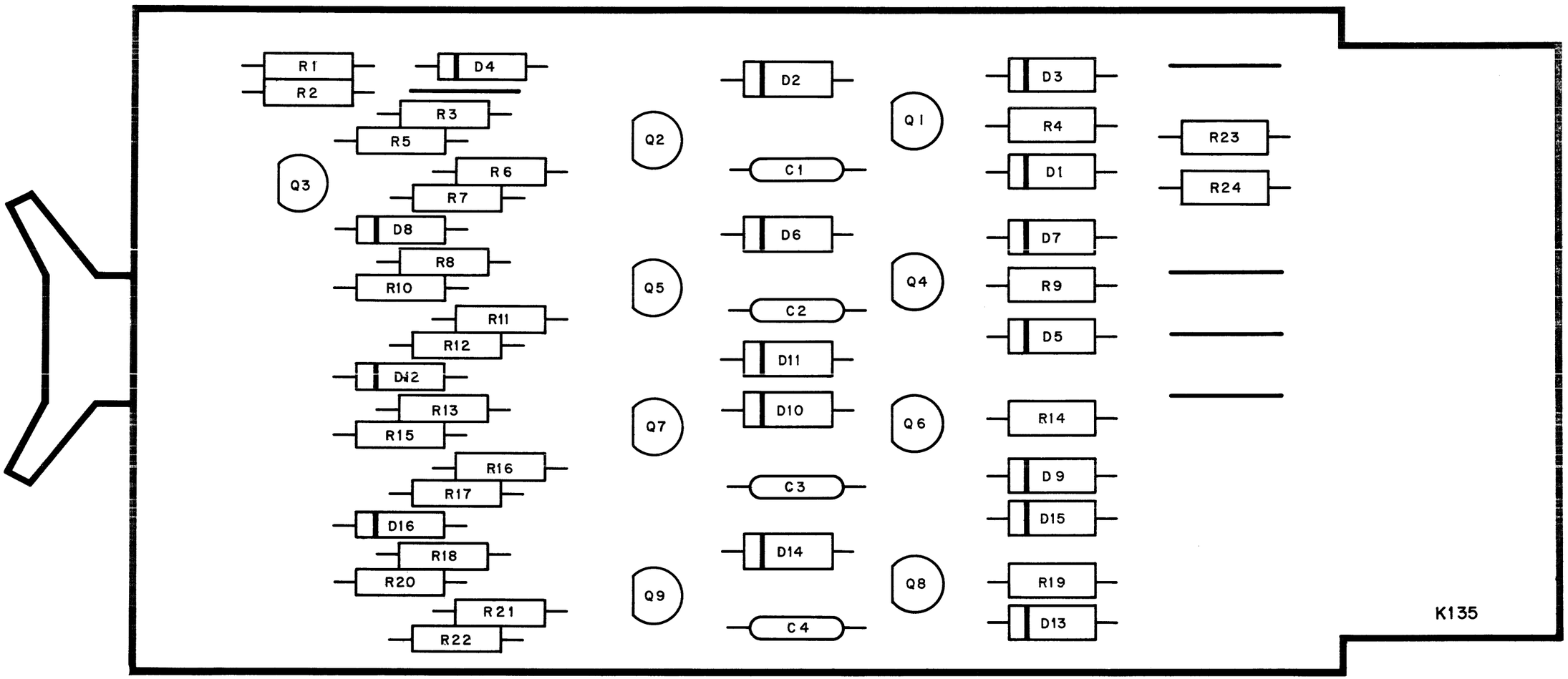
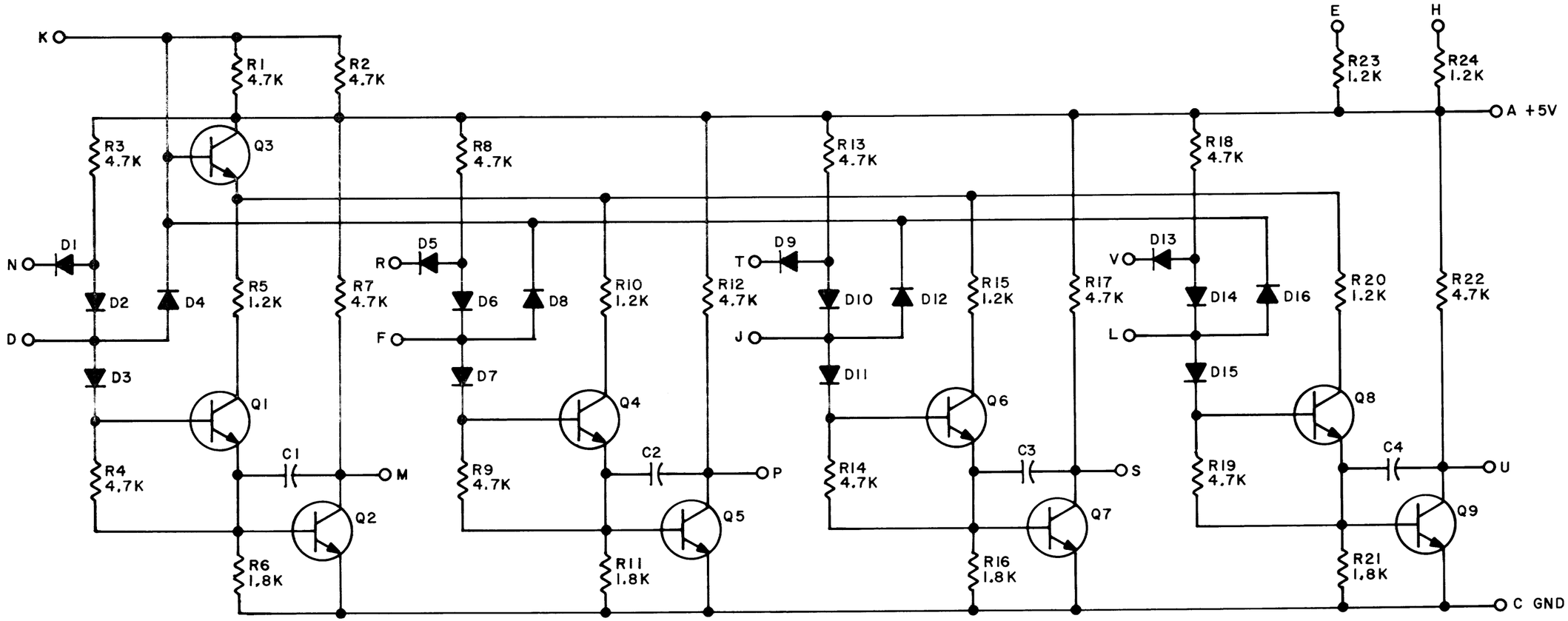


Figure II-54 Inverters K135 Component Locations



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W 10%
CAPACITORS ARE 220 MMF
DIODES ARE D600
TRANSISTORS ARE DEC1
PARTS LIST IS A-PL-K135-0-1

Figure II-55 Inverters K135 Circuit Schematic

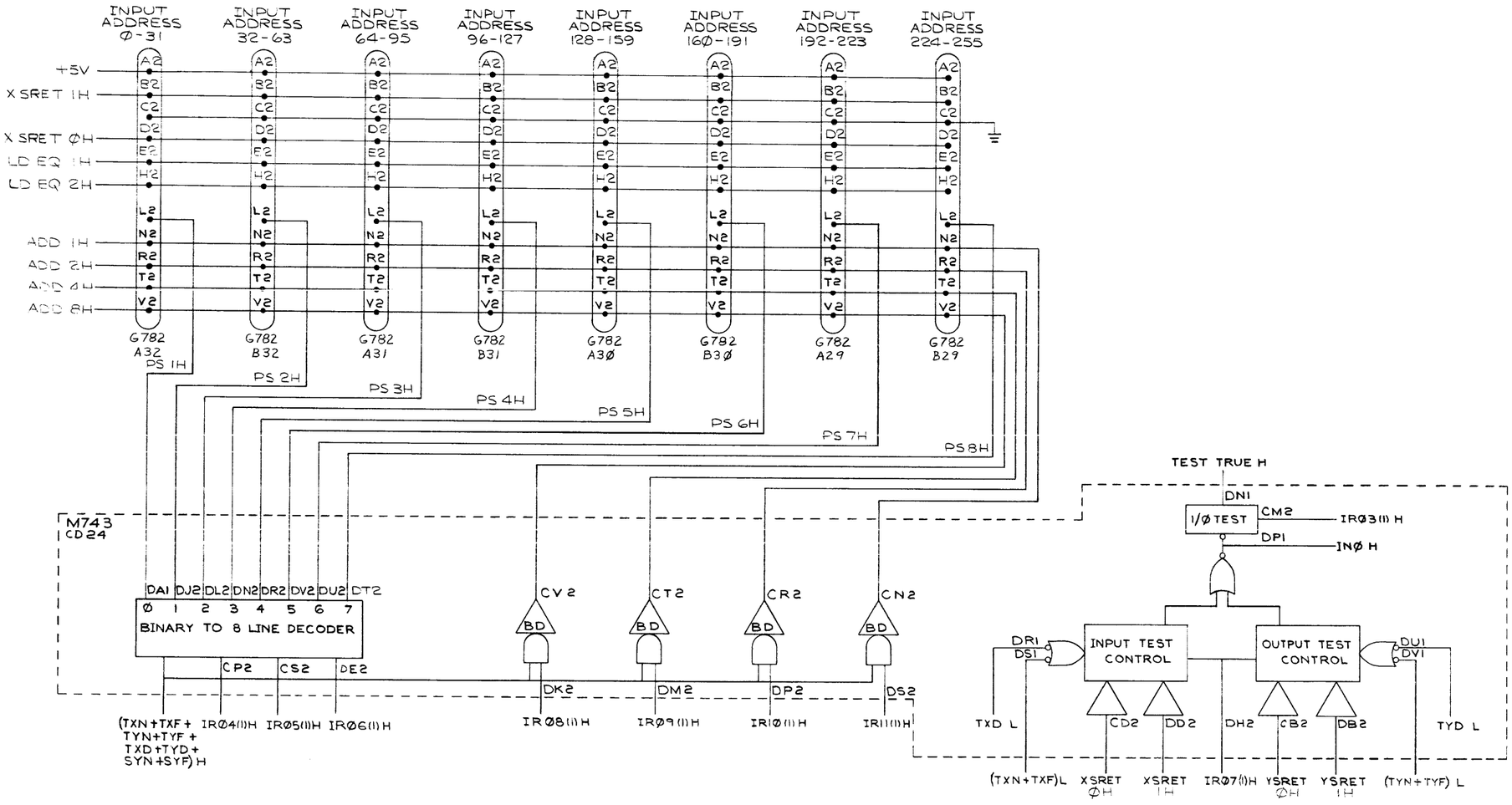


Figure II-56 Interface Box Control (Input and Sample Return) Block Schematic

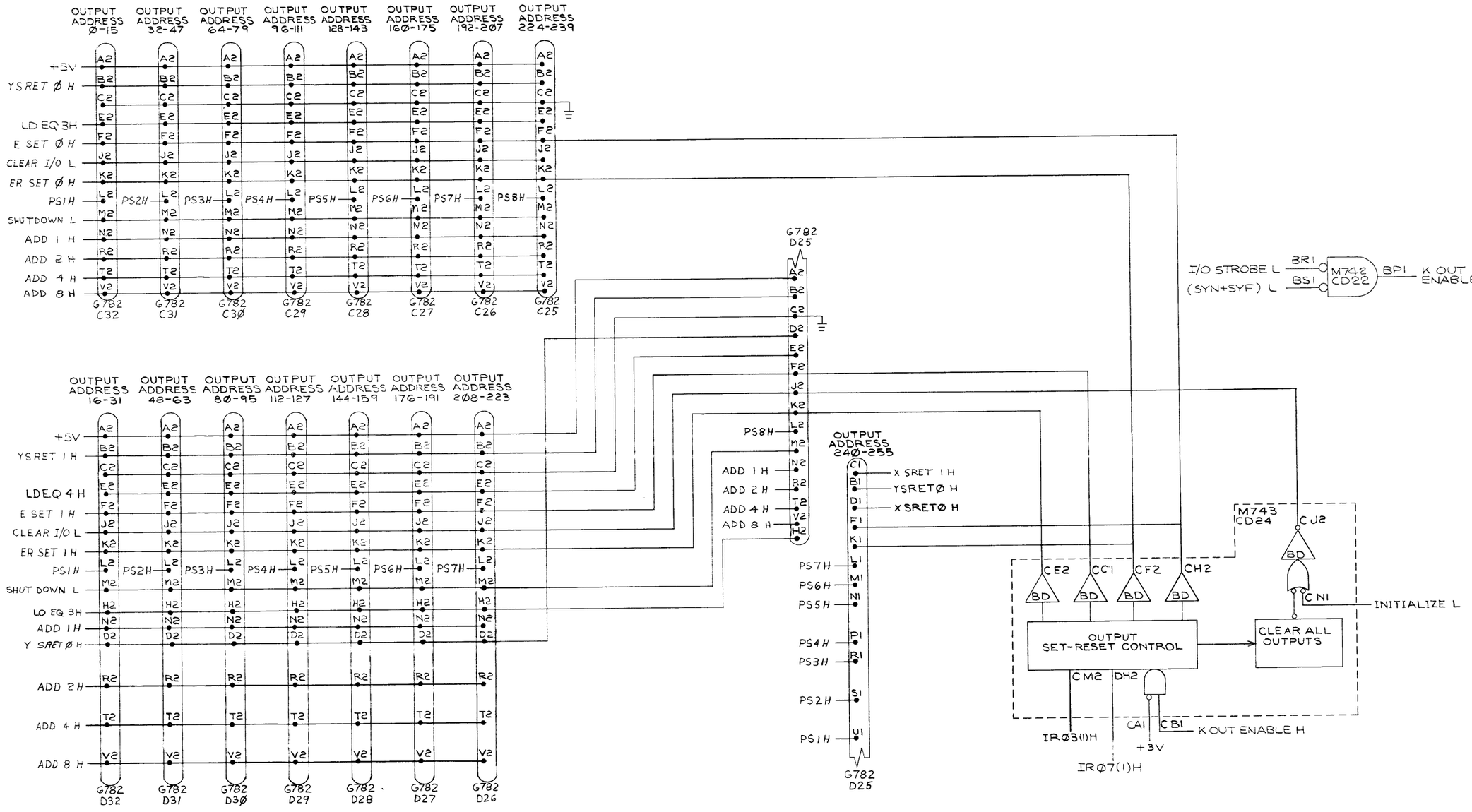


Figure II-57 Interface Box Control (O, S, and A-Box Control) Block Schematic

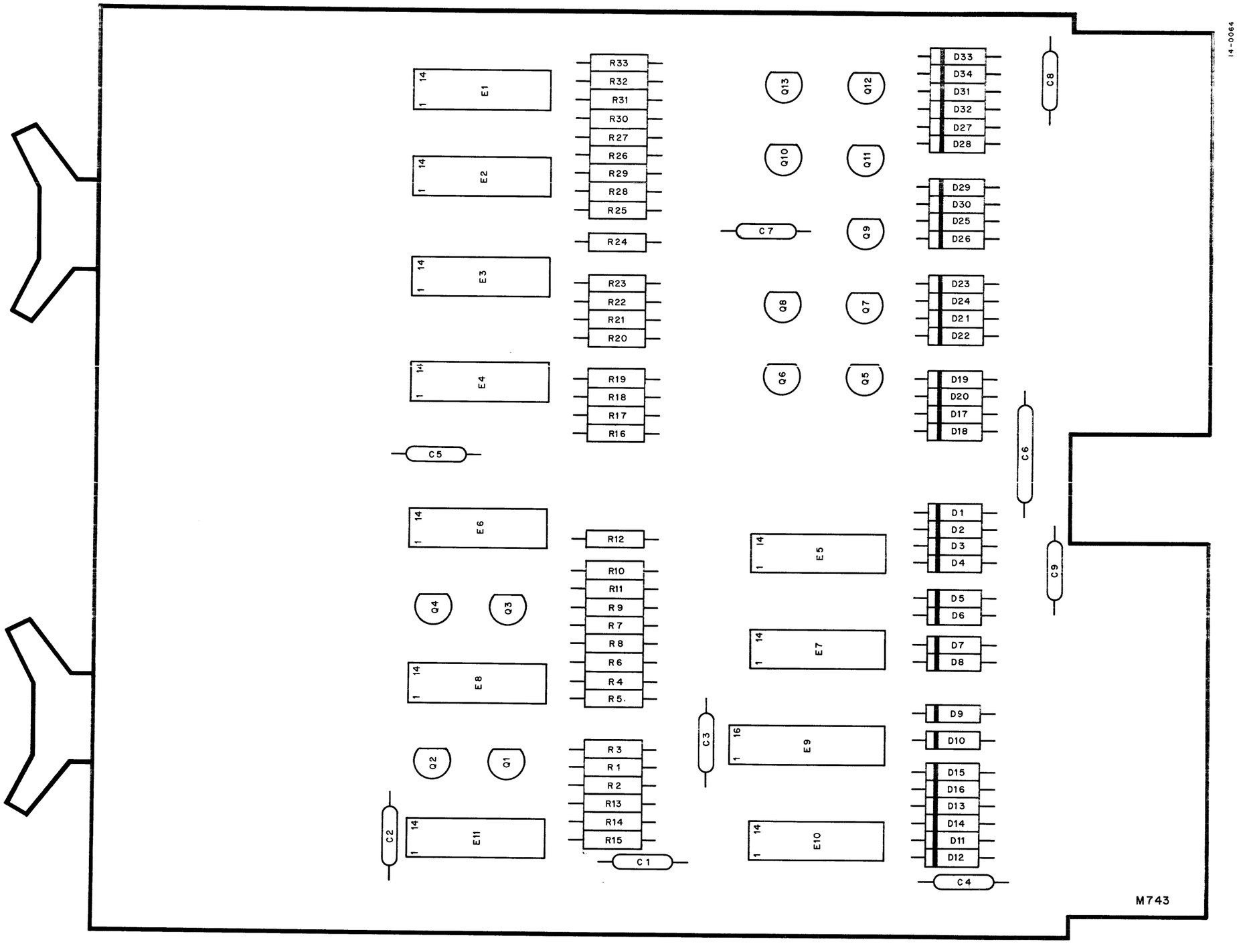
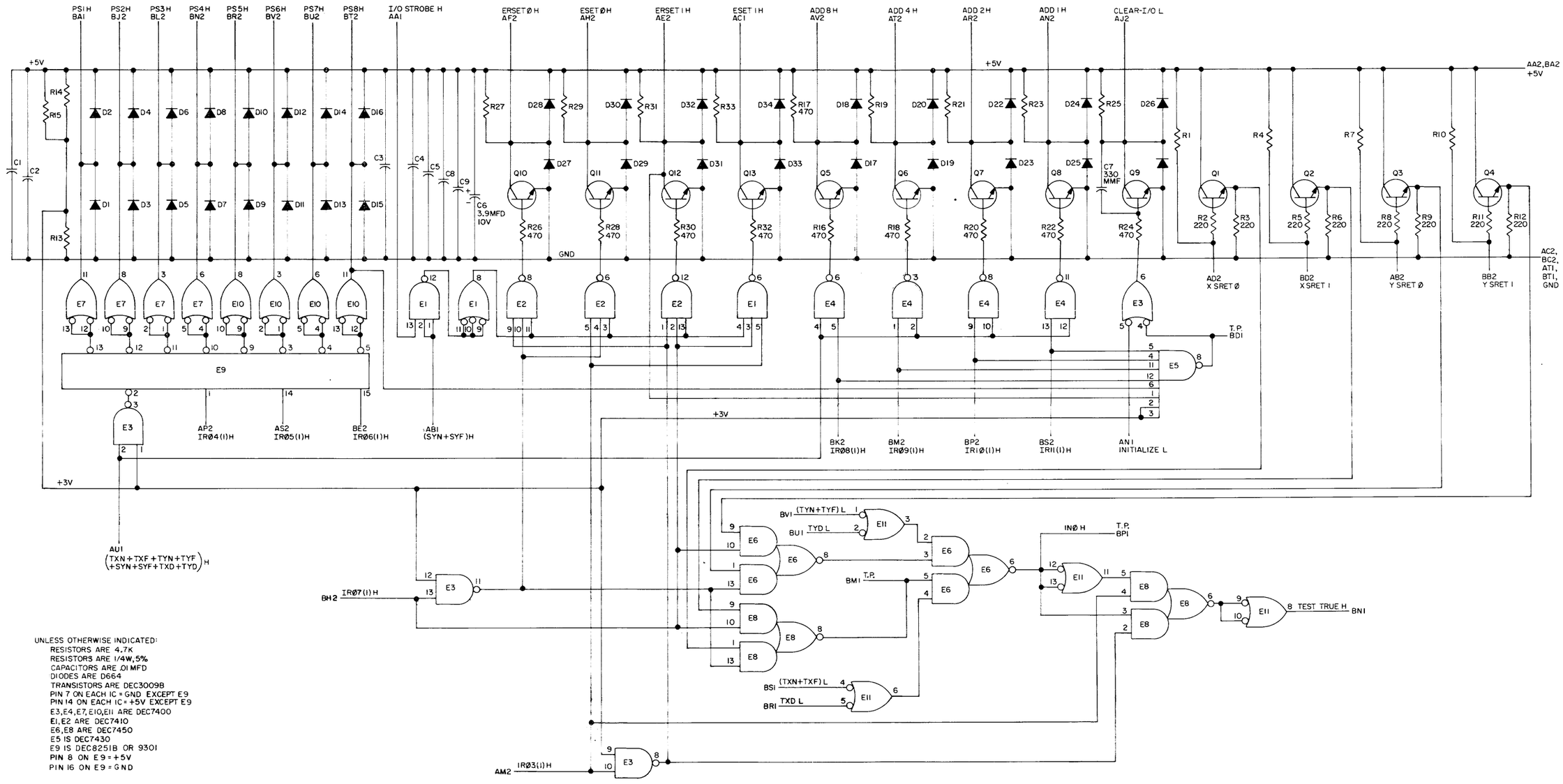
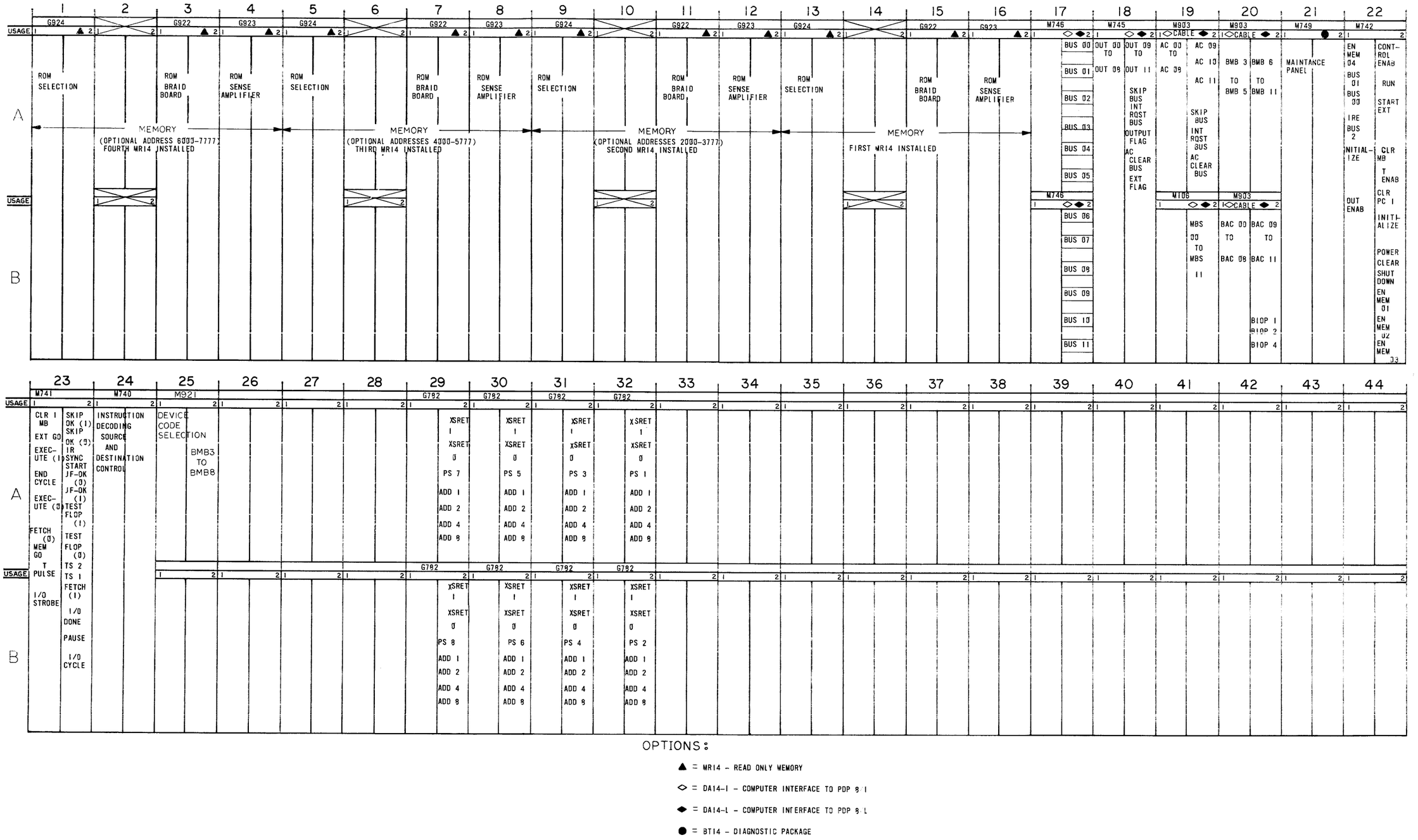


Figure II-58 K Interface Control M743 Component Locations



UNLESS OTHERWISE INDICATED:
- RESISTORS ARE 4.7K
- RESISTORS ARE 1/4W, 5%
- CAPACITORS ARE .01 MFD
- DIODES ARE D664
- TRANSISTORS ARE DEC30098
- PIN 7 ON EACH IC = GND EXCEPT E9
- PIN 14 ON EACH IC = +5V EXCEPT E9
- E3, E4, E7, E10, E11 ARE DEC7400
- E1, E2 ARE DEC7410
- E6, E8 ARE DEC7450
- E5 IS DEC7430
- E9 IS DEC8251B OR 9301
- PIN 8 ON E9 = +5V
- PIN 16 ON E9 = GND

Figure II-59 K Interface Control M743 Circuit Schematic



OPTIONS:

▲ = MR14 - READ ONLY MEMORY

◇ = DA14-I - COMPUTER INTERFACE TO PDP 8-I

◆ = DA14-L - COMPUTER INTERFACE TO PDP 8-L

● = BT14 - DIAGNOSTIC PACKAGE

Figure II-60 Module Utilization (Control Unit Rows A and B)

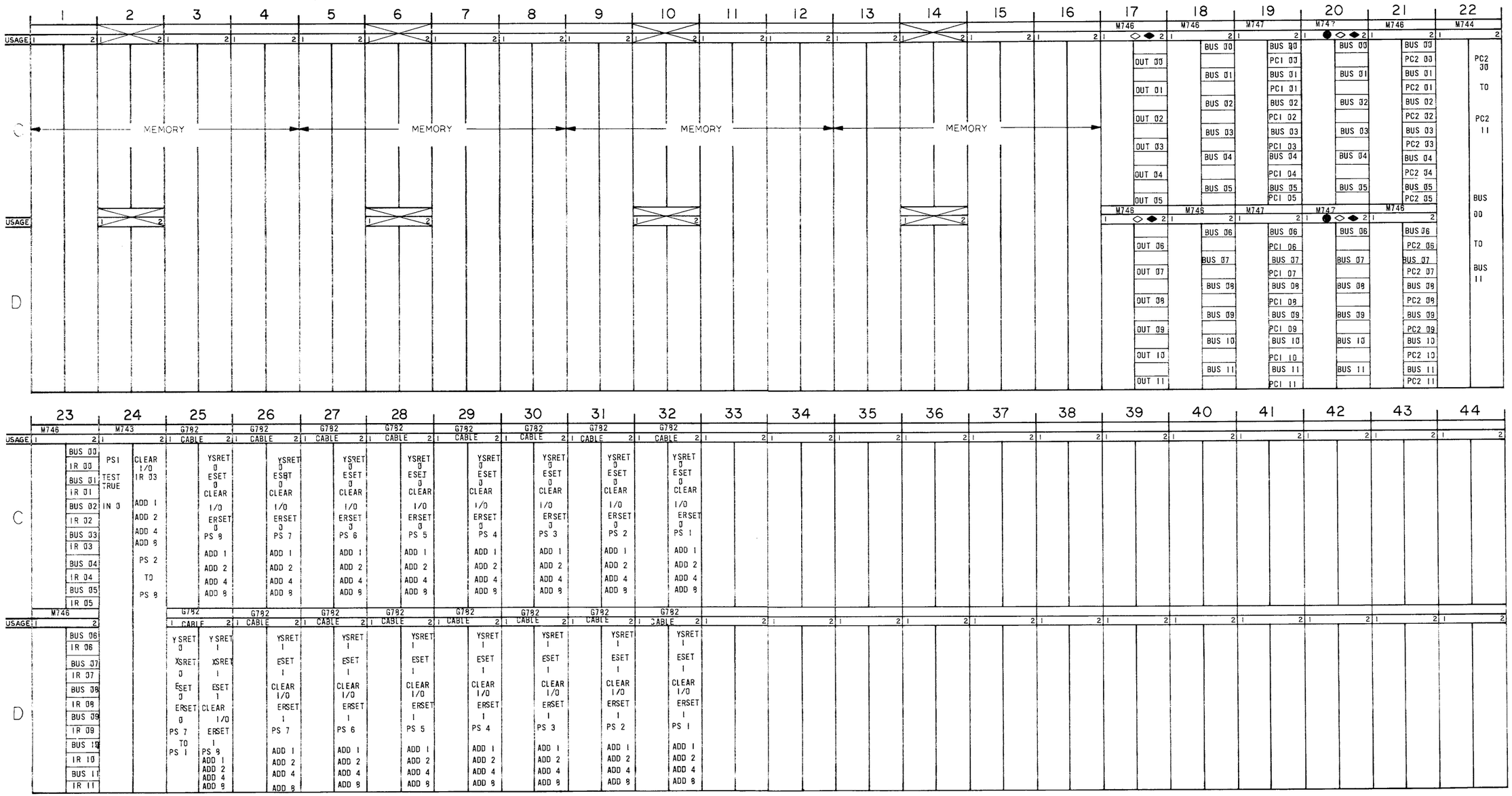


Figure II-61 Module Utilization (Control Unit Rows C and D)

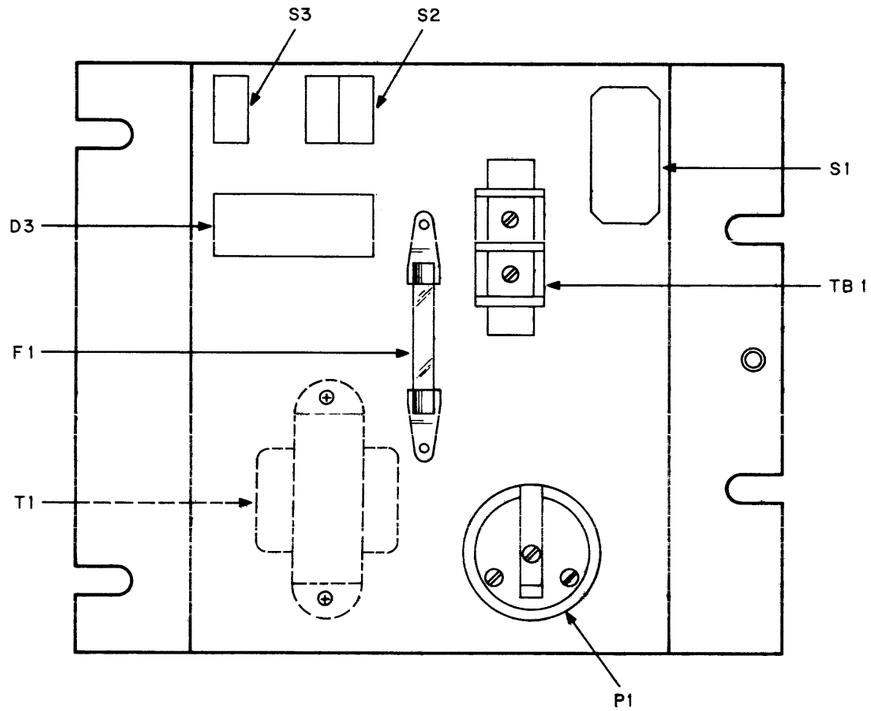


Figure II-62 Power Supply Filter Assembly Component Locations

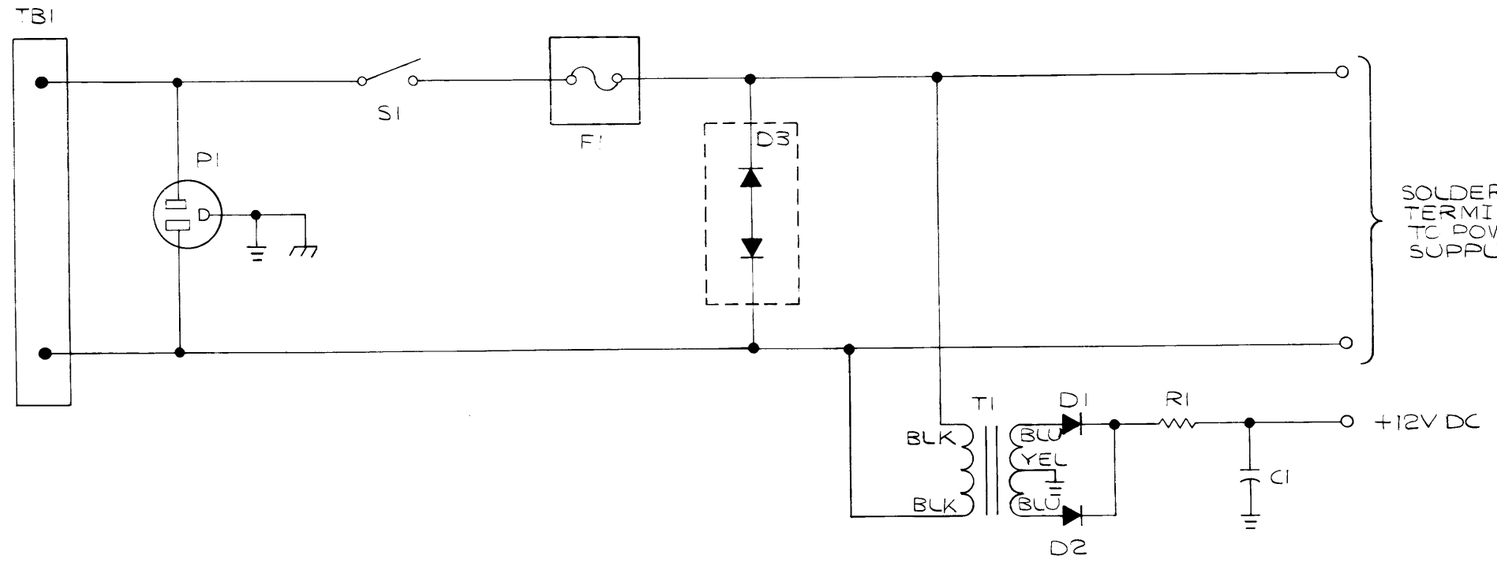


Figure II-63 Power Supply Filter Assembly Circuit Schematic