pdp11

DZ11
user's manual

digital

EK-DZ11-OP-PR1

DZ11
user's manual

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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The DZ11 is an asynchronous multiplexer that provides an interface between a PDP-11 processor and eight (8) asynchronous serial lines. It can be used with PDP-11 systems in a variety of applications that include communications processing, time sharing, transaction processing and real time processing. Local operation to terminals or computers is possible at speeds up to 9600 baud using either EIA RS232C interfaces or 20 mA current loop signaling. Remote operation using the public switched telephone network is possible with DZ11 models offering EIA RS232C interfaces. Enough data-set control is provided to permit dial up (auto answer) operation with modems capable of full duplex* operation such as the Bell models 103 or 113 or equivalent. Remote operation over private lines for full duplex* point to point or full duplex* multipoint as a control (master) station is also possible. Figure 1-1 depicts several of the possible applications for the DZ11 in a PDP-11 system.

*The DZ11 data-set control does not support half duplex operations or the secondary transmit and receive operations available with some modems such as the Bell model 202, etc.

The DZ11 has several features that provide flexible control of parameters such as baud rate, character length, number of stop bits for each line, odd or even parity for each line, and transmitter-receiver interrupts. Additional features include limited data set control, auto receiver baud rate, break generation and detection, silo buffering of received data, module plug-in to hex SPC slots, and line turnaround.

Each DZ11 module provides for operation of eight (8) asynchronous serial lines. Since the module interfaces to these channels with a sixteen (16) line distribution panel, two (2) DZ11 modules can be used with one panel. Also note that the two versions of the DZ11 (EIA or 20 mA output) consists of different module and panel types. This fact allows a system to mix EIA and 20 mA by using multiple DZ11s.

1.2 PHYSICAL DESCRIPTION

The DZ11 (8-line configuration) comprises a single hex SPC module and a 5.25-inch, unpowered distribution panel, connected by a 15-foot ribbon cable. Several types of interconnecting cables are used between the distribution panel and the modem or terminal, depending on the device. A 16-line configuration uses two modules and a single distribution panel connected by two ribbon cables. The DZ11 modules, cables, and distribution panel are shown in Figures 1-2 and 1-3. The subsequent paragraphs present a detailed description of the physical and electrical specifications of the various DZ11 options and configurations.

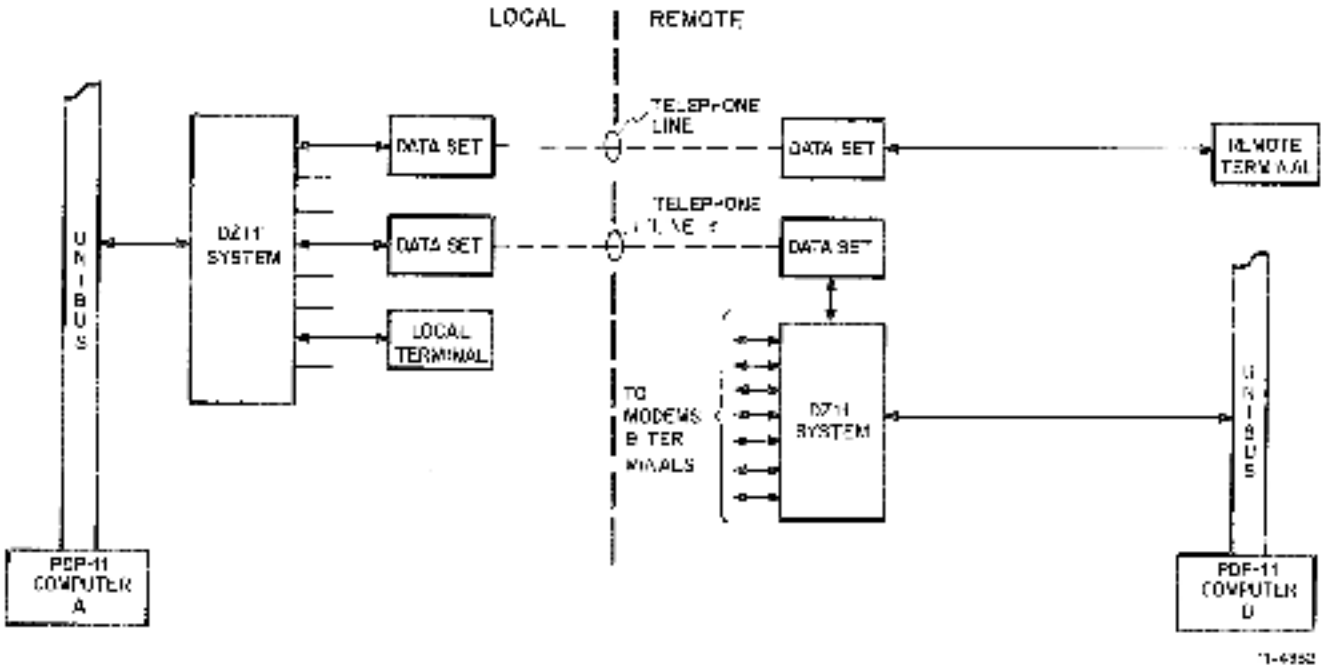


Figure 1-1 DZ11 System Applications

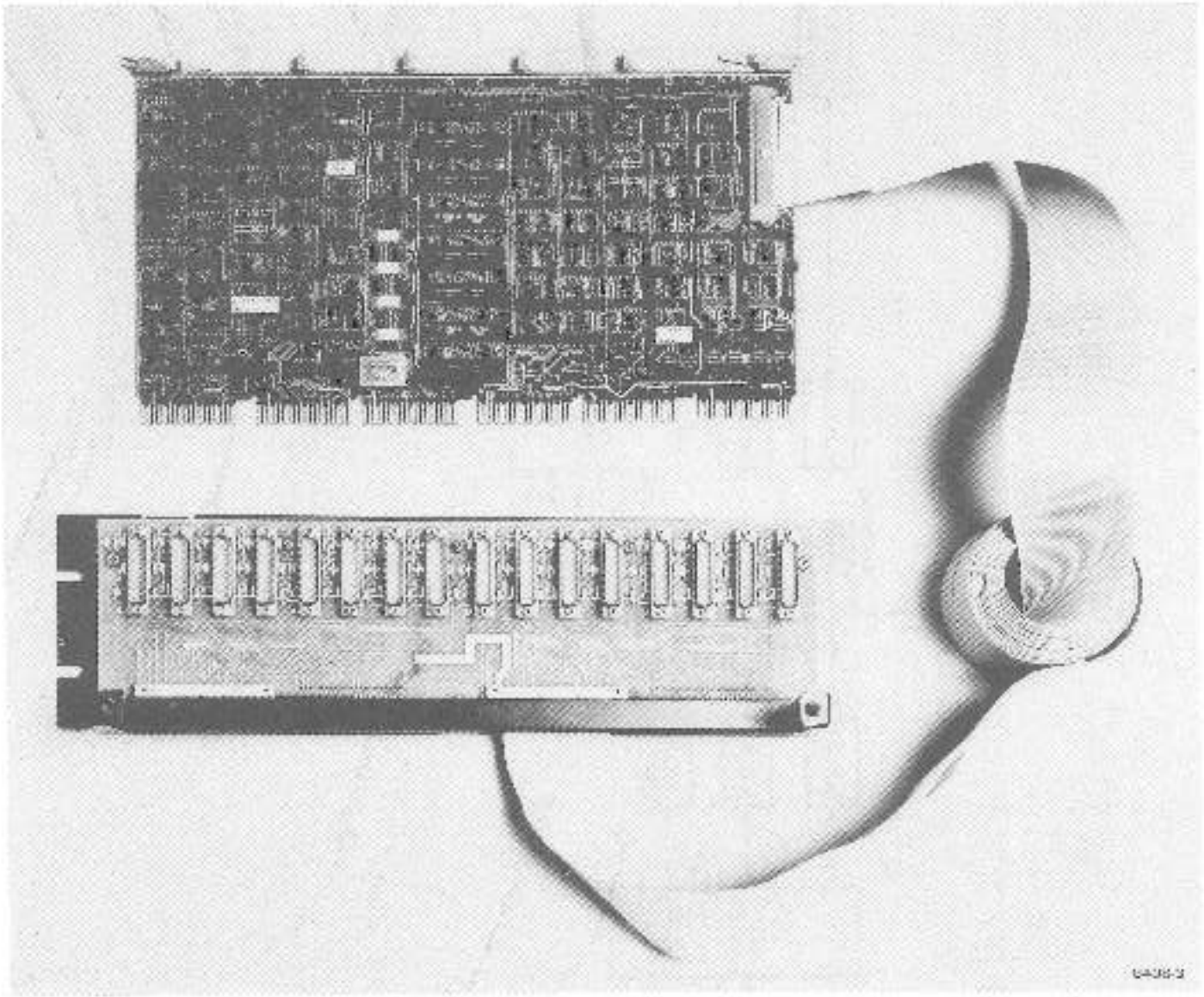


Figure 1-2 DZ11 STA Module (M7819), Distribution Panel (H317-E), and Cable (BC05N-15)

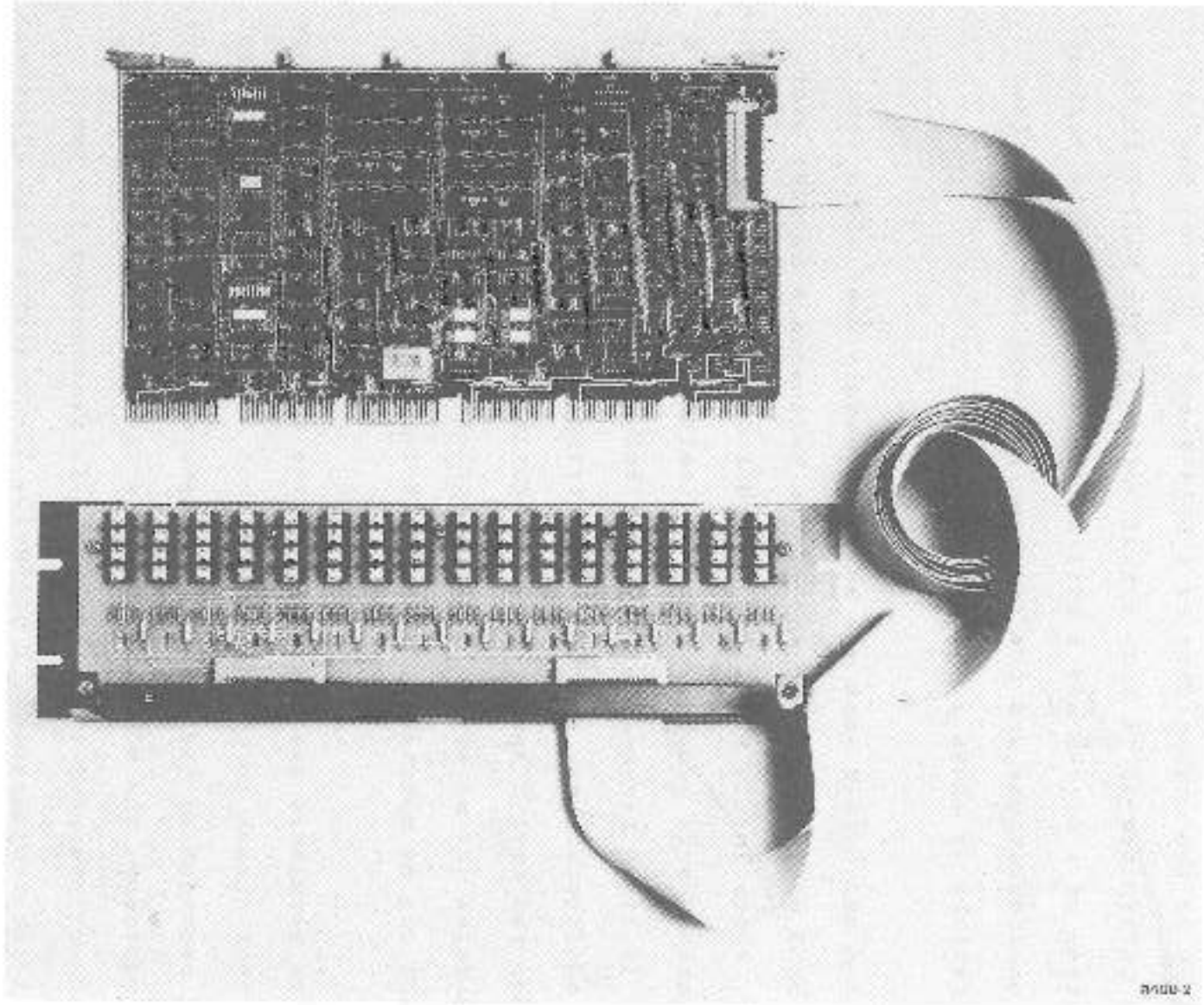


Figure 1-3 D211 20 mA Module (M7B14), Distribution Panel (H317-F), and Cable (BC08S-15)

1.2.1 DZ11 Configurations

The DZ11 can be supplied in six different configurations, each designated by a suffix letter (A, B, C, D, E, or F). The DZ11-A and the DZ11-B options are EIA devices with partial modem control. The DZ11-E is the combination of a DZ11-A and a DZ11-B. The DZ11-C and the DZ11-D are 20 mA loop output versions. The DZ11-F is the combination of a DZ11-C and a DZ11-D. Table 1-1 shows the various option configurations and the required hardware for the various configurations is shown in Figure 1-4.

The DZ11-A and DZ11-B each use an M7819 module that plugs into slot 2 or 3 of a DD11-B, or any system unit with a hex SPC slot; however, slots in the PDP-11/20 BA11 box cannot be used. The H317-E distribution panel provides 16 communication lines from two M7819 modules (8 lines per module), and is included with the DZ11-A and DZ11-E configurations. The H317-F distribution panel provides 16 lines for the DZ11-C and DZ11-F configurations, which use the M7814 modules (20 mA system). The distribution panels require no power and can be mounted in an H960 19-inch cabinet.

Modems or terminals are connected to the H317-E, the EIA panel, by cables that attach to its 16 DB25P cinch connectors. These cables are not provided by the DZ11 and therefore must be bought separately by the customer. The BC05D-25 cable is recommended for data set interconnections, and the BC03N cable is recommended for local terminal interconnections. A BC05W-10, 50-conductor flat shielded cable connects from the M7819 module to the EIA panel. This conductor carries the data and control signals of all 8 lines. Connections between terminals and the H317-F, the 20 mA panel, are by customer

Table 1-1 DZ11 Model Configurations

Model	Output	Module	Panel	Connector	Cable
DZ11-A	EIA	M7819	H317-E	H325/**H327	BC05W
DZ11-B	EIA	M7819	--	**H327	BC05W
DZ11-E	EIA	*M7819	H317-B	H325/***H327	*BC05W
DZ11-C	20 mA	M7814	H317-C	***H3190	BC08S
DZ11-D	20 mA	M7814	--	***H3190	BC08S
DZ11-F	20 mA	*M7814	H317-F	****H3190	*BC08S

*=quantity of two

**=H327 will be replaced by H3271 in later models. Check shipping list to see if there is one.

***-Not supplied with early models. Check shipping list to see if there is one.

supplied cables to its 16 (four screw) terminal strips. The data and control signals of all 8 lines are carried to the distribution panel by a BC08S-15 40 conductor, flat shielded ribbon cable.

Two accessory test connectors, H325 and H3271* are provided with each DZ11-A. The H325 plugs into an EIA connector on the distribution panel or on the end of the BC05D cable to loop back data and modem signals onto a single line. The H3271 connects to the module with the BC05N cable (two M7819 modules can be connected to one H3271) and staggers the data and modem lines as shown in Figure 1-5. The connectors are shown in Figure 1-7.

The 20 mA (M7814 module) option also have a staggered turnaround connector (H319C). This is a new item and the shipping list should be checked to see if you have one. The H319C connects to the M7814 using the BC08S cable, and staggers the lines as shown in Figure 1-6.

A priority level 5 insert plugs into a socket on the M7819 or M7814 module to establish interrupts at level 5 on the Unibus.

Maximum configuration allows 16 DZ11 modules per Unibus.

*This is a new item replacing the H327. The H327 may be used until the H3271 becomes available. The H327 plugs directly into J1 on the M7819 module.

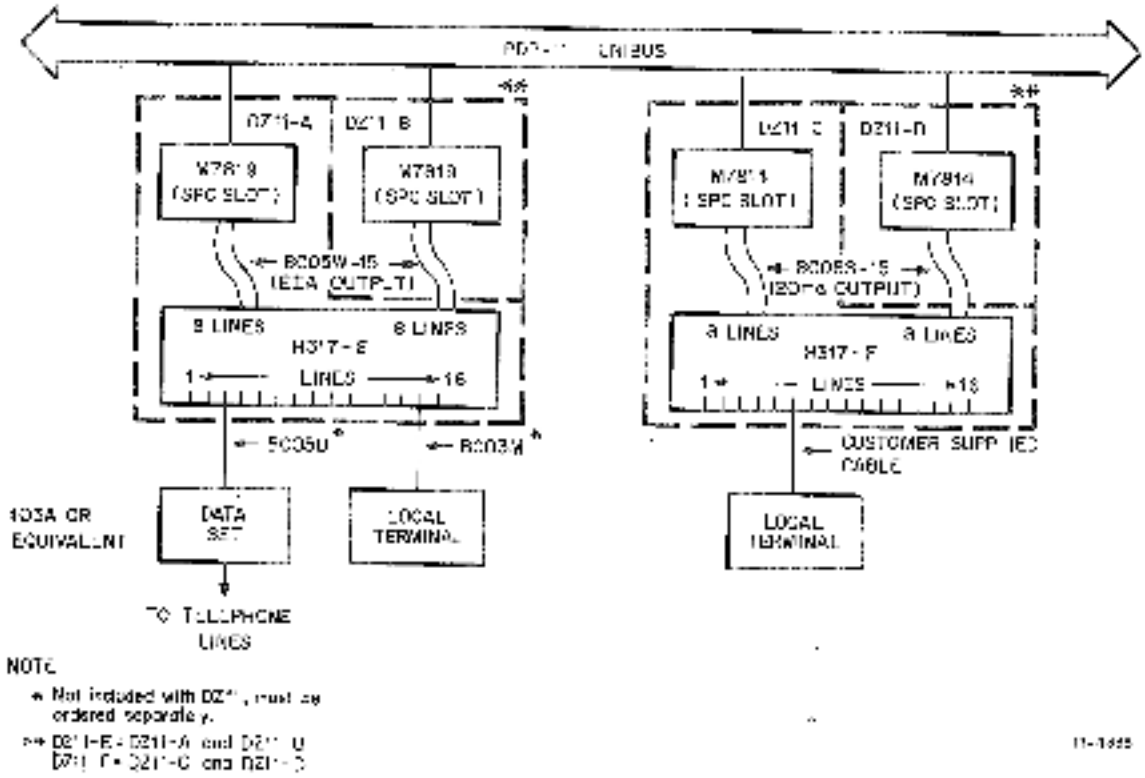
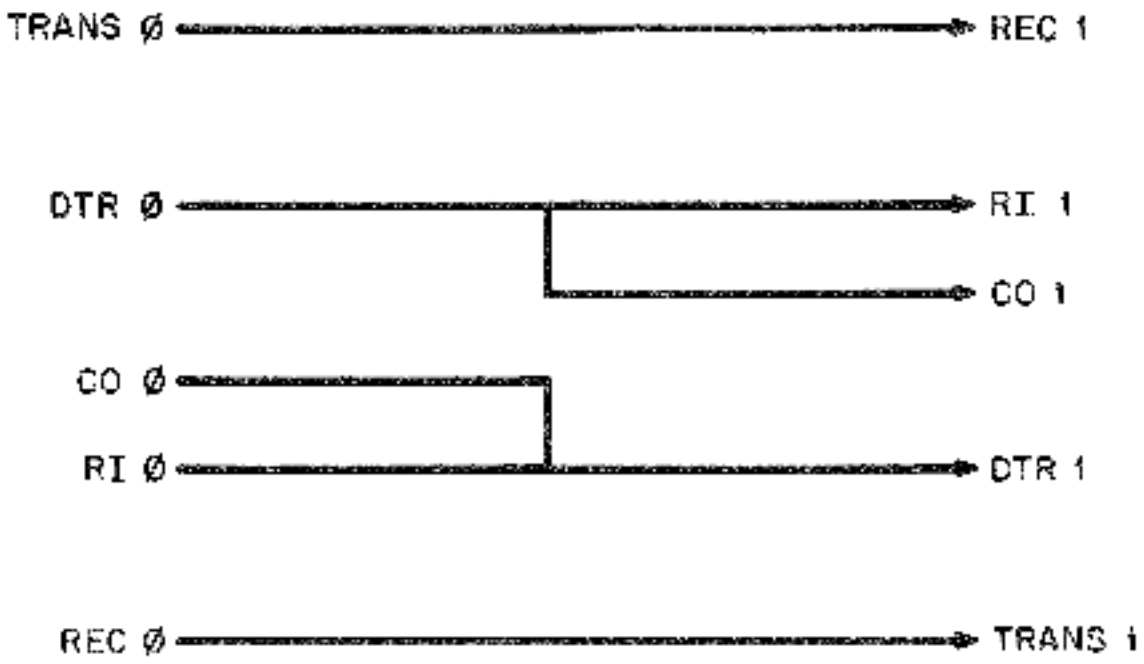


Figure 1-4 DZ11 Hardware Interconnections



NOTE:
Lines 2 & 3, 4 & 5 and 6 & 7 are staggered the same way.

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Figure 1-5 3271 or 8327 Turnaround

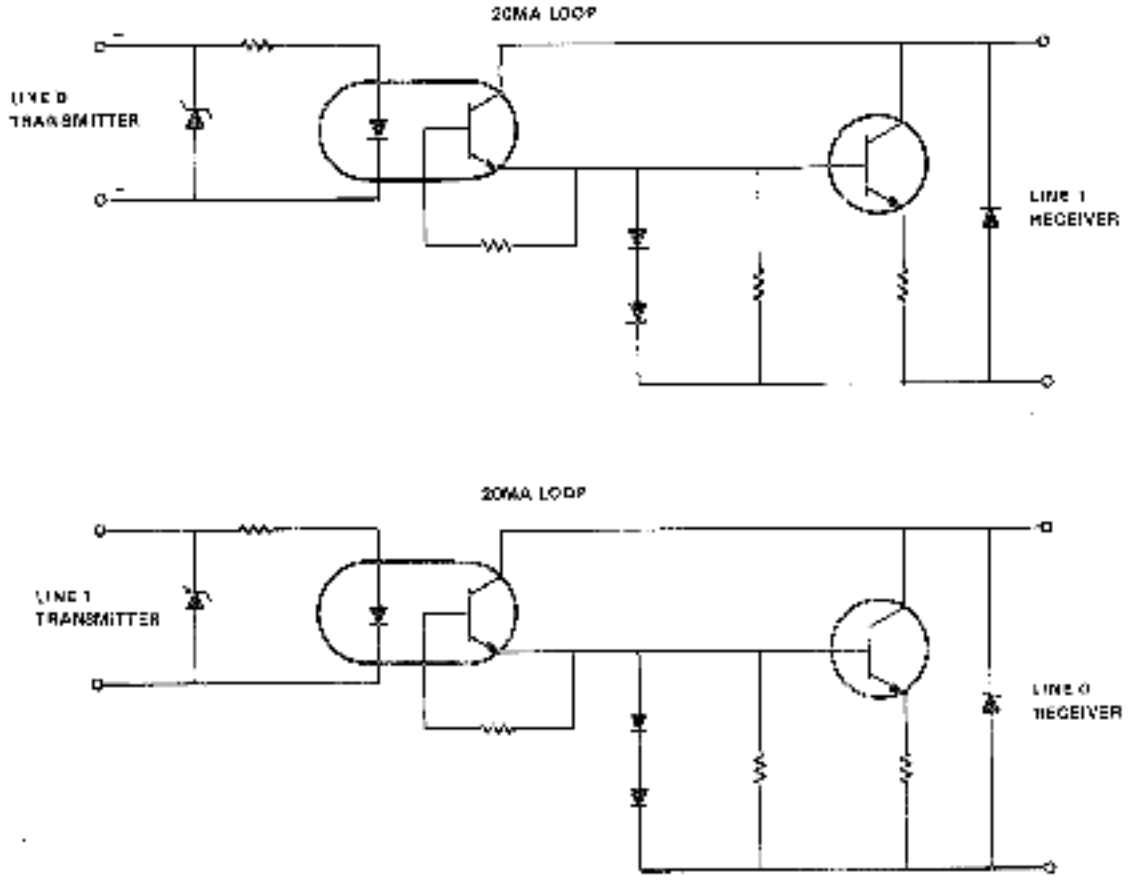


Figure 1-6 H3190 Staggered Line Turnaround

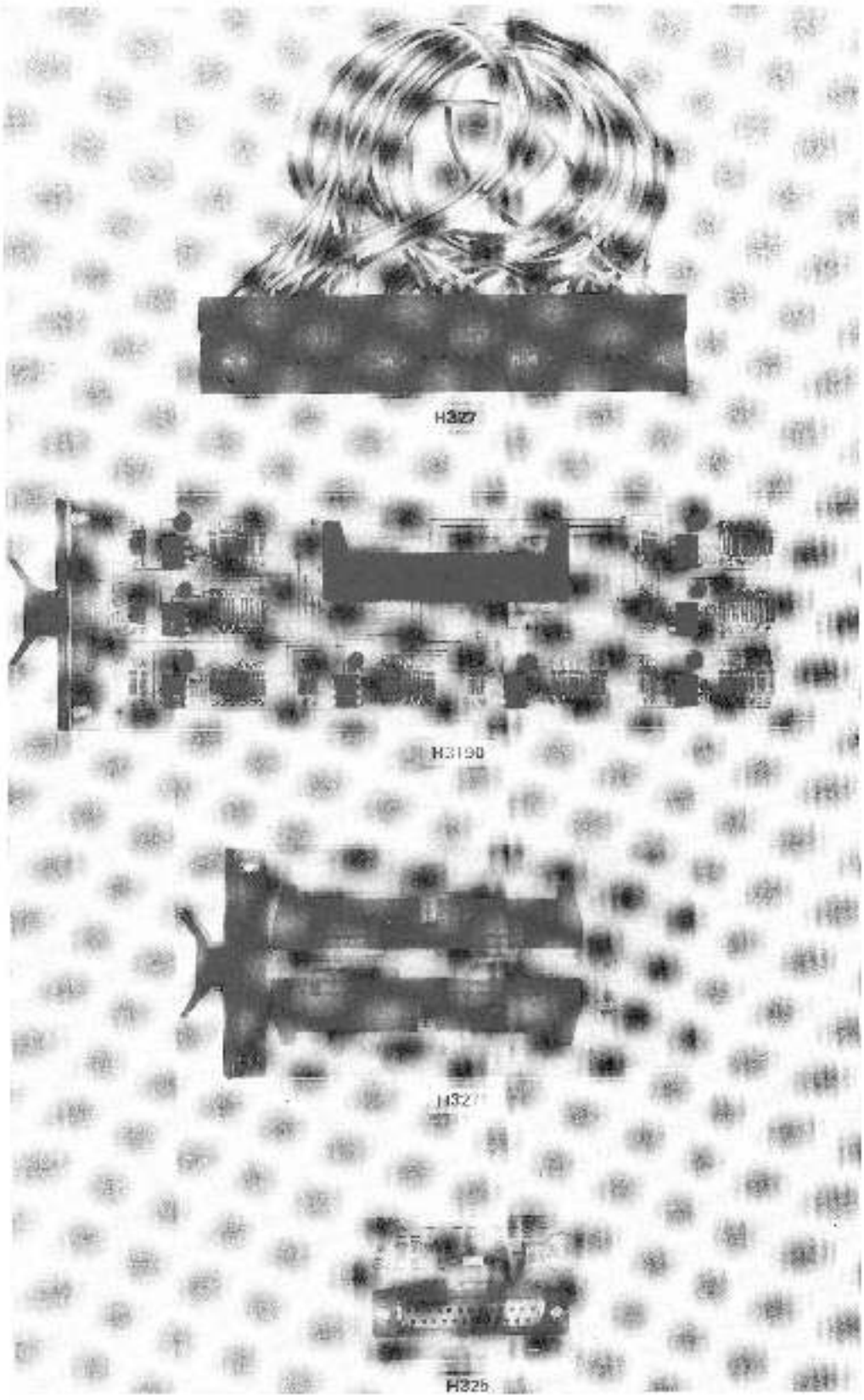


Figure 1-7 Test Connectors H327, H3190, H3271, and H325

1.3 GENERAL SPECIFICATIONS

The following paragraphs contain electrical, environmental, and performance specifications for all DZ11 configurations. Table 1-2 lists the performance parameters of DZ11.

1.3.1 Outputs

1.3.1.1 DZ11-A, -B, and -E - Each line provides voltage levels and connector pinnings that conform to ELECTRONIC INDUSTRIES ASSOCIATION (EIA) standard RS232C and CCITT recommendation V.24. The leads supported by this option are:*

a. Circuit AA (CCITT 101) - Pin 1 Protective Ground
b. Circuit AB (CCITT 102) - Pin 7 Signal Ground
c. Circuit BA (CCITT 103) - Pin 2 Transmitted Data
d. Circuit BB (CCITT 104) - Pin 3 Received Data
e. Circuit CD (CCITT 108.2) - Pin 20 Data Terminal Ready
f. Circuit CE (CCITT 125) - Pin 22 Ring Indicator
g. Circuit CF (CCITT 109) - Pin 8 Carrier

NOTE

Signal Ground and Protective Ground are connected together.

*Circuit CA (CCITT 105, Request to Send, is connected to circuit CD (DTR) through a jumper on the distribution panel. This allows the H325 or H315 test connector to turn around DTR into both CD and RI (circuits CF and CE). It also allows control of the Request to Send (RTS) (CA) line for full duplex modem data set applications that use the 202 data set.

1.3.1.2 DZ11-C, -D, and -F - Each line is a 20 mA current loop used for connection to local terminals (no data set control is provided). All lines are active and, therefore, can only drive a passive device. However, a pair of H3'9 20 mA receivers (for each line) may be used to convert from active to passive operation in order to allow the DZ11 to drive an active device.

1.3.2 Inputs

The PDP-11 Unibus is the input for all DZ11s. The DZ11-A, B, C, and D present one unit load to the Unibus and the DZ11-E and -F present two unit loads to the Unibus.

1.3.3 Power Requirements, DZ11-A, -B, and -E*

Typical	Maximum	
2.2	2.5	amperes at + 5.0 volts, dc
0.13	0.15	amperes at -15.0 volts, dc
0.1	0.13	amperes at +15.0 volts, dc

1.3.4 Power Requirements, DZ11-C, -D, and -F*

Typical	Maximum	
2.1	2.3	amperes at + 5.0 volts, dc
0.4	0.42	amperes at -15.0 volts, dc
0.12	0.15	amperes at +15.0 volts, dc

*DZ11-E and DZ11-F are twice the above given values.

1.3.5 Environmental Requirements - all DZ11s:

Class C Environment Operating Temperature:	5° C to 50° C* (41° F to 122° F)
Relative Humidity:	10% or less to 95%, with a maximum wet bulb of 32° C (90° F) and a minimum dewpoint of 2° (36° F)

Cooling

DZ11-A, -B, -C, and -D:	Air flow 3 cu. feet/min.
DZ11-E and -F:	Air flow 6 cu. feet/ min.

Heat Dissipation

DZ11-A and -B:	57 Btu/hr
DZ11-E:	114 Btu/hr
DZ11-C and -D:	93 Btu/hr
DZ11-P:	110 BTU/hr

*Maximum operating temperature is reduced 1.8° C per 1000 meters (1.0° F per 1000 feet) for operation at altitude.

1.3.6 Distortion - DZ11-A, -B, and -E

The maximum "space to mark" and "mark to space" distortion allowed in a received character is 40%.

The maximum speed distortion allowed in a received character for 2000 baud is 3.8%. All other baud rates allow 4%. The maximum speed distortion from the transmitter for 2000 baud is 2.2%. All other baud rates have less than 2%.

1.3.7 Interrupts

RDONE - Occurs each time a character appears at the silo output.

SA - Silo Alarm, occurs after 16 characters enter the silo. Rearmed by reading the silo. This interrupt disables the RDONE interrupt.

TRDY - Occurs when the scanner finds a line ready to transmit on.

NOTE

There are no modem interrupts.

1.3.7.1 Interrupt Level - Normally, Level 5 priority plug is supplied. The interface level can be modified to Level 4, 6, or 7 by using the proper priority plug.

Table 1-2 DZ11 Performance Parameters

PARAMETER	DESCRIPTION			
Operating Mode:	Full Duplex			
Data Format:	Asynchronous, serial by bit, one start and 1, 1-1/2 (5 level codes only), or 2 stop bits supplied by the hardware under program control.			
Character Size:	5, 6, 7, or 8 bits - program selectable. (Does not include parity bit.)			
Parity:	Parity is program selectable. There may be none, or it may be odd or even.			
Bit Polarities:	Unibus	Interface	EIA Out	20 MA Loop
DATA SIGNAL	Low = 1 High = 0	High = 1 Low = 0	Low = 1 = MARK High = 0 = SPACE	0-5 MA 15-20 MA
CONTROL SIGNAL	Low = 1 High = 0	High = 1 Low = 0	Low = OFF High = ON	
Order of Bit:	Transmission/reception low order bit first			

Table 1-2 DZ11 Performance Parameters (Cont)

PARAMETER	DESCRIPTION
Baud Rates:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, and 9600.
Breaks:	Can be generated and detected on each line.
Throughput:	21,940 characters/sec = *

$$*: \frac{(\text{Bits/second} \times \text{No. Lines} \times \text{direction})}{\text{Bits/Character}} = \text{See Example}$$

Example: $\frac{(9600 \times 8 \times 2)}{7} = 21,940$ characters/sec

NOTE

21,940 is a theoretical maximum. Actual throughput is dependent on other factors such as type of CPU, system software, etc.

Line Speed: The baud rate for a line (both transmitter and receiver) is program selectable. Also, the receiver for each line can be individually turned on or off under program control. (See Baud Rates in Table 1-2 for a list of available baud rates).

Distance: DZ11-A, -B, and -E -

15 meters (50 feet) at up to 9600 baud with a BC05D cable or equivalent.

Operation beyond 50 feet does not conform to the RS232C or CCITT V.24 specifications. However, operation will often be possible at longer distance depending on the terminal equipment, type of cable, speed of operation and electrical environment. Reliable communication over long cables depends on the absence of excessive electrical noise. For these reasons, Digital can not guarantee error free communication beyond 50 feet. However, the EIA versions of the DZ11 may be connected to local Digital terminals (and most other terminals at distances beyond 50 feet with satisfactory results if the

terminal and computer are located in the same building, in a modern office environment. Shielded twisted pair (Belden 8777 or equivalent) is recommended and is used in the BC03M null modem cable.

With cable made with shielded twisted pairs, such as the Belden 8777 or equivalent, the following rate/distance table may be used as a guide. This chart is for informational purposes only and is not to be construed as a warranty by Digital Equipment Corporation of error free operation of the DZ11 at these speeds and distances under all circumstances.

90 m	(300 feet) at 9600 Baud
300 m	(1000 feet) at 4800 Baud
300 m	(1000 feet) at 2400 Baud
900 m	(3000 feet) at 1200 Baud
1500 m	(5000 feet) at 300 Baud

NOTE

The ground potential difference between the DZ11 and terminal must not exceed two volts. This requirement will generally limit operation to within a single building served by one AC power service. In other cases, or in noisy electrical environments, 20 mA operation should be used.

DZ11-C, -D, and -F -

The length of cable that may be used reliably is a function of electrical noise, loop resistance, cable type, and speed of operation. The following chart is given as a guide, however, there is no guarantee of error-free operation under all circumstances.

SPEED (Baud)	Belden 8777, 22 AWG, shielded, twisted pairs (shields floating) DEC P/N 9107723	22 AWG, 4 conductor inside station wire DEC P/N 9105856-4
9600	150 m (500 ft)	300 m (1000 ft)
4800	300 m (1000 ft)	540 m (1800 ft)
2400	600 m (2000 ft)	900 m (3000 ft)
1200 and below	1200 m (4000 ft)	1500 m (5000 ft)

1.4 FUNCTIONAL DESCRIPTION

The following paragraphs present a general description of DZ11 operation. Figure 1-8 is a general functional block diagram that divides the DZ11 into three basic components: Unibus Interface, Control Logic, and Line Interface.

1.4.1 PDP-11 Unibus Interface

The PDP-11 Unibus Interface component of the DZ11 handles all transactions between the Unibus and the DZ11 Control Logic. The Unibus Interface performs three functions: data handling, address recognition, and interrupt control. In its data handling function, the Interface routes data to and from the various registers in the Control Logic and provides the voltage conditioning necessary to transmit and receive data to and from the PDP-11 Unibus. The address recognition and control logic activates the proper load and read signals when it recognizes its preselected address on the Unibus. These signals are used by the data handling function to route the incoming and outgoing data to the desired locations. The interrupt control function initiates and controls interrupt processing between the DZ11 and the PDP-11 processor.

1.4.2 Control Logic

The Control Logic provides the required timing and control signals to handle all transmitter and receiver operations. The Control Logic can be divided into two major sections: the scanner and the registers. The scanner continuously examines each line in succession, and based on information from the Line Interface and the registers, it generates signals that cause data to flow to or from the appropriate line.

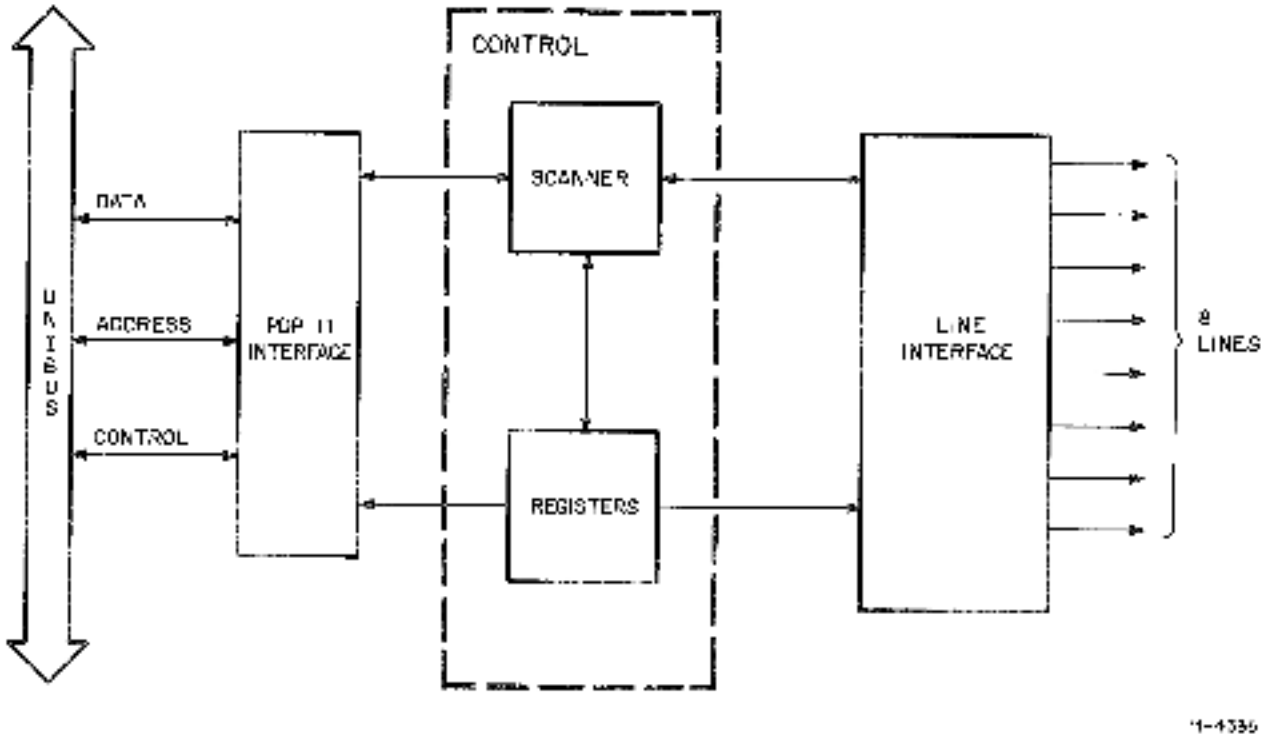


Figure 1-8 General Functional Block Diagram

The scanner comprises a 5.068 MHz oscillator (clock), a 64-word FIFO receiver buffer, a four-phase clocking network, and other control generating logic.

The DZ11 uses four Device Registers in a manner that yields six unique and accessible registers, each having a 16-bit word capacity. The six discrete registers temporarily store input and output data, monitor control signal conditioning, and establish DZ11 operating status. Depending on their functions, some of the registers are accessible in bytes or words; others are restricted to word-only operation. Registers can be read or loaded (written), depending on the operation. The ability to read or write a register allows the use of two of the Device Registers as four independent registers.

1.4.3 Line Interface

Two of the most important operations in the DZ11 are the conversions from serial-to-parallel and parallel-to-serial data formats. These conversions are required since the DZ11 is located between the PDP-11 Unibus (a parallel data path) and either local terminals or telephone lines (serial data paths). Conversions for each line in the DZ11 are performed by independent Universal Asynchronous Receiver-Transmitter (UART) integrated circuits. Another component of the Line Interface, the Line Receiver or Driver, converts the TTL voltage levels in the DZ11 so that they correspond to those in the external device input lines (modem or terminal).

CHAPTER 2

INSTALLATION

2.1 SCOPE

This chapter contains the procedures for the unpacking, installation, and initial checkout of the DZ11 Asynchronous Multiplexer.

2.2 CONFIGURATION DIFFERENCES

The DZ11 can be supplied with or without a distribution panel. The DZ11-B and -D do not have distribution panels. The following list describes the variations:

DZ11-A EIA level conversion with distribution panel (8 lines)

DZ11-B EIA level conversion without distribution panel (8 lines)

DZ11-C 20 mA loop conversion with distribution panel (8 lines)

DZ11-D 20 mA loop conversion without distribution panel (8 lines)

DZ11-E DZ11-A and DZ11-B (16 lines)

DZ11-F DZ11-C and DZ11-D (16 lines)

2.3 UNPACKING AND INSPECTION

The DZ11 is packaged in accordance with commercial packaging practices. First, remove all packing material and check the equipment against the shipping list. Damage or shortages should be reported to the shipper immediately, and notification given the DEC representative. Inspect all parts and carefully inspect the module for cracks, loose components, and separations in the etched paths. Table 2-1 contains a list of supplied items per configuration.

2.4 INSTALLATION PROCEDURE

The following paragraphs should be followed to install the DZ11 module in a PDP-11 system.

Table 2-1 Items Supplied Per Configuration

Quantity	Description	A	B	E	C	D	F
1	M7819 Module	x	x	*			
1	H3271 Test Connector**	x		x			
1	H317-E Distribution Panel Assembly	x		x			
1	H325 Test Connector	x		x			
1	BC05W-15 Cable	x	x	*			
1	Printset (B-TC-DZ11-0-6)	x		x			
1	Printset (B-TC-DZ11-0-10)		x				
1	Software Kit	x		x	x		x
1	Panel Mounting Hardware Set	x		x	x		x
1	Priority Insert (5)	x	x	*	x	x	*
1	DZ11 User's Manual (EK-DZ11-OP-001)	x		x	x		x
1	M7814 Module				x	x	*
1	BC08S Cable				x	x	*
1	H317-F Distribution Panel Assembly				x		x
1	Printset (B-TC-DZ11-0-11)				x		x
1	Printset (B-TC-DZ11-0-12)					x	
1	H3190 Test Connector***				x	x	*

*Shipment contains two of the items listed.

**New item: An H327 will be shipped with each M7819 unit until this one becomes available. Check shipping list to see if there is one.

***New item; Check shipping list to see if there is one.

2.4.1 M317 Distribution Panel Installation

Install the M317 Distribution Panel according to the Unit Assembly Drawing D-UA-DZ11-0-0.

2.4.1.1 EIA Option - For the DZ11-A or DZ11-E option, check to ensure that all of the machine-insertable jumpers on the Distribution Panel are in place. See Drawing E-UA-5411328-0-0 in the Printset for jumper locations. These jumpers are in anticipation of future use of the DZ11 with modems other than the 103; however, two of the jumpers are now functional. The jumper labeled DTR (Refer to D-CS-5911328-0-1) connects DTR to pin 4 or Request to Send. This allows the DZ11 to assert both DTR and RTS if using a 202 data set. The jumper labeled BUSY is also connected to the DTR lead for use in modems that implement the Force Busy function. This jumper should normally be cut out unless the modem has the Force Busy feature and the software implemented to control it.

2.4.1.2 20 mA Option - For the DZ11-C or DZ11-F option, refer to D-UA-5411974-0-0. Each line has a jumper on the Distribution Panel (W1 through W16) which should be in if the terminal operates at 300 baud or less. The jumper should be removed for higher baud rates.

2.4.2 M7819 Module Installation

To install the M7819 module, perform the following:

a. Ensure that the Priority Insert (level 5) is properly seated in socket E52 on the M7819 module(s). Refer to drawing D-UA-M7819-0-0.

b. Refer to paragraph 2.1.1 for descriptions of the Address Assignments. Set the switches at E87 such that the module will respond to its assigned address. When a switch is closed (on), a binary 1 is decoded. When a switch is open (off), a binary 0 is decoded. Note that the switch labeled #1 corresponds to bit 3, #2 corresponds to bit 4, etc. See Figure 2-1.

c. Vector selection is accomplished by the eight-position switch at E11. Switch position #1 and #8 are not used. Switch position #2 corresponds to vector bit 3, #3 corresponds to vector bit 4, etc. When a switch is closed (on), a binary 0 is decoded. When a switch is open (off), a binary 1 is decoded. Note that this is opposite of the address switch decoding. See Figure 2-2.

d. If you do not have the new H3271 test connector, go to step g, otherwise do the following:

1. Insert the module (s) into an SPC slot and connect the flat shielded cable (BC05W-15) to J1 on the module(s). Connect the other end of the cable to the H3271.*

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides, and possibly changing switch settings inadvertently.

*The H3271 has room for two H7819 cables.

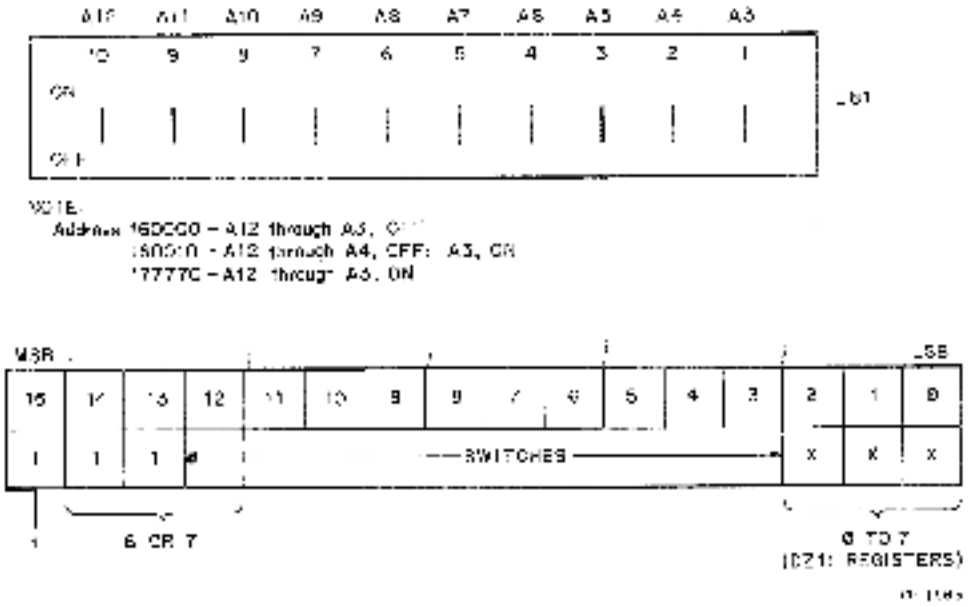
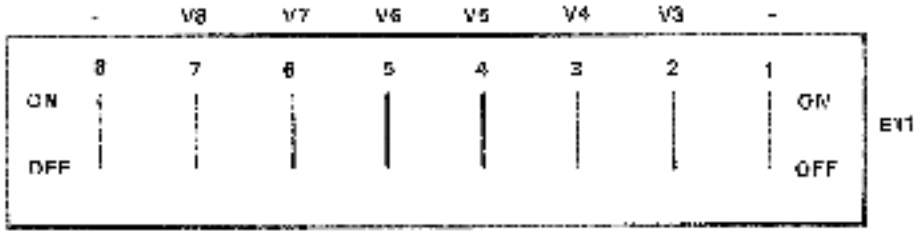


Figure 2-1 M7819 Address Selection



NOTE:

- = OFF

ON = ON

VECTOR	V8	V7	V6	V5	V4	V3
300	ON	-	-	ON	ON	ON
310	ON	-	-	ON	ON	-
.			.	.	.	.
.			.	.	.	.
770	-	-	-	-	-	-

11-a814

Figure 2-3 M7819 Vector Selection

2. Run the DZ11 diagnostic in staggered mode to verify module operation. Refer to MAINDEC-11-DZDZA, the diagnostic listing. Run at least two passes without error.

3. Remove the BC05W-15 cable(s) from the H3271 and insert it at J18 or J20 on the H317-E Distribution Panel. BE SURE THAT A TWIST IS PUT IN THE CABLE. See Figure 2-3.

4. Go to step h.

e. Ensure that the H327 Test Connector is properly installed at J1 (the cable connector at the top of the M7819).

f. Insert the M7819 in its SPC slot and run diagnostic in the staggered mode to verify module operation. Refer to MAINDEC-11-DZDZA, the diagnostic listing for the correct procedure. Run at least two passes without error.

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides, and possibly changing switch settings inadvertently.

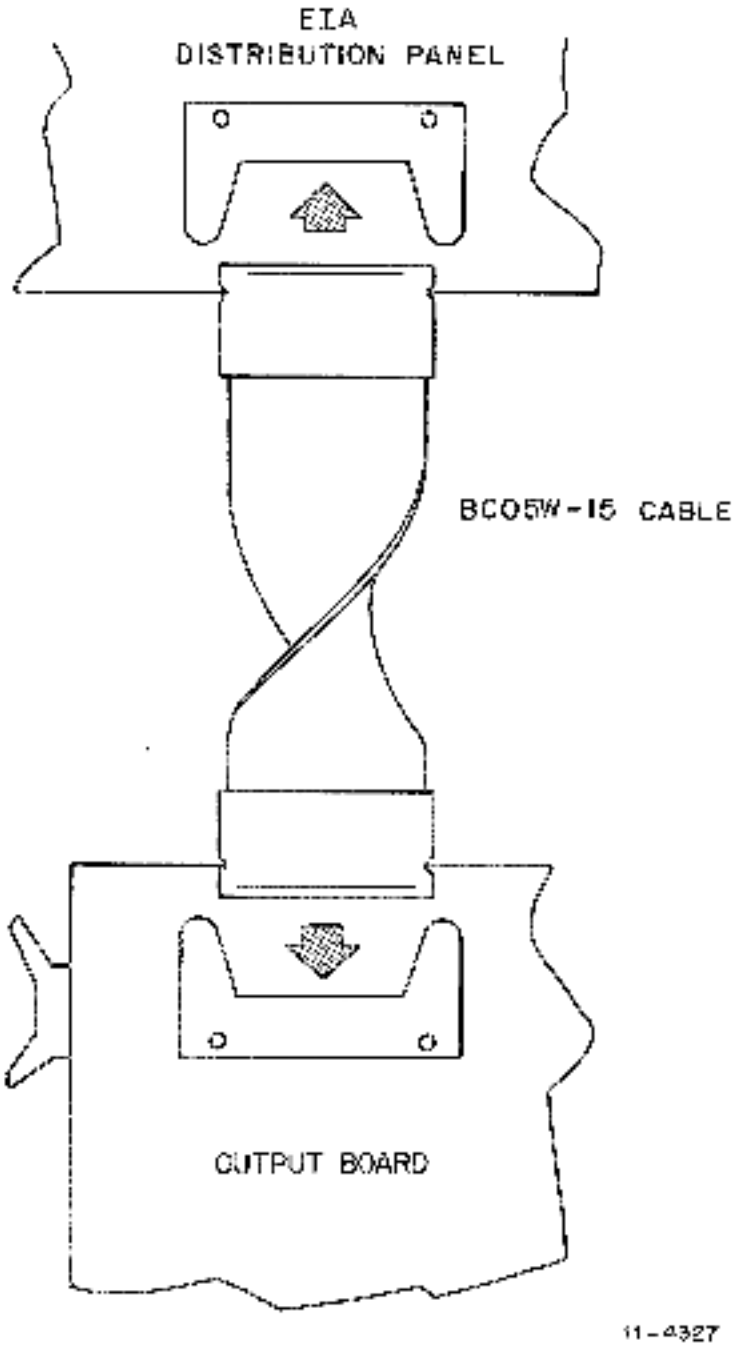


Figure 2-3 BC05X-15 Interconnection

g. Replace the H327 Test Connector with the BC05W-15 cable, and observe the same caution as in Step f above. Insert the other end of the cable at J18 or J20 of the Distribution panel. BE CERTAIN THAT A TWIST IS MADE IN THE CABLE. See Figure 2-3.

h. Connect the H325 (or an H315) connector to the first line and run the Diagnostics in External mode. Repeat this step for each line.

i. Run DEC/X11 System Exerciser to verify the absence of Qubus interference with other system devices.

j. The DZ11 is now ready for connection to external equipment. If EIA (H317-E), and the connection is to a terminal, a null modem cable must be used. The BC03M, H312-A, or BC03J null modem cables will suffice for connection between the Distribution panel and the terminal. However, if the H312-A null modem unit is used, two BC05D EIA cables (one on each side of the null modem unit) are required. If connection is to a Bell 103 or equivalent modem, a BC05D-25 foot cable is required between the Distribution panel and the modem. All of the cables mentioned must be ordered

separately as they are NOT components of a standard DZ11 shipment. If 20 mA (H317-F), then the connection to the terminal is by a customer supplied cable. Run the echo test for both 20 mA and 61A without error.

2.4.3 M7814 Module Installation

To install the M7814 Module, perform the following:

a. Ensure that the priority insert (level 5) is properly seated in socket E41. Refer to drawing D-UA-M7814-0-0.

b. Refer to paragraph 3.1.1 for a description of address assignments. Set the switches at E72 such that the module will respond to its assigned address. When a switch is closed (on), a binary 1 is decoded. When a switch is open (off), a binary 0 is decoded. Note that the switch labeled #1 corresponds to bit 3, #2 to bit 4, etc. See Figure 2-4.

c. Vector selection is by an eight-position switch at E91 on the module(s). When a switch is closed (on), a binary 0 is decoded. When a switch is open (off), a binary 1 is decoded. Note that this is the opposite of the address switch decoding. Also note, that switch positions #1 and #8 are not used and switch #6 corresponds to bit 3, #5 to bit 4, etc. Refer to Figure 2-5.

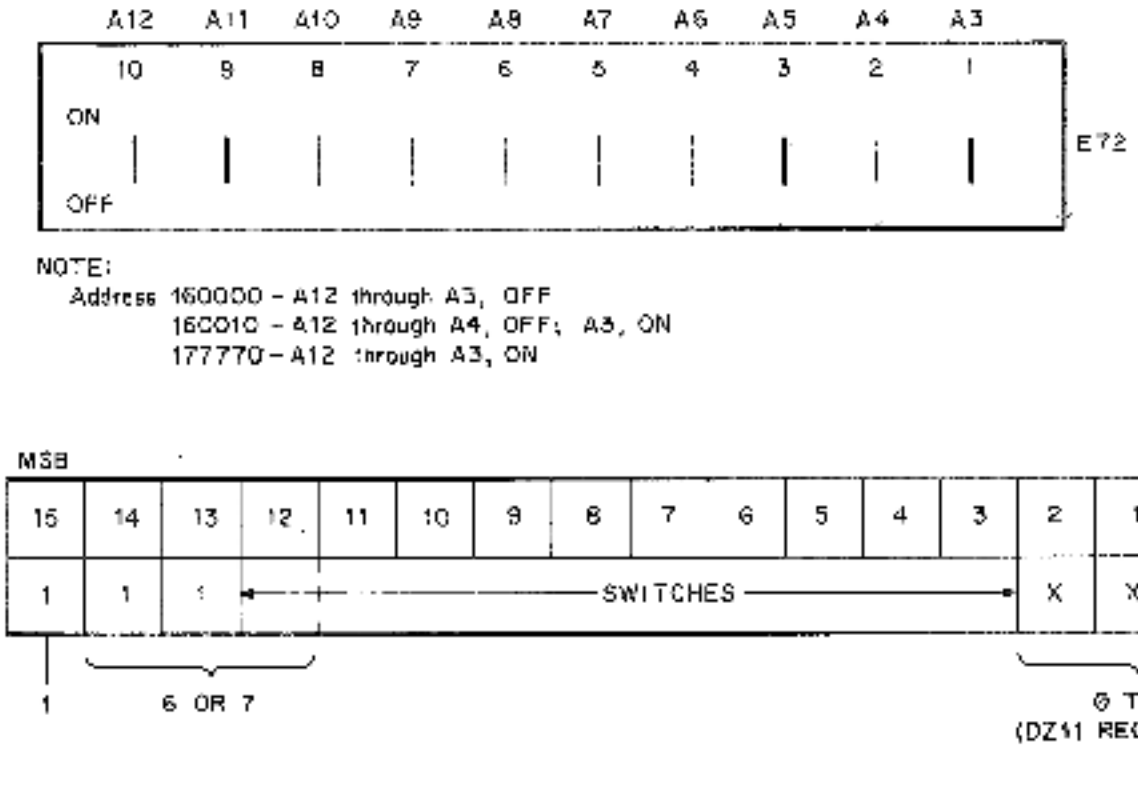
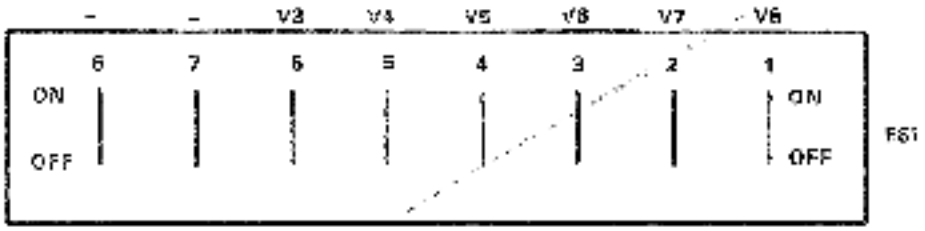


Figure 2-4 A7814 Address Selection



NOTE:

- = OFF

ON = ON

VECTOR	V8	V7	V6	V5	V4	V3
300	ON	-	-	ON	ON	ON
310	ON	-	-	ON	ON	-
770	-	-	-	-	-	

11-5143

Figure 2-5 M7814 Vector Selection

CAUTION

Insert and remove modules slowly and carefully to avoid snagging module components on the card guides, and possibly changing switch settings inadvertently.

d. Connect the BC08S cable to J1 on the module(s). Insert module(s) into their assigned SPC slot(s).

e. Skip this step if you have an H3190 test connector otherwise do the following:

1. Connect the other end of the BC08S cable to J1 or J2 on the distribution panel (H317-F).
2. Run the DZ11 diagnostic in internal (Maintenance) mode for two error free passes. Refer to MAINDEC-11-DZDZA, the diagnostic listing, for the proper procedure.
3. Go to step f.

f. Connect the other end of the BC08S cable to the H3190 test connector.

g. Run the DZ11 diagnostic in staggered mode for two error free passes. Refer to MAINDEC-11-DZDZA, the diagnostic listing, for the correct procedure.

h. Remove the BC08R cable from the H3190 test connector and plug it into J1 or J2 on the distribution panel (H317-F).

i. Run the DEC/X11 system exerciser to verify the absence of unibus interference with other system devices.

j. The DZ11 is now ready for connection to external equipment. This is accomplished with a customer supplied cable. When hookup is complete run the echo test on each line without any errors occuring.

NOTE

For customer terminals that can only transmit or receive in a single direction, the echo test can not be run.

CHAPTER 3

PROGRAMMING

3.1 INTRODUCTION

This chapter provides basic information for programming the DZ11. A description of each DZ11 register, its format, programming constraints, and bit functions are presented to aid programming and maintenance efforts. Special programming features are also presented in this chapter.

3.1.1 Device and Vector Address Assignments

The DZ11's device and vector addresses are selected from the floating vector and device address space.

NOTE

The device floating address space is 160010_8 to 163776_8. The vector floating address space is 300_8 to 776_8.

Its floating address space follows the DJ11; DH11; DQ11; DU11; DUP11; LK11; and DMC11.

Its floating vector space follows the DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DN11-BB and other modem control vectors; DR11-A; DR11-C; PA611 reader, PA611 punch; DT11; DX11; DL11-C, D, E; DJ11; DH11; GT40; LPS11; DQ11; KW11-W; DU11; DUP11; CV11; LK11-A; DWUN;

and DMC11. If a DZ11 is installed in a system with any of the above listed options, then its assigned vector and device address should follow the vector and device address of the other options.

Two examples follow:

First, the simplest case where there is only one DZ11:

Option	Address	Vector	Comment
GAP	160010		No DJ11s
GAP	160020		No DH11s
GAP	160030		No DQ11s
GAP	160040		No DU11s
GAP	160050		No DUP11s
GAP	160060		No LK11s
GAP	160070		No DMC11s
DZ11	160100	300	
GAP	160110		No more DZ11s

Next, a system with one DJ11, one DH11, one GT40, one KW11-W and two DZ11s.

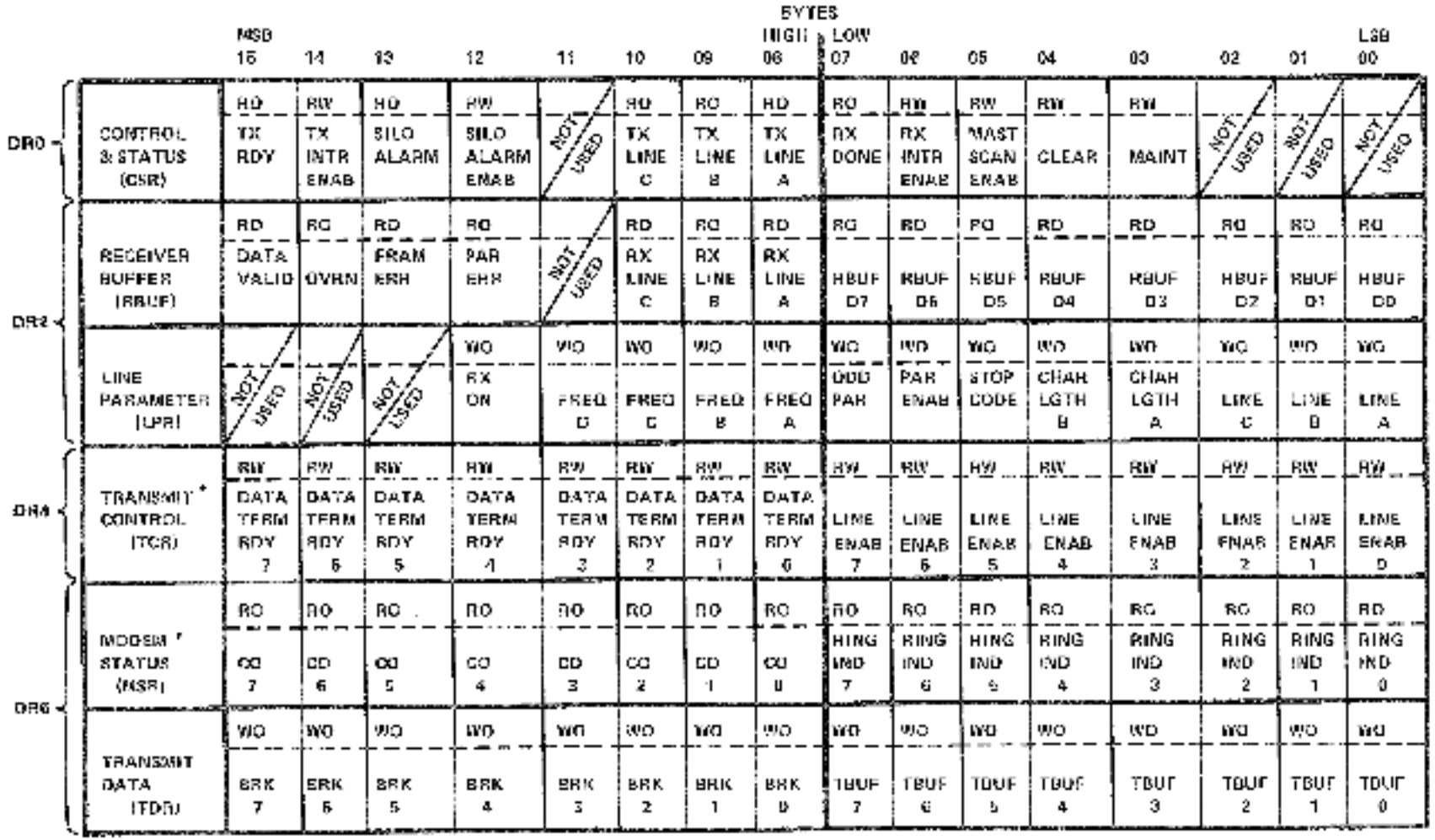
Option	Address	Vector	Comment
DJ11	160010	300	
GAP	160020		No more DJ11s
GAP	160030		DH11 must start on an address boundary that is a multiple of 20.
DH11	160040	310	
	160050		
GAP	160060		No more DH11s
GT40		320	GT40 address is not in the floating address space.
KW11-W		330	KW11-W address is not in the floating address space.
GAP	160070		No DQ11s
GAP	160100		No DU11s
GAP	160110		No DUP11s
GAP	160120		No LK11s
GAP	160130		No DMC11s
DZ11	160140	340	
DZ11	160150	350	
GAP	160160		No more DZ11s

3.2 REGISTER BIT ASSIGNMENTS

A comprehensive pictorial of all register bit assignments is shown in Figure 3-1. The four device registers (DR0, DR2, DR4, and DR6) are subdivided to form six unique registers. This subdivision is accomplished in DR2 and DR6 by assigning read-only (RO) or write-only (WO) status to each register. Since the reading and writing of DR2 and DR6 accesses two registers, PDP-11 processor instructions that perform a read-modify-write (DATIP) bus cycle cannot be used with DR2 or DR6. Also, DR2 permits only word instructions, but either byte or word instructions may be used with DR6. DR0 and DR4 have no programming constraints. In all register operations, the following applies: read-only bits are not affected by an attempt to write, and write-only and "not-used" bits appear as a binary 0 if a read operation is performed. Specific programming constraints for each register are discussed in the following paragraphs. A description of each bit function is presented in Tables 3-1 through 3-3.

3.2.1 Control and Status Register (CSR)

The control and status register (CSR) contains the states of flags and enable bits for scanning, processor interrupts, clearing and maintenance. The 16-bit CSR has no programming constraints. The format is depicted in Figure 3-1, and bit functions are described in Table 3-1. Write-only and "not-used" bits read as zeros to the Unibus, and read-only bits are not affected by write attempts.



		BYTES HIGH								BYTES LOW							
		MSB 15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	LSB 00
DR0	CONTROL & STATUS (CSR)	RO	RW	RO	RW	NOT USED	RO	RO	RO	RO	RW	RW	RW	RW	NOT USED	NOT USED	NOT USED
		TX RDY	TX INTR ENAB	SILO ALARM	SILO ALARM ENAB		TX LINE C	TX LINE B	TX LINE A	RX DONE	RX INTR ENAB	MAST SCAN ENAB	CLEAR	MAINT			
DR2	RECEIVER BUFFER (RBUF)	RO	RO	RO	RO	NOT USED	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
		DATA VALID	OVRN	FRAM ERR	PAR ERR		RX LINE C	RX LINE B	RX LINE A	RBUF D7	RBUF D6	RBUF D5	RBUF D4	RBUF D3	RBUF D2	RBUF D1	RBUF D0
	LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
					RX ON	FREQ D	FREQ C	FREQ B	FREQ A	ODD PAR	PAR ENAB	STOP CODE	CHAR LGTH B	CHAR LGTH A	LINE C	LINE B	LINE A
DR4	TRANSMIT * CONTROL (TCR)	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
		DATA TERM RDY 7	DATA TERM RDY 6	DATA TERM RDY 5	DATA TERM RDY 4	DATA TERM RDY 3	DATA TERM RDY 2	DATA TERM RDY 1	DATA TERM RDY 0	LINE ENAB 7	LINE ENAB 6	LINE ENAB 5	LINE ENAB 4	LINE ENAB 3	LINE ENAB 2	LINE ENAB 1	LINE ENAB 0
DR6	MODEM * STATUS (MSR)	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
		CD 7	CD 6	CD 5	CD 4	CD 3	CD 2	CD 1	CD 0	RING IND 7	RING IND 6	RING IND 5	RING IND 4	RING IND 3	RING IND 2	RING IND 1	RING IND 0
	TRANSMIT DATA (TDR)	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
		BRK 7	BRK 6	BRK 5	BRK 4	BRK 3	BRK 2	BRK 1	BRK 0	TBUF 7	TBUF 6	TBUF 5	TBUF 4	TBUF 3	TBUF 2	TBUF 1	TBUF 0

* The High byte of the TCR (Data Terminal Ready) and the MSR are not used with the 20ma options.

Figure 3-1 Register Bit Assignments

Table 3-1 CSR Bit Functions

Bit	Title	Function
0-2	Not Used	
3	MAINT	A read/write bit, when set, causes the serial output data from the transmitter to be fed back as serial input data to the receiver. All lines are turned around. Bit is cleared by BUS INIT and CLR.
4	CLR (clear)	A read/write bit that fires a one-shot to generate a 15-microsecond reset which clears the receiver silo, all UARTs, and the CSR. After a CLR is issued, the CSR and line parameters must be set again. CLR in progress is indicated by CLR = 1. Modem control registers are not affected, nor bits 00 through 14 of RBUF.
5	Master Scan Enable	A read/write bit that activates the scanner to enable the Receiver Transmitter and Silo. Cleared by CLR and BUS INIT.
6	RCV INT Enable	A read/write bit that enables the receiver interrupt. Cleared by CLR and BUS INIT.

Table 3-1 CSR Bit Functions (Cont)

Bit	Title	Function
7	RDONE	A read only bit (hardware set) that generates a RCV INT if bit 06 = 1 and bit 12 = 0. The bit clears when the RBUF is read and resets when another word reaches the output of the silo (RBUF). If bit 06 = 0, RDONE can be used as a flag to indicate that the silo contains a character. If bit 12 = 1, RDONE does not cause interrupts but otherwise acts the same.
8-10	Tran Line#	When bit 15 = 1, these three read-only bits indicate the line that is ready to transmit a character. Bit 15 clears when the character is loaded into the transmit buffer, but sets again if another line is ready. A new line number could appear within a minimum of 1.8 microseconds. The bits 08-10 return to line 0 after a CLR or BUS INIT. These bits are meaningful only when bit 15 (TRDY) is true.
11	Not Used	

Table 3-1 CSR Bit Functions (Cont)

Bit	Title	Function
12	SAE (Silo Alarm Enable)	A read/write bit that enables the silo alarm and prevents RDONE from causing interrupts. If bit 06 = 1, the SAE allows the SA (bit 13) to cause an interrupt after 16 entries in the silo. If bit 06 = 0, the SA can be used as a flag. The bit is cleared by CLR and BUS INIT.
13	SA (Silo Alarm)	A read-only bit set by the hardware after 16 characters enter the silo. It causes an interrupt if bit 06 = 1 and is cleared by CLR, BUS INIT, and reading the RBUF. When the silo flag occurs (SA = 1), the silo must be emptied because the flag will not be set again until 16 additional characters enter the silo.
14	TIE (Tran Int Enab)	A read/write bit that allows an interrupt if bit 15 = 1 (TRAN Ready).

Table 3-1 CSR Bit Functions (Cont)

Bit	Title	Function
15	TRDY (Tran Ready)	A read-only bit set by hardware when a line number is found that has its transmit buffer empty and its LINE ENAB bit set. It is cleared by CLR, BUS INIT, and by loading the TBUF register.

3.2.2 Receiver Buffer (RBUF)

The receiver buffer (RBUF) register contains the received character bits, with line identification, error status, and data validity flag. As one of two registers in DR2 (RBUF and LPR), RBUF is accessed when a read operation is performed (write operation accesses the LPR). The RBUF register has several programming constraints which are:

1. Byte instructions cannot be used.

2. It is a "Read Only" register.

3. TST or BIT instructions cannot be used as they cause the loss of a character.

4. The register requires master scan Enable (CSR bit 5) to be set in order to be functional. When this bit is off, bits 00 to 14 of the RBUF become invalid regardless of the state of bit 15 (DATA VALID) and the silo is held

empty. The register format of RBUF is depicted in Figure 3-1 and bit functions are described in Table 3-2. Each reading of the RBUF register advances the silo and presents the next character to the program. Bits 00 through 14 do not go to zero after a CLR or BUS INIT; however, they become invalid and the silo is emptied. Bit 15 (Data Valid) does clear to zero and is explained in Table 3-2.

3.2.3 Line Parameter Register (LPR)

The line parameter register (LPR) is a 16-bit register that sets the parameters (character and stop code lengths, parity, speed, and receiver clock) for each line. Bits 00-02 select the line for parameter loading. Line parameters for each line must be reloaded after a CLR (bit 04 of CSR) or BUS INIT operation. The programming constraints for the LPR are:

1. It is a write only register.
2. BIS or BIC instructions are not allowed.
3. Byte operations cannot be used.

Table 3-2 RBUF Bit Functions

Bit	Title	Function
0-7	RCV Character	These bits contain the received character. If the selected code level is less than 8 bits wide, the high order bits are forced to zero.
8-10	Line Number	These bits present the line number on which the character was received.
11	Not Used	
12	Parity Error	This bit indicates whether the received bit had a parity error. The parity bit is generated by hardware and does not appear in the RBUF word.
13	Framing Error	This bit indicates improper framing (stop bit not a mark) of the received character, and can be used for break detection.
14	Overrun	This bit indicates receiver buffer overflow. The result is a received character which is replaced by another received character before storage in the

Table 3-2 RBUF Bit Functions (Cont)

Bit	Title	Function
		silo. A character is lost but the received character put in the silo is valid.
15	Data Valid	This bit indicates that the character read from the silo (RBUF) is valid. The RBUF is read until the DV bit = 0, indicating an invalid character and empty silo. Bit is cleared by CLR and BUS INIT.

Table 3-3 LPR Bit Functions

Bit	Title	Function
0-2	Line Number	These bits select the line for parameter loading.
3-4	Character Length	These bits set the character length for the selected line. The parity bit is not part of the character length.

4	3	
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

5	Stop Code	This bit sets the Stop Code length. (0 = One-unit stop, 1 = Two-unit stop or 1.5-unit stop if a 5-level code is employed.)
6	Parity	This bit selects the parity option (0 = No parity check, 1 = Parity enabled on TRAN and RCV.)
7	Odd Parity	This bit selects the kind of parity selected (0 = Even Parity Select, 1 =

Table 3-3 LPR Bit Functions (Cont)

Bit	Title	Function
		Odd Parity Select.) Bit 06 must be set for this bit to have effect.
8-11	Speed Select	These bits select the TRAN and RCV speed for the line selected by bits 0-2. Refer to Table 3-4 for list of available baud rates.
12	RCVR ON	This bit must be set when loading parameters to activate the receiver clock. (Transmitter clock is always on.) A CLR or BUS INIT turns the receiver clock off.

3.2.4 Transmit Control Register (TCR)

The Transmit Control Register contains sixteen (16) bits for the EIA options (M7819 module) and eight (8) bits for the 20 mA option (M7814 module). The difference is that the Data Terminal Ready (DTR) lines that make up the high byte (bits 8 through 15) of the TCR are not used by the 20 mA options because they do not have modem control capabilities.

The high byte (M7819 only) contains a Read/Write DTR bit for each line. This byte is cleared by BUS INIT only, not CLR. When the high byte is not used (M7814 only), it reads back to the Unibus as all zeros. Also, attempts to write into it, will have no effect. The low byte contains a Read/Write Line Enable bit for each line. A set bit allows transmission on the corresponding line. Paragraph 3.3.7 explains how to properly use this bit. This byte is cleared by CLR and BUS INIT.

3.2.5 Modem Status Register (MSR)

This is a 16 bit register used only with the EIA options (M7819 module). The 20 mA options (M7814 module) do not have modem control capabilities. When not used, this register reads all zeroes to the Unibus.

The MSR consists of two bytes: The low byte (bits 00 through 07) and the high byte (bits 08-15). The low byte monitors the state of each line's Ring Indicator (RI) lead; the high byte monitors

the state of each line's carrier (CO) lead. The MSR is the Read only portion of DR6 and has the following Programming characteristics:

1. It's a Read only register.

2. CLR and BUS INIT have no effect.

3. Bit format is shown in Figure 3-1.

3.2.6 Transmit Data Register (TDR)

The TDR consists of two 8-bit bytes. The low byte is the Transmit Buffer (TBUF) and holds the character that is to be transmitted. The high byte is the BREAK register with each line controlled by an individual bit. When a BREAK bit is set, the line associated with that bit starts sending zeroes immediately and continuously. The TDR register is the Write only portion of DR6 and has the following Programming characteristics:

1. A Write only register.

2. BIS or BIC instructions cannot be used.

3. For character lengths less than 8-bits, the character loaded into the TBUF must be right justified because the hardware forces the most significant bits to zero.

4. The BREAK register has no effect when running in the Maintenance mode (i.e. CRS bit 3 = 1).

5. Cleared by CLR and BUS INIT.

6. Bit format is shown in Figure 3-1.

3.3 PROGRAMMING FEATURES

The DZ11 has several programming features that allow control of baud rate, character length, stop bits, parity, and interrupts. This section discusses the application of these controls to achieve the desired operating parameters.

3.3.1 Baud Rate

The selection of the desired transmission and reception speed is controlled by the conditions of bits 08 through 11 of the LPR. Table 3-4 depicts the required bit configuration for each operating speed. Also, the baud rate for each line is the same for both the transmitter and receiver. Furthermore, the receiver clock is turned on and off by setting and clearing bit 12 in the LPR for the selected line.

Table 3-4 Baud Rate Selection Chart

Bits				
11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not Used

3.3.2 Character Length

The selection of one of the four available character lengths is controlled by bits 03 and 04 of the LPR. The bit conditions for bits 04 and 03, respectively, are as follows: 00 (5 level), 01 (6 level), 10 (7 level), and 11 (8 level). For character

lengths of 5, 6, and 7, the high order bits are forced to zero.

3.3.3 Stop Bits

The length of the stop bits in a serial character string is determined by bit 05 of the LPR. If bit 05 is a zero, the stop length is one unit; bit 05 set to a one selects a two-unit stop, unless the 5-level character length (bits 03 and 04 at zero) is selected, then the stop bit length is 1.5 units.

3.3.4 Parity

The parity option is selected by bit 06 of the LPR. Parity is enabled on transmission and reception by setting bit 06 to a one. Bit 07 of the LPR allows selection of even or odd parity, and bit 06 must be set for bit 07 to be significant. The parity bit is generated and checked by hardware, and does not appear in the RBUF or TBUF. The parity error (bit 12, RBUF) flag is set when the received character had a parity error.

3.3.5 Interrupts

The Receiver Interrupt Enable (RIE) and Silo Alarm Enable (SAE) bits in the CSR control the circumstances upon which the DZ11 receiver interrupts the PDP-11 processor.

If RIE and SAE are both clear, the DZ11 never interrupts the PDP-11 processor. In this case, the program must periodically check for the availability of data in the SILO and empty the SILO

when data is present. If the program operates off a clock it should check for characters in the SILO at least as often as the time it takes for the SILO to fill, allowing a safety factor to cover processor response delays and time to empty the silo. The RDONE bit in the CSR will set when a character is available in the SILO. The program can periodically check this bit with a TSTB or BIT instruction. When RDONE is set the program should empty the SILO.

If RIE is set and SAE is clear, the DZ11 will interrupt the PDP-1 processor to the DZ11 receiver vector address when RDONE is set, indicating the presence of a character at the bottom of the SILO. The interrupt service routine can obtain the character by performing a MOV instruction from the RBUF. If the program then dismisses the interrupt, the DZ11 will interrupt when another character is available (which may be immediately if additional characters were placed in the SILO while the interrupt was being serviced). Alternately, the interrupt service routine may respond to the interrupt by emptying the SILO before dismissing the interrupt.

If RIE and SAE are both set, the DZ11 will interrupt the PDP-11 processor to the DZ11 receiver vector when the SILO ALARM (SA) bit in the CSR is set. The SA bit will be set when sixteen characters have been placed in the silo since the last time the program has accessed the RBUF. Accessing the RBUF will clear the SA bit and the associated counter. The program should follow the

procedure described in Paragraph 3.3.6 to empty the silo completely in response to a silo alarm interrupt. This will ensure that any characters placed in the silo while it is being emptied are processed by the program.

NOTE

If the program processes only 16 entries in response to each silo alarm interrupt, characters coming in while interrupts are being processed will build up without being counted by the silo alarm circuit and the silo may eventually overflow without the alarm being issued.

If the silo alarm interrupt is used, the program will not be interrupted if fewer than 16 characters are received. In order to respond to short messages during periods of moderate activity the PDP-11 program should periodically empty the silo. The scanning period will depend on the required responsiveness to received characters. While the program is emptying the silo it should ensure that DZ11 receiver interrupts are inhibited. This should be done by raising the PDP-11 processor priority. The silo alarm interrupt feature can significantly reduce the PDP-11 processor overhead required by the DZ11 receiver by eliminating the need to enter and exit an interrupt service routine each time a character is received.

The transmitter interrupt enable bit (TIE) controls transmitter interrupts to the PDP-11 processor. If enabled, the DZ11 will interrupt the PDP-11 processor to the DZ11 transmitter interrupt vector when the Transmitter Ready (TRDY) bit in the CSR is set, indicating that the DZ11 is ready to accept a character to be transmitted.

3.3.6 Emptying the Silo

The program can empty the SILO by repeatedly performing MOV instructions from the RBUF to temporary storage. Each MOV instruction will copy the bottom character in the SILO so it won't be lost and will clear out the bottom of the SILO, allowing the next character to move down for access by a subsequent MOV instruction. The program can determine when it has emptied the SILO by testing the DATA VALID bit in each word moved out of the RBUF. A zero value indicates that the SILO has been emptied. The test can be performed conveniently by branching on the condition code following each MOV instruction. A TST or BIT instruction must not access the RBUF because these instructions will cause the next entry in the SILO to move down without saving the current bottom character. Furthermore, following a MOV from the RBUF, the next character in the silo will not be available for at least 1 microsecond. Therefore, on fast CPU's, the program must use sufficient instructions or NOPs to ensure that successive MOVs from the RBUF are separated by a minimum of 1 microsecond. This will prevent a false indication of an empty silo.

3.3.7 Transmitting a Character

The program controls the DZ11 transmitter through five registers on the Unibus: the Control and Status Register (CSR), the Line Parameter Register (LPR), the Line Enable Register, the Transmitter Buffer (TBUF) and the Break Register (BRK).

Following DZ11 initialization, the program must use the LPR register to specify the speed and character format for each line to be used and must set the Master Scan Enable (MSE) bit in the CSR.

The program should set the Transmitter Interrupt Enable (TIE) bit in the CSR if it wants the DZ11 transmitter to operate on a program interrupt basis.

The Line Enable Register is used to enable and disable transmission on each line. One bit in this eight bit register is associated with each line. The program can set and clear bits by using MOV, MOVB, BIS, BISB, BIC and BICB instructions. (If word instructions are used, the Line Enable Register and the DTR registers on M7819 modules are simultaneously accessed.)

The DZ11 transmitter is controlled by a scanner which is constantly looking for an enabled line (Line Enable bit set) which has an empty UART transmitter buffer. When the scanner finds such a line it loads the number of the line into the 3-bit Transmit Line Number (TLINE) field of the CSR and sets the TRDY bit, interrupting the PDP-11 processor if the TIE bit is set. The program can clear the TRDY bit by moving a character for the indicated line into the TBUF or by clearing the Line Enable bit.

Clearing the TRDY bit frees the scanner to resume its search for lines needing service.

To initiate transmission on an idle line, the program should set the TCR bit for that line and wait for the scanner to request service on the line, as indicated by the scanner loading the number of the line into TLINE and setting TRDY. The program should then load the character to be transmitted into the TBUF by using a MOVB instruction. If interrupts are to be used, a convenient way of starting up a line is to set the TCR bit in the main program and let the normal transmitter interrupt routine load the character into the TBUF.

NOTE

The scanner may find a different line needing service before it finds the line being started up. This will occur if other lines request service before the scanner can find the line being started. The program must always check the TLINE field of the CSR when responding to TRDY to ensure it loads characters for the correct line. Assuming the program services lines as requested by the scanner, the scanner will eventually find the line being started. If several lines require

NOTE (Cont)

service, the scanner will request service in priority order as determined by line number. Line 7 has the highest priority and line 0 the lowest.

To continue transmission on a line, the program should load the next character to be transmitted into the TBUF each time the scanner requests service for the line as indicated by TLINE and TRDY.

To terminate transmission on a line, the program loads the last character normally and waits for the scanner to request an additional character for the line. The program clears the Line Enable bit at this time instead of loading the TBUF.

The normal rest condition of the Transmitted Data lead for any line is the 1 state. The Break Register (BRK) is used to apply a continuous zero signal to the line. One bit in this eight bit register is associated with each line. The line will remain in this condition so long as the bit remains set. The program should use a MOVB instruction to access the BRK register. If the program continues to load characters for a line after setting the break bit, transmitter operation will appear normal to the program despite the fact that no characters can be transmitted while the line is in the continuous zero sending state. The program may

use this facility for sending precisely timed zero signals by setting the break bit and using Transmit Ready interrupts as a timer.

It should be remembered that each line in the DZ11 is double buffered. The program must not set the BRK bit too soon or the two data characters preceding the break may not be transmitted. The program must also ensure that the line returns to the 1 state at the end of the zero sending period before transmitting any additional data characters. The following procedure will accomplish this. When the scanner requests service the first time after the program has loaded the last data character, the program should load an all-zero character. When the scanner requests service the second time, the program should set the BRK bit for the line. At the end of the zero sending period the program should load an all-zero character to be transmitted. When the scanner requests service indicating this character has begun transmission the program should clear the BRK bit and load the next data character.

3.3.8 Data Set Control

DZ11 models with EIA interfaces include data set control as a standard feature. The program may sense the state of the Carrier and Ring Indicator signals from each data set and may control the state of the Data Terminal Ready signal to each data set. The program uses three 8-bit registers to access the DZ11 data set control logic. One bit in each register is associated with

each of the 8 lines. There are no hardware interlocks between the data set control logic and the receiver and transmitter logic. Any required coordination should be done under program control.

The Data Terminal Ready (DTR) register is a read/write register. Setting or clearing a bit in this register will turn the appropriate Data Terminal Ready signal on or off. The program may access this register with word or byte instructions. (If word instructions are used the SCR and Line Enable registers will be simultaneously accessed.) The DTR register is cleared by the INIT signal on the Unibus but is not cleared if the program clears the DZ11 by setting the CLR bit of the CSR.

The Carrier Register (CAR) and Ring Register (RING) are read-only registers. The program can determine the current state of the carrier signal for a line by examining the appropriate bit of the CAR register. It can determine the current state of the ring signal by examining the appropriate bit of the RING register. The program can examine these registers separately by using MOVB or BITB instructions or can examine them as a single 16 bit register by using MOV or BIT instructions. The DZ11 data set control logic does not interrupt the PDP-11 processor when a carrier or ring signal changes state. The program should periodically sample these registers to determine the current status. Sampling at a high rate is not necessary.

3.4 PROGRAMMING EXAMPLES

The following five examples are sample programs for the DZ11 option. These examples are presented only to indicate how the DZ11 can be used.

Example 1 - Initializing the DZ11

The DZ11 is initialized by: a power-up sequence, a reset instruction, or a device clear instruction.

Device Clearing the DZ11

```
001000      012737      START:   MOV #20, DZCSR   ;Set bit 4 in the
001002      000020                                ;DZ11 control and
001004      160100                                ;status register.
001006      032737      1$:      BIT #20, DZCSR   ;Test bit 4.
001010      000020
001012      160100
001014      001374               BNE 1$           ;If bit 4 is still
                                                  ;set, the branch
                                                  ;condition is true
                                                  ;and the device clear
                                                  ;function is still in
                                                  ;progress.
001016      000000               HALT             ;The device clear
                                                  ;function is complete
                                                  ;and the DZ11 has been
                                                  ;cleared.
```

DZCSR = 160100 = control and status register address

Example 2 - Transmit binary count pattern on one line

```
001000    012737    START:    MOV #20, DZCSR    ;Set bit 4 in the DZ11
001002    000020                                ;control and status
                                                ;register.
001004    160100
001006    032737    1$:       BIT #20, DZCSR    ;Test bit 4.
001010    000020
001012    160100
001014    001374              BNE 1$            ;If bit 4 is still set,
                                                ;the branch condition
                                                ;is true and the device
                                                ;clear function is still
                                                ;in progress.
001016    012737              MOV #n, DZLPR     ;Load the parameters
001020    001070                                ;for line 3: 8 bit
001022    160102                                ;character; 2 stop bit;
                                                ;110 baud.
001024    012737              MOV #1, DZTCR     ;Enable line 0
                                                ;transmitter.
001026    000001
001030    160104
001032    012737              MOV #m, DZCSR     ;Set scanner enable bit
001034    000040                                ;5 in the control and
001036    160100                                ;status register.
001040    005000              CLR R0            ;Set binary count
                                                ;pattern to zero.
```

Example 2 (Cont)

```
001042    005737    2$:     TST DZCSR       ;Test the transmitter
001044    160100              ;ready flag (bit 15).
001046    100375            BPL 2$          ;If branch condition
                            ;is false, continue;
                            ;otherwise test again.
001050    110037            MOVB R0, DZTDR  ;Load character to be
001052    160106            ;transmitted.
001054    105200            INCB R0         ;Increment binary count.
001056    100371            BPL 2$          ;If branch condition is
                            ;false, the binary count
                            ;pattern is complete.
001060    000000            HALT
```

R0 = Register 0 = Binary Count Pattern

DZCSR = DZ11 Control and Status Register Address = 160100

DZLPR = DZ11 Line Parameter Register Address = 160102

DZTCR = DZ11 Transmit Control Register Address = 160104

DZTDR = DZ11 Transmit Data Register Address = 160106

Example 3 - Transmit a binary count in Maintenance Loopback mode, with the receiver "On" in the interrupt mode. Output received data to console.

```
001200    005000            CLR R0          ;Set binary count
                            ;to zero.
001202    012701            MOV #1400, R1   ;Set R1 to first
001204    001400            ;address of data
                            ;buffer.
```

Example 3 (Cont)

```
001206    012706          MOV #SP, R6       ;Initialize stack
001210    001100                            ;pointer.
001212    012737          MOV #INT, RVEC    ;Set DZ11 vector
001214    001304                            ;address to start of
001216    000300                            ;receiver interrupt
                                            ;routine.
001220    005037          CLR (RVEC+2)      ;Set up processor
001222    000302                            ;status word for DZ11
                                            ;receiver interrupt.
001224    012737          MOV #20, DZCSR    ;Set bit 4 in the
001226    000020                            ;DZ11 control and
                                            ;status register.
001230    160100
001232    032737    1$:   BIT #20 DZCSR     ;Test bit 4.
001234    000020
001236    160100
001240    001374          BNE 1$            ;if bit 4 is still
                                            ;set, the branch
                                            ;condition is true
                                            ;and the device clear
                                            ;function is still in
                                            ;progress.
001242    012737          MOV #PAR, DZLPR   ;Load the parameters
001244    011070                            ;for line 0: 8 bit
001246    160102                            ;character; 2 stop bits;
```

Example 3 (Cont)

```
                                                ;110 baud; no
                                                ;parity; receiver on.
001250      012737          MOV #1, DZTCR       ;Enable line 0
                                                ;transmitter.
001252      000001
001254      160104
001256      012737          MOV #150, DZCSR     ;Turn scanner on,
001260      000150
001262      160000                              ;enable receiver
                                                ;interrupts, and loop
                                                ;lines back on themselves
001264      005737    2$:   TST DZCSR           ;Test the transmitter
001266      160100                              ;ready flag.
001270      100375          BPI 2$              ;If branch condition is
                                                ;false, continue
                                                ;otherwise test again.
001272      110037          MOVB R0, DZTBUF     ;Load character to be
001274      160106                              ;transmitted.
001276      105200          INCB R0             ;Increment binary count.
001300      001371          BNE 2$              ;If branch condition is
                                                ;false, the binary count
                                                ;pattern is complete.
001302      000777          BR.                 ;Wait for last character
                                                ;transmitted to be
                                                ;received.
```

Receiver Interrupt Service Routine

```
001304    013711          MOV DZRBUF, (R1) ;Store received
001306    160102                           ;character in memory
                                           ;table.
001310    022721          CMP #100377,     ;Check for last
001312    100377          (R1)+            ;character.
001314    001401          BEQ .+2          ;Branch condition is
                                           ;true when last
                                           ;transmitted character
                                           ;is received.
001316    000002          RTI              ;Exit routine.
001320    012701          MOV #1400, R1    ;Initialize pointer
001322    001400                           ;to start of received
                                           ;data buffer in memory.
001324    105737    3$:   TSTB TPS         ;Test to see if console
001326    177564                           ;is ready.
001330    100375          BPL 3$           ;Wait, and test again.
                                           ;If condition is met,
001332    111137          MOVB (R1), TPB   ;transfer character
001334    177566                           ;to console.
001336    022721          CMP #100377,     ;Check for last
001340    100377          (R1)+            ;character.
001342    001370          BNE 3$           ;Not finished if
                                           ;condition is true.
001344    000000          HALT             ;finished.
```

RVEC = DZ11 Receiver Interrupt Vector Address

DZCSR = DZ11 Control and Status Word Address

DZLPR = DZ11 Line Parameter Register (Write Only) Address

DZTCR = DZ11 Transmit Control Register Address

DZTBUF = DZ11 Transmit Buffer Address

DZRBUF = DZ11 Receiver Buffer Address (Read Only Register)

TPS = Teletype Punch Status Register Address

TPB = Teletype Punch Data Register Address

Example 4 - Transmit and receive in Maintenance mode on a single line. The Switch register bits SWR00-SWR07 holds the desired data pattern (character).

```
001000    012737    START:    MOV #LINE, DZTCR ;Select the line for
001002    000002                               ;transmitting on.
                                               ;Choose one of eight.
001004    160104                               ;Line #1 selected.
001006    012737              MOV #PAR, DZLPR  ;Select desired line
001010    017471                               ;parameters for
                                               ;transmitting line
001012    160102                               ;and turn on receiver
                                               ;for that line.
                                               ;8 level code, 2 stop
                                               ;bits, and no parity
                                               ;selected.
```

Example 4 (Cont)

```
                                                    ;19.2K baud selected
                                                    ;Note: 19.2K baud is
                                                    ;not used by the
                                                    ;customer but can be
                                                    ;used for diagnostic
                                                    ;purposes to speed up
                                                    ;the transmit-receive
                                                    ;loop to make it easier
                                                    ;to scope.
001014    012737              MOV #N, DZCSR         ;Start scanner and set
001016    000050                                    ;maintenance bit 3.
001020    160100
001022    005737    Test 1:   TST DZCSR             ;Test for bit 15
001024    160100                                    ;(transmitter ready).
001026    100375              BPL Test 2            ;If the branch condition
                                                    ;is false, the transmitter
                                                    ;is ready; if true, go
                                                    ;back and test again.
001030    113737              MOVB SWR,             ;Load the transmit
001032    177570              DZTBUFF               ;character from the
001034    160106                                    ;Switch register.
001036    000240              NOP                   ;No operation. This
                                                    ;location can be changed
                                                    ;to a branch instruction
                                                    ;if only test 1 is
```

Example 4 (Cont)

```
                                                    ;desired (replace 000240
                                                    ;with 000771).
001040      012701              MOV #DEL, R1        ;Delay equals a
            177670                                  ;constant that will
                                                    ;allow enough time for
                                                    ;the receiver done
                                                    ;flag to set before
                                                    ;recycling the test.
                                                    ;The value will change
                                                    ;with baud rate and
                                                    ;processor. The
                                                    ;constant given is
                                                    ;good for 19.2K baud
                                                    ;on a PDP-11/05.
001044      105737      Test 2: TSTB DZCSR          ;Test bit 2 - receiver
001044      160100                                  ;done flag.
001046      100402              BMI 1$              ;When the branch
                                                    ;condition is true,
                                                    ;the receiver done
                                                    ;flag is set.
001050      005201              INC R1              ;Increment delay.
001052      001373              BNE TEST 2          ;If the branch
                                                    ;condition is true, the
                                                    ;delay is not finished.
001054      013700      1$:     MOV DZRBUF, R0      ;Read the DZ11
```

Example 4 (Cont)

```
001056    160102                        ;receiver buffer to
                                        ;register 0.
001060    000760        BR TEST 1       ;Loop back and
                                        ;test again.
```

Example 5 - Transmit and receive on a single line using silo alarm in Maintenance mode.

```
001200    012706        MOV #1100, R6   ;Initialize stack
001202    001100                        ;pointer.
001204    012737        MOV #3$, TVEC   ;Initialize transmitter
001206    001274                        ;vector address.
001210    000304
001212    005037        CLR TVEC+2      ;Initialize transmitter
001214    000306                        ;vector processor status
                                        ;word.
001216    012700        MOV #DBUF, R0   ;Set first address of
001220    001304                        ;input data table
                                        ;into R0.
001222    012737        MOV #1, DZTCR   ;Enable line 0
                                        ;transmitter.
001224    000001
001226    160104
001230    012737        MOV #17470,     ;Set up line parameters
001232    017470        DZLPR           ;and turn on the receiver
001234    160102                        ;clock for line 0.
```

Example 5 (Cont)

```
001236    012737          MOV #50C50,     ;Enable transmitter
001240    050C50          DZCSR           ;interrupt and silo
001242    160100                          ;alarm. Turn on
                                          ;scanner and Maintenance
                                          ;mode.
001244    032737    1$:   BIT #200C0,     ;Test for silo alarm.
001246    020000
                          DZCSR
001250    160100
001252    001774          BEQ 1$          ;Loop until silo alarm
                                          ;flag sets.
001254    013720    2$:   MOV DZRBUF,     ;Read DZ11 silo
001256    160102          (R0)+           ;receiver buffer output.
001260    000240          NOP             ;Delay to allow next
001262    000240          NOP             ;word in silo to filter
                                          ;down to the silo
                                          ;output.
001264    100773          BMI 2$          ;Data valid set says
                                          ;that word is good,
                                          ;go back for more.
001266    012700          MOV #DBUF, R0   ;Silo has been emptied.
001270    001304                          ;Reinitialize data
                                          ;table address pointer.
001272    000764          BR 1$           ;Do it again.
```

Transmitter Interrupt Service Routine

```
001274      112737    3$          MOVB DAT, DZTBUF ;Transmit
001276      000252                                 ;character 252
001300      160106
001302      000002                 RTI
```

Data Table

```
1304                  100252                     ;Word #1
1306                  100252                        .
    .                    .                          .
                         .                          .
    .                    .                          .
    .                    .                          .
    .                    .                          .
    .                    .                          .
1340                  100252                     ;Word #16
1342                  000252                     ;Data valid not set
                                                 ;character is invalid
```

NOTE: It is possible to get more than 16 words because they are being put into the silo simultaneously with the reading of the silo.

Example 6 - Echo test on a single line. (Transmit received data)

```
001000      012737    START:    MOV #PAR, DZLPR  ;Load line parameters
                                                 ;for line being used.
001002      011073                               ;Line #3, 8 bit
001004      160102                               ;character, 2 stop
```

Example 6 (Cont)

```
                                                ;bits, no parity,
                                                ;110 baud, and receiver
                                                ;clock on.
001006    012737          MOV #LINE, DZTCR      ;Turn line #3
001010    000010                                ;transmitter on.
001012    160104
001014    012737          MOV #n, DZCSR         ;turn scanner on
001016    000040                                ;(set CSR-5)
001020    160100
001022    105737    1$:   TSTB DZCSR            ;test (bit 7) for
001024    160100                                ;RDONE
001026    100375          BPL 1$                ;If bit 7 is not set
                                                ;go back and test again.
001030    005737    2$:   TST DZCSR             ;Test (bit 15) for
001032    160160                                ;TRDY
001034    100375          BPL 2$                ;If bit 15 is not set
                                                ;go back and test again.
001036    013700          MOV RBUF, R0          ;Read Received Data
001040    160102                                ;word into R0
001042    110037          MOVB R0, DZTDR        ;load character
001044    160106                                ;into DZ11 TBUF
                                                ;Register for
                                                ;transmitting.
001046    000765          BR 1$                 ;repeat.
```

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