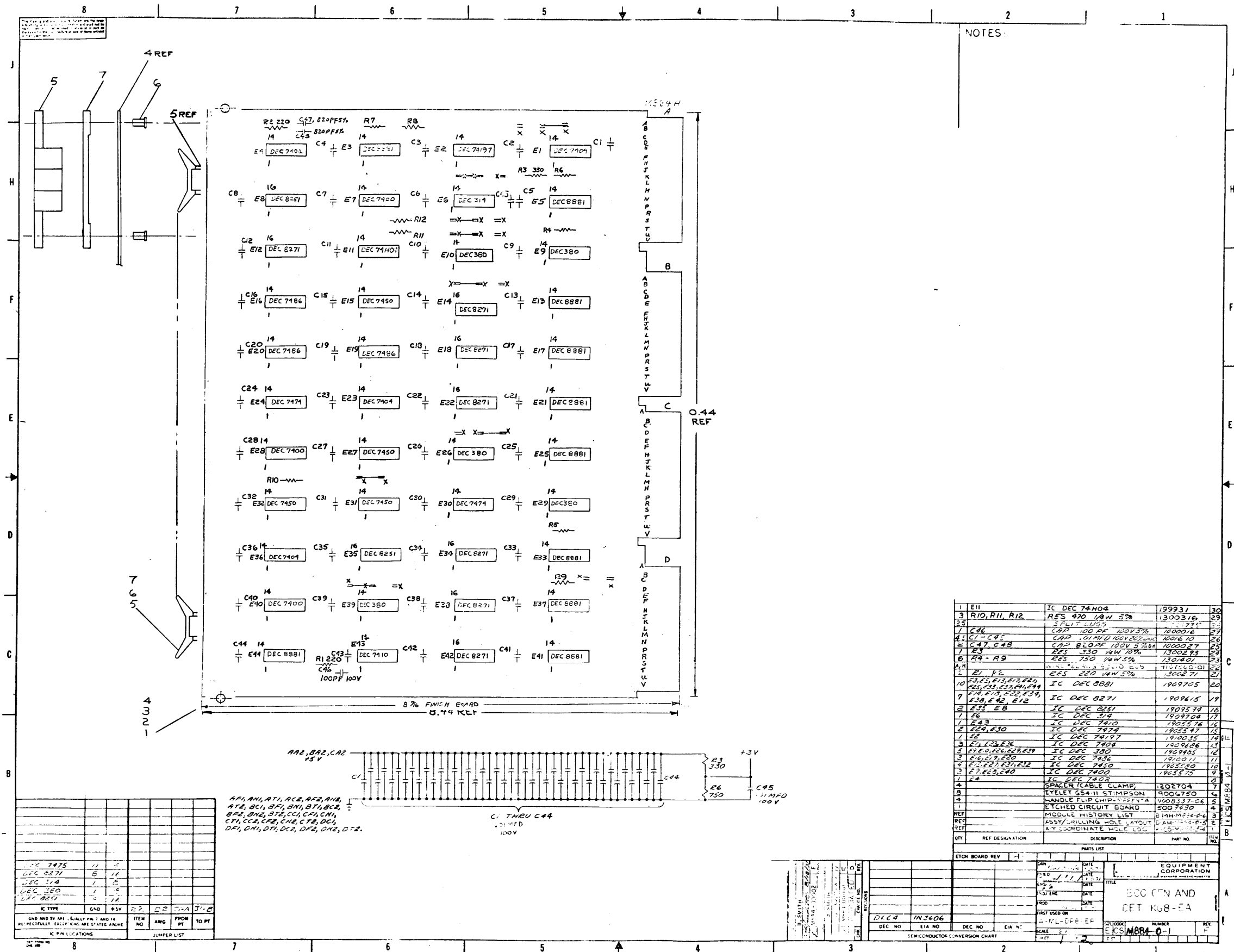
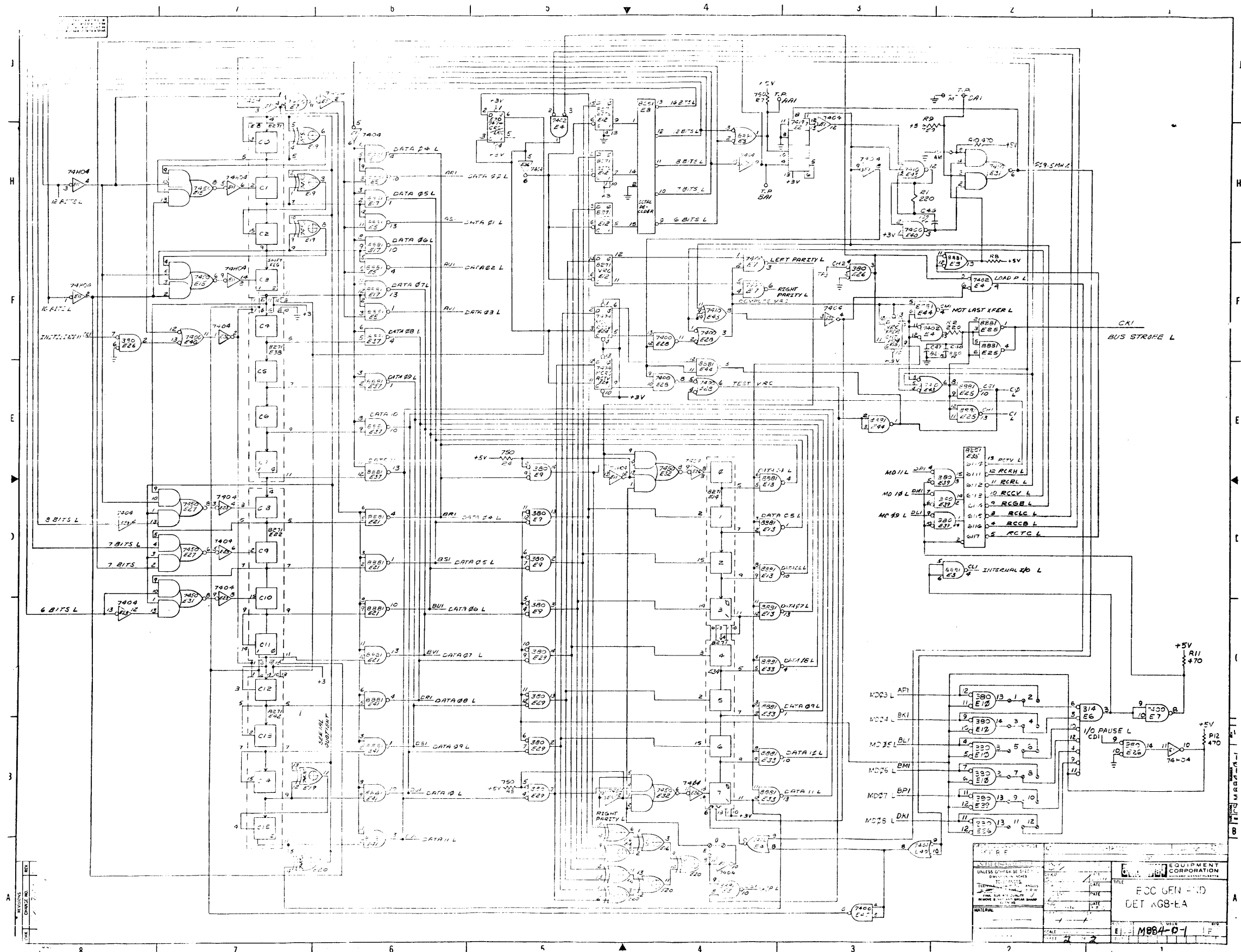


KG8-E
generator/detector
engineering drawings





EQUIPMENT CORPORATION	
ECC GEN AND DET AG8-EA	
M084-0-1	
DATE: 10/1/64	
BY: [Signature]	
CHECKED: [Signature]	
APPROVED: [Signature]	
SCALE: 1/2"	
SHEET: 1 OF 1	

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DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION				DATE 7/1/71		
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		KG8E-00002	B.SMITH	7-72		7/1/72
Formerly DP8-EP Redundancy Check.						
ENG	APPD	SIZE	CODE	NUMBER	REV	
Robert Smith		A	SP	KG8-EA-1	A	

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION			
0.0 Overall Description			
The KG8-EA Block Check Character Generation and Detection Option provides error detection capabilities for data communications applications. This option performs directly with the PDP8/E bi-directional data bus, coupled with input/output instruction. Thus, it can perform, non-currently, with a number of Communication devices. Additionally, the KG8-EA adds an exclusive "OR" Instruction to the PDP8/E repertoire.			
1.0 General Specification			
1.1 Definition of Basic System			
The Block Check Character Generation and Detection Option provides three types of error detection facilities: Vertical Redundancy Check (VRC), Longitudinal Redundancy Check (LRC) and Cyclic Redundancy Check (CRC). Refer to appendix for detailed definition and example of VRC, LRC and CRC. The System Block Diagrams (Fig. 1) shows the error detection capabilities simplified. The basic parts are: The cyclic 16-bit shift register for LRC and CRC, the Shift/Hold Register, the VRC logic, and the control. <u>Cyclic Shift Register</u>: accumulates the Block, check character (BCC) for LRC and CRC. The contents of the cyclic shift register is available to the program for testing and/or transferring to some data communications facilities. <u>Shift/Hold Register</u>: Provides a) shift register for a serial data transfer to the cyclic shift register, b) hold or latch register for generation of Vertical Redundancy. <u>VRC Logic</u>: Generates or tests character parity. <u>Control</u>: Provides a) buffering to (from) the PDP8/E OMNIBUS, b) device selection c) function selection and d) timing.			
1.2 Option: Either ODD parity or EVEN parity (VRC) can be jumper selected.			
		SIZE	CODE
		A	SP
		NUMBER	REV
		KG8-EA-1	A

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION			
1.3 Mechanical Packaging: The Redundancy logic is contained in one 8½ inch Quad Logic module. Pin assignments conform to the PDP8/E OMNIBUS specifications. 1.4 Environmental Specification: 1.4.1 Power Required +5 @ 931 ma (max) +15 @ NONE -15 @ NONE 1.4.2 Temperature Range 0° - 60°C C 95% Humidity (non-condensing) 1.5 Performance Specifications: 1.5.1 Vertical Redundancy Check (VRC): Test or generate odd or even parity for up to eight bit characters. The parity bit is either right justified to AC11 or left justified to AC04. 1.5.2 Longitudinal Redundancy Check (LRC): Computes or compares check sum for 6, 7, 8, 12 and 16 bit characters. Two bytes are required for LRC 12 & 16. 1.5.3 Cyclic Redundancy Check (CRC): IBM compatible for CRC-16 and CRC-12. Constants utilized are $x^{16} + x^{15} + x^2 + 1$ and $x^{12} + x^{11} + x^3 + x^2 + x + 1$ for CRC-16 and CRC-12 respectively. "X" is module two. 1.5.4 Cycle Time: VRC compute 1.5 usec. VRC Test 1.2 usec. CRC/LRC 1.2 usec.			

2.0 Vendor
None3.0 Programming:

3.1 Instructions

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION			
issued with the RCGB instruction if the appropriate control bit is selected. See RCGB and RCLC instructions for details. Additionally, the hardware clears the AC. 6XX1 Read BCC High (RCRH) JAM transfers the Least Significant (LSB) 8 bits of the BCC accumulation to the AC (right justified). This instruction is utilized only for 16-bit check sums. If the characters included in the BCC had their MSB in AC11 then RCRL will deliver the LSB of the BCC in AC04. 6XX2 Read BCC Low (RCRL) JAM transfers the Most Significant (MSB) 8 or 12 bits of the BCC Accumulation to the AC (right justified). If the characters included in the BCC had their MSB in AC11, then RCRH will deliver the MSB of the BCC to AC11. 6XX3 Compute VRC (RCCV) Generates character parity for the contents of AC04 to AC11 (unused bits must be negated). Parity bit can be in position AC04 or AC11 and this function may be issued with the RCGB instruction if the appropriate control bit is selected. See RCGB and RCLC instructions for details. Hardware Procedure: The character in the AC is latched into the KG8-EA, with corrected parity, and via an extended cycle the character is then JAM transferred back to AC04 - AC11. 6XX4 Generate BCC (RCGB) Generates a LRC or CRC Block check character (BCC). The LRC can be generated from 6, 7, 8, 12 and 16 bit characters. Note the LRC 12 is accumulated with two 6-bit bytes and LRC 16 with two 8-bit bytes. The CRC is generated from 6 or 8 bit characters for a 12 and 16 bit BCC, respectively. The Receive and Transmit BCC's are compared by treating the transmitted BCC as data and including it in the Receive accumulation. In doing so, the Receive BCC generator will go to Zero if there were no errors in transmission.			
SIZE	CODE	NUMBER	REV
A	SP	KG8-EA-1	A

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION			
Additionally, the hardware clears the AC if RCCV is not micro programmed with RCGB. Also this instruction provides the functions defined for RCCV and RCTV instructions - if the appropriate control bit is selected. (See RCLC instruction) 6XX5 Load Control (RCLC) "JAM" transfers the contents of the AC to the control register. The control functions are as follows: AC05 One: cyclic redundancy check Zero: Longitudinal redundancy check AC Bit 678: 000: 16 Bit BCC 001: 12 Bit BCC 010: 8 Bit BCC 011: 7 Bit BCC 100: 6 Bit BCC AC09 One: Generated VRC bit → AC11 Zero: Generated VRC bit → AC04 AC10 One: A RCGB instruction also causes an RCCV sequence to occur. The BCC will be generated utilizing the character with corrected parity. AC11 One: A RCGB instruction also causes an RCTV sequence to occur. 6XX6 Clear BCC Accumulation (RCCB) Clears the 16-bit Cyclic Register. This register is also cleared by INITIALIZE. 6XX7 Maintenance Clock RCTC When the "M" jumper is installed this instruction causes one clock pulse for BCC computation. 4.0 Interface Specification The interface conforms to the PDP8/E OMNIBUS specifications. 5.0 Test Procedures The diagnostic program for the KG8-EA is MAINDEC-8E-D8CA. Refer to the document for operating instructions.			
SIZE A	CODE SP	NUMBER KG8-EA-1	REV A

ENGINEERING SPECIFICATION		CONTINUATION SHEET															
TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION																	
APPENDIX																	
A. <u>Vertical Redundancy</u> is parity on a character basis, where one bit of each character is reserved as the parity bit. The parity bit forces the character to have either an even or odd number of ONE's. This option will generate *EVEN/ODD parity. However, odd or even parity may be checked. B. <u>Longitudinal Redundancy</u> is a checksum accumulation over a Block of Characters and is more reliable than VRC in detecting errors. A common configuration utilizes LRC and VRC to increase the probability of detecting multiple errors. The LRC accumulation is an exclusive "OR" of all characters in a message, by column (Figure A1).																	
<table><tr><td></td><td>Column</td></tr><tr><td></td><td>P 7 6 5 4 3 2 1</td></tr><tr><td>Character 1</td><td>0 1 1 1 1 0 0 1</td></tr><tr><td>Character 2</td><td>1 0 0 1 1 0 0 0</td></tr><tr><td>Character 3</td><td>0 0 0 0 0 1 1 1</td></tr><tr><td>Character 4</td><td>1 1 1 1 0 0 0 0</td></tr><tr><td>LRC Check Sum</td><td>0 0 0 1 0 1 1 0</td></tr></table>					Column		P 7 6 5 4 3 2 1	Character 1	0 1 1 1 1 0 0 1	Character 2	1 0 0 1 1 0 0 0	Character 3	0 0 0 0 0 1 1 1	Character 4	1 1 1 1 0 0 0 0	LRC Check Sum	0 0 0 1 0 1 1 0
	Column																
	P 7 6 5 4 3 2 1																
Character 1	0 1 1 1 1 0 0 1																
Character 2	1 0 0 1 1 0 0 0																
Character 3	0 0 0 0 0 1 1 1																
Character 4	1 1 1 1 0 0 0 0																
LRC Check Sum	0 0 0 1 0 1 1 0																
FIGURE A1																	
The hardware implementation is cyclic. Figure A2 illustrates the hardware configuration for an eight bit code whereas the polynomial is $(X^8 + 1)$.																	
Figure A2																	
Both the Transmitting and Receiving Stations are expected to compute the check sum. At the end of each message block, the transmitting stations sends its check sum. The receiving station than compares the check sums--if equal--the message is assumed to be without error. *For EVEN parity: Install jumper "E"; remove jumper "O". For ODD parity: Install jumper "O"; remove jumper "E".																	
SIZE A	CODE SP	NUMBER KG8-EA-1	REV A														

ENGINEERING SPECIFICATION

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CONTINUATION SHEET

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

C. Cyclic Redundancy (CRC) as implemented in this option is IBM compatible for CRC-12 and CRC-16.

The CRC Check sum is a division using the numeric binary value of a message as the dividend which is divided by a constant. The division is performed serially with the quotient discarded. When the process is completed, the remainder becomes the check sum.

Both the Transmitting and Receiving Stations are expected to compute the check sum. At the end of each message block, the transmitting stations sends its check sum. The receiving station then compares the check sums--if equal--the message is assumed to be without error.

The probability of error detection is somewhat increased when CRC and VRC are combined.

C.1 CRC-12

When operating with six bits per character, the BCC accumulation is 12 bits and utilizes the generator polynomial $x^{12} + x^{11} + x^3 + x^2 + x + 1$. This polynomial has the prime factors $(X + 1)$ and $(x^{11} + x^2 + 1)$, and provides error detection of butst up to 12 bits in lenth. Additionally, 99.955% of error burst greater than 12 bits will be detected.

Figure A3 illustrates the operation of the cyclic generators for CRC-12 block check. NOTE: the crosses are exclusive OR's and the squares are stages of the shift register.

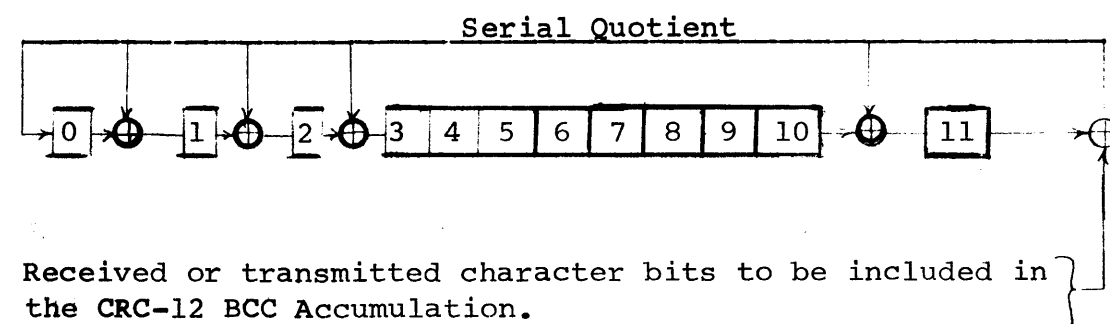


Figure A3

SIZE A	CODE SP	NUMBER KG8-EA-1	REV A
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0101101

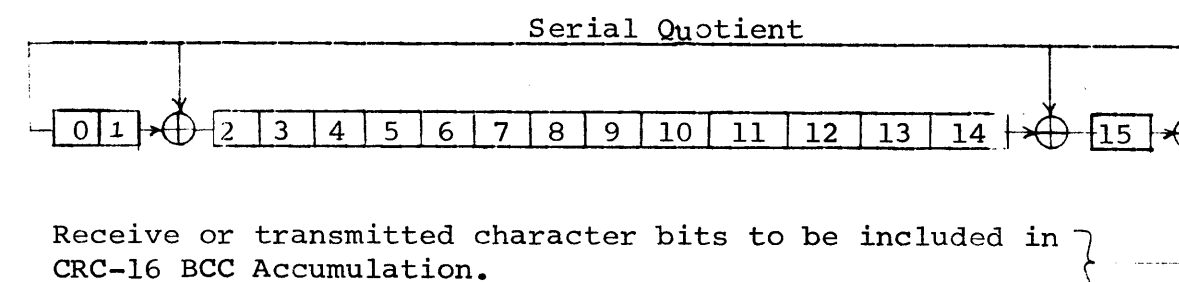
CONTINUATION SHEET

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

C.2 CRC-16

When operating with 8 bits per character, the BCC accumulation is 16 bits and utilizes the generator polynomial $x^{16} + x^{15} + x^2 + 1$. This polynomial has the prime factors $(X + 1)$ and $(x^{15} + x + 1)$ and provides error detection of burst up to 16 bits in length. Additionally, 99.9997% of error burst greater than 16 bits will be detected.

Figure A4 illustrates the operation of the cyclic generator for CRC-16 block check. NOTE: the crosses are exclusive OR's and the squares are stages of the shift register.



Receive or transmitted character bits to be included in }
CRC-16 BCC Accumulation.

Figure A4

C.3 CRC-16 example

The data used to accumulate a CRC-16 BCC is the ACSII coded letters A, B, C with odd character parity.

The transmit sequence is illustrated in Figure A5. Illustrated is the step-by-step shift pattern of the cyclic generator as the data is serially applied to the input.

Line 1: the first row of numbers, lines, and asterisks is symbolic of the hardware configuration for CRC-16. The asterisks represent exclusive OR operations and the lines represent the feedback path (quotient) and direction. Note that the encoded data is shifted from left to right.

Line 2: is the initial conditons, an all Zero register.

Line 3: a ONE is presented to the input line, from data for transmit, and is exclusive OR'ed with a ZERO from bit 15. The resultant on the serial quotient line is a ONE. Further, the serial quotient is presented to: a) bit 0 b) the exclusive OR between bits 1 and 2, c) the exclusive OR between bits 14 and 15. When the feed back settles down

SIZE A	CODE SP	NUMBER KG8-EA-1	REV A
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TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

Figure A5 Transmit CRC 16

* Indicates an exclusive OR function.

Line #	SERIAL QUOTIENT															SERIAL QUOTIENT	DATA FOR TRANSMIT
1	0	1	*	2	3	4	5	6	7	8	9	10	11	12	13	14	* 15 *
2	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	Input_ -- Initial_
3	1	0		1	0	0	0	0	0	0	0	0	0	0	0	1	1
4	1	1		1	1	0	0	0	0	0	0	0	0	0	0	1	0
5	1	1		0	1	1	0	0	0	0	0	0	0	0	0	1	0 A
6	1	1		0	0	1	1	0	0	0	0	0	0	0	0	1	0
7	1	1		0	0	0	1	1	0	0	0	0	0	0	0	1	0
8	1	1		0	0	0	0	1	1	0	0	0	0	0	0	1	0
	0	1		1	0	0	0	0	1	1	0	0	0	0	0	0	1
	1	0		0	1	0	0	0	0	1	1	0	0	0	0	1	1
	1	1		1	0	1	0	0	0	0	1	1	0	0	0	1	0
	0	1		1	1	0	1	0	0	0	0	1	1	0	0	0	1
	0	0		1	1	1	0	1	0	0	0	0	1	1	0	0	0
	0	0		0	1	1	1	0	1	0	0	0	0	1	1	0	0
	0	0		0	0	1	1	1	0	1	0	0	0	0	1	1	0
	0	0		0	0	0	1	1	1	0	1	0	0	0	0	1	1
	0	0		0	0	0	0	1	1	1	0	1	0	0	0	0	0
	1	0		1	0	0	0	0	0	1	1	1	0	1	0	0	1
	0	1		0	1	0	0	0	0	0	1	1	1	0	1	0	0
	0	0		1	0	1	0	0	0	0	0	1	1	1	0	1	0
	0	0		0	1	0	1	0	0	0	0	0	1	1	1	0	1
	1	0		1	0	1	0	1	0	0	0	0	0	1	1	1	0
	1	1		1	1	0	1	0	1	0	0	0	0	0	1	1	0
	1	1		0	1	1	0	1	0	1	0	0	0	0	0	1	0
	0	1		1	0	1	1	0	1	0	1	0	0	0	0	1	0
	0	1		1	0	1	1	0	1	0	1	0	0	0	0	1	0

BCC

TRANSMIT BIT PATTERN (LEFT TO RIGHT)

10000011 01000011 110000010 1000001010110110

 a b c BCC

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

the first shift takes place netting line 3.

This shift also presents a new bit, for encoding, at the input line causing another serial quotient.

The next shift leads to line 4 etc., etc. This is continued until all data bits have been processed. The BCC is the contents of the shift register after the last shift.

The BCC is expected to be transmitted most significant bit first (ie. bit 15).

See the bottom of figure A5 for the transmit bit pattern.

The receive step-by-step sequence is illustrated in figure A6 and is identical in procedure used for the transmit sequence. Additionally, the Receive shift register operates (encodes) on the transmitted BCC. This last step is really a comparison of the Transmitted BCC to the Receive BCC and MUST result in an all ZERO receive shift register.

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CONTINUATION SHEET

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

Figure A6 Receive CRC 16

*Indicates an exclusive OR function

SERIAL QUOTIENT																	SERIAL QUOTIENT	RECEIVED DATA		
0	1	*	2	3	4	5	6	7	8	9	10	11	12	13	14	*	15	*	← INPUT	INITIAL
0	0		0	0	0	0	0	0	0	0	0	0	0	0	0		0			
1	0		1	0	0	0	0	0	0	0	0	0	0	0	0		1		1	1
1	1		1	1	0	0	0	0	0	0	0	0	0	0	0		1		1	0
1	1		0	1	1	0	0	0	0	0	0	0	0	0	0		1		1	0 A
1.	1	.																		0
.		.																		
.		.																		
.		.																		
.		.																		
.		.																		
1	1		1	1	0	1	0	1	0	0	0	0	0	1	1	1			1	0 C
1	1		0	1	1	0	1	0	1	0	0	0	0	0	1	0			1	1
0	1		1	0	1	1	0	1	0	1	0	0	0	0	0	1			0	0
0	0		1	1	0	1	1	0	1	0	1	0	0	0	0	0			0	1
0	0		0	1	1	0	1	1	0	1	0	1	0	0	0	0			0	0 B
0	0		0	0	1	1	0	1	1	0	1	0	1	0	0	0			0	0 C
0	0		0	0	0	1	1	0	1	1	0	1	0	1	0	0			0	0 C
0	0		0	0	0	0	1	1	0	1	1	0	1	0	1	0			0	0
0	0		0	0	0	0	0	1	1	0	1	1	0	1	0	1			0	0
0	0		0	0	0	0	0	0	1	1	0	1	1	0	1	0			0	1
0	0		0	0	0	0	0	0	0	1	1	0	1	1	0	1			0	0
0	0		0	0	0	0	0	0	0	0	1	1	0	1	1	0			0	1
0	0		0	0	0	0	0	0	0	0	0	1	1	0	1	1			0	1
0	0		0	0	0	0	0	0	0	0	0	0	1	1	0	1			0	1
0	0		0	0	0	0	0	0	0	0	0	0	0	1	1	0			0	1
0	0		0	0	0	0	0	0	0	0	0	0	0	0	1	1			0	0
0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	1			0	0
0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Message is assumed to be without error if the CRC register is returned to all zeroes.

SIZE
A

CODE	
SP	

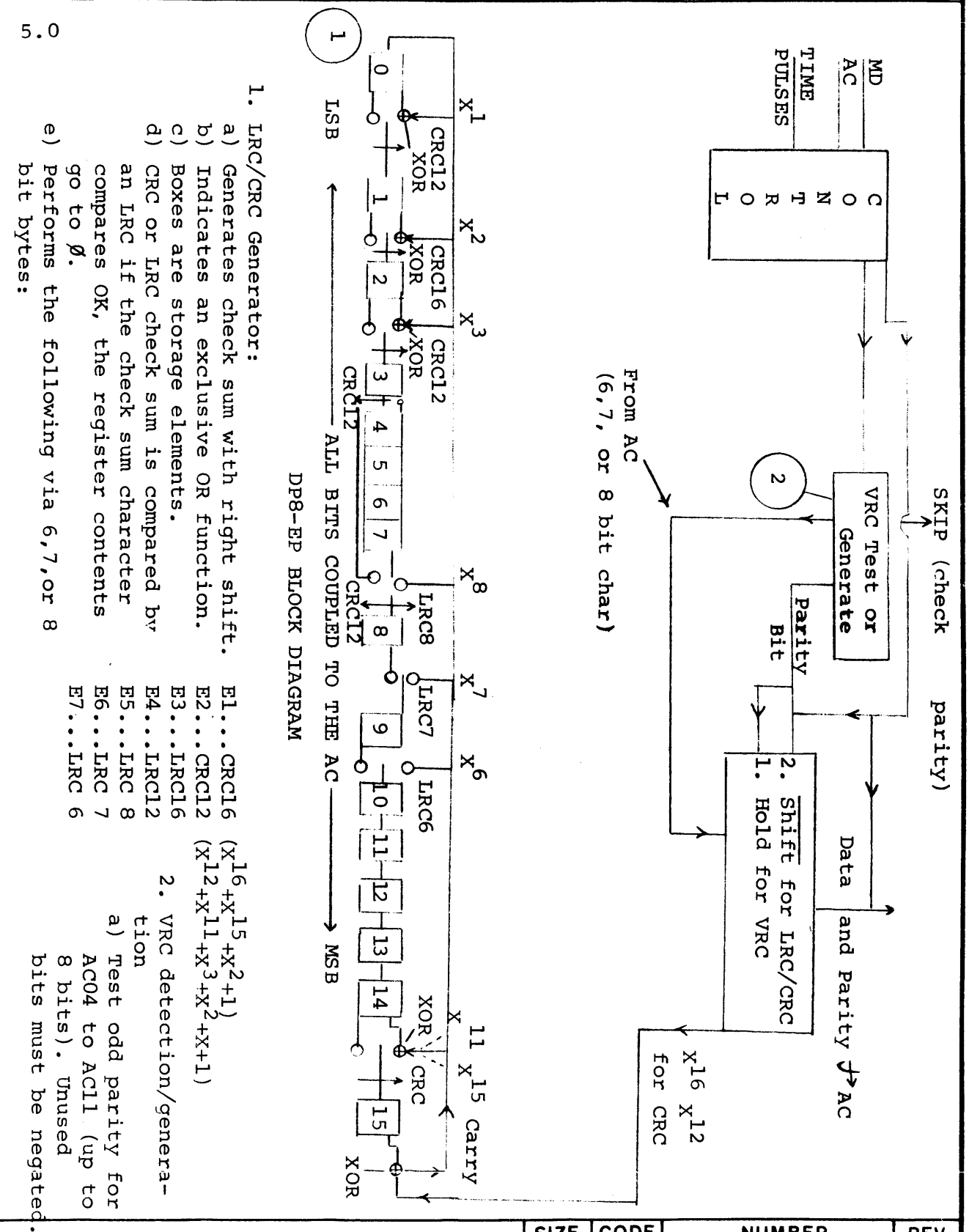
NUMBER
KG8-EA-1

REV
A

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CONTINUATION SHEET

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION



SIZE	A
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CODE	SP
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NUMBER
KG8-EA-1

REV
A

[illegible]

DEC FORM DEC 16 (325)-1031 N870
DRA 110

