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KY11-LB programmer's console/interface module operation and maintenance manual

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KY11-LB programmer's console/interface module operation and maintenance manual

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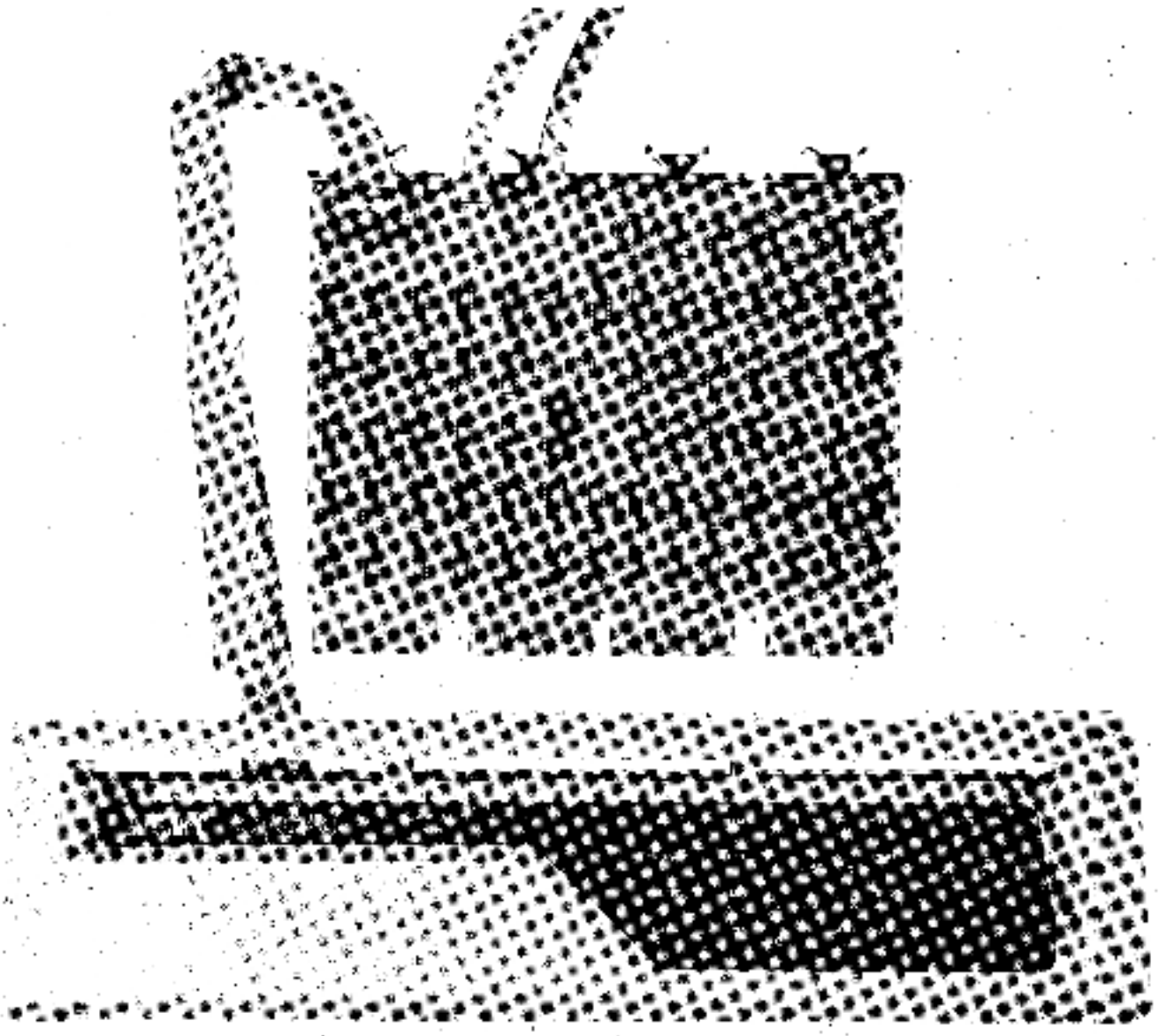

PREFACE

The *KY11-LB Programmer's Console/Interface Module Operation and Maintenance Manual* provides the information required to operate this option in console or maintenance mode. The manual also presents a detailed theory of operation of the interface module hardware and software components, data on the utilization of the programmer's console as a maintenance tool for the PDP-11/04/34 processors, and information on the troubleshooting and maintenance of the interface module itself. The information is presented in nine chapters:

Chapter 1	Provides an introduction, general description, and overview of electrical and mechanical specifications.
Chapter 2	Presents a functional description of the console, operating modes, controls and indicators, and a general discussion of interface module hardware organization and software facilities.
Chapter 3	Describes, on a detailed block diagram level, interface module functions, registers and controls, and the functions of the MOS/LSI microprocessor.
Chapter 4	Describes the microprocessor instruction set.
Chapter 5	Presents a description of the M7859 Interface module to the logic level.
Chapter 6	Provides operating information on console utilization in console mode.
Chapter 7	Contains procedures for using the console in maintenance mode (maintenance of PDP-11/04/34 processor).
Chapter 8	Covers some maintenance techniques for the KY11-LB interface module.
Chapter 9	Describes installation procedures for various options.

NOTES

In the material presented in this manual, the term "processor" refers to the KD11-D, KD11-E, and KD11-EA PDP-11/04/34 processors.

If the operator is not familiar with console functions, Chapter 6 should be consulted.

CHAPTER 1
OPERATING CHARACTERISTICS

1.1 INTRODUCTION

The PDP-11/04/34 Programmer's Console and Interface module (KY11-LB) provides all the functions now offered with the PDP-11/05. The Programmer's console interfaces to the Unibus (Figure 1-1) through a quad SPC module. To use this option, the normally provided KY11-LA Programmer's Console must be removed and the KY11-LB Console installed in its place. The KY11-LB Console contains a 7-segment LED display and a 20-key keypad for generating the console commands. Several indicators are also provided for additional convenience in monitoring system status.

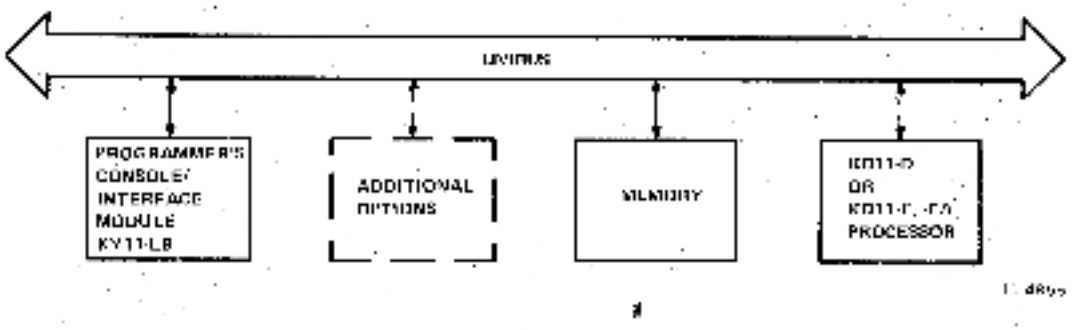

Figure 1-1 Programmer's Console/Interface – PDP-11/04/34 Configuration

The KY11-LB Programmer's Console/Interface module comprises an INTEL 8008 single-chip, large scale integration (LSI) microprocessor and associated registers, Unibus control logic, and auxiliary memory. The unit is also provided with a 20-key keypad for operator/programmer interaction with the KD11-D, -E, -EA via the interface module, six indicator LEDs, a 6-digit, 7-segment display for address or data, and a dc power switch. The microprocessor communicates with a read-only memory (ROM) which contains a number of fixed routines for use during normal console and maintenance operation.

1.2 GENERAL DESCRIPTION

The M7859 Interface module (Figure 1-2) functions as the interface between the programmer's console and the KD11-D, KD11-E, or KD11-EA processor, via the Unibus. The unit consists of solid state integrated circuits with TTL-compatible input and output lines. The heart of the interface module is a single-chip, large scale integration (LSI) microprocessor which executes designated keyboard functions via programs stored in ROM memory. Auxiliary logic functions including clock, decoding and timing circuitry, and addressing and Unibus drivers/receivers comprise the remaining logic of the board.

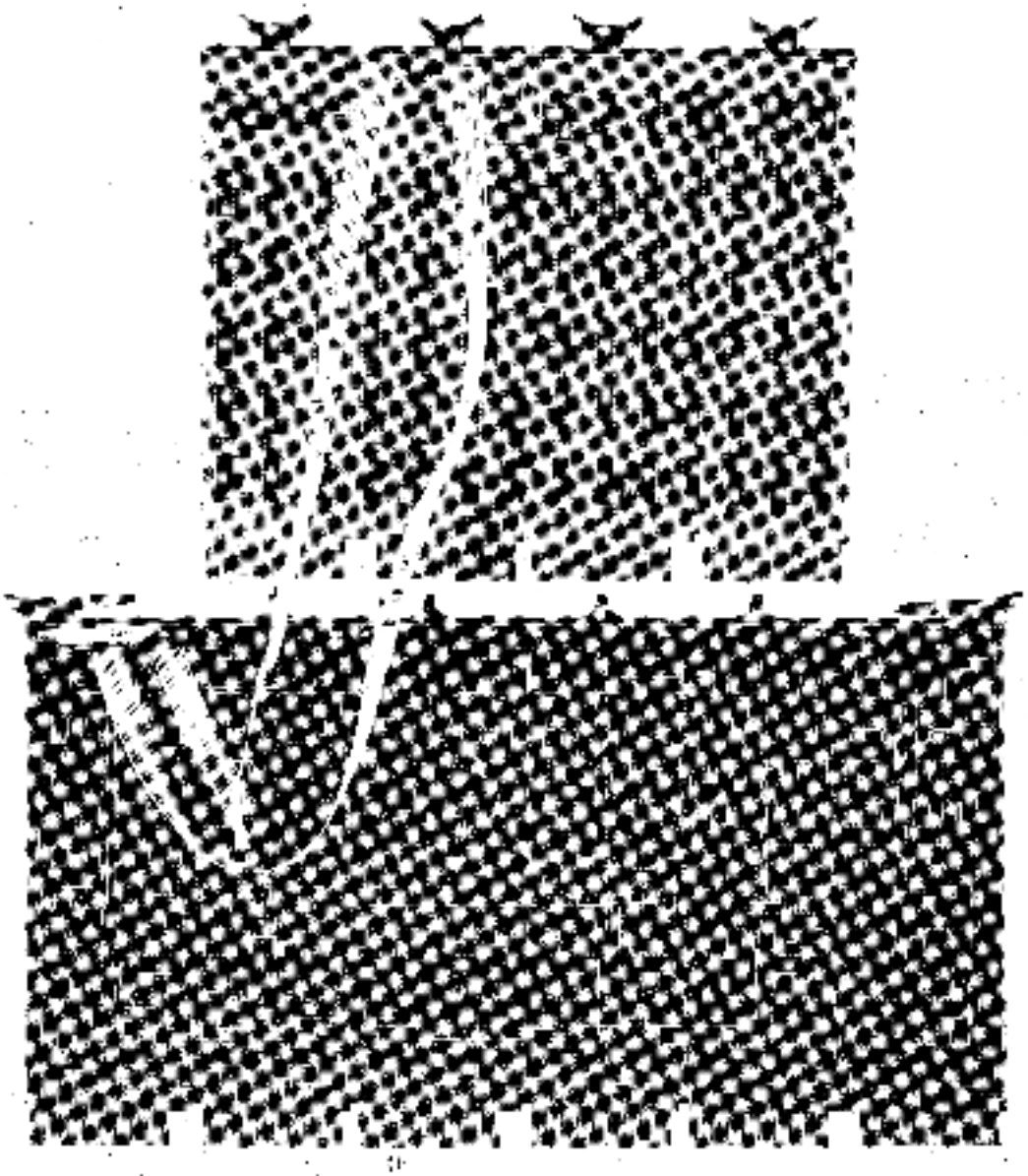

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Figure 1-2 Interface Module (M7859)

The microprocessor chip is an 8-bit, parallel control element packaged as a single metal oxide silicon circuit in an 18-pin, dual in-line package. With the addition of external clock driving circuitry and decoding elements, plus memory and data bus control, the unit is capable of performing as a powerful, general-purpose, central processing unit. Internal logic of the microprocessor chip is structured around an 8-bit internal data bus and includes instruction decoding, memory control; accumulator and scratchpad memory, arithmetic and logical capability, program stack, and condition code indicators. Data transfer between the microprocessor chip and the remaining logic functions of the interface module is accomplished through an 8-bit, bidirectional data port which is an integral part of the microprocessor. An internal stack (scratchpad memory) contains a 14-bit program counter (PC) and an additional complement of seven 14-bit registers for nesting up to seven levels of subroutines. The 14-bit addressing capacity allows the microprocessor to access up to 16K memory locations which may comprise any mix of ROM or RAM.

1.3 FUNCTIONAL DESCRIPTION

The KY11-LB Programmer's Console permits the implementation of a variety of functions through a 20-key keypad located on the front panel of the programmer's console. Keypad functions are divided into two distinct modes: console mode and maintenance mode. In console mode operation, a number of facilities exist for displaying addresses and data, for depositing data in and examining the content of Unibus addresses including processor registers for entering data into a temporary buffer for use as address or data, and for single instruction stepping the processor. The latter feature is especially useful during program debugging functions.

Normal console keyboard functions are not available during maintenance mode. This mode permits sampling and display of the Unibus address lines and Unibus data lines, and may allow the console to take control of the Unibus to examine and deposit Unibus addresses if a processor is not present in the system or is malfunctioning. Additionally, the maintenance function permits assertion of the manual clock enable and display of the current processor microprogram counter (MPC). Single-clock cycling of the MPC is also possible to facilitate step by step checkout of processor op codes and control logic during maintenance functions. In conjunction with this function, assertion of manual clock enable permits the processor to be stepped through its power-up routine. The manual clock enable may be dropped via the START key at any time with a resulting dislay of the current MPC. Exit from maintenance mode to console mode may be accomplished at any time by depressing the CLR key on the keypad.

1.4 SPECIFICATIONS

1.4.1 M7859 Interface Module Performance Specifications

Operating Speed at 500 kHz	
Two-Phase Clock Period	2 μs
Time State (SYNC)	4 μs
Instruction Time (Microprocessor)	12–44 μs
Word Size	
Data	8-bit word
Instruction	1, 2, or 3 8-bit words
Address	14 bits
Memory Size	
ROM	4 512 × 4 organized as 1024 8-bit words
RAM	16 words by 8 bits

Input/Output Lines	
Memory Data	16 bits
Address	18 bits
Control (Address)	2 bits
Unibus Control	5 bits
Microprocessor Instruction Repertoire	
48 Basic Instructions	
Instruction Categories	Register Operation Accumulator PC and Stack Control I/O Machine

1.4.2 Electrical Specifications

Power Supply	+5 V at 3.0 A −15 V at 60 mA
Input Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.8 Vdc
TTL Logic High	2.0 to 3.6 Vdc
Output Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.4 Vdc
TTL Logic High	2.4 to 3.6 Vdc
Power Consumption	
Interface Module	14 W
Monitor/Control Panel	1 W

1.4.3 Mechanical Specifications

M7859 Interface Module	
Board Type	Quad SPC
Dimensions	
Height	21.44 cm (8.44 in)
Length	26.08 cm (10.44 in)
Programmer's Console (Overall Panel Dimensions)	
Width	47.63 cm (18.75 in)
Height	13.02 cm (5.125 in)
Depth	6.76 cm (2.66 in)

1.4.4 Environmental Specifications

Ambient Operating Temperature	5° to 50° C (41° to 122° F)
Humidity	10% to 95% maximum, wet bulb 32° C (90° F)

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

Logical organization of the KY11-LB Interface module is centered around a microprocessor and a bidirectional data bus (Figure 2-1). The 8-bit data and address bus (D0–D7) is time multiplexed to permit control signals, 14-bit addresses, and data to be transmitted between the microprocessor, memory, and additional buffer registers. Two registers, the switch register and the bus address register, contain data and addresses (respectively) to be routed to the Unibus. The transceivers permit 16-bit data words to be loaded into the microprocessor from the Unibus via the 2-way data bus. Data flow depends on the type of operation indicated by the keypad and the instruction the microprocessor is executing at a given time.

In a typical operation involving an instruction fetch, for example, the microprocessor program counter contents are transferred to the address register in two successive 8-bit bytes. The address register outputs activate the appropriate ROM location containing the instruction. The instruction is routed back via the tristate transceivers and the bidirectional bus to the microprocessor for decoding and subsequent execution. Instructions range from one to three bytes in length; the state counter decoding is capable of discriminating between the op code types and the resulting instruction length. The microprocessor is driven by a nominal 500-kHz, symmetrical, two-phase, nonoverlapping clock and is capable of responding to externally generated interrupt conditions. The data interface is a bidirectional 8-bit bus and the unit also provides four control outputs which include three state control signals and a sync signal. The control signals are applied to external decoding logic to generate system timing states and are subsequently distributed to the remaining interface module control circuitry. The state control signals are also utilized in the chip for sequencing data processing operations.

2.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTIONS/CONTROLS AND INDICATORS

Operator/programmer control of the KY11-LB is accomplished through a 20-key keypad located on the console panel (Figure 2-2). A summarized description of the key functions and other controls and indicators is contained in Table 2-1. The table first presents those functions involved in console mode which are primarily of interest to the programmer. A second portion of the table describes entry into maintenance mode and presents facilities useful for processor checkout and maintenance. The CNTRL key functions primarily as an interlock which prevents accidental interference with other console operations.

2.2.1 Console Mode

Detailed presentation of console mode keypad functions and their use in program debugging is reserved for a later chapter; the various functions are outlined and briefly described in Table 2-1. The operator indicators available for both modes are also described. Upon power-up, the programmer's console is in console mode. If in maintenance mode, pressing the CLR key causes a reversion to console mode through a HALT.

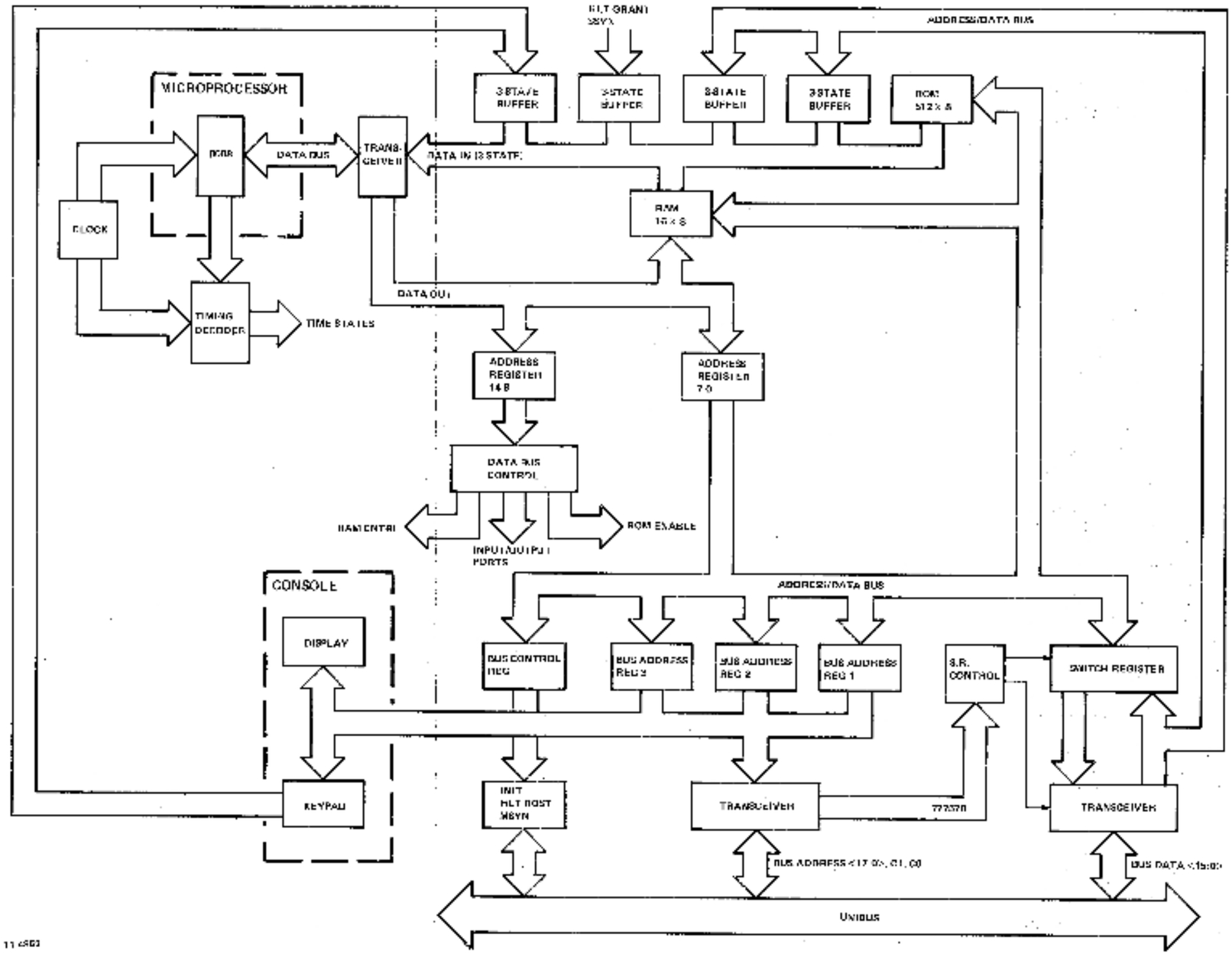


Figure 2-1 KY11-LB Logical Organization

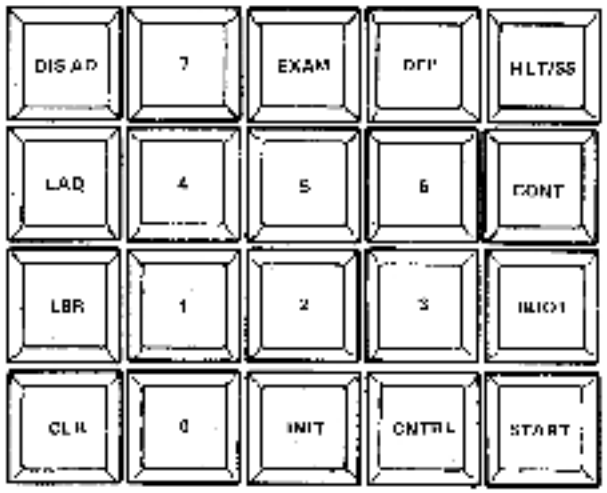


Figure 2-2 KY11-LB Keypad

Table 2-1 KY11-LB Controls and Indicators

Control/Indicator	Function
	Keyboard – Console Mode
LAD	Load Address – Moves the 18-bit number in the temporary register into the Unibus address pointer. The temporary register is then cleared and displayed.
LSR	Load Switch Register – Moves the 16 lower bits of the temporary register to a register which can be read via Unibus address 777570. The switch register contents will be displayed.
DEP	Deposit – Causes the console to do a **DATO** on the bus address pointed to, using the data in the temporary register (two MSBs are truncated). Sequential deposits cause the address pointer to be incremented. This key is operative only if the processor is halted.
0–7	Numerics – These keys are used to enter data into a temporary data buffer prior to use as either address or data. Use of a numeric key forces the console to display the data held in the temporary buffer. A 6-digit number is generated as octal digits are entered from the right and left shifted.
CNTRL	Control – This key is used only in conjunction with other keys either to prevent accidental operation of certain functions or to provide entry into maintenance mode or other features. When used, the CNTRL key must be pressed first and held down while the second key is pressed. Those keys which are interlocked with the CNTRL key are indicated by "CNTRL-second key" (e.g., CNTRL-START).

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
CNTRL-INIT	Initialize – Operative only if the processor is halted. Causes BUS INIT L to be generated for 150 ms.
DIS AD	Display Address – This key causes the current Unibus address pointer to be displayed. The next examine or deposit will occur at the address displayed.
EXAM	Examine – Causes the console to do a DATI on the bus address pointed to and stores the data in the temporary register which is then displayed. Sequential examines cause the address pointer to be incremented by 2 or by 1 if the address is in the range 777700–777717. This key is operative only if the processor is halted.
CLR	Clear Entry – Clears the current contents of the temporary register which is then displayed.
CNTRL-BOOT	Causes M9301 bootstrap terminator to be activated if present in the system. Console will boot only if the processor is halted.
CNRL-HALT/SS	Halt/Single Step – Halts the processor if the processor is running. If the processor is already halted it will single-instruction step the processor. It also retrieves and displays the contents of R7 (program counter). The CNTRL key is not required to Single-Instruction Step the machine.
CNTRL-CONT	Continue – Allows processor to continue using its current program counter from a halted state. The contents of the switch register are displayed.
CNTRL-START	Operative only if halted, this causes the program counter (R7) to be loaded with the contents of the Unibus address pointer. BUS INIT L is then generated and the processor is allowed to run. Switch register contents are then displayed.
CNTRL-7	Causes the Unibus address pointer to be added to the temporary data buffer which is also incremented by 2. This allows the console to calculate the correct offset address when mode 6 or 7, register 7 PIC (Position Independent Code) instructions are encountered.
CNTRL-6	This causes the switch register to be added to the temporary data buffer. This is useful when mode 6 or 7 instructions are encountered not using R7.
CNTRL-1	Maintenance Mode – This combination puts the console into maintenance mode with certain maintenance features available. When the console is in maintenance mode, the normal console mode keypad functions are not available. The CLR key causes the console to exit from maintenance mode into console mode via a processor halt.

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
	Keyboard – Maintenance Mode
	NOTE **In maintenance mode the keypad functions are redefined with the following definitions.**
DIS AD	Causes the Unibus address lines to be sampled and displayed.
CLR	Returns the console to console mode via a console halt.
EXAM	Causes the console to sample the Unibus data lines and display the data.
5	Causes the console to take control of the Unibus. Should be used only when a processor is not present in the system.
HLT/SS	Asserts manual clock enable and displays the current microprogram counter (MPC).
CONT	Asserts manual clock enable, generates a manual clock pulse, and displays the current MPC.
BOOT	Boots the M9301. If manual clock enable is asserted, this will allow the processor to be stepped through the power-up routine.
START	Drops manual clock enable and displays the current MPC.
	Indicator LEDs – Any Mode
DC ON	All dc power (+5 V) to logic is on.
BATT	Battery monitor indicator, operative only in machines having the battery back-up option. This indicator has four states: Off – Indicates either no battery present or battery failure if a battery is present. On (continuous) – Indicates that a battery is present and charged. Flashing (slow) – Indicates ac power is ok and battery is charging. Flashing (fast) – Indicates loss of ac power and that battery is discharging while maintaining MOS memory contents.
RUN	Indicates the state of the processor, either running or halted.

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
SR DISP	Indicates that the content of the switch register is being displayed.
MAINT	Indicates that console is in maintenance mode.
BUS ERR	Indicates that an examine or deposit resulted in a SSYN time-out or that HALT REQUEST failed to receive a HALT GRANT.
DC Power Switch	
DC OFF	All dc power to logic is off.
DC ON	All dc power to logic is on.
STNBY	DC power is provided to MOS memory only.*

*Available in all BA11-C machines. Available in BA11-K boxes which have Battery Backup Option only.

Table 2-1 refers to certain registers which are located in the scratchpad RAM. These include the following:

1. Display Data
2. Keypad Image
3. Temporary Data Buffer
4. Unibus Address Pointer
5. Switch Register Image
6. EXAM, DEP, ENB and C1 flags

Detailed discussion of the scratchpad RAM and its registers is set forth in Chapter 5.

2.2.2 Maintenance Mode

Maintenance mode is entered by pressing the CNTRL key and the 1 key simultaneously. Note that the functions performed by the appropriate keys are quite different from console mode. This mode offers the ability to assert the manual clock enable and thus to single-clock cycle the processor while monitoring the contents of the processor microprogram counter.

2.3 HARDWARE ORGANIZATION

A detailed block diagram of the interface module showing data flow and control is indicated in Figure 2-3. The control functions shown include those for the Unibus interface and the internal data bus with the microprocessor. The latter controls include those for reading from and writing into the RAM, enabling ROMs 1 and 2, and reading the Unibus temporary buffer register or loading the bus address and switch registers. All of these functions occur on appropriate control from the stored program and keypad.

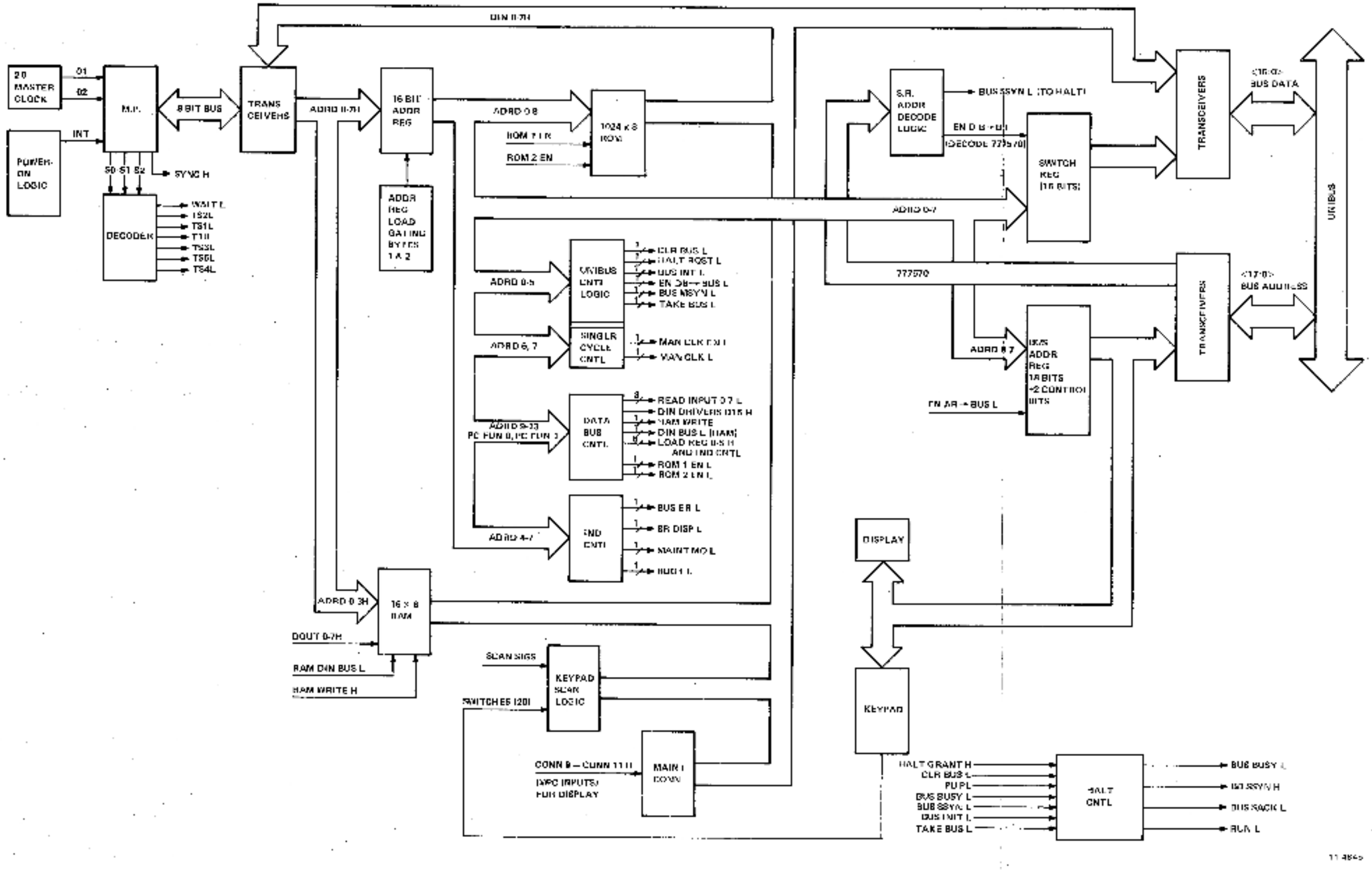


Figure 2-3 Interface Module Detailed Block Diagram

Under microprogram control, the data bus control logic develops the loading or reading signal for the appropriate register and thus determines the selected input/output port via the data bus control and the function currently being executed.

As shown in Chapter 3 when the detailed microprocessor cycle is presented, the microprocessor executes four basic machine cycles. They are summarized here to show their relation to interface module functions.

1. *PCI* – This is always the first cycle of a microprocessor instruction and initiates the instruction fetch. The program counter is transferred in two bytes from the microprocessor to the 16-bit interface module address register (14 bits of address, 2 control bits) to fetch the instruction data from either the ROM or RAM. A single byte of instructions is retrieved during this cycle.

2. *PCR* – This cycle may retrieve an additional byte of instruction (if the instruction is a 2- or 3-byte instruction) or it may fetch a data byte if the indicated instruction contains only one byte.

3. *PCC* – This cycle specifies the function as an I/O operation. This machine cycle reads and loads the address and data registers which cause information to be read from or written into the microprocessor.

4. *PCW* – This cycle controls the memory write function according to the designated address.

Figure 2-3 shows that the basic satellite logic and control for the microprocessor chip consists of the following elements:

2-phase master clock
Decoder for interface module time states
Power-up logic
16-bit address register
16-word × 8-bit RAM
1024-word × 8-bit RAM (four – 512 × 4)
Switch register (16 bit)
Switch register address decoding
Bus address register (20 bit)
Tristate transceivers
Keypad scan and display logic
Data bus control
Unibus control and single-cycle control
Indicator control
Halt control

These major functions are briefly described in the following paragraphs; detailed theory of operation is presented in Chapter 5.

2-Phase Master Clock
The master clock drives the microprocessor internal logic and generates the system states for instruction sequencing. The nominal 1 MHz clock frequency is toggled down to two nonoverlapping, 500-kHz pulses known as phase 1 (Ø1) and phase 2 (Ø2). Phase 1 is normally used to pre-charge data lines and memories while phase 2 controls data transfers within the microprocessor.

Decoder for Timing States
The decoder element receives the state outputs S0, S1, and S2 from the microprocessor and generates the time states for the operation of the interface module. A sync pulse corresponding to two phase clock periods (1 time state) is also provided by the microprocessor.

Power-up Logic
This circuitry activates the microprocessor, clearing its various registers and generating a clear line to all the registers of the interface module. There are separate clears for the address register and all other registers.

Address Register
This 16-bit register is the principal buffer between the microprocessor and the remainder of the logic of the interface module. Although designated as an address register, the element also handles control data for the Unibus, data bus, and other control functions and outputs to the bus address and switch registers. One of its major functions is to receive the microprocessor program counter contents for fetching new instructions from the ROM or RAM.

RAM
The 16-word by 8-bit RAM gives the interface module a scratchpad memory which may be read or whose contents may be modified under program control.

ROM
The ROM, consisting of four 512 × 4-bit ROMs, makes a total of 1024 8-bit bytes available for the stored programs which execute the console functions.

Switch Register Address Decoding
This logic decodes 777570, an 18-bit address defining the switch register and a DATI on the Unibus to cause the switch register to be enabled onto the Unibus.

Switch Register
This 16-bit buffer register handles the data word to the Unibus.

Bus Address Register
This 20-bit register buffers address information between the interface module and the Unibus. Eighteen bits are allocated for the actual address, and two control bits indicate the direction of data flow. Scan signals for the keypad and NUM lines for the display logic are specified by this register.

Tristate Gates
These units are used to gate buffered Unibus data (16 bits) and Unibus address (18 bits) lines onto the tristate data bus by asserting an appropriate read input line. Keypad outputs and those maintenance lines provided for display of the processor microprogram counter are similarly buffered and gated. The outputs are all wire ORed onto the internal data bus and applied as input to the tristate transceivers.

Keypad Scan and Display Logic
This circuitry develops read and drive signals for the keypad and LED display respectively. Five read signals developed from the scan signals are used to scan the keypad switch closures in groups of four. The drive signals are applied to the LED displays whose values are determined by the 3-bit NUM input.

Data Bus Control
This circuitry performs all internal interface module control functions including RAM control, ROM enable, and selection of input/output ports. The logic also determines system operation during instruction, data fetch, or data out (TS3) via a 32- × 8-bit ROM.

Unibus Control
The Unibus control register supervises data transfers between the interface module and the Unibus. According to the input bit patterns to the register, data transfer from the interface module to the Unibus, halt request, bus master sync, and other functions may be generated as required for proper interfacing of the two elements. Two other signals generated in the Unibus control register permit single stepping of the processor clock.

Indicator Logic
This 4-bit register drives appropriate console indicators to show certain console states or errors. An indicator is turned on to show the existence of a bus error, when the switch register is being displayed or when in maintenance mode.

Halt Logic
This circuitry halts the processor under various conditions and performs handshaking functions when the console takes complete control of the bus. When a HALT from the console is detected by the processor, the processor recognizes it as an interrupt request. The processor then inhibits its clock and returns a recognition signal to the console causing the console to assert an acknowledge. The console now has complete control of the Unibus and processor and may maintain this condition, with the processor halted, as long as desired.

2.4 MICROPROCESSOR INSTRUCTION SET

The interface module microprocessor has a repertoire of 48 basic instructions. According to the instruction type, these may range from 1 to 3 bytes (8 to 24 bits) in length. The successive bytes of a given instruction must be located in sequential memory locations. Instructions fall into one of five categories:

Index Register
Accumulator (Arithmetic/Logical)
Program Counter and Stack Control
Input/Output
Machine

A description of the microprocessor instructions and the number of time states required for their execution is given in Chapter 4.

CHAPTER 3
INTERFACE MODULE

3.1 MICROPROCESSOR

3.1.1 General Organization

The microprocessor sends and receives data over an 8-bit data and address bus (D_0 to D_7) and utilizes four input and four output lines (Figure 3-1). The microprocessor contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits, and an 8-bit parallel binary arithmetic unit. The arithmetic element is capable of performing addition, subtraction, and logical operations. Additionally, a memory stack containing a 14-bit program counter and seven 14-bit words is used to store program and subroutine addresses. The microprocessor machine cycle usually requires five sequential states: TS1, TS2, TS3, TS4, and TS5. During time states TS1 and TS2, the external memory is addressed by a lower and an upper address byte respectively to form a 14-bit address. Also at TS1 time, the program counter (PC) is incremented for the next instruction fetch cycle. During time state TS3, the instruction addressed during states TS1 and TS2 is fetched and during the final two cycles, TS4 and TS5, it is executed. Figure 3-2 shows the possible number and sequence of the instruction states. Note that for this application of the microprocessor, the interrupt function is utilized only during the power-on sequence.

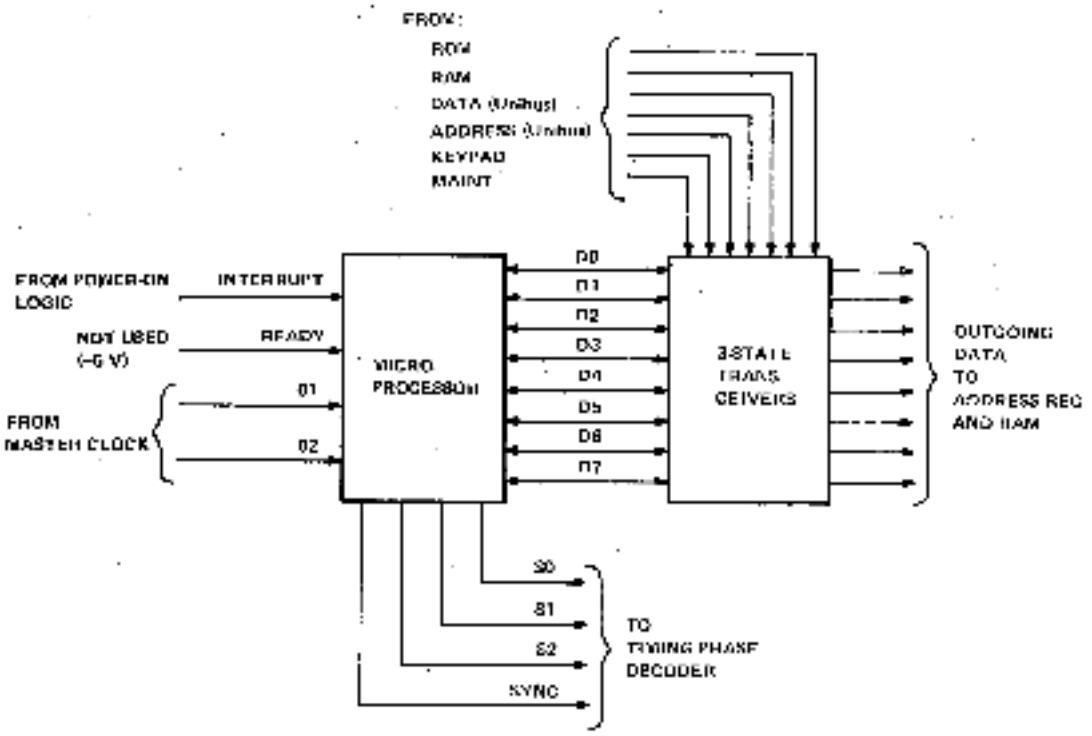


Figure 3-1 Microprocessor Signal Interface

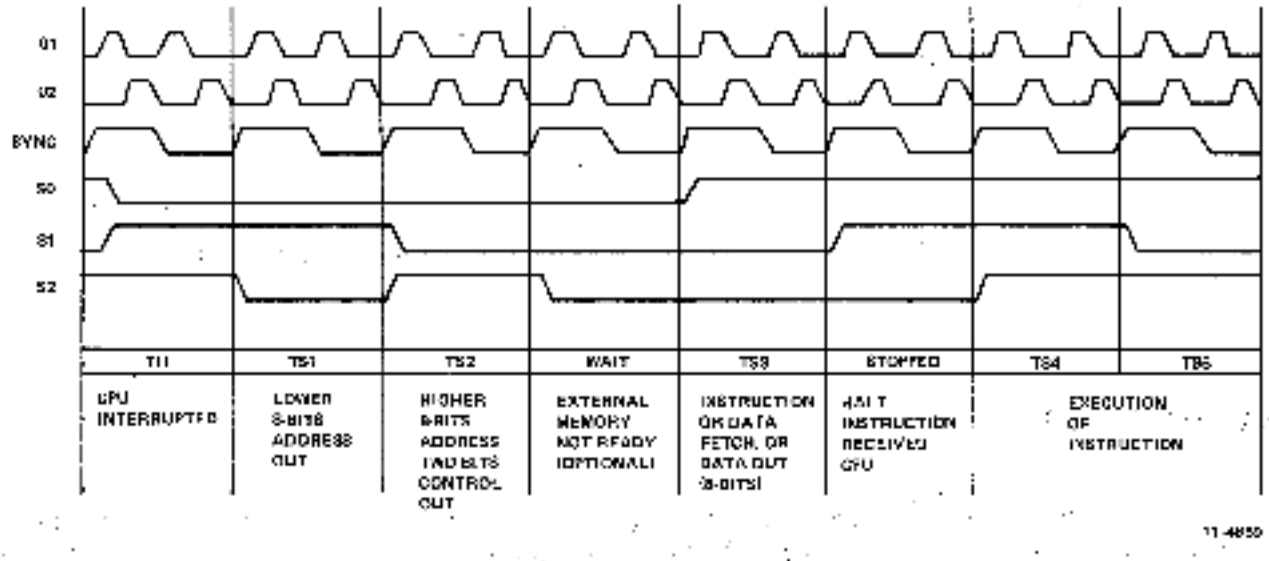


Figure 3-2 Timing Diagram – Microprocessor Instruction

3.1.2 State Control

The microprocessor operates as a sequential state machine, controls the use of the data bus, and, according to its stored program, determines whether it sends or receives data. Output state signals S0, S1, and S2 are decoded externally and distributed to the peripheral control logic. Table 3-1 shows the coding of the state bits to yield a given phase.

3.1.3 Microprocessor Timing

The microprocessor machine cycle is shown in Figure 3-2. Since machine operation is asynchronous, the exact timing sequences depend on the instruction executed. A typical cycle may consist of five states. During T1 and T2, an address is sent to memory; at T3 time, instruction or data fetch occurs; T4 and T5 provide execution time.

A number of microprocessor instructions may require up to three cycles and do not require the two execution states T4 and T5. As a result, cycle length is variable and the state counter determines whether T4 and T5 are to be executed or omitted. This is accomplished via the cycle control coding (Table 3-2) in bits D6 and D7. Cycle 1 is always an instruction fetch cycle (PCI). The second and third cycles are for data reading (PCR), data writing (PCW), or I/O operations (PCC). The cycle type bits D6 and D7 are present on the data bus during T2 time only.

Table 3-1 State Control Coding

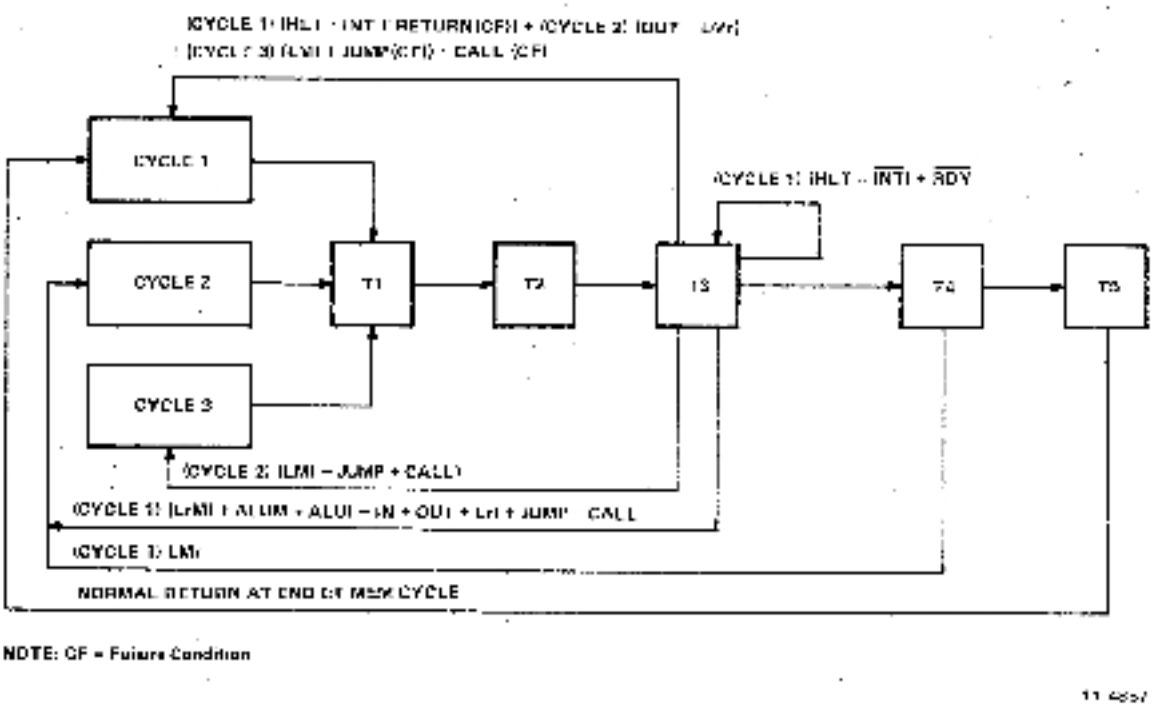
S0	S1	S2	State
0	1	0	T1
0	1	1	T11
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

Table 3-2 Cycle Coding

D_6	D_7	Cycle	Function
0	0	PCI	Designates the address is for a memory read (first byte of instruction).
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data).
1	0	PCC	Designates the data is a command I/O operation.
1	1	PCW	Designates the address is for a memory write data.

3.1.4 Transition State Diagram

Possible state transitions within the processor are shown in Figure 3-3. Note that a normal machine cycle would begin at cycle 1, run from T1–T5, and revert back to cycle 1 again. The state counter within the microprocessor operates as a 5-bit feedback shift register with the feedback path controlled by the current instruction. The number of states normally required by each instruction is discussed in Chapter 4.



NOTE: CF = Failure Condition

Figure 3-3 Transition State Diagram

3.1.5 System Start-Up

The microprocessor of the interface module is running any time power is applied to the system. When power (VDD) and clocks (01, 02) are first turned on, a flip-flop internal to the microprocessor is set by sensing the rise of VDD. This internal signal forces a HALT (00000000) into the instruction register and the microprocessor is then in the stopped state. The next 16 clock periods are required to clear internal chip memories and other external logic and registers. Upon clearing the registers the system is ready for operation. If for any reason during operation, the microprocessor decodes a HALT, the system reverts to the beginning of the program after 16 clock periods.

3.2 INTERFACE MODULE REGISTERS AND CONTROLS (Figure 2-1)

3.2.1 Address Register

This is the principal buffer register between the microprocessor and the rest of the interface module logic. It has a capacity of 16 bits (two 8-bit bytes). The low order byte is loaded by time state TS1 and the high order byte by time state TS2 during each cycle.

3.2.2 Bus Address Register

The bus address register buffers address data between the interface module and the Unibus. Address information may be loaded into this register at time state TS3.

3.2.3 Switch Register

Similar to the bus address register, the switch register buffers outgoing data. This element may also be loaded at TS3.

3.2.4 Data Bus Control

The principal function of the data bus control is to determine interface module operation during TS3 time. It determines, through input bit coding, the type of function to be performed (i.e., RAM control, ROM enable) or programs any of its other I/O in accordance with the stored program.

3.2.5 Unibus Control

This register is also loaded at TS3 and is selected by the data bus control for activation at that time. According to its input coding, U.C.R. may issue a HALT request, BUS INIT, enable-data bus-to-bus, or generate a bus master sync in addition to other functions.

CHAPTER 4
MICROPROCESSOR INSTRUCTION DESCRIPTION

4.1 DATA AND INSTRUCTION FORMATS

Data in the CPU is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference I/O arithmetic or logical, rotate or return instructions.

Two Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Immediate mode instructions.
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	

Three Byte Instructions

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	

*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

4.2 MICROPROCESSOR INSTRUCTIONS

4.2.1 Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

Mnemonic	Minimum States Required	Instruction Code D_7D_6	$D_5D_4D_3$	$D_2D_1D_0$	Description of Operation
(1) Lr_1r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) LrM	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) LrI	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INr	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

4.2.2 Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

Mnemonic	Minimum States Required	Instruction Code D_7D_6	$D_5D_4D_3$	$D_2D_1D_0$	Description of Operation
ADr	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ACr	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACM	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	

Mnemonic	Minimum States Required	Instruction Code D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Description of Operation
SUr	(5)	1 0 0 1 0 S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0 0 1 0 1 1 1	
SUI	(8)	0 0 0 1 0 1 0 0 B B B B B B B B	
SBr	(5)	1 0 0 1 1 S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1 0 0 1 1 1 1 1	
SBI	(8)	0 0 0 1 1 1 0 0 B B B B B B B B	
NDr	(5)	1 0 1 0 0 S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1 0 1 0 0 1 1 1	
NDI	(8)	0 0 1 0 0 1 0 0 B B B B B B B B	
XRr	(5)	1 0 1 0 1 S S S	Compute the Exclusive OR of the content of index register r, memory M, or data B . . . B with the accumulator.
XRM	(8)	1 0 1 0 1 1 1 1	
XRI	(8)	0 0 1 0 1 1 0 0 B B B B B B B B	
ORr	(5)	1 0 1 1 0 S S S	Compute the Inclusive OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
ORM	(8)	1 0 1 1 0 1 1 1	
ORI	(8)	0 0 1 1 0 1 0 0 B B B B B B B B	
CPr	(5)	1 0 1 1 1 S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1 0 1 1 1 1 1 1	
CPI	(8)	0 0 1 1 1 1 0 0 B B B B B B B B	
RLC	(5)	0 0 0 0 0 0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0 0 0 1 0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0 0 1 0 0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0 0 1 1 0 1 0	Rotate the content of the accumulator right through the carry.

4.2.3 Program Counter and Stack Control Instructions

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
(4) JMP	(11)	0 1 X X X 1 0 0 B_3 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$.
(5) JFc	(9 or 11)	0 1 0 C_4 C_3 0 0 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) JTc	(9 or 11)	0 1 1 C_4 C_3 0 0 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
(4) CAL	(11)	0 1 X X X 1 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$. Save the current address (up one level in the stack).
(5) CFc	(9 or 11)	0 1 0 C_4 C_3 0 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(5) CTc	(9 or 11)	0 1 1 C_4 C_3 0 1 0 B_2 B_2 B_2 B_2 B_2 B_2 B_2 B_2 X X B_3 B_3 B_3 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3 B_2 \ldots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(4) RET	(5)	0 0 X X X 1 1 1	Unconditionally return (down one level in the stack).
(5) RFc	(3 or 5)	0 0 0 C_4 C_3 0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) RTc	(3 or 5)	0 0 1 C_4 C_3 0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0 A A A 1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

4.2.4 Input/Output Instructions

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
INP	(8)	0 1 0 0 M M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1 R R M M M 1	Write the content of the accumulator into the selected output port (RRMMM) (RR ≠ 00).

4.2.5 Machine Instruction

Mnemonic	Minimum States Required	Instruction Code D_7D_6 $D_5D_4D_3$ $D_2D_1D_0$	Description of Operation
(4) HLT	(4)	0 0 0 0 0 0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1 1 1 1 1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register
DDD = Destination Index Register
These registers, r_i, are designated A (accumulator 000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00 overflow or underflow), zero (01-result is zero), sign (10 MSB of result is "1"), parity (11-parity is even).

CHAPTER 5
INTERFACE MODULE DETAILED LOGIC DESCRIPTION

5.1 INTRODUCTION

Keypad operation initiates appropriate microprocessor routines which perform certain data transfers within the interface module, between the interface module and the Unibus, and between the interface module and the programmer's console display. Prior to discussing the interface module logic, the sequences (i.e., register transfer, I/O operations, etc.) which occur after pressing a given key are briefly described.

Figure 5-1 shows the 16-word by 8-bit scratchpad RAM and its address allocations. This data is also summarized in Table 5-1. The keypad image within the RAM is shown in Figure 5-2.

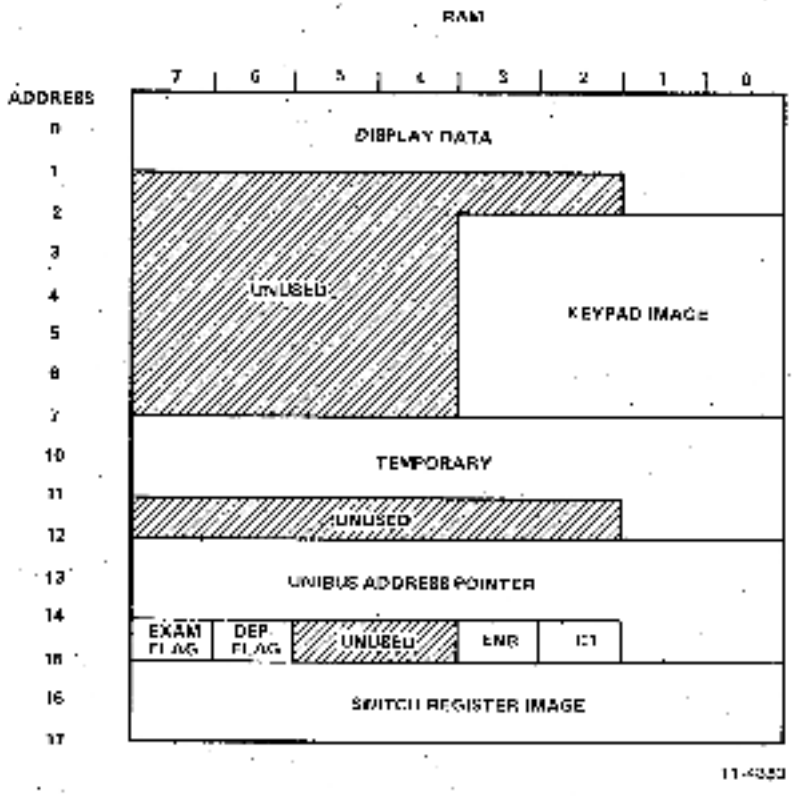


Figure 5-1 RAM Address Allocations

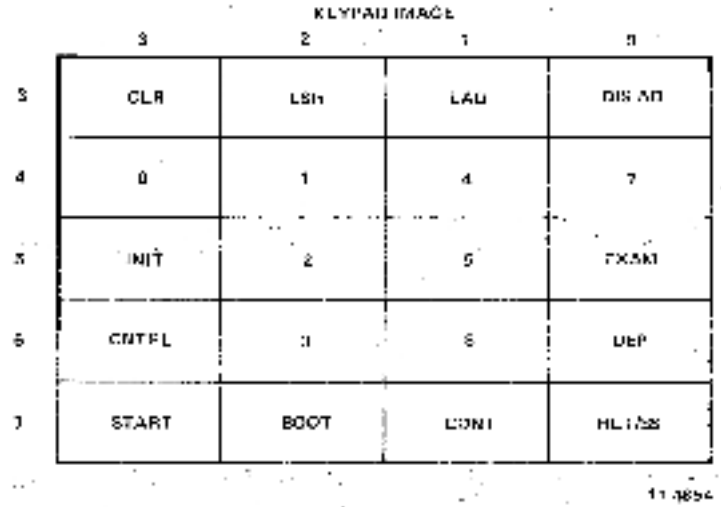


Figure 5-2 Keypad Image

Table 5-1 RAM Function Address Assignments

Function	Address (Octal)	Address Bits
Display Data (18 bits)	Word 0	Bits 0–7
	Word 1	Bits 0–7
	Word 2	Bits 0, 1
Keypad Image (20 bits)	Word 3	Bits 0–3
	Word 4	Bits 0–3
	Word 5	Bits 0–3
	Word 6	Bits 0–3
	Word 7	Bits 0–3
Temporary Data Buffer (18 bits)	Word 10	Bits 0–7
	Word 11	Bits 0–7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0–7
	Word 14	Bits 0–7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
C1 FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0–7
	Word 17	Bits 0–7

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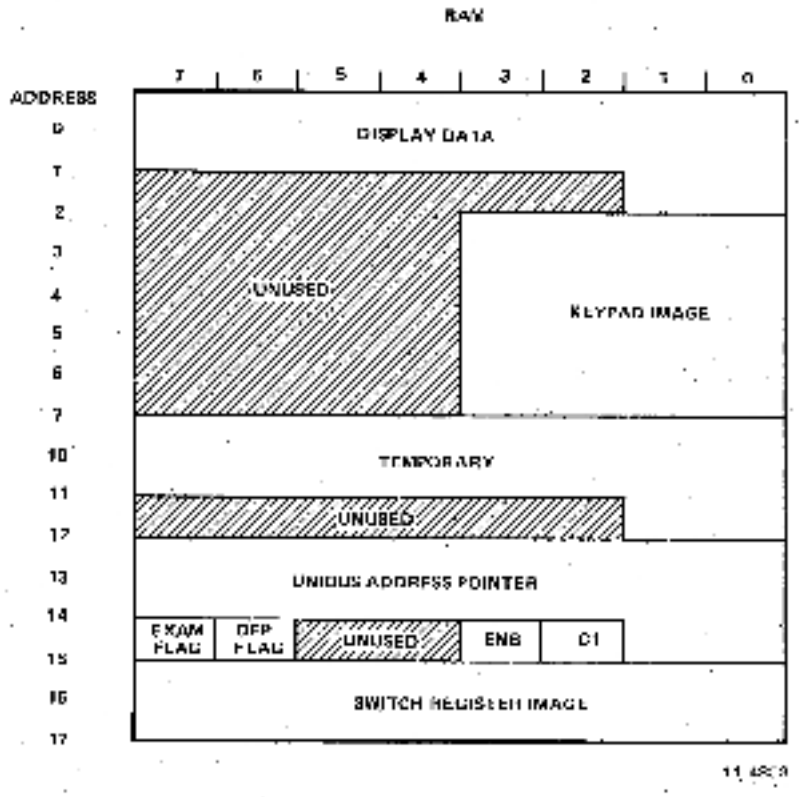
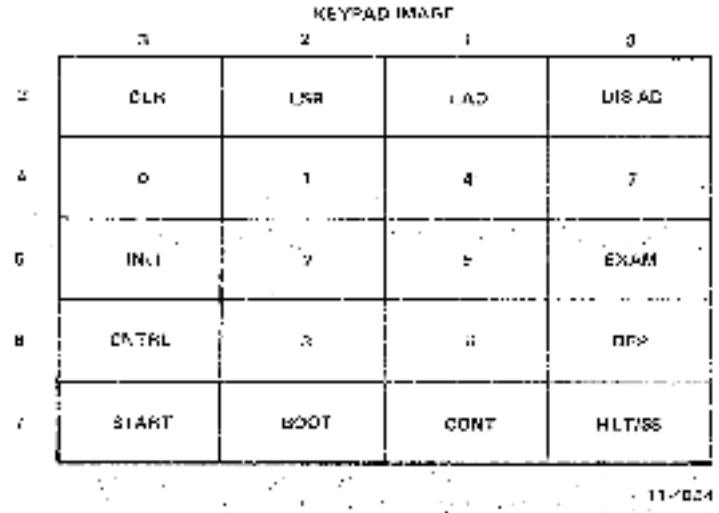


Figure 5-1 RAM Address Allocations



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	Word 5	Bits 0–3
	Word 6	Bits 0–3
	Word 7	Bits 0–3
Temporary Data Buffer (18 bits)	Word 10	Bits 0–7
	Word 11	Bits 0–7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0–7
	Word 14	Bits 0–7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
C1 FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0–7
	Word 17	Bits 0–7

5.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTION SEQUENCES

5.2.1 Console Mode Key Functions

NUMERICS (0–7)

1. Value of Key $\xrightarrow{\text{(left shifted)}}$ Temporary Data Buffer
2. Temporary → Display
3. Clear indicators.

LAD

1. Temporary → Unibus Address Pointer
2. Zero → Temporary
3. Temporary → Display
4. Clear/Indicators.

LSR

1. Temporary → Switch Register Image
2. Switch Register Image → Switch Register
3. SR DISP indicator is set.

CLR

1. Zero → Temporary
2. Temporary → Display
3. Clear indicators.

EXAM

1. Pre-increment Unibus address pointer if the EXAM flag is set.
2. Unibus Address Pointer → Bus Address Register
3. Bus Address Register → Unibus Address
4. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data → Temporary
6. Temporary → Display
7. Set EXAM flag.

DEP

1. Pre-increment Unibus address pointer if the DEP flag is set.
2. Unibus Address Pointer → Bus Address Register with C1 = 1.
3. Bus Address Register → Unibus Address
4. Temporary → Switch Register
5. Switch Register → Unibus Data
6. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

7. Set DEP flag.
8. Switch Register Image → Switch Register

DIS AD

1. Unibus Address Pointer → Display
2. Clear EXAM or DEP flag if set.

CNTRL–INIT

1. Set BUS INIT and HALT REQUEST for 150 ms.

CNTRL–HLT/SS

1. Clears BUS SACK/BUS BUSY if set and sets HALT REQUEST
2. When HALT BUSY is active, sets 777707 → Bus Address Register
3. Bus Address Register → Unibus Address
4. Assert MSYN

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data → Temporary
6. Temporary → Display

CNTRL–CONT

1. Clears BUS SACK and BUS BUSY.
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL–BOOT

1. Sets and clears BOOT signal
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL–START

1. 777707 → Bus Address Register with C1 = 1
2. Bus Address Register → Unibus Address
3. Unibus Address Pointer → Switch Register
4. Switch Register → Unibus Data
5. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μs, the transfer is aborted and the BUS ERR indicator is set.

6. Switch Register Image → Switch Register
7. Assert BUS INIT for 150 ms.
8. Switch Register Image → Display
9. Set SR DISP indicator.

CNTRL–7

1. Unibus Address Pointer + Temporary +2 → Temporary

CNTRL–6

1. Temporary + Switch Register Image → Temporary

CNTRL-P
1. Set maintenance indicator.
2. MPC Lines (sampled) → Display

5.2.2 Maintenance Mode Key Functions

CLR
1. Clears indicators.
2. Clears manual clock enable, if set.
3. Goes to halt condition.

DIS AD
1. Unibus Address (sampled) → Display

EXAM
1. Unibus Data (sampled) → Display

HLT/ISS
1. Sets manual clock enable.
2. Clears BUS SACK and BUS BUSY.
3. MPC (sampled) → Display

CONT
1. Sets and clears manual clock
2. MPC (sampled) → Display

BOOT
1. Sets and clears BOOT signal.

START
1. Clears manual clock enable, if set.
2. MPC (sampled) → Display

No. 5
1. Sets TAKE BUS signal, forcing console to assert BUS BUSY.

5.3 DETAILED LOGIC DESCRIPTION

5.3.1 Clock Circuitry

The M7859 Interface board is driven by an MC 4024 (E42) 1-MHz clock (drawing CS M7859-0-1, sheet 2). The 1-MHz output at E42-8 is toggled down to two nonoverlapping 500-kHz pulses at E12-5, 6, and E30, and these pulses are applied to the microprocessor (E18) input as 01 and 02. The 02 clock, designated as KY1 CK2 H and KY1 CK2 L, is also used as a control pulse to clear system registers and together with the sync pulse to define the end of a timing cycle.

Figure 5-1 shows the relation between the two clock pulses.

5.3.2 Power-Up Logic/Interrupt (Drawing CS M7859, Sheet 2)

The power-up logic/interrupt circuitry is comprised of E1-6, E40-10, E1-4, E36, E12, E29-1, E6, and E26. These elements sense when the system turns on, generate the interrupt to the microprocessor needed to start it, and clear registers to force program startup at location 0.

BUS DC LO at E1-3 initiates the function by clearing E36 which is configured as an 8-bit counter and generates KY1 PUP 1 L. This signal is routed to the Unibus control, indicator control, switch register, and bus address register as a master clear line. The address register is provided with its own clear line. KY1 ADR CLR L.

BUS DC LO L puts the microprocessor in the STOP state. The counter starts counting in the STOP state (E6, E36). KY1 STOP L and KY1 C2 L at E29-1 clock E6. E6 is a divide by two on the clock, while E36 counts from 0–7. Sixteen clock periods are thus counted. At the transition of E36 from 7 to 0, the interrupt is generated at E12-8 and the microprocessor goes into the TIT state (Interrupt). KY1 TIT L and KY1 CK2 L then reset E12 and clear the address register via E6-6 and the system is initialized.

5.3.3 Microprocessor (Drawing CS M7859, Sheet 2)

The 8008 Microprocessor Chip (E18) was discussed in detail in Chapter 3. According to drawing CS M7859, sheet 2, the unit communicates over an 8-bit bidirectional data bus via 8833 tristate transceivers E16 and E17, with the satellite logic of the interface module. A single interrupt line is received from the power-up logic to initiate microprocessor operations. Driven by a 2-phase, 500-kHz clock (Figure 5-1), the element yields a 3-bit state output code, S0, S1, and S2, plus a sync pulse, to drive a 7442 Timing Phase Decoder. The latter element provides eight separate timing cycles for the sequencing of interface module data transfers and other discrete operations.

5.3.4 Timing State Decoder

The timing state decoder (E23) receives the state outputs S0, S1, and S2 from the microprocessor and generates the timing states for the interface modules (drawing CS M7859, sheet 2). This unit is a 7442 4-line to 10-line decoder, with two unused outputs, that yields an 8-output sequence according to its 3-input state code. State control coding is presented in Chapter 3. State control inputs are determined in the microprocessor and depend on an internal 5-bit feedback shift register with the feedback path controlled by the instruction being executed.

5.3.5 Address Register (Drawing CS M7859, Sheet 2)

The address register, the principal buffer between the microprocessor and the remainder of the interface module logic, consists of four 74175 quad, D-type, double rail output latches. The low order bits are handled by E5 and E4 which generate KY1 ADRD 0 L through KY1 ADRD 3 L (E5) and their complements (for RAM addressing), and KY1 ADRD 4 H through KY1 ADRD 7 H (E4), respectively. This 8-bit byte is the low order unit of the address or data with E10 and E28 containing the high order information ADRD 08–13 and PC FUN 1 and 0.

The data contained in the address register is routed to the following locations according to direction by the stored program:

1. ROM (address of next instruction)(KY1 ADRD 0 L → KY1 ADRD 8 L plus ROM 1 EN L or ROM 2 EN L)
2. RAM (address of data to be read or written) (KY1 ADRD 0 L → KY1 ADRD 3 L)
3. Unibus Control (KY1 ADRD 0 H → KY1 ADRD 3 H)
4. Indicator Control (KY ADRD 4 H → KY1 ADRD 7 H)
5. Data Bus Control (KY1 ADRD 9 H → KY1 ADRD 13 H, KY1 PC FUN 0 H, KY1 PC FUN 1 H)
6. Switch Register (KY1 ADRD 0 H → KY1 ADRD 7 H)
7. Bus Address Register (KY ADRD 0 H → KY1 ADRD 7 H)

The address register is loaded with a low order byte (E4 and E5) by signal KY1 LD AD 1 H, generated by AND E22-12 at time state TS1. The high order byte is gated in E28 and E10 by KY1 LD AD 2 H generated at E22-6 at timing state TS2.

5.3.6 ROM

The interface module ROM consists of E3, E21, E33, and E39 (drawing CS M7859, sheet 3). The four 512-word by 4-bit elements are addressed so that the ensemble looks like two 512- × 8-bit RMs. E3 and E21 are activated by KY4 ROM 1 EN L and E33 and E39 by KY4 ROM 2 EN L. Address bits KY1 ADRD 0 H through KY1 ADRD 8 H are routed to all four ROM elements with the enable 1 or 2 determining the address activated and thus yielding 1024 8-bit locations. Outputs are wire ORed with various inputs to give the KY2 DIN 0 H through KY2 DIN 7 H inputs to the tristate transceivers, E16 and E17.

The ROM 1 or RM 2 enables are generated by the data bus control logic.

5.3.7 RAM

The scratchpad RAM consists of E11 and E27 (drawing CS M7859, sheet 3). These units effectively comprise a 16-word by 8-bit read/write memory, and serve as working storage for the microprocessor programs in storing addresses and data. Data is routed to the RAM (KY1 DOUT 0 H through KY1 DOUT 7 H) directly from the tristate transceivers of the microprocessor bidirectional data bus during RAM write operations. The 4-bit address lines KY1 ADRD 0 L through KY1 ADRD 3 L specify the address to be read from or written into during read/write.

Selection of the RAM for read or write is determined by the stored program via the data bus control. Either KY4 RAM → DIN BUS L or KY4 RAM WRITE H must be true to select the RAM. Output lines are wire ORed with various other microprocessor input ports to be routed to the 8833 tristate transceivers.

5.3.8 Switch Register (Drawing CS M7859, Sheet 6)

The switch register contains the 16-bit data used and consists of four 74175 quad, D-type, double rail output latches. The four elements comprising the register are E9, E19, E2, and E15. These units feed the 8641 bus transceivers E7, E25, E8, and E13 (respectively). Incoming 16-bit data (KY5 BB D00 H through KY5 BB D15 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control. Outgoing data (BUS D00 L through BUS D15 L) is gated by KY4 EN DB L, a signal generated in the switch register address decoding logic (sheet 5).

The switch register is addressable from the Unibus as address 777570 as described in Paragraph 5.3.9.

5.3.9 Switch Register Address Decode Logic (Drawing CS M7859, Sheet 5)

The switch register address decoding logic allows the Unibus to address the switch register via a decoding of address 777570. The logic has two outputs:

1. BUS SSYN L
2. KY4 EN DB → BUS L

K44 EN DB → BUS L at E43-10 gates the data lines onto the Unibus (CS M7859, sheet 6) while the assertion of BUS SSYN L designates that the slave device has completed its part of the data transfer. The second stage of the address decode at E32 is gated by assertion of BUS MSYN L at E32-10. Assertion of MSYN requests that the slave defined by the A (address) lines perform the function required by the C lines. In this case, KY7 BB C1 H at invertor E40-9 specifies that the data is to be transferred to the Unibus data lines.

5.3.10 Bus Address Register (Drawing CS M7859, Sheets 7 and 8)

The bus address register consists of five 74175 quad, D-type, double rail output latches. The five elements comprising the register are E67, E57, E73, E58, and E51. Input to the bus address register is from the address register (KY1 ADRD 0 H through KY1 ADRD 7 H). Outputs are routed to the display and keypad logic and to the 8641 Unibus transceivers E61, E56, E65, E55, and E50.

A Unibus address is enabled to the Unibus via the bus address transceivers from the bus address register by KY7 EN AR L generated at E51-11. The switch register is available to the Unibus as address 777570 via the bus address transceivers and the switch register decode logic. The latter function is discussed in Paragraph 5.3.9.

E67 and E57 contain the keypad scan signals (KY6 SCAN 1 L through KY6 SCAN 6 L) while E73 drives the display (KY6 NUM 1 H through KY6 NUM 3 H).

Incoming 18-bit address information (KY6 BB A00 H through KY7 BB A17 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control.

5.3.11 Data Bus Control Logic (Drawing CS M7859, Sheet 5)

The data bus control directs the reading and loading of the various interface module registers, the reading of the ROMs, and the reading/writing of the RAM. It also determines the direction of data flow in the interface module and between the interface module and the Unibus, i.e., whether data will be read from or be routed to the Unibus. A list of I/O functions and associated select signals follows:

Select Signal	Function
READ INPUT 0 L READ INPUT 1 L	UNIBUS DATA
READ INPUT 2 L READ INPUT 3 L READ INPUT 4 L	UNIBUS ADDRESS
READ INPUT 5 L	KEYPAD REG
READ INPUT 6 L READ INPUT 7 L	MAINTENANCE
LD REG 0 H LD REG 1 H LD REG 2 H	BUS ADDR REG
LD REG 3 H LD REG 4 H	SWITCH REG
LD REG 5 H	UNIBUS CONT LOGIC
EN ROM 1 L EN ROM 2 L	ROM SELECT
RAM WRITE H	RAM WRITE
RAM DIN BUS L	ENABLE RAM DATA
DIN DRIVERS DIS H	DISABLE DATA IN

Specifically, the data bus control logic decodes memory references into three areas (ROM 1, ROM 2, and RAM) and determines whether the access is a read or write. The logic also decodes I/O instructions and generates loading or gating signals depending on the direction of data transfer and the port selected.

In order to facilitate understanding of the logic, the following explanation of memory address allocation and I/O instruction operation is included.

ROM 2 (E33 and E39)
Memory addressing space spans locations 0 through 777.

ROM 1 (E3 and E21)
Memory addressing space spans locations 4000 through 4777.

RAM (E11 and E27)
Memory addressing space spans locations 20000 through 20017.

The two bus control signals provided by the microprocessor and latched with the upper byte of the address register, KY1 PC FUN 0 H and KY1 PC FUN 1 H, determine data transfer direction and I/O operations. The following table explains the decoding of these signals.

PC FUN 0	PC FUN 1	
L	L	Memory read of first byte of instruction only (fetch)
L	H	Memory read of additional bytes of instruction or data.
H	H	Memory write (used only to write into RAM).
H	L	I/O operation

Memory reads and writes signify that the address register (KY1 ADRD 0 H through KY1 ADRD 13 H) contains the address of the location in memory to be accessed.

The code for I/O operations, however, signifies a very different situation. This is due to the following occurring after the initial instruction fetch cycle:

1. During TS1 the content of the A register (accumulator) in the microprocessor is available on the data lines and is latched into the low byte of the address register.

2. During TS2 the content of the instruction register (containing the I/O instruction) is available on the data lines and is latched into the high byte of the address register.

3. During TS3 of an INP (input) instruction, data on the data lines is loaded into the A register. On OUT (output) instructions, the data is strobed out of the low byte of the address register.

   I/O Instruction Code:

   INP 01 OOMMM1
   OUT 01 RRMMM1

Note that the two most significant bits of the instruction will correspond to PC FUN 0 = 1 and PC FUN 1 = 0 when loaded into the high byte of the address register, thus denoting an I/O operation. Therefore, the data bus control logic determines whether to gate data into the microprocessor during TS3 (INP) or to load the data from the low byte of the address register into an output port during TS3 (OUT).

The 32 × 8 PROM (E34) does the initial decoding of the type of transfer (read, write, or I/O) from the signals KY1 PC FUN 0 H and KY1 PC FUN 1 H. If the transfer is a memory read or write, it is decoded into one of the following four signals. KY4 RAM → DIN BUS L (RAM read), KY4 ROM 1 EN L (memory read in address range 4000–4777), KY4 ROM 2 EN L (memory read in address range 000–777), and an enable which is ANDed with KY1 SYNC H, KY1 TS3 L, and KY1 CK2 L to provide a write pulse, KY4 RAM WRITE H, to the RAM.

Another enable from the PROM is ANDed with KY1 TS3 L to provide the signal KY4 DIN DRIVER DIS H. This signal is normally high, disabling the driver portions of the 8833 transceivers (E16 and E17). It will be low only during TS3 and when data transfer is into the microprocessor.

Two other outputs of the PROM are used for I/O operations. One output of the PROM (E34-7), when low, enables the 74154 4-to-16 decoder on all I/O instructions. The second output (E34-9) determines whether the I/O instruction is INP or OUT. If the instruction is OUT, then the signal will be high.

Note that address register bits KY1 ADRD 11, KY1 ADRD 10 H, and KY1 ADRD 9 H, are applied to the low order inputs of the 74154. This selects which of the possible ports will be used. The fourth input, the highest order input, determines if it is an INP or OUT instruction. This input is the ANDed condition of the PROM output (E34-9), KY1 SYNC H, KY1 TS3, and KY1 CK2. Thus, if the instruction is an INP, then the input gating signal will be one of the lower order eight outputs of the 74154 (KY4 READ IN 0 L through KY4 READ IN 7 L).

If the PROM signal (E34-9) is high, signifying an OUT instruction, then initially a low order output is selected (does not substantially affect anything) and then a high order output will be pulsed as the gated clock pulse is applied to the high order input of the 74154. Thus, the high order outputs are pulsed and buffered to provide loading pulses to the selected registers (KY4 LD REG 0 H, etc.).

5.3.12 Unibus Control (Drawing CS M7859, Sheet 5)

Unibus control is accomplished via two 74175 quad, D-type, double rail output latches, E52 and E64. The stored program input bit configurations are read in under control of an appropriate data bus control signal, LD REG 5 H. E64 D2 and D3 latches are utilized for the manual clock enable and manual clock lines while the other six lines are Unibus control signals.

5.3.13 Keypad Scan Logic (Drawing CS 5411800-0-1)

The logic and driving circuitry for the keypad and display elements is located on a circuit board in the rear of the programmer's console panel.

Scan signals for the keypad are generated at the interface module (bus address register). These six lines (KY6 SCAN 1 L through KY6 SCAN 6 L) are then routed through hex 7417 buffer drivers to the console circuit board where they are designated as READ and DRIVE signals. As indicated by CS 5411800-0-1, sheet 2, READ 1 through READ 5 signals continuously scan the keypad in groups of 4. As each READ signal is applied to check for a pressed key, a corresponding DRIVE signal is simultaneously generated and applied to the appropriate transistor in the LED display circuitry (CS 11800-0-1, sheet 3).

A pressed key thus results in activation of 1 to 4 lines. This information is routed out through J1 to the interface module and applied to the data bus for eventual read-in to the miroprocessor.

5.3.14 Indicator Logic (Drawing CS M7859, Sheet 5)

The indicator control consists of a single quad, D-type, latch configuration, 74175 (E68) and four 7417 open collector inverters (E69) for driving the panel indicators. Input bit coding KY1 ADRD 4 H through KY1 ADRD 7 H via the stored program determines which of the following panel indicators are turned on:

1. BUS ERR
2. SR DISP
3. MAINT
4. BOOT

5.3.15 Halt Logic (Drawing CS M7859-0-1, Sheet 9)

The halt logic allows the console to obtain control of the Unibus in order to perform Unibus transactions. Control of the Unibus is passed to the KY11-LB from the PDP-11 processor via a HALT REQUEST and HALT GRANT sequence. Use of the HALT/SS key initiates a program sequence within the KY11-LB to issue a HALT REQUEST to the PDP-11 processor. The processor will arbitrate the request and at the appropriate time will respond with HALT GRANT. The reception of HALT GRANT H by the halt logic direct sets the HALT SACK flip-flop on E63-4, causing BUS SACK L to be generated at E62-13. The set output of the HALT SACK flip-flop (E63-5) sets up the data input of the HALT BUSY flip-flop (E63-12).

The reception of BUS SACK L by the PDP-11 processor will cause it to drop HALT GRANT H. When the Unibus becomes free (unasserted BUS BUSY L and BUS SSYN L), the E63-11 will be clocked, setting the HALT BUSY flip-flop. This, in turn, asserts BUS BUSY L through E62-10 and causes the RUN indicator to be turned off via the 7417 buffer (E66-12). This logic operates in the same manner if the HALT GRANT is generated not by a HALT REQUEST from the KY11-LB but by a HALT instruction in the PDP-11 processor. The output of the HALT BUSY flip-flop (KY8 HALT BUSY H) can be tested by the microprocessor program to check if the console has control of the Unibus before performing Unibus transactions.

The HALT SACK and HALT BUSY flip-flops are direct cleared by either BUS INIT L from the Unibus or by the signal KY4 CLR BUS L which can be generated by the microprocessor program. Clearing these flip-flops relinquishes control of the Unibus to the PDP-11 processor.

The signal KY4 TAKE BUS L, which can direct set the HALT BUS flip-flop, allows the microprocessor program to perform Unibus operations without first obtaining the Unibus through a legal request. This signal is only used during maintenance mode operation of the KY11-LB to bypass a failing or hung processor.

5.3.16 Buffers (Drawing CS M7859, Sheet 4)

5.3.16.1 Tristate Buffers (8093) – The following units, which are gated by read input signals from the data bus control, buffer input data from several sources.

1. Unibus Data
2. Unibus Address
3. Keypad Register
4. Maintenance Inputs (from processor microprogram counter).

Outputs from the 8093s are wire ORed and sent to the tristate transceivers with the ROM and RAM data as KY2 DIN 0 H through KY2 DIN 7 H.

5.3.16.2 Tristate Transceivers (8833) – These units buffer data between the microprocessor bidirectional data bus and the satellite logic of the interface module.

CHAPTER 6
CONSOLE MODE OPERATION

6.1 INTRODUCTION

This chapter is a recapitulation of all console key and indicator functions. Operation, use, and examples of the utilization of each key are presented. Key operations are divided into console mode and maintenance mode. Examples of console sequences to demonstrate the proper use of the KY11-LB are presented together with further notes and hints on operation.

6.2 CONSOLE KEY OPERATIONS

This section describes the operation of each key in a step-by-step procedure. The reader is assumed to have read earlier chapters as some descriptions include the use of keys previously described.

A notation for each key will be introduced in each description and is enclosed in angle brackets < >. These notations are used extensively in Paragraph 6.4 to describe various sequences of key operations.

<CLR> – Used to clear an incorrect entry or existing data.

1. Press and release the CLR key.
2. The display (six digits) will be all zeros.
3. Clears the SR DISP, BUS ERR, or MAINT indicators if on.

Numerics 0–7 – Used to key in an octal numeric digit (0 through 7).

1. Press a numeric key (0 through 7).
2. The corresponding digit will be left shifted into the 6-digit octal display with the previously displayed digits also being left shifted.
3. Release the numeric key.

To enter the number <xxxxxx>, e.g., 123456:

1. Press and release the CLR key (000000 will be displayed).
2. Press and release the 1 key (000001 will be displayed).
3. Press and release the 2 key (000012 will be displayed).
4. Press and release the 3 key (000123 will be displayed).
5. Press and release the 4 key (001234 will be displayed).
6. Press and release the 5 key (012345 will be displayed).
7. Press and release the 6 key (123456 will be displayed).

The number has now been entered. Leading zeros do not have to be entered.

<LSR> – Used to load the switch register (accessible as Unibus address 777570).

1. Press and release the LSR key.
2. The display will show the data loaded and the SR DISP indicator will be on.

To load the number 777 i.e., **<LSR 777>**, into the switch register:

1. Press and release the CLR key.
2. Key in the number 777.
3. Press and release the LSR key.
4. 777 will be displayed and the SR DISP indicator will be on.

<LAD> – Used to load the Unibus address pointer prior to performing an EXAMINE, DEPOSIT, or START.

1. Press and release the LAD key.
2. Display will be all zeros.

To load address 200, i.e., **<LAD 200>**:

1. Press and release the CLR key.
2. Key in 200.
3. Press and release the LAD key.
4. Display is all zeros.

<DIS AD> – Displays the current contents of the Unibus address pointer.

1. Press and release the DIS AD key.
2. Display will show the current Unibus address pointer.

To perform the sequence:

LAD 400
DIS AD

1. Press and release the CLR key.
2. Key in 400.
3. Press and release the LAD key (display is all zeros).
4. Press and release the DIS AD key.
5. Display shows the 400 from the Unibus address pointer.

<DEP> – Used to deposit a number into the location pointed to by the Unibus address pointer.

1. Processor must be halted (RUN indicator off); otherwise key is ignored.
2. Press and release the DEP key.
3. Display shows the data deposited.

To deposit <DEP xxxx> (e.g., 5252) into location 1000, the sequence is as follows:

```
LAD 1000
DEP 5252
```

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Key in 5252.
5. Press and release the DEP key.

<EXAM> – Used to examine the contents of a location pointed to by the Unibus address pointer.

1. Machine must be halted.
2. Press and release the EXAM key.
3. Display shows the contents of the location examined.

To examine general-purpose register R7 (program counter) at Unibus address 777707, the following sequence is used:

```
LAD 777707
EXAM
```

1. Press and release the CLR key.
2. Key in 777707.
3. Press and release the LAD key.
4. Press and release the EXAM key.
5. The contents of R7 will be displayed.

<CNTRL> – The CNTRL key is always used in conjunction with some other key. When it is used it must be pressed and held down while the second key is pressed and released.

<CNTRL–HLT/SS> – Used to halt the processor.

1. Press and hold down the CNTRL key.
2. Press and release the HLT/SS key.
3. Display will show the current contents of R7 (program counter) and the RUN indicator will be off.
4. Release the CNTRL key.

If the processor is already halted, the use of the HLT/SS key will single-instruction step the processor. (The CNTRL key is not required to single-instruction step the processor once halted.)

1. Press and release the HLT/SS key.
2. Processor will perform one instruction and halt.
3. Display will show the new current contents of R7 (program counter).

<CNTRL–CONT> – Used to allow the processor to begin running from a halt.

1. Press and hold down the CNTRL key.
2. Press and release the CONT key.
3. Processor will run unless a program halt instruction is encountered. The RUN and SR DISP indicators should be on and the contents of the switch register should be displayed. If a halt instruction was encountered, the indicators will be off and the program counter will be displayed.
4. Release the CNTRL key.

NOTE

If the processor is already running, use of <CNTRL–CONT> will result in the switch register being displayed; there will be no other effect on the processor.

<CNTRL–BOOT> – Used to initiate running of M9301 Bootstrap program.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the BOOT key.
4. Processor should start running (RUN indicator on) the bootstrap program selected on the M9301.

NOTE

For more information concerning the M9301 Bootstrap program, consult the system users guide.

5. Release the CNTRL key.

<CNTRL–START> – Used to start the processor running a program from a given starting address.

1. Processor must be halted; otherwise key is ignored.
2. Press and hold down CNTRL key.
3. Press and release the START key.
4. RUN indicator will be on unless a halt instruction is encountered. The SR DISP indicator should also be on and the contents of the switch register should be displayed.
5. Release the CNTRL key.

To start running a program at location 1000, the following sequence is used:

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Press and hold down the CNTRL key.
5. Press and release the START key.
6. Release the CNTRL key.

<CNTRL–INIT> – Generates a Bus Initialize without the processor starting.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the INIT key.
4. Bus Initialize will be generated for 150 ms.
5. Release the CNTRL key.

<CNTRL-7> – Used to calculate the correct address when a mode 6 or 7 register R7 instruction is encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 7 key.
3. Display will show the new temporary register which contains the old temporary register plus the Unibus address point or plus 2.

See Paragraph 6.4 for an example.

<CNTRL-6> – Used to calculate the offset address when mode 6 or 7 instructions other than register R7 are encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 6 key.
3. Display shows the new temporary register, which contains the old temporary plus the switch register.
4. Release the CNTRL key.

See Paragraph 6.4 for an example.

<CNTRL-1> – Used to enter the console into maintenance mode. Maintenance mode should only be used as an aid to troubleshooting hardware problems. Maintenance mode provides no help in debugging software problems.

1. Press and hold down the CNTRL key.
2. Press and release the 1 key.
3. MAINT indicator will be on and the MPC (microprogram counter) will be sampled and displayed.
4. Release the CNTRL key.

6.3 NOTES ON OPERATION

An erroneous display will result if, while the processor is running and the switch register is being displayed, a numeric key is pressed. Although the SR DISP indicator will remain on, the display no longer reflects the actual contents of the switch register. If at any time while the processor is running, it is desired that the switch register contents be displayed, the CNTRL–CONT keys should be used.

As a general practice, prior to entering a new 6-digit number and if the display is nonzero, the CLR key should be used to initially zero the display.

In order to single-instruction step the processor from a given starting address, the program counter (R7) must be loaded with the starting address using the Unibus address of R7 (777707) i.e., to single-instruction step from the beginning of a program starting at location 1000, the following sequence is necessary:

```
LAD 777707
DEP 1000
CNTRL–INIT (if desired)
HLT/SS
HLT/SS
etc.
```

The console requires an 18-bit address. This is especially important to remember when accessing device registers (i.e., 777560 instead of 177560). Otherwise an erroneous access to memory or to a nonexistent address will occur.

The Unibus addresses for the general-purpose registers can only be used by the console. A PDP-11 program using the Unibus addresses for the general-purpose registers will trap as a nonexistent address. Also, internal registers R10 through R17, which are used for various purposes (depending upon processor), may be accessed by the console through Unibus addresses 777710 through 777717.

The BUS ERR indicator on the console reflects a bus error by the console only. The indicator will not reflect bus errors due to other devices such as the processor.

6.4 EXAMPLES OF CONSOLE SEQUENCES

This section combines key operations with example sequences to demonstrate the proper use of the KY11-LB Programmer's Console.

The following sequences use the notations for key operations as described in Paragraph 6.2.

The angle brackets < > will be used in the sequences to identify the display contents after the operation is performed, i.e., LAD 200 <0>

1. Press and release the CLR key.
2. Press and release 2 key.
3. Press and release 0 key.
4. Press and release 0 key.
5. Press and release the LAD key.
6. 000000 will be displayed in the 6-digit readout.

Example 1

This sequence uses the examine function and the switch register Unibus address 777570 to read the contents of the switch register.

LSR 123456	<123456>
LAD 777570	<0>
EXAM	<123456>
DIS AD	<777570>
LSR 777	<777>
EXAM	<777>

Example 2

This sequence demonstrates the use of the following keys: LAD, DIS AD, LSR, EXAM, DEP, CNTRL-START, CNTRL-CONT, and CNTRL-HLT/SS.

This example loads the following program into memory, which is then run to demonstrate various operations.

Program	Memory Location/Contents
1000/13737	;Move the contents of
1002/177570	the switch register to
1004/1014	memory location 1014
1006/0000	;Halt
1010/137	;Jump to location 1000
1012/1000	
1014/0000	

Sequence	
LAD 1000	<0>
DEP 13737	<13737>
DEP 177570	<177570>
DEP 1014	<1014>
DEP 0	<0>
DEP 137	<137>
DEP 1000	<1000>
DEP 0	<0>
LAD 1000	<0>
EXAM	<13737>
EXAM	<177570>
EXAM	<1014>
EXAM	<0>
EXAM	<137>
EXAM	<1000>
EXAM	<0>
DIS AD	<1014>
LSR 123456	<123456>
LAD 1000	<0>
CNTRL-START	<1010>
LAD 1014	<0>
EXAM	<123456>
DEP 0	<0>
EXAM	<0>
DIS AD	<1014>
LSR 125252	<125252>
CNTRL-CONT	<1010>
LAD 1014	<0>
EXAM	<125252>
DEP 0	<0>
LAD 1006	<0>
DEP 240	<240>
EXAM	<240>
LAD 1000	<0>
CNTRL-START	<125252>
LSR 70707	<10707>
CNTRL-HLT/SS	
LAD 1014	<0>
EXAM	<10707>
HLT/SS	
HLT/SS	
HLT/SS	
•	
•	
•	
LSR 05252	<052525>
HLT/SS	
LAD 1014	<0>
EXAM	<052525>

Example 3
This sequence demonstrates the use of CNTRL-7 and CNTRL-6. The following data are loaded into memory:

```
1000/177
1002/100
1004/000
1006/5060
1010/1020

1104/1006

RO = 777760
```

The sequence to load the data is as follows:

LAD 1000	<0>
DEP 177	<177>
DEP 100	<100>
DEP 0	<0>
DEP 5060	<5060>
DEP 1020	<1020>
LAD 1104	<0>
DEP 1006	<1006>
LAD 777700	<0>
DEP 777760	<777760>

Sequence

LAD 1000	<0>
EXAM	<177>
EXAM	<100>
CNTRL-7	<1104>
LAD	<0>
EXAM	<1006>
LAD	<0>
EXAM	<5060>
EXAM	<1020>
LSR	<1020>
LAD 777700	<0>
EXAM	<777760>
CNTRL-6	<100006>
LAD	<0>
EXAM	<177>

CHAPTER 7
MAINTENANCE MODE OPERATION

7.1 INTRODUCTION

This chapter covers the keypad facilities of the programmer's console available for hardware maintenance of the processor.

7.2 MAINTENANCE MODE KEY OPERATIONS

The following definitions apply to a subset of the same keys used in console mode; however the functions and operations differ from those in console mode. In general, console mode functions are not available while in maintenance mode, and many keys have no function in maintenance mode.

NOTE

Maintenance mode operation is indicated by the MAINT indicator being on.

In order to use the hardware maintenance features available in maintenance mode, the maintenance cable (11/04) or cables (11/34) must be connected between the KY11-LB interface board (M7859) and the corresponding processor board (M7263-11/04, M7266-11/34, M8266-11/34A, or M8267-TP11A). An exception to this is the 5 (maintenance mode) operation which allows the console to examine or deposit into memory or device registers without the processor being either present or functional.

DIS AD (Maintenance Mode) – Used to display Unibus address lines.

1. Press and release the DIS AD key.
2. Unibus address lines will be sampled (read once) and displayed, i.e., display will not be updated as address lines change.

EXAM (Maintenance Mode) – Used to display Unibus data lines.

1. Press and release the EXAM key.
2. Unibus data lines will be sampled and displayed.

HLT/SS (Maintenance Mode) – Asserts manual clock enable and displays MPC (microprogram counter).

1. Press and release the HLT/SS key.
2. Manual clock enable will be asserted.
3. MPC will be sampled and displayed.

CONT (Maintenance Mode) – Single microsteps the processor through one microstate and displays the MPC.

1. Press and release the CONT key.
2. Manual clock will be pulsed.
3. New MPC will be sampled and displayed.

BOOT (Maintenance Mode) – Boots the M9301. If manual clock enable is asserted, the M9301 routine will not be entered but because the M9301 simulates a power fail the processor will power up through location 24.

1. Press and release the BOOT key.
2. The display is not affected. If manual clock enable is asserted, the MPC is now at the beginning of the power-up sequence. To see the new MPC, use the HLT/SS key.

START (Maintenance Mode) – Drops manual clock enable.

1. Press and release the START key.
2. Manual clock enable is released.
3. MPC will be sampled and displayed.

CLR (Maintenance Mode) – Returns console to console mode operation.

1. Press and release the CLR key.
2. MAINT indicator is off.
3. Processor should halt.
4. Program counter should be displayed.

5 (Maintenance Mode) – Allows the console to take control of the Unibus if a processor is not in the system.

1. Press and release the 5 key.
2. The MAINT indicator will be off (console mode operation now).
3. Console attempts to read the program counter which is not present and therefore the BUS ERR indicator will be on.

7.3 NOTES ON OPERATION

If the single-microstep feature in maintenance mode is to be used, it is preferable that the processor be halted prior to entering maintenance mode, if it is possible. This is because the assertion of manual clock enable, which turns off the processor clock if it is running, cannot be synchronized with the processor clock. Therefore, if the processor is not halted, the clock may be running and the assertion of manual clock enable may cause an erroneous condition to occur.

In order to single-microstep the processor from the beginning of the power-up sequence, the following steps may be used:

1. Halt the processor if possible.
2. Use CNTRL 1 to enter maintenance mode.
3. Use HLT/SS to assert manual clock enable (RUN indicator should come on).
4. Use BOOT to generate a simulated power-fail (will not work if M9301 is not present in the system).

5. Use HLT/SS to display the MPC (microprogram counter) for the first microstep in the power-up routine.

6. Use CONT to single-microstep the processor through the power-up routine. (The new MPC will be displayed at each step.)

7. Unibus address lines and Unibus data (see NOTE below) lines may be examined at any microstep by using DIS AD and EXAM, respectively. Use of these keys does not advance the microprogram. To redisplay the current MPC without advancing the microprogram, use the HLT/SS key.

8. To return from maintenance mode, use the CLR key.

9. To single-microstep through a program, the program counter (R7) must first be loaded with the starting address of the program as in single-instruction stepping the processor prior to entering maintenance mode.

NOTE

Because the data transfer occurs asynchronously with the processor clock, Unibus data will not be displayed on DATI in maintenance mode when using the console with an 11/04 processor. Unibus data on DATO on the 11/04 and both DATI and DATO on the 11/34 will be displayed.

Due to hardware changes, the M8266 module will gate the AMUX lines onto the Unibus when manual clock enable is asserted and a Unibus transaction is not occurring.

CHAPTER 8
KY11-LB MAINTENANCE

8.1 PRELIMINARY CONSIDERATIONS

The following is a guide to locating possible problems on the KY11-LB.

1. Power Switch Failure – If the power switch fails to control the power supply, check cable 7011414-2-2 (BA11-L) at J2 or cable 7011992-0-0 (BA11-K) at Faston tabs TB4 and TB5 on the bezel-mounted board to ensure that cable(s) are securely and correctly installed.

2. If the power switch does turn on the power supply (fans turn) but the DC ON indicator does not come on, check cable 7011992-0-0 (BA11-K) at tabs TB6 and TB7 on the bezel-mounted board.

3. If the four indicators on the left side of the keypad are all on, then the cable 7012214-0-0 connecting the bezel-mounted board to the interface board (M7859) is probably plugged in backward on one end.

4. If no display and none of the four indicators are on, then check cable 7012214-0-0 at J1 on the bezel-mounted board and M7859 board to ensure that it is correctly and securely installed.

5. Note that there should be no cables from either the bezel-mounted board or the M7859 board attached to the backplane. The connection at the backplane is for use by the KY11-LA Operator Console only.

6. If the RUN indicator is on but there is no display and no response from the keypad, the problem is probably at the M7859 Interface module. Check the module to ensure that the microprocessor chip (E18) is securely installed in its socket.

7. If the display works and the console responds to the keypad except for the BOOT key, check that cable 7011413-0-0 is properly connected to the M9301 and to the bezel-mounted board at tabs TB1 and TB2.

8. If the display MPC, single microstep, etc. functions in maintenance mode do not work correctly, check that the cable(s) from J2 and J3 of the M7859 are properly installed.

NOTE

These cables should be installed only for maintenance of the processor. By disconnecting these cables for normal operation, the effect is that the maintenance functions are nonoperative except for the TAKE BUS function.

8.2 M7859 FAILURES

In general, there are two levels of possible failures on the M7859 module. The first level and most difficult to fix is the microprocessor and its support logic which constitutes about 1/3 of the logic. The second level is failures which occur in the peripheral logic constituting the Unibus interface and the display/keypad interface. These are generally easier to troubleshoot.

Generally, a first level failure is readily apparent and will usually be indicated when no display is on and the only indicators on are DC ON and RUN.

A second level failure, although easier to troubleshoot, is not always readily apparent as it may only occur on certain key functions or may be data dependent. A failure on the display/keypad interface would be indicated by odd displays, row, or column failures on the keypad. The Unibus interface can be tested with a good confidence level by loading the switch register with a 123456 data pattern and then reading it back over the Unibus by examining location 777570.

The following is a guide to troubleshooting a failing M7859 module. Generally, the minimum equipment needed is a dual-trace oscilloscope with delayed sweep.

1. Check that 9 V is available at pin 1 of the microprocessor, E18.

2. Check that the clock frequency is 1.0 MHz ± 2% at the test point, TP1. The frequency can be corrected if needed by adjusting the variable resistor at the top of the module.

3. Check that the two clock signals are at E18-15 and E18-16. These clocks should be 500 kHz frequency with nonoverlapping positive pulses of 0.5 ms duration (Figure 8-1).

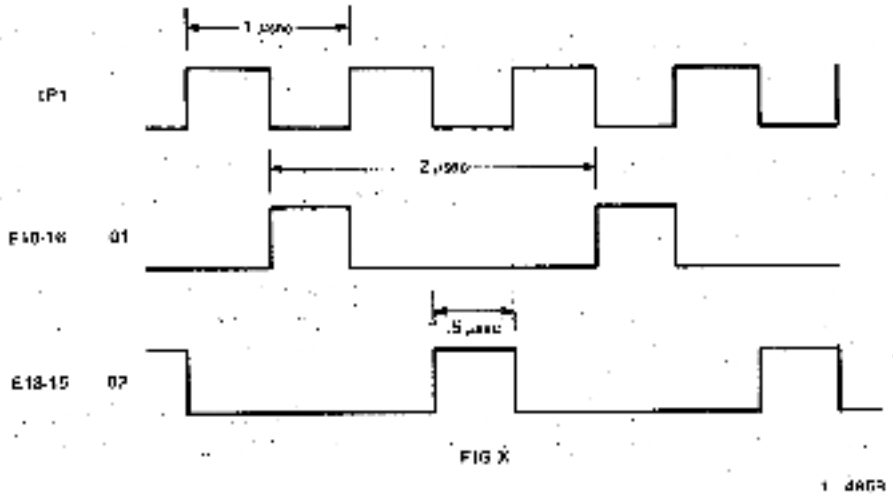

Figure 8-1 Clock Waveforms

4. Check the signal at E18-18 which should be at logic low. If the signal is high the microprocessor may not have responded to the interrupt request on power-up. If the signal is toggling, this may be indicative of a different class of problems discussed in the following paragraphs.

5. The M7859 logic is such that if the microprocessor encounters a HALT instruction and goes to the STOP state, peripheral logic will automatically try to restart the microprocessor from location 0. Hence, if there are problems in the microprocessor support logic, such as address or data failures, time state decoding failures, etc., the microprocessor will not follow the program and generally encounters a HALT instruction.

   The general technique to solve this class of problems is to sync off of the signal STOP L and to use delayed sweep to track addresses backward to find the specific failing address. A quick check of the number of times TS1 L is true between the times that STOP L is true will give an idea of how far into the program the failure occurs. In general the easiest technique is to use the TS3 L signal as a visual key on one channel while using the other channel to probe addresses, data, timing signals, etc.

CHAPTER 9
KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-connector cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.

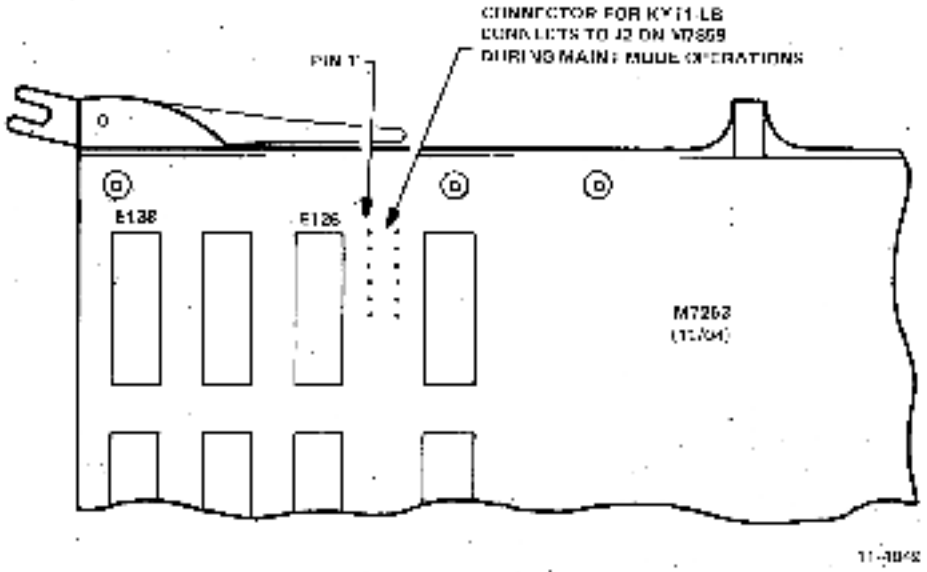

Figure 9-1 M7263

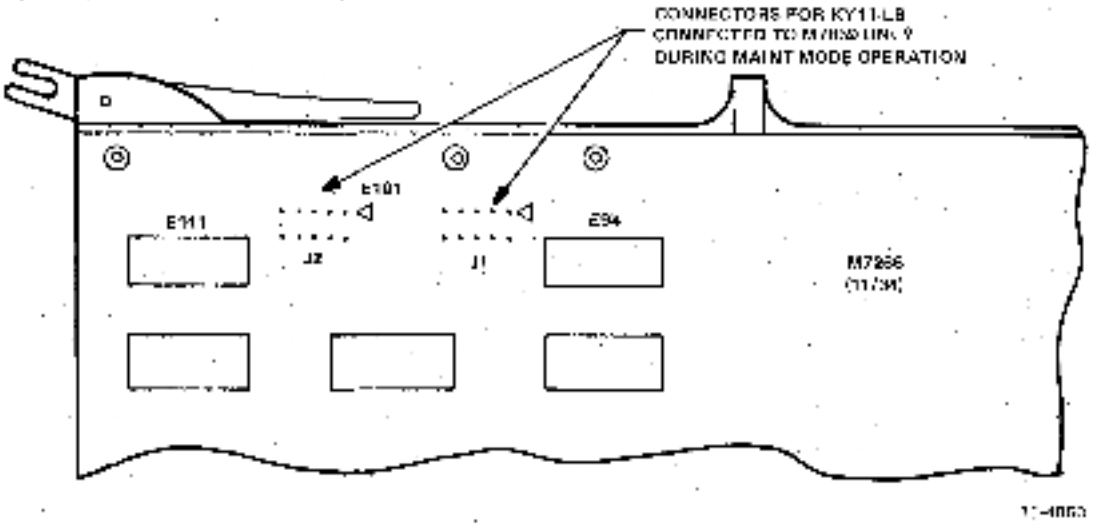

Figure 9-2 M7266

CHAPTER 9
KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-connector cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.

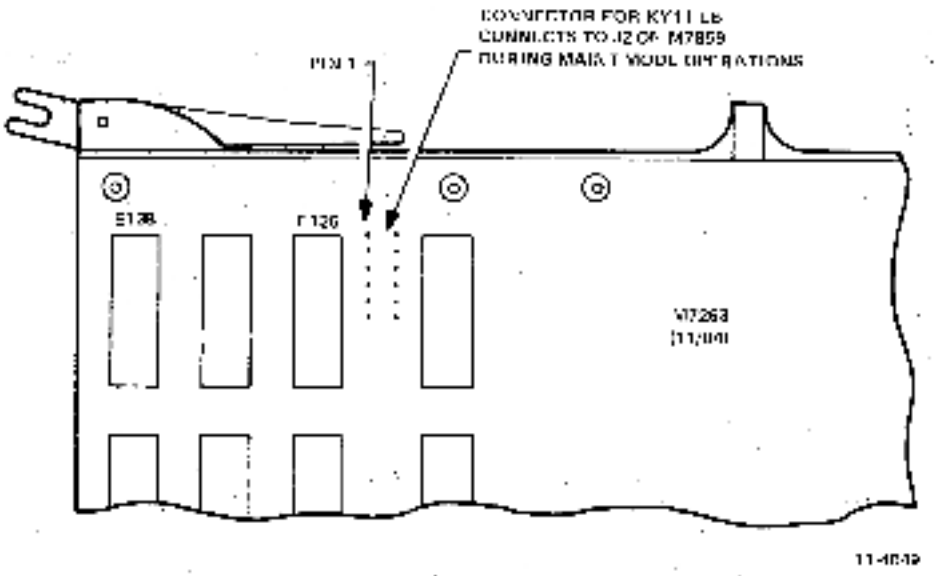

Figure 9-1 M7263

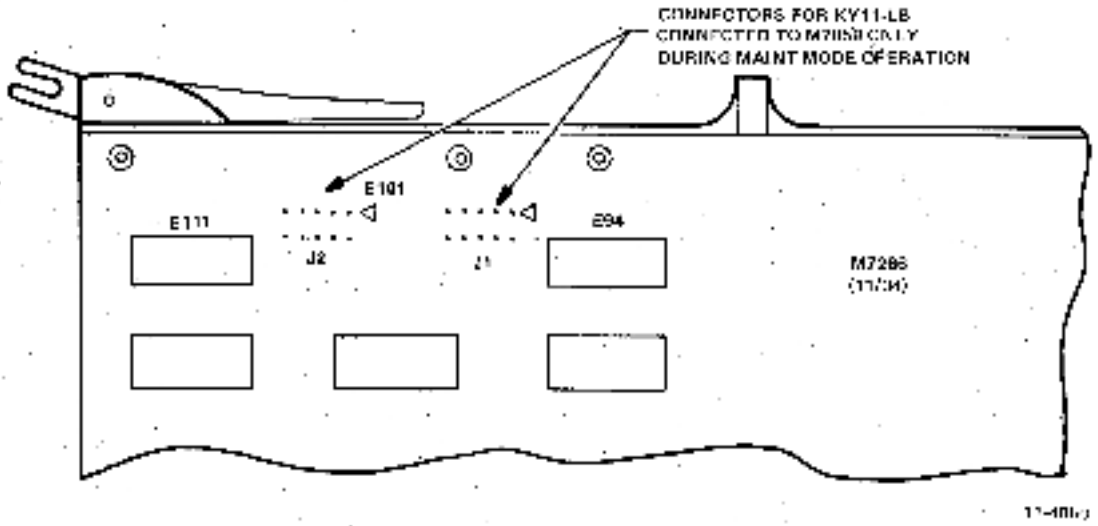

Figure 9-2 M7266

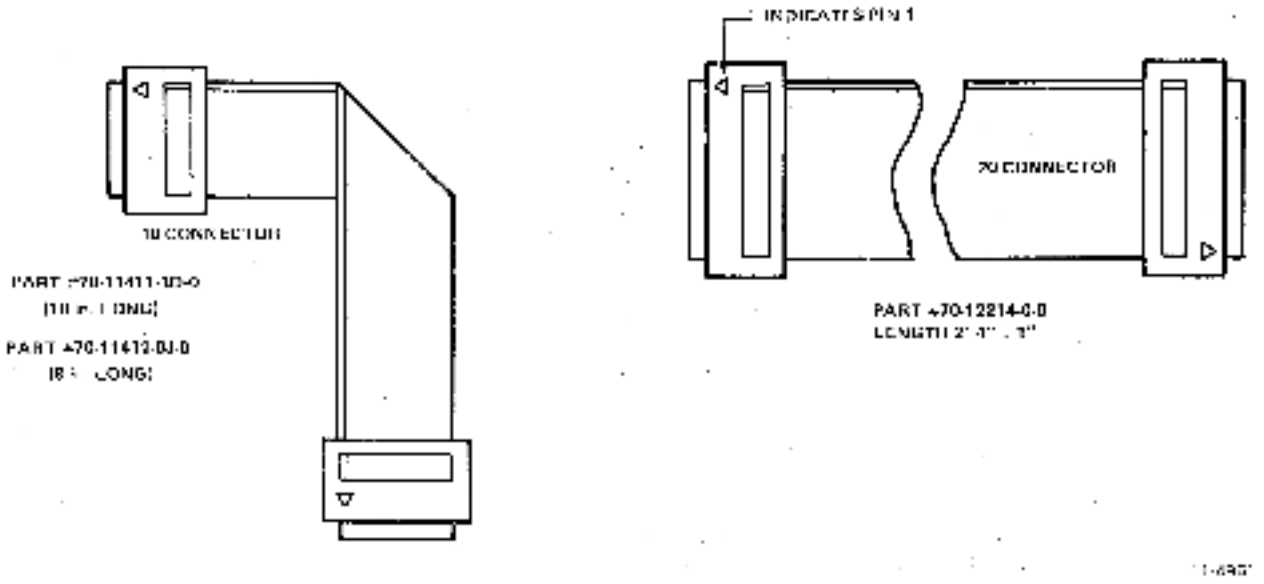

Figure 9-3 Cables

2. Install M7859 (KY11-LB interface) in any SPC slot (within CPU backplane) and connect it to the KY11-LB bezel as shown in Figure 9-4.

CONFIGURATION NOTE

The M7859 consumes 2A at +5 V and can only be plugged into the CPU backplane.

WARNING

When doing any reconfigurating of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

9.5 BA11-K 26.7 CM (10-1/2 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connection will be the same tabs on the KY11-LB (Figure 9-5). You will notice that J2 on the operator's console is not used on the BA11-K box. The signals and voltages that come in on this jack in the BA11-L box come in on Faston tabs in the BA11-K box. The cable connecting the CPU backplane to J1 on the operator's console must be removed and no connection from the backplane to the KY11-LB is made.

2. Install M7859 (KY11-LB interface) in any SPC slot (with CPU backplane) and connect to KY11-LB bezel as shown in Figure 9-5.

WARNING

When doing any reconfigurating of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

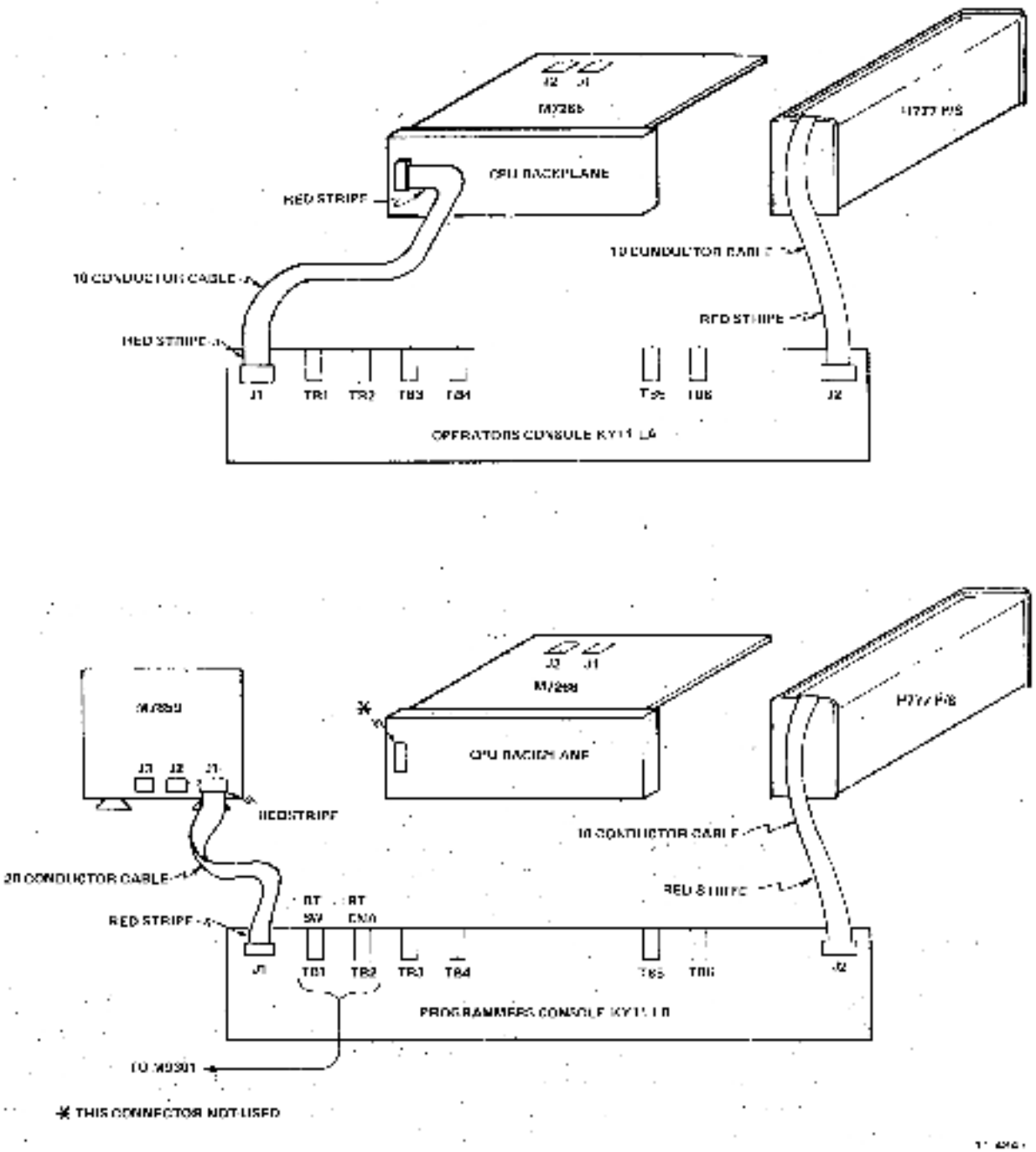

Figure 9-4 BA11-L

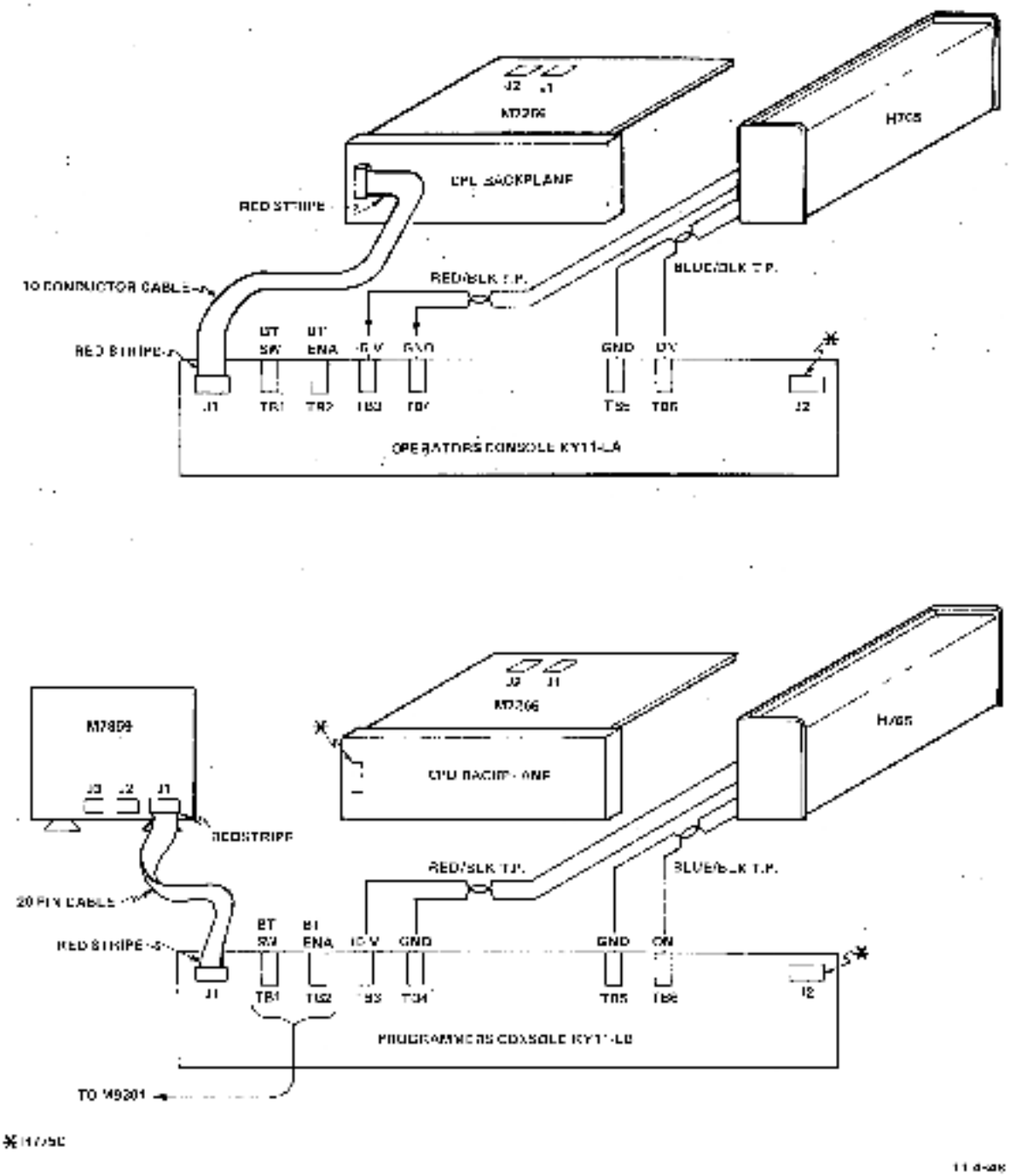

Figure 9-5 BA11-K

9.6 MAINTENANCE MODE HOOK-UP

To utilize the KY11-LB as a maintenance tool for troubleshooting the CPU or system, additional cable(s) must be installed. The 11/04 requires one additional cable and the 11/34 requires two additional cables.

PDP-11/04 (Maintenance Mode Cabling)

The 11/04 requires only one additional cable for maintenance mode operation. This 10-conductor cable (Part No. 70-11411-1D-0) connects J2 of the M7859 to the unmarked male connector on the M7263 (11/04 CPU). The cable (70-11411-1D-0) has a pointer on each end to indicate pin 1 as shown in Figure 9-3. Install the cable with the pointer on the end of the cable lined up with pin 1 on the CPU module (M7263). Pin 1 on M7263 is called out on Figure 9-1. Points on J2 (M7859) and the cable should also be lined up.

PDP-11/34 (Maintenance Mode Cabling)

The 11/34 requires two additional cables for maintenance mode operation. Both cables are the same and are the same part as is used on the 11/04. See Figure 9-3 for part number.

NOTE

Maintenance cables for both 11/04 and 11/34 are all 45.7 cm (18 inch) long, 10-conductor cables.

When installing maintenance cables connect J2 (M7859) to J1 (M7266) and J3 (M7859) to J2 (M7266). The pointers on the cable and board must be matched at both ends of the cables.

APPENDIX A
KY11-LB MICRO-CODE LISTINGS

```
KY1 1.0 'BCBRAN  07-1  V00.0 LN07-10    02-JAN25 PAGE 3

                 ASSEMBLY OF BCBR                    02/JAN/A          AT  1
2
KY1  .0 'BCBRAN  07-1  V00.0 LN07-10    02-JAN25 PAGE 7

5
KY1  .0 'BCBRAN  07-1  V00.0 LN07-10    02-JAN25 PAGE 8


2         000000          ;PROJECT
1         000000          ;-0
3                         ;I TLE 'CICLE PROGRAM
4         000000          CICLE
7         000401          BEGIN
8         000401          BEGIN2
9         000403          BEGIN3
10        000404          BEGIN4
11        000405          BEGIN5
12        000406          LIBRARY
13        000407          BEGIN7
14        000402          ERLAB1
2         000404          EXAMP2
15        000405          NUM1=BLANK
17        000403          NUM2=BLANK
18        000402          NUM3=BLANK
19        000401          NUM4=BLANK
20        000400          NUM5=BLANK
21        000000          ;-----
22        000000          ;BEGIN
23        000000          ;-----
24 000000         START   LST 10          INITIALIZE PL/I  G.
   000000    0 L
25 000003         P I S I   IO 240        PRINCIPLE REGISTER IO  0.ST IO GAP 240 AND TO SET
   000003    05F
   000002    240
26                                        PL/I 120 IO CHANL  ALLOCATE ADDRESS IN PRINTER
27                                        SIN PROGRAMMED HALT.
28 000007                   LLI 20        PRESET REGISTER IO  0.ST IO GAP.
   000006    0A1
   000004    02F
29 000F5                    SHI 0V.F
   000005    1A1
   000A      0 2
   000007    000
30 000010                   JMP DIG A
   000010    J01
   000J      001
   000012    000
31 000014         DIGAN   LEI 0           ZERO REG BYTE E.
   000013    01E
   000014    000
32 000015                   LR E            ZERO REGISTER A.
   000015    30A
33 000016         P RIT   LR A            ZERO MEMORY LOCATION ADDRESS POINTED TO BY REGISTERS H & L.
   000016    .10
34 000017                   BCT             JUMP BACK  0  TIMES.
   000017    0A1
35 000020                   JFE D'GA        JUMP BACK UNTIL RUN IS ALL ZERO DEC.
   000020    J2A
   000J      01E
   000021    000
36 000023         DISPIT  CAL  DISPIT       PULL DISP AT SUBROUTINE ADDRESS  & DISPLAY CHARACTER
   000023    12E
   000021    02J
   000025    000
<111 0:00 GAP  07-1  V00.0 LN07-10    02-JAN25 PAGE 9-
```

```
37
38 0037A                 JMP  SETUP      ;JUMP AROUND INTERRUPT ROUTINE
   0037B    12A                         ;INTERRUPT FLOW CHART
   0037C    175
   0037D    001
39                                      ;JUMP TO KEY & PRINT ROUTINE.
40
41
42 0037E          INTSUB                ;THIS IS SUBROUTINE.
   0037F    005
43                                      ;LOAD PORT, SIDE, AND REG THAT A AND B
44                                      ;FOR UNCONFIGURED HP    IN 82C55.
45 00380                 MVI  A,80      ;A PORT, C PORT SET AS OUTPUT PORTS FOR
   00381    044                         ;MODE 0.
   00382    080
46 00383                 OUT  PA        ;SET.
   00384    050
   00385    003
   00386    001
47 00387                 MVI  B,10      ;OTHERWISE, SET B=10 HEX FOR DELAY OF 16
   00388     16                         ;MILLISECONDS.
48 00389                 MVI  A,0       ;A=0 FOR TURNING OFF LED'S,
   0038A    03A
   0038B    000
49 0038C                 JMP  A,0       ;CLEAR FLIP-FLOP 1 IF EVENT FLIPFLOP IS
   0038D    05E                         ;SET.
   0038E    03A
                                        ;OFF THE ALL 8 OF PA0.
50 0038F                 OUT  PA        ;TURN ON ALL 8 PA0-7 ROUTINE.
   00390     04
   00391    0E7
   00392    010
51 00393          DELAY  JMP  A,0       ;ITERATION TO MAKE THE DELAY LONGER.
   00394    03A
   00395    000
52
                                        ;THIS SUBROUTINE CAUSES A 1 MILLISECOND DELAY FOR EACH COUNT IN
53 00396                 LXI  B,0       ;WHEN SET TO ZERO (SYSTEM IS 1.0 MICROSECOND PER CLOCK
   00397    001                         ;PERIOD).
54 00398                 MVI  A,00,     ;EXIT IF BIT WAS SET INDICATING TIMER = KEY WAS
   00399    03A                         ;PRESS OR RADIO HAS BEEN PUSHED.
   0039A    000
55 0039B                 DCX  B         ;DECREMENT REGISTER B AND C BY USED TO COUNT DOWN
   0039C    0B0
56 0039D                 JNZ  DELAY     ;IF NOT ZERO, DECREMENT A AND C BY USED TO COUNT DOWN
   0039E    03A
   0039F    001
57 003A0          DISPLY LXI  A,0       ;INITIALIZE REGISTER A = 0 = ZERO.
   003A1    07A
   003A2    000
58 003A3                 CALL DELAY     ;CALCULATE TIME DELAY OF THE DISPLAY.
   003A4     03
59 003A5                 LXI  B,0       ;CLEAR MEMORY PAIR REGISTER B TO ZERO
MCS-80  MACRO  V1.1  ASSEMBLY OF  MODULE  00113125 PAGE 3-
```

```
   00067A    030
A2
A2 00067                  LDA K             GET THE CONTENTS OF THE LOWEST 4 BITS OF A LOCATION IN RAM.
   00067    207
A4 00068                  ANI 7             MASK OFF THE LOWEST 3 BITS ONLY
   00069    047
   00071    007
A6 00072                  OUT DIS1          GO OUTPUT TO THE DISPLAY.
   00072    1A5
A8 00073                  LAI 0             SIGNAL TO ENTER 0 DIGITS INTO A REGISTER AND DISPLAY IT
   00074    203
AA 00075                  CAL MSIG          MSIG TURNS ON THE PROPER DIGIT ON THE DISPLAY.
   00076    12
AC                                           WHILE WAITING FOR INPUT FROM KEYPAD
AD                                           FOR A KEY PRESS (BIT).
AE 00078                  LAI 5             GO TO SUBROUTINE TO SCAN KEYPAD AND RETURN KEY
   00079    215
B0 00079                  KBD               SET A BIT TO TURN ON THE NEXT DIGIT.
   00079    042
B2 00080                  LBI A
   00081    320
B4 00082                  LBI 2             GET KEY BYTE, 5 WITH 1 2 TO PASS TO SHIFT
   00082    016
   00083    005
B6 00084                  CAL SHFT          SUBROUTINE TO SHIFT THE DISPLAY PATTERN
   00085    .06
   00086    A25
   00088    +00
BA                                           SPEED.DOWN.
BB 00089                  LBI 0             OUR RETURN FROM SHIFT SUBROUTINE. SAVE REGISTER
   00089    A02
BD 00090                  OUT 1             SAVE TO OUTPUT PORT 0 AND CHECK FOR A 1 TO SEE IF LAST
   00090    024
   00091    041
BF                                           DIGIT IS BEING ENTERED.
C1 00092                  JTZ DIS7 05       IF LAST DIGIT IS ENTERED GO DISPLAY AND JUMP OVER KEYPAD
   00092    E50
   00093    137
   00095    000
C6                                           SCAN ROUTINE.
C7 00096                  ADI 1             INCREASE BY ONE A 1 TO REGISTER F (CONTAINING ROW NUMBER)
   00096    004
   00097    001
C9 00098                  LBI A             SAVE NEW POINTER TO POINT TO KEYPAD INPUT
   00098    36A
CB                                           AREA 3 IN RAM.
CC 00099                   XS K 15          INPUT A 00 OPEN FROM THE KEYPAD AND
   00099    1E5
CE 00100                  NDI 7             MASK OUT UNWANTED BITS.
   00100    047
   00102    017
D0 00103                  JTZ DISP4         CHECK FOR NO KEYS DOWN (00) AND
   00104    150
   00106    10a
   00108    A00
D4 00109                  XS K              COMPARE CONTENTS OF THE PREVIOUS AND
   00109    2E7
NT LIB PROGRAM 'RT-1 MACRO V4.2-10    00:03:25 PAGE 10
```

```
                        JT2 DISP3       ; D DECISION THAT THE KEY AD IS STABLE.
    00125     C0
    00126     .32
    00127     000
                        INR E           ; INCREMENT REGISTER E BY THREE IF THE KEY IS OPEN (01).
    00130     040
                        IN E            ;CHECK NEXT PATTERN AND CONTINUE.  REGISTER E WILL
    0013A     040
                DISP3:  IN E            ;B. INCREMENT B BY ONE IF TWO ARE A MATCH.
    00132     046
                        INP KEYS        ;INPUT THE CODE OF KEYPAD MAIN AND
    00134     117
                        ANI 17          ;MASK FOR FOUR RIGHT BITS.
    00136     044
    00138     017
                DISP4:  A A             ;RETURN IN KEYPAD INDEX AREA OF RAM FOR NEXT TIME.
    00139     470
                DISP4A: DCR C           ;DECREMENT C BY ONE AND TEST
    0013B     021
                        JPZ DISP2       ;IF NOT ZERO JUMP BACK AND DISPLAY NEXT DIGIT.
    0013E     13A
    00140     072
    00141     004
                        LAI 0           ;IF ALL LIMITS HAVE BEEN DISPLAYED AND KEYPAD HAS
    00142     000
    00144     0F0
                        ORI 0F0H        ;THEN READ: LOAD REGISTER A WITH A FOR PROPER INPUT
    00146     .71
                                        ;TO TURN DISPLAY OFF.
                        LAI 0           ;READY PORT 1 (LED) WITH 0 TO BE PUSHED TO THE SHIFT
    00148     .
    0014A     010
    0014B     006
                        ORI 0H0         ;SUBROUTINE:  SIX PORT 1 BITS ARE RELOCATED TO
    0014D     10A
    0014F     28A
    00150     006
                                        ;FINISH SHIFTING AT 1 OF 6 NUMBER (BIT 1 DIGIT 6)
                                        ;FOUR BITS IN MEMORY IN THE RAM (4 WORDS).
                        LA              ;PUT THE CONTENTS OF REGISTER A AND CHECK
    00153     004
                        CPI 20H
    00154     074
    00156     200
                        JFZ DISP5       ;IF ANY NUMBER IS NOT EQUAL TO KEY NO LONGER DEPRESSED
    00159     15A
    0015B     00A
    0015C     000
                        LEI 0           ;IF NO KEYS ARE DEPRESSED, FLAG IS CLEARED.
    0015E     040
    0015F     000
                DISP5:  LM E            ; OTHER WISE, PUT A RIGHT M FOR ; OR A 0
    00160     006
                        LAI 1           ;A1 IF 2 KEYS ARE DEPRESSED AND AR. STABLE)
    00162     001
    00163     00
                        RTZ             ;RETURN IF FALSE TO MAIN PROGRAM A SLAVE SUBROUTINE TO SERVICE
    00164     007
MCS-8 MICRO PROGRAM ASSEMBLER (CPU-1  VERSION V02.01)  10/17/75 PAGE 3-4
```

```
0167                 CPI 2            ;[illegible]
0170       074
0170       007
0171                 RZ
017?       054
0172                 JMP DISP15       ;STAY IN DISPLAY SUBROUTINE
017?       104
0173       0??
0174       0?0

                                      ;KEY SERVICE ROUTINE.
                                      ;THIS ROUTINE DECODES THE CONSOLE MODE KEYS
                                      ;[illegible] ROUTINE [illegible]
                                      ;[illegible]
                                      ;[illegible] KEY.
0175           KEYSEV: MVI D          ;RESET REGISTER D TO ZERO.
0175       026
0176       000
0177                 LXI 20?          ;SET KEY[illegible] FLAG TO INDICATE THAT [illegible] HAS BEEN [illegible]
0?77       ???
0200       200
020?                 LXI ?            ;SET UP MEMORY POINTER TO THE KEYPAD IMAGE AREA.
020?       ???
020?       00?
020?                 LDA M            ;GET THE FIRST COLUMN OF KEYS FROM THE KEYPAD IMAGE
020?       ???
0204                 RAL              ;[illegible] ROTATE THE VALUE OF THE FIRST KEY IN THAT
0204       037
0205                 JTC DISPAD       ;COLUMN INTO THE CARRY BIT AND JUMP TO THE [illegible]
0205       140
020?       3??
0207       0??
0210                 RAL              ;ROUTINE FOR THAT KEY IF THE C BIT IS SET. OTHERWISE
0210       037
021?                 JTC [illegible]  ;[illegible] NEXT KEY AND SO ON UNTIL
021?       ?40
0212       ?0?
0213       0?0
0214                 RAL              ;THE WHOLE COLUMN HAS BEEN [illegible].
0214       037
0215                 JTC LER1
0215       140
0216       ???
0217       0?0
0220                 RAL
0220       037
0221                 JTC CLR1
0221       140
0222       327
0223       0?0
0224                 [illegible]      ;[illegible]
0224       06?
0225                 LDA M            ;MEMORY POINTER AND GET THE VALUES OF THE NEXT COLUMN
0225       307
0226                 RAL              ;OF KEYS FROM THE KEYPAD IMAGE AREA. DECODE THESE
0226       027
0227                 JTC [illegible]  ;[illegible]
[illegible]
```

```
     0229     49
     022a     c9
     022b     11
156  022c              RET
     022d     e2
172  022e              JPO L0B8
     022f     b8
     0230     01
     0231     01
178  0232              RET
     0233     e2
189  0234              JPO MJM1
     0235     40
     0236     03
     0237     e9
140  0238              RET
     0239     c9
141  023a              JPO PJM0
     023b     40
     023c     03
     023d     01
142  023e              MVI
     023f     e0
144  0240              LDA M
     0241     a7
145  0242              ANA
     0243     e2
146  0244              JPO LOAP1
     0245     40
     0246     17
     0247     00
146  0248              RET
     0249     c9
147  024a              JPO MJM1
     024b     40
     024c     03
     024d     01
148  024e              RET
     024f     c2
149  0250              JPO NJM0
     0251     40
     0252     03
     0253     00
150  0254              RET
     0255     c2
151  0256              JPO INIT1
     0257     40
     0258     11
     0259     10
152  025a              MVI
     025b     e0
157  025c              LDA M
     025d     a7
158  025e              RAR
     025f     e2
 65  0260              JPO LOP1
     0261     40
BY 1 0  M:JMP9   1 -1  1%0.1 %80/- 0    001(33) 1%0 11
```

```
     0274    070
     0275    001
1b6  0276            XAL
     0277    0b2
1b7  0278            JTC NUM6
     0279    ...
     0a00    07.
     0a01    017
1b  0a02            R'S
     0a03    0d2
1b9  0a04            .IC 'DP.
     0a05    140
     0a06    ...
     0a07    ...
1ba  0a08            JU              WHILE THAT LAST DIGIT KEY IS NOT RECORDED, H RE
     0a09    0a6
1b  0a0a            A 7             BECAUSE IT IS NOT A TERMINATION ACTION KEY, YET IS
     0a0b    a07
1bc  0a0c            RAR             ID= 'DIGITS'
     0a0d    083
1bd  0a0e            .IC 1,21
     0a0f    .40
     0a10    073
     0a11    010
1be  0a12            MA  .
     0a13    0d2
1bf  0a14            .IC CONT
     0a15    140
     0a16    ...
     0a17    017
1c0  0a18            RAR
     0a19    0a2
1c1  0a1a            .IC BUZ1
     0a1b    140
     0a1c    0d8
     0a1d    001
1c2  0a1e            XAL
     0a1f    0b0
1c3  0a20            JTC SIR1
     0a21    140
     0a22    150
     0a23    0.0
1c4  0a24            .EI 6           ; ( ALLOW 6 (NOT THE CONTROL KEY) TO BEEN DEPRESSED
     0a25    07e
     0a26    a0c
1c5  0a27            JIF DIGP1       ; (YES) ALL (OTHER KEYS (NOT DIGIT BECODED)  KEY(ERVICE)
     0a28    1d1
     0a29    ...
     0a2a    ...
1c6                                  ; (I AM NOT AT ALL SURE THAT A RECORDED KEY MAY BE
1c7                                  ; DECODED IN SUBROUTINE WITH THE CONTROL KEY.
1c8
1c9                                  ; SPECIFICATION :
1ca                                  ; THIS SUBROUTINE IS TO BE USED WITH THE DIGPLAY
1cb                                  ; CONTROL AREA OF THE RAM (FIGHT 5 EQUATIONS:
1cc                                  ; THE NUMBER OF BIT POSITIONS PASSED UNDER
1cd  P'0a0A'  R1=11 R2=0C 0x00  ;    DECIMAL MODE B+
```

```
 10                                     ;U TO DISPLAY R.
 11 0342          SHIFT   EQU     $
    0342    0046
    0343    0003
182 0344                    LA      3           ;S.T UP MEMORY TO READ 1 IN  R.G.T 3 LA .IGAIN MO.D
    0345    0006
    0346    0000
183 0347                    CAR                 ;LOOK FOR  ERO R A FIELD A NOT RIAT  T.T PAS.TH
    0348    0079
184 0349                    BC                  ;DARKY A T.
    034A    0041
185 034B            CAPTR1  LA      1           ;RECOVER THE MEMORY POINTER AND GET THE FIRST
    034C    0007
186 034D                    AR                  ;ADD 1 T.  GET NEX.
    034E    0079
187 034F                    IN A                ;STORE TH.S WORD BACK IN THE LOW 3 THE C BIT.
    0350    0076
188 0351                    BC                  ;BRANCH TO MEMORY THE OBJECT 0 VALUE.
    0352    0041
189 0353                    JFS SHIFT           ;RECOVER RD BRANCH POINTER TO NEXT WORD AND
    0354    0000
    0355    0342
    0356    0000
190 0357                    LI  1               ;R. THE TIME THROUGH BACK.
    0358    0001
    0359    0007
191 035A                    LA 5                ;FIND L.NE S  THE TIME  S FOUND CHAR. AND IF YOU IN THE
    035B    0005
192 035C                    MAR                 ;T.T  THE S THE 0 BL IN YOU OF THE  SIGNIFICANT WORD.
    035D    0079
193 035E                    RRC                 ;MEMORY POINTER .S READY TO VOLT SIGNIFICANT WORD.
    035F    0019
194 0360                    LA A                ;AND C BIT SA FIEL  INTO  B3.  THE WORD
    0361    0078
195 0362                    BT 8                ;IS THEN .MMATED TO PLY LED INTO MEM POSITION.
    0363    0043
196 0364                    BF2 SH.FT           ;END.T COUNTER IS DECREMENTED AND IF NON  RETURN
    0365    0342
    0366    0000
197 0367                    RET                 ;FROM SUBROUTINE.
    0368    0007
198
 99
200                                             ;ADDIC TEST SUBROUTINE.
201                                             ;THIS SUBROUTINE IS USED TO VERIFY THE
202                                             ;SERVICE ROUTINES TO CHECK IF THE CNTRL KEY
203                                             ;HAS BEEN DEPRESSED PRIOR TO SERVICING THOSE
204                                             ;KEYS WHICH REQUIRE THE CNTRL KE
205                                             ;TO BE U.
206 0369          KDIST1  LI  =               ;SET MEMORY POINTER TO KEYPAD IMAGE AREA AND
    036A    00A6
    036B    00A
207 036C                    LA M                ;GET WORD WHICH HAS THE VALUE OF THE CNTRL KEY.
    036D    0007
208 036E                    NI  10              ;IS  THIS THE CNTRL KEY AND  F NOT  RETURN.
    036F    0010
RTL V 1 PROGRAM  (C) 1  MACRO ASSEMBLER    04-15-75  08:51
```

```
     0372      010
     0372                          JTZ DISP1          /RETURN TO DISPLAY ROUTINE, OTHERWISE RETURN TO THE WHICH
     0372      150
     0373      123
     0374      000
     0375                          RET                /ROUTINE WHICH CALLED.
     0375      007



                                                      /NUMERIC ROUTINE.
                                                      /THIS ROUTINE GENERATES THE PROPER 4 BIT
                                                      /CODE WHEN ANY NUMERIC KEY IS DEPRESSED AND
                                                      /THEN SHIFTS IT INTO THE TEMPORARY AREA
                                                      /OF THE RAM.
     0376               NUMBX4    IN B                /INCREMENT THE B REGISTER THE CORRECT NUMBER
     0376      010
     0377               NUMBX3    IN B                /OF TIMES DEPENDING UPON THE NUMERIC KEY DEPRESSED
     0377      010
     0400               NUMBX2    IN B                /NOTE THE B REGISTER WAS CLEARED AT THE BEGINNING
     0400      010
     0401               NUMBX1    IN B                /OF THE KEY SCANNING ROUTINE.
     0401      010
     0402               NUMBX0    IN B
     0402      010
     0403               NUMBX-    IN B
     0403      010
     0404               NUMBX7    IN B
     0404      010
     0405               NUMBX8    LCI 1
     0405      076
     0406      004
     0407               NUMBX     LLI 30              /SET THE MEMORY POINTER TO THE TEMPORARY AREA IN THE RAM.
     0407      046
     0410      030
     0411                          LA M               /ROTATE THE THREE WORDS OF THE TEMPORARY AREA ONE
     0411      307
     0412                          RAL                /BIT AT A TIME, THE CARRY AROUND SO THAT ALL THREE WORDS
     0412      022
     0413                          LM A               /HAVE BEEN SHIFTED THREE TIMES.
     0413      370
     0414                          IN
     0414      060
     0415                          LA M
     0415      307
     0416                          RAL
     0416      022
     0417                          LM A
     0417      370
     0420                          IN L
     0420      060
     0421                          LA M
     0421      307
     0422                          RA
     0422      022
     0423                          LM A
     0423      370
     0424                          DC C
```

```
     0428    07
029  042A                LI  #0FH
     042B    110
     042C    007
     042D    00A
040  042E                LDI  0C          #LEAST SIGNIFICANT DIGIT TO LEAST SIGNIFICANT WORD.
     042F    00C
     0430    00C
041  0431                LDA  1           #GET THE ADDR ATTRIBUTE FOR THE LEAST THREE SIGNIFICANT
     0432    007
042  0433                ANI  0F0         #KEYS.
     0434    044
     0435    000
043  0436                ADD  3           #ADD IN THE THREE BIT DIGIT FROM SECTION M OF PAM
     0437    001
044  0438                LDA  0           #GET CHR IN MEMORY.
     0439    020
045  043A                ANI  0           #SEND DISPLAY INDICATIONS.
     043B    00A
     043C    000
046  043D                JZ   NEXA
     043E    135
047
048
049                                      #MOVE ROUTINE.
050                                      #THIS ROUTINE  IS USED TO MOVE THE TEMPORARY
051                                      #AREA IN THE RAM WHERE CHARACTERS IMAGE AREA OF
052                                      #THE RAM TO THE DISPLAY AREA OF THE RAM.
053  043F        MOVE:   LDI  0           #SET UP MEMORY POINTER TO TEMPORARY AREA IN RAM.
     0440    06a
     0441    010
054  0442        MOVE1:  LD   M           #READ THE FIRST THREE WORDS FROM RAM INTO ACCUMULATOR
     0443    017
055  0444                ANI  0           #B. C. AND D.
     0445    0a0
056  0446                JZ   *
     0447    207
057  0448                IN
     0449    160
058  044A                 B   *
     044B    209
059  044C                LDI  0           #RESET MEMORY POINTER TO THE DISPLAY AREA OF THE
     044D    04e
     044E    000
060  0450                LD   B           #RAM AND  ONE REGISTER  #, C, AND D FROM  THE MEMORY.
     0451    171
061  0452                IN   L
     0453    07f
062  0454                LD   C
     0455    173
063  0456                ANI  0
     0457    020
064  0458                JNZ  *
     0459    273
065  045A                LAP  0,0         #GO BACK TO DISPLAY ROUTINE.
     045B    130
     045C    023
MY LCD PROGRAM  RT-11 MACRO V05.00 to    30-OCT-85 PAGE 8-
```

```
                                ;EXIT ROUTINE.
                                ;THIS ROUTINE TURNS ON A.I.D. BUSY BIT
                                ;JUMPS TO SWITCH REG BYTE  DISPLAY ROUTINE.
0171 0162           PROEXIT:    CALL TIMER          ;CALL SUBROUTINE TO INCR LOCATR  BY 10 BEFORE EXIT.
     0163  10
     0164  2B
     0165  00
0173 0166                       CALL HLTBT          ;CALL SUBROUTINE TO INCR LOCATR BY 1 AND STORE IN MEMORY.
     0167  10
     0168  B2
     0169  00
0176 016A                       MVI A,20H           ;SET THE BUSY BIT IN A REGISTER TO TURN ON LEDS FOR PROGRAM
     016B  3E
     016C  20
                                ;EXIT.
017F 016D                       ORI 20H             ;SET THE BUSY BIT.
     016E  F6
     016F  20
0182 0170                       OUT REG
     0171  D3
0184 0172                       LXI B
     0173  0A
     0174  01
0187 0175                       DCR B               ;COUNT THE BUSY BIT.
     0176  05
018A 0177                       CALL TIMER          ;DELAY.
     0178  CD
     0179  03
     017A  01
                                ;
018D                            ;CLEAR BUSY BIT.
                                ;THE BUSY BIT IS USED TO SERVICE THE EXAM
                                ;KEY.
0190 017B           EXAM:       CALL DELAY
     017C  1E
     017D  A0
     017E  01
0193 017F                       ANI 11
     0180  E6
     0181  11
                                ;CHECK THAT PROGRAM IS DONE.
0198 0182                       CPI 0
     0183  FE
     0184  00
019B 0185                       JNZ EXAM            ;GET INPUT FROM SWITCHES AND CHECK IF
     0186  C2
     0187  7B
     0188  01
                                ;THE LOWER NIBBLE OF A IS ZERO IF ALL MEMORY
```

```
291 0328                    ORI 1 0x11      ;DI INC USED. CHECK TO SEE IF IT WAS 0,1 OR  NCREMENTED
    0329    46
    032A    174
    032B    011
292 032C                    CAL INCAD       ;BY USE 'GENERAL REGISTER' OR 'P' TAG.
    032D    186
    032E    10
    032F    03.
293 0330            EXPAND: CAL BAILD       ;LOAD THE ADDRESS POINTER (RAY) INTO THE FIELDS
    0330    185
    0331    144
    0332    70
294 0333                    T, *P           ;ADDRESS REGISTER.
    0333    146
    0334    0 C
295 0335                    A 1             ;MASK OFF THE TAG DATA BITS AND SET THE EXPANSION
    0335    307
296 0336                    XOI 3           ;COMP OF LOCATION 35.
    0336    014
    0337    003
297 0338                    ORI 200
    0338    064
    0339    200
298 033A                    LP A
    033A    020
299 033B                    CAL INTI.       ;CALL TO INTERPRET THE AND JUMP TO THE MOVE ROUTINE
    033B    00
    033C    240
    033D    03.
300 033E                    JMP MOVE        ;TO LOAD THE NEXT DATA.
    033E    104
    033F    045
    0340    001
301
302
303                                         ;NORMAL ADDRESS EVALUATION.
304                                         ;THE DOUBLE INCREMENTS THE CURRENT ADDRESS
305                                         ;POINTER IN THE  RAY BY  1.
306 0341            INCRAD: LLI 15          ;SAVE A 1 IN THE LEAST SIGNIFICANT BIT.
    0341    064
    0342    015
307 0343                    LA 0            ;GET  L UNIQUE ADDRESS POINTER FROM TAG
    0343    007
308 0344                    AI 1            ;AND THEN 'ADD THE SAVED 1' INTO THE NEXT TAG
    0344    074
    0345    01
309 0346                    LA P            ;REMOVE THE TAG BITS IN THE LAST ADDRESS
    0346    170
310 0347                    IN              ;PUT THIS INCREMENTED ADDRESS.
    0347    166
311 0348                    JAL 6
    0348    106
    0349    006
312 034A                    AC 4
    034A    044
313 034B                    JM 4
    034B    374
WHILE PROGRAM  R1 = 1 MEMORY WORD =  0    0011212 PAGE 11
```

```
314 0564               ML
    0564    060
315 0565               LAI 0
    0565    006
    0566    000
316 0567               AD H
    0567    202
317 0570               NDI 3
    0570    044
    0571    003
318 0572               LK A
    0572    370
319 0573               RET
    0573    007
320
321
322                                     ;GENERAL REGISTER TEST SUBROUTINE.
323                                     ;THIS SUBROUTINE TESTS THE UNIBUS ADDRESS
324                                     ;POINTER TO SEE IF IT IS IN THE RANGE OF
325                                     ;GENERAL PURPOSE ADDRESSES 177700-177717.
326                                     ;IF IT IS NOT A GENERAL REGISTER ADDRESS
327                                     ;THEN THIS SUBROUTINE WILL INCREMENT THE
328                                     ;ADDRESS BY ONE-IF IT IS IN THE RANGE IT
329                                     ;WILL NOT INCREMENT AT ALL.
330 0574         GRTST LA M
    0574    307
331 0575               NDI 2
    0575    044
    0576    002
332 0577               CPI 2            ;ARE ADDRESS BITS 17 AND 16 ONES?
    0577    074
    0600    002
333 0601               JFZ GRTST        ;NO.
    0601    110
    0602    214
    0603    001
334 0604               DC L             ;YES.
    0604    061
335 0605               LA M
    0605    307
336 0606               CPI 377          ;ARE ADDRESS BITS 15 THRU 8 ONES?
    0606    074
    0607    377
337 0610               JFZ GRTST        ;NO.
    0610    110
    0611    214
    0612    001
338 0613               DC L             ;YES.
    0613    061
339 0614               LA M
    0614    307
340 0615               NDI 300          ;ARE ADDRESS BITS 7 AND 6 ONES AND
    0616    044
    0617    300
341 0620               CPI 300          ;BITS 5 AND 4 ZEROES?
    0621    074
    0622    300
KY11 LB PROGRAM  V01-10 MACRO VM03-10    03:13:25 PAGE 54
```

```
342 0627                JIZ SPRI3       ;YES.
    0627    150
    0628    207
    0629    001
343 062A        GPRI2:  DAL INLAB       ;NO. INCREMENT ADDRESS BY ONE.
    062A    106
    062B    151
    062C    001
344 062D        GPRI3:  LAT
    062D    007
345
346
347                                     ;DATI SUBROUTINE.
348                                     ;THIS SUBROUTINE PERFORMS A DATI ON THE
349                                     ;UNIBUS ADDRESS POINTED TO BY THE UNIBUS ADDRESS
350                                     ;REGISTER.THE RECEIVED DATA IS STORED INTO
351                                     ;THE TEMPORARY AREA IN RAM.
352 062E        DATI:   LAI 10          ;SET UP MEMORY POINTER TO TEMPORARY.
    062E    000
    062F    010
353 0630                LA  10          ;SET MUS MSYN BIT.
    0630    006
    0631    0 0
354 0632                DAT  (0)
    0632    172
355 0633                INP  (0)        ;READ BUS DATA WITH ALL ZEROS
    0633    1 3
356 0634                NOI 20
    0634    044
    0635    020
357 0636        .       JIZ MUSERR      ;NO. RETURN SUS  ERROR.
    0636    150
    0637    257
    0638    001
358 0639        DATI2:  INP BDLB        ;YES. PUT LOW BYTE OF UNIBUS DATA
    0639    101
359 063A                LM ^            ;STORE AND STORE IN MEMORY.
    063A    370
360 063B                IN 1
    063B    060
361 063C                INP BDHB        ;GET HIGH BYTE OF UNIBUS DATA AND
    063C    103
362 063D                LM ^            ;RETURN IN MEMORY.
    063D    370
363 063E                IN 1
    063E    060
364 063F                LAI 0
    063F    000
    0640    000
365 0641                LM ^            ;ZERO LOW WORD OF TEMPORARY.
    0641    370
366 0642                OUT PORT        ;CLEAR MUS MSYN BIT.
    0642    126
367 0643                OUT REG2        ;PUT UNIBUS ADDRESS LINES.
    0643    012
368 0644                RET
    0644    007
KY1 FB TIBUNAM  V1-11 MACRO VM02-10   001.2125 PAGE 8+
```

```
369
370
371                                     ;FUNCTION: ERROR SUBROUTINE.
372                                     ;THIS SUBROUTINE SETS THE BLG ERROR
373                                     ; INDICATOR AND TERMINATES THE UNIBUS TRANSACTION.
374 0657         ERR:    PUSH ST(1,A1 20
    0657    005
    0658    020
375 065a                 MOV R,R6       ;SET BUS ERROR INDICATOR.
    065b    135
376 065c                  AI  0
    065c    006
    065d    000
377 065e                 JN: RESET      ;DROP BUS MSYN.
    065e    132
378 065f                 MOV DROP       ;DROP UNIBUS ADDRESS LINES.
    065f    122
379 0660                 JMP CLR2       ;GO TO CLEAR THE DISPLAY.
    0660    104
    0661    032
    0662    000
380
381
382                                     ;DEPOSIT SUBROUTINE.
383                                     ;THIS ROUTINE SERVICES THE DEPOSIT KEY.
384 0663         DEP:    CAL HITS1      ;CHECK FOR PROCESSOR HALT.
    0663    104
    0664    001
    0665    000
385 0666                 AI 0
    0666    006
    0667    000
386 0668                 MOV REG        ;CLEAR THE INDICATORS.
    0668    135
387 0669                 LOC 15         ;SET UP ADDRESS POINTER AND CHECK DEPOSIT FLAG.
    0669    066
    066a    015
388 066b                 LA P
    066b    207
389 066c                 NEI 100        ;FIRST DEPOSIT?
    066c    014
    066d    100
390 066e                 JMP LOOP       ;YES.
    066e    110
    066f    131
    0670    001
391 0671                 OP. G+R1       ;NO. CHECK FOR OVERFLOW REGISTER.
    0671    104
    0672    241
    0673    001
392 0674                 OP. INCR0      ;INCR ADDR BUS POINTER.
    0674    104
    0675    151
    0676    001
393 0677         DEP1:   LA N
    0677    307
394 0678                 OMI 10         ;SET THE BUS C1 BIT (IN RAM) TO DO A DATO.
PAGE 8 (DEPOSIT)  MICRO VAX-U    04-SEP-85 15:00:00
```

```
                                                                                
     07.A    014
     07..    010
395  0720            LW A
     0720    370
396  0721            CAL BADLD       ;LOAD UP UNIBUS ADDRESS REGISTER.
     072.    106
     0722    344
     0723    001
397  0724            LIT 15
     0724    066
     0725    015
398  0726            LA M
     0726    307
399  0727            NOT 3
     0727    044
     0730    003
400  0731            DRI 100         ;SET THE DEVICE'S LOAD.
     0731    064
     0732    100
401  0733            LM A
     0733    370
402  0734            .LLI 10         ;RESET MEMORY POINTER TO TEMPORARY AREA OF RAM.
     0734    026
     0735    010
403  0736            CAL DATO1       ;CALL THE DATO SUBROUTINE USING THE TEMPORARY AREA
     0736     06
     0737    361
     0740    001
404  0741            JMP REVI        ;GO DATA- DISPLAY TEMPORARY AREA.
     0741    104
     0742    042
     0743    001
405
406
407                                 ;UNIBUS ADDRESS REGISTER LOAD SUBROUTINE.
408                                 ;THIS SUBROUTINE LOADS THE UNIBUS ADDRESS
409                                 ;POINTER FROM RAM INTO THE UNIBUS ADDRESS
410                                 ;REGISTER AND ENABLES THE REGISTER ONTO
411                                 ;THE UNIBUS.
412  0744       BADLD:  LWI 13      ;SET UP MEMORY POINTER TO UNIBUS ADDRESS POINTER.
     0744    066
     0745    013
413  0746            LA M
     0746    307
414  0747            OUT 3600        ;MOVE FIRST WORD TO UNIBUS ADDRESS REGISTER.
     0747    124
415  0750            IN L
     0750    006
416  0751            LA M
     0751    307
417  0752            OUT REG1        ;MOVE NEXT WORD TO REGISTER.
     0752    122
418  0753            IN H
     0753    060
419  0754            LA A
     0754    307
420  0755            ORI 4           ;SET THE ENABLE BIT.
MY11LN PDP11RAM  V1-11 MACRO VM02-10   20-JAN-82 PAGE 8+
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```
     0755    084
     0756    094
420  0757            OUT R'G2        ;LOAD LAST PART OF REGISTER.
     0757    122
422  0758            RET
     0759    087
423
424
425                                 ;-----------------
426                                 ;THIS SUBROUTINE PERFORMS THE DATE
427                                 ;READ/WRITE, TOD DISPLAY AND START KEY FUNCTIONS.
428  075A      DATIO  EQU $         ;NOTE - MUST LOAD FROM MEMORY(FROM TEMPORARY OR DEPOSITE
     075A    307
429  075B            OLY ERLE        ;AND INDEXED ADDRESS POINTER ON START) AND LOAD
     075B     97
430  075C            IN L            ;LOW BYTE OF BUFFER REGISTER.
     075D    0e3
431  075E            LA H            ;GET SECOND WORD OF DATA AND LOAD INTO
     075E    307
432  0760            DCI =0HF        ;FIND IF I/O SWITCH LOOP.
     0761    121
433  0762            LA 4'           ;SET BIT TO ENABLE SWITCH REGISTER INTO
     0763    0f6
     0764    004
434  0765            OUT DEV         ;I/O CONTROL.
     0765    .23
435  0767            LI 14
     0767    034
     0768    014
436  0769            OUT REG5        ;POWER) SUPPLY.
     0769    153
437  076A            INP REG5        ;FIND STATUS OF FLAGS
     076A    172
438  076B            ANP ME42        ;JUMP OVER NON MEMORY BOUNDARY.
     076C    104
     076D    000
     076E    010
439  1000            NOP
     1000    000
440  1001    REPEAT  XOI 00
     1001    044
     1002    020
441  1003            JTZ OLDER       ;NO.
     1003    140
     1004    057
     1005    001
442  1006             AI A           ;YES.
     1006    006
     1007    004
443  1010            OUT REG5        ;DROP BUS METH.
     1010    133
444  1011             AI 0
     1011    006
     1012    000
445  1013            OUT PORT5       ;DROP THE SWITCH REGISTER ENABLE.
     1013    155
446  1014            OUT REG2        ;TO AS THE WINDOW ALLOWING REGISTER AND PANEL
TOTAL PROGRAM: R1 - 1 HEXRD UP02-10    ASSEMBLY TAKEN IT
```

```
     1014     1[illegible]
     1015                         OUT REG        ;[illegible] THE UNIBUS.
     1015     1[illegible]
     1016                         OUT REG0
     1016     121
     1017                         CAL [illegible]       ;CALL ROUTINE TO [illegible] THE CONTENTS OF SWITCH REGISTER.
     1017     1[illegible]
     1020     [illegible]
     1021     [illegible]
     1022                         RET
     1022     007


                                                 ;HALT ROUTINE.
                                                 ;THIS ROUTINE SERVICES THE HALT/SINGLE STEP
                                                 ;KEY FUNCTION AND ALSO SERVICES A PROGRAM
                                                 ;HALT BY THE PROCESSOR.
     1023              HLT1:      INP REG3
     1023     113
     1024                         NDI 40         ;IS PROCESSOR ALREADY HALTED?
     1024     044
     1025     040
     1026                         J[illegible]Z SS1        ;YES, DO SINGLE STEP FUNCTION.
     1026     110
     1027     034
     1030     010
     1031                         CAL NOTST      ;NO, IS CNTRL KEY 0 PRESSED?
     1031     106
     1032     365
     1033     000
     1034              SS1:       LA  41         ;YES SET HALT REQUEST AND CLEAR BUS BITS.IF PROCESSOR
     1034     006
     1035     041
     1035                         OUT REG3       ;IS HALTED IT WILL PROCEED ONE INSTRUCTION.
     1035     133
     1037              HLT15:     LA  1          ;[illegible] THE CLEAR BUS BIT.
     1037     006
     1040     001
     1041                         OUT REG3
     1041     133
     1042              HLT2:      LC  0          ;SET UP A TIMING LOOP TO WAIT FOR HALT
     1042     026
     1043     000
     1044                         LB  12         ;GRANTS IN CASE PROCESSOR IS DOING A RESET.
     1044     016
     1045     012
     1045              HLT25:     INP REG3
     1045     113
     1047                         ND  40         ;HALT GRANT RECEIVED?
     1047     044
     1050     040
     1051                         JTZ HLT3       ;YES.
     1051     110
     1052     067
     1053     010
     1054                         [illegible]            ;[illegible] COUNT.
     1054     02[illegible]
KY[illegible] PROGRAM  [illegible] MAC[illegible] JAN02-1[illegible]  [illegible]:13:25 PAGE 8[illegible]
```

```
427 1045                        JMP WAIT2       ;DONE COUNTING.
    1047    1 0
    1048    04e
    1049    019
427 1050                        DEC R0          ;DECREMENT COUNTER.
    1050    011
429 1051                        JMP PLT23       ;TIMED OUT? NO.
    1053    110
    1054    046
    1055    019
474 1056                        JMP RUBBER      ;YES, GO TO BUS ERROR ROUTINE.
    1056    .09
    1057    '07
    1058    001
475 1059            LIB         CAL #           ;RESOLVED GRANT,NOW CLEAR INDICATORS.
    1059    006
    1070    000
476 1071                        CLT RECA
    1071    137
477 1072                        MOV #.007       ;LOAD UNIBUS ADDRESS OF PC (R7: 777707)
    1072    006
    1073    007
478 1074                        CLT RESD        ;INIT THE UNIBUS ADDRESS REGISTER AND
    1074    121
479 1075                        CAL 777         ;ENABLE CNTL THE UNIBUS.
    1075    006
    1076    377
480 1077                        CLT REG
    1077    122
481 1100                        CAL 7
    1100    006
    1101    007
482 1102                        CLT REG2
    1102    122
483 1103                        CAL DAT 1       ;CALL THE DATI SUBROUTINE.
    1103    197
    1104    270
    1105    001
484 1106                        JMP MOVI        ;DISPLAY THE 7.
    1106    101
    1107    042
    1110    001
485
486
487                                             ;INIT KEY SERVICE ROUTINE.
488                                             ;THIS ROUTINE PROVIDES THE INIT KEY
489                                             ;FUNCTION.
490 1111            INIT 1      CAL #INTX       ;BLOCK UNTIL INTRL KEY HAS BEEN DEPRESSED AND
    1111    .08
    1112    305
    1113    000
491 1114                        CAL #LTST       ;THAT THE PROCESSOR IS HALTED.
    1114    105
    1115    252
    1116    010
492 1117                        CAL INITX       ;CALL THE INITIALIZE SUBROUTINE.
    1117    100
KY11 D *B(1)PAR  M 11 MACRO VM02-10    00:33:23 PAGE 81
```

```
     1129    140
     1121    010
495  1123                    IA  1           ;SAVE THE BUS 'BI' BIT AGAINST UP NEXT REQUEST
     1122    004
     1124    00
496  1 24                    OUT REQ7        ;BIT SET.
     1 24    133
495  1 25                    JMP BUSY1
     1 26    104
     1 26    128
     1 27    000
496
497
498                                          ;INIT BUSY SUBROUTINE.
499                                          ;THIS SUBROUTINE SETS THE BUS INIT
500                                          ;B.T FOR 150 MILLISECONDS. THIS IS USED
501                                          ;BY THE START AND INIT KEY FUNCTIONS.
502  1150        INITX1  LAI 3
     1150    00a
     1151    004
503  1152                OLI REWL            ;SET BIT 'BI' IN INIT AND INIT MOMENT BUS.
     1152     35
504  1154        TIMER1  LAI 12              ;SET UP COUNTER TO A 150 MILLISECOND DELAY.
     1154    014
     1154    012
505  1156                LCI 0
     1157    006
     1159    000
506  1159        INITX2: DS 0                ;DECREMENT COUNTER AND BRANCH UNTIL ZERO.
     1159    021
507  1160                JFZ INITX2
     1160    1 0
     1161    159
     1162    010
508  1163                DS 3
     1163    011
509  1164                JFZ INITX2
     1164    110
     1165    159
     1166    010
510  1167                RET
     1167    007
511
512
513                                          ;START KEY SUBR.
514                                          ;THIS ROUTINE SERVICES THE START K.F. FUNCTION
515                                          ;BY LOADING THE PC (R7) WITH THE LNIBUS
516                                          ;ADDRESS POINTING TO INITIATING BUS INIT, AND
517                                          ;ALLOWING THE PROCESSOR TO CONTINUE.
518  1150        START1  CAL RESET           ;RESET THAT CNTRL KEY IS DEPRESSED AND
     1150    106
     1151    3e5
     1152    000
519  1152                CAL WAIT            ;THAT PROCESSOR IS HALTED.
     1152    106
     1154    3a2
     1155    010
KY11B PROGRAM  (7-1) MACRO VNC2-10    30-DEC-75 PAGE 8-4
```

```
                        LAI 240         ;DISABLE INTERRUPTS FROM ALL PIOs (204).
                        OUT 3E3         ;DISABLE ACCUMULATOR BY SETTING ALL BITS
                        LAI 3F          ;
                        OUT 3E3         ;DISABLE ACCUMULATOR INPUT LATCH.
                        LAI 3F
                        OUT 3E1
                        LA  17          ;SET THE ENABLE BIT (4) AND THE
                        OUT 3E2         ;BUS CLEAR BIT (5).
                        LXI H           ;SET THE MEMORY POINTER TO CONTROL ADDRESS OF PIO#1
                        CA  DATA1       ;AND LOAD IT WITH DATA SUBROUTINE.
                        CA  INITX       ;CALL THE INITIALIZE SUBROUTINE TO SET PIO#1
                        LAI 2           ;BUS INITIALIZE.
                        OUT R:05        ;ONLY THIS BIT AND HALT BIT SET ON
                        LAI 0           ;CLEAR BIT, THEN SET BUS CLEAR BIT.
                        OUT R:05
                        JMP 0:0 EP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
;
;
;                                       ;CONTINUE ROUTINE.
;                                       ;WHILE ROUTINE SERVICES THE CONTROL KEY FUNCTION,
;                       CONTIN:  CAL RL:01      ;CHECK IF THE CONTROL KEY IS DEPRESSED.
                        LHI 240         ;RESET PROGRAMMED HALT FLIP.
                        LHI 10          ;SET THE BUS CLEAR BIT TO ALLOW PROCESSOR
;
TITLE PROGRAM  RT-11 MACRO V02  0    06-JAN-82 PAGE 8T
```

```
542 1235                    OUT REGS        ;IO CONTINUE, & TYPE 'PROCEED' IF ALREADY
    1237    1A7
543 1238                     AI 0           ;USING AC THIS WILL HAVE NO EFFECT.
    1239    006
    123A    000
544  123C                   HLT 0/05
    123C    03C
545  123D                   JMP SLDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    123E     04
    123F    0e1
    1240    014
546
547
548                                         ;LOAD SWITCH REGISTER ROUTINE.
549                                         ;THIS ROUTINE ALLOWS THE USE OF SWITCH
550                                         ;REGISTER TEMPORARY AREA (PAGE 13) AS A
551                                         ;BUFFER AREA WHEN THEN LOADS THE SWITCH
552                                         ;REGISTER AND SETS ER FOR 'PROCEED' INDICATION.
553 1241          LDR1:   LUI 13            ;SET MEMORY POINTER TO TEMPORARY AREA AND
    1241    07A
    1242    010
554 1243                    LI H            ;PAGE 13 (WORK) TO REGISTERS A AND B.
    1243    017
555 1244                    IX L
    1244    0a0
556 1245                    LI P
    1245    017
557 1246                    LUI 14          ;SET UP TEMP POINTER TO SWITCH REGISTER
    1246    0aA
    1247    01A
560  1248                   LW P            ;PHASE WORK AREA CONTENTS FROM REGISTERS
    1248    07C
561  1249                   LW              ;TO AND B.
    1249    040
562  124A                   LM 0
    124A    007
563 124B                    CAL CALD        ;CALL THE 'F' LOAD SUBROUTINE, AND
    124B     0a
    124C    010
    124D    014
564 124E                   JMP SLDISP       ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    124E     04
    124F    0A1
    1250    010
565
566
567                                         ;'F' LOAD SUBROUTINE.
568                                         ;THIS SUBROUTINE LOADS THE SWITCH REGISTER
569                                         ;WITH THE CONTENTS OF THE SWITCH REGISTER
570                                         ;TEMPORARY AREA. A RETURN SUBROUTINE JUMP IS USED
571                                         ;BY THE LOAD SWITCH REGISTER ROUTINE AND
572                                         ;AN ILLEGAL CALL TO RESTORE THE SWITCH REGISTER.
573 1251          SRLD:   LUI 16            ;SET MEMORY POINTER TO SWITCH REGISTER PAGE AND A
    1251    0aA
    1252    016
574 1253                    LP M            ;AND LOAD THE LOW BYTE OF THE SWITCH REGISTER
    1253    017
577  8 PROGRAM  (7-1) VAX-8 VM03-10    #01-MAR-85 PAGE 9+
```

```
523 1253                LA R            ;WITH THE FIRST WORD.
    1253    241
524 1254                OUT SR:0
    1254    127
525 1255                IN L
    1255    030
526 1256                LA R            ;LOAD THE LOW BYTE OF THE BUFFER ADDRESS
    1256    207
527 1257                OUT SR+1        ;WITH THE NEXT WORD FROM MEMORY.
    1257    131
528 1259                RET
    1259    007
529
530
531                                     ;SEARCH REGISTER DISPLAY ROUTINE.
532                                     ;THIS ROUTINE MOVES THE CONTENTS OF THE
533                                     ;SEARCH REGISTER (MAR, INSTR OR RDR) TO THE
534                                     ;DISPLAY PROGRAM WHERE IT CAN BE DISPLAYED
535                                     ;ALONGSIDE R0 OR SPLASTS (DEPENDING ON MODE).
536 1261         SRDISP: LI 16
    1261    020
    1262    016
537 1263                LI 0
    1263    000
    1264    000
538 1265                LA R
    1265    307
539 1266                IN I
    1266    060
540 1267                 B  M
    1267    017
541 1270                LI 0
    1270    000
    1271    000
542 1272                LM 1
    1272    171
543 1273                IN
    1273    040
544 1274                LM M
    1274    171
545 1275                IN -
    1275    041
546 1276                 M C
    1276    170
547 1277                LAI 40
    1277    004
    1300    040
548 1301                OUT REG
    1301    132
549 1302                JMP DISP1
    1302    104
    1303    022
    1304    000
550
551
552                                     ;LOAD ADDRESS ROUTINE.
553                                     ;THIS ROUTINE SERVICES THE LOAD KEY FUNCTION
KT11B PROGRAM  RT-11 MACRO VM02-10    08-SEP-82 PAGE 84
```

```
543 1221                        OUT R2HS        ;TC.CONTINUE, IF THE PROCESSOR IS ALREADY
    1223    135
544 1224                        LXI D           ;DETERMINE THIS JOB HAVE AN EF FILE
    1227    030
    1229    040
545 1224                        DLI 1,1B
    1224    145
546 1225                        JMP SRDISP      ;JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
    1228    134
    1229    96
    1227    010
547
548
549                                             ;LOAD SWITCH REGISTER ROUTINE.
550                                             ;THIS ROUTINE SERVICES THE LSR KEY FUNCTION.
551                                             ;LOADS TEMPORARY AREA INTO THE SWITCH
552                                             ;REGISTER. PAGE ADDR WHEN LOADS THE SWITCH
553                                             ;REGISTER AND SETS PROJECT NO LOADS.
554 1230        ;SR1:   LXI D                   ;SET R/W PROTECTION TO USR MEMORY AT A PAG
    1230    960
    1231    010
555 1232                LP H                    ;MOVE THE WORDS TO R REGISTER H AND L
    1232    247
556 1233                DA L
    1233    060
557 1234                LP H
    1234    217
560 1235                LXI SP                  ;RESET STACK POINTER TO SA TCH REGISTER
    1235    006
    1237    016
561  237                LP A                    ;PAGE ALEA AND LOAD MEMORY FROM REGISTERS
    1237    170
562 1240                DA I                    ;A AND I
    1240    040
563 1241                LP B
    1   171
564 1242                CAL SRLI                ;CALL THE SR  GUT SUBROUTINE AND
    1242    106
    1245    250
    1247    0 0
565 1245                JMP SRDISP              ;JUMP TO SWITCH REGIST R DISPLAY ROUTINE.
    1245    104
    1246    261
    1247    0 0
566
567
570                                             ;SR LOAD SUBROUTINE.
571                                             ;THIS SUBROUTINE LOADS THE SWITCH REGISTER
572                                             ;WITH THE CONTENTS OF THE SWITCH REGISTER
573                                             ;IMAGE PREA IN ROM-THIS SUBROUTINE IS USED
574                                             ;BY THE LOAD SWITCH REGISTER ROUTINE, AND
575                                             ;AFTER DATA'S TO RESTORE THE SWITCH REGISTER.
57. 1210        SRLI:   LXI SP                  ;SET MEMORY POINTER TO SWITCH REGISTER  PAGE ADDR
    1210    166
    1211    016
576 1212                LP M                    ;AND LOAD THE CONTENTS OF THE SWITCH REGIST
    1212    217
MYILB PROGRAM  RT-1  YAGLO VMQP-10    COMPILED WED 11
```

```
573 1235                LA A            GET TH' FIRST WORD
    1235    301
574 1236                OUT SALE
    1236    177
575 1237                IN L
    1237    060
576 1240                LA A            LOAD IN HIGH BYTE OF TH' SWITCH REGISTER
    1240    302
577 1241                OUT SCHB        WITH IN  NEXT DISPLAY MEMORY
    1241    131
578 1242                RET
    1242    007
579
580
581                                     ;SWITCH REGISTER DISPLAY ROUTINE.
582                                     ;THIS ROUTINE MOVES TH' CONTENTS OF THE
583                                     ;SWITCH REGISTER FRAME AREA OF RAM TO T E
584                                     ;DISPLAY AREA OF RAM AND SETS THE SWITCH
585                                     ;REGISTER ACTIVE LEVEL (SR FIG') INDICATOR.
586 1243        SRDISP: LIT 1A
    1243    06A
    1244    016
587 1245                LCI 5
    1245    035
    1247    000
588 1250                LA A
    1250    307
589 1251                IN L
    1251    0a0
590 1252                LB  M
    1252    317
591 1253                LL  0
    1253    066
    1254    000
592 1255                IN 0
    1255    370
593 1256                IN
    1256    060
594 1257                LA B
    1257    371
595 1260                IN
    1260    060
596 1261                 N 2
    1261    372
597 1262                LAI 40
    1262    004
    1263    040
598 1264                NDI 40H
    1264    174
599 1265                JMP ,DISP1
    1265    144
    1266    022
    1267    000
600
601
602                                     ;LOAD ADDRESS ROUTINE.
603                                     ;THIS SUBROUTINE LOADS THE LOAD ADDRESS
MCILIB PROGRAM  RT-11 MACRO V05.00    08-JAN-93 PAGE  81
```

```
                                        ;BY MOVING THE CONTENTS OF THE TEMPORARY
                                        ;AREA BACK TO THE USER'S ADDRESS POINTER
                                        ;AREA OF HOW MANY WORDS THE TEMPORARY
                                        ;AREA.
                        .DEF1-  LAI 0   ;CLEAR ANY INFORMATION.
                                DIT RES6
                                LLI 10          ;FROM TEMPORARY TO USER'S ADDRESS POINTER.
                                LD M
                                LK L
                                LI M
                                EXI
                                 A Y
                                MDI 7,
                                 M I
                                LM I
                                IN L
                                 N B
                                 M .
                                LA A
                        .DR1-   LAI 0
                                LI  REL6
                        .DL2I   L  10           ;CLEAR THE TEMPORARY AREA.
                                LH A
                                LA L
                                LI A
                                IN
                                .M 0
                                JMP MD21
<FILE PROGRAM  R1-11 MACRO VM02-10    20113125 PAGE 10-
```

```
      1342    042
      1343    001
632
633
634                                     ;DISPLAY ADDRESS ROUTINE.
635                                     ;THIS ROUTINE SERVICES THE DISPLAY KEY
636                                     ;FUNCTION.  IT MOVES THE USERS ADDRESS TO MEM
637                                     ;TO THE DISPLAY AREA IN RAM.
638 1344          DISPADI LXI D
      1344    00E
      1345    00F
639 1346                  ORI 1 OA      ;DISPLAY INDICATORS.
      1346    0A
640 1347                  LLI 13
      1347    06E
      1350    0 D
64  1351                  LA M
      1351    307
642 1352                  NDI 2         ;CLEAR EXAMINE AND DISPLAY FLAGS.
      1352    FF4
      1353    002
643 1354                  LM A
      1354    370
644 1355                  LLI 13        ;SET MEMORY POINTER TO UNIBUS ADDR LO POINTER AND
      1355    06E
      1356    013
645 1357                  JMP MOV2      ;JUMP TO MOVE ROUTINE TO MOVE THE DATA TO DISPLAY.
      1357    104
      135B    044
      1361    001
646
647
648                                     ;WAIT TEST SUBROUTINE.
649                                     ;THIS ROUTINE TESTS TO SEE IF THE
650                                     ;PROCESSOR IS WAITING.
651 1363          WAITST  INP REDP
      1363    115
652 1364                  NI  40        ;IS WAIT KEY SET?
      1364    040
      1365    040
653 1366                  JTZ DISPL     ;NO, GO TO DISPLAY.
      1366    C20
      1367    033
      1370    040
654 1371                  RET           ;YES, RETURN.
      1371    007
655 1372          NUM1:   LLI 6
      1372    046
      1373    00A
656 1374                  LA M
      1374    307
657 1375                  NI  10        ;CONTROL KEY DEPRESSED?
      1375    010
      1376    010
658 1377                  JTZ NUM1X     ;NO, GO TO DIGIT-1 ROUTINE.
      1377    1F1
      1400    004
MYILE PROGRAM  01-11 MACRO ASSEMBLER    DEVELOPMENT VERSION
```

```
    1406    001
630 1401        MAINT1:  LHI A0          ;YES, MAINTENANCE MODE!!!
    1402    056
    1403    040
650 1404                 LA, 103         ;DO NOT LOOK FOR POWERED HALTS AND
    1405    006
    1406    100
651 1407                 OUT MISC        ;SET THE MAINTENANCE MODE INDICATOR.
    1410    172
652 1411                 LLI 0           ;KEEP IN 12 BITS OF PC AND DISPLAY.
    1412    046
    1413    000
653 1414                 INP R1A
    1415    105
654 1416                 LM A
    1417    370
655 1420                 IN 1
    1421    041
656 1422                 NI 0F7
    1423    367
657 1424                 NI 17
    1425    044
    1426    017
660 1427                 LM A
    1430    370
661 1431                 LA L
    1432    060
662 1433                 LMI 0
    1434    076
    1435    000
663 1436        MAINT2:  CAL DISP        ;CALL THE DISPLAY SUBROUTINE.
    1437    104
    1440    041
    1441    000
664 1442                 LBT 0           ;TIE COMMAND IS TO BYPASS ROUTINE
    1443    016
    1444    000
665 1445                 LI 200          ;FLAG THOSE KEY FUNCTIONS AVAILABLE IN
    1446    006
    1447    200
674 1450                 L A I           ;MAINTENANCE MODE.
    1451    076
    1452    007
675 1453                 LI 0
    1454    207
676 1455                 RAR
    1456    052
677 1457                 JTS KDISP
    1460    140
    1461    167
    1462    0 1
700 1463                 XAR
    1464    370
701 1465                 XAR
    1466    372
702 1467                 XAR
    1470    370
```

```
681 144a                    JTC MOD 4
    144b    140
    1448    144
    144c    01
682 144e                    IN 1
    1448    040
683 1447                    IN ..
    1447    060
684 1450                    LO M
    1450    307
685 1451                    RAR
    1451    032
686 1452                    JTC MSBDAT
    1452    140
    1453    126
    1119    011
687 1455                    RA:
    1455    072
688 1456                    JTC TORBJS
    1460    140
    1457    001
    1460    011
689 .46..                   JN L
    .46.    020
690  462                    JN L
    467     020
691 .465                    LO M
    .46A    .07
692  464                    RAC
    .464    032
693 .465                    JTC PHLT
    .465    140
    .466    122
    .467    011
694 1470                    RAC
    170     023
695  47                     JTC PCUST1
    47      140
    .472    142
    .473    011
696  471                    RAR
    471     023
697  475                    JTC PUDJ1
    475     140
    476     202
    477     011
698 1500                    MAR
    500     037
699 .50                     JTC PSTCT1
    50.     140
    .502    124
    .503    011
700  504                    JMP MAIN10
    .504    .04
    .505    072
    .506    011
701 1507        PDIEADI L.I 0           *READ IN UNIBUS ADDR SS LINES AND DISP AY.
PDP11/M PROCESSOR  V7-1  MACRO JM02-10    30-13:25 PAGE 84
```

```
                1502    044
                1503    000
7C4 1504                        LXI H,0
                1507    000
7C8 1508                        LX A
                1509    320
7C9 150B                         M L
                150C    003
7CB 150D                         M F,M2
                150F    1C7
7CE 1510                        LX A
                1511    303
7D0 1513                         M L
                1514    047
7D1 1515                        INR B,G+
                1516    1 1
7D3 1518                        VDI 7
                1519    0F1
                151A    000
7D6 151C                        LXI D
                151D    E70
7D  151E                        JMP MAINT2
                151F    104
                1520    07F
                1521    FF.
7E2 1522        <DSIVC1 LXI D           #R:AD IN UNIQUE DATA TIMES AND DCB LOC+
                1523    C86
                1525    000
7E6 1526                        JMP LOLP
                1527    1D7
7E9 1529                        LX A
                152A    320
7EC 152C                         V I
                152D    C80
7EE 152F                        JMP UBFF
                1530    .A3
7F1 1531                        LX A
                1532    7C0
7F4 1534                         V I
                1535    0E0
7F6 1537                        LXI D
                1538    000
                1539    0C0
7FC 153C                        JM  FAJBIJ
                153D    V1
                153E    0D7
                153F    V1J
7C1 1540        R INIT1 : AI 200        ; ENTER HERE IF DCB OK  WAIT AND CANCEL
                1542    0D1
                1543    3D7
7C8 1545                        MI M,0          FILEIN B.IS+
                1546    1A1
7CB 1548                        AI  00          FILEIR NABLAL L.DLN 211+
                1549    0DE
                154A    1A0
7D0 154C                        CUT REIS
                154D    1C0
RV 1.0 P1.0867[1]  RT .. AnZR0 JMH.2-10    ...1A/05 /A1A 8+
```

```
                        IN   PA,PT
                        AND  I,1
                        SKP  Z
                        JMP  .-3
                        IOF
                        JMP  .-5
                        IOT  PTR,RCC
                        JMP  .-1
                        IOT  PTR,RSB
                        JMP  .-1
                        IOT  PTR,RCB
                        JMP  .-1
                        IOT  PTR,RSF
                        JMP  .-1
                        IOT  PTR,RRB
                        DAC  I,1
                        ISZ  I,1
                        JMP  .-3
                        JMP  @I,1
```

```
     161a    C0.
     161b    01
745  161c          NUM7:   L.I A
     161d    036
     161e    036
746  161f                  IA P
     1620    307
747  1621                  NI  10          #CNTRL KEY DEPRESSED?
     1622    044
     1623    010
748  1624                  JIZ NUM7X       #NO. GO TO DIGIT 7 ROUTINE.
     1625    150
     1626    376
     1627    000
749  1628                  LCI 2           #OFFSET ADDRESS CALCULATED BY ADDING THE
     1629    026
     162a    007
750  162b                  LII  A          #UNIQUE ADDRESS POINTER TO TEMPORARY PLUS
     162c    060
     162d    0.4
751  162e          ADD:    LB A            #ADD.
     162f    312
752  1630                  BC L
     1631    041
753  1632                  LA M
     1633    307
754  1634                  LLI 10
     1635    066
     1636    010
755  1637                  AD C
     1638    202
756  1639                  AI M
     163a    107
757  163b                  LM A
     163c    320
758  163d                   N L
     163e    060
759  163f                  LA B
     1640    301
760  1641                  AD M
     1642    217
761  1643                  LM A
     1644    270
762  1645                  JFF *001        #CHECK AT ANSWER TO THE UPPER.
     1646    101
     1647    002
     1648    001
763  1649          NUM8:   L.I A
     164a    0aA
     164b    036
764  164c                  IA P
     164d    307
765  164e                  NI  10          #CNTRL KEY DEPRESSED?
     164f    044
     1650    010
766  1651                  JIZ NUM8X       #NO. GO TO DIGIT 8 ROUTINE.
     1652    150
BY LCD PROGRAM  01.11 ASSEMBLY ORDER 10    00112425 PAGE 84
```

```
     1e11    122
     16e2    900
7a7 16e3                .CI 0           ;YES, SET UP MEMORY POINTER TO ADD
     16e5    126
     1e14    000
7a8 16e7                .LI 17          ;THE SWITCH REGISTER FLAG IS TEMPORARY
     16e9    0A6
     1e4a    017
7a9 16e7                .MP ADD         ;CLOSE ZERO
     16e7    104
     1e40    264
     1e41    01
7a0                                     ;THATS IT FOLKS !!
//       000000 *                .MI
KY.1.3 PRIMRIM  RT-11 MACRO VM02-10     00:17:25 PAGE 81
SYMBOL TABLE

.          = 000640          ADD     00.e3?          A       = 00000
BADLD   000746          BEHIN   000000          BEG1    000016
BUFF    000845          BUFNM   000827          C       = 000002
CLR1    00.327          CLR2    00 352          CURT.   00.312
D       = 000007          DATI    000650          DAII2   000607
DATO1   0007e           DBHP    0*0001          DBL0    = 000000
DEP1    000e7           DEP2    000217          D.E*AD  00.344
DIS*1   000027          DIS 17  000041          D'E*2   000642
DIS*3   000132          DIS*A   0*013A          D.E*5   000157
DISP5   000145                  000016          DP*9    000007
.XMT2   000130          DPRIJ   0005/*          DPU(2   000674
DPRI3   000622                  000000          ELIB    001342
ELT1    00152X          ELIN    001017          ELI2    00.042
ELN.    001046          ENTA    001067          .ASCII  00.051
EN.IX   001133          .NIT*   001137          'NIT1   0011.1
E.*0    = 000005          K.YBU.  000.74          L       = 000006
LADI    00.345          LER.    001230          M       = 000001
MA.NTL  001411          M*INI2  001477          MBUFI   001407
MCLT    0015L4          MC[NI1  001544          ML IBM  001567
MDM.AT  001574          ML IBI  000646          MLM2    001001
MLL1    0015e2          MOV.    000410          MOV2    000414
MS.LII  001544          MLMX    00040.          NLM0    = 000402
NUMCX   000412          NLM.    001471          NLM*X   000404
NLM2    = 000403          NLM2X   000402          NLM3    = 000402
NUM2X   000403          NLM4    = 000401          NLM4X   000401
NLM5    = 000400          NLM5X   000400          NLMA    001457
NLM6X   000572          NLM7    001420          NLM7X   000376
NX7     0*0012          OVER    000014          R0      = 000000
R1      = 000001          R2      = 000002          R3      = 000003
R4      = 000004          R5      = 000005          R6      = 000006
R7      = 000007          RIN*1   000641          RT      = 000647
SBRISP  001.2e1         SAVD    = 000004          SP      = 000006
SRLI    001229          SE1     001034          START   000300
STR11   0*.110          TMR2L5  001401          TIME*   001.43

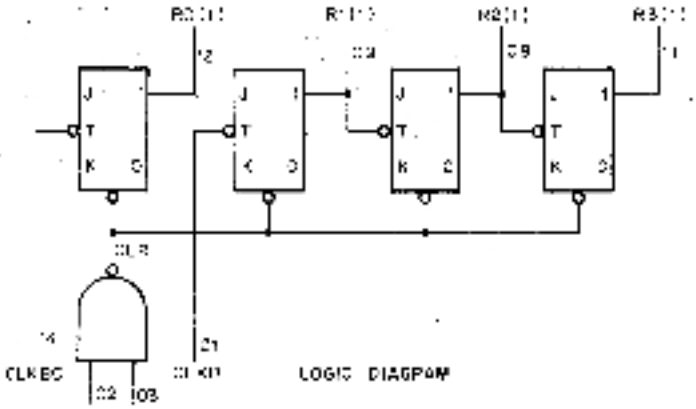
. ABS.  001672      000
        000000      00
LINKING RLIB:[1,1]SYSLIB/LB:Q
FREE CODE:  2480. WORDS

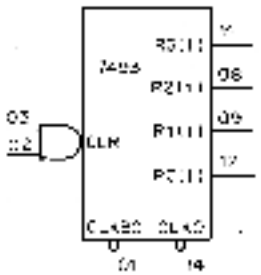
TEXT.TEXT=0.BE.TEXT

x
```

APPENDIX B
IC DESCRIPTIONS

7493 BINARY COUNTER





7493 TRUTH TABLE
(SEE NOTES)

CLOCK INPUT PULSE	OUTPUT			
	QD	R1	R2	QA
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

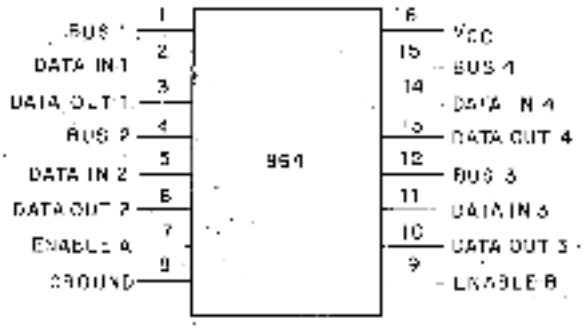
H = HIGH

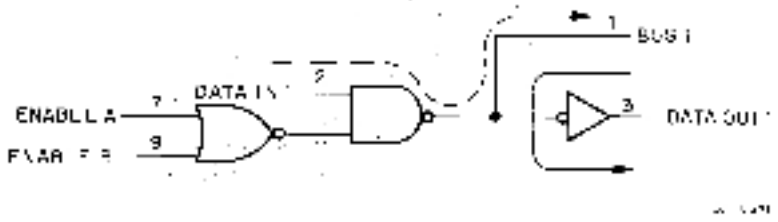
Notes:

1. Truth table applies when 7493 is used as 4-bit ripple-through counter.
2. Output QD(11) connected to input CLKB.
3. To reset all outputs to logical 0 both pins R0(1) and R0(2) must be high.
4. Either or both reset inputs R0(1) and R0(2) must be low to count.

8641 QUAD BUS TRANSCEIVER

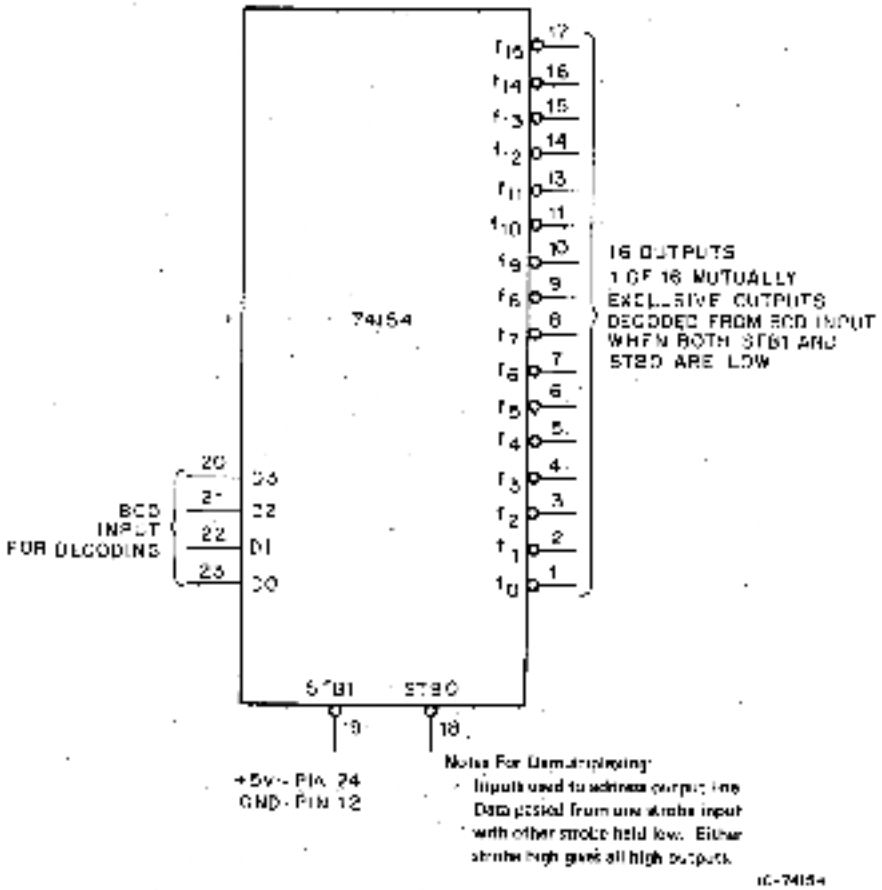
The 8641 consists of four identical receiver/drivers and a single enabling gate in one package for interfacing with the PDP-11 Unibus. The transceiver drivers are enabled when **ENABLE A** and **ENABLE B** are both low. The other input of each driver is connected to the data to be sent to the Unibus. For example, when enabled, **DATA IN 1** (pin 2) is read to the Unibus via **BUS 1** (pin 1). During a write operation, data comes from the Unibus as **BUS 1** (pin 1) and is passed through the receiver to the device as **DATA OUT 1** (pin 3).





74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

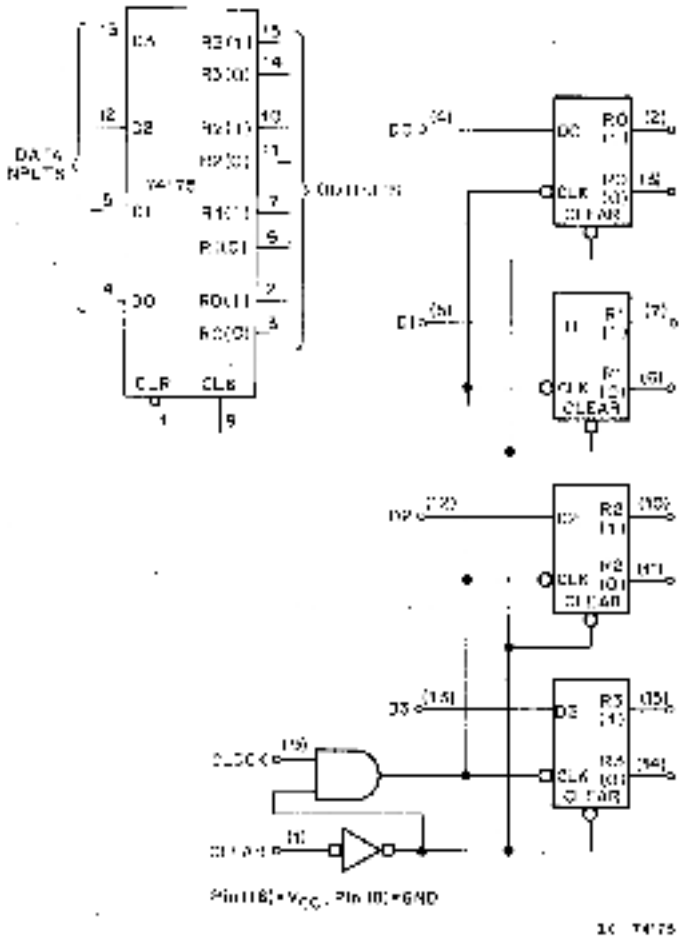


TRUTH TABLE

INPUT t_n D	OUTPUTS t_{n+1} Q0 Q1 Q2 Q3
H	H L
L	L H

t_n = Bit time before clock pulse.

t_{n+1} = Bit time after clock pulse.



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Module Operation and Maintenance Manual
EK-KY11B-MM-001

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