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**KY11-LB programmer's
console/interface module
operation and maintenance
manual**

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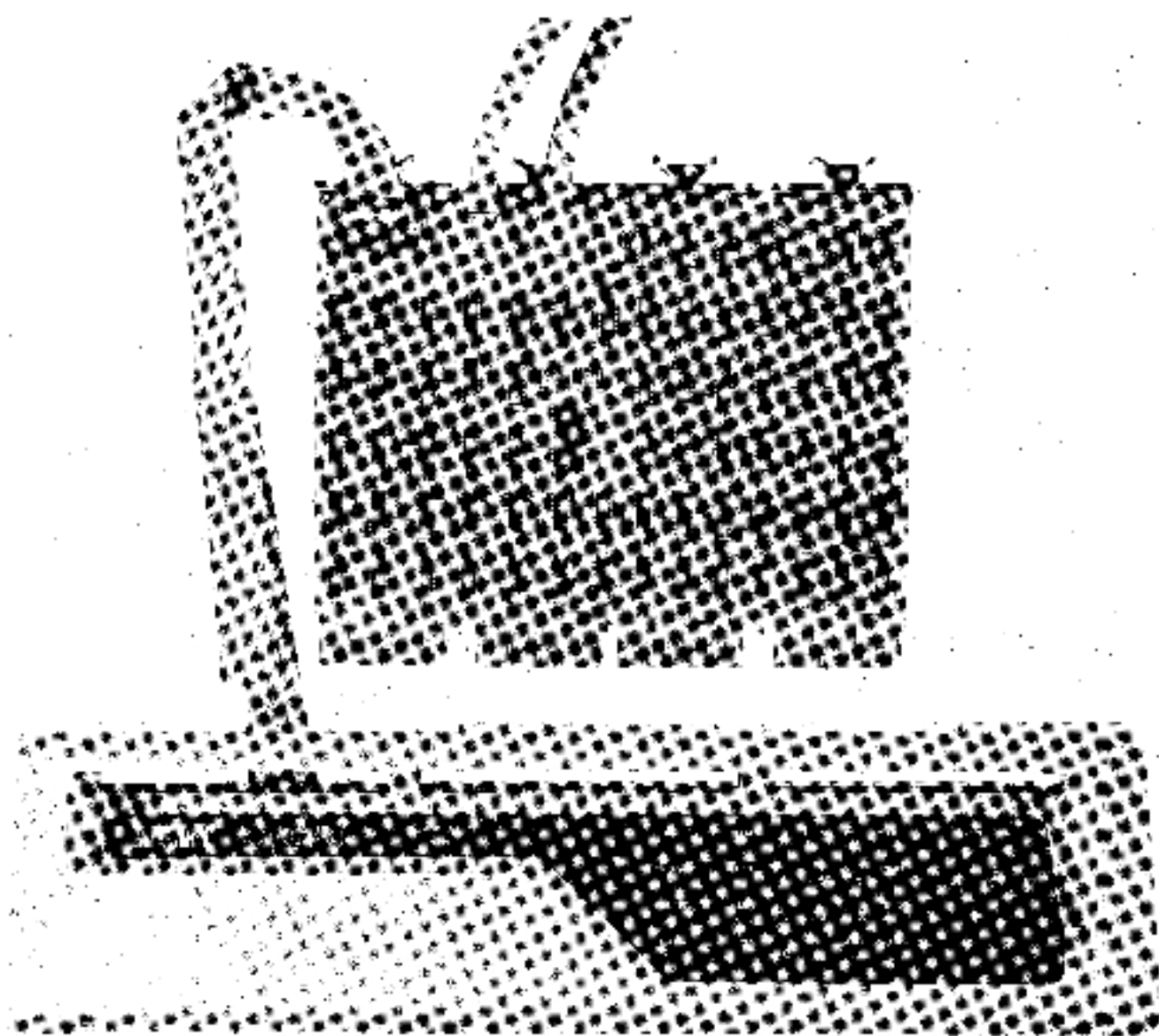
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KY11-LB PROGRAMMER'S CONSOLE/INTERFACE MODULE OPERATION



PREFACE

The *KY11-LB Programmer's Console/Interface Module Operation and Maintenance Manual* provides the information required to operate this option in console or maintenance mode. The manual also presents a detailed theory of operation of the interface module hardware and software components, data on the utilization of the programmer's console as a maintenance tool for the PDP-11/04/34 processors, and information on the troubleshooting and maintenance of the interface module itself. The information is presented in nine chapters:

- | | |
|-----------|---|
| Chapter 1 | Provides an introduction, general description, and overview of electrical and mechanical specifications. |
| Chapter 2 | Presents a functional description of the console, operating modes, controls and indicators, and a general discussion of interface module hardware organization and software facilities. |
| Chapter 3 | Describes, on a detailed block diagram level, interface module functions, registers and controls, and the functions of the MOS/LSI microprocessor. |
| Chapter 4 | Describes the microprocessor instruction set. |
| Chapter 5 | Presents a description of the M7859 Interface module to the logic level. |
| Chapter 6 | Provides operating information on console utilization in console mode. |
| Chapter 7 | Contains procedures for using the console in maintenance mode (maintenance of PDP-11/04/34 processor). |
| Chapter 8 | Covers some maintenance techniques for the KY11-LB interface module. |
| Chapter 9 | Describes installation procedures for various options. |

NOTES

In the material presented in this manual, the term "processor" refers to the RD11-D, RD11-E, and RD11-EA PDP-11/04/34 processors.

If the operator is not familiar with console functions, Chapter 6 should be consulted.

CHAPTER 1 OPERATING CHARACTERISTICS

1.1 INTRODUCTION

The PDP-11/04/34 Programmer's Console and Interface module (KY11-LB) provides all the functions now offered with the PDP-11/05. The Programmer's console interfaces to the Unibus (Figure 1-1) through a quad SPC module. To use this option, the normally provided KY11-LA Programmer's Console must be removed and the KY11-LB Console installed in its place. The KY11-LB Console contains a 7-segment LED display and a 20-key keypad for generating the console commands. Several indicators are also provided for additional convenience in monitoring system status.

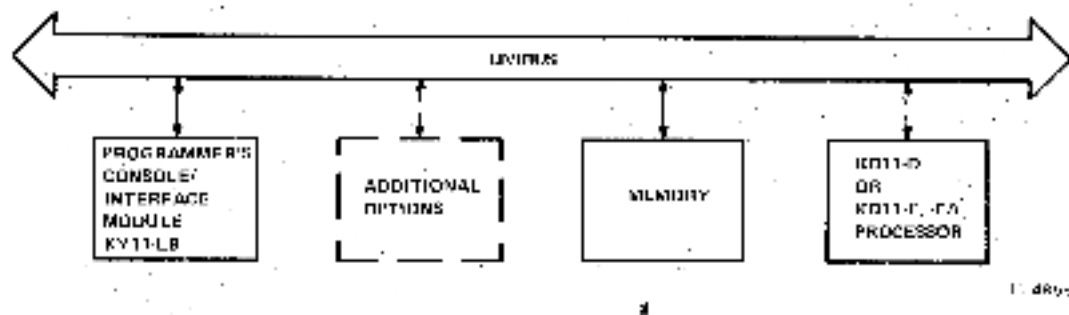
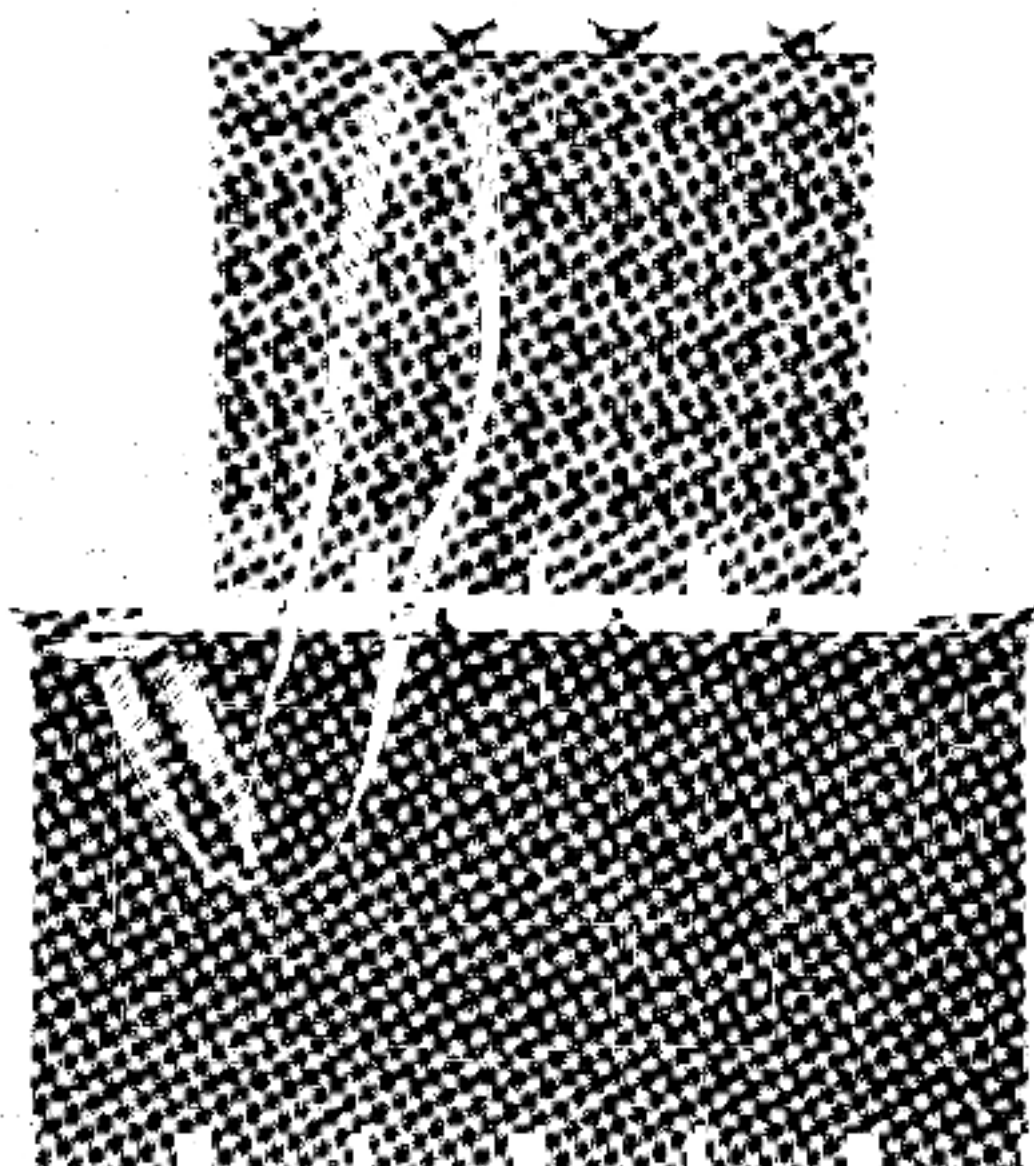


Figure 1-1 Programmer's Console/Interface - PDP-11/04/34 Configuration

The KY11-LB Programmer's Console/Interface module comprises an INTEL 8008 single-chip, large scale integration (LSI) microprocessor and associated registers, Unibus control logic, and auxiliary memory. The unit is also provided with a 20-key keypad for operator/programmer interaction with the KD11-D, -E, -EA via the interface module, six indicator LEDs, a 6-digit, 7-segment display for address or data, and a dc power switch. The microprocessor communicates with a read-only memory (ROM) which contains a number of fixed routines for use during normal console and maintenance operation.

1.2 GENERAL DESCRIPTION

The M7859 Interface module (Figure 1-2) functions as the interface between the programmer's console and the KD11-D, KD11-E, or KD11-EA processor, via the Unibus. The unit consists of solid state integrated circuits with TTL-compatible input and output lines. The heart of the interface module is a single-chip, large scale integration (LSI) microprocessor which executes designated keyboard functions via programs stored in ROM memory. Auxiliary logic functions including clock, decoding and timing circuitry, and addressing and Unibus drivers/receivers comprise the remaining logic of the board.



H141-14

Figure 1-2 Interface Module (M7859)

The microprocessor chip is an 8-bit, parallel control element packaged as a single metal oxide silicon circuit in an 18-pin, dual in-line package. With the addition of external clock driving circuitry and decoding elements, plus memory and data bus control, the unit is capable of performing as a powerful, general-purpose, central processing unit. Internal logic of the microprocessor chip is structured around an 8-bit internal data bus and includes instruction decoding, memory control, accumulator and scratchpad memory, arithmetic and logical capability, program stack, and condition code indicators. Data transfer between the microprocessor chip and the remaining logic functions of the interface module is accomplished through an 8-bit, bidirectional data port which is an integral part of the microprocessor. An internal stack (scratchpad memory) contains a 14-bit program counter (PC) and an additional complement of seven 14-bit registers for nesting up to seven levels of subroutines. The 14-bit addressing capacity allows the microprocessor to access up to 16K memory locations which may comprise any mix of ROM or RAM.

1.3 FUNCTIONAL DESCRIPTION

The KY11-LB Programmer's Console permits the implementation of a variety of functions through a 20-key keypad located on the front panel of the programmer's console. Keypad functions are divided into two distinct modes: console mode and maintenance mode. In console mode operation, a number of facilities exist for displaying addresses and data, for depositing data in and examining the content of Unibus addresses including processor registers for entering data into a temporary buffer for use as address or data, and for single instruction stepping the processor. The latter feature is especially useful during program debugging functions.

Normal console keyboard functions are not available during maintenance mode. This mode permits sampling and display of the Unibus address lines and Unibus data lines, and may allow the console to take control of the Unibus to examine and deposit Unibus addresses if a processor is not present in the system or is malfunctioning. Additionally, the maintenance function permits assertion of the manual clock enable and display of the current processor microprogram counter (MPC). Single-clock cycling of the MPC is also possible to facilitate step by step checkout of processor op codes and control logic during maintenance functions. In conjunction with this function, assertion of manual clock enable permits the processor to be stepped through its power-up routine. The manual clock enable may be dropped via the START key at any time with a resulting display of the current MPC. Exit from maintenance mode to console mode may be accomplished at any time by depressing the CLR key on the keypad.

1.4 SPECIFICATIONS

1.4.1 M7859 Interface Module Performance Specifications

Operating Speed at 500 kHz

Two-Phase Clock Period	2 μ s
Time State (SYNC)	4 μ s
Instruction Time (Microprocessor)	12-44 μ s

Word Size

Data	8-bit word
Instruction	1, 2, or 3 8-bit words
Address	14 bits

Memory Size

ROM	4 512 X 4 organized as 1024 8-bit words
RAM	16 words by 8 bits

Input/Output Lines	
Memory Data	16 bits
Address	18 bits
Control (Address)	2 bits
Unibus Control	5 bits
Microprocessor Instruction Repertoire	
48 Basic Instructions	
Instruction Categories	Register Operation
	Accumulator
	PC and Stack Control
	I/O
	Machine

1.4.2 Electrical Specifications

Power Supply	+5 V at 3.0 A -15 V at 60 mA
Input Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.8 Vdc
TTL Logic High	2.0 to 3.6 Vdc
Output Logic Levels (all modules)	
TTL Logic Low	0.0 to 0.4 Vdc
TTL Logic High	2.4 to 3.6 Vdc
Power Consumption	
Interface Module	14 W
Monitor/Control Panel	1 W

1.4.3 Mechanical Specifications

M7859 Interface Module	
Board Type	Quad SPC
Dimensions	
Height	21.44 cm (8.44 in)
Length	26.08 cm (10.44 in)
Programmer's Console (Overall Panel Dimensions)	
Width	47.63 cm (18.75 in)
Height	13.02 cm (5.125 in)
Depth	6.76 cm (2.66 in)

1.4.4 Environmental Specifications

Ambient Operating Temperature	5° to 50° C (41° to 122° F)
Humidity	10% to 95% maximum, wet bulb 32° C (90° F)

CHAPTER 2

FUNCTIONAL DESCRIPTION

2.1 INTRODUCTION

Logical organization of the KY11-LB Interface module is centered around a microprocessor and a bidirectional data bus (Figure 2-1). The 8-bit data and address bus (D0-D7) is time multiplexed to permit control signals, 14-bit addresses, and data to be transmitted between the microprocessor, memory, and additional buffer registers. Two registers, the switch register and the bus address register, contain data and addresses (respectively) to be routed to the Unibus. The transceivers permit 16-bit data words to be loaded into the microprocessor from the Unibus via the 2-way data bus. Data flow depends on the type of operation indicated by the keypad and the instruction the microprocessor is executing at a given time.

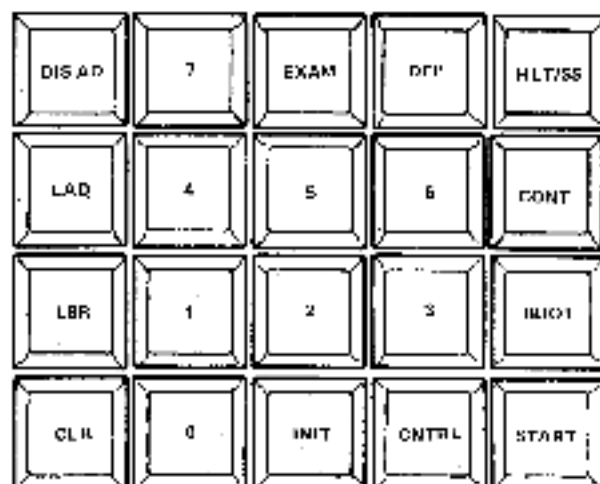
In a typical operation involving an instruction fetch, for example, the microprocessor program counter contents are transferred to the address register in two successive 8-bit bytes. The address register outputs activate the appropriate ROM location containing the instruction. The instruction is routed back via the tristate transceivers and the bidirectional bus to the microprocessor for decoding and subsequent execution. Instructions range from one to three bytes in length; the state counter decoding is capable of discriminating between the op code types and the resulting instruction length. The microprocessor is driven by a nominal 500-kHz, symmetrical, two-phase, nonoverlapping clock and is capable of responding to externally generated interrupt conditions. The data interface is a bidirectional 8-bit bus and the unit also provides four control outputs which include three state control signals and a sync signal. The control signals are applied to external decoding logic to generate system timing states and are subsequently distributed to the remaining interface module control circuitry. The state control signals are also utilized in the chip for sequencing data processing operations.

2.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTIONS/CONTROLS AND INDICATORS

Operator/programmer control of the KY11-LB is accomplished through a 20-key keypad located on the console panel (Figure 2-2). A summarized description of the key functions and other controls and indicators is contained in Table 2-1. The table first presents those functions involved in console mode which are primarily of interest to the programmer. A second portion of the table describes entry into maintenance mode and presents facilities useful for processor checkout and maintenance. The CNTRL key functions primarily as an interlock which prevents accidental interference with other console operations.

2.2.1 Console Mode

Detailed presentation of console mode keypad functions and their use in program debugging is reserved for a later chapter; the various functions are outlined and briefly described in Table 2-1. The operator indicators available for both modes are also described. Upon power-up, the programmer's console is in console mode. If in maintenance mode, pressing the CLR key causes a reversion to console mode through a HALT.



11-4242

Figure 2-2 KY11-1.B Keypad

Table 2-1 KY11-1.B Controls and Indicators

Control/Indicator	Function
Keyboard - Console Mode	
LAD	Load Address - Moves the 18-bit number in the temporary register into the Unibus address pointer. The temporary register is then cleared and displayed.
LSR	Load Switch Register - Moves the 16 lower bits of the temporary register to a register which can be read via Unibus address 777570. The switch register contents will be displayed.
DEP	Deposit - Causes the console to do a DATO on the bus address pointed to, using the data in the temporary register (two MSBs are truncated). Sequential deposits cause the address pointer to be incremented. This key is operative only if the processor is halted.
0-7	Numerics - These keys are used to enter data into a temporary data buffer prior to use as either address or data. Use of a numeric key forces the console to display the data held in the temporary buffer. A 6-digit number is generated as octal digits are entered from the right and left shifted.
CNTRL	Control - This key is used only in conjunction with other keys either to prevent accidental operation of certain functions or to provide entry into maintenance mode or other features. When used, the CNTRL key must be pressed first and held down while the second key is pressed. Those keys which are interlocked with the CNTRL key are indicated by "CNTRL-second key" (e.g., CNTRL-START).

Table 2-1 KY 11-LB Controls and Indicators (Cont)

Control/Indicator	Function
CNTRL-INIT	Initialize - Operative only if the processor is halted. Causes BUS INIT L to be generated for 150 ms.
DIS AD	Display Address - This key causes the current Unibus address pointer to be displayed. The next examine or deposit will occur at the address displayed.
EXAM	Examine - Causes the console to do a DAT1 on the bus address pointed to and stores the data in the temporary register which is then displayed. Sequential examines cause the address pointer to be incremented by 2 or by 1 if the address is in the range 777700-777717. This key is operative only if the processor is halted.
CLR	Clear Entry - Clears the current contents of the temporary register which is then displayed.
CNTRL-BOOT	Causes M9301 bootstrap terminator to be activated if present in the system. Console will boot only if the processor is halted.
CNTRL-HALT/SS	Halt/Single Step - Halts the processor if the processor is running. If the processor is already halted it will single-instruction step the processor. It also retrieves and displays the contents of R7 (program counter). The CNTRL key is not required to Single-Instruction Step the machine.
CNTRL-CONT	Continue - Allows processor to continue using its current program counter from a halted state. The contents of the switch register are displayed.
CNTRL-START	Operative only if halted, this causes the program counter (R7) to be loaded with the contents of the Unibus address pointer. BUS INIT L is then generated and the processor is allowed to run. Switch register contents are then displayed.
CNTRL-7	Causes the Unibus address pointer to be added to the temporary data buffer which is also incremented by 2. This allows the console to calculate the correct offset address when mode 6 or 7, register 7 PIC (Position Independent Code) instructions are encountered.
CNTRL-6	This causes the switch register to be added to the temporary data buffer. This is useful when mode 6 or 7 instructions are encountered not using R7.
CNTRL-1	Maintenance Mode - This combination puts the console into maintenance mode with certain maintenance features available. When the console is in maintenance mode, the normal console mode keypad functions are not available. The CLR key causes the console to exit from maintenance mode into console mode via a processor halt.

Table 2-1 KY11-LB Controls and Indicators (Cont)

Control/Indicator	Function
Keyboard - Maintenance Mode	
NOTE	
In maintenance mode the keypad functions are redefined with the following definitions.	
DIS AD	Causes the Unibus address lines to be sampled and displayed.
CLR	Returns the console to console mode via a console halt.
EXAM	Causes the console to sample the Unibus data lines and display the data.
5	Causes the console to take control of the Unibus. Should be used only when a processor is not present in the system.
HLI/SS	Asserts manual clock enable and displays the current microprogram counter (MPC).
CONT	Asserts manual clock enable, generates a manual clock pulse, and displays the current MPC.
BOOT	Boots the M9301. If manual clock enable is asserted, this will allow the processor to be stepped through the power-up routine.
START	Drops manual clock enable and displays the current MPC.
Indicator LEDs - Any Mode	
DC ON	All dc power (+5 V) to logic is on.
BATT	Battery monitor indicator, operative only in machines having the battery back-up option. This indicator has four states: - Off - Indicates either no battery present or battery failure if a battery is present. - On (continuous) - Indicates that a battery is present and charged. - Flashing (slow) - Indicates ac power is ok and battery is charging. - Flashing (fast) - Indicates loss of ac power and that battery is discharging while maintaining MOS memory contents.
RUN	Indicates the state of the processor, either running or halted.

Table 2-1 KY11-1.B Controls and Indicators (Cont)

Control/Indicator	Function
SR DISP	Indicates that the content of the switch register is being displayed.
MAINT	Indicates that console is in maintenance mode.
BUS ERR	Indicates that an examine or deposit resulted in a SSYN timeout or that HALT REQUEST failed to receive a HALT GRANT.
DC Power Switch	
DC OFF	All dc power to logic is off.
DC ON	All dc power to logic is on.
STNBY	DC power is provided to MOS memory only.*

*Available in all BA11-C machines. Available in BA.1-K boxes which have Battery Backup Option only.

Table 2-1 refers to certain registers which are located in the scratchpad RAM. These include the following:

1. Display Data
2. Keypad Image
3. Temporary Data Buffer
4. Unibus Address Pointer
5. Switch Register Image
6. EXAM, DEP, ENB and CI flags

Detailed discussion of the scratchpad RAM and its registers is set forth in Chapter 5.

2.2.2 Maintenance Mode

Maintenance mode is entered by pressing the CNTRL key and the I key simultaneously. Note that the functions performed by the appropriate keys are quite different from console mode. This mode offers the ability to assert the manual clock enable and thus to single-clock cycle the processor while monitoring the contents of the processor microprogram counter.

2.3 HARDWARE ORGANIZATION

A detailed block diagram of the interface module showing data flow and control is indicated in Figure 2-3. The control functions shown include those for the Unibus interface and the internal data bus with the microprocessor. The latter controls include those for reading from and writing into the RAM, enabling ROMs 1 and 2, and reading the Unibus temporary buffer register or loading the bus address and switch registers. All of these functions occur on appropriate control from the stored program and keypad.

Under microprogram control, the data bus control logic develops the loading or reading signal for the appropriate register and thus determines the selected input/output port via the data bus control and the function currently being executed.

As shown in Chapter 3 when the detailed microprocessor cycle is presented, the microprocessor executes four basic machine cycles. They are summarized here to show their relation to interface module functions.

1. *PCI* - This is always the first cycle of a microprocessor instruction and initiates the instruction fetch. The program counter is transferred in two bytes from the microprocessor to the 16-bit interface module address register (14 bits of address, 2 control bits) to fetch the instruction data from either the ROM or RAM. A single byte of instructions is retrieved during this cycle.
2. *PCR* - This cycle may retrieve an additional byte of instruction (if the instruction is a 2- or 3-byte instruction) or it may fetch a data byte if the indicated instruction contains only one byte.
3. *PCC* - This cycle specifies the function as an I/O operation. This machine cycle reads and loads the address and data registers which cause information to be read from or written into the microprocessor.
4. *PCW* - This cycle controls the memory write function according to the designated address.

Figure 2-3 shows that the basic satellite logic and control for the microprocessor chip consists of the following elements:

- 2-phase master clock
- Decoder for interface module time states
- Power-up logic
- 16-bit address register
- 16-word $\times$ 8-bit RAM
- 1024-word $\times$ 8-bit RAM (four - 512×4)
- Switch register (16 bit)
- Switch register address decoding
- Bus address register (20 bit)
- Tristate transceivers
- Keypad scan and display logic
- Data bus control
- Unibus control and single-cycle control
- Indicator control
- Halt control

These major functions are briefly described in the following paragraphs; detailed theory of operation is presented in Chapter 5.

2-Phase Master Clock

The master clock drives the microprocessor internal logic and generates the system states for instruction sequencing. The nominal 1 MHz clock frequency is toggled down to two nonoverlapping, 500-kHz pulses known as phase 1 (O1) and phase 2 (O2). Phase 1 is normally used to pre-charge data lines and memories while phase 2 controls data transfers within the microprocessor.

Decoder for Timing States

The decoder element receives the state outputs S0, S1, and S2 from the microprocessor and generates the time states for the operation of the interface module. A sync pulse corresponding to two phase clock periods (1 time state) is also provided by the microprocessor.

Power-up Logic

This circuitry activates the microprocessor, clearing its various registers and generating a clear line to all the registers of the interface module. There are separate clears for the address register and all other registers.

Address Register

This 16-bit register is the principal buffer between the microprocessor and the remainder of the logic of the interface module. Although designated as an address register, the element also handles control data for the Unibus, data bus, and other control functions and outputs to the bus address and switch registers. One of its major functions is to receive the microprocessor program counter contents for fetching new instructions from the ROM or RAM.

RAM

The 16-word by 8-bit RAM gives the interface module a scratchpad memory which may be read or whose contents may be modified under program control.

ROM

The ROM, consisting of four 512×4 -bit ROMs, makes a total of 1024 8-bit bytes available for the stored programs which execute the console functions.

Switch Register Address Decoding

This logic decodes 777570, an 18-bit address defining the switch register and a DATI on the Unibus to cause the switch register to be enabled onto the Unibus.

Switch Register

This 16-bit buffer register handles the data word to the Unibus.

Bus Address Register

This 20-bit register buffers address information between the interface module and the Unibus. Eighteen bits are allocated for the actual address, and two control bits indicate the direction of data flow. Scan signals for the keypad and NUM lines for the display logic are specified by this register.

Tristate Gates

These units are used to gate buffered Unibus data (16 bits) and Unibus address (18 bits) lines onto the tristate data bus by asserting an appropriate read input line. Keypad outputs and those maintenance lines provided for display of the processor microprogram counter are similarly buffered and gated. The outputs are all wire ORed onto the internal data bus and applied as input to the tristate transceivers.

Keypad Scan and Display Logic

This circuitry develops read and drive signals for the keypad and LED display respectively. Five read signals developed from the scan signals are used to scan the keypad switch closures in groups of four. The drive signals are applied to the LED displays whose values are determined by the 3-bit NUM input.

Data Bus Control

This circuitry performs all internal interface module control functions including RAM control, ROM enable, and selection of input/output ports. The logic also determines system operation during instruction, data fetch, or data out (IS3) via a 32×8 -bit ROM.

Unibus Control

The Unibus control register supervises data transfers between the interface module and the Unibus. According to the input bit patterns to the register, data transfer from the interface module to the Unibus, halt request, bus master sync, and other functions may be generated as required for proper interfacing of the two elements. Two other signals generated in the Unibus control register permit single stepping of the processor clock.

Indicator Logic

This 4-bit register drives appropriate console indicators to show certain console states or errors. An indicator is turned on to show the existence of a bus error, when the switch register is being displayed or when in maintenance mode.

Halt Logic

This circuitry halts the processor under various conditions and performs handshaking functions when the console takes complete control of the bus. When a HALT from the console is detected by the processor, the processor recognizes it as an interrupt request. The processor then inhibits its clock and returns a recognition signal to the console causing the console to assert an acknowledge. The console now has complete control of the Unibus and processor and may maintain this condition, with the processor halted, as long as desired.

2.4 MICROPROCESSOR INSTRUCTION SET

The interface module microprocessor has a repertoire of 48 basic instructions. According to the instruction type, these may range from 1 to 3 bytes (8 to 24 bits) in length. The successive bytes of a given instruction must be located in sequential memory locations. Instructions fall into one of five categories:

- Index Register
- Accumulator (Arithmetic/Logical)
- Program Counter and Stack Control
- Input/Output
- Machine

A description of the microprocessor instructions and the number of time states required for their execution is given in Chapter 4.

CHAPTER 3 INTERFACE MODULE

3.1 MICROPROCESSOR

3.1.1 General Organization

The microprocessor sends and receives data over an 8-bit data and address bus (D₀ to D₇) and utilizes four input and four output lines (Figure 3-1). The microprocessor contains six 8-bit data registers, an 8-bit accumulator, two 8-bit temporary registers, four flag bits, and an 8-bit parallel binary arithmetic unit. The arithmetic element is capable of performing addition, subtraction, and logical operations. Additionally, a memory stack containing a 14-bit program counter and seven 14-bit words is used to store program and subroutine addresses. The microprocessor machine cycle usually requires five sequential states: TS1, TS2, TS3, TS4, and TS5. During time states TS1 and TS2, the external memory is addressed by a lower and an upper address byte respectively to form a 14-bit address. Also at TS1 time, the program counter (PC) is incremented for the next instruction fetch cycle. During time state TS3, the instruction addressed during states TS1 and TS2 is fetched and during the final two cycles, TS4 and TS5, it is executed. Figure 3-2 shows the possible number and sequence of the instruction states. Note that for this application of the microprocessor, the interrupt function is utilized only during the power-on sequence.

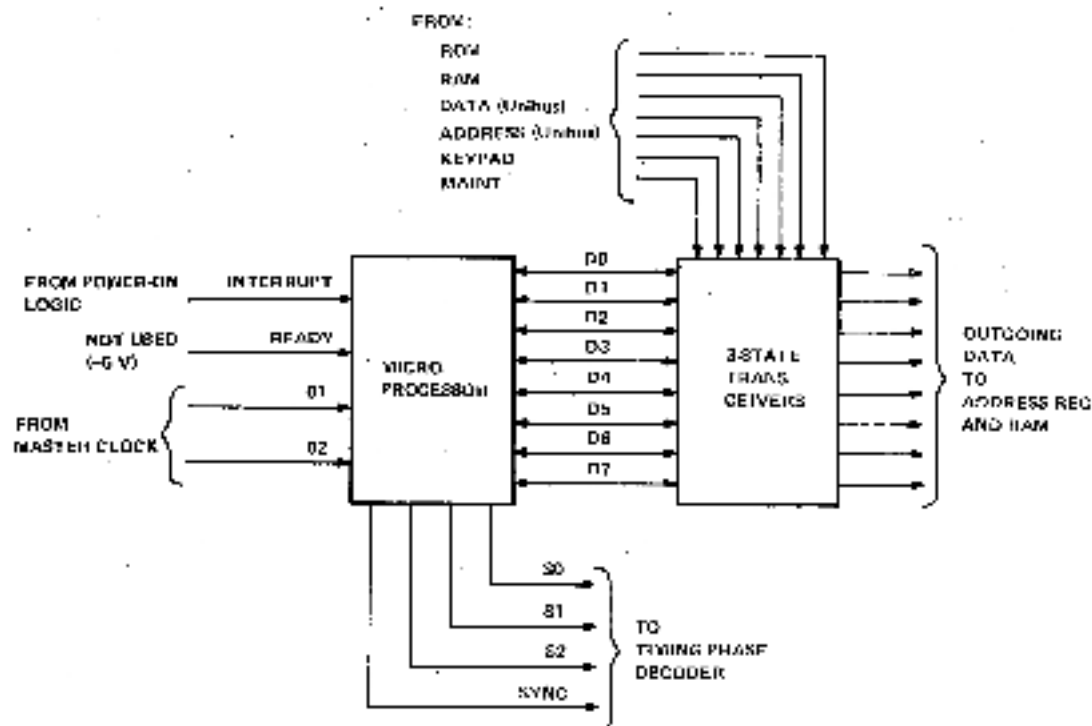
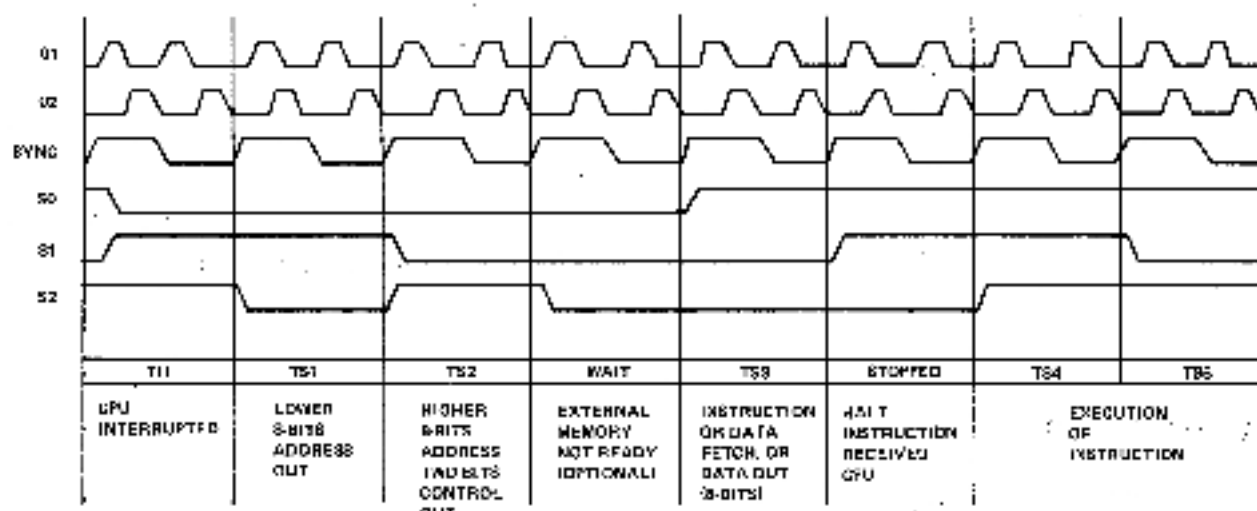


Figure 3-1 Microprocessor Signal Interface

11-4036



11-4830

Figure 3-2 Timing Diagram - Microprocessor Instruction

3.1.2 State Control

The microprocessor operates as a sequential state machine, controls the use of the data bus, and, according to its stored program, determines whether it sends or receives data. Output state signals S0, S1, and S2 are decoded externally and distributed to the peripheral control logic. Table 3-1 shows the coding of the state-bits to yield a given phase.

3.1.3 Microprocessor Timing

The microprocessor machine cycle is shown in Figure 3-2. Since machine operation is asynchronous, the exact timing sequences depend on the instruction executed. A typical cycle may consist of five states. During T1 and T2, an address is sent to memory; at T3 time, instruction or data fetch occurs; T4 and T5 provide execution time.

A number of microprocessor instructions may require up to three cycles and do not require the two execution states T4 and T5. As a result, cycle length is variable and the state counter determines whether T4 and T5 are to be executed or omitted. This is accomplished via the cycle control coding (Table 3-2) in bits D6 and D7. Cycle 1 is always an instruction fetch cycle (PCI). The second and third cycles are for data reading (PCR), data writing (PCW), or I/O operations (PCC). The cycle type bits D6 and D7 are present on the data bus during T2 time only.

Table 3-1 State Control Coding

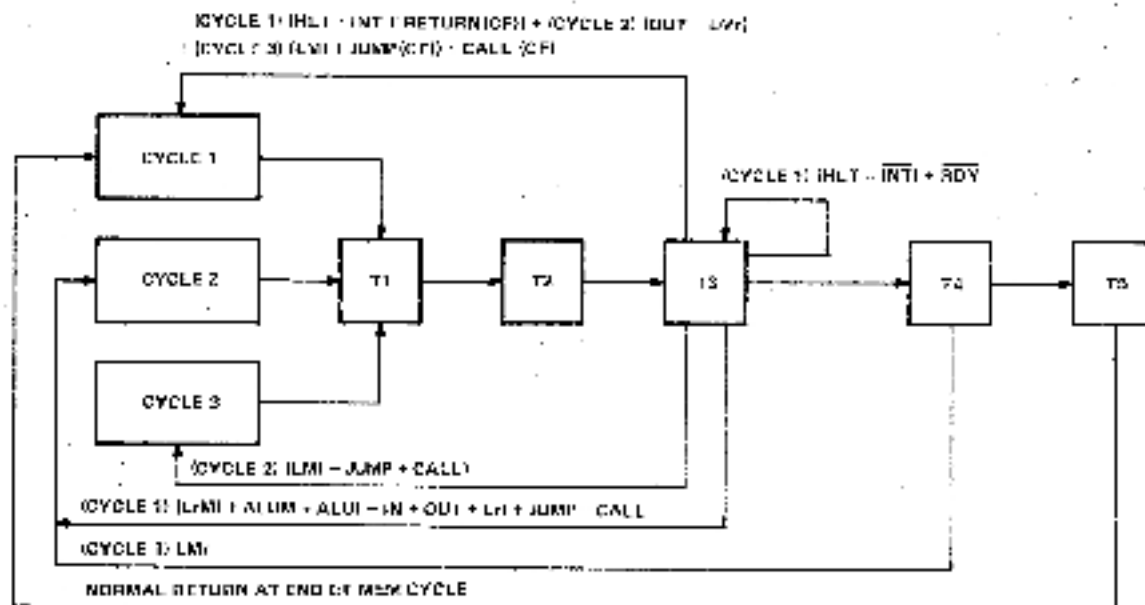
S0	S1	S2	State
0	1	0	T1
0	1	1	T11
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOPPED
1	1	1	T4
1	0	1	T5

Table 3-2 Cycle Coding

D ₆	D ₇	Cycle	Function
0	0	PCJ	Designates the address is for a memory read (first byte of instruction).
0	1	PCR	Designates the address is for a memory read data (additional bytes of instruction or data).
1	0	PCC	Designates the data is a command I/O operation.
1	1	PCW	Designates the address is for a memory write data.

3.1.4 Transition State Diagram

Possible state transitions within the processor are shown in Figure 3-3. Note that a normal machine cycle would begin at cycle 1, run from T1-T5, and revert back to cycle 1 again. The state counter within the microprocessor operates as a 5-bit feedback shift register with the feedback path controlled by the current instruction. The number of states normally required by each instruction is discussed in Chapter 4.



NOTE: CF = Future Condition

11-4051

Figure 3-3 Transition State Diagram

3.1.5 System Start-Up

The microprocessor of the interface module is running any time power is applied to the system. When power (VDD) and clocks (01, 02) are first turned on, a flip-flop internal to the microprocessor is set by sensing the rise of VDD. This internal signal forces a HALT (00000000) into the instruction register and the microprocessor is then in the stopped state. The next 16 clock periods are required to clear internal chip memories and other external logic and registers. Upon clearing the registers the system is ready for operation. If for any reason during operation, the microprocessor decodes a HALT, the system reverts to the beginning of the program after 16 clock periods.

3.2 INTERFACE MODULE REGISTERS AND CONTROLS (Figure 2-1)

3.2.1 Address Register

This is the principal buffer register between the microprocessor and the rest of the interface module logic. It has a capacity of 16 bits (two 8-bit bytes). The low order byte is loaded by time state TS1 and the high order byte by time state TS2 during each cycle.

3.2.2 Bus Address Register

The bus address register buffers address data between the interface module and the Unibus. Address information may be loaded into this register at time state TS3.

3.2.3 Switch Register

Similar to the bus address register, the switch register buffers outgoing data. This element may also be loaded at TS3.

3.2.4 Data Bus Control

The principal function of the data bus control is to determine interface module operation during TS3 time. It determines, through input bit coding, the type of function to be performed (i.e., RAM control, ROM enable) or programs any of its other I/O in accordance with the stored program.

3.2.5 Unibus Control

This register is also loaded at TS3 and is selected by the data bus control for activation at that time. According to its input coding, U.C.R. may issue a HALT request, BUS INIT, enable-data bus-to-bus, or generate a bus master sync in addition to other functions.

CHAPTER 4

MICROPROCESSOR INSTRUCTION DESCRIPTION

4.1 DATA AND INSTRUCTION FORMATS

Data in the CPU is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

OP CODE

Register to register, memory reference
I/O arithmetic or logical, rotate or
return instructions.

Two Byte Instructions

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

OP CODE

Immediate mode instructions.

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

OPERAND

Three Byte Instructions

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

OP CODE

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

LOW ADDRESS

JUMP or CALL instructions

$X X D_5 D_4 D_3 D_2 D_1 D_0$

HIGH ADDRESS*

*For the third byte of this instruction, D_5 and D_7 are "don't care" bits.

4.2 MICROPROCESSOR INSTRUCTIONS

4.2.1 Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

Mnemonic	Minimum States Required	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Description of Operation
(1) Lr ₁ r ₂	(5)	1 1 D D D S S S	Load index register r ₁ with the content of index register r ₂ .
(2) LrM	(8)	1 1 D D D 1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1 1 1 1 S S S	Load memory register M with the content of index register r.
(3) LrI	(8)	0 0 D D D 1 1 0 B B B B B B B B	Load index register r with data B ... B.
LMI	(9)	0 0 1 1 1 1 1 0 B B B B B B B B	Load memory register M with data B ... B.
INr	(5)	0 0 D D D 0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0 D D D 0 0 1	Decrement the content of index register r (r ≠ A).

4.2.2 Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

Mnemonic	Minimum States Required	Instruction Code D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Description of Operation
ADr	(5)	1 0 0 0 0 S S S	Add the content of index register r, memory register M, or data B ... B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0 0 0 0 1 1 1	
ADI	(8)	0 0 0 0 0 1 0 0 B B B B B B B B	Add the content of index register r, memory register M, or data B ... B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACr	(5)	1 0 0 0 1 S S S	
ACM	(8)	1 0 0 0 1 1 1 1	
ACI	(8)	0 0 0 0 1 1 0 0 B B B B B B B B	

Mnemonic	Minimum States Required	Instruction Code								Description of Operation
		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
SU _r	(5)	1	0	0	1	0	S	S	S	Subtract the content of index register <i>r</i> , memory register <i>M_i</i> , or data <i>B</i> . . . <i>B</i> from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1	0	0	1	0	1	1	1	
SUI	(8)	0	0	0	1	0	1	0	0	
		B	B	B	B	B	B	B	B	
SBr	(5)	1	0	0	1	1	S	S	S	Subtract the content of index register <i>r</i> , memory register <i>M_i</i> , or data <i>B</i> . . . <i>B</i> from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1	0	0	1	1	1	1	1	
SBI	(8)	0	0	0	1	1	1	0	0	
		B	B	B	B	B	B	B	B	
ND _r	(5)	1	0	1	0	0	S	S	S	Compute the logical AND of the content of index register <i>r</i> , memory register <i>M_i</i> , or data <i>B</i> . . . <i>B</i> with the accumulator.
NDM	(8)	1	0	1	0	0	1	1	1	
NDI	(8)	0	0	1	0	0	1	0	0	
		B	B	B	B	B	B	B	B	
XR _r	(5)	1	0	1	0	1	S	S	S	Compute the Exclusive OR of the content of index register <i>r</i> , memory <i>M_i</i> , or data <i>B</i> . . . <i>B</i> with the accumulator.
XRM	(8)	1	0	1	0	1	1	1	1	
XRI	(8)	0	0	1	0	1	1	0	0	
		B	B	B	B	B	B	B	B	
OR _r	(5)	1	0	1	1	0	S	S	S	Compute the Inclusive OR of the content of index register <i>r</i> , memory register <i>M_i</i> , or data <i>B</i> . . . <i>B</i> with the accumulator.
ORM	(8)	1	0	1	1	0	1	1	1	
ORI	(8)	0	0	1	1	0	1	0	0	
		B	B	B	B	B	B	B	B	
CP _r	(5)	1	0	1	1	1	S	S	S	Compare the content of index register <i>r</i> , memory register <i>M_i</i> , or data <i>B</i> . . . <i>B</i> with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1	0	1	1	1	1	1	1	
CPI	(8)	0	0	1	1	1	1	0	0	
		B	B	B	B	B	B	B	B	
RLC	(5)	0	0	0	0	0	0	1	0	Rotate the content of the accumulator left.
RRC	(5)	0	0	0	0	1	0	1	0	
RAL	(5)	0	0	0	1	0	0	1	0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0	0	0	1	1	0	1	0	

4.2.3 Program Counter and Stack Control Instructions

Mnemonic	Minimum States Required	Instruction Code		Description of Operation
		$D_7 D_6$	$D_5 D_4 D_3 D_2 D_1 D_0$	
(4) JMP	(11)	0 1	X X X 1 0 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Unconditionally jump to memory address $B_3 \dots B_3 B_2 \dots B_2$.
(5) JFc	(9 or 11)	0 1	0 $C_4 C_3$ 0 0 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Jump to memory address $B_3 \dots B_3 B_2 \dots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) JFc	(9 or 11)	0 1	1 $C_4 C_3$ 0 0 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Jump to memory address $B_3 \dots B_3 B_2 \dots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
(4) CAL	(11)	0 1	X X X 1 1 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Unconditionally call the subroutine at memory address $B_3 \dots B_3 B_2 \dots B_2$. Save the current address (up one level in the stack).
(5) Cf c	(9 or 11)	0 1	0 $C_4 C_3$ 0 1 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Call the subroutine at memory address $B_3 \dots B_3 B_2 \dots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(5) CTc	(9 or 11)	0 1	1 $C_4 C_3$ 0 1 0 $B_3 B_2 B_1 B_0 B_3 B_2 B_1 B_0$	Call the subroutine at memory address $B_3 \dots B_3 B_2 \dots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
(4) RET	(5)	0 0	X X X 1 1 1	Unconditionally return (down one level in the stack).
(5) RFc	(3 or 5)	0 0	0 $C_4 C_3$ 0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
(5) RTc	(3 or 5)	0 0	1 $C_4 C_3$ 0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RSI	(5)	0 0	A A A 1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

4.2.4 Input/Output Instructions

Mnemonic	Minimum States Required	Instruction Code $D_7 D_6 \quad D_5 D_4 D_3 \quad D_2 D_1 D_0$	Description of Operation
INP	(8)	0 1 0 0 M M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1 R R M M M 1	Write the content of the accumulator into the selected output port (RRMMM) ($RR \neq 00$).

4.2.5 Machine Instruction

Mnemonic	Minimum States Required	Instruction Code $D_7 D_6 \quad D_5 D_4 D_3 \quad D_2 D_1 D_0$	Description of Operation
(4) HLT	(4)	0 0 0 0 0 0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1 1 1 1 1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

- (1) SSS = Source Index Register These registers, r_i , are designated A (accumulator 000),
DDD = Destination Index Register R(001), C(010), D(011), E(100), H(101), L(110).
- (2) Memory registers are addressed by the contents of registers H & L.
- (3) Additional bytes of instruction are designated by BBBBBBBB.
- (4) X = "Don't Care".
- (5) Flag flip-flops are defined by $C_4 C_5$: carry (00 overflow or underflow), zero (01-result is zero),
sign (10 MSB of result is "1"), parity (11-parity is even).

CHAPTER 5

INTERFACE MODULE DETAILED LOGIC DESCRIPTION

5.1 INTRODUCTION

Keypad operation initiates appropriate microprocessor routines which perform certain data transfers within the interface module, between the interface module and the Unibus, and between the interface module and the programmer's console display. Prior to discussing the interface module logic, the sequences (i.e., register transfer, I/O operations, etc.) which occur after pressing a given key are briefly described.

Figure 5-1 shows the 16-word by 8-bit scratchpad RAM and its address allocations. This data is also summarized in Table 5-1. The keypad image within the RAM is shown in Figure 5-2.

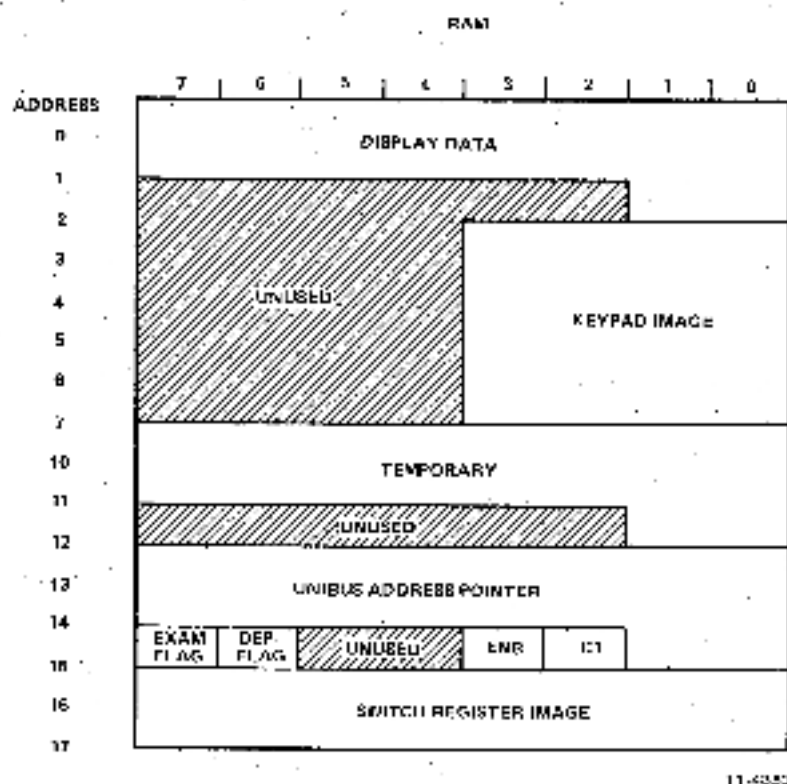


Figure 5-1 RAM Address Allocations

	KEYPAD IMAGE			
	3	2	1	0
3	CLR	LSH	LAU	DIS AB
4	0	1	4	7
5	INIT	2	5	EXAM
6	CTRL	3	6	DEP
7	START	BOOT	CONT	HLT/AS

11-4854

Figure 5-2 Keypad Image

Table 5-1 RAM Function Address Assignments

Function	Address (Octal)	Address Bits
Display Data (18 bits)	Word 0	Bits 0-7
	Word 1	Bits 0-7
	Word 2	Bits 0, 1
Keypad Image (20 bits)	Word 3	Bits 0-3
	Word 4	Bits 0-3
	Word 5	Bits 0-3
	Word 6	Bits 0-3
	Word 7	Bits 0-3
Temporary Data Buffer (18 bits)	Word 10	Bits 0-7
	Word 11	Bits 0-7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0-7
	Word 14	Bits 0-7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
CI FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0-7
	Word 17	Bits 0-7

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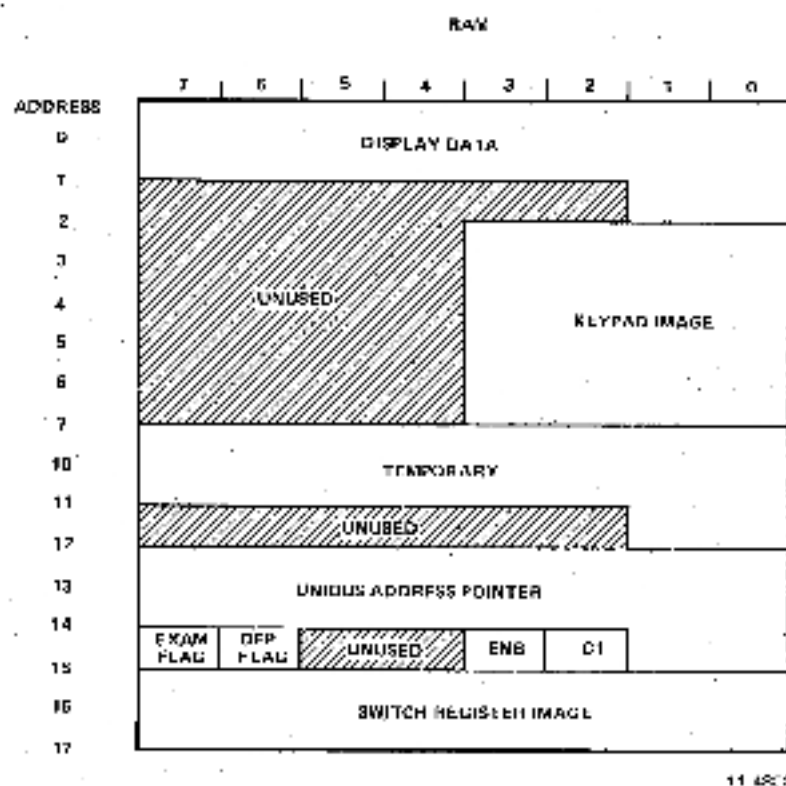


Figure 5-1 RAM Address Allocations

	KEYPAD IMAGE			
	3	2	1	0
2	CLK	LSR	LOAD	DIS AD
4	0	1	4	7
6	INCL	7	5	EXAM
8	CTRL	3	6	DEP
7	START	BOOT	CONT	HLT/SS

11-004

Figure 5-2 Keypad Image

Table 5-1 RAM Function Address Assignments

Function	Address (Octal)	Address Bits
Display Data (18 bits)	Word 0	Bits 0-7
	Word 1	Bits 0-7
	Word 2	Bits 0, 1
Keypad Image (20 bits)	Word 3	Bits 0-3
	Word 4	Bits 0-3
	Word 5	Bits 0-3
	Word 6	Bits 0-3
	Word 7	Bits 0-3
Temporary Data Buffer (18 bits)	Word 10	Bits 0-7
	Word 11	Bits 0-7
	Word 12	Bits 0, 1
Unibus Address Pointer (18 bits)	Word 13	Bits 0-7
	Word 14	Bits 0-7
	Word 15	Bits 0, 1
EXAM FLAG	Word 15	Bit 7
DEP FLAG	Word 15	Bit 6
ENB FLAG	Word 15	Bit 3
CI FLAG	Word 15	Bit 2
Switch Register Image (16 bits)	Word 16	Bits 0-7
	Word 17	Bits 0-7

5.2 PROGRAMMER'S CONSOLE KEYPAD FUNCTION SEQUENCES

5.2.1 Console Mode Key Functions

NUMERICS (0-7)

1. Value of Key $\xrightarrow{\text{(left shifted)}}$ Temporary Data Buffer
2. Temporary $\rightarrow$ Display
3. Clear indicators.

LAD

1. Temporary $\rightarrow$ Unibus Address Pointer
2. Zero $\rightarrow$ Temporary
3. Temporary $\rightarrow$ Display
4. Clear/Indicators.

LSR

1. Temporary $\rightarrow$ Switch Register Image
2. Switch Register Image $\rightarrow$ Switch Register
3. SR DISP indicator is set.

CLR

1. Zero $\rightarrow$ Temporary
2. Temporary $\rightarrow$ Display
3. Clear indicators.

EXAM

1. Pre-increment Unibus address pointer if the EXAM flag is set.
2. Unibus Address Pointer $\rightarrow$ Bus Address Register
3. Bus Address Register $\rightarrow$ Unibus Address
4. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μ s, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data $\rightarrow$ Temporary
6. Temporary $\rightarrow$ Display
7. Set EXAM flag.

DEP

1. Pre-increment Unibus address pointer if the DEP flag is set.
2. Unibus Address Pointer $\rightarrow$ Bus Address Register with C1 = 1.
3. Bus Address Register $\rightarrow$ Unibus Address
4. Temporary $\rightarrow$ Switch Register
5. Switch Register $\rightarrow$ Unibus Data
6. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μ s, the transfer is aborted and the BUS ERR indicator is set.

7. Set DEP flag.
8. Switch Register Image $\rightarrow$ Switch Register

DIS AD

1. Unibus Address Pointer → Display
2. Clear EXAM or DEP flag if set.

CNTRL-INIT

1. Set BUS INIT and HALT REQUEST for 150 ms.

CNTRL-HLT/SS

1. Clears BUS SACK/BUS BUSY if set and sets HALT REQUEST
2. When HALT BUSY is active, sets 777707 → Bus Address Register
3. Bus Address Register → Unibus Address
4. Assert MSYN

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μ s, the transfer is aborted and the BUS ERR indicator is set.

5. Unibus Data → Temporary
6. Temporary → Display

CNTRL-CONT

1. Clears BUS SACK and BUS BUSY.
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL-BOOT

1. Sets and clears BOOT signal
2. Switch Register Image → Display
3. Set SR DISP indicator.

CNTRL-START

1. 777707 → Bus Address Register with C1 = 1
2. Bus Address Register → Unibus Address
3. Unibus Address Pointer → Switch Register
4. Switch Register → Unibus Data
5. Assert MSYN.

NOTE

Console waits for BUS SSYN to be returned. If SSYN does not occur within 20 μ s, the transfer is aborted and the BUS ERR indicator is set.

6. Switch Register Image → Switch Register
7. Assert BUS INIT for 150 ms.
8. Switch Register Image → Display
9. Set SR DISP indicator.

CNTRL-7

1. Unibus Address Pointer + Temporary + 2 → Temporary

CNTRL-6

1. Temporary + Switch Register Image → Temporary

CNTRL-1

1. Set maintenance indicator.
2. MPC Lines (sampled) → Display

5.2.2 Maintenance Mode Key Functions

CLR

1. Clears indicators.
2. Clears manual clock enable, if set.
3. Goes to halt condition.

DIS AD

1. Unibus Address (sampled) → Display

EXAM

1. Unibus Data (sampled) → Display

HLT/ISS

1. Sets manual clock enable.
2. Clears BUS SACK and BUS BUSY.
3. MPC (sampled) → Display

CONT

1. Sets and clears manual clock
2. MPC (sampled) → Display

BOOT

1. Sets and clears BOOT signal.

START

1. Clears manual clock enable, if set.
2. MPC (sampled) → Display

No. 5

1. Sets TAKE BUS signal, forcing console to assert BUS BUSY.

5.3 DETAILED LOGIC DESCRIPTION

5.3.1 Clock Circuitry

The M7859 Interface board is driven by an MC 4024 (E42) 1-MHz clock (drawing CS M7859-0-1, sheet 2). The 1-MHz output at E42-8 is toggled down to two nonoverlapping 500-kHz pulses at E12-5, 6, and E30, and these pulses are applied to the microprocessor (E18) input as 01 and 02. The 02 clock, designated as KY1 CK2 H and KY1 CK2 L, is also used as a control pulse to clear system registers and together with the sync pulse to define the end of a timing cycle.

Figure 5-1 shows the relation between the two clock pulses.

5.3.2 Power-Up Logic/Interrupt (Drawing CS M7859, Sheet 2)

The power-up logic/interrupt circuitry is comprised of E1-6, E40-10, E1-4, E36, E12, E29-1, E6, and E26. These elements sense when the system turns on, generate the interrupt to the microprocessor needed to start it, and clear registers to force program startup at location 0.

BUS DC LO at E1-3 initiates the function by clearing E36 which is configured as an 8-bit counter and generates KY1 PUP 1 L. This signal is routed to the Unibus control, indicator control, switch register, and bus address register as a master clear line. The address register is provided with its own clear line, KY1 ADR CLR L.

BUS DC LO L puts the microprocessor in the STOP state. The counter starts counting in the STOP state (E6, E36). KY1 STOP L and KY1 C2 L at E29-1 clock E6. E6 is a divide by two on the clock, while E36 counts from 0-7. Sixteen clock periods are thus counted. At the transition of E36 from 7 to 0, the interrupt is generated at E12-8 and the microprocessor goes into the TII state (Interrupt). KY1 TII L and KY1 CK2 L then reset E12 and clear the address register via E6-6 and the system is initialized.

5.3.3 Microprocessor (Drawing CS M7859, Sheet 2)

The 8008 Microprocessor Chip (E18) was discussed in detail in Chapter 3. According to drawing CS M7859, sheet 2, the unit communicates over an 8-bit bidirectional data bus via 8833 tristate transceivers E16 and E17, with the satellite logic of the interface module. A single interrupt line is received from the power-up logic to initiate microprocessor operations. Driven by a 2-phase, 500-kHz clock (Figure 5-1), the element yields a 3-bit state output code, S0, S1, and S2, plus a sync pulse, to drive a 7442 Timing Phase Decoder. The latter element provides eight separate timing cycles for the sequencing of interface module data transfers and other discrete operations.

5.3.4 Timing State Decoder

The timing state decoder (E23) receives the state outputs S0, S1, and S2 from the microprocessor and generates the timing states for the interface modules (drawing CS M7859, sheet 2). This unit is a 7442 4-line to 10-line decoder, with two unused outputs, that yields an 8-output sequence according to its 3-input state code. State control coding is presented in Chapter 3. State control inputs are determined in the microprocessor and depend on an internal 5-bit feedback shift register with the feedback path controlled by the instruction being executed.

5.3.5 Address Register (Drawing CS M7859, Sheet 2)

The address register, the principal buffer between the microprocessor and the remainder of the interface module logic, consists of four 74175 quad, D-type, double rail output latches. The low order bits are handled by E5 and E4 which generate KY1 ADRD 0 L through KY1 ADRD 3 L (E5) and their complements (for RAM addressing), and KY1 ADRD 4 H through KY1 ADRD 7 H (E4), respectively. This 8-bit byte is the low order unit of the address or data with E10 and E28 containing the high order information ADRD 08-13 and PC FUN 1 and 0.

The data contained in the address register is routed to the following locations according to direction by the stored program:

1. ROM (address of next instruction) (KY1 ADRD 0 L → KY1 ADRD 8 L plus ROM 1 EN L or ROM 2 EN L)
2. RAM (address of data to be read or written) (KY1 ADRD 0 L → KY1 ADRD 3 L)
3. Unibus Control (KY1 ADRD 0 H → KY1 ADRD 3 H)
4. Indicator Control (KY1 ADRD 4 H → KY1 ADRD 7 H)
5. Data Bus Control (KY1 ADRD 9 H → KY1 ADRD 13 H, KY1 PC FUN 0 H, KY1 PC FUN 1 H)
6. Switch Register (KY1 ADRD 0 H → KY1 ADRD 7 H)
7. Bus Address Register (KY1 ADRD 0 H → KY1 ADRD 7 H)

The address register is loaded with a low order byte (E4 and E5) by signal KY1 LD AD 1 H, generated by AND E22-12 at time state TS1. The high order byte is gated in E28 and E10 by KY1 LD AD 2 H generated at E22-6 at timing state TS2.

5.3.6 ROM

The interface module ROM consists of E3, E21, E33, and E39 (drawing CS M7859, sheet 3). The four 512-word by 4-bit elements are addressed so that the ensemble looks like two 512- X 8-bit RMs. E3 and E21 are activated by KY4 ROM 1 EN L, and E33 and E39 by KY4 ROM 2 EN L. Address bits KY1 ADDR 0 H through KY1 ADDR 8 H are routed to all four ROM elements with the enable 1 or 2 determining the address activated and thus yielding 1024 8-bit locations. Outputs are wire ORed with various inputs to give the KY2 DIN 0 H through KY2 DIN 7 H inputs to the tristate transceivers, E16 and E17.

The ROM 1 or RM 2 enables are generated by the data bus control logic.

5.3.7 RAM

The scratchpad RAM consists of E11 and E27 (drawing CS M7859, sheet 3). These units effectively comprise a 16-word by 8-bit read/write memory, and serve as working storage for the microprocessor programs in storing addresses and data. Data is routed to the RAM (KY1 DOUT 0 H through KY1 DOUT 7 H) directly from the tristate transceivers of the microprocessor bidirectional data bus during RAM write operations. The 4-bit address lines KY1 ADDR 0 L through KY1 ADDR 3 L specify the address to be read from or written into during read/write.

Selection of the RAM for read or write is determined by the stored program via the data bus control. Either KY4 RAM → DIN BUS L or KY4 RAM WRITE H must be true to select the RAM. Output lines are wire ORed with various other microprocessor input ports to be routed to the 8833 tristate transceivers.

5.3.8 Switch Register (Drawing CS M7859, Sheet 6)

The switch register contains the 16-bit data used and consists of four 74175 quad, D-type, double rail output latches. The four elements comprising the register are E9, E19, E2, and E15. These units feed the 8641 bus transceivers E7, E25, E8, and H13 (respectively). Incoming 16-bit data (KY5 BB D00 H through KY5 BB D15 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control. Outgoing data (BUS D00 L through BUS D15 L) is gated by KY4 EN DB L, a signal generated in the switch register address decoding logic (sheet 5).

The switch register is addressable from the Unibus as address 777570 as described in Paragraph 5.3.9.

5.3.9 Switch Register Address Decode Logic (Drawing CS M7859, Sheet 5)

The switch register address decoding logic allows the Unibus to address the switch register via a decoding of address 777570. The logic has two outputs:

1. BUS SSYN L
2. KY4 EN DB → BUS L

K44 EN DB → BUS L at F43-10 gates the data lines onto the Unibus (CS M7859, sheet 6) while the assertion of BUS SSYN L designates that the slave device has completed its part of the data transfer. The second stage of the address decode at E32 is gated by assertion of BUS MSYN L at E32-10. Assertion of MSYN requests that the slave defined by the A (address) lines perform the function required by the C lines. In this case, KY7 BB C1 H at inverter F40-9 specifies that the data is to be transferred to the Unibus data lines.

5.3.10 Bus Address Register (Drawing CS M7859, Sheets 7 and 8)

The bus address register consists of five 74175 quad, D-type, double rail output latches. The five elements comprising the register are E67, E57, E73, E58, and E51. Input to the bus address register is from the address register (KY1 ADRD 0 H through KY1 ADRD 7 H). Outputs are routed to the display and keypad logic and to the 8641 Unibus transceivers E61, E56, E65, E55, and E50.

A Unibus address is enabled to the Unibus via the bus address transceivers from the bus address register by KY7 EN AR L generated at E51-11. The switch register is available to the Unibus as address 777570 via the bus address transceivers and the switch register decode logic. The latter function is discussed in Paragraph 5.3.9.

E67 and E57 contain the keypad scan signals (KY6 SCAN 1 L through KY6 SCAN 6 L) while E73 drives the display (KY6 NUM 1 H through KY6 NUM 3 H).

Incoming 18-bit address information (KY6 BB A00 H through KY7 BB A17 H) is applied to the 8093 tristate buffers and gated by an appropriate read line from the data bus control.

5.3.11 Data Bus Control Logic (Drawing CS M7859, Sheet 5)

The data bus control directs the reading and loading of the various interface module registers, the reading of the ROMs, and the reading/writing of the RAM. It also determines the direction of data flow in the interface module and between the interface module and the Unibus, i.e., whether data will be read from or be routed to the Unibus. A list of I/O functions and associated select signals follows:

Select Signal	Function
READ INPUT 0 L READ INPUT 1 L	UNIBUS DATA
READ INPUT 2 L READ INPUT 3 L READ INPUT 4 L	UNIBUS ADDRESS
READ INPUT 5 L	KEYPAD REG
READ INPUT 6 L READ INPUT 7 L	MAINTENANCE
LD REG 0 H LD REG 1 H LD REG 2 H	BUS ADDR REG
LD REG 3 H LD REG 4 H	SWITCH REG
LD REG 5 H	UNIBUS CONT LOGIC
EN ROM 1 L EN ROM 2 L	ROM SELECT
RAM WRITE H	RAM WRITE
RAM DIN BUS L	ENABLE RAM DATA
DIN DRIVERS DIS H	DISABLE DATA IN

Specifically, the data bus control logic decodes memory references into three areas (ROM 1, ROM 2, and RAM) and determines whether the access is a read or write. The logic also decodes I/O instructions and generates loading or gating signals depending on the direction of data transfer and the port selected.

In order to facilitate understanding of the logic, the following explanation of memory address allocation and I/O instruction operation is included.

ROM 2 (E33 and E39)

Memory addressing space spans locations 0 through 777.

ROM 1 (E3 and E21)

Memory addressing space spans locations 4000 through 4777.

RAM (E11 and E27)

Memory addressing space spans locations 20000 through 20017.

The two bus control signals provided by the microprocessor and latched with the upper byte of the address register, KY1 PC FUN 0 H and KY1 PC FUN 1 H, determine data transfer direction and I/O operations. The following table explains the decoding of these signals.

PC FUN 0	PC FUN 1	
L	L	Memory read of first byte of instruction only (fetch)
L	H	Memory read of additional bytes of instruction or data.
H	H	Memory write (used only to write into RAM).
H	L	I/O operation

Memory reads and writes signify that the address register (KY1 ADDR 0 H through KY1 ADDR 13 H) contains the address of the location in memory to be accessed.

The code for I/O operations, however, signifies a very different situation. This is due to the following occurring after the initial instruction fetch cycle:

1. During TS1 the content of the A register (accumulator) in the microprocessor is available on the data lines and is latched into the low byte of the address register.
2. During TS2 the content of the instruction register (containing the I/O instruction) is available on the data lines and is latched into the high byte of the address register.
3. During TS3 of an INP (input) instruction, data on the data lines is loaded into the A register. On OUT (output) instructions, the data is strobed out of the low byte of the address register.

I/O Instruction Code:

```
INP 01 00MMM1
OUT 01 RRMMM1
```

Note that the two most significant bits of the instruction will correspond to PC FUN 0 = 1 and PC FUN 1 = 0 when loaded into the high byte of the address register, thus denoting an I/O operation. Therefore, the data bus control logic determines whether to gate data into the microprocessor during TS3 (INP) or to load the data from the low byte of the address register into an output port during TS3 (OUT).

The 32 x 8 PROM (E34) does the initial decoding of the type of transfer (read, write, or I/O) from the signals KY1 PC FUN 0 H and KY1 PC FUN 1 H. If the transfer is a memory read or write, it is decoded into one of the following four signals. KY4 RAM → DIN BUS L (RAM read), KY4 ROM 1 EN L (memory read in address range 4000-4777), KY4 ROM 2 EN L (memory read in address range 000-777), and an enable which is ANDed with KY1 SYNC H, KY1 TS3 L, and KY1 CK2 L to provide a write pulse, KY4 RAM WRITE H, to the RAM.

Another enable from the PROM is ANDed with KY1 TS3 L to provide the signal KY4 DIN DRIVER DIS H. This signal is normally high, disabling the driver portions of the 8833 transceivers (E16 and E17). It will be low only during TS3 and when data transfer is into the microprocessor.

Two other outputs of the PROM are used for I/O operations. One output of the PROM (E34-7), when low, enables the 74154 4-to-16 decoder on all I/O instructions. The second output (E34-9) determines whether the I/O instruction is INP or OUT. If the instruction is OUT, then the signal will be high.

Note that address register bits KY1 ADDR 11, KY1 ADDR 10 H, and KY1 ADDR 9 H, are applied to the low order inputs of the 74154. This selects which of the possible ports will be used. The fourth input, the highest order input, determines if it is an INP or OUT instruction. This input is the ANDed condition of the PROM output (E34-9), KY1 SYNC H, KY1 TS3, and KY1 CK2. Thus, if the instruction is an INP, then the input gating signal will be one of the lower order eight outputs of the 74154 (KY4 READ IN 0 L through KY4 READ IN 7 L).

If the PROM signal (E34-9) is high, signifying an OUT instruction, then initially a low order output is selected (does not substantially affect anything) and then a high order output will be pulsed as the gated clock pulse is applied to the high order input of the 74154. Thus, the high order outputs are pulsed and buffered to provide loading pulses to the selected registers (KY4 LD REG 0 H, etc.).

5.3.12 Unibus Control (Drawing CS M7859, Sheet 5)

Unibus control is accomplished via two 74175 quad, D-type, double rail output latches, E52 and E64. The stored program input bit configurations are read in under control of an appropriate data bus control signal, LD REG 5 H. E64 D2 and D3 latches are utilized for the manual clock enable and manual clock lines while the other six lines are Unibus control signals.

5.3.13 Keypad Scan Logic (Drawing CS 5411800-0-1)

The logic and driving circuitry for the keypad and display elements is located on a circuit board in the rear of the programmer's console panel.

Scan signals for the keypad are generated at the interface module (bus address register). These six lines (KY6 SCAN 1 L through KY6 SCAN 6 L) are then routed through hex 7417 buffer drivers to the console circuit board where they are designated as READ and DRIVE signals. As indicated by CS 5411800-0-1, sheet 2, READ 1 through READ 5 signals continuously scan the keypad in groups of 4. As each READ signal is applied to check for a pressed key, a corresponding DRIVE signal is simultaneously generated and applied to the appropriate transistor in the LED display circuitry (CS 11800-0-1, sheet 3).

A pressed key thus results in activation of 1 to 4 lines. This information is routed out through J1 to the interface module and applied to the data bus for eventual read-in to the microprocessor.

5.3.14 Indicator Logic (Drawing CS M7859, Sheet 5)

The indicator control consists of a single quad, D-type, latch configuration, 74175 (E68) and four 7417 open collector inverters (E69) for driving the panel indicators. Input bit coding KY1 ADDR 4 H through KY1 ADDR 7 H via the stored program determines which of the following panel indicators are turned on:

1. BUS ERR
2. SR DISP
3. MAINT
4. BOOT

5.3.15 Halt Logic (Drawing CS M7859-0-1, Sheet 9)

The halt logic allows the console to obtain control of the Unibus in order to perform Unibus transactions. Control of the Unibus is passed to the KY11-LB from the PDP-11 processor via a HALT REQUEST and HALT GRANT sequence. Use of the HALT/SS key initiates a program sequence within the KY11-LB to issue a HALT REQUEST to the PDP-11 processor. The processor will arbitrate the request and at the appropriate time will respond with HALT GRANT. The reception of HALT GRANT H by the halt logic direct sets the HALT SACK flip-flop on E63-4, causing BUS SACK L to be generated at E62-13. The set output of the HALT SACK flip-flop (E63-5) sets up the data input of the HALT BUSY flip-flop (E63-12).

The reception of BUS SACK L by the PDP-11 processor will cause it to drop HALT GRANT H. When the Unibus becomes free (unasserted BUS BUSY L and BUS SSYN L), the E63-11 will be clocked, setting the HALT BUSY flip-flop. This, in turn, asserts BUS BUSY L through E62-10 and causes the RUN indicator to be turned off via the 7417 buffer (E66-12). This logic operates in the same manner if the HALT GRANT is generated not by a HALT REQUEST from the KY11-LB but by a HALT instruction in the PDP-11 processor. The output of the HALT BUSY flip-flop (KYB HALT BUSY H) can be tested by the microprocessor program to check if the console has control of the Unibus before performing Unibus transactions.

The HALT SACK and HALT BUSY flip-flops are direct cleared by either BUS INIT L from the Unibus or by the signal KY4 CLR BUS L which can be generated by the microprocessor program. Clearing these flip-flops relinquishes control of the Unibus to the PDP-11 processor.

The signal KY4 TAKE BUS L, which can direct set the HALT BUS flip-flop, allows the microprocessor program to perform Unibus operations without first obtaining the Unibus through a legal request. This signal is only used during maintenance mode operation of the KY11-LB to bypass a failing or hung processor.

5.3.16 Buffers (Drawing CS M7859, Sheet 4)

5.3.16.1 Tristate Buffers (8093) - The following units, which are gated by read input signals from the data bus control, buffer input data from several sources.

1. Unibus Data
2. Unibus Address
3. Keypad Register
4. Maintenance Inputs (from processor microprogram counter).

Outputs from the 8093s are wire ORed and sent to the tristate transceivers with the ROM and RAM data as KY2 DIN 0 H through KY2 DIN 7 H.

5.3.16.2 Tristate Transceivers (8833) - These units buffer data between the microprocessor bidirectional data bus and the satellite logic of the interface module.

CHAPTER 6 CONSOLE MODE OPERATION

6.1 INTRODUCTION

This chapter is a recapitulation of all console key and indicator functions. Operation, use, and examples of the utilization of each key are presented. Key operations are divided into console mode and maintenance mode. Examples of console sequences to demonstrate the proper use of the KY11-LB are presented together with further notes and hints on operation.

6.2 CONSOLE KEY OPERATIONS

This section describes the operation of each key in a step-by-step procedure. The reader is assumed to have read earlier chapters as some descriptions include the use of keys previously described.

A notation for each key will be introduced in each description and is enclosed in angle brackets < >. These notations are used extensively in Paragraph 6.4 to describe various sequences of key operations.

<CLR> - Used to clear an incorrect entry or existing data.

1. Press and release the CLR key.
2. The display (six digits) will be all zeros.
3. Clears the SR DISP, BUS ERR, or MAINT indicators if on.

Numerics 0-7 - Used to key in an octal numeric digit (0 through 7).

1. Press a numeric key (0 through 7).
2. The corresponding digit will be left shifted into the 6-digit octal display with the previously displayed digits also being left shifted.
3. Release the numeric key.

To enter the number <xxxxxx>, e.g., 123456:

1. Press and release the CLR key (000000 will be displayed).
2. Press and release the 1 key (000001 will be displayed).
3. Press and release the 2 key (000012 will be displayed).
4. Press and release the 3 key (000123 will be displayed).
5. Press and release the 4 key (001234 will be displayed).
6. Press and release the 5 key (012345 will be displayed).
7. Press and release the 6 key (123456 will be displayed).

The number has now been entered. Leading zeros do not have to be entered.

<LSR> - Used to load the switch register (accessible as Unibus address 777570).

1. Press and release the LSR key.
2. The display will show the data loaded and the SR DISP indicator will be on.

To load the number 777 i.e., **<LSR 777>**, into the switch register:

1. Press and release the CLR key.
2. Key in the number 777.
3. Press and release the LSR key.
4. 777 will be displayed and the SR DISP indicator will be on.

<LAD> - Used to load the Unibus address pointer prior to performing an EXAMINE, DEPOSIT, or START.

1. Press and release the LAD key.
2. Display will be all zeros.

To load address 200, i.e., **<LAD 200>**:

1. Press and release the CLR key.
2. Key in 200.
3. Press and release the LAD key.
4. Display is all zeros.

<DIS AD> - Displays the current contents of the Unibus address pointer.

1. Press and release the DIS AD key.
2. Display will show the current Unibus address pointer.

To perform the sequence:

LAD 400
DIS AD

1. Press and release the CLR key.
2. Key in 400.
3. Press and release the LAD key (display is all zeros).
4. Press and release the DIS AD key.
5. Display shows the 400 from the Unibus address pointer.

<DEP> - Used to deposit a number into the location pointed to by the Unibus address pointer.

1. Processor must be halted (RUN indicator off); otherwise key is ignored.
2. Press and release the DEP key.
3. Display shows the data deposited.

To deposit <DEP XXX> (e.g., 5252) into location 1000, the sequence is as follows:

LAD 1000
DEP 5252

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Key in 5252.
5. Press and release the DEP key.

<EXAM> - Used to examine the contents of a location pointed to by the Unibus address pointer.

1. Machine must be halted.
2. Press and release the EXAM key.
3. Display shows the contents of the location examined.

To examine general-purpose register R7 (program counter) at Unibus address 777707, the following sequence is used:

LAD 777707
EXAM

1. Press and release the CLR key.
2. Key in 777707.
3. Press and release the LAD key.
4. Press and release the EXAM key.
5. The contents of R7 will be displayed.

<CNTRL> - The CNTRL key is always used in conjunction with some other key. When it is used it must be pressed and held down while the second key is pressed and released:

<CNTRL-HLT/SS> - Used to halt the processor.

1. Press and hold down the CNTRL key.
2. Press and release the HLT/SS key.
3. Display will show the current contents of R7 (program counter) and the RUN indicator will be off.
4. Release the CNTRL key.

If the processor is already halted, the use of the HLT/SS key will single-instruction step the processor. (The CNTRL key is not required to single-instruction step the processor once halted.)

1. Press and release the HLT/SS key.
2. Processor will perform one instruction and halt.
3. Display will show the new current contents of R7 (program counter).

<CNTRL-CONT> - Used to allow the processor to begin running from a halt.

1. Press and hold down the CNTRL key.
2. Press and release the CONT key.
3. Processor will run unless a program halt instruction is encountered. The RUN and SR DISP indicators should be on and the contents of the switch register should be displayed. If a halt instruction was encountered, the indicators will be off and the program counter will be displayed.
4. Release the CNTRL key.

NOTE

If the processor is already running, use of <CNTRL-CONT> will result in the switch register being displayed; there will be no other effect on the processor.

<CNTRL-BOOT> - Used to initiate running of M9301 Bootstrap program.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the BOOT key.
4. Processor should start running (RUN indicator on) the bootstrap program selected on the M9301.

NOTE

For more information concerning the M9301 Bootstrap program, consult the system users guide.

5. Release the CNTRL key.

<CNTRL-START> - Used to start the processor running a program from a given starting address.

1. Processor must be halted; otherwise key is ignored.
2. Press and hold down CNTRL key.
3. Press and release the START key.
4. RUN indicator will be on unless a halt instruction is encountered. The SR DISP indicator should also be on and the contents of the switch register should be displayed.
5. Release the CNTRL key.

To start running a program at location 1000, the following sequence is used:

1. Press and release the CLR key.
2. Key in 1000.
3. Press and release the LAD key.
4. Press and hold down the CNTRL key.
5. Press and release the START key.
6. Release the CNTRL key.

<CNTRL-INIT> - Generates a Bus Initialize without the processor starting.

1. Processor must be halted.
2. Press and hold down the CNTRL key.
3. Press and release the INIT key.
4. Bus Initialize will be generated for 150 ms.
5. Release the CNTRL key.

<CNTRL-7> - Used to calculate the correct address when a mode 6 or 7 register R7 instruction is encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 7 key.
3. Display will show the new temporary register which contains the old temporary register plus the Unibus address point or plus 2.

See Paragraph 6.4 for an example.

<CNTRL-6> - Used to calculate the offset address when mode 6 or 7 instructions other than register R7 are encountered.

1. Press and hold down the CNTRL key.
2. Press and release the 6 key.
3. Display shows the new temporary register, which contains the old temporary plus the switch register.
4. Release the CNTRL key.

See Paragraph 6.4 for an example.

<CNTRL-1> - Used to enter the console into maintenance mode. Maintenance mode should only be used as an aid to troubleshooting hardware problems. Maintenance mode provides no help in debugging software problems.

1. Press and hold down the CNTRL key.
2. Press and release the 1 key.
3. MAINT indicator will be on and the MPC (microprogram counter) will be sampled and displayed.
4. Release the CNTRL key.

6.3 NOTES ON OPERATION

An erroneous display will result if, while the processor is running and the switch register is being displayed, a numeric key is pressed. Although the SR-DISP indicator will remain on, the display no longer reflects the actual contents of the switch register. If at any time while the processor is running, it is desired that the switch register contents be displayed, the CNTRL-CONT keys should be used.

As a general practice, prior to entering a new 6-digit number and if the display is nonzero, the CLR key should be used to initially zero the display.

In order to single-instruction step the processor from a given starting address, the program counter (R7) must be loaded with the starting address using the Unibus address of R7 (777707) i.e., to single-instruction step from the beginning of a program starting at location 1000, the following sequence is necessary:

```
LAID 777707
DEP 1000
CNTRL-INIT (if desired)
HLT/SS
HLT/SS
etc.
```

The console requires an 18-bit address. This is especially important to remember when accessing device registers (i.e., 777560 instead of 177560). Otherwise an erroneous access to memory or to a nonexistent address will occur.

The Unibus addresses for the general-purpose registers can only be used by the console. A PDP-11 program using the Unibus addresses for the general-purpose registers will trap as a nonexistent address. Also, internal registers R10 through R17, which are used for various purposes (depending upon processor), may be accessed by the console through Unibus addresses 777710 through 777717.

The BUS ERR indicator on the console reflects a bus error by the console only. The indicator will not reflect bus errors due to other devices such as the processor.

6.4 EXAMPLES OF CONSOLE SEQUENCES

This section combines key operations with example sequences to demonstrate the proper use of the KY11-LB Programmer's Console.

The following sequences use the notations for key operations as described in Paragraph 6.2.

The angle brackets < > will be used in the sequences to identify the display contents after the operation is performed, i.e., LAD 200 <0>

1. Press and release the CLR key.
2. Press and release 2 key.
3. Press and release 0 key.
4. Press and release 0 key.
5. Press and release the LAD key.
6. 000000 will be displayed in the 6-digit readout.

Example 1

This sequence uses the examine function and the switch register Unibus address 777570 to read the contents of the switch register.

LSR 123456	<123456>
LAD 777570	<0>
EXAM	<123456>
DIS AD	<777570>
LSR 777	<777>
EXAM	<777>

Example 2

This sequence demonstrates the use of the following keys: LAD, DIS AD, LSR, EXAM, DEP, CNTRL-START, CNTRL-CONT, and CNTRL-HLT/SS.

This example loads the following program into memory, which is then run to demonstrate various operations.

Program	Memory Location/Contents
1000/13737	;Move the contents of
1002/177570	the switch register to
1004/1014	memory location 1014
1006/00100	;Halt
1010/137	;Jump to location 1000
1012/1000	
1014/0000	

Sequence

LAD 1000	<0>
DEP 13737	<13737>
DEP 177570	<177570>
DEP 1014	<1014>
DEP 0	<0>
DEP 137	<137>
DEP 1000	<1000>
DEP 0	<0>
LAD 1000	<0>
EXAM	<13737>
EXAM	<177570>
EXAM	<1014>
EXAM	<0>
EXAM	<137>
EXAM	<1000>
EXAM	<0>
DIS AD	<1014>
LSR 123456	<123456>
LAD 1000	<0>
CNTRL-START	<1010>
LAD 1014	<0>
EXAM	<123456>
DEP 0	<0>
EXAM	<0>
DIS AD	<1014>
LSR 125252	<125252>
CNTRL-CONT	<1010>
LAD 1014	<0>
EXAM	<125252>
DEP 0	<0>
LAD 1006	<0>
DEP 240	<240>
EXAM	<240>
LAD 1000	<0>
CNTRL-START	<125252>
LSR 70707	<10707>
CNTRL-HLT/SS	
LAD 1014	<0>
EXAM	<10707>
HLT/SS	
HLT/SS	
HLT/SS	
.	
.	
.	
LSR 05252	<052525>
HLT/SS	
LAD 1014	<0>
EXAM	<052525>

Example 3

This sequence demonstrates the use of CNTRL-7 and CNTRL-6. The following data are loaded into memory:

100H/177
1002/100
1004/000
1006/5060
1010/1020

1104/1106

RO = 777760

The sequence to load the data is as follows:

LAD 1000	<0>
DEP 177	<177>
DEP 100	<100>
DEP 0	<0>
DEP 5060	<5060>
DEP 1020	<1020>
LAD 1104	<0>
DEP 1006	<1006>
LAD 777700	<0>
DEP 777760	<777760>

Sequence

LAD 1000	<0>
EXAM	<177>
EXAM	<100>
CNTRL-7	<1104>
LAD	<0>
EXAM	<1006>
LAD	<0>
EXAM	<5060>
EXAM	<1020>
LSR	<1020>
LAD 777700	<0>
EXAM	<777760>
CNTRL-6	<100006>
LAD	<0>
EXAM	<177>

CHAPTER 7

MAINTENANCE MODE OPERATION

7.1 INTRODUCTION

This chapter covers the keypad facilities of the programmer's console available for hardware maintenance of the processor.

7.2 MAINTENANCE MODE KEY OPERATIONS

The following definitions apply to a subset of the same keys used in console mode; however the functions and operations differ from those in console mode. In general, console mode functions are not available while in maintenance mode, and many keys have no function in maintenance mode.

NOTE

Maintenance mode operation is indicated by the
MAINT indicator being on.

In order to use the hardware maintenance features available in maintenance mode, the maintenance cable (11/04) or cables (11/34) must be connected between the KY11-LB interface board (M7859) and the corresponding processor board (M7263-11/04, M7266-11/34, M8266-11/34A, or M8267-TP11A). An exception to this is the 5 (maintenance mode) operation which allows the console to examine or deposit into memory or device registers without the processor being either present or functional.

DIS AD (Maintenance Mode) - Used to display Unibus address lines.

1. Press and release the DIS AD key.
2. Unibus address lines will be sampled (read once) and displayed, i.e., display will not be updated as address lines change.

EXAM (Maintenance Mode) - Used to display Unibus data lines.

1. Press and release the EXAM key.
2. Unibus data lines will be sampled and displayed.

HLT/SS (Maintenance Mode) - Asserts manual clock enable and displays MPC (microprogram counter).

1. Press and release the HLT/SS key.
2. Manual clock enable will be asserted.
3. MPC will be sampled and displayed.

CONT (Maintenance Mode) - Single microsteps the processor through one microstate and displays the MPC.

1. Press and release the **CONT** key.
2. Manual clock will be pulsed.
3. New MPC will be sampled and displayed.

BOOT (Maintenance Mode) - Boots the M9301. If manual clock enable is asserted, the M9301 routine will not be entered but because the M9301 simulates a power fail the processor will power up through location 24.

1. Press and release the **BOOT** key.
2. The display is not affected. If manual clock enable is asserted, the MPC is now at the beginning of the power-up sequence. To see the new MPC, use the **HLT/SS** key.

START (Maintenance Mode) - Drops manual clock enable.

1. Press and release the **START** key.
2. Manual clock enable is released.
3. MPC will be sampled and displayed.

CLR (Maintenance Mode) - Returns console to console mode operation.

1. Press and release the **CLR** key.
2. **MAINT** indicator is off.
3. Processor should halt.
4. Program counter should be displayed.

5 (Maintenance Mode) - Allows the console to take control of the Unibus if a processor is not in the system.

1. Press and release the **5** key.
2. The **MAINT** indicator will be off (console mode operation now).
3. Console attempts to read the program counter which is not present and therefore the **BUS ERR** indicator will be on.

7.3 NOTES ON OPERATION

If the single-microstep feature in maintenance mode is to be used, it is preferable that the processor be halted prior to entering maintenance mode, if it is possible. This is because the assertion of manual clock enable, which turns off the processor clock if it is running, cannot be synchronized with the processor clock. Therefore, if the processor is not halted, the clock may be running and the assertion of manual clock enable may cause an erroneous condition to occur.

In order to single-microstep the processor from the beginning of the power-up sequence, the following steps may be used:

1. Halt the processor if possible.
2. Use **CNTRL 1** to enter maintenance mode.
3. Use **HLT/SS** to assert manual clock enable (**RUN** indicator should come on).
4. Use **BOOT** to generate a simulated power-fail (will not work if M9301 is not present in the system).

5. Use HLT/SS to display the MPC (microprogram counter) for the first microstep in the power-up routine.
6. Use CONT to single-microstep the processor through the power-up routine. (The new MPC will be displayed at each step.)
7. Unibus address lines and Unibus data (see NOTE below) lines may be examined at any microstep by using DIS AD and EXAM, respectively. Use of these keys does not advance the microprogram. To redisplay the current MPC without advancing the microprogram, use the HLT/SS key.
8. To return from maintenance mode, use the CLR key.
9. To single-microstep through a program, the program counter (RT) must first be loaded with the starting address of the program as in single-instruction stepping the processor prior to entering maintenance mode.

NOTE

Because the data transfer occurs asynchronously with the processor clock, Unibus data will not be displayed on DATI in maintenance mode when using the console with an 11/04 processor. Unibus data on DATO on the 11/04 and both DATI and DATO on the 11/34 will be displayed.

Due to hardware changes, the M8266 module will gate the AMUX lines onto the Unibus when manual clock enable is asserted and a Unibus transaction is not occurring.

CHAPTER 8 KY11-LB MAINTENANCE

8.1 PRELIMINARY CONSIDERATIONS

The following is a guide to locating possible problems on the KY11-LB.

1. Power Switch Failure - If the power switch fails to control the power supply, check cable 7011414-2-2 (BA11-L) at J2 or cable 7011992-0-0 (BA11-K) at Faston tabs TB4 and TB5 on the bezel-mounted board to ensure that cable(s) are securely and correctly installed.
2. If the power switch does turn on the power supply (fans turn) but the DC ON indicator does not come on, check cable 7011992-0-0 (BA11-K) at tabs TB6 and TB7 on the bezel-mounted board.
3. If the four indicators on the left side of the keypad are all on, then the cable 7012214-0-0 connecting the bezel-mounted board to the interface board (M7859) is probably plugged in backward on one end.
4. If no display and none of the four indicators are on, then check cable 7012214-0-0 at J1 on the bezel-mounted board and M7859 board to ensure that it is correctly and securely installed.
5. Note that there should be no cables from either the bezel-mounted board or the M7859 board attached to the backplane. The connection at the backplane is for use by the KY11-LA Operator Console only.
6. If the RUN indicator is on but there is no display and no response from the keypad, the problem is probably at the M7859 Interface module. Check the module to ensure that the microprocessor chip (E18) is securely installed in its socket.
7. If the display works and the console responds to the keypad except for the BOOT key, check that cable 7011413-0-0 is properly connected to the M9301 and to the bezel-mounted board at tabs TB1 and TB2.
8. If the display MPC, single microstep, etc. functions in maintenance mode do not work correctly, check that the cable(s) from J2 and J3 of the M7859 are properly installed.

NOTE

These cables should be installed only for maintenance of the processor. By disconnecting these cables for normal operation, the effect is that the maintenance functions are nonoperative except for the TAKE BUS function.

8.2 M7859 FAILURES

In general, there are two levels of possible failures on the M7859 module. The first level and most difficult to fix is the microprocessor and its support logic which constitutes about 1/3 of the logic. The second level is failures which occur in the peripheral logic constituting the Unibus interface and the display/keypad interface. These are generally easier to troubleshoot.

Generally, a first level failure is readily apparent and will usually be indicated when no display is on and the only indicators on are DC ON and RUN.

A second level failure, although easier to troubleshoot, is not always readily apparent as it may only occur on certain key functions or may be data dependent. A failure on the display/keypad interface would be indicated by odd displays, row, or column failures on the keypad. The Unibus interface can be tested with a good confidence level by loading the switch register with a 123456 data pattern and then reading it back over the Unibus by examining location 777570.

The following is a guide to troubleshooting a failing M7859 module. Generally, the minimum equipment needed is a dual-trace oscilloscope with delayed sweep.

1. Check that 9 V is available at pin 1 of the microprocessor, E18.
2. Check that the clock frequency is $1.0 \text{ MHz} \pm 2\%$ at the test point, TP1. The frequency can be corrected if needed by adjusting the variable resistor at the top of the module.
3. Check that the two clock signals are at E18-15 and K18-16. These clocks should be 500 kHz frequency with nonoverlapping positive pulses of 0.5 μs duration (Figure 8-1).

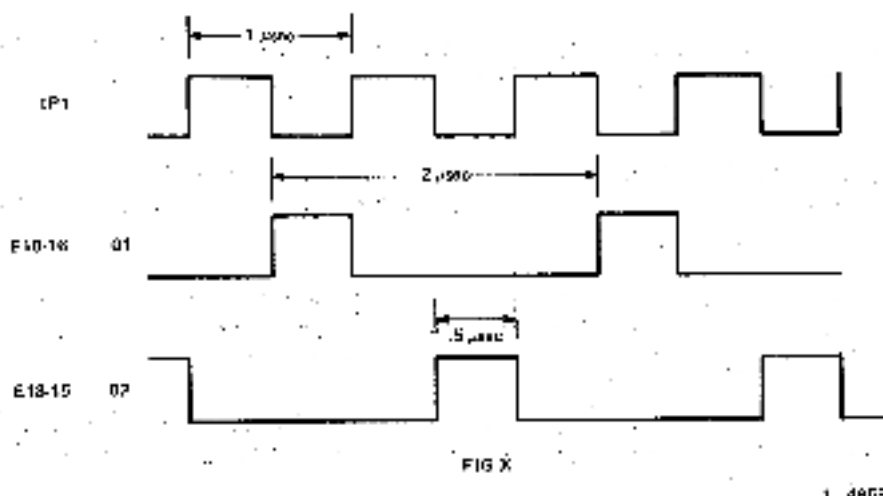


Figure 8-1 Clock Waveforms

4. Check the signal at E18-18 which should be at logic low. If the signal is high the microprocessor may not have responded to the interrupt request on power-up. If the signal is toggling, this may be indicative of a different class of problems discussed in the following paragraphs.
5. The M7859 logic is such that if the microprocessor encounters a HALT instruction and goes to the STOP state, peripheral logic will automatically try to restart the microprocessor from location 0. Hence, if there are problems in the microprocessor support logic, such as address or data failures, time state decoding failures, etc., the microprocessor will not follow the program and generally encounters a HALT instruction.

The general technique to solve this class of problems is to sync off of the signal STOP L and to use delayed sweep to track addresses backward to find the specific failing address. A quick check of the number of times TS1 L is true between the times that STOP L is true will give an idea of how far into the program the failure occurs. In general the easiest technique is to use the TS3 L signal as a visual key on one channel while using the other channel to probe addresses, data, timing signals, etc.

CHAPTER 9

KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programmer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-conductor cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

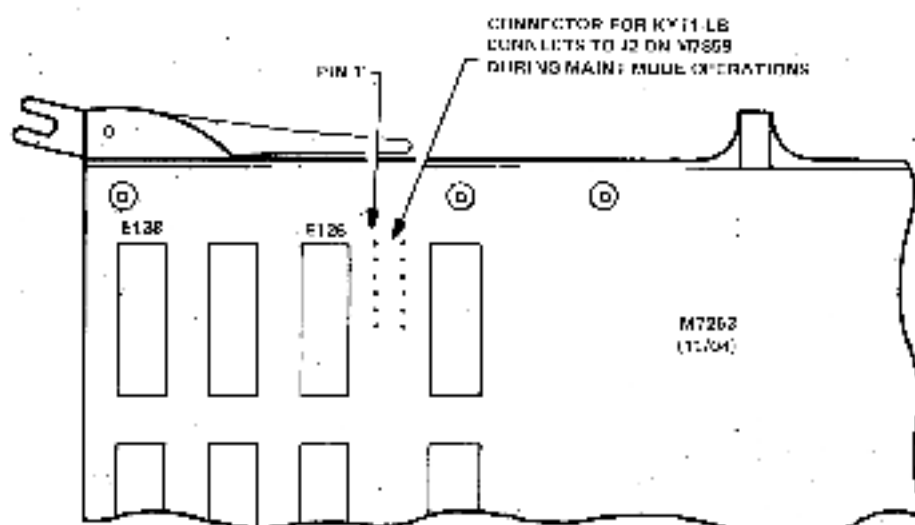
9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

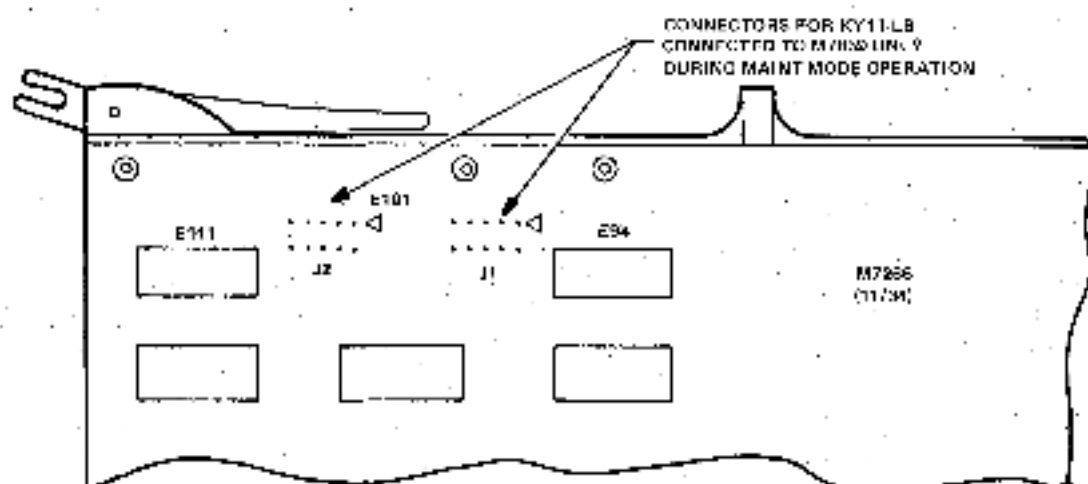
9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.



11-1042

Figure 9-1 M7263



11-1053

Figure 9-2 M7266

CHAPTER 9

KY11-LB INSTALLATION

9.1 KY11-LB DESCRIPTION

The KY11-LB is a programmer's console option for both the 11/04 and 11/34 CPUs. It replaces the KY11-LA (operator's console) which is the standard console on 11/04s and 11/34s. The hardware in the KY11-LB option is exactly the same for both the 11/04 and 11/34. The KY11-LB contains a bezel assembly (consisting of a keypad, 7-segment display, indicator lamps, and ON/OFF switch) and a separate SPC quad interface module (M7859). Also, three loose piece cables: two 10-conductor, 45.7 cm (18 inch) long cables and one 20-conductor cable. The two 10-conductor cables are not required for normal console functions and should only be installed when using the console in maintenance mode.

9.2 CPU BOX TYPE

PDP-11/04s and 11/34s are available in both the BA11-L 13.4 cm (5-1/4 inch) box and BA11-K 26.7 cm (10-1/2 inch) box. The difference between these two boxes creates the only difference in installing the KY11-LB. In all cases, the 10-conductor cable, running from the operator's console to the CPU backplane, is not used and must be removed when the KY11-LB is installed. It is extremely important not to connect this cable to the KY11-LB as a short circuit may result.

9.3 CPU DIFFERENCES

The 11/04 is a single-module CPU (M7263). The 11/34 is a 2-module CPU (M7265 and M7266). Maintenance mode connections between KY11-LB and 11/04 are made on the M7263. Maintenance mode connections between KY11-LB and 11/34 are made on the M7266 (Figures 9-1 and 9-2). Note that all figures in this procedure show the M7266 module (11/34). This is done because the hook-up for normal KY11-LB operation is the same for both CPUs.

To identify cables and part numbers for cables, refer to Figure 9-3.

9.4 BA11-L 13.3 CM (5-1/4 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connections will be to the same tabs on the KY11-LB. The cable from H777 Power Supply plugged into J2 on the KY11-LA will plug into J2 on the KY11-LB. The cable from the CPU backplane to J1 on the KY11-LA must be removed. No connection is made from the backplane to the KY11-LB.

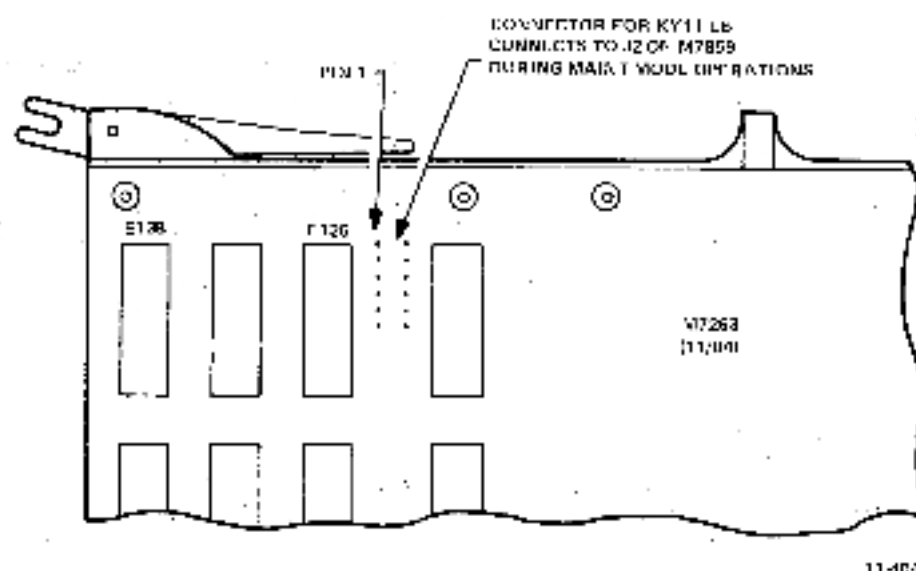


Figure 9-1 M7263

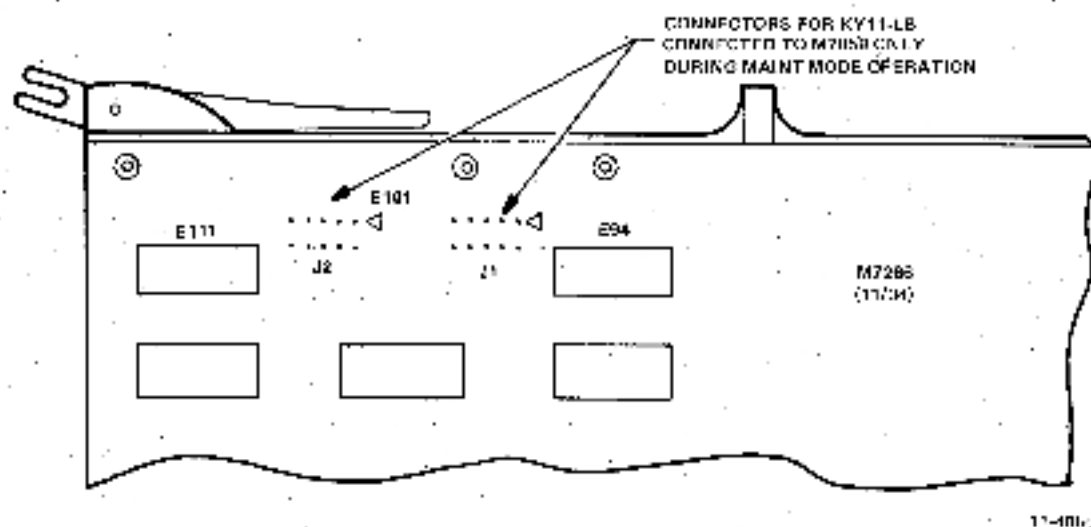


Figure 9-2 M7266

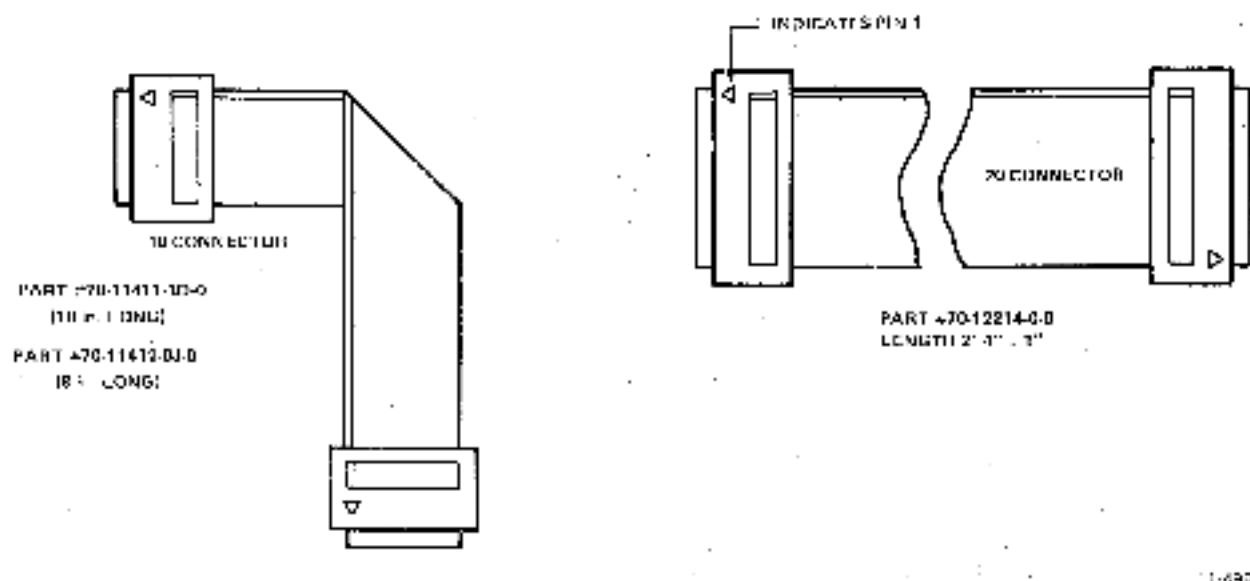


Figure 9-3 Cables

2. Install M7859 (KY11-LB interface) in any SPC slot (within CPU backplane) and connect it to the KY11-LB bezel as shown in Figure 9-4.

CONFIGURATION NOTE

The M7859 consumes 2A at +5 V and can only be plugged into the CPU backplane.

WARNING

When doing any reconfiguring of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

9.5 BA11-K 26.7 CM (10-1/2 INCH BOX) INSTALLATION

1. Remove the operator's console (KY11-LA), noting to which Faston tabs the M9301 is connected. The connection will be the same tabs on the KY11-LB (Figure 9-5). You will notice that J2 on the operator's console is not used on the BA11-K box. The signals and voltages that come in on this jack in the BA11-L box come in on Faston tabs in the BA11-K box. The cable connecting the CPU backplane to J1 on the operator's console must be removed and no connection from the backplane to the KY11-LB is made.
2. Install M7859 (KY11-LB interface) in any SPC slot (with CPU backplane) and connect to KY11-LB bezel as shown in Figure 9-5.

WARNING

When doing any reconfiguring of the CPU backplane that might be necessary to make room for the M7859, be sure that the M9302 is never installed in a modified Unibus slot (which results in short circuits).

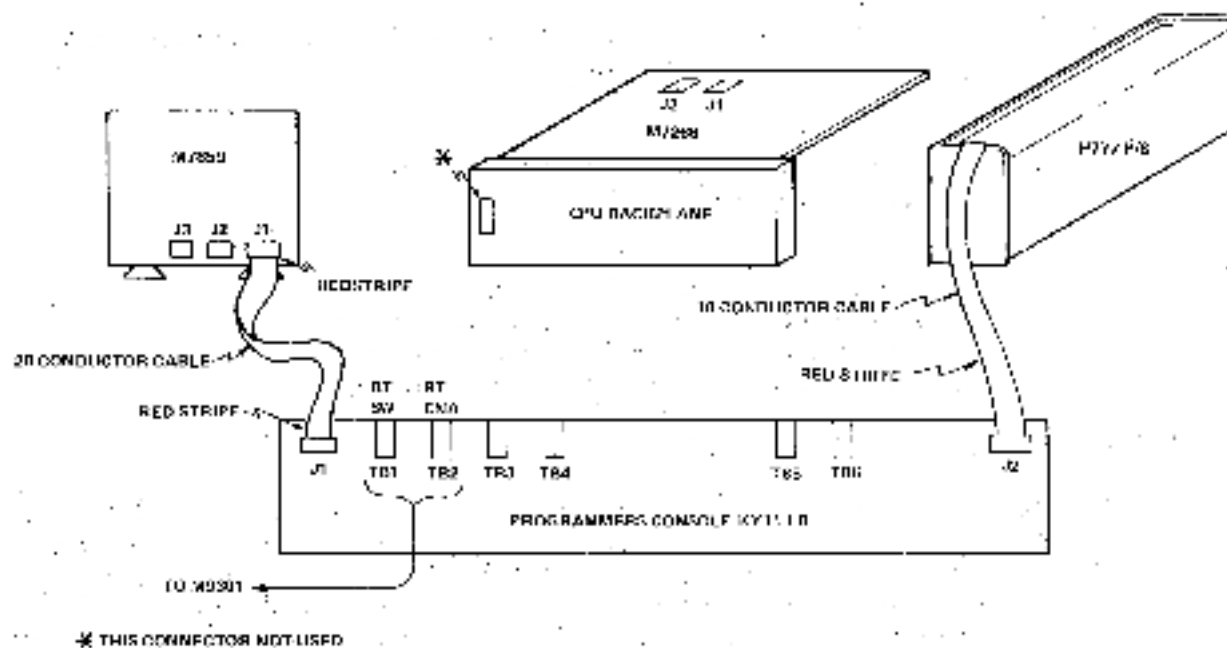
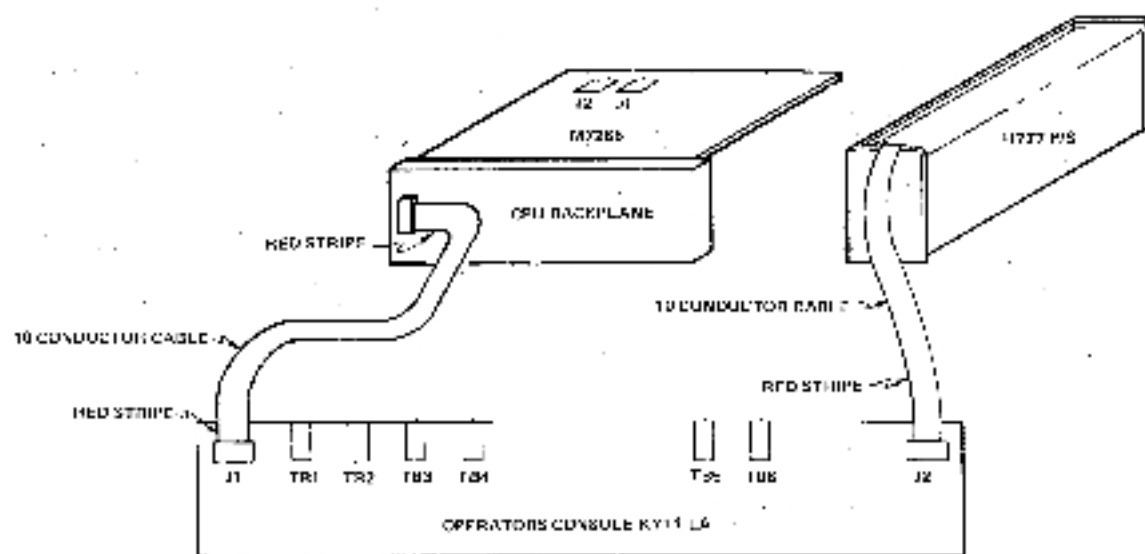
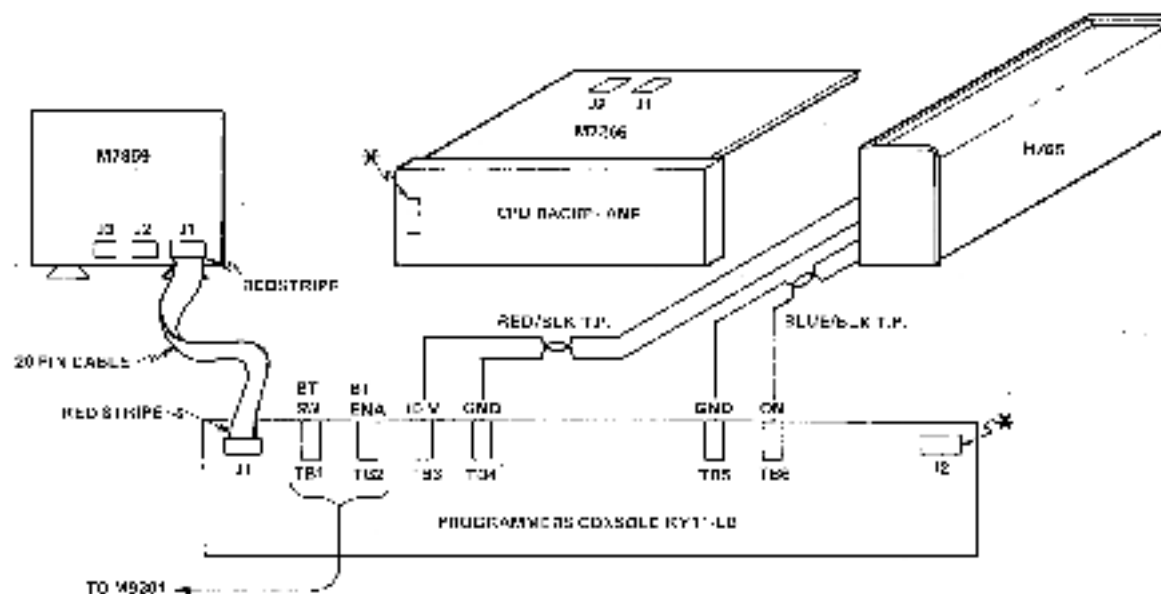
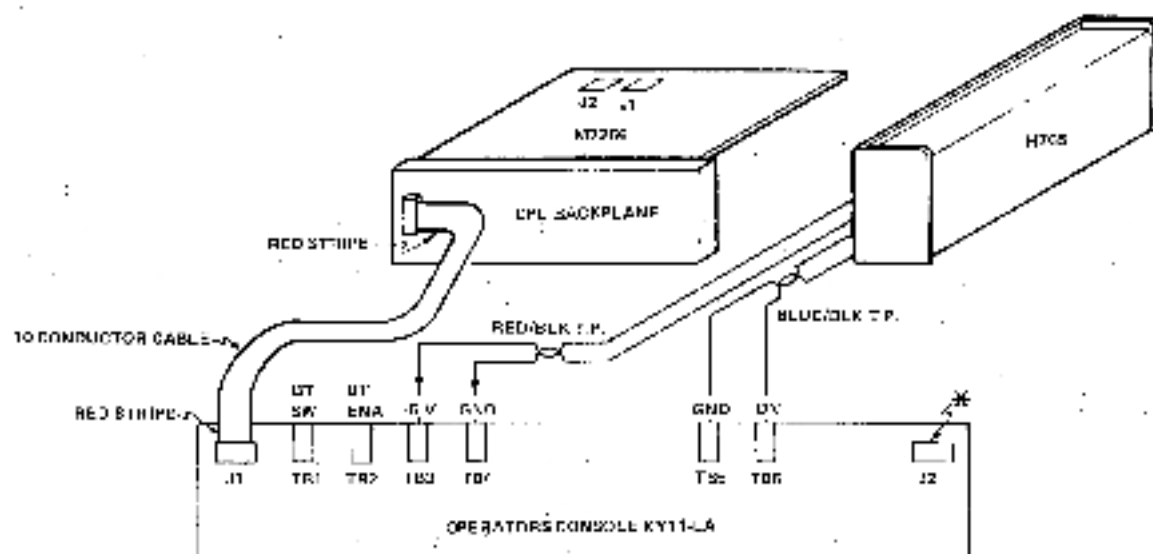


Figure 9-4 BA11-L



*11/50

11-50

Figure 9-5 BA11-K

9.6 MAINTENANCE MODE HOOK-UP

To utilize the KY11-LB as a maintenance tool for troubleshooting the CPU or system, additional cable(s) must be installed. The 11/04 requires one additional cable and the 11/34 requires two additional cables.

PDP-11/04 (Maintenance Mode Cabling)

The 11/04 requires only one additional cable for maintenance mode operation. This 10-conductor cable (Part No. 70-11411-1D-0) connects J2 of the M7859 to the unmarked male connector on the M7263 (11/04 CPU). The cable (70-11411-1D-0) has a pointer on each end to indicate pin 1 as shown in Figure 9-3. Install the cable with the pointer on the end of the cable lined up with pin 1 on the CPU module (M7263). Pin 1 on M7263 is called out on Figure 9-1. Points on J2 (M7859) and the cable should also be lined up.

PDP-11/34 (Maintenance Mode Cabling)

The 11/34 requires two additional cables for maintenance mode operation. Both cables are the same and are the same part as is used on the 11/04. See Figure 9-3 for part number.

NOTE

Maintenance cables for both 11/04 and 11/34 are all
45.7 cm (18 inch) long, 10-conductor cables.

When installing maintenance cables connect J2 (M7859) to J1 (M7266) and J3 (M7859) to J2 (M7266). The pointers on the cable and board must be matched at both ends of the cables.

APPENDIX A
KY11-LB MICRO-CODE LISTINGS

NY1 10 REGRAN RT-1 MACRO JMC2-12 0013125 PAGE 1

CHAPTER 100000

0013125

AL 1

2
NY1 8 REGRAN RT-1 MACRO JMC2-12 0013125 PAGE 2

6
NY1 8 REGRAN RT-1 MACRO JMC2-12 0013125 PAGE 3

1	000000	START		
2	000000	END		
3		FILE CHISEL PROGRAM		
4	000000	START		
5	000001	END		
6	000002	END		
7	000003	END		
8	000004	END		
9	000005	END		
10	000006	END		
11	000007	END		
12	000008	END		
13	000009	END		
14	000010	END		
15	000011	END		
16	000012	END		
17	000013	END		
18	000014	END		
19	000015	END		
20	000016	END		
21	000017	END		
22	000018	END		
23	000019	END		
24	000020	END		
25	000021	END		
26	000022	END		
27	000023	END		
28	000024	END		
29	000025	END		
30	000026	END		
31	000027	END		
32	000028	END		
33	000029	END		
34	000030	END		
35	000031	END		
36	000032	END		
37	000033	END		
38	000034	END		
39	000035	END		
40	000036	END		
41	000037	END		
42	000038	END		
43	000039	END		
44	000040	END		
45	000041	END		
46	000042	END		
47	000043	END		
48	000044	END		
49	000045	END		
50	000046	END		
51	000047	END		
52	000048	END		
53	000049	END		
54	000050	END		
55	000051	END		
56	000052	END		
57	000053	END		
58	000054	END		
59	000055	END		
60	000056	END		
61	000057	END		
62	000058	END		
63	000059	END		
64	000060	END		
65	000061	END		
66	000062	END		
67	000063	END		
68	000064	END		
69	000065	END		
70	000066	END		
71	000067	END		
72	000068	END		
73	000069	END		
74	000070	END		
75	000071	END		
76	000072	END		
77	000073	END		
78	000074	END		
79	000075	END		
80	000076	END		
81	000077	END		
82	000078	END		
83	000079	END		
84	000080	END		
85	000081	END		
86	000082	END		
87	000083	END		
88	000084	END		
89	000085	END		
90	000086	END		
91	000087	END		
92	000088	END		
93	000089	END		
94	000090	END		
95	000091	END		
96	000092	END		
97	000093	END		
98	000094	END		
99	000095	END		
100	000096	END		
101	000097	END		
102	000098	END		
103	000099	END		
104	000100	END		
105	000101	END		
106	000102	END		
107	000103	END		
108	000104	END		
109	000105	END		
110	000106	END		
111	000107	END		
112	000108	END		
113	000109	END		
114	000110	END		
115	000111	END		
116	000112	END		
117	000113	END		
118	000114	END		
119	000115	END		
120	000116	END		
121	000117	END		
122	000118	END		
123	000119	END		
124	000120	END		
125	000121	END		
126	000122	END		
127	000123	END		
128	000124	END		
129	000125	END		
130	000126	END		
131	000127	END		
132	000128	END		
133	000129	END		
134	000130	END		
135	000131	END		
136	000132	END		
137	000133	END		
138	000134	END		
139	000135	END		
140	000136	END		
141	000137	END		
142	000138	END		
143	000139	END		
144	000140	END		
145	000141	END		
146	000142	END		
147	000143	END		
148	000144	END		
149	000145	END		
150	000146	END		
151	000147	END		
152	000148	END		
153	000149	END		
154	000150	END		
155	000151	END		
156	000152	END		
157	000153	END		
158	000154	END		
159	000155	END		
160	000156	END		
161	000157	END		
162	000158	END		
163	000159	END		
164	000160	END		
165	000161	END		
166	000162	END		
167	000163	END		
168	000164	END		
169	000165	END		
170	000166	END		
171	000167	END		
172	000168	END		
173	000169	END		
174	000170	END		
175	000171	END		
176	000172	END		
177	000173	END		
178	000174	END		
179	000175	END		
180	000176	END		
181	000177	END		
182	000178	END		
183	000179	END		
184	000180	END		
185	000181	END		
186	000182	END		
187	000183	END		
188	000184	END		
189	000185	END		
190	000186	END		
191	000187	END		
192	000188	END		
193	000189	END		
194	000190	END		
195	000191	END		
196	000192	END		
197	000193	END		
198	000194	END		
199	000195	END		
200	000196	END		
201	000197	END		
202	000198	END		
203	000199	END		
204	000200	END		
205	000201	END		
206	000202	END		
207	000203	END		
208	000204	END		
209	000205	END		
210	000206	END		
211	000207	END		
212	000208	END		
213	000209	END		
214	000210	END		
215	000211	END		
216	000212	END		
217	000213	END		
218	000214	END		
219	000215	END		
220	000216	END		
221	000217	END		
222	000218	END		
223	000219	END		
224	000220	END		
225	000221	END		
226	000222	END		
227	000223	END		
228	000224	END		
229	000225	END		
230	000226	END		
231	000227	END		
232	000228	END		
233	000229	END		
234	000230	END		
235	000231	END		
236	000232	END		
237	000233	END		
238	000234	END		
239	000235	END		
240	000236	END		
241	000237	END		
242	000238	END		
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247	000243	END		
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250	000246	END		
251	000247	END		
252	000248	END		
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254	000250	END		
255	000251	END		
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263	000259	END		
264	000260	END		
265	000261	END		
266	000262	END		
267	000263	END		
268	000264	END		
269	000265	END		
270	000266</			

37	00000			ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
38	00001	100	LYP OF 000	ROUTINE FOR LYP OF 00000 LINE 10
	00002	100		
	00003	100		
39				
40				
41				
42	00004	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
43	00005	100		ROUTINE FOR LYP OF 00000 LINE 10
44				
45	00006	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00007	100		ROUTINE FOR LYP OF 00000 LINE 10
	00008	100		
46	00009	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00010	100		ROUTINE FOR LYP OF 00000 LINE 10
	00011	100		
47	00012	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00013	100		ROUTINE FOR LYP OF 00000 LINE 10
48	00014	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00015	100		ROUTINE FOR LYP OF 00000 LINE 10
	00016	100		
49	00017	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00018	100		ROUTINE FOR LYP OF 00000 LINE 10
	00019	100		
50	00020	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00021	100		ROUTINE FOR LYP OF 00000 LINE 10
	00022	100		
51	00023	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00024	100		ROUTINE FOR LYP OF 00000 LINE 10
	00025	100		
52	00026	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00027	100		ROUTINE FOR LYP OF 00000 LINE 10
	00028	100		
53	00029	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00030	100		ROUTINE FOR LYP OF 00000 LINE 10
	00031	100		
54	00032	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00033	100		ROUTINE FOR LYP OF 00000 LINE 10
	00034	100		
55	00035	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00036	100		ROUTINE FOR LYP OF 00000 LINE 10
	00037	100		
56	00038	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00039	100		ROUTINE FOR LYP OF 00000 LINE 10
	00040	100		
57	00041	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00042	100		ROUTINE FOR LYP OF 00000 LINE 10
	00043	100		
58	00044	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00045	100		ROUTINE FOR LYP OF 00000 LINE 10
	00046	100		
59	00047	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00048	100		ROUTINE FOR LYP OF 00000 LINE 10
	00049	100		
60	00050	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00051	100		ROUTINE FOR LYP OF 00000 LINE 10
	00052	100		
61	00053	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00054	100		ROUTINE FOR LYP OF 00000 LINE 10
	00055	100		
62	00056	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00057	100		ROUTINE FOR LYP OF 00000 LINE 10
	00058	100		
63	00059	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00060	100		ROUTINE FOR LYP OF 00000 LINE 10
	00061	100		
64	00062	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00063	100		ROUTINE FOR LYP OF 00000 LINE 10
	00064	100		
65	00065	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00066	100		ROUTINE FOR LYP OF 00000 LINE 10
	00067	100		
66	00068	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00069	100		ROUTINE FOR LYP OF 00000 LINE 10
	00070	100		
67	00071	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00072	100		ROUTINE FOR LYP OF 00000 LINE 10
	00073	100		
68	00074	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00075	100		ROUTINE FOR LYP OF 00000 LINE 10
	00076	100		
69	00077	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00078	100		ROUTINE FOR LYP OF 00000 LINE 10
	00079	100		
70	00080	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00081	100		ROUTINE FOR LYP OF 00000 LINE 10
	00082	100		
71	00083	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00084	100		ROUTINE FOR LYP OF 00000 LINE 10
	00085	100		
72	00086	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00087	100		ROUTINE FOR LYP OF 00000 LINE 10
	00088	100		
73	00089	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00090	100		ROUTINE FOR LYP OF 00000 LINE 10
	00091	100		
74	00092	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00093	100		ROUTINE FOR LYP OF 00000 LINE 10
	00094	100		
75	00095	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00096	100		ROUTINE FOR LYP OF 00000 LINE 10
	00097	100		
76	00098	100	LYP OF 000	ROUT. 2 IS 1 TO DELIVER TO A PROGRAM PAGE NUMBER.
	00099	100		ROUTINE FOR LYP OF 00000 LINE 10
	00100	100		

NY118 ROGRAM 07-1 NADIN VARY 10

0010125 PAGE 3-

63	00065	000			STD FILE OF THE POSITION OF THE FORM LOCATIONS IN RAM.
64	00066		A 2		GET THE CONTENTS OF THE LAST OF 4 TOP IN RAM.
65	00067	207			
66	00068		SP 2		SWITCH OFF THE LOWEST 2 BITS OF
67	00069	047			
68	00070	007			
69	00071		OUT 011		SEND TO THE DISPLAY.
70	00072	125			
71	00073		LD 0		READ THE 16 BITS INTO A REGISTER AND MULTIPLY IT
72	00074	203			
73	00075		SHR 10		STD TURN ON THE PROPER DIGIT OF THE DISPLAY. IT
74	00076	17			
75					WILL ALSO BE LEFT POSITIONED ON LINE OF THE KEYPAD
76	00077				FOR LOCAL PACK LINE.
77	00078	203	LD 0		GET THE CONTENTS OF REGISTER 0 AND RETAIN LEFT
78	00079	042	R 0		AND THE 16 BITS ON THE NEXT DIGIT.
79	00080	320			
80	00081		LD 0		READ THE 16 BITS HIGH 16 TO PASS TO THE SHIFTER
81	00082	015			
82	00083	000			
83	00084		OUT 011		COMBINATIONS WILL BE SHOWN ON DISPLAY RATE 2
84	00085	125			
85	00086	000			
86	00087				OPERATIONS.
87	00088	302	LD 0		FOR RETURN FROM SHIFT SUBROUTINE. LOAD REGISTER 0
88	00089		OUT 1		AND A 16 BIT SHIFTER AND CHECK FOR A 1 TO SEE IF LAST
89	00090	024			
90	00091	001			
91					THIS TIME BEING LAYED.
92	00092		JNZ 011 05		IF LAST DIGIT IS 0 AND DISPLAYED LINE OVER KEYPAD
93	00093	125			
94	00094	127			
95	00095	000			
96					FOR THE MESSAGE.
97	00096		AND 0		FOR THE 16 BIT A 1 TO REGISTER 0 (CONTAINS NINE RATES R 0)
98	00097	004			
99	00098	001			
100	00099		LD 0		LOAD THE 16 NEXT POINTER TO POINT TO KEYPAD FROM
101	00100	324			
102					FOR THE 16 NEXT
103	00101		LD 0		LOAD THE 16 NEXT
104	00102	112			POINT A 16 NEXT FROM THE KEYPAD AND
105	00103		NDI 17		MAKE THE 16 NEXT BITS.
106	00104	040			
107	00105	017			
108	00106	000	JNZ 013 04		CHECK FOR 16 NEXT 0 OR 16 NEXT 16 NEXT
109	00107	125			
110	00108	172			
111	00109	000			
112	00110		XP 1		COMPARE AGAINST THE CONTENTS OF THE REGISTER 0 AND
113	00111	207			
114	00112				0000111111111111

MY 113 PROGRAM RT-1 MICRO UP-2-10

[illegible]

162	0374	000		
	0375	001		
163	0376		END	
	0377	000		
164	0378	000	JTC NLRG	
	0379	000		
	0380	001		
	0381	001		
165	0382	000	END	
	0383	000		
166	0384	000	JTC NLRG	
	0385	000		
	0386	000		
167	0387	000		
	0388	000		
168	0389	000	END	
	0390	000		
169	0391	000	JTC NLRG	
	0392	000		
	0393	000		
	0394	000		
170	0395	000	END	
	0396	000		
	0397	000		
171	0398	000	JTC NLRG	
	0399	000		
172	0400	000		
173	0401	000		
174	0402	000		
175	0403	000		
176	0404	000		
177	0405	000		
178	0406	000		
179	0407	000		
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181	0409	000		
182	0410	000		
183	0411	000		
184	0412	000		
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199	0427	000		
200	0428	000		

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00112 PROGRAM RI-11 PAGE 5000 0

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11	0323	0323	0323		
	0324	0324	0324		
182	0327	0327	0327		
	0328	0328	0328		
183	0341	0341	0341		
	0342	0342	0342		
184	0342	0342	0342		
	0343	0343	0343		
185	0343	0343	0343		
	0344	0344	0344		
186	0344	0344	0344		
	0345	0345	0345		
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	0346	0346	0346		
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300	0357	0357	0357		

007	007			
008	008	007	007	RETURN TO THE LAST ROUTINE. OTHERWISE RETURN TO DEWIDE
009	009	008	008	
010	010	009	009	ROUTINE WHICH CALLED.
011	011			
012	012			
013	013			NUMERIC ROUTINE.
014	014			THIS ROUTINE GENERATES THE NUMBER 5 BIT
015	015			0001 USING NUMERIC KEY IS DE REEED AND
016	016			LEFT SHIFTS LEFT THE TEMPORARY AREA
017	017			0001 AREA.
018	018	017	017	DETERMINES THE 12 BIT OF THE CURRENT NUMBER
019	019	018	018	
020	020	019	019	FOR TIMES DEPENDING UPON THE NUMERIC KEY DE REEED.
021	021	020	020	MAKES THE 5 R-SHIFT AND CLEARS THE REGISTER
022	022	021	021	ON THE REGISTER ROUTINE.
023	023	022	022	
024	024	023	023	
025	025	024	024	
026	026	025	025	
027	027	026	026	
028	028	027	027	
029	029	028	028	
030	030	029	029	
031	031	030	030	
032	032	031	031	
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036	036	035	035	
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041	041	040	040	
042	042	041	041	
043	043	042	042	
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081	081	080	080	
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WHILE PROGRAM - 11-11 PAGES 0000-11
 CONTAINS PAGE 11

023	0401	07		
	0402	110		
	0403	007		
	0404	001		
240	0405	060	LLI 00	RESET MEMORY POINTER TO LEAST SIGNIFICANT WORD.
	0406	000		
241	0407	007	LD 1	GET THE WORD ADDRESS THE LEAST THREE SIGNIFICANT
242	0408	041	LD 2	BYTES.
	0409	000		
243	0410	001	ADD	THE THREE BIT DIGIT FROM SECTION B BACK
244	0411	000	LD 1	TO THE MEMORY.
245	0412	000	LD 2	TO THE DISPLAY INDICATORS.
246	0413	000		
247	0414	130		
248				
249				
250				
251				
252				
253	0415	060	LD 1	FROM ROUTINE.
	0416	010		
	0417	010		
254	0418	010	LD 1	FROM THE LEAST THREE WORDS FROM PAN INTO A REGISTER
	0419	010		
255	0420	000	LD 1	TO THE AND B.
	0421	000		
256	0422	007	LD 1	
257	0423	000	LD 1	
	0424	000		
258	0425	007	LD 1	
	0426	000		
259	0427	000	LD 1	RESET MEMORY POINTER TO THE LEAST AREA OF THE
	0428	000		
260	0429	000	LD 1	FROM AND ONE REGISTER TO THE AND B FROM THE MEMORY.
261	0430	000	LD 1	
	0431	000		
262	0432	000	LD 1	
	0433	000		
263	0434	000	LD 1	
	0435	000		
264	0436	000	LD 1	
	0437	000		
265	0438	000	LD 1	FROM THE DISPLAY ROUTINE.
	0439	000		
266	0440	000		
	0441	000		

BY JCS PROGRAM RT-1 NAME: WOOD TO 00000000 PAGE 3-

0452	040		
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374 0657      PUS SP LAL 20
      0657      003
      0660      020
375 0661      000 R 06      SET BUS ERROR INDICATOR
      0661      132      AL 0
376 0662      006
      0662      000
      0663      000
377 0664      000 R 05      DROP BUS MEYN.
      0664      132
378 0665      000 R 04      DROP UNIQUE ADDRESS LINES.
      0665      122
379 0666      000 CLR2      NO IDLE TIME DISPLAY.
      0666      104
      0667      032
      0670      010
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384 0671      000 L 1      CAL HITST
      0671      104
      0672      000
      0673      010
385 0674      000 L 0
      0674      006
      0675      000
386 0676      000 R 04      CLEAR THE INDICATORS.
      0676      135
387 0677      000 L 15      SET IN READY WINTER AND CHECK DEPOSIT FLAG.
      0677      056
      0678      015
388 0679      000 L 4
      0679      207
389 0680      000 R 1 100      FIRST DEPOSIT
      0680      014
      0681      000
390 0682      000 L 1 100      YES.
      0682      10
      0683      010
      0684      001
391 0685      000 R 1 0-RT1      INC. CHECK IN GENERAL REGISTER.
      0685      104
      0686      010
      0687      001
392 0688      000 R 1 1000      SEND ALL BUSES ADDR 98 POINT R.
      0688      104
      0689      010
      0690      001
393 0691      000 L 1 100      LAL N
      0691      307
394 0692      000 L 10      SET THE BUS 01 BIT (ON RND) TO 00.0.0.0.
      0692      000
395 0693      000 L 10

```


0755	064		
0756	094		
121 0757		OUT R162	LOAD LAST PART OF REGISTER.
0757	121		
422 0758		REI	
0758	007		
423			
424			
425			
426			
427			
428 0761		LDI R10	LDI R10
0761	307		
429 0762		OUT R161	SEND UNIQUE ADDRESS POINTER ON STARTED AND LOAD
0762	97		
430 0763		LD L	LOAD BYTE OF SWITCH REGISTER.
0763	060		
431 0764		LD M	LOAD SECOND WORD OF DATA AND LOAD INTO
0764	307		
432 0765		OUT R161	SEND BYTE OF DATA ON ADDRESS.
0765	121		
433 0766		LD R10	TEST BIT TO ENABLE SWITCH REGISTER DATA
0766	006		
0767	004		
434 0768		OUT R161	SEND CONTROL.
0768	121		
435 0769		LD R10	
0769	006		
0770	014		
436 0771		OUT R161	POWERED SW. HIGH.
0771	153		
437 0772		INP R161	THIS SW. IS HIGH.
0772	153		
438 0773		JMP R161	JUMP OVER FOR MEMORY BOUNDARY.
0773	104		
0774	307		
0775	010		
439 1000		NOP	
1000	300		
440 1001		INP R161	
1001	044		
1002	020		
441 1003		JZ R161	AND.
1003	150		
1004	257		
1005	001		
442 1006		AI 4	INCR.
1006	306		
1007	004		
443 1010		OUT R161	INCR. SW. HIGH.
1010	153		
444 1011		AI 0	
1011	006		
1012	000		
445 1013		INP R161	INCR. THE SWITCH REGISTER ENABLE.
1013	153		
446 1014		OUT R161	INCR. THE SWITCH REGISTER ENABLE AND POWER.
1014	153		

00113 PROGRAM R1 = 1 WORD UPON 10
0011425 END

100	1015	101	OUT REG	FROM THE UNIBUS.
101	1015	101		
102	1015	101	OUT REG3	
103	1015	101		
104	1015	101	OUT REG3	
105	1015	101		
106	1015	101	OUT REG3	
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298	1015	101	OUT REG3	
299	1015	101		
300	1015	101	OUT REG3	

471	1045		JF2 H1L1	LDONE COUNTING.
	1046	1 0		
	1046	048		
	1047	010		
472	1050		INC B	DECREMENT COUNTER.
	1050	011		
473	1051		JF2 H1L2	STINEB CUT7 NO.
	1051	110		
	1052	048		
	1053	010		
474	1064		JM1 H1H1R	STLS. GO TO BUS ERROR ROUTINE.
	1064	04		
	1065	057		
	1066	001		
475	1067		L1J2 L1J2	RECEIVED GRANT, NOW CLEAR INDICATORS.
	1067	048		
	1070	000		
476	1071		OUT REGA	
	1071	137		
477	1072		L1J3 J07	LOAD LINEAR ADDRESS OF PC (B7) 1277.007.
	1072	006		
	1073	007		
478	1074		INT REGA	FIND THE UNIBUS ADDRESS REGISTER AND
	1074	101		
479	1075		LAL J07	RELOAD INTO THE UNIBUS.
	1075	006		
	1076	077		
480	1077		INT REG	
	1077	102		
481	1100		LAL J	
	1100	006		
	1101	007		
482	1102		OUT REG2	
	1102	102		
483	1103		CALL DAL 1	CALL THE DAL1 SUBROUTINE.
	1103	107		
	1104	070		
	1105	001		
484	1106		JM1 H0V1	DISPLAY THE PC.
	1106	104		
	1107	043		
	1108	001		
485				
486				
487				
488				
489	1111		INIT DAL H0V1	FIND KEY SERVICE ROUTINE.
	1111	008		
	1112	008		
	1113	000		
491	1114		DAL H1T5	THAT THE PERMISSION IS GRANTED.
	1114	100		
	1115	052		
	1116	010		
492	1117		DAL INITX	REAL THE INITIALIZE SUBROUTINE.
	1117	106		
KEY1 2	1118			
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1120	140		
1121	010		
493 1122		LA 1	REMOVE THE HLT AT 1121 AVOIDING THE HLT REQUEST
1123	004		
1124	00		
494 1125		OUT REGT	EXIT REG.
1126	133		
495 1127		AND 01001	
1128	104		
1129	423		
1130	000		
496			
497			
498			
499			
500			
501			
502 1130		INSTR: LFI 3	
1131	004		
1132	004		
503 1133		OLD REGT	PREPARE FOR INIT AND WAIT FOR INIT BUS-
1134	23		
504 1135		INSTR: LFI 12	FOR INIT BUS REQUEST ON A 150 MILLISECOND DELAY.
1136	014		
1137	012		
505 1138		LFI 8	
1139	036		
1140	030		
506 1141		INSTR: DE C	ADJOURNMENT COUNTERS ARE DECREMENTED HERE.
1142	021		
507 1143		JFZ INTRX	
1144	1 0		
1145	1 0		
1146	010		
508 1147		DE B	
1148	011		
509 1149		JFZ INTRX	
1150	110		
1151	1 0		
1152	010		
510 1153		RET	
1154	007		
511			
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518 1155		INSTR: CML INTR	RESTART INIT BUS.
1156	1 0		
1157	3 0		
1158	000		
519 1159		END INTR	INIT PROCESSING IS HALTED.
1160	1 0		
1161	3 0		
1162	010		
520 1163			
1164	010		
1165	010		
1166	010		

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503	1181		LBI 240	RESET PROGRAMMER HALT FLAG.
	1182	016		
	1183	010		
504	1184		LBI 307	DEAL ADDRESS OF IN 00000000 AND THE
	1185	000		
	1186	007		
505	1187		OUT REED	FUNCTION ADDRESS OF IN 00000000.
	1188	10		
506	1189		LBI 377	
	1190	000		
	1191	007		
507	1192		OUT REED1	
	1193	100		
508	1194		LBI 17	SET THE ENABLE BIT (0) AND THE
	1195	000		
	1196	007		
509	1197		OUT REED2	FROM IN 00000000.
	1198	100		
510	1199		LBI 12	SET THE MEMORY POINTER TO INITIAL ADDRESS OF PROGRAM.
	1200	000		
	1201	007		
511	1202		CA 0000	LOAD IN 00000000 TO INITIALIZE.
	1203	100		
	1204	000		
	1205	007		
512	1206		CA 0000	LOAD THE INITIALIZE ADDRESS TO IN 00000000.
	1207	100		
	1208	000		
	1209	007		
513	1210		LBI 1	TRUE INITIALIZE.
	1211	000		
	1212	007		
514	1213		OUT R005	FROM IN 00000000 AND IN 00000000 AND SET DIS-
	1214	100		
515	1215		LBI 0	CLEAR BIT, THEN FROM BUS CLEAR BIT.
	1216	000		
	1217	007		
516	1218		OUT R005	
	1219	100		
517	1220		JHI 000 EP	JUMP TO EMULATED REGISTER DISPLAY ROUTINE.
	1221	100		
	1222	000		
518	1223			
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719	1424			
720	1425			
721	1426			
722	1427			
723	1428			
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725	1430			
726	1431			
727	1432			
728	1433			
729	1434			
730	1435			
731	1436			
732	1437			
733	1438			
734	1439			
735	1440			
736	1441			
737	1442			
738	1443			
739	1444			
740	1445			
741	1446			
742	1447			
743	1448			
744	1449			
745	1450			
746	1451			
747	1452			
748	1453			
749	1454			
750	1455			
751	1456			
752	1457			
753	1458			
754	1459			
755	1460			
756	1461			
757	1462			
758	1463			
759	1464			
760	1465			
761	1466			
762	1467			
763	1468			
764	1469			
765	1470			
766	1471			
767	1472			
768	1473			
769	1474			
770	1475			
771	1476			

542	1221		OUT REGS	END OF THIS ROUTINE. THE PROGRAM IS ALREADY
543	1222	100	AL 0	ENDING AS THIS WILL HAVE NO EFFECT.
	1223	006		
	1224	000		
544	1224		OUT REGS	
	1224	032		
545	1225		JMP SUBDISP	JUMP TO SUBROUTINE: DISPLAY ROUTINE.
	1225	04		
	1226	061		
	1227	010		
546				
547				
548				
549				
550				
551				
552				
553	1230		BR1: LDI 10	
	1230	006		
	1231	010		
554	1231		LD R	MOVE ADDRESS TO REGISTERS A AND B.
	1232	007		
555	1233		IN 1	
	1233	060		
556	1234		LD R	
	1234	017		
557	1235		LD 16	MOVE TEMPORARY POINTER TO SWITCH REGISTER
	1235	006		
	1236	010		
558	1237		LD R	FINISH AREA AND LOAD MEMORY FROM REGISTERS
	1237	010		
559	1240		IN	A AND B.
	1240	060		
560	1241		LD R	
	1241	007		
561	1242		CALL 16	CALL THE 16 LOAD SUBROUTINE AND
	1242	006		
	1243	010		
	1244	010		
562	1245		JMP SUBDISP	JUMP TO SUBROUTINE: DISPLAY ROUTINE.
	1245	004		
	1246	061		
	1247	010		
563				
564				
565				
566				
567				
568				
569				
570				
571	1250		BR1: LDI 16	
	1250	006		
	1251	016		
572	1251		LD R	SEND 1600 THE LOW BYTE OF THE SWITCH REGISTER
	1252	017		
573	1252			
574	1253			

575: 8 PROGRAM (7-1) MACRO V003-10
 576: 1253 PAGE 54

523	1253		LA R	WITH THE FIRST WORD.
	1254	291		
524	1254		OUT BRFB	
	1254	127		
525	1253		IN L	
	1254	010		
526	1254		LA R	LOAD THE 104 BYT OF THE 1000-REGISTER
	1254	297		
527	1257		OUT BRFB	WITH THE NEXT WORD FROM MEMORY.
	1257	131		
528	1259		RT	
	1260	097		
529				
530				
531				
532				SEARCH REGISTER DISPLAY ROUTINE.
533				THIS ROUTINE MOVES THE CONTENTS OF THE
534				SEARCH REGISTER 1040, OVER OF ROM TO THE
535				DISPLAY AREA IN ROM AND THEN THE 1001
536				REGISTER IS DISPLAYED FOR 1000 THE 1001.
536	1261		BRI IN: L: 16	
	1261	066		
	1262	016		
537	1263		LD 0	
	1263	016		
	1264	000		
538	1263		LA R	
	1263	307		
539	1266		IN 1	
	1266	060		
540	1267		LD H	
	1267	3 7		
541	1269		LD 0	
	1269	066		
	1271	000		
542	1272		LD 1	
	1272	370		
543	1273		LD	
	1273	060		
544	1274		LD H	
	1274	371		
545	1275		IN 1	
	1275	060		
546	1276		LD 1	
	1276	372		
547	1277		LD 40	
	1277	060		
	1300	040		
548	1301		OUT BRFB	
	1301	171		
549	1302		JHI DISP1	
	1302	104		
	1303	022		
	1304	000		
550				
551				
552				
553				
KILLB PROGRAM RT-11 MICRO VM02-10				LOAD ADDRESS ROUTINE.
				THIS ROUTINE SERVICES THE LAA KEY FUNCTION
				00112120 PAGE 81

542	1221		OUT R20C	IFC CONTINUE, IF THE PROCESSOR IS ALREADY
543	1222	0.5	END	OPERATION THIS WILL HAVE NO EFFECT.
	1223	0.5		
	1224	0.5		
544	1225	1.45	OUT R20C	
	1226			
545	1227	1.45	JMP BRDISP	JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
	1228	1.4		
	1229	1.4		
	1230	0.10		
546				
547				
548				
549				LOAD SWITCH REGISTER ROUTINE.
550				THIS ROUTINE SERVICES THE LS: KEY FUNCTION.
551				LOADS TEMPORARY PREG INTO THE SWITCH
552				REGISTER, PREG ADDRESS FROM DATA THE SWITCH
553				REGISTER AND SETS THE SWITCH REGISTER.
554	1231		LDI R1	SET PREG POINTER TO TEMPORARY PREG ADDRESS
	1232	0.5		
	1233	0.10		
555	1234		LD R1	MOVE TWO WORDS TO REGISTER R1 AND R2
	1235	0.5		
556	1236	0.5	LD R1	
	1237	0.10		
557	1238		LDI R1	RESET WINDOW POINTER TO SWITCH REGISTER
	1239	0.5		
	1240	0.10		
558	1241		LD R1	PAGE AREA AND LOAD WINDOW FROM REGISTER
	1242	0.5		
559	1243		LDI R1	ADDRESS
	1244	0.5		
560	1245		LD R1	
	1246	0.10		
561	1247		CALL BRDI	CALL THE BR DI SUBROUTINE AND
	1248	0.5		
	1249	0.10		
	1250	0.5		
562	1251		JMP BRDISP	JUMP TO SWITCH REGISTER DISPLAY ROUTINE.
	1252	1.4		
	1253	0.10		
563				
564				
565				FOR LOAD SUBROUTINE.
566				THIS SUBROUTINE LOADS THE SWITCH REGISTER
567				WITH THE CONTENTS OF THE SWITCH REGISTER
568				ADDRESS PREG IN ROM. THIS SUBROUTINE IS USED
569				BY THE LOAD WINDOW REGISTER ROUTINE, AND
570				AFTER DATA TO RESTORE THE SWITCH REGISTER.
571	1254		LDI R1	SET WINDOW POINTER TO SWITCH REGISTER ADDRESS
	1255	0.5		
	1256	0.10		
572	1257		LD R1	LOAD DATA FROM WINDOW OF THE SWITCH REGISTER
	1258	0.5		
	1259	0.10		
AT ILB PROGRAM RT-1 MACRO VMOF-13				
CROSSING PAGE 11				

573	1233		LA B	WITH IN FIRST WORD
574	1234	301	OUT SALE	
	1234	127		
575	1235		IN L	
	1235	000		
576	1236		LA A	LOAD IN FOUR BYTE OF THE SWITCH REGISTER
	1236	301		
577	1237		OUT SALE	WITH IN SEAT WORD FROM MEMORY
	1237	121		
578	1240		RET	
	1240	007		
579				
580				
581				
582				
583				
584				
585				
586	1241		ENDISPI	LI 1 16
	1241	016		
	1241	016		
587	1242		LI 1 16	
	1242	034		
	1242	030		
588	1243		LA B	
	1243	307		
589	1244		IN L	
	1244	090		
590	1245		LA B	
	1245	317		
591	1246		LI 1 16	
	1246	066		
	1246	000		
592	1247		IN A	
	1247	470		
593	1248		IN	
	1248	040		
594	1249		LA B	
	1249	471		
595	1250		IN	
	1250	060		
596	1251		IN 2	
	1251	472		
597	1252		LA 1 16	
	1252	007		
	1252	040		
598	1253		OUT SALE	
	1253	170		
599	1254		ENDISPI	
	1254	104		
	1254	012		
	1254	000		
600				
601				
602				
603				
KYLE PROGRAM RT-1 MICRO MICRO-10				LOAD ADDRESS 10000 THIS ROUTINE SERVES THE LA 1 16 FUNCTION 00113:25 140 01

604					
605					
606					
607					
608	1304		LDI	1304	
	1304	004			
	1304	000			
609	1307				
	1307	178			
610	1310				
	1310	004			
	1310	000			
611	1310				
	1310	307			
612	1312				
	1312	040			
613	1313				
	1313	317			
614	1314				
	1314	000			
615	1316				
	1316	307			
616	1317				
	1317	044			
	1317	003			
617	1321				
	1321	040			
618	1322				
	1322	307			
619	1324				
	1324	000			
620	1324				
	1324	071			
621	1325				
	1325	300			
622	1327				
	1327	300			
623	1328				
	1328	014			
	1328	000			
624	1330				
	1330	178			
625	1331				
	1331	001			
	1331	000			
626	1334				
	1334	307			
627	1335				
	1335	040			
628	1336				
	1336	070			
629	1337				
	1337	000			
630	1340				
	1340	000			
631	1341				
	1341	104			

BY ROUTING THE CONTENTS OF THE TEMPORARY
AREA OF RAM TO THE INPUT ADDRESS POINTER
AREA OF RAM AND BY ROUTING THE TEMPORARY
AREA.

FROM THE TEMPORARY TO INPUT ADDRESS POINTER.

TO THE TEMPORARY AREA.

632	042	042		
633	043	001		
634				DISPLAY ADDRESS ROUTINE.
635				THIS ROUTINE SERVICES THE DIS AD KEY
636				FUNCTION. IT MOVES THE CURSOR ADDRESS TO A16,
637				TO THE DISPLAY AREA IN RAM.
638	0244		DISF001 L01 0	
639	0245	002		
640	0246	003		
641	0247	004	LLI 13	INCRAS INDICATORS.
642	0248	005	LLI 13	
643	0249	006	LLI 13	
644	0250	007	LLI 13	
645	0251	008	LLI 13	
646	0252	009	LLI 13	
647	0253	010	LLI 13	
648	0254	011	LLI 13	
649	0255	012	LLI 13	
650	0256	013	LLI 13	
651	0257	014	LLI 13	
652	0258	015	LLI 13	
653	0259	016	LLI 13	
654	0260	017	LLI 13	
655	0261	018	LLI 13	
656	0262	019	LLI 13	
657	0263	020	LLI 13	
658	0264	021	LLI 13	
659	0265	022	LLI 13	
660	0266	023	LLI 13	
661	0267	024	LLI 13	
662	0268	025	LLI 13	
663	0269	026	LLI 13	
664	0270	027	LLI 13	
665	0271	028	LLI 13	
666	0272	029	LLI 13	
667	0273	030	LLI 13	
668	0274	031	LLI 13	
669	0275	032	LLI 13	
670	0276	033	LLI 13	
671	0277	034	LLI 13	
672	0278	035	LLI 13	
673	0279	036	LLI 13	
674	0280	037	LLI 13	
675	0281	038	LLI 13	
676	0282	039	LLI 13	
677	0283	040	LLI 13	
678	0284	041	LLI 13	
679	0285	042	LLI 13	
680	0286	043	LLI 13	
681	0287	044	LLI 13	
682	0288	045	LLI 13	
683	0289	046	LLI 13	
684	0290	047	LLI 13	
685	0291	048	LLI 13	
686	0292	049	LLI 13	
687	0293	050	LLI 13	
688	0294	051	LLI 13	
689	0295	052	LLI 13	
690	0296	053	LLI 13	
691	0297	054	LLI 13	
692	0298	055	LLI 13	
693	0299	056	LLI 13	
694	0300	057	LLI 13	
695	0301	058	LLI 13	
696	0302	059	LLI 13	
697	0303	060	LLI 13	
698	0304	061	LLI 13	
699	0305	062	LLI 13	
700	0306	063	LLI 13	
701	0307	064	LLI 13	
702	0308	065	LLI 13	
703	0309	066	LLI 13	
704	0310	067	LLI 13	
705	0311	068	LLI 13	
706	0312	069	LLI 13	
707	0313	070	LLI 13	
708	0314	071	LLI 13	
709	0315	072	LLI 13	
710	0316	073	LLI 13	
711	0317	074	LLI 13	
712	0318	075	LLI 13	
713	0319	076	LLI 13	
714	0320	077	LLI 13	
715	0321	078	LLI 13	
716	0322	079	LLI 13	
717	0323	080	LLI 13	
718	0324	081	LLI 13	
719	0325	082	LLI 13	
720	0326	083	LLI 13	
721	0327	084	LLI 13	
722	0328	085	LLI 13	
723	0329	086	LLI 13	
724	0330	087	LLI 13	
725	0331	088	LLI 13	
726	0332	089	LLI 13	
727	0333	090	LLI 13	
728	0334	091	LLI 13	
729	0335	092	LLI 13	
730	0336	093	LLI 13	
731	0337	094	LLI 13	
732	0338	095	LLI 13	
733	0339	096	LLI 13	
734	0340	097	LLI 13	
735	0341	098	LLI 13	
736	0342	099	LLI 13	
737	0343	100	LLI 13	
738	0344	101	LLI 13	
739	0345	102	LLI 13	
740	0346	103	LLI 13	
741	0347	104	LLI 13	
742	0348	105	LLI 13	
743	0349	106	LLI 13	
744	0350	107	LLI 13	
745	0351	108	LLI 13	
746	0352	109	LLI 13	
747	0353	110	LLI 13	
748	0354	111	LLI 13	
749	0355	112	LLI 13	
750	0356	113	LLI 13	
751	0357	114	LLI 13	
752	0358	115	LLI 13	
753	0359	116	LLI 13	
754	0360	117	LLI 13	
755	0361	118	LLI 13	
756	0362	119	LLI 13	
757	0363	120	LLI 13	
758	0364	121	LLI 13	
759	0365	122	LLI 13	
760	0366	123	LLI 13	
761	0367	124	LLI 13	
762	0368	125	LLI 13	
763	0369	126	LLI 13	
764	0370	127	LLI 13	
765	0371	128	LLI 13	
766	0372	129	LLI 13	
767	0373	130	LLI 13	
768	0374	131	LLI 13	
769	0375	132	LLI 13	
770	0376	133	LLI 13	
771	0377	134	LLI 13	
772	0378	135	LLI 13	
773	0379	136	LLI 13	
774	0380	137	LLI 13	
775	0381	138	LLI 13	
776	0382	139	LLI 13	
777	0383	140	LLI 13	
778	0384	141	LLI 13	
779	0385	142	LLI 13	
780	0386	143	LLI 13	
781	0387	144	LLI 13	
782	0388	145	LLI 13	
783	0389	146	LLI 13	
784	0390	147	LLI 13	
785	0391	148	LLI 13	
786	0392	149	LLI 13	
787	0393	150	LLI 13	
788	0394	151	LLI 13	
789	0395	152	LLI 13	
790	0396	153	LLI 13	
791	0397	154	LLI 13	
792	0398	155	LLI 13	
793	0399	156	LLI 13	
794	0400	157	LLI 13	
795	0401	158	LLI 13	
796	0402	159	LLI 13	
797	0403	160	LLI 13	
798	0404	161	LLI 13	
799	0405	162	LLI 13	
800	0406	163	LLI 13	
801	0407	164	LLI 13	
802	0408	165	LLI 13	
803	0409	166	LLI 13	
804	0410	167	LLI 13	
805	0411	168	LLI 13	
806	0412	169	LLI 13	
807	0413	170	LLI 13	
808	0414	171	LLI 13	
809	0415	172	LLI 13	
810	0416	173	LLI 13	
811	0417	174	LLI 13	
812	0418	175	LLI 13	
813	0419	176	LLI 13	
814	0420	177	LLI 13	
815	0421	178	LLI 13	
816	0422	179	LLI 13	
817	0423	180	LLI 13	
818	0424	181	LLI 13	
819	0425	182	LLI 13	
820	0426	183	LLI 13	
821	0427	184	LLI 13	
822	0428	185	LLI 13	
823	0429	186	LLI 13	
824	0430	187	LLI 13	
825	0431	188	LLI 13	
826	0432	189	LLI 13	
827	0433	190	LLI 13	
828	0434	191	LLI 13	
829	0435	192	LLI 13	
830	0436	193	LLI 13	
831	0437	194	LLI 13	
832	0438	195	LLI 13	
833	0439	196	LLI 13	
834	0440	197	LLI 13	
835	0441	198	LLI 13	
836	0442	199	LLI 13	
837	0443	200	LLI 13	
838	0444	201	LLI 13	
839	0445	202	LLI 13	
840	0446	203	LLI 13	
841	0447	204	LLI 13	
842	0448	205	LLI 13	
843	0449	206	LLI 13	
844	0450	207	LLI 13	
845	0451	208	LLI 13	
846	0452	209	LLI 13	
847	0453	210	LLI 13	
848	0454	211	LLI 13	
849	0455	212	LLI 13	
850	0456	213	LLI 13	
851	0457	214	LLI 13	
852	0458	215	LLI 13	
853	0459	216	LLI 13	
854	0460	217	LLI 13	
855	0461	218	LLI 13	
856	0462	219	LLI 13	
857	0463	220	LLI 13	
858	0464	221	LLI 13	
859	0465	222	LLI 13	
860	0466	223	LLI 13	
861	0467	224	LLI 13	
862	0468	225	LLI 13	
863	0469	226	LLI 13	
864	0470	227	LLI 13	
865	0471	228	LLI 13	
866	0472	229	LLI 13	
867	0473	230	LLI 13	
868	0474	231	LLI 13	
869	0475	232	LLI 13	
870	0476	233	LLI 13	
871	0477	234	LLI 13	
872	0478	235	LLI 13	
873	0479	236	LLI 13	
874	0480	237	LLI 13	

1400	001		
839 1401	PRINT1: HI 40		YES, MAINTENANCE MODE!!!
1402	006		
1403	040		
840 1404	RA 100		DID NOT LOCK THE PROGRAMMED HATCH AND
1405	006		
1406	100		
841 1407	SHI REG		SET TO MAINTENANCE MODE INDICATOR.
1408	170		
842 1409	ALI 0		KEYS IN 12 BITS OF KPC AND DISPLAY.
1410	006		
1411	000		
843 1412	INF REG		
1413	1-5		
844 1414	LM 1		
1415	070		
845 1416	IM 1		
1417	000		
846 1418	IM 0 HZ		
1419	17		
847 1420	IM 17		
1421	040		
1422	017		
848 1423	LV 0		
1424	040		
849 1425	LM 1		
1426	040		
850 1427	LM 0		
1428	070		
851 1429	PRINT2: CAL 13075		CALL THE DISPLAY SUBROUTINE.
1430	04		
1431	047		
852 1432	LET 1		THE FOLLOWING IS THE KEY ROUTINE ROUTINE
1433	016		
1434	000		
853 1435	LET 200		IFLX (HOLD KEY PENDING) EVAL ADD 1 IN
1436	040		
1437	000		
854 1438	LET 1		MAINTENANCE MODE.
1439	016		
1440	017		
855 1441	LV 0		
1442	007		
856 1443	VAR		
1444	040		
857 1445	VAR		
1446	040		
858 1447	VAR		
1448	070		
859 1449	VAR		
1450	040		
860 1451	VAR		
1452	040		
861 1453	VAR		
1454	040		
862 1455	VAR		
1456	040		
863 1457	VAR		
1458	040		
864 1459	VAR		
1460	040		
865 1461	VAR		
1462	040		
866 1463	VAR		
1464	040		
867 1465	VAR		
1466	040		
868 1467	VAR		
1468	040		
869 1469	VAR		
1470	040		
870 1471	VAR		
1472	040		
871 1473	VAR		
1474	040		
872 1475	VAR		
1476	040		
873 1477	VAR		
1478	040		
874 1479	VAR		
1480	040		
875 1481	VAR		
1482	040		
876 1483	VAR		
1484	040		
877 1485	VAR		
1486	040		
878 1487	VAR		
1488	040		
879 1489	VAR		
1490	040		
880 1491	VAR		
1492	040		
881 1493	VAR		
1494	040		
882 1495	VAR		
1496	040		
883 1497	VAR		
1498	040		
884 1499	VAR		
1500	040		

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481	1443		JTC MISC
	1443	140	
	1444	144	
	1444	01	
482	1445		IN
	1445	040	
483	1447		IN
	1447	060	
484	1450		LO H
	1450	307	
485	1451		RAS
	1451	032	
486	1452		JTC MISC
	1452	140	
	1453	126	
	1454	011	
487	1455		RAS
	1455	032	
488	1456		JTC TORBUS
	1456	140	
	1457	003	
	1458	011	
489	1459		IN L
	1459	040	
490	1460		IN L
	1460	040	
491	1461		LO H
	1461	007	
492	1462		RAS
	1462	032	
493	1463		JTC PHL
	1463	140	
	1464	140	
	1465	011	
494	1470		RAS
	1470	023	
495	1471		JTC MISC
	1471	140	
	1472	140	
	1473	011	
496	1474		RAS
	1474	023	
497	1475		JTC MISC
	1475	140	
	1476	007	
	1477	011	
498	1478		RAS
	1478	040	
499	1479		JTC MISC
	1479	140	
	1480	174	
	1481	011	
500	1482		JTC MISC
	1482	140	
	1483	072	
	1484	011	

701 1107
 811111 1107

PCREAD: L11 0
 11-11 1107 1107-10

PCREAD IN LINES ALDR 88 LINES AND 1107 1107
 1107 1107 1107 1107

1307	044		
1310	000		
202 1311		EXP. 5000	
1311	001		
202 1312		EXP. A	
1312	320		
204 1313		B. L.	
1313	040		
204 1314		EXP. 5000	
1314	007		
204 1315		EXP. A	
1315	040		
202 1316		B. L.	
1316	040		
201 1317		EXP. 5000	
1317	111		
209 1320		EXP. 5	
1320	044		
1321	000		
210 1322		B. L.	
1322	270		
21 1323		EXP. 5000	
1323	104		
1324	000		
1325	001		
212 1326		EXP. 5000	EXP. 5000
1326	040		
1327	000		
213 1328		EXP. 5000	
1328	107		
214 1329		EXP. 5	
1329	320		
214 1330		B. L.	
1330	040		
214 1331		EXP. 5000	
1331	040		
214 1332		EXP. 5000	
1332	040		
214 1333		EXP. 5000	
1333	040		
214 1334		EXP. 5000	
1334	040		
214 1335		B. L.	
1335	040		
214 1336		EXP. 5000	
1336	040		
214 1337		EXP. 5000	
1337	040		
214 1338		EXP. 5000	
1338	040		
214 1339		EXP. 5000	
1339	040		
214 1340		EXP. 5000	
1340	040		
214 1341		EXP. 5000	
1341	040		
214 1342		EXP. 5000	
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214 1343		EXP. 5000	
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214 1344		EXP. 5000	
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214 1345		EXP. 5000	
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214 1346		EXP. 5000	
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214 1349		EXP. 5000	
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214 1350		EXP. 5000	
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214 1351		EXP. 5000	
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214 1353		EXP. 5000	
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214 1354		EXP. 5000	
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214 1361		EXP. 5000	
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214 1362		EXP. 5000	
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214 1363		EXP. 5000	
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214 1364		EXP. 5000	
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214 1365		EXP. 5000	
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214 1366		EXP. 5000	
1366	040		
214 1367		EXP. 5000	
1367	040		
214 1368		EXP. 5000	
1368	040		
214 1369		EXP. 5000	
1369	040		
214 1370		EXP. 5000	
1370	040		
214 1371		EXP. 5000	
1371	040		
214 1372		EXP. 5000	
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214 1373		EXP. 5000	
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214 1374		EXP. 5000	
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214 1380		EXP. 5000	
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214 1381		EXP. 5000	
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214 1387		EXP. 5000	
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214 1388		EXP. 5000	
1388	040		
214 1389		EXP. 5000	
1389	040		
214 1390		EXP. 5000	
1390	040		
214 1391		EXP. 5000	
1391	040		
214 1392		EXP. 5000	
1392	040		
214 1393		EXP. 5000	
1393	040		
214 1394		EXP. 5000	
1394	040		
214 1395		EXP. 5000	
1395	040		
214 1396		EXP. 5000	
1396	040		
214 1397		EXP. 5000	
1397	040		
214 1398		EXP. 5000	
1398	040		
214 1399		EXP. 5000	
1399	040		
214 1400		EXP. 5000	
1400	040		

725	1551		IF: PA 11	
	1552	001		
	1553	011		
726	1554	001	CALL 0	COLLAR IN MAINTENANCE MODE. INDICATOR ON
	1555	000		
727	1556	000	OUT RING	JUMP OUT OF MAINTENANCE MODE VIA THE HALL SQUAD
	1557	000		
728	1557	000	IF: PA 11	
	1558	001		
	1559	000		
	1560	000		
729	1561	000	IF: PA 11	REMOVE MANUAL BLOCK EMERGENCY AND CLEAR THE SIGNAL
	1562	000		
	1563	000		
730	1564	000	OUT RING	
	1565	000		
731	1565	000	IF: PA 11	REMOVE CLEAR FOR BUS
	1566	000		
	1567	000		
732	1567	000	OUT RING	
	1568	000		
733	1569	000	JMP POINT	
	1570	000		
	1571	000		
	1572	000		
734	1573	000	IF: PA 11	REMOVE MANUAL BLOCK EMERGENCY
	1574	000		
	1575	000		
735	1576	000	OUT RING	
	1577	000		
736	1578	000	JMP POINT	
	1579	000		
	1580	000		
	1581	000		
737	1582	000	IF: PA 11	REMOVE CLEAR FOR BUS
	1583	000		
	1584	000		
738	1585	000	OUT RING	JUMP OUT OF MAINTENANCE MODE
	1586	000		
739	1587	000	IF: PA 11	
	1588	000		
	1589	000		
740	1590	000	IF: PA 11	REMOVE AND CLEAR THE SIGNAL
	1591	000		
	1592	000		
741	1593	000	OUT RING	
	1594	000		
742	1595	000	IF: PA 11	
	1596	000		
	1597	000		
743	1598	000	OUT RING	
	1599	000		
744	1600	000	JMP POINT	
	1601	000		

745 1602 000 IF: PA 11
 746 1603 000
 747 1604 000
 748 1605 000
 749 1606 000
 750 1607 000
 751 1608 000
 752 1609 000
 753 1610 000
 754 1611 000
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 996 1853 000
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 998 1855 000
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 1000 1857 000

1616	09		
1617	01		
745 1620	006	NOF72	L 1 5
1621	006		
746 1622	007		L A P
1623	007		
747 1624	008		NO 10
1625	008		
748 1626	009	LIZ NOF7X	NO 30 TO DIGIT 7 ROUTINE.
1627	009		
749 1628	010		
1629	010		
750 1630	011	LCI 2	OFFSET ADDRESS CALCULATED BY ADDING THE
1631	011		
751 1632	012		FINISH ADDRESS POINTER TO TEMPORARY PLUS
1633	012		
752 1634	013	ADD1	LD A
1635	013		
753 1636	014		LD A
1637	014		
754 1638	015		LD A
1639	015		
755 1640	016		LD A
1641	016		
756 1642	017		LD A
1643	017		
757 1644	018		LD A
1645	018		
758 1646	019		LD A
1647	019		
759 1648	020		LD A
1649	020		
760 1650	021		LD A
1651	021		
761 1652	022		LD A
1653	022		
762 1654	023		LD A
1655	023		
763 1656	024		LD A
1657	024		
764 1658	025		LD A
1659	025		
765 1660	026		LD A
1661	026		
766 1662	027		LD A
1663	027		
767 1664	028		LD A
1665	028		
768 1666	029		LD A
1667	029		
769 1668	030		LD A
1669	030		
770 1670	031		LD A
1671	031		
771 1672	032		LD A
1673	032		
772 1674	033		LD A
1675	033		
773 1676	034		LD A
1677	034		
774 1678	035		LD A
1679	035		
775 1680	036		LD A
1681	036		
776 1682	037		LD A
1683	037		
777 1684	038		LD A
1685	038		
778 1686	039		LD A
1687	039		
779 1688	040		LD A
1689	040		
780 1690	041		LD A
1691	041		
781 1692	042		LD A
1693	042		
782 1694	043		LD A
1695	043		
783 1696	044		LD A
1697	044		
784 1698	045		LD A
1699	045		
785 1700	046		LD A
1701	046		
786 1702	047		LD A
1703	047		
787 1704	048		LD A
1705	048		
788 1706	049		LD A
1707	049		
789 1708	050		LD A
1709	050		
790 1710	051		LD A
1711	051		
791 1712	052		LD A
1713	052		
792 1714	053		LD A
1715	053		
793 1716	054		LD A
1717	054		
794 1718	055		LD A
1719	055		
795 1720	056		LD A
1721	056		
796 1722	057		LD A
1723	057		
797 1724	058		LD A
1725	058		
798 1726	059		LD A
1727	059		
799 1728	060		LD A
1729	060		
800 1730	061		LD A
1731	061		
801 1732	062		LD A
1733	062		
802 1734	063		LD A
1735	063		
803 1736	064		LD A
1737	064		
804 1738	065		LD A
1739	065		
805 1740	066		LD A
1741	066		
806 1742	067		LD A
1743	067		
807 1744	068		LD A
1745	068		
808 1746	069		LD A
1747	069		
809 1748	070		LD A
1749	070		
810 1750	071		LD A
1751	071		
811 1752	072		LD A
1753	072		
812 1754	073		LD A
1755	073		
813 1756	074		LD A
1757	074		
814 1758	075		LD A
1759	075		
815 1760	076		LD A
1761	076		
816 1762	077		LD A
1763	077		
817 1764	078		LD A
1765	078		
818 1766	079		LD A
1767	079		
819 1768	080		LD A
1769	080		
820 1770	081		LD A
1771	081		
821 1772	082		LD A
1773	082		
822 1774	083		LD A
1775	083		
823 1776	084		LD A
1777	084		
824 1778	085		LD A
1779	085		
825 1780	086		LD A
1781	086		
826 1782	087		LD A
1783	087		
827 1784	088		LD A
1785	088		
828 1786	089		LD A
1787	089		
829 1788	090		LD A
1789	090		
830 1790	091		LD A
1791	091		
831 1792	092		LD A
1793	092		
832 1794	093		LD A
1795	093		
833 1796	094		LD A
1797	094		
834 1798	095		LD A
1799	095		
835 1800	096		LD A
1801	096		
836 1802	097		LD A
1803	097		
837 1804	098		LD A
1805	098		
838 1806	099		LD A
1807	099		
839 1808	100		LD A
1809	100		
840 1810	101		LD A
1811	101		
841 1812	102		LD A
1813	102		
842 1814	103		LD A
1815	103		
843 1816	104		LD A
1817	104		
844 1818	105		LD A
1819	105		
845 1820	106		LD A
1821	106		
846 1822	107		LD A
1823	107		
847 1824	108		LD A
1825	108		
848 1826	109		LD A
1827	109		
849 1828	110		LD A
1829	110		
850 1830	111		LD A
1831	111		
851 1832	112		LD A
1833	112		
852 1834	113		LD A
1835	113		
853 1836	114		LD A
1837	114		
854 1838	115		LD A
1839	115		
855 1840	116		LD A
1841	116		
856 1842	117		LD A
1843	117		
857 1844	118		LD A
1845	118		
858 1846	119		LD A
1847	119		
859 1848	120		LD A
1849	120		
860 1850	121		LD A
1851	121		
861 1852	122		LD A
1853	122		
862 1854	123		LD A
1855	123		
863 1856	124		LD A
1857	124		
864 1858	125		LD A
1859	125		
865 1860	126		LD A
1861	126		
866 1862	127		LD A
1863	127		
867 1864	128		LD A
1865	128		
868 1866	129		LD A
1867	129		
869 1868	130		LD A
1869	130		
870 1870	131		LD A
1871	131		
871 1872	132		LD A
1873	132		
872 1874	133		LD A
1875	133		
873 1876	134		LD A
1877	134		
874 1878	135		LD A
1879	135		
875 1880	136		LD A
1881	136		
876 1882	137		LD A
1883	137		
877 1884	138		LD A
1885	138		
878 1886	139		LD A
1887	139		
879 1888	140		LD A
1889	140		
880 1890	141		LD A
1891	141		
881 1892	142		LD A
1893	142		
882 1894	143		LD A
1895	143		
883 1896	144		LD A
1897	144		
884 1898	145		LD A
1899	145		
885 1900	146		LD A
1901	146		
886 1902	147		LD A
1903	147		
887 1904	148		LD A
1905	148		
888 1906	149		LD A
1907	149		
889 1908	150		LD A
1909	150		
890 1910	151		LD A
1911	151		
891 1912	152		LD A
1913	152		
892 1914	153		LD A
1915	153		
893 1916	154		LD A
1917	154		
894 1918	155		LD A
1919	155		
895 1920	156		LD A
1921	156		
896 1922	157		LD A
1923	157		
897 1924	158		LD A
1925	158		
898 1926	159		LD A
1927	159		
899 1928	160		LD A
1929	160		

770 RT-11 RT-11 NADRO UN02-10 00113125 PAGE 01

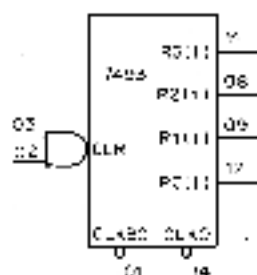
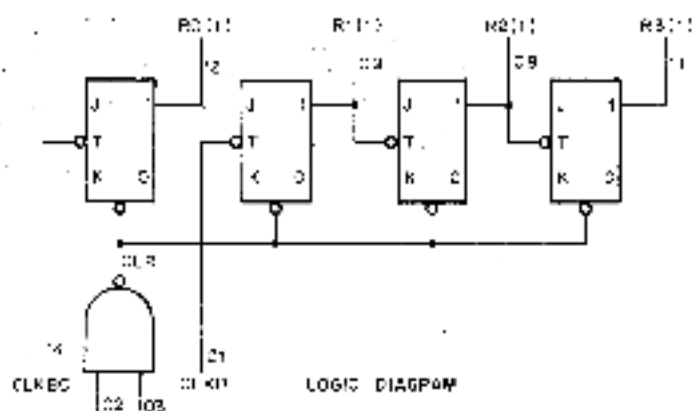
• 015- 001872 100
000000 00

FREE CASE: 2480, HERDES

TEXT,TEXT=9:038E,TEXT

APPENDIX B
IC DESCRIPTIONS

7493 BINARY COUNTER



7493A Pin 14
GND Pin 7

7493 TRUTH TABLE
(SEE NOTES)

INPUT DEC	P1 (103)	OUTPUT		
		QA (1)	QB (2)	QC (3)
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

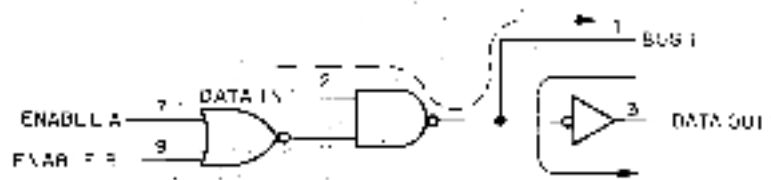
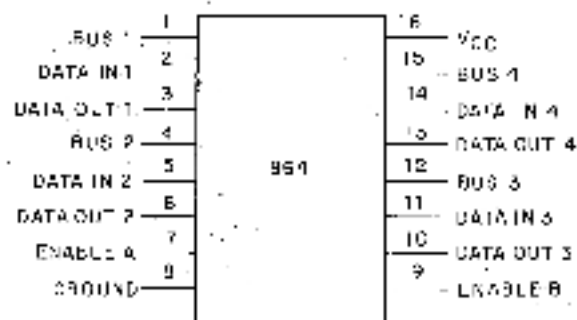
0 = LOW 1 = HIGH

Notes

1. Truth table applies when 7493 is used as 4-bit counter. (See pin 103.)
2. Output QA (1) is connected to input 103.
3. To use all 4 outputs, input 103 must be high.
4. Output QA (1) is connected to input 103.

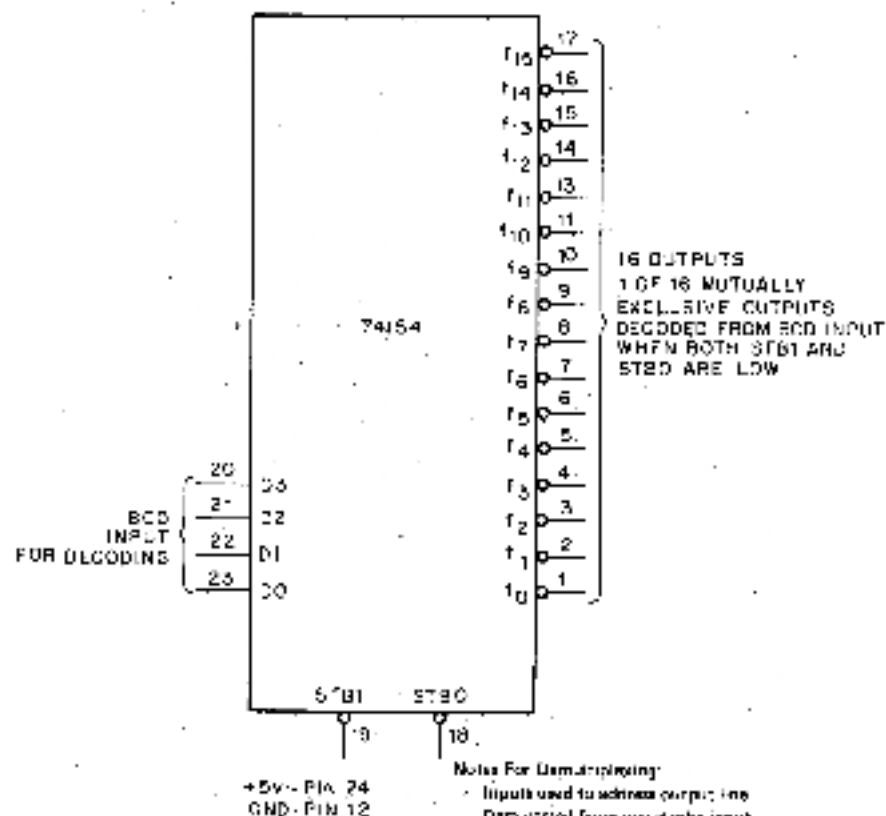
8641 QUAD BUS TRANSCEIVER

The 8641 consists of four identical receiver/drivers and a single enabling gate in one package for interfacing with the PDP-11 Unibus. The transceiver drivers are enabled when ENABLE A and ENABLE B are both low. The other input of each driver is connected to the data to be sent to the Unibus. For example, when enabled, DATA IN 1 (pin 2) is read to the Unibus via BUS 1 (pin 1). During a write operation, data comes from the Unibus as BUS 1 (pin 1) and is passed through the receiver to the device as DATA OUT 1 (pin 3).



74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



Notes For Demultiplexing:

- Inputs used to address output line
- Data passed from one strobe input with other strobe held low. Either strobe high gives all high outputs.

IC-74154

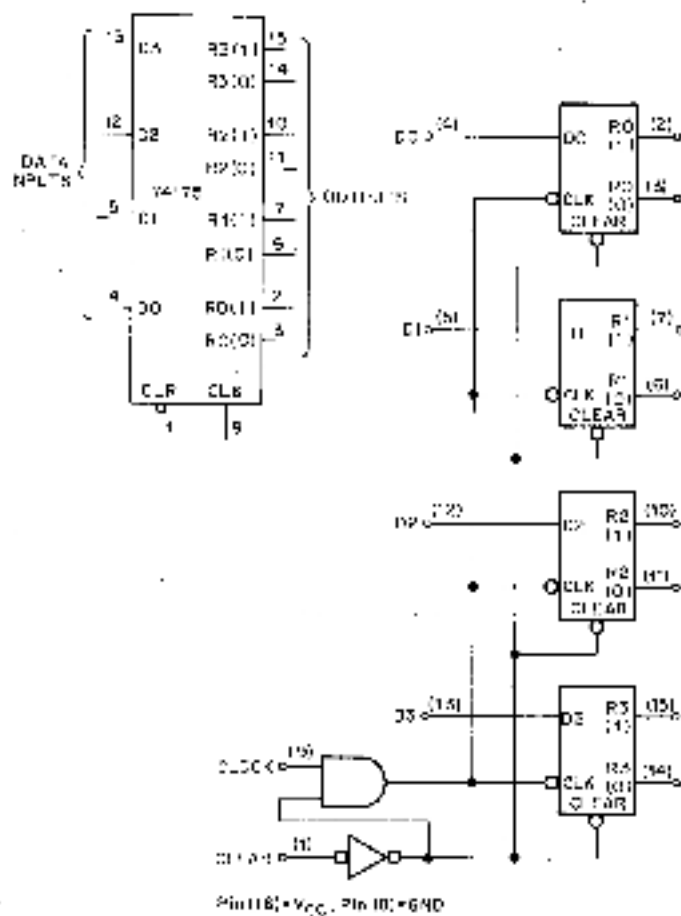
74175 QUAD STORAGE REGISTER

TRUTH TABLE

INPUT I_n	OUTPUTS Q_{n+1}
D	$P_n(I_n)Q_n$
H	F L
L	L H

t_{H-30} = 30 ns before clock pulse.

t_{L+30} = 30 ns after clock pulse.



1C 74175

Reader's Comments

KY11-LB Programmer's Console/Interface
Module Operation and Maintenance Manual
EK-KY11LB-MM-001

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