digital LSI-11

PDP-11/03

MAINTENANCE CARD

ODT COMMANDS

Format	Description
(CR)	Close current location and open next sequential location.
↑ (↑)	Close current location and open previous location, or (↑↑).
' or `	Open word at location in GPR.
nnnnnn	Take octal value nnnnnn, open location. Index by contents of PC and open that location.
@	Take octal value of word. Open location as above and open that location.
/	Open the word at location 0.
/	Reopen the last location.
$ / or $ nn	Open general register n [R-0 or R-7 if no n specified].
G or nnnnG	Go to location and start program.
nnnnL	Load an hexadecimal bootstrap program into device CSR. Current value set is 177560.
P or nnnnP	Proceed with program execution.
RUBOUT or DELETE	Erase previous numeric character. Response is a question mark [?].
S	Print internal register contents. Data indicates how CPU arrived at ODT. XXXXXX where: Value = 4 Halt instruction or BPT trap (BUS ERR). 1 or 3 Breakpoint trap. 2 or 8 Successful completion of T-bit. 5 Double bus error (stack overflow, non-existent stack). 6 Reserved instruction trap. 7 Condition 1, 2, 4 occurred. * Register value can be displayed only if CPU condition code is set.
T	Set trace trap. Trace one instruction and print registers.
nnnnT	Set trace trap. Trace nnnn instructions and print registers.
U	Print octal value of word at location.

* Register value can be displayed only if CPU condition code is set. To display register value immediately, this command must be executed immediately.

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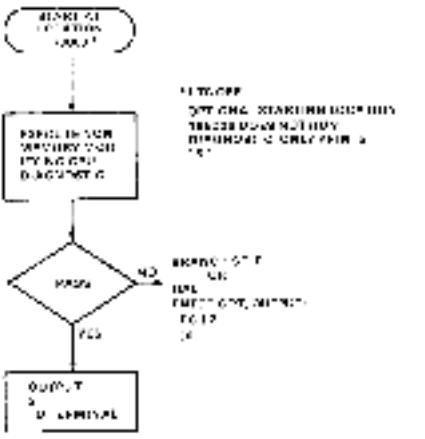
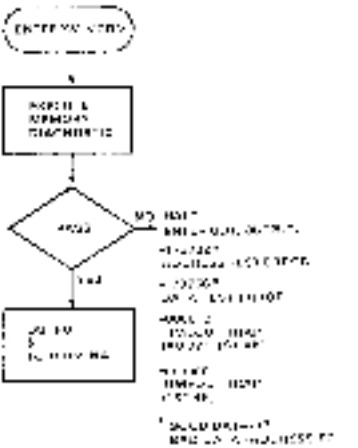
SWITCH REGISTER TO DIGITAL CONVERSION

SWITCH	VALUE
0	1
1	2
2	4
3	10
4	20
5	40
6	100
7	200
8	400
9	1000
10	2000
11	4000
12	10000
13	20000
14	40000
15	100000

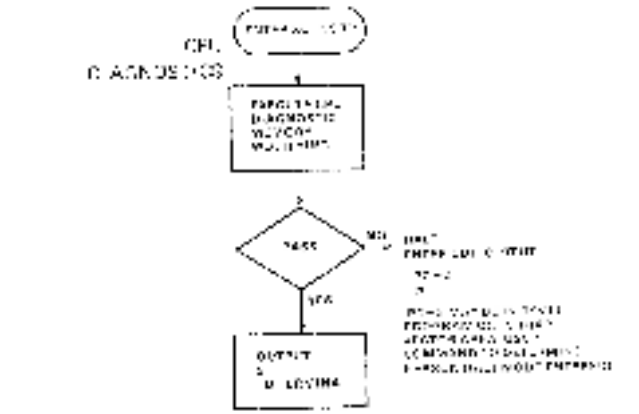
REV11 STARTUP FLOWCHART

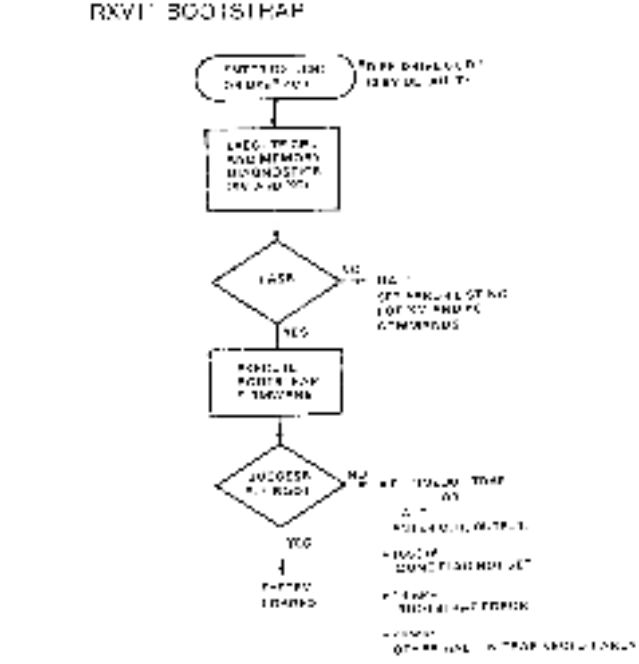


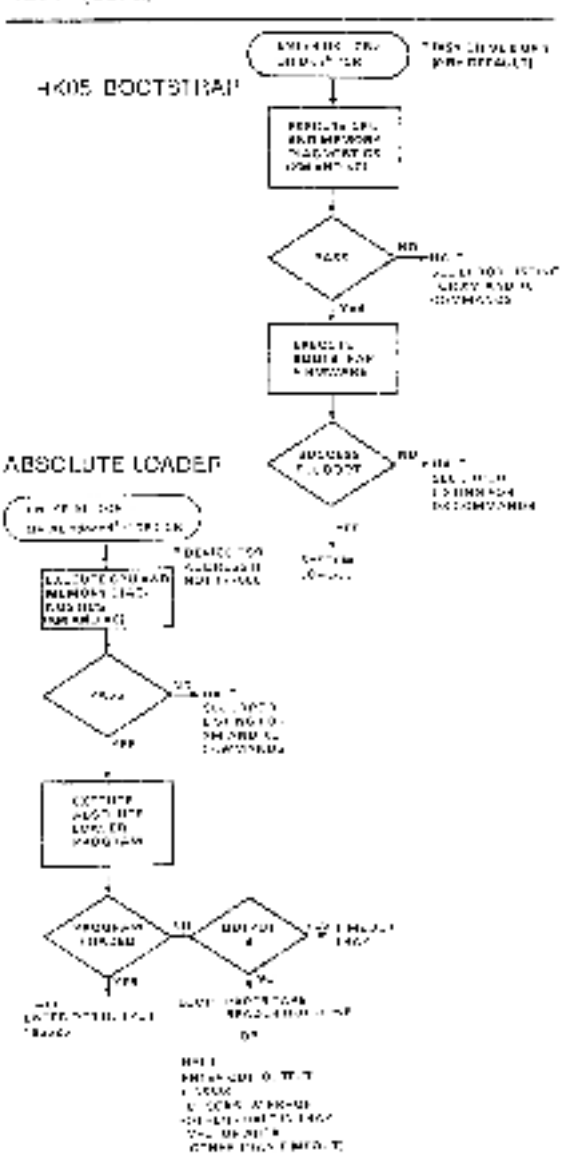
MEMORY DIAGNOSTIC



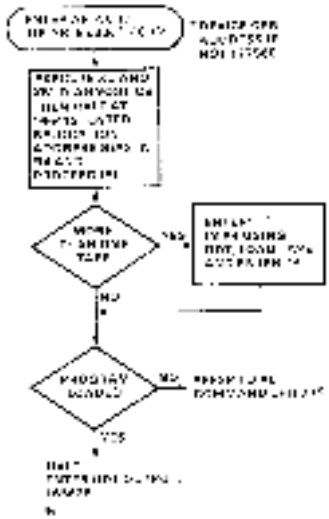
ODT



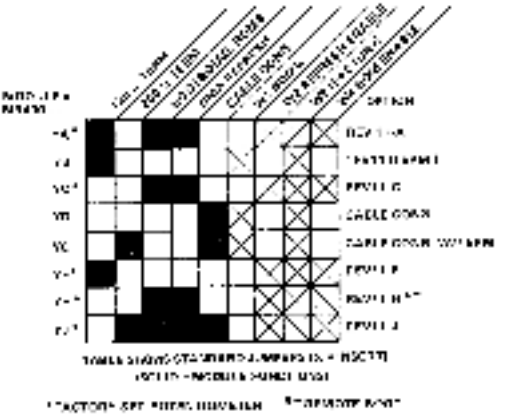



4K05 BOOTSTRAP
ABSOLUTE LOADER

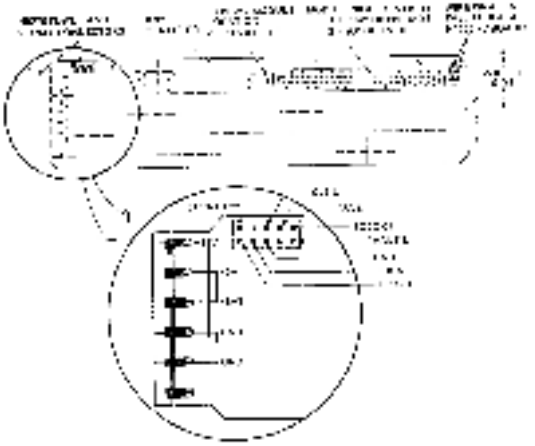
ABSOLUTE LOADER (RELOCATED)



MODULE VERSIONS AND JUMPERS



HB270 PIN IDENTIFICATION

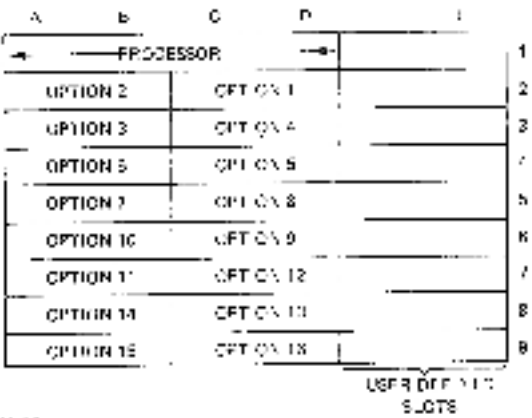


HB270

A	B	C	D
PROFESSIONAL MODULE			
OPTION 2		OPTION 1	
OPTION 3		OPTION 4	
OPTION 6		OPTION 5	

NOTE 1: Unused slots may be used for Euroconnex
BIAK (0)
BIDIG (0)

DDW11-B



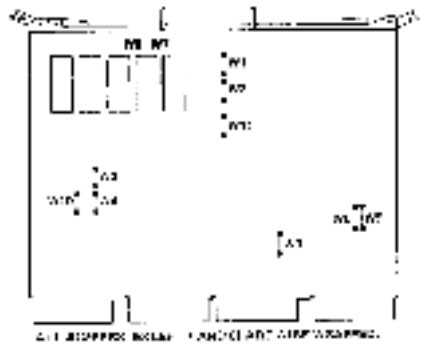
NOTE 1. Unused slots require backplane jumpers for
BBSKI/O L
BDMGI/O L

NOTE 2. A terminator is required in the last unused option slot. If 7 to 15 volt cards are installed, the module must be removed.

MULTIPLE BACKPLANE CONFIGURATION

NUMBER OF BA23 BACKPLANES	BACKPLANE OPTION DW11B-XA* 1st to 2nd	DW11A-XX* 2nd to 3rd	3rd
2	W9400 YE to W9401	W9400 YE to W9401	
3	W9400 YE to W9401	W9400 YE to W9401	W9400 YE to W9401

*NOTE: XX denotes cable length. DW11B-XA and DW11A-XX cables must be ordered separately. Different lengths may be used.



M7264 ETCH REV 1 (AND LATER)

M7264 ETCH REV C, D (NOT FOR NEW DESIGNS)

DESIGN IDENTIFICATION

	MICROSYSTEMS	PDP-11/03	PDP-11/23
MOS	KD11-H	KD11-A	KD11-Q
NMOS	KD11-F	KD11-L	KD11-P

ALLOCATION OPTIONS

REGISTER MEMORY ADDRESSING

INVOKED BY:

Bank	A15	W7
0	0	1
1	1	0
Not addressed	0	0

FETCH INTERVAL

	W5
Fetch A	0
Skip fetch	1

PROCESSOR HALT MASK

	W4
Enable	0
Disable	1

POWER UP

MODE	W3	W2
0 — to 24	1	0
1 — to 28T	1	0
2 — to 773000	0	1
3 — to special	1	1

Dynamic mode = Factory Set

KD11-F, -E AND -ABOVE ONLY JUMPERS

	Jumper	Enable	Disable
BOOTSTRAP	W3, W8	FACTORY	FACTORY
CONSOLE PROTOCOL MEMORY			
ENABLE	W9	0	1
REFRESH REPLY	W10	0	1
MEMORY SELECT	W11	1	0

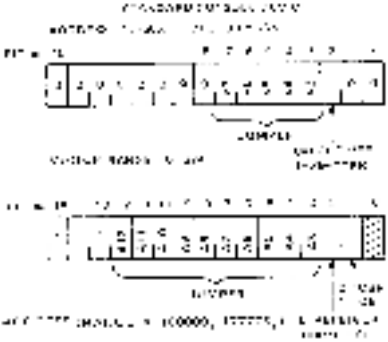
S-71	C51	A5	M-3	2019
16k	1	1		1
2K	1			1
8K		1	5	0
1K		8	1	8

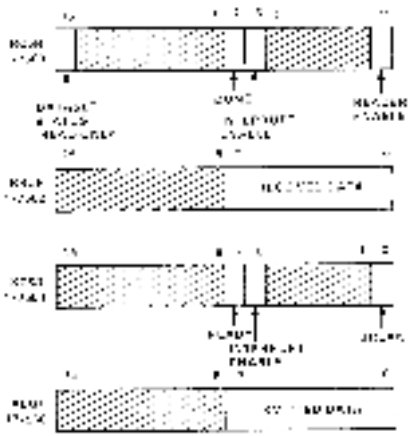
M-1, 2, 3, and M-Century Tests p. 444
MEMTEST 86 | Windows | p. 99 | 1997-
2006 (Disc utilized 4K, 19 Euv
Chromium, Fedora Gen. [subtitle]

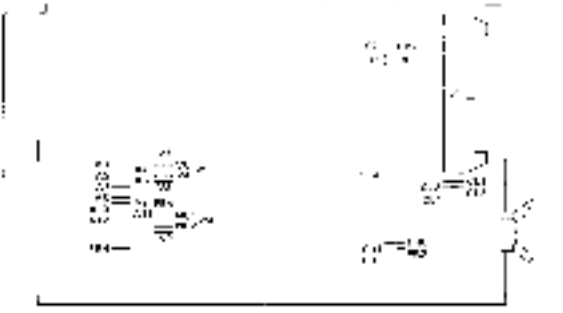
MEM-1-2			[illegible]			MEM-1-3				[illegible]	[illegible]
[illegible]			[illegible]			[illegible]					
M1	M2	M3	[illegible]			[illegible]					
1		1	0	0	1		0	1	0	1	1
		1	1	0	1	1	0	1	1	1	[illegible]
1	1		0	1	1		0	1	0	1	[illegible]
1	1	1	1	1	0		0	1	1	1	[illegible]
0			0	0	1		1	0	1	0	[illegible]
0			1	0	1		1	0	1	0	[illegible]
1	1		0	1	1	1	1	1	0	0	[illegible]

[illegible] [illegible]
[illegible]

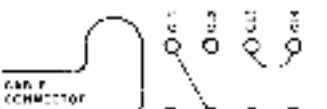
SWITCH [illegible]
1 [illegible] 0 [illegible]
0 [illegible] 1 [illegible]







XMIT/RECEIVE MODE



DLV11 (Cont.)

PARITY

	PSV	NP
ENABLE (W)	1	
(R)	0	
DISABLE		0

BREAK

	0
ENABLE	
DISABLE	0

DATA FORMAT

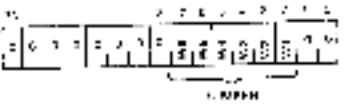
NO. OF BITS	SB	XB1	XB2
5	1	1	
6	1	1	
7	1	0	
8	0	0	

NO. OF STOP BITS	SB
1	1
2	1

NOTE: * FOR LT33 (A) OR LT33 (A)BD, MAINTAIN A MINIMUM OF 1 SPACE BETWEEN TPS AND TPB.

+ DATA CABLE BD09A-X

o 20 mA CURRENT LOOP CABLE BC05M-X



DCL

COMMAND FUNCTIONS

000	[illegible]
001	[illegible] Buffer
010	Write Buffer
011	Write Error
011	Test Receiver
100	Reserved
101	Reset Status
110	Write Station with related data
111	Read Error Code

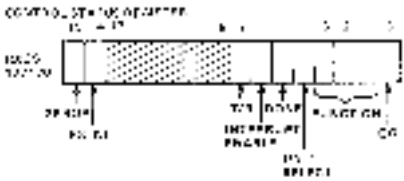
COMMAND PROTOCOL

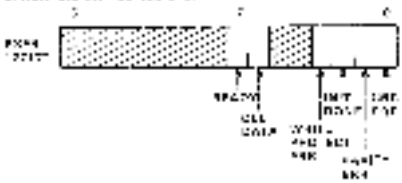
Test Status

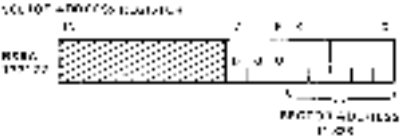
1. Issue Function and DCL
2. Wait for Ready
3. Check Status for Error

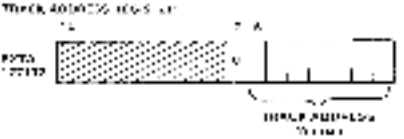
Read Error Code Protocol

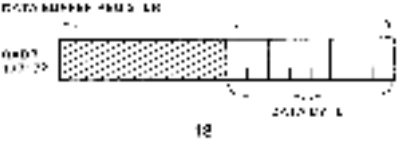
1. Issue Function and DCL
2. Wait for Ready
3. Check Status for Error Bit Set







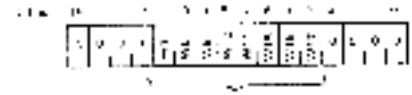


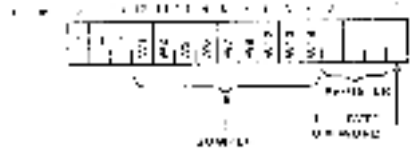


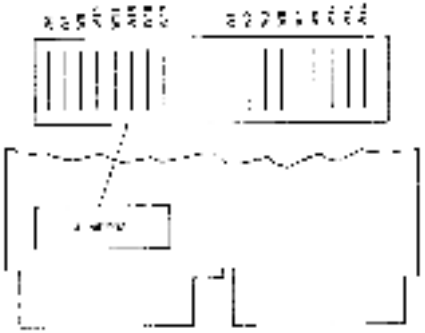
ERROR CODES AND WARNINGS

[illegible]

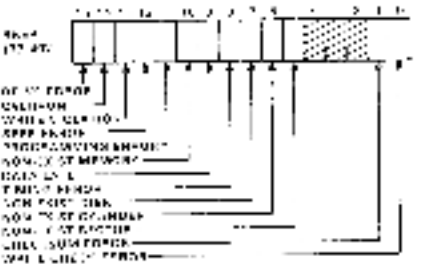
[illegible]







[illegible]



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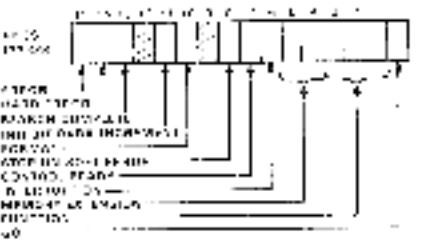

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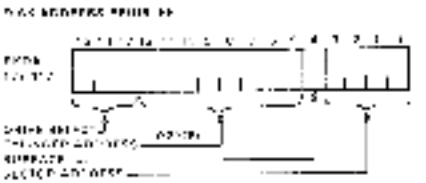

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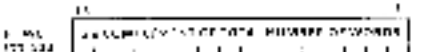
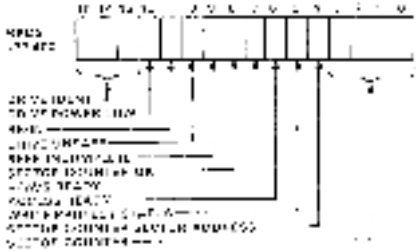
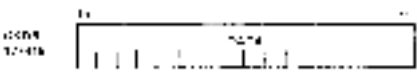


[illegible]

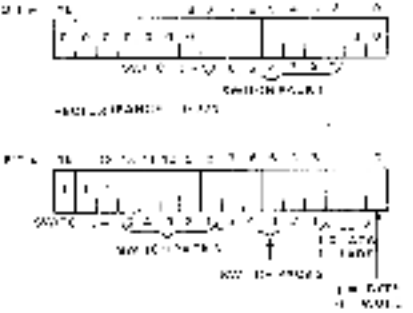


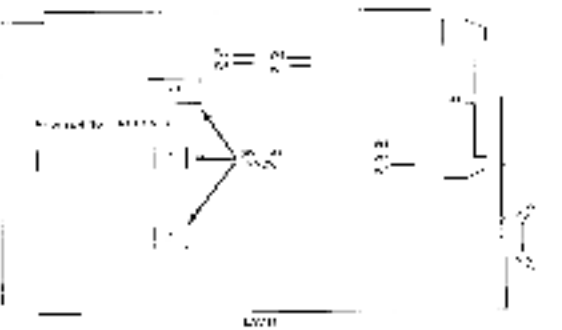


[illegible]

[illegible]

[illegible]





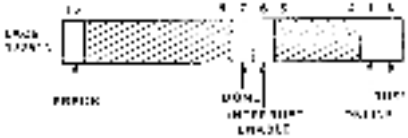
LOOPBACK CONFIGURATION

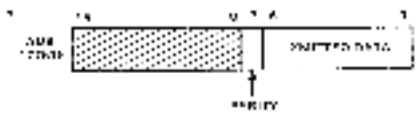
[illegible]	[illegible][1]	[illegible][2]
[illegible]		
[illegible]		[illegible]
[illegible]	[illegible]	
[illegible]	[illegible]	[illegible]
[illegible]		
[illegible]	[illegible]	[illegible]
[illegible]		

[illegible] [illegible]

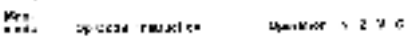
(Values: 01, 101A, 1001, 1010A, 200.

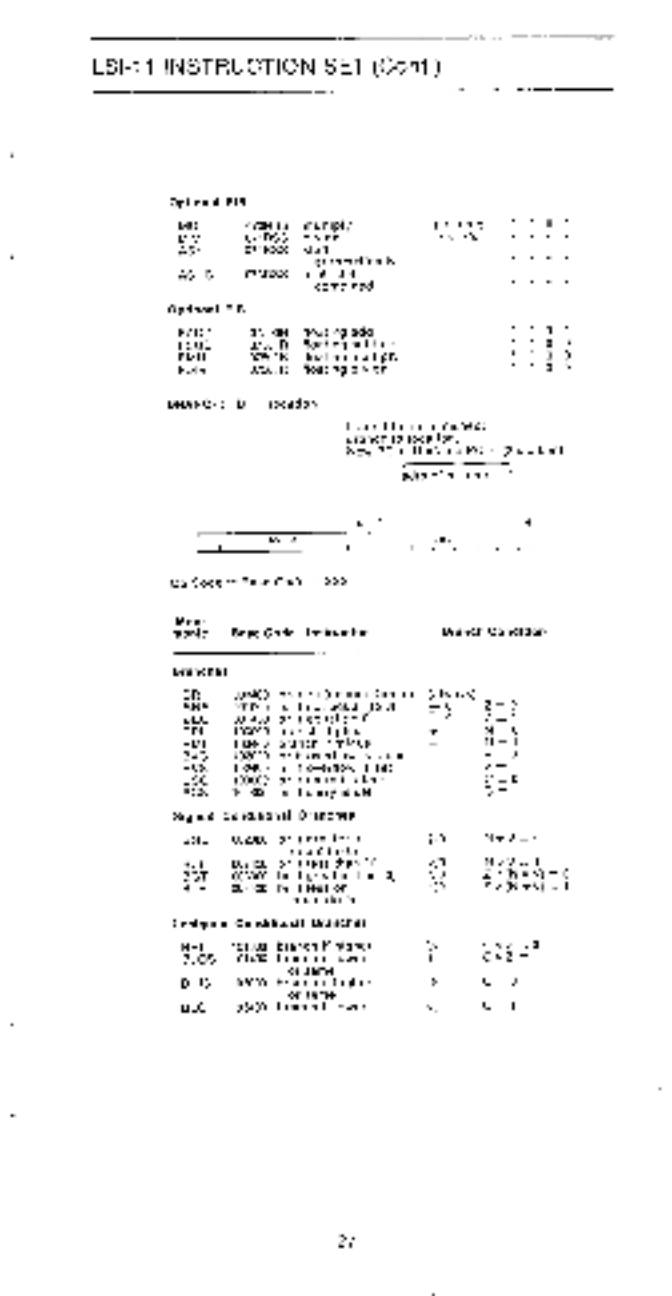
2 CAUTION [illegible]





LSI-11 INSTRUCTION SET (Cont.)





JUMP & RETURN

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	[illegible]	[illegible]
JSR	004RDD	[illegible]	[illegible]
RTS	00020R	[illegible]	[illegible]
MARK	0064nn	[illegible]	[illegible]
SPL	0023Dn	[illegible]	[illegible]

TRAP & INTERRUPT

Mnemonic	Op Code	Instruction	Notes
BPT	000003	[illegible]	[illegible]
IOT	000004	[illegible]	[illegible]
RTI	000002	[illegible]	[illegible]
EMT	104000	[illegible]	[illegible]
TRAP	104400	[illegible]	[illegible]

MISCELLANEOUS

Mnemonic	Op Code	Instruction
HALT	000000	[illegible]
WAIT	000001	[illegible]
RESET	000005	[illegible]
CCC	000257	[illegible]
NOP	000240	[illegible]

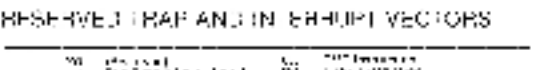
CONDITION CODE OPERATORS

[illegible]

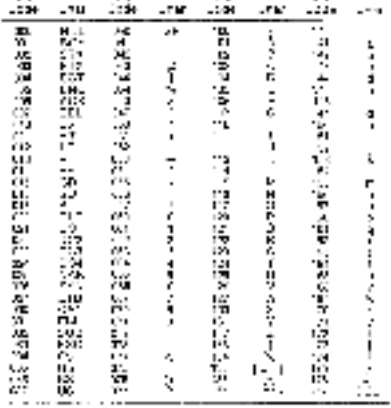
Mnemonic	Op Code	Instruction	N	Z	V	C
CLC	000241	[illegible]				0
CLV	000242	[illegible]			0	
CLZ	000244	[illegible]		0		
CLN	000250	[illegible]	0			
CCC	000257	[illegible]	0	0	0	0
SEC	000261	[illegible]				1
SEV	000262	[illegible]			1	
SEZ	000264	[illegible]		1		
SEN	000270	[illegible]	1			
SCC	000277	[illegible]	1	1	1	1

LSI-11 INSTRUCTION SET (Cont'd)

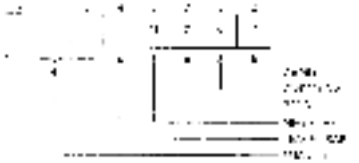
RESERVED TRAP AND INTERRUPT VECTORS



7-BIT ASCII CODE



PROCESSOR STATUS WORD



NOTES:

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digital

EQUIPMENT
CORPORATION

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