EK-LSIFS-SV-005

LSI-11 Systems Service Manual

Volume II

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LSI-11	Rainbow	Work Processor
MASSBUS	RSTS	

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AAV11-A DIGITAL-TO-ANALOG CONVERTER

Amps		Bus Loads		Cables
1 A	1 P	AC	DC	
1 A	0.4	1.91	1	BC04Z BC04R BC11V BC08P used with H9273

Standard Addresses

DAC1	170440
DAC2	170442
DAC3	170444
DAC4	170446

Vectors

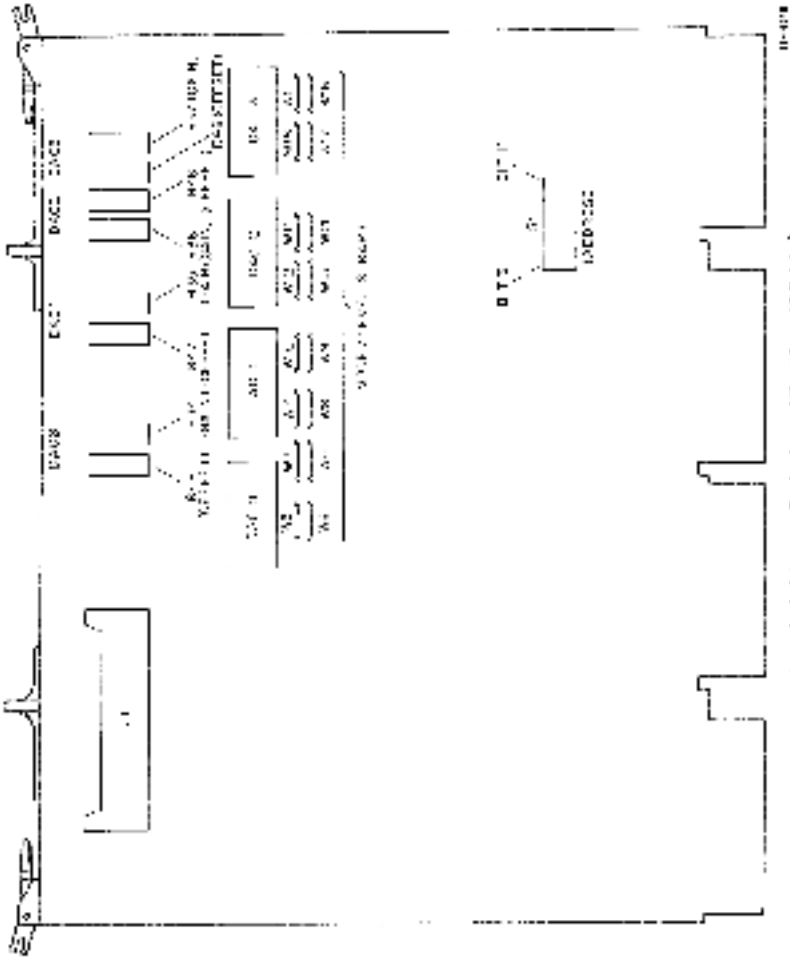
None. The AAV11 does not cause interrupts.

Diagnostic Programs

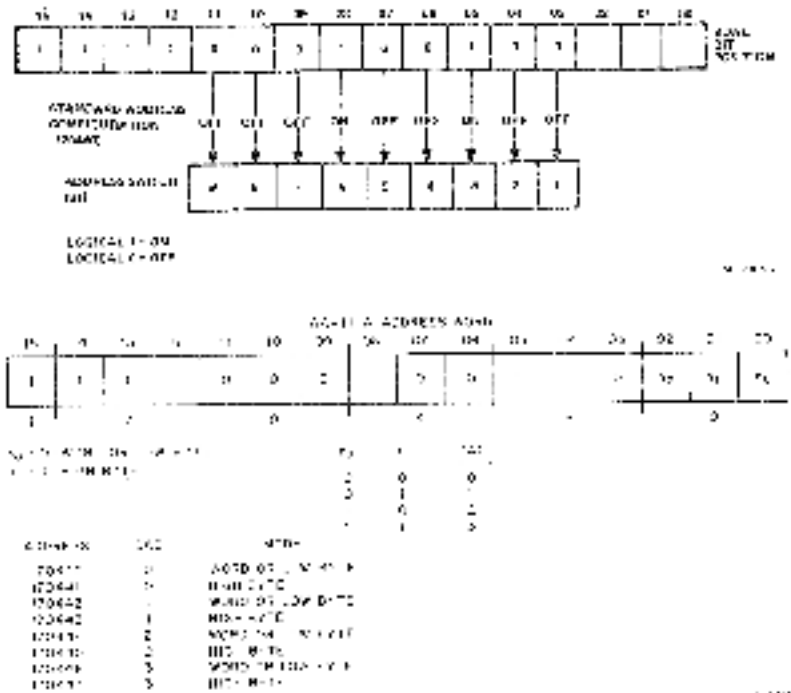
Refer to Appendix A.

Related Documentation

AAV11-A, KAV11-A, AAV11-A, DRV11 User's Manual (EK-AAV11-OP)
Field Maintenance Print Set (MP001968)
Microcomputer Interfaces Handbook (EB-20175-20)



AAV11-A Address Switches (Set for 170464)



AAV11 A Address Decoding

Jumper Configurations for Bipolar Operation (as Shipped)

	± 2.56 V	± 5.12 V	± 10.24 V
DAC1			
W3	IN	IN	OUT
W4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC2			
W7	IN	IN	OUT
W8	OUT	OUT	IN
W9	IN	OUT	OUT
W10	IN	IN	IN
DAC3			
W11	IN	IN	OUT
W12	OUT	OUT	IN
W13	IN	OUT	OUT
W14	IN	IN	IN
DAC4			
W15	IN	IN	OUT
W16	OUT	OUT	IN
W17	IN	OUT	OUT
W18	IN	IN	IN

Jumper Configurations for Unipolar Operation

	0 V ~ 5.12 V	0 V ~ 10.24 V
DAC1		
W4	IN	IN
W5	OUT	OUT
W6	IN	OUT
W8	OUT	OUT
DAC2		
W7	IN	IN
W8	OUT	OUT
W9	IN	OUT
W10	OUT	OUT
DAC3		
W11	IN	IN
W12	OUT	OUT
W13	IN	OUT
W14	OUT	OUT
DAC4		
W15	IN	IN
W16	OUT	OUT
W17	IN	OUT
W18	OUT	OUT

AAV11-A Input Code/Output Voltage Relationship

Input Code	Unipolar	Bipolar
0000	0 V	−FS
4000	1/2 FS	0 V
7FFF	+FS − 1/2 LSB	+FS − 1/2 LSB

AAV11-C DIGITAL-TO-ANALOG CONVERTER

Power Requirements

+5 V b.. @ 2.5 A

Bus Loads

AC	DC
0.9	-

Standard Addresses

DAC A	170440
DAC B	170442
DAC C	170444
DAC D	170446

Vectors

None. The AAV11-C does not request interrupts.

Diagnostic Programs

Refer to Appendix A.

Related Documentation

LSI-11 Analog System User's Guide (EK-AXV11-UG)
Field Maintenance Print Set (MP01294)

CONFIGURATION

The AAV11-C has switches and two jumpers to set up the device address. The board also has jumpers to select the output voltage range for unipolar and bipolar operation.

Selecting AAV11-C Device Address

The AAV11-C device address is the I/O address assigned to the first of the four DAC registers. The user selects the device address by means of a switch pack for address bits DAL 3 - 10 and two jumpers for bits DAL 11 and DAL 12. The device address can range from 160000 to 177770 in increments of 10. The device address is usually set at 170440. A switch in the on position represents a 0; a switch in the off position represents a 1. Jumper A11 is installed to place a 0 at address bit DAL 11. Jumper A12 is removed to place a 1 at address bit DAL 12.

Selecting AAV11-C Device Address

Selecting AAV11-C Output Voltage Range

Each DAC on the AAV11-C has separate voltage range jumpers. These jumpers are located above their corresponding D/A converter IC on the printed circuit board. The jumpers to install and select the output voltage range are described in the following table.

AAV11-C Output Voltage Range Jumpers

Polarity	Output Voltage Range	Install Jumpers
Unipolar	0 to +10 V	A1 to C
Bipolar*	±10 V	A1 to B; D

* = factory configuration

PROGRAMMING THE AAV11-C

The AAV11-C has four addressable read/write registers. Each register is used by one of four digital-to-analog converters and can be addressed as one word or as two bytes, allowing complete use of the LSI-11 instruction set. The AAV11-C device address is the base address of the first register, usually 170440. The other registers are addressed in increments of 2 above the base address.

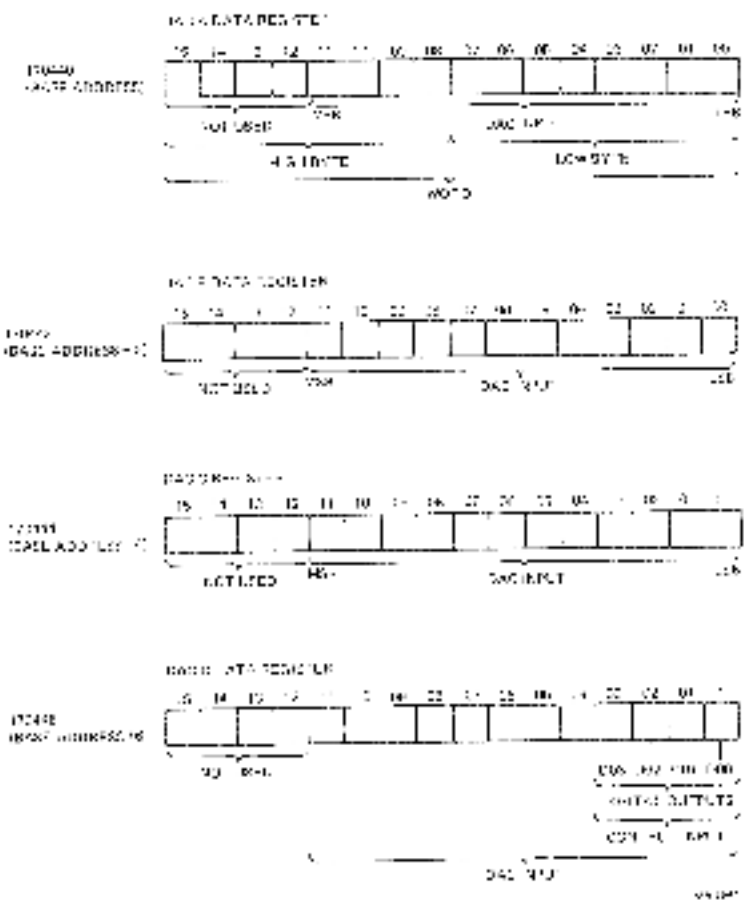
AAV11-C Address Decoding

The four registers of the AAV11-C can be written or read as one word, bits 00-11, or as two bytes, bits 00-07 (low byte) and bits 08-11 (high byte). When the specific register is addressed, it forms the DAC DATA and controls the output of the board.

The output of the board can be configured for either straight binary notation for unipolar operation or offset binary notation for bipolar operation.

The fourth DAC register has four bits that may be used for control signals. Bits 00-03 of this register are routed to the I/O connector on the board for use as CRT intensity, blank, erase, etc. Check the CRT installation manual to find out which bits are connected to the CRT circuits.

Control instructions in these four bit positions affect the output of any 12 bit D/A conversion that occurs on this register at the same time. However, because they use only the least significant bits of the word, the error is less than 0.4 percent of the full-scale value.



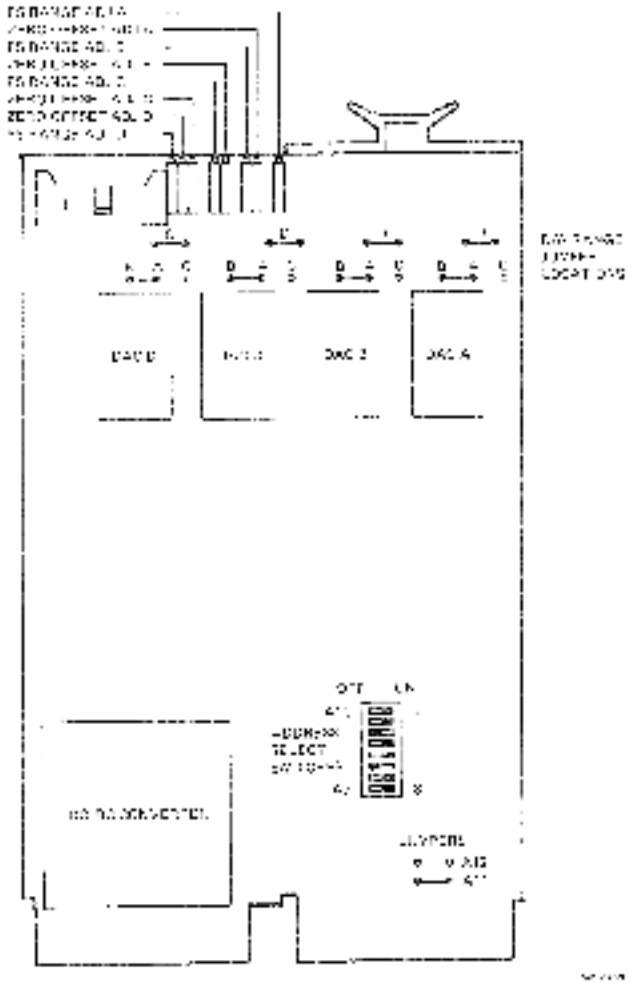
AAV11-C Four DAC Registers

I/O INTERFACE

The I/O interface signals use a 3M #3421-7020 connector and are defined in the following table.

AAV11-C Connector J1 Pin Assignments

Pin	Signal	Pin	Signal
1	DCO H	2	D GND
3	DO1 H	4	D GND
5	DO2 H	6	D GND
7	DO3 H	8	D GND
9		10	
11	A GND	12	A GND
13	DAC D OUT	14	A GND
15	DAC C OUT	16	A GND
17	DAC B OUT	18	A GND
19	DAC A OUT	20	A GND



AAV11-C Module Layout

ADV11-A ANALOG-TO-DIGITAL CONVERTER

Amps		Bus Loads		Cables
+5	-12	AC	DC	
2.0	0.45	3.25	1	BC11A-Z BC05R BCV11 BC05T used with LA30

Standard Addresses

CSR	170400
DBR	170402

Vectors

A/D Done	400
Error	404

Diagnostic Programs

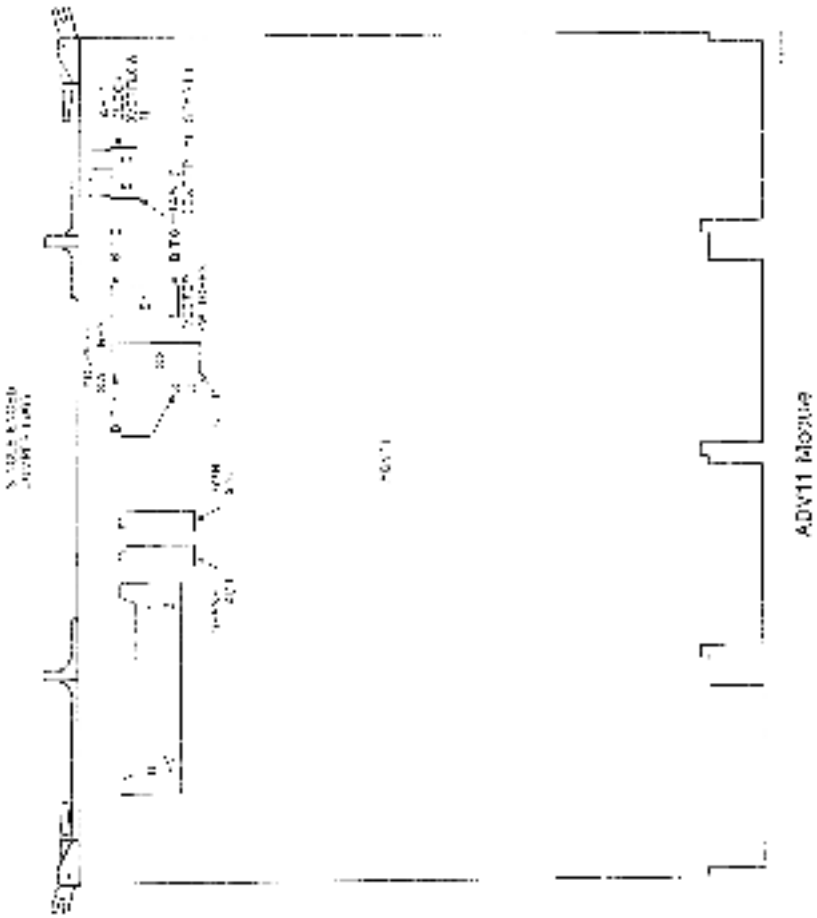
Refer to Appendix A

NOTE

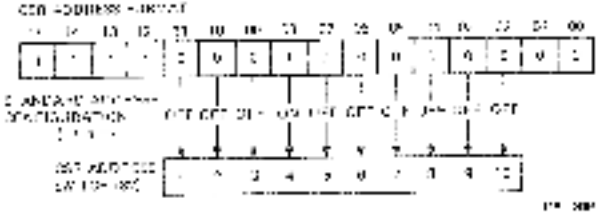
CVADA?? and CXADC?? tests require wraparound connector PN 70-12894.

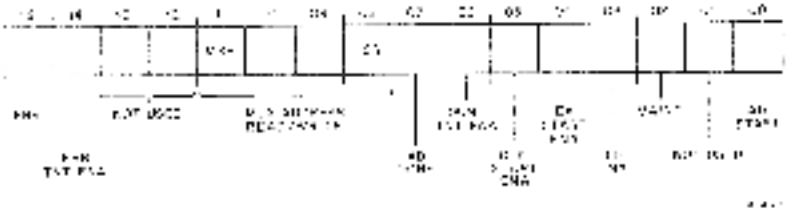
Related Documentation

ADV11-A, KMV11-A AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00102)
Microcomputer Interfaces Handbook (EB-20175-20)


ADV11 Module

Jumper W3 is inserted for single-ended operation and removed for quasi-differential operation.





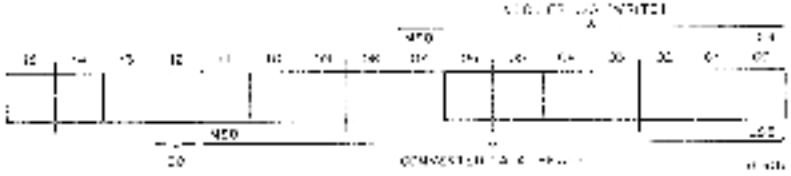
ADV11-A Control/Status Register (CSR)

CSR Bit Definition

Bit	Function
15	A/D Error (read/write) – The A/D Error may be program set or cleared and is cleared by the processor initialize. It is set by any of the following: a. attempting an external or clock start during the transition interval b. attempting any start during a conversion in progress c. failing to read the result of a previous conversion before the end of the current conversion.
14	Error Interrupt Enable (read/write) – When set, enables a program interrupt upon an error condition (A/D Error). Interrupt is generated whenever bits 14 and 15 are set, regardless of which was set first.
13, 12	Not used.
11–8	Multiplexer Address (read/write) – Contain the number of the current analog input channel being addressed.
07	A/D Done (read) – Set at the completion of a conversion when the data buffer is updated. Cleared when the data buffer is read, and by the processor initialize. If enabled, interrupts are requested simultaneously by bits 07 and 15, bit 07 has the higher priority.
06	Done Interrupt Enable (read/write) – When set, enables a program interrupt at the completion of a conversion (A/D Done). Interrupt is generated when bit 07 and bit 06 are both set, regardless of sequence.
05	Clock Start Enable (read/write) – When set, enables conversions to be initiated by an overflow from the clock option.
04	External Start Enable (read/write) – When set, enables conversions to be initiated by an external signal or through a Schmitt trigger from the clock option.
03	ID Enable (read/write) – When set, causes bit 12 of the data buffer register to be loaded to a 1 at the end of any conversion.

CSR Bit Definition (Cont)

Bit	Function
02	Maintenance (read/write) – Loads, when set, all bits of the converted data output equal to multiplexer address LSB (bit 08) at the completion of the next conversion. Cleared by the processor initialize. Used for "all 0s" and "all 1s" tests of A/D conversion logic.
01	Not used.
00	A/D Start (read/write) – Initiates a conversion when set. Cleared at the completion of the conversion and by the processor initialize.



ADV11-A Data Buffer Register (DBR)

DBR Bit Definition

The DBR is actually two separate registers: one read only, the other, write only.

Bit	Function
Read Only	(Cleared at processor initialize.)
15–13	Not used. Should read as 0.
12	ID (read) – When ID Enable (bit 03) of the CSR has been set, BDR bit 12 will be loaded to a 1 at the end of conversion.
11–00	Converted Data (read) – These bits contain the results of the last A/D conversion.
Write Only	(Set to 200 at processor initialize.)
15–08	Not used.
07–00	Vernier D/A (write) – These bits provide a programmable offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200 (mid-range). Values greater than 200 make the input voltage appear more positive.

ADV11-C ANALOG-TO-DIGITAL CONVERTER

Power Requirements

+5 V (± 5%) @ 6.0 A

Bus Loads

AC	DC
1.3	1

Standard Addresses

Standard Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control status	CSR	170400	170420
Data buffer	DBR	170402	170422
Interrupt Vectors			
A/D DONE		400	410
ERROR		404	414

Diagnostic Programs

Refer to Appendix A

Related Documentation

LSI-11 Analog System User's Guide (EK-AXV11-UG)
Field Maintenance Print Set (MP01382)

ADV11 C Module Layout

CONFIGURATION

The ADV11-C has jumpers to select the device address, the interrupt vector address, and the analog configuration. The user may select the A/D input range, polarity, and the output data notation.

Selecting ADV11-C Device Address

The ADV11-C device address is the I/O address assigned to the A/D control status register. The device address is selected by jumpers A3 through A12. The jumpers allow the user to set the device address within the range of 160000 to 177770. The device address is usually set at 170400. A jumper installed decodes a 1 in the corresponding bit position, a jumper out decodes a 0.

Selecting ADV11-C Control Status Address

Selecting ADV11-C Interrupt Vector Address

The ADV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The basic interrupt vector address is assigned to A/D DONE.

The basic interrupt vector address can be set within the range of 0 to 770. It is usually set to 400 by jumpers V3 through V8.

Selecting ADV11-C Interrupt Vector Address

Selecting ADV11-C Analog Input Range, Type, and Polarity
The ADV11-C allows software control over the full-scale range selection. The effective ranges provided by the programmable gain are as follows:

Effective Input Range

Gain	Unipolar	Bipolar
1	0 V to +10 V	± 10 V
2	0 V to +5 V	± 5 V
4	0 V to +2.5 V	± 2.5 V
8	0 V to 1.25 V	± 1.25 V

The analog input type jumpers that must be installed are described in the following table. The board comes from the factory set for 16 channel, single ended, bipolar inputs.

Selecting ADV11-C Analog Input Type

Input Type	Install Jumpers
Single ended inputs*	P1 to P2, P8 to P9
Differential inputs	P2 to P3; P4 to P5

*Factory configuration

NOTE

Jumpers P6 and P7 are factory installed for the programmable gain feature and should be left in.

Selecting ADV11-C A/D Output Data Notation
The ADV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation. Refer to jumper groups D and E near the handle of the board.

Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale 0 V	007777 000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale 0 V − full scale	007777 004000 000000
2's complement	OUT	IN	IN	OUT	IN	OUT	+ full scale 0 V full scale	003777 000000 174000

*Factory configuration

Selecting Source of External Trigger

The A/D conversions within the ADV11-C can be started in one of the following three ways.

1. Under program control, using the A/D START bit in the CSR.
2. By a real-time clock input at J1, pin V1, or at pin RTC IN.
3. By an external trigger, either at J1 pin 19, or at the BEVNT line on the LSI-11 bus.

The user can select the source of the external trigger using two jumpers on the board. The jumpers installed to select the source of the external trigger are as follows:

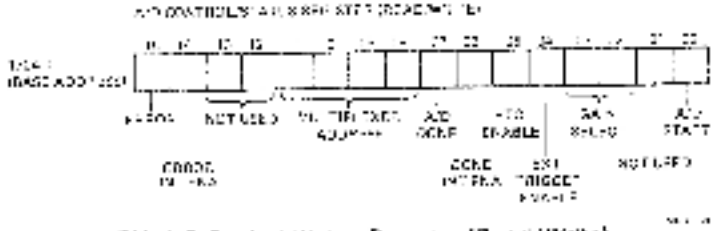
Selecting ADV11-C External Trigger

External Trigger Source	Jumpers F1	F2
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

*Factory configuration

CSR BITs

The CSR bits are as follows.



ADV11-C Control Status Register (Read/Write)

ADV11-C Control Status Register Bit Assignments

Bit	Name	Description
00	A/D START	Write only – When set, this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0
01	Not used	
02, 03	GAIN SELECT	Read/write – Set these bits to select the gain for the analog input as follows. Gain: 1 (GS1 0, GS0 0); 2 (0, 1); 4 (1, 0); 8 (1, 1)
04	EXT TRIG ENABLE	Read/write – When set, this bit allows an external trigger to start an A/D conversion.
05	RTC ENABLE	Read/write – When set, this bit allows a real-time clock input to start an A/D conversion.
06	DONE INTERRUPT ENABLE	Read/write – When set, this bit enables an interrupt on A/D DONE (bit 07). Both bits are cleared by INIT.

ADV11-C Control Status Register Bit Assignments (Cont)

Bit	Name	Description
07	A/D DONE	Read only. This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.
08 - 11	MULTIPLEXER ADDRESS	Read/write - These bits select 1 of 16 analog input channels
12-13	Not used	
14	ERROR INTERRUPT ENABLE	Read/write - When set, this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.
15	ERROR	Read/write. When set, this bit indicates that an error has occurred due to one of the following. 1. Trying an external start or clock start during multiplexer settling time. 2. Trying a start while an A/D conversion is in process. 3. Trying any start while the A/D DONE bit is set. This bit can be cleared by writing the CSR or by an INIT.

DATA BUFFER REGISTER
The data buffer register bits are as follows.

ADV11-C Data Buffer Register (Read Only)

ADV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
00–11	A/D DATA	These bits hold the parallel digital output after completion of the A/D conversion in one of the following data notations. Binary Offset binary 2's complement The user selects the data notation.
12–15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

I/O INTERFACE

The I/O interface signals use a 3M #3399-7026 connector and are defined in the following table.

ADV11-C Connector J1 Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	CH 0	2	CH 8 or RETURN 0
3	CH 1	4	CH 9 or RETURN 1
5	CH 2	6	CH 10 or RETURN 2
7	CH 3	8	CH 11 or RETURN 3
9	CH 4	10	CH 12 or RETURN 4
11	CH 5	12	CH 13 or RETURN 5
13	CH 6	14	CH 14 or RETURN 6
15	CH 7	16	CH 15 or RETURN 7
17	A GND	18	AMP L
19	EXT TRIG IN L	20	D GND
21	RTC IN L	22	D GND
23		24	A/D REF
25		26	A/D REF

AXV11-C ANALOG INPUT/OUTPUT

Power Requirements

+5 V (+5%) @ 2.0 A

Bus Loads

AC	DC
1.3	1

Standard Addresses

AXV11-C Standard Address Assignments

Description	Mnemonic	First Module Address	Second Module Address
Registers			
Control status	CSR	170400	170420
Data buffer	DBR	170402	170422
DAC A	DAA	170404	170424
DAC B	DAB	170406	170426
Interrupt Vectors			
A-D DONE		400	410
ERROR		404	414

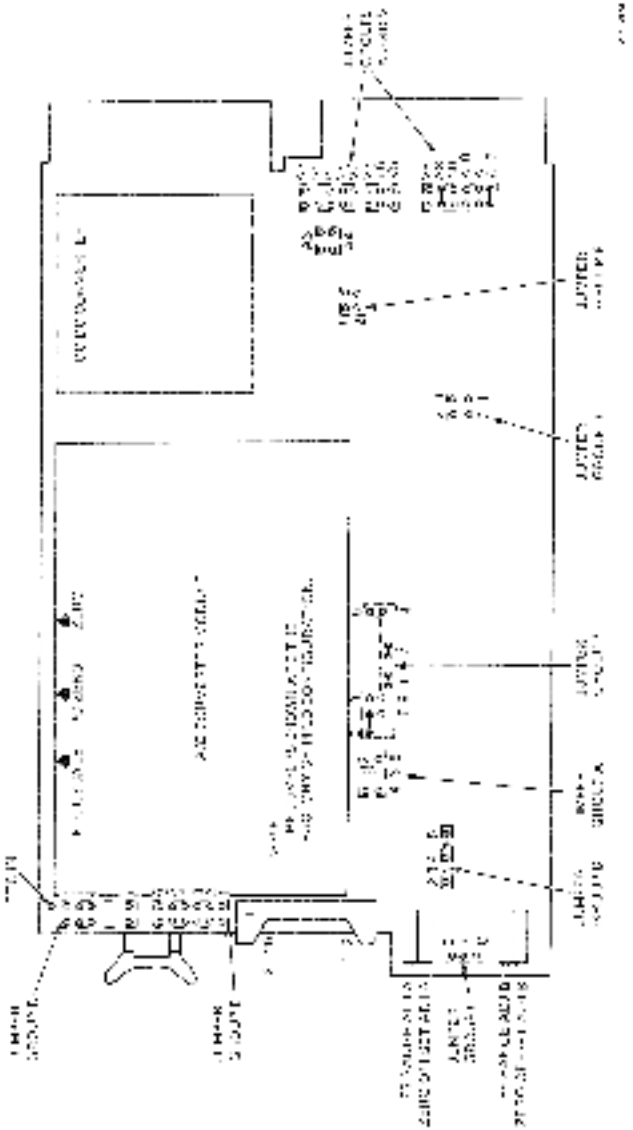
Diagnostic Programs

Refer to Appendix A

Related Documentation

LSI-11 Analog System Users Guide (EK-AXV11-UG)
Field Maintenance Print Set (MP01291)

AXV11-C/A0026



AXV11-C Module layout

CONFIGURATION

The AXV11-C has jumpers to set up the device address, the interrupt vector address, the analog configuration, and the DAC configuration. The user may select the A/D input range, polarity, and the output data notation. The user may select the D/A input data notation, output range, and polarity of each DAC.

Selecting AXV11-C Device Address

The AXV11-C device address is the I/O address assigned to the control status reg ster. The device address is selected by jumpers A3 through A12. The jumpers allow the user to set the device address within the range of 160000 to 177770. The device address is usual y set at 170400. A jumper installed decodes a 1 in the corresponding bit position; a jumper out decodes a 0.

Selecting AXV11-D Device Address

Selecting AXV11-C Interrupt Vector Address

The AXV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts, if enabled, occur when the A/D DONE bit or the ERROR bit is set in the CSR. The base interrupt vector address is assigned to A/D DONE. (The ERROR interrupt automatically is assigned the base interrupt vector address + 4.)

The base interrupt vector address can be set within the range of 0 to 770, in increments of 10. It is usually set to 400 by jumpers V3 through V8.

Selecting AXV11-C Interrupt Vector Address

Selecting AXV11-C Analog Input Range, Type, and Polarity

The AXV11-C allows software control over the full-scale range select or the effective ranges provided by the programmable gain are as follows:

Effective Input Range

Gain	Unipolar	Bipolar
1	0 V to +10 V	−10 V
2	0 V to +5 V	−5 V
4	0 V to +2.5 V	−2.5 V
8	0 V to +1.25 V	±1.25 V

The analog input type jumpers that must be installed are described in the following table. The board comes from the factory set for 16-channel, single-ended, bipolar inputs.

Selecting AXV11-C Analog Input Type

Input Type	Install Jumpers
Single-ended inputs*	P1 to P2; P8 to P9
Differential inputs	P2 to P3; P4 to P5

*Factory configuration

NOTE

Jumpers P6 and P7 are factory installed for the programmable gain feature and should be left in.

Selecting AXV11-C A/D Output Data Notation

The AXV11-C allows the user to select the data notation to be used for the A/D output, as either binary, offset binary, or 2's complement notation as described in the following table. Refer to jumper groups D and E near the handle of the board.

Selecting A/D Output Data Notation

A/D Output Data Notation	Jumpers 1D	4D	5D	6D	5E	6E	Input Voltage	Output Code (Octal)
Binary	IN	OUT	OUT	IN	OUT	IN	+ full scale 0 V	007777 000000
Offset binary*	OUT	IN	OUT	IN	OUT	IN	+ full scale 0 V full scale	007777 004000 000000
2's Complement	OUT	IN	IN	OUT	IN	OUT	+ full scale 0 V full scale	003777 000000 174000

*Factory configuration

Selecting Source of External Trigger

The A/D conversions within the AXV11-C can be started in one of the following three ways.

1. Under program control using the A/D START bit in the CSR.
2. By a real-time clock input at J1, pin 21 or at pin RTC IN.
3. By an external trigger, either at J1, pin 19, or at the BEVNT line on the LSI-11 bus.

The user can select the source of the external trigger using two jumpers on the board. (See Jumper group F.) The jumpers installed to select the source of the external trigger are described in the following table. (Jumper C1 to C2 should always be installed.)

Selecting AXV11-C External Trigger

External Trigger Source	Jumpers F1	F2
BEVNT line (LSI-11 bus)	IN	OUT
EXT TRIG IN (J1 pin 19)*	OUT	IN

*Factory configuration

Selecting AXV11-C D/A Configuration

The user can select the input data notation and the output voltage range for the two D/A converters on the AXV11-C. DAC A and DAC B can be configured for different polarities; however, the input data notation selected and the output polarity selected must be the same for each DAC. The DAC A and DAC B jumpers are described in the following tables.

Selecting DAC A Jumper Configuration

Range and Polarity	Binary	D/A Input Data Notation Offset Binary	2's Complement
± 10 V	N/A	5A to 5A* D1 to D3	5A to 5A D to D2
0 to +10 V	1A to 2A D1 to D3	N/A	N/A

*Factory configuration
N/A — not applicable

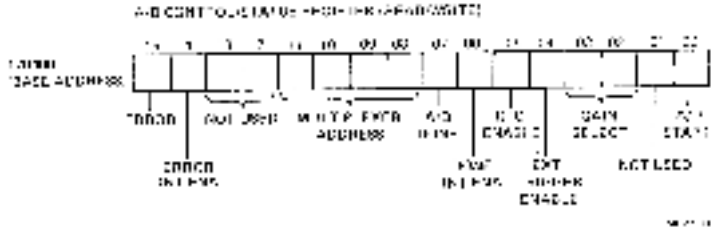
Selecting DAC B Jumper Configuration

Range and Polarity	Binary	D/A Input Data Notation Offset Binary	2's Complement
± 10 V	N/A	1B to 5B* D1 to D3	1B to 5B D to D2
0 to +10 V	2B to 3B D1 to D3	N/A	N/A

*Factory configuration
N/A — not applicable

CSR BITS

The control status register is a read/write register. A control instruction is written into the CSR; the A/D status is read from the CSR. The following information describes the CSR bits.



AXV11-C Control Status Register (Read/Write)

AXV11-C Control Status Register Bit Assignments

Bit	Name	Description
00	A/D START	Write only – When set, this bit starts an A/D conversion. This bit is cleared by internal logic after starting conversion. It always reads back 0.
01	Not Used	
02, 03	GAIN SELECT	Read/write – Set these bits to select the gain for the analog input as follows. Gain / GS1 (bit 03) / GS0 (bit 02) 1 / 0 / 0 2 / 0 / 1 4 / 1 / 0 8 / 1 / 1
04	EXT TRIG ENABLE	Read/write – When set, this bit allows an external trigger to start an A/D conversion.
05	RTC ENABLE	Read/write – When set, this bit allows a real-time clock input to start an A/D conversion.

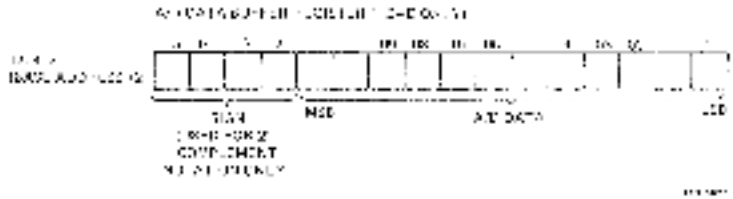
AXV11-C/A0026

AXV11-C Control Status Register Bit Assignments (Cont)

Bit	Name	Description
06	DONE INTERRUPT ENABLE	Read/write - When set, this bit enables an interrupt on A/D DONE (bit 07). Both bits are cleared by INIT.
07	A/D DONE	Read only - This bit is set at the end of an A/D conversion and is reset by reading the A/D data buffer register.
08-11	MULTIPLEXER ADDRESS	Read/write - These bits select 1 of 16 analog input channels.
12-13	Not used	
14	ERROR INTERRUPT ENABLE	Read/write - When set, this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT.
15	ERROR	Read/write - When set, this bit indicates that an error has occurred due to one of the following: 1. Trying an external start or clock start during multiplexer setting time. 2. Trying a start while an A/D conversion is in process. 3. Trying any start while the A/D DONE bit is set. This bit can be cleared by writing the CSR or by an INIT.

DATA BUFFER REGISTER

The data buffer register is a read only register that holds the digital data after the A/D conversion is complete. The DBR can be read after the A/D DONE bit is set in the CSR. The DBR is cleared after reading the register or upon initializing the LSI-11 bus. The following information describes the DBR bits.



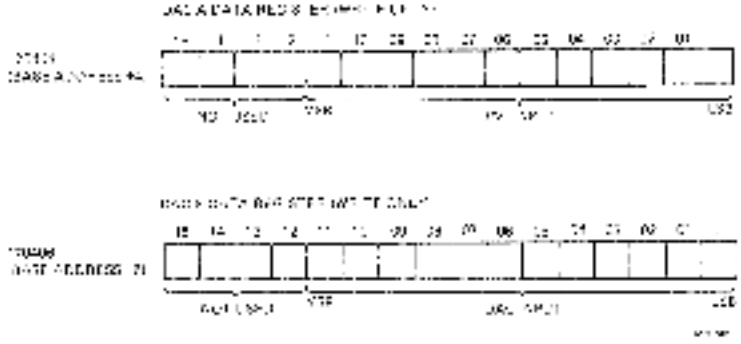
AXV11-C Data Buffer Register (Read Only)

AXV11-C Data Buffer Register Bit Assignments

Bit	Name	Description
00-11	A/D DATA	These bits hold the parallel digital outputs after completion of the A/D conversion in one of the following data notations. Binary Offset binary 2's complement The user selects the data notation.
12-15	SIGN	These bits are the sign for the bipolar inputs when using 2's complement notation. These bits are not used for binary or offset binary notation.

DAC A AND DAC B REGISTERS

DAC A register and DAC B register are 12 bit, write only registers. They are loaded from the LSI-11 bus with digital data and are changed to an analog voltage. The format for each register is shown in the following figure. Each DAC responds immediately to the data word stored in its register. Each register holds its last value until written again or until power is turned off.



AXV11-C DAC A and DAC B Registers

I/O INTERFACE

The I/O interface signals use a 3M #3399-7026 connector and are defined in the following table.

AXV11-C Connector J1 Pin Assignments

Pin	Signal Name	Pin	Signal Name
1	CH 0	2	CH 8 or RETURN 0
3	CH 1	4	CH 9 or RETURN 1
5	CH 2	6	CH 10 or RETURN 2
7	CH 3	8	CH 11 or RETURN 3
9	CH 4	10	CH 12 or RETURN 4
11	CH 5	12	CH 13 or RETURN 5
13	CH 6	14	CH 14 or RETURN 6
15	CH 7	16	CH 15 or RETURN 7
17	A GND	18	AMP L
19	EXT TRIG IN L	20	D GND
21	RTC IN L	22	D GND
23	DAC A RETURN	24	DAC A OUT
25	DAC B RETURN	26	DAC B OUT

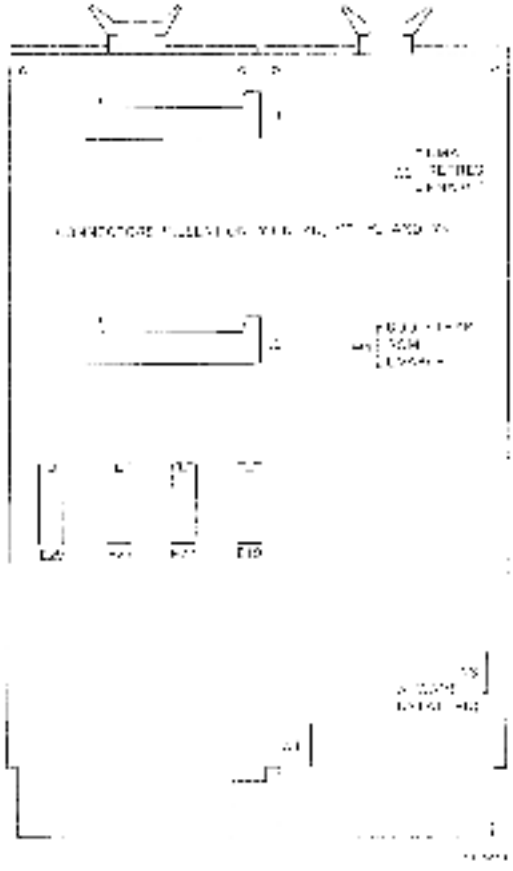
BCV1X BUS TERMINATOR, DIAGNOSTIC, AND BOOTSTRAP MODULES

M9400 (REV11 - REV11 and BCV1X) bus diagnostic, bootstrap, terminator, and DMA refresh option variations.

	Amps		Bus Loads		Cables
	+5	−12	AC	DC	
M9400-YA (REV11-A)	1.84 (2.24 max.)	0	2.21	1.0	
M9400-YB (REV11-B)	0.54 (0.70 max.)	0		1.0	
M9400-YC (REV11-C)	1.0 (1.80 max.)	0	2.21	1.0	
M9400-YD (BCV1A)	0	0	0	0	(2) BC05L
M9400-YE (BCV1B)	0.28	0	0	0	(2) BC05I
M9400-YF (REV11-F)					
M9400-YH (REV11-H)	1.84	0	2.21	1.0	
M9400-YJ (REV11-J)					(2) BC05I
M9400-YK (REV11-K)					
M9400-YL (REV11-L)					
M9400-YM (REV11-M)					
M9400-YN (REV11-N)	1.84	0	2.21	1.0	

Related Documentation

REV11-A, -C Field Maintenance Print Set (MP00070)
REV11-H Field Maintenance Print Set (MP00331)
REV11-F Field Maintenance Print Set (MP00074)
Microcomputer Interfaces Handbook (EB-20175-20)



M9400 Jumper Locations

W1: Installed to enable BDMG arbitration.
Installed on -YB, -YD, and -YE modules.
Not installed on -YA, -YC, -YF, -YH, -YK, and -YJ modules.

W2: Installed to enable DMA refresh.

W3: Always installed.

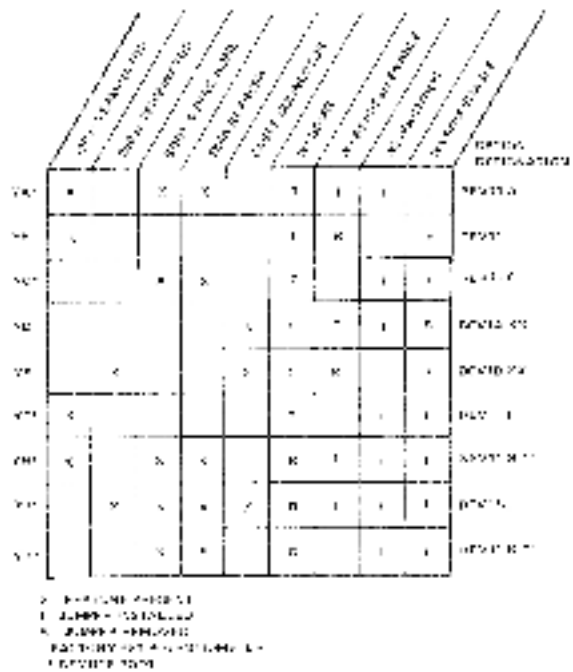
W4: Installed to enable bootstrap ROMs.

If REV11 refresh is enabled, the memory electrically farthest from the REV11 must reply to refresh. Also, processor refresh must be disabled.

NOTES

1. If no memory replies to REV11 refresh, the REV11 may hang the processor. The problem will appear to be a non-functioning CPU.

2. If the REV11 is not up to ECO no. 5 level or greater, the same symptoms may occur if a DRV11 is present that has an external capacitor to extend NEW DATA READY to greater than 1.8 µs.



M9400 Jumper Variations

The jumper states indicated in the preceding figure are as they are set from the factory.

BCV options also include M9401 banks and connectors and BC05L expansion cables. Certain rules for cable lengths and module locations must be observed. Refer to the "Systems Configurations" section for these configuration rules.

REV11 ROM Program Commands

Command	Function
OD	ODT (Rs I). This allows the operator to examine and/or alter memory and register locations via the console device. Control can be returned to the REV11 program by entering the ODT P (proceed) command if the PC has not been altered, and the console device will display the $ prompt character. If the PC has been altered, the operator can start program execution by entering the starting address 165006 and the G (go) commands as follows: @ 165006 $ The processor responds by displaying the $ prompt character on a new line and another REV11 command can be entered.
XM<CR>	Memory Diagnostic program. After successfully completing the diagnostic, the prompt character ($) is displayed on the console device. Errors are indicated by the following displays on the console device. 1. *177772* @ This is an address test error. The expected (normal) data is in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command. 2. *173756* @ This is a data test error. The expected (normal) data is stored in R3 and the invalid data is in the memory location pointed to by R2. If desired, continue diagnostic program execution by entering the ODT P command. 3. 000010 @ A timeout trap has occurred in testing memory locations outside of the first (lowest) 4K memory.

BEV11 ROM Program Commands (Cont)

Command	Function
	4 nnnnnn @ A timeout trap has occurred in testing memory locations within the first 4K memory. The nnnnnn displayed is an indeterminate number. The actual memory test consists of an address test and a data test. The address test first writes all memory locations with addresses, i. then reads and verifies the addresses. The data test consists of two parts. An "all 1s" word is first walked through all memory locations, which are initially 0. The second part consists of walking an all 0s word through all memory locations which are all 1s.
XC<CR>	Processor Diagnostic program. This is a memory modifying instruction test. Successful execution of the diagnostic program results in the prompt character (@) being displayed on the console device. Errors are indicated by the following. 1. The program halts when an instruction sequence is not correctly executed. 2. The program halts in the trap vector area for various traps.

NOTE

When a halt occurs, the console ODT M command can be used to determine how the halt mode was invoked. When the system fails to successfully execute the above diagnostics, maintenance diagnostic programs should be used to thoroughly test processor (and memory) functions.

DX<CR> or DXn<CR>	RXV11 floppy disk system bootstrap. Entering the DX<CR> command starts the memory-resident CPU instruction test and memory test execution (see the XC and XM commands). Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number (n) as 0 (drive 0) or 1 (drive 1).

REV11 ROM Program Commands (Cont)

Command	Function
	Floppy disk bootstrap errors are:
	1. The program halts and the console device displays the following: *165016* @ This indicates that the device done flag in the REV11 interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be restarted by entering the P command; the @ is then displayed on the console device and the bootstrap command can be entered.
	2. The program halts and the console displays the following: *165614* @ This indicates that a bootstrap error occurred. The REV11 *error/req* error contents are stored in R2. By examining the contents of R2 and using the information contained in the *REV11 User's Manual*, the exact nature of the error can be determined. Examine the contents of R2 (octal) as follows: @ R2/*xxxxxx*<CR> @ P *$*
	After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.
	3. The program halts in the trap vector for traps; a timeout trap returns the program to the @ prompt character. If a timeout trap occurs, first check for proper system cable connections and device interface module installation. Then, attempt to bootstrap the system by again entering the desired bootstrap command.

BEV11 ROM Program Commands (Cont)

Command	Function
DK<CR> or DKn<CR>	Disk Drive System Bootstrap. Entering the DK command starts the memory modifying CPU instruction test and memory test execution (see the XC and XA commands). Successful test execution results in execution of the bootstrap program for disk drive 0, the system disk. Otherwise, specify the drive number n as 0 (drive 0), 1 (drive 1), or 2 (drive 2). Disk bootstrap errors are: 1. The program halts and the console device displays the following: *165724* *@* This indicates that the device done flag in the RKV11-D interface was not set within the required time (approximately 1.3 seconds). The bootstrap can be started by entering the P command. The 5 is then displayed on the terminal and the bootstrap command can be entered. 2. The program halts and the console then displays the following: *165644* *@* This indicates that a bootstrap error occurred. The RKV11-D error register contents are stored in R2. By examining the contents of R2 and using the information contained in the *RKV11-D User's Guide*, EK-(RKV11-OP-UG), the nature of the error can be determined. Examine the contents of R2 (nnnnnn) as follows: *@R2/nnnnnn<CR>* *@* *$* After examining R2, the bootstrap can be restarted by the P command; enter the desired bootstrap command immediately after the $ prompt character.

REV11 ROM Program Commands (Cont)

Command	Function
	4. The program halts in the trap vector for trap 4 (timeout trap) returns the program to the $ prompt character. If a timeout trap occurs, first check for proper system cable connections and device interface module installation. Then, attempt to bootstrap the system by again entering the desired bootstrap command.
AL<CR>	Absolute Loader program, normal (absolute address) loading operation. Entering AL <CR> specifies that a paper tape is to be loaded via the console device (CSR address = 177560). However, another device can be specified by entering the appropriate CSR address. For example, to load paper tapes in absolute loader format via a device whose CSR address is 177550, enter the following command. $ AL 177550<CR> The program responds by first executing the memory modifying CPU instruction test and memory test (refer to the XC and XM commands). Successful test execution results in execution of the Absolute Loader program. A successful program load is indicated when the console device displays the following. *165625* @ The loaded program automatically starts execution. or Absolute Loader errors are. 1. Checksum error, with the program halting and producing the following display *166634* @ 2. Program halts in the trap vector area for traps other than a timeout trap. 3. Timeout trap occurs, causing the display of $ on a new line on the console device.

REV11 ROM Program Commands (Cont)

Command	Function
AP<CR>	Absolute Loader program relocated loading operation. When this command is entered, the memory-modifying CPU instruction test and memory test are automatically first executed (refer to the XC and XM commands), followed by the Absolute Loader program. Successful execution of the tests results in the program halting with the following console display: *165412* *@* The operator must then enter the appropriate "software switch register" contents in R4. To select relocated loading, which uses an address (bias) contained in the software switch register, enter the following commands: *@* R4/ *xxxxxx* nnnnnn<CR> *@* P The value nnnnnn is a relocation value selected by the operator as directed in the *RSX-11 Paper Tape Software Handbook*, DEC-XP11A-BD. Observe that the least significant "n" value entered must be an odd number; this sets the software switch register (R4) bit 0 to a logical "1", selecting the relocated loading mode. Note that the program being loaded must be in Position Independent Code (PIC) format for relocated loading. When large programs are contained on more than one tape, the program halts at the end of the first tape. Install the second tape in the reader and enter a "1" in R4 using the /01 command shown below; resume loading by entering the P command. *@* R4/*xxxxxx* 1<CR> *@* P The six octal digits (xxxxxx) are the present contents of R4. Entering a value of 1 selects relocated loading for the next program tape, starting at the address following the end of the previous program operation. The P command allows the Absolute Loader program execution to continue the loading process once the software switch register value has been entered.

REV11 ROM Program Commands (Cont)

Command	Function
	A successful program load is indicated when the loaded program automatically starts execution, or the console device displays.
	165626 @
	Absolute Loader errors are as described for the AL command.

BDV11 BUS TERMINATOR, BOOTSTRAP, AND DIAGNOSTIC ROM

Amps		Bus Loads		Cables
5	−12	AC	DC	
1.6	.07	2	1	None

Standard Addresses

ROM Window	173000–173776
Page Control Reg	177520
Scratch Pad Reg	177522
Option Select Reg	177524 (read only)
Display Reg	177524 (write only)
Line Clock CSR	177546

Standard Vectors

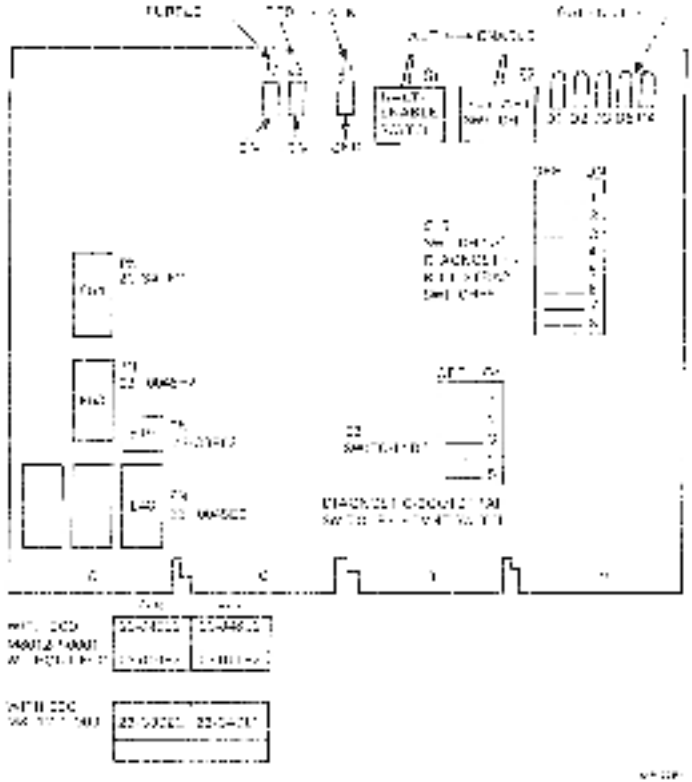
Line Clock	100

Diagnostic Programs

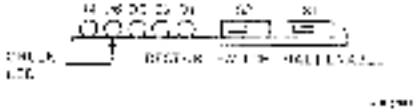
Refer to Appendix A

Related Documentation

BDV11 Bus Terminator, Bootstrap, Diagnostic ROM Technical Manual (EK-BDV11-TM)
Field Maintenance Print Set (MP00436)
Microcomputer Interfaces Handbook (EB-20175-20)

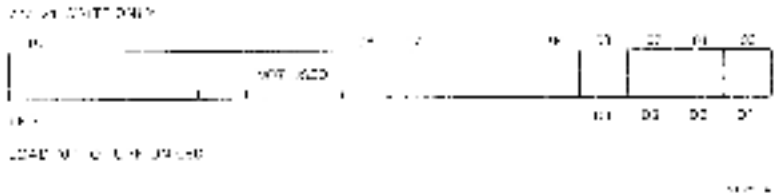


BDV11 A Switches and Indicators

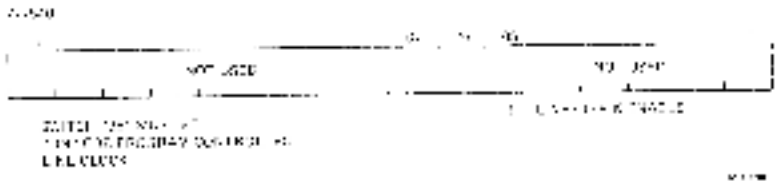


Diagnostic Light Display

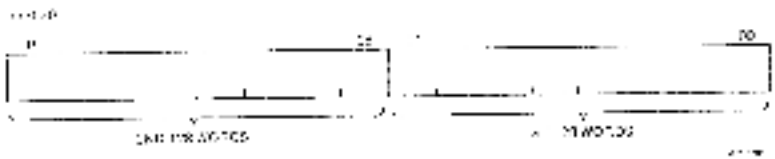
Switch Register



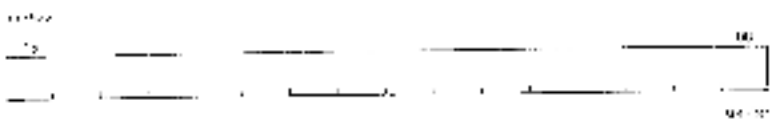
Display Register



Line Clock CSR



Page Control Register



Read/Write Register

BDV11 Hardware Registers

Register	Function	Bus Address
Page Control Register (PCR)	Controls mapping of ROM pages into physical ROM addresses. Cleared when power is turned on or when RESTART switch is activated. Seven bits	177520. Word or byte byte addressable; can be read or written
Read/Write Register	Maintenance register used for diagnostics. Cleared when power is turned on or when RESTART switch is activated. Sixteen bits.	177522. Word or byte byte addressable, can be read or written.
Switch Register	Used for maintenance and system configuration (selects diagnostic and/or bootstrap programs for execution). Bits 0 [illegible] in the register (corresponding to E18-1 through E18-8 and E21-1 through E21-4, respectively) are associated with ROM [illegible] respectively. When an individual switch of the register is closed (on), the corresponding BDAL signal is low (1). Twelve bits	177524. Read-only register.
Display Register	Controls the diagnostic light display. Bits 0-3 of the register control LEDs D1-D4, respectively. When a bit is set, the corresponding LED is off; cleared (all lights on) when power is turned on or when RESTART switch is activated. Four bits.	177524. Word or byte addressable; write only register.

BDV11 Hardware Registers (Cont)

Register	Function	Bus Address
Line Clock CSR	When cleared, this register clamps the BEVNT signal low (if BEVNT switch is closed). This action permits program control of the KW11-L line time clock (LTC) function. Register cleared when power is turned on or when RESTART switch is activated. One bit.	777546. Word or byte addressable; write-only register.

(See ECO M8012-I-001.)

BDV11 (For ROMs 23-045E2 and 23-046E2 only)

Switch Settings and Mnemonics
For the discussion that follows, the M8012 switch S1b will be called "A" and S1a will be "B."

Switches A1 through A8 are defined as follows:

A1 ON Execute CPU tests on power-up or restart
A2 ON Execute memory test on power up or restart
A3 ON DECNET BOOT – A4, A5, A6, A7 are used as arguments

Device	A4	A5	A6	A7
DLV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

DLV11-E RCSR = 176610, DLV11-F RCSR = 176500

A4 ON Console test and stop (A5 OFF).
A4 OFF Turnkey BOOT dispatched by switch setting (A5 OFF).
Switches A5, A6, A7, A8, B1 are used as arguments.

Device	A5	A6	A7	A8	B1
Loop on Error	OFF	OFF	OFF	OFF	ON
RK05	OFF	OFF	OFF	ON	OFF
RL01	OFF	OFF	ON	OFF	OFF
RX01	OFF	ON	OFF	OFF	OFF
RX02	OFF	ON	ON	OFF	OFF
BDV11 ROM	ON	OFF	OFF	OFF	OFF

The BDV11 ROM BOOT uses the following switches as arguments (X = don't care):

ROM	B2	B3	B4
Extended DIAG	ON	X	X
2708s	OFF	ON	X
Program RUM	OFF	OFF	ON

All unused patterns or mnemonics will default to ROM BOOT if switch B2, B3, or B4 is ON.

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, the presence of additional ROM is checked (by checking B2, 3, 4) and if present, the ROM BOOT is invoked.

If an unrecognized switch setting is encountered, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch checking routine will halt or the mnemonic routine will reprompt.

If the console test is selected, the console test prompts with:

ZZK Where ZZ is the decimal multiple of 1024.
START? Words of RAM found in the system.

Allowed responses are a two character mnemonic with a one-to-six digit octal unit number or one of two special, single-character mnemonics. The response must be followed by a return. The special single-character mnemonics are:

Y Use switch settings to determine boot device; or,
N HALT. Enter microcode ODT.

The two-character mnemonics are as follows. "N" is a digit from 0 to 7 indicating the unit number of the device.

DKN	RK05 bootstrap
DLN	RL01 bootstrap
DXN	RX01 bootstrap
DYN	RX02 bootstrap

BDV11 HALT/ENABLE, RESTART, AND BEVNT SWITCHES

HALT/ENABLE Switch

When this switch is in the ENABLE position, the LSI-11 CPU can operate under program control. If the switch is placed in the HALT position, the CPU enters the halt mode and responds to console ODT commands. While in the halt mode, the CPU can execute single instructions, facilitating maintenance of the system. Program control is re-established by returning the switch to the ENABLE position and entering a "P" command at the console terminal (provided the contents of register R7 were not changed). Refer to chapter 2 of the *Microcomputer Handbook* (1977–1978) for a description of console ODT command usage.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, the system can be rebooted at any time for maintenance purposes.

BEVNT L Switch

Connector 6 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open) the LSI-11 bus BEVNT L signal can be controlled by the power-supply-generated LTC signal. When the switch is on (closed), the LTC function is program controlled; i.e., a single-bit write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.) The KW11-L line clock option also uses bit 6 as the enable bit.

POWER OK LED and Tip Jacks

This green LED is lighted when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560 Ω resistor in series to prevent damage from a short circuit. Use at least a 20 000 Ω V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	−12 Vdc

Secondarily, the LED indicates the initial point for the diagnostic light display.

The BDV11 (M8012) is the new bootstrap module for the PDP-11/03. It is a quad module and it has 2K words of diagnostics in ROM installed on the board. The failures of these diagnostics are indicated by the HALT address in the RDV and by the state of the error lights on the board.

The "Diagnostic LED Error Display" table provides a cross-reference between the failed part of the error lights and the failing system function. The "BDV11 Diagnostic Error Addresses" table provides a cross reference between the HALT PC and the failing system function. (The HALT PC will be displayed on the console terminal.)

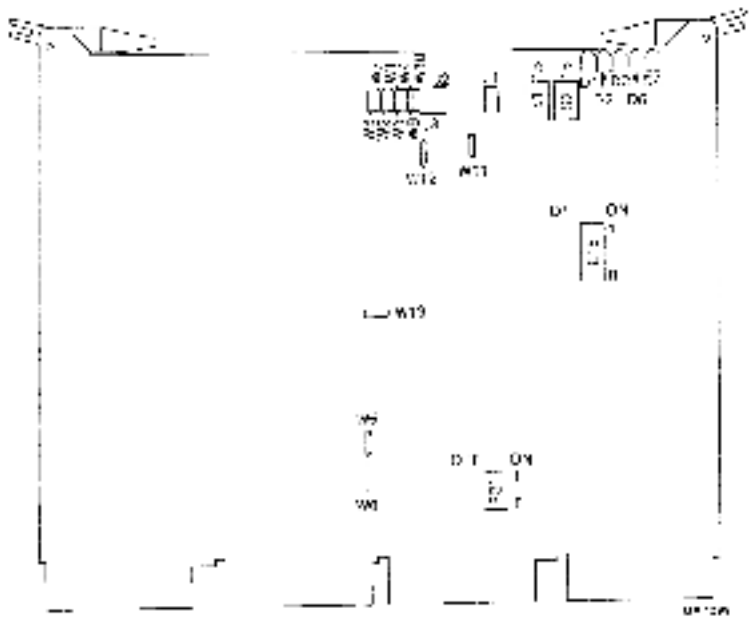
Diagnostic LED Error Display

D4 Red	D6 Green DC OK	D3 Red	D2 Red	D1 Red	Comments
X	OFF	X	X	X	−12 Vdc or +5 Vdc is bad.
OFF	ON	OFF	OFF	ON	CPU test error or fault or configuration error.
OFF	ON	OFF	ON	OFF	Memory test error; register R1 points to bad location
OFF	ON	OFF	ON	ON	Console serial line unit does not transmit
OFF	ON	ON	OFF	OFF	Console terminal test waiting for response from operator on keyboard.
OFF	ON	ON	OFF	ON	Load device status error.
OFF	ON	ON	ON	OFF	Secondary bootstrap code incorrect. NOP instruction is not in location 000000; the medium is probably bad.
OFF	ON	ON	ON	ON	DECNET waiting for response from host computer
ON	ON	OFF	OFF	OFF	DECNET received CONF FLAG set
ON	ON	OFF	OFF	ON	DI-CNF-I message received.
ON	ON	OFF	ON	OFF	ROM BOOTSTRAP error.
ON	ON	ON	ON	ON	HALT switch is ON; unable to run (check computer and BDV11 HALT switch); or power up mode is wrong, or system is hung.

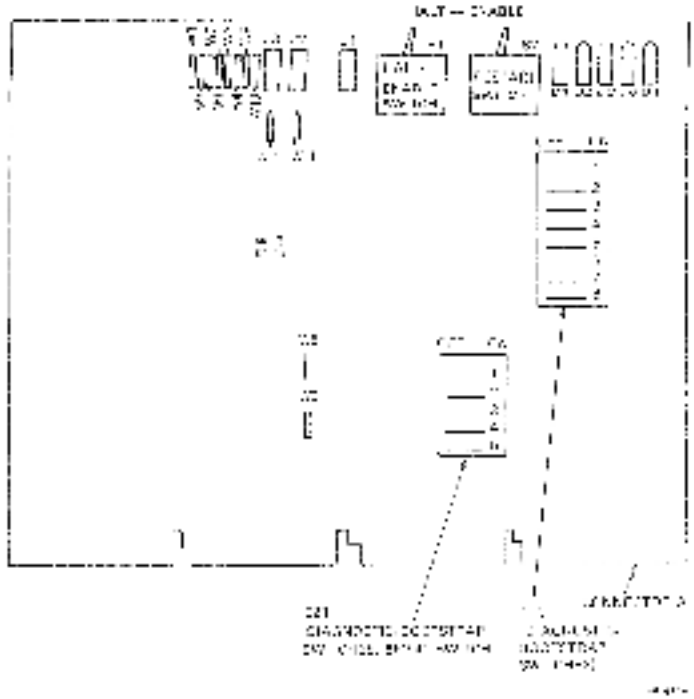
Diagnostic LED Error Display

BDV11 Diagnostic Error Addresses

Error Address	Cause of Error
173029	Memory error 1. Write address test itself.
173040	Serial line unit switch select or incorrect error in switches.
173046	Serial line unit error. CSR address for selected device in error. Check CSR for selected device in floating CSR address area.
173050	CPU error 1. Register R0 contains address of error.
173052	Memory error 2. Data test failed.
173100	Memory error 3. Write and read bytes failed.
173202	ROM loader error. Checksum on data block.
173240	CPU error 4. R0 contains address of error.
173366	ROM loader error. Checksum on address block.
173402	ROM loader error. Jump address is odd.
173530	RL device error.
173604	CPU error 5. R0 points to cause of error.
173612	A 'NO' typed in console terminal test.
173656	Switch mode HALT. A switch was not made with switches.
173656	RK device error.
173670	Console terminal test. No DONE flag.
173706	CPU error 6. R0 points to cause of error.
173712	RX device error.



BDV11 Switch and Jumper Locations



BDV11 Switches and Indicators

Socket Selection Logic

The socket selection logic determines which pair of sockets responds to the ROM address signals. (Although the ROMs in the sockets actually respond, it is said, for ease of explanation, that the sockets respond).

Jumpers are inserted selectively in positions W1-W4 and W9-W12. These jumpers cause the PCR page numbers and the select-on signals (and, therefore, the sockets) to be related in definite ways. Group A in the "BDV11 Selection Signals/Sockets" table indicates that PCR pages are assigned to specific ROM sockets. This is true within the confines of the BDV11 module shipped by DIGITAL. On such a module, jumpers W1-W4 and W9-W12 are arranged as indicated under Group A in the table. Thus, the PCR pages 0-17, for example, cause selection signal SEL L to be asserted, and SEL L causes sockets XE50 and XE48 to respond to address signals A<0:10> H. Other combinations of jumpers are possible, as indicated by Groups B through G in the table. Note that each selection signal always selects the same pair of sockets; however, the relation of PCR pages to selected sockets varies with jumper configuration.

BDV11 Selection Signals/Sockets

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<15:14>=0)	Sockets Selected
A	R	I		H		R	R	I	0-17	BR1 L	0K-2K	XC53/XC45
									20-37	BR2 L	2K-4K	XC56/XC44
									40-57	SE1 L	4K-6K	XC57/XC43
									60-77	SC4 L	6K-8K	XC52/XC36
									300-317	BT1 L	30K-32K	XC58/XC50
									320-337	BT2 L	32K-34K	XC42/XC46
									340-357	BT3 L	34K-36K	XC47/XC49
									360-377	BT4 L	36K-38K	XC41/XC48
									200-217	BT5 L	20K-22K	XC55/XC37
									220-237	BT6 L	22K-24K	XC38/XC51
									240-257	BT7 L	24K-26K	XC39/XC54
									260-277	BT8 L	26K-28K	XC40/XC49
B	I	I	I	I	I	R	I	R	40-57	BD1 L	4K-6K	XC53/XE45
									60-77	BD2 L	6K-8K	XC55/XE41
									0-7	BC1 L	0K-1K	XC57/XE40
									10-17	BE2 L	1K-2K	XC52/XE56
C	I	I	I	I	R	I	R	I	200-217	BB1 L	16K-18K	Unused
									220-237	BB2 L	18K-20K	
									240-247	BB3 L	20K-21K	
									250-257	BB4 L	21K-22K	
D	I	I	I	I	R	I	I	R	340-357	BD1 L	20K-22K	Used
									360-377	BD2 L	22K-24K	
									200-207	BE1 L	16K-17K	
									210-217	BE2 L	17K-18K	

BDV11 Selection Signals/Sockets (Cont)

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<13:0>14,15=H)	Sockets Selected
F	I	R	I	R	*	*	*	*	270-277	SP1 L	32K-24K	XE52/XE50
									260-267	SP2 L	24K-22K	XE15/XE46
									230-237	SP3 L	19K-20K	XE47/XE12
									210-217	SP4 L	17K-18K	XE51/XE48
									250-257	SP5 L	22K-23K	XE55/XE37
									240-247	SP6 L	20K-21K	XE53/XE41
									220-227	SP7 L	18K-19K	XE56/XE42
									200-207	SP8 L	16K-17K	XE54/XE44
E	R	I	R		*	*	*	*	160-167	SP1 L	14K-16K	Ibid.
									110-157	SP2 L	12K-14K	
									120-127	SP3 L	10K-12K	
									100-107	SP4 L	8K-10K	
									50-57	SP5 L	6K-8K	
									40-47	SP6 L	4K-6K	
									30-37	SP7 L	2K-4K	
									0-7	SP8 L	0K-2K	
G	I	R	R	I	*	*	*	*	70-77	SP1 L	7K-8K	Ibid.
									50-57	SP2 L	5K-6K	
									30-37	SP3 L	3K-4K	
									10-17	SP4 L	1K-2K	
									60-67	SP5 L	5K-7K	
									40-47	SP6 L	4K-5K	
									20-27	SP7 L	2K-3K	
									0-7	SP8 L	0K-1K	

I = Inserted; R = removed

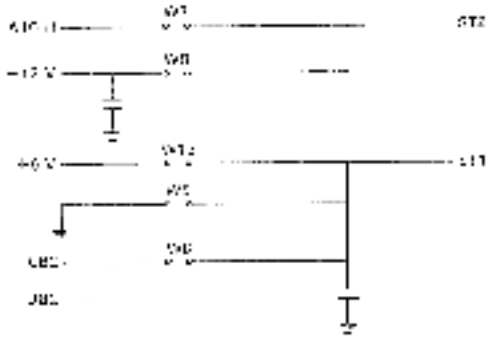
ROM Sockets Logic

The following figure represents the ROM sockets and shows the address signals and enabling signals for each functional group of sockets. The diagnostic/bootstrap ROM sockets (which are selected by signals SB1 L and SB2 L) are supplied with 11 address bits, since these sockets are reserved for 2K-word ROMs. The EPROM sockets (selected by signals SE1 L and SE2 L) are reserved for 1K ROMs; therefore, these sockets are supplied with 10 address bits. The system ROM sockets can be populated by either 2K ROMs or 1K ROMs; five jumpers on the BDV11 module permit ROMs of either size to be used.

The following figure shows how these five jumpers control the selection signals for the system ROM sockets, and relates the jumpers to the types of ROM that can be used in the BDV11. (If ROMs other than 8316E, 2716, and 2708 are used, do not alter configuration. See Caution.)

CAUTION

Improper configuration of these jumpers may cause ROM damage. Be sure of ROM type.



ROM TYPE	JUMPERS ASSERTED				
	W5	W9	W7	W8	W13
2708	B	1	B	1	B
2716	B	B	1	B	1
2732	1	B	1	B	B
2732A	B	B	1	B	1

1. [illegible]
2. [illegible]
3. [illegible]

W1	W2	W3
LOW	LOW	LOW

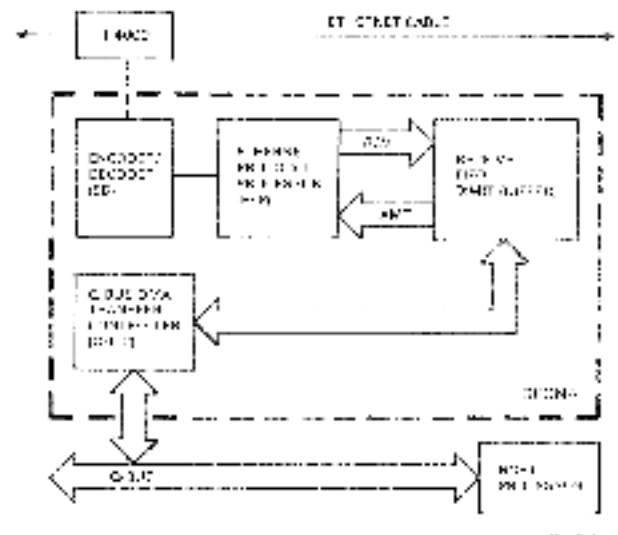
7. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS

W1	W2	W3
[illegible]	[illegible]	[illegible]

DEQNA INTERFACE (ETHERNET)

GENERAL

The DEQNA Q-Bus (LSI-11 bus) data communications controller interfaces the DIGITAL LSI-11 processor family to the Ethernet local area network. It works with both 18- and 22-bit address numbers. The DEQNA conforms to the Ethernet specification, Version 2.0, which performs the data link layer functions and is part of the physical layer functions.



DEQNA Major Functional Areas

Voltage	Bus Loads	
	AC	DC
+5 Vdc @ 2.5 A (3.0 A max)	2.3	0.5
+12 Vdc @ 0.5 A		

DEQNA/M7504

Standard Addresses

16-bit Addressing	174440	174460
18-bit Addressing	1774440	1774460
22-bit Addressing	17774440	17774460

Vectors

Assigned floating vectors with a 47 priority rank

Diagnostic Programs

ZQNA?? Q18-Q22-bit systems

Related Documentation

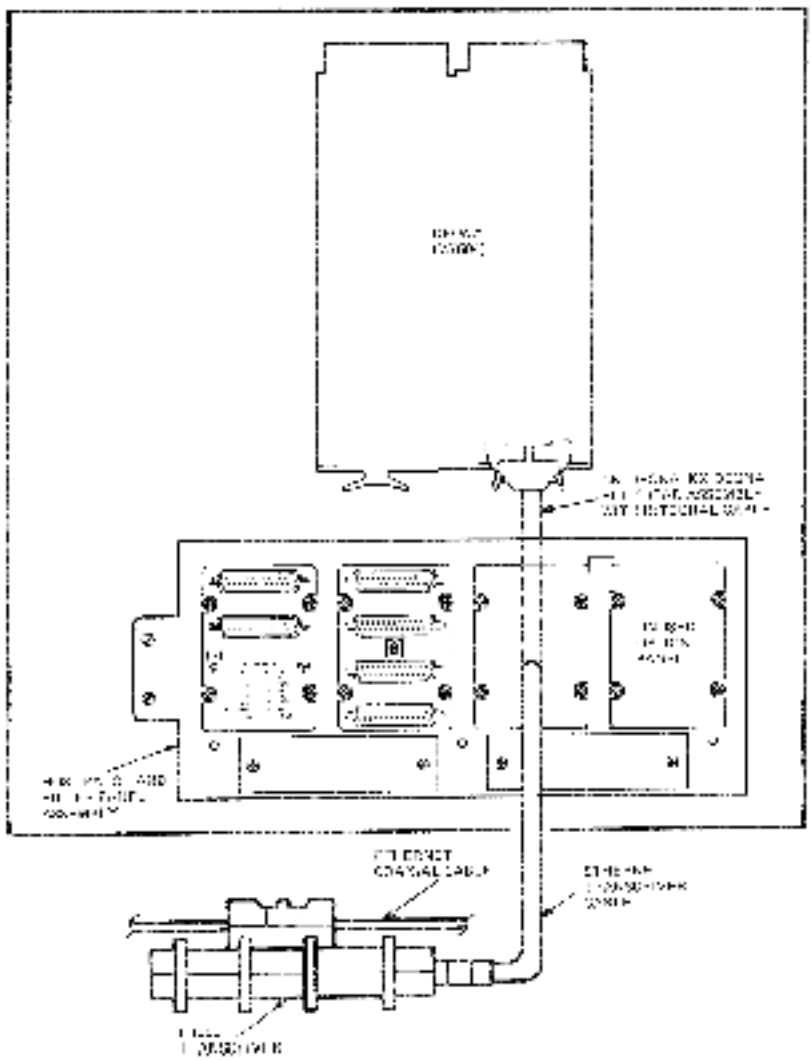
H4000 Ethernet Transceiver Field Maintenance Print Set (MP-01301)
H4000 Ethernet Transceiver Technical Manual (EK-01240-TM)
Ethernet, A Local Area Network Data Link Layer and Physical Layer Specification (AA-K759A-TK)
DECNA User's Guide (EK-DEQNA-UG)
Introduction To Local Networks (EE-22714-18)

Features

The DEQNA has the following features:

- Transmits and receives data at a rate of 10 Mbits per second
- Recognizes heartbeat and collision detection
- Performs packet serialization, formatting, Manchester encoding, and multiple retransmission
- Generates and checks 32-bit CRC
- Interfaces with the H4000 Ethernet transceiver
- Performs direct memory access (DMA) transfers to and from CPU memory
- Contains quick verify diagnostics for power-up and boot
- Performs internal and external loopback, and can assist on loopback of data from other stations
- Supports host system interrupt response
- Supports host down-line load and remote boot by other nodes on the network

The DEQNA comprises one dual (SI) module. It plugs into the Q-Bus backplane and resides in the same enclosure. The DEQNA is physically and electrically connected to the H4000 transceiver.



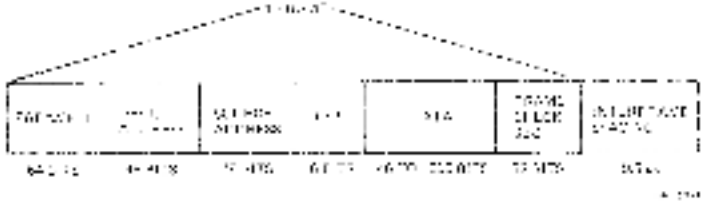
DEQNA to Ethernet Connection

DEQNA System Operation

The DEQNA and host communicate via two levels of data structures in host memory. First level communication is via eight I/O page addresses in host memory space which correspond to 16 port registers in the DEQNA. This level passes control and status, such as DEQNA error information (as opposed to packet error status), interrupt enable, and DEQNA initialization. Second level communication via the host resident memory area, primarily comprises DMA transfers of transmit and receive data.

Ethernet Overview

The Ethernet is a network that supports high-speed data exchange among computers and other digital devices, within a limited geographic area. The branching bus topology of the Ethernet provides a 10 Mbits per second data rate over a coaxial cable at a distance of 2.5 km (1.74 mi) or less. The Ethernet is a data communications network, with a higher data rate than low-speed networks, which carry data hundreds or thousands of kilometers, and a greater distance than very high-speed interconnects, which are usually limited to tens of meters.



Ethernet Packet Format (Frame)

The primary applications for the Ethernet are office automation, distributed data processing, terminal access, and other applications which require an economical local medium for exchanging data at high peak data rates.

PREINSTALLATION VERIFICATION

To verify that the DEQNA can be correctly installed in the host system, the following requirements and constraints must be met.

Host Boot/Diagnostic ROMs

This is to verify that the correct boot/diagnostic ROMs are installed in the host CPU. That is, the host CPU must be capable of loading the extended bootstrap code from the DEQNA ROM.

Backplane Requirements

The DEQNA requires one dual LSI-11 module slot configured for G22 ans (that is, an extended LSI-11 bus operation for highest performance.

Bus Latency Constraints

To get the best performance and avoid losing packets, the DEQNA should be the highest priority device on the G-Bus; that is, the DMA device nearest to the CPU.

When two DEQNAs are installed, a clock-mode memory is required. If high Ethernet traffic rates are to be handled. The following is a recommended module installation:

Processor	Slot 1
Memory	Slot 2
DEQNA 1	Slot 3
DEQNA 2 / Other	Slot 4
Others	Slots 5–8

Loading Requirements

Check that system loading capacity is not exceeded by installing the DEQNA. The table below shows the DEQNA Q-bus loading and the next table shows the DEQNA and transceiver power requirements.

POWER CHECKS

Power supply voltages should be checked before and after installation to verify the absence of overloading and overvoltage conditions.

Specifications

Specification	Description
Operating mode	Half-duplex (non-loopback)
Data format	Manchester encoding, serial
Ethernet data rate	10 megabits per second
Q-Bus electrical loading	0.5 dc load 2.2 ac loads
DC power requirements (typical)	
DEQNA	+5 V, 3.5 A
H4000 transceiver	+12 V, 0.2 A
Operating environment	
Temperature	5 to 50° C (41° to 122° F)
Relative humidity	10% to 90%
Wet Bulb temperature (max.)	32° C (89° F)
Dewpoint (min.)	2° C (36° F)
Altitude	Same as for system
Shipping environment	
Temperature	Same as for system
Relative humidity	Same as for system
Altitude	Same as for system

DEQNA Power Requirements

Module	Voltage Rating (Typical Values)	Typical Current	Maximum Current	Backplane Pins
M7504	+5 ± 0.25 V @ 3.5 A	3.5 A	5.0 A	AA1, BA1, BV1
	+12 + 0.60 V @ 0.5 A (for transceiver)	0.5 A	*	BL2
	Logic reference			AJ1, AK1, AT1, AC2, DJ1, BV1, BC2
	Transceiver return			ST1

* At power-up or powered up connect, transceiver surge current at the power connection is high enough to current-limit and power fail some power supplies. The DEQNA does not contain power supply surge protection; it must be provided elsewhere if required by the system configuration.

M7504 MODULE

The DEQNA module M7504 is configured with three jumpers, W1 through W3, which are installed during manufacture. The disposition of these jumpers is described in the following paragraphs.

Device Address Assignment (W1)

The DEQNA I/O page addresses are 17774440 (first DEQNA) and 17774450 (second DEQNA). If two DEQNAs are being installed, move jumper W1 onto the second DEQNA position, to set its I/O page address to 17774460.

Bus Request Holdoff Timer (W2)

Jumper W2 provides "fair" access to all DMA devices using the Q Bus and should not be removed, except for unusual requirements (not supplied).

Sanity Timer (W3)

If installed, this jumper disables the sanity timer at initialization. If removed, jumper W3 enables the sanity timer at initialization.

DEQNA Jumper Functions

Jumper	Function	In	Out/ 2nd Position
W1	I/O page address	17774410	17774430
W2	BDMR holdoff timer	No Delay	5 μs Delay
W3	Sanity timer at initialization	Disabled	Enabled

Jumper Configurations (3 jumpers)

Device address W1 I/O page address 17774440 on first DEQNA when only one DEQNA is present.

W2 in – Bus Request Holdoff Timer - fair access to DMA devices enabled, normally installed

W2 out – only for unusual requirements

W3 in – Sanity Timer – disables sanity timer at initialization

W3 out – enables sanity timer at initialization

	In	Out
W1	17774440	17774480
W2	No delay	800 delay
W3	disabled	enabled

Temporary vector address 774 when system is bootstrapped through the DEQNA and is running DEQNA self test code.

Recommended M7504 Installation

Slot 1 CPU processor
Slot 2 memory
Slot 3 DEQNA-1
Slot 4 DEQNA-2
Slot 5-8 others

The transceiver cable bulkhead assembly will be installed in an unused option panel location on the system I/O panel as shown on the next page. Remove the option panel by removing the four screws. Save the screws.

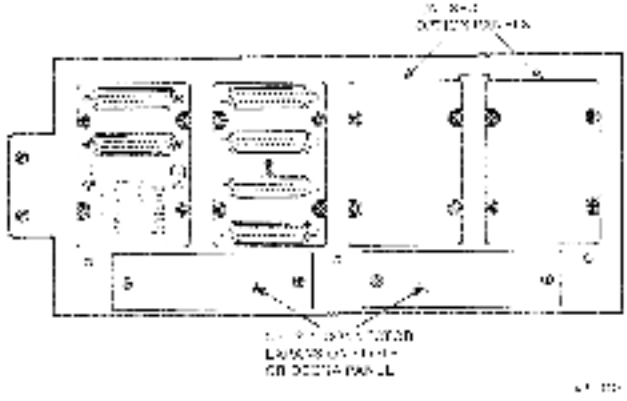
Install and cable the DEQNA and the bulkhead assembly as follows:

1. Slide the M7504 module in to the card guides with the component side next to the processor module. Do not insert the module all the way into the slot at this time.

3. Insert the transceiver cable assembly into the system I/O panel with the tool supplied when the blank panel was removed.

3. Connect the keyed panel of the quick-lock assembly to the module.

4. Slide the M7504 in the way into the card slot.



Panel and Filler Panel Assembly

DEQNA Cables

CK-DEQNA-KA – 53 cm (21 in) shielded cable kit for PDP-11/23

CK DEQNA KB – 38 cm (15 in) shielded cable kit for MICRO 11

CK-DEQNA KC – 76 cm (30 in) shielded cable kit for PDP-11/23 PLUS

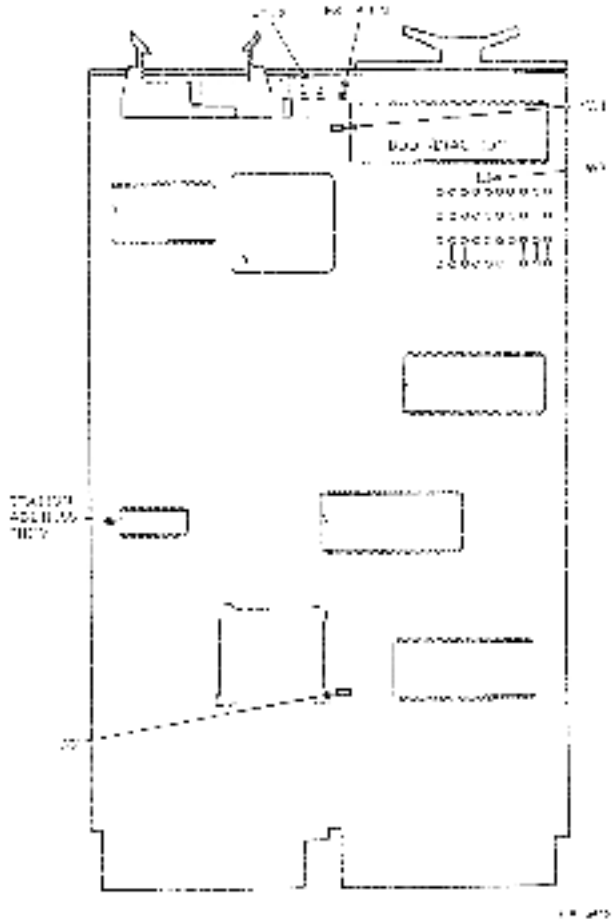
CK-DEQNA-KD – 4 meters (13 ft) shielded cable kit for general use

Light Emitting Diode (LED) Checks
The M7504 module includes three LEDs which indicate the operational status of the DEQNA, shown on the next page. This figure also defines the LED indicators.

Connect either an Ethernet transceiver with cable or a loopback connector to the transceiver cable connector on the panel and filler panel assembly.

2. Turn system power ON; all three LEDs on the M7504 module should be on.

3. Boot the system from the DEQNA. Note that new CPU PROM's (with code for booting from the DEQNA) must have been installed. The LEDs should be turned off, one at a time, until no LEDs are on.



DEQNA Jumpers and LED Indicators

DEQNA BOOT SEQUENCE

1. Load the first 512 bytes of BD ROM. This is the EP2 code.
2. Verify descriptor status and the CRC.
3. In the host, set up registers R0 and R1 and location 12 (octal) of main memory (see next step). Continue.
4. If a failure is detected, examine location 12 (octal) of main memory. If location 12 is zero, halt the EP2. If location 12 is non-zero, transfer control to the address contained in location 12.
5. Load the remaining bytes of the BD ROM into host memory.
6. Verify the BD ROM data transfer using the ROM checksum.
7. The host executes the citizenship test.
8. If the citizenship test fails, return control the the EP2 and halt.

DEQNA LED Indicators

LED 1	LED 2	LED 3	Definition
OFF	OFF	OFF	The DEQNA passed all citizenship tests.
OFF	OFF	ON	Transceiver, Ethernet, or cable error.
OFF	ON	ON	DEQNA internal error.
ON	ON	ON	Cannot upload BD ROM contents, the bootstrap has not yet executed, or the first setup packet (PE1) has failed.

Error Codes – If the CC test fails, the LED indications read:

LED 1	LED 2	LED 3	Definition
OFF	OFF	ON	Transceiver or Ethernet error.
OFF	ON	ON	DEQNA internal error.
ON	ON	ON	Cannot upload BD ROM contents or the first set-up packet (PE1) failed.

If the DEQNA passed the tests, all the LEDs are off.

The bits in register R0 indicate the test that failed. If bit 15 is the only bit set, the DEQNA passed all the QQ tests except those which require a connected transceiver. The errors/bits are defined as follows (multiple bits can be set).

Error Bit	Error Definition and Source(s)
15	External loopback not operational (tests 7 and 8) Ethernet not operational H4000 not operational (blown fuse, disconnected)
14	Operation completion status check (all tests) CSR status after final reset not nominal CSR status after transmit and/or receive not nominal Receive descriptor flags and status word 1 not nominal Received byte length check Transmit descriptor flags and status word 1 not nominal TDR value = 0
13	Sanity timer interrupt (general error) Power failed during test Unexpected sanity timer interrupt
12	Set-up packet or target address echo check (all tests) Set-up packet transmit time-out Transmit status not nominal Set-up packet receive time-out Receive status not nominal Echoed data not identical to transmitted data Extra word at end of set-up packet not nominal
11	Spurious or missing device interrupt (general error) Expected device interrupt not detected Device did not detect nonexistent memory (NXM) bus state 16- or 22-bit addressing failure Unexpected DEQNA device interrupt
10	Bus time out or NXM interrupt (general error) I/O page not accessible for read or write Cannot read station address ROM Test code attempted to access nonexistent memory

Error Bit	Error Definition and Source(s)
09	Device operation time-out (all tests) Unit under test failed to complete a transmit and/or receive in time
08	Undefined
07	Undefined
06	Undefined
05	Error non external loopback test check (test 6) Ethernet protocol processing check Ethernet min short vs. d length processing check Ethernet maximum valid length processing check
04	DMA interface processing check (test 6) DMA odd/even length and address processing check Multi element transmit descriptor processing check Chained transmit descriptor processing check
03	Internal extended loopback transmit buffer data check (test 5) Ethernet protocol processing check Transmit buffer memory malfunction Packet size processing error (protocol error)
02	Station address compare test check (test 4) Address filter logic passing all addresses Address filter logic not passing expected addresses
01	Station address/receive FIFO processing check (test 3) Target address RAM malfunction Packets not properly stored in receive FIFO Receive FIFO memory malfunction
00	Invalid ethernet station address (test 1) I/O page register read failure (see also bit 10) Unit under test is not a DEQNA (M7504) Station address ROM malfunction Invalid DEQNA address

DHV11 8-LINE ASYNCHRONOUS MULTIPLEXER

GENERAL

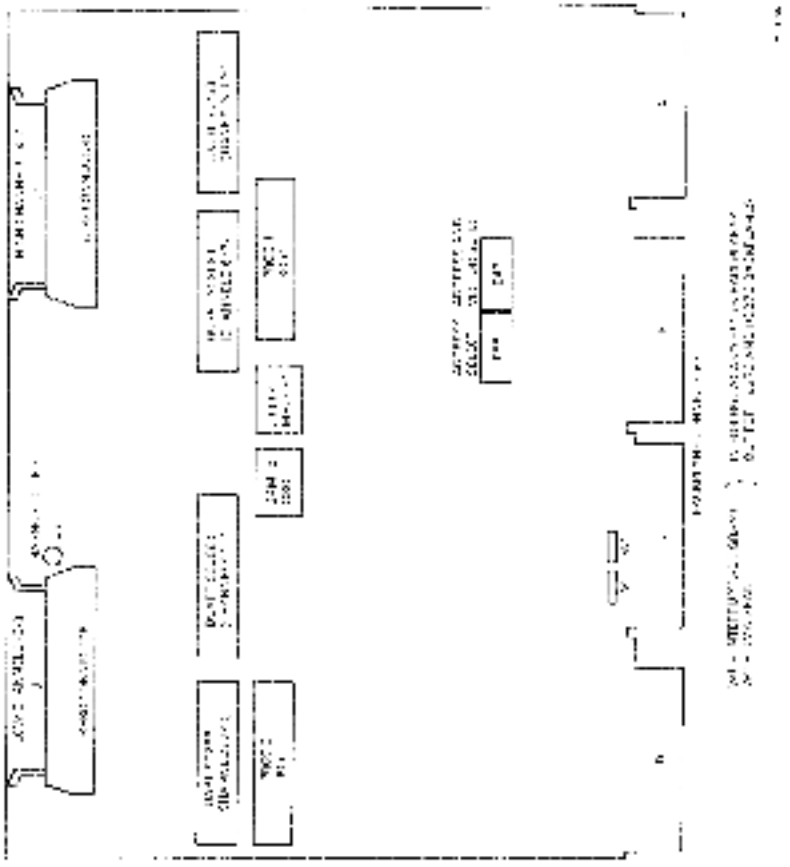
The DHV11/M3104 is an asynchronous multiplexer which provides eight full duplex serial data channels on a Q Bus system (Q18+, Q18-, and Q22 bit addressing). Uses include data concentration, terminal interfacing, and control.

Features:

- Eight full-duplex asynchronous data channels
- Direct memory access (DMA) or single character programming transfers on transmit
- Large 256-entry first in first-out (FIFO) buffer for received characters, dataset status changes, and diagnostic information
- RS-423-A/V.10/X.26 and RS-232-C/V.28 compatible
- Full duplex point-to-point or auto-answer dial-up operation
- Programmable split speed per line
- Total module throughput of 15,000 characters-per-second
- Q18+, Q18-, and Q22-bus compatible
- Automatic flow control of transmitted and received data
- Self-test and background monitor diagnostics
- Programmable test facilities
- Single quad height module (M3104).

NOTE

All functions are programmable, except for device address and vector selection which are done by module hardware switches.



M3104 module

Voltage	Bus Loads	
	AC	DC
5 Vdc ±5% @ 4.0 A 8.0 A (max.)	1.0	7.8

±12 Vdc ±3% @ 475 mA
900 mA (max.)

Standard Addresses

Floating addresses 17760020 to 17760030

Vectors

Floating vectors 300 to 700

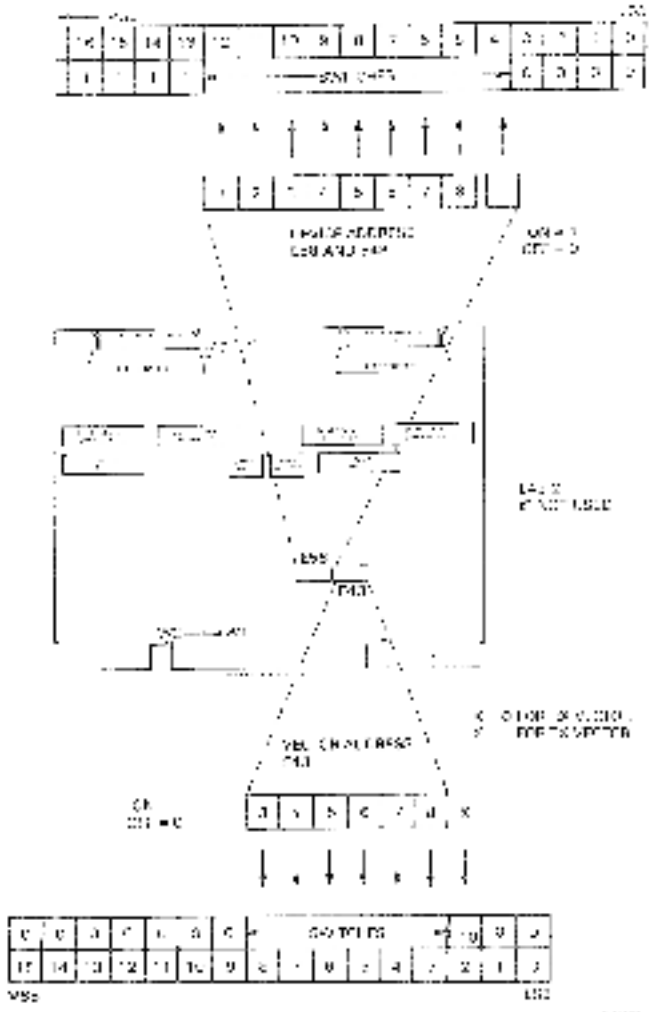
Diagnostic Programs

CVDHA?
CVDHB?
CVDHC?

Related Documentation

DHV11 Technical Manual (EK-DHV11-TM)

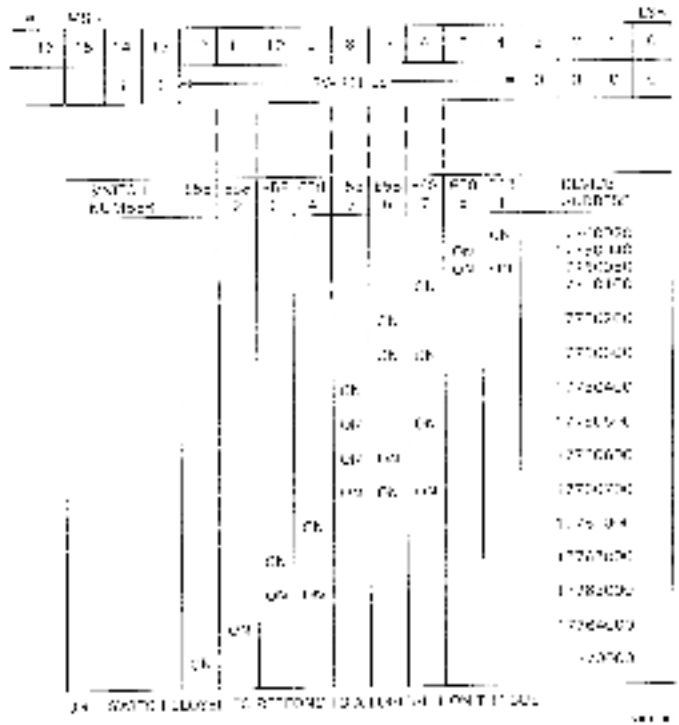
Switches and Jumpers
Two switchpacks select the device address and the vector address of the module



Switch and jumper locations

Address Switches

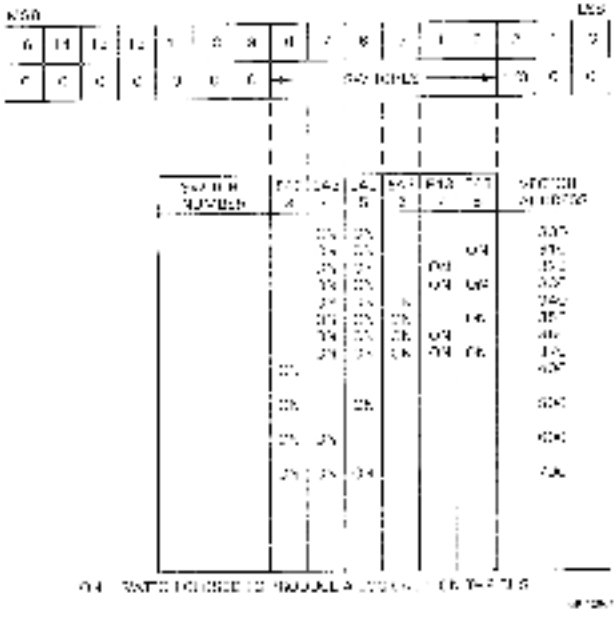
The device address for the DHV11 is set on switchpacks E58 and E43. The following table explains the relationship between device addresses and switch positions. The table gives the Q22 bus address for each entry. The equivalent Q16 and Q18 bus addresses will be 161xxx and 76xxxx respectively.



Device Address Selection Guide

Vector Switches

During an interrupt acknowledge sequence, the DHV11 returns a 7-bit interrupt to the host. The six high order bits of this vector are derived from S15-S0 to S5. The table below explains how switch positions relate to vector addresses.



Vector Address Selection Guide

Throughput
Each channel is capable of full duplex operation at data rates up to 38,400 bits/s.

Maximum Throughput

Per Channel Mode	Send	Receive
Character mode	1800 char	4000 char
DMA mode	7800 char	4000 char

M3104 Jumpers (W1 and W2)
The M3104 is compatible with all Q-Bus backplanes, including those that have slots C and D.

Backplanes	W1	W2
Q/Q – 19275	IN	IN
Q/Q – 19270	IN	IN
Q/QD – 19276	OUT	OUT
Q/QD – 19272	OUT	OUT

Bus Grant Continuity Jumpers – Backplanes suitable for DHV11 fall into two groups:

Q/CD – Q-Bus on A and B connectors, user-defined signals on C and D
Q/Q – Q-Bus on A and B, and C and D connectors.

In Q/CD backplanes, bus grant signals pass through each installed module via the A and B connectors of each bus slot.

Q/Q backplanes are designed so that quad-height options can be installed in a quad-height bus slot. The Q-Bus lines are routed as follows:

AR, first slot
CD, first slot
CD, second slot
AB, second slot – and so on

DHV11 Bus Connections

Category	Signal	Function	Pin Number
Data/Address	BDAL0L – 15L	Data/Address lines	AU2 – AV2 BE2 – BV2
	BDAL16L – 17L		AC1 – AD1
	BDAL18L – 21L		BC1 – BF1
Data Control	BDOUTL	Data output enable	AF2
	SYPLYL	Reply handshake	AH2
	BDINL	Data input strobe	AJ2
	BSYNCL	Synchronize synchr	AJ2
	BWTBTL	Write byte control	AK2
	BDCOKL	I/O page select	AP2
Interrupt Control	BINTL	Int. req. level 4	AL2
	BIAKIL	Int. ack. input	AV2
	BIAKOL	Int. ack. output	AN2
DMA Control	BDMRL	DMA request	AN1
	BDMGIL	DMA grant input	AH2
	BDMGOL	DMA grant output	AG2
	BSACKL	Bus grant acknowledge	BN1
System Control	BINITL	Initialization strobe	AT2
Power Supplies	+5 V	dc volts	AA2 – DA2
	+12 V	dc volts	BD2
Grounds	GND	Ground connections	AC2 – DC2
	GND	Ground connections	AT1 – DT1
	GND	Ground connections	AJ1 – BJ1
	GND	Ground connections	AM1 – BV1

MODULE INSTALLATION

Once the backplane position of the DHV11 has been defined, the module can be installed in the backplane.

CAUTION

Switch off power before inserting or removing modules. Be careful not to snag module components on the card guides or adjacent modules.

1. Connect the H3304 cables to J1 and J2 as shown above.
2. Install the module in its correct backplane position.
3. Check that -5 V is present between AA1 and ground.
4. Check that +12 V is present between BB2 and ground.

DHV11 Installation

CABLES AND CONNECTORS

Cable Kit Contents

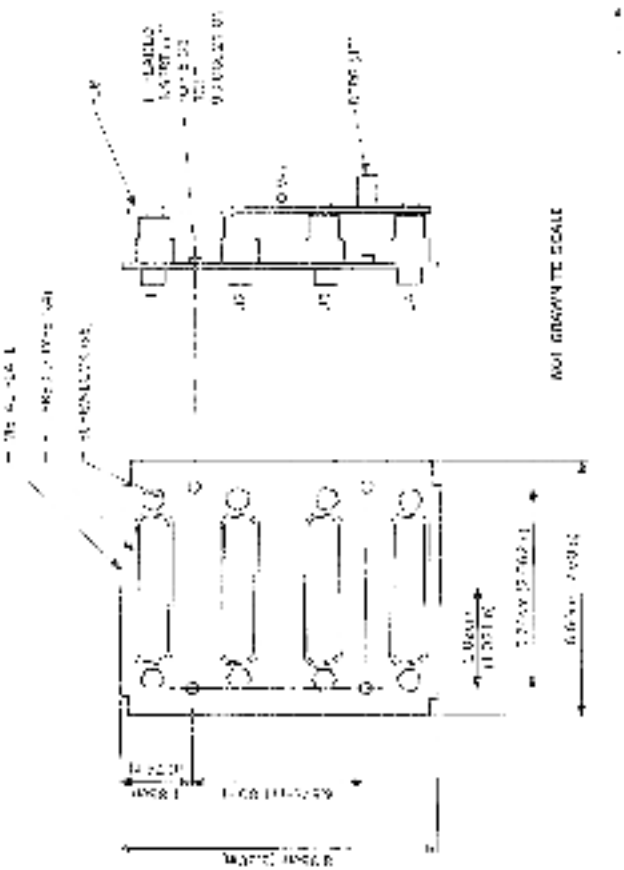
- 2 BC05 L cables (system defined length)
- 2 H3173-A distribution panels
- 1 Staggered loopback connector
- 1 H325 line loop connector

Cable Kit Ordering Information:

DHV11-AP	**System option.** Includes module, interface, cables and I/O connection cable insert. This option must be ordered with the system in which it is to be installed.
DHV11-M	**Upgrade option.** Includes case module only. For system installation select one of the following cabinet kits:
CK-DHV11-AA	Cabinet kit. For use with (PDP-11/23) BA11-VA/MF box.
CK-DHV11-AB	Cabinet kit. For use with (MICRO/PDP-11) BA23 box.
CK-DHV11-AC	Cabinet kit. For use with (PDP-11/23-PLUS) H949 panel.

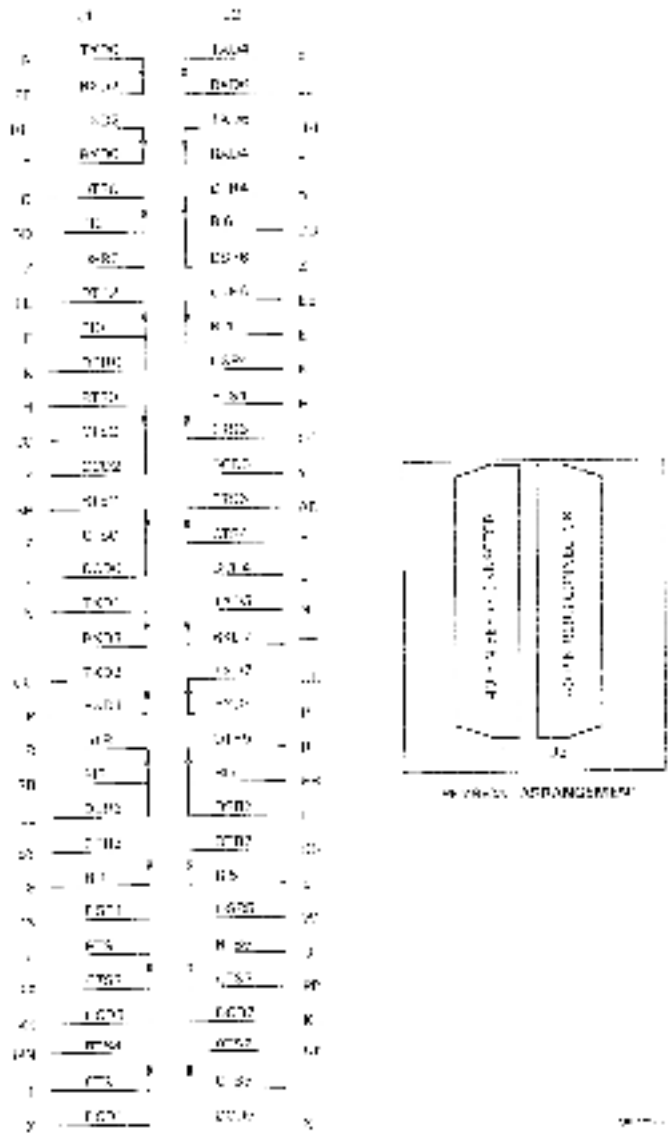
Distribution Panel

Each H3173-A distribution panel adapts one of the DHV11's dany connectors to four subminiature D-type (RS232C) connectors. Noise filtering is provided on each pin of the RS232C connectors. This reduces electromagnetic radiation from the cables. It also provides the logic with some protection against static discharge.



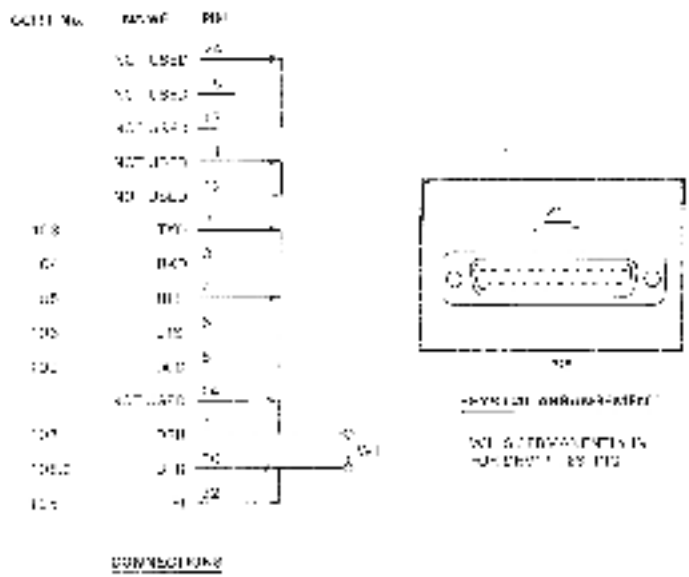
Staggered Loopback Test Connector H9277

The H9277 test connector is used during diagnostic tests. It allows all channels to be tested. Using this connector you can trace a channel fault to one of two channels.



Staggered Loopback Test Connector

The line loopback test connector (H325) can be used during diagnostic tests to trace a fault to a single channel.



Connector Pin Designation

Null Modem Cables

Null modem cables are used for local RS232C connection. Because of FCC regulation, the cable specifications for the United States and Canada are different from those for non-FCC countries. Other countries may also have similar electromagnetic interference (EMI) control regulations. EMC/RFI shielded cabinets are now available for systems which conform to FCC requirements.

Recommended null modem cables are as follows:

BC22U (for EMC/RFI shielded cabinets)

Round 6 conductor fully shielded cable to FCC specification

Subminiature 25-pin D-type female connector mounted on each end

Lengths available:

BC22D-10 3.1 m (10 ft)
BC22D-25 7.62 m (25 ft)
BC22D-35 10.72 m (35 ft)

BC22D-50 – 15.24 m (50 ft)
BC22D-75 – 22.9 m (75 ft)
BC22D-A0 – 30.48 m (100 ft)
BC22D-B3 – 76.2 m (250 ft).

BC03M

Round 6-conductor (three twisted pairs), each pair shielded

Cables over 30.48 m (100 ft) have a 25-pin, subminiature, D-type female connector at one end. The other end is unterminated for running through conduit.

Cables 30.48 m (100 ft) and less have a similar connector at each end.

Lengths available

BC03M-25 – 7.62 m (25 ft)
BC03M-A0 – 30.48 m (100 ft)
BC03M-B3 – 76.2 m (250 ft)
BC03M-F0 – 152.4 m (500 ft)
BC03M-10 – 304.8 m (1000 ft).

BC22A

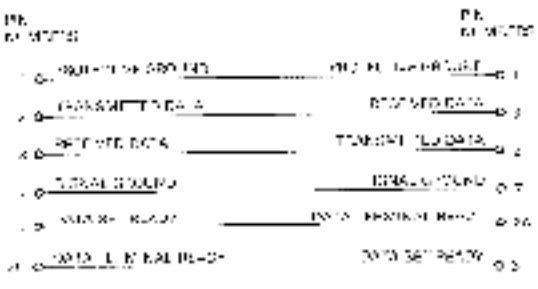
Round 8 conductor cable

Subminiature, 25-pin, D-type female connector moulded at each end

Lengths available:

BC22A-10 – 3.1 m (10 ft)
BC22A-25 – 7.62 m (25 ft)

Cables of groups 1, 2, and 3 are all connected. The cables are not polarized. They can be connected either way around.



Null Modem Cable Connections

Full Modem Cables

Recommended full modem cables are as follows:

BC22F (for H4000/H7 shielded cabinets)

Round 25-conductor fully shielded cable
Subminiature, 25-pin, D type female connector on one end, male connector on the other

Lengths available:

BC22F-10 – 3.1 m (10 ft)
BC22F-25 – 7.62 m (25 ft)
BC22F-35 – 10.72 m (35 ft)
BC22F-50 – 15.24 m (50 ft)
BC22F-75 – 22.9 m (75 ft)

BC05D

Round 25-conductor cable

Subminiature, 25-pin, D-type female connector on one end, male connector on the other

Lengths available:

BC05D-10 – 3.1 m (10 ft)
BC05D-25 – 7.62 m (25 ft)
BC05D-50 – 15.24 m (50 ft)
BC05D-60 – 18.3 m (60 ft)
BC05D-A8 – 30.48 m (100 ft)

CAUTION

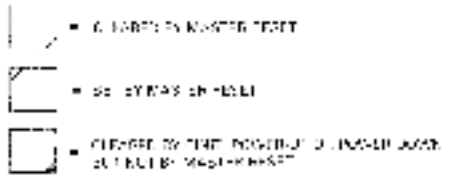
In some countries, protective hardware may be needed when connecting to certain lines. Refer to the national regulations before making a connection.

Register Bit Definitions

Register formats which provide the definitions of register bits, are coded as follows:

Bits marked ' may hold data, set, status, or special information from the diagnostic programs.

Registers which are modified by reset sequences are coded, as shown below:



Register Coding

DHV11 Registers

Register		Address (Octal)	Type
Control/Status Register	(CSR)	Base	Read/write
Receive Buffer	(RBUF)	Base + 2	Read only
Transmit Character	(TXCHAR)	Base + 2 (M)	Write only
Line Parameter Register	(LPR)	Base + 4 (M)	Read/write
Line Status	(STAT) 6 (V)	Base + 6 (M)	Read only
Line Control	(LNCTRL)	Base + 10 (M)	Read/write
Transmit Buffer Address 1	(TBUFADR1)	Base + 12 (M)	Read/write
Transmit Buffer Address 2	(TBUFADR2)	Base 14 (M)	Read/write
Transmit Buffer Count	(TBUFCT)	Base 16 (M)	Read/write

Control and Status Register (CSR)

Bit	Name	Description
<3:0>	IND.ADDR.REG (indirect address register) (R/W)	These bits are used to select the wanted channel register when accessing a block of indexed (M) registers. They form the binary number of the channel which is to be accessed.
5	MASTER.RESET (master reset) (R/W)	Set by the host, in order to reset DHV11. Stays set while DHV11 runs a self-test diagnostic, and then performs an initialization sequence. The bit is then cleared to tell the host that the process is complete. This bit is set by BINIT (bus initialization signal) or by the host processor setting CSR<5>. The host should not write to this bit when it is already set.
6	RXIE (receiver interrupt enable) (R/W)	When set, this bit allows the DHV11 to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated under the following conditions: 1. RXIE is set and a character is placed into an empty FIFO. 2. The FIFO is not empty and RXIE is changed from 0 to 1. Cleared by BINIT but not by MASTER.RESET.

Control and Status Register (CSR) (Cont)

Bit	Name	Description
7	RX DATA AVAIL (received data available (RD)	When set, indicates that a received character is available. This bit is clear when the FIFO is empty. It is used to request an RX interrupt. Set after MASTER.RESET because the FIFO contains diagnostic information
<11:8>	TX.LINE (transmit line number) (RD)	If TX.ACTION is set, these bits hold the binary number of the channel which has just: 1. Completed a DMA block transfer 2. Accepted a single character for transmission 3. Aborted a DMA block transfer. If TX.DMA.ERR is also set, these bits contain the binary number of the channel which has failed during a DMA transfer.
12	TX.DMA.ERROR (transmit DMA error) (RD)	A set with TX.ACTION also set, means that the channel indicated by CSR<11:8> has failed to transfer DMA data within 10.7 microseconds of the bus request being acknowledged, or that there is a memory parity error. TBUFFAD1 and TBUFFAD2 registers will contain the address of the memory location which could not be accessed. TBUFFDT will be cleared.
13	DIAG FAIL (diagnostic fail) (RD)	When set, indicates that DHV11 internal diagnostics have detected an error. The error may have been detected by the self-test diagnostic or by the DMP.

Control and Status Register (CSR) (Cont)

BR	Name	Description
		This bit is associated with the diagnostic-passed LED. When it is set, the LED will be off. When it is cleared, the LED will be on. The bit is set by MASTER.RESET. It is cleared after the internal diagnostic programs have been run successfully. It is only valid after the MASTER.RESET bit (CSR<00>) has been cleared.
14	TXIE (Transmit Interrupt enable) (R/W)	When set, allows the DHV11 to (TX.ACT ON) becomes set. Cleared by BINIT but not by MASTER.RESET. This bit is set by DHV11 when:
15	TX.ACTION (Transmitter Action) (RO)	1. The last character of a DMA buffer has left the DUART. 2. A DMA transfer has been aborted. 3. A DMA transfer has been terminated by the DHV11 because of nonexistent memory being addressed, or because of a memory parity error. 4. When a single-character programmed output has been accepted. That is to say, the character has been taken from TX BUFF. This bit is cleared when the CSR is read by the host. Also cleared by MASTER RESET.

NOTE

CSR contents should only be changed by a MOV or MOVB instruction. Other instructions may lose the state of the TX ACTION bit (CSR<15>).

DLV11 SERIAL LINE UNIT

Amps		Bus Loads		Cables
+5	+12	AC	DC	
II	0.12	2.40	*	BC05M for 20 mA
(1.0 max.)	(0.25 max.)			BC05C for Bell 103 modem and EIA
				BC05C plus H312A or H888 for EIA terminal

Standard Addresses

	Console	Second Terminal	Modem (Auto Mode)
RCSR	177560	176500	176610
RBUF	177562	176502	176612
XCSR	177564	176504	176614
XBUF	177566	176506	176616

Vectors

	Console	Second Terminal	Modem
Receiver Interrupt	60	400	300
Transmitter Interrupt	64	304	314

Diagnostic Program

Refer to Appendix A.

NOTE

The DECX module DLA7 requires a wraparound connector to run. The connector is not available and must be made up from the following parts:

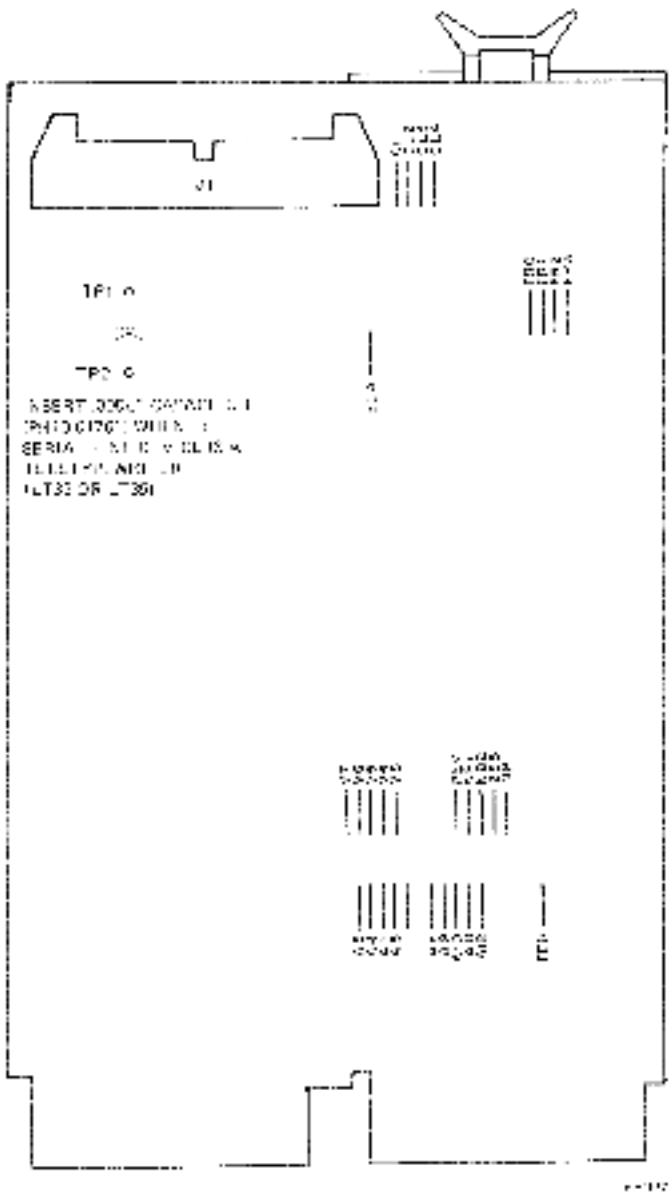
Berg connector	PN 12-10918-15
Berg pins	PN 12-10089-07
No. 22 AWG wire	PN 90-07350-00.

Connect the following pins:

F to J
H to E

Related Documentation

Field Maintenance Print Set (MP00066)
Microcomputer Interfaces Handbook (EB-20175-20)



2. V11 Jumpers

DLV11 Address Bits

DLV11 Interrupt Vector Bits

DLV11 SLU Factory Jumper Configuration

Jumper Designation	Jumper Status	Function
A3	I	This arrangement of jumpers A3 through A12 im-
A4	R	plements the octal device address 17756X,
A5	R	which is the assigned address for the console
A6	R	device SLU. The least significant digit is hard
A7	I	wired on the module to address the four SLU de-
A8	R	vice registers as follows:
A9	R	
A10	R	X — C, XCSR address
A11	R	X — 8, Receive data register address
A12	R	X — A, XCSR address
		X — 9, Transmit data register address.
V3	I	This jumper arrangement implements the inter-
V4	R	rupt vector addresses 60 for received data and
V5	R	64 for transmitted data.
V6	I	
V7	I	
NP	R	No parity.
2SB	R	Two stop bits (installed on D322 and D324).
NB2	R	8 bit data bits
NB1	R	
PEV	R	Even parity if NP installed.
FEI	I	Halt on framing error (removed on D322 and D324).
EIA	R	RS-232-C EIA operation disabled (installed on D322 and D324).
BR0	R	
BR1	R	9600 baud rate selected.
BR2	R	
BR3	R	
CL1	I	20 mA current loop active receiver and trans- mitter selected.
CL2	I	
CL3	I	
CL4	I	

Number of Data Bits

	W21	W22
5	Installed	Installed
6	Removed	Installed
7	Installed	Removed
8	Removed	Removed

Number of Stop Bits Transmitted

W23 installed — one stop bit.
W23 removed — two stop bits.

Parity Transmitted

W24 removed — no parity bit.
W24 and W25 installed — odd parity.
W24 installed and W25 removed — even parity.

Framing Error

W26 installed — halt on framing error (console).
W26 removed — do not halt on framing error.

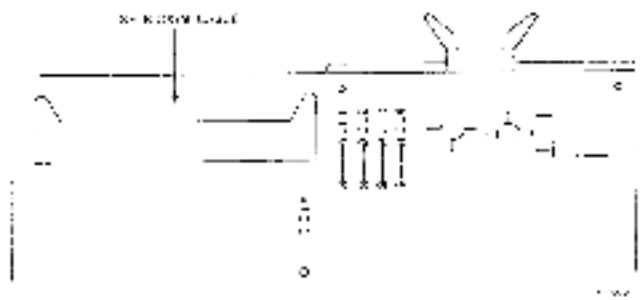
Unit	Address	Address Jumpers									
		A12	A11	A10	A9	A8	A7	A6	A5	A4	A3
Console	177560	R	R	R	R	R	I	R	R	R	I
First Option	176500	R	R	R	I	R	I	R	I	I	I
Second Option	176510	R	R	R	I	R	I	R	I	I	R
Third Option	176520	R	R	R	I	R	I	R	I	R	I
Modem	176610	R	R	I	R	R	R	I	I	I	R

Unit	Vector	Vector Jumpers				
		V7	V6	V5	V4	V3
Console	60	I	I	R	R	I
First Option	300	R	R	I	I	I
Second Option	310	R	R	I	I	R
Third Option	320	R	R	I	R	I
Modem	500	R	R	I	I	I

Baud Rate Selection

Baud Rate	FR3	FR2	FR1	FR0
50	I	I	R	I
75	I	I	R	R
110	R	R	R	R
134.5	I	R	I	I
150	R	R	R	I
200	I	R	I	R
300	R	R	I	R
600	I	R	R	I
1200	R	I	R	R
1800	R	I	R	I
*2400	I	R	R	R
*2400	R	R	I	I
4800	R	I	I	R
9600	R	I	I	I

*Either configuration may be used. Use second configuration for DD22 and DS74.

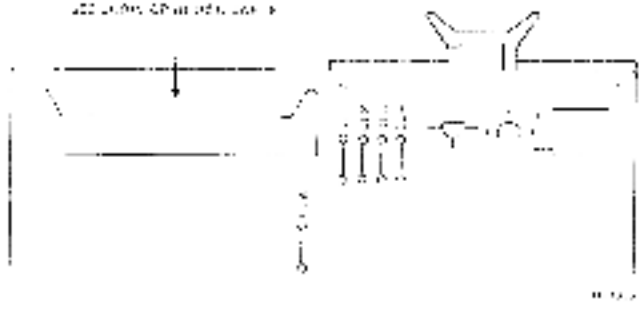


Active transmit - CL3 and CL4 installed.
Active receive - CL1 and CL2 installed.

NOTE
CL2 And CL3 are 160 Ω resistors.

Passive transmit — CL3 and CL4 as in preceding figure.
Passive receive — CL1 and CL2 as in preceding figure.

NOTE
When configured for passive operation, the ( ) and ( ) lines are reversed. Use a BC05F cable.

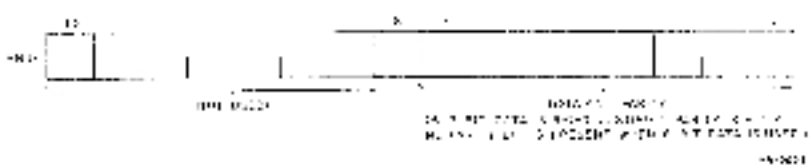


Jumper H7 must be inserted for H7 operation. Jumpers CL1 through CL4 do not have to be removed when CIA is inserted.

Receiver Control/Status Register (RCSR)

RCSR Bit Definitions

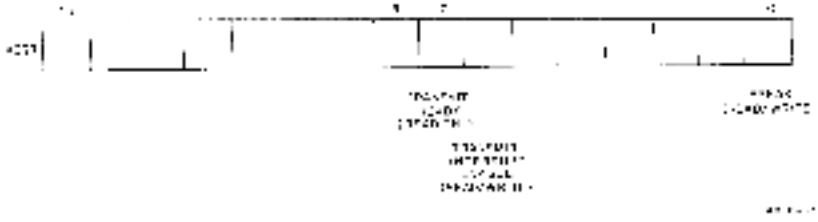
Bit	Function
15	Dataset Status – Set when CARRIER or CLEAR TO SEND and DATA SET READY signals are asserted by an E A device. Read-only
14-08	Not used. Read as 0
07	Receiver Done – Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is addressed or when the SDOOK H signal goes false (low). A receiver interrupt is enabled by the DLV11 when this bit is set and receiver interrupt is enabled (bit 6 is also set). Read-only
06	Interrupt Enable – Set under program control when it is desired to generate a receiver interrupt request when a character is ready for input to the processor (bit 7 is set). Cleared under program control or by the BINIT signal. Read/write
05-01	Not used. Read as 0.
00	Reset Enable – Set by program control to advance the paper tape reader on a teletypewriter device to input a new character. Automatically cleared by the new character's start bit. Write only.



Receiver Buffer Register (RBUF)

RBUF Bit Definitions

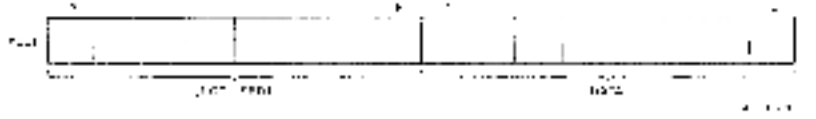
Bit	Function
15-02	Not used. Read as 0.
07-00	Contains zero to eight data bits in a right justified format. MSB is the optional parity bit. Read only.



Transmitter Control/Status Register (XCSR)

XCSR Bit Definitions

Bit	Function
15-08	Not used. Read as 0.
07	Transmit Ready – Set when XBUF is empty and can accept another character for transmission. It is also set during the power-up sequence by the BDCOK H signal. Automatically cleared when XBUF is loaded. When transmitter interrupt is enabled (bit 6 also set), an interrupt request is asserted by the DLV11 when this bit is set. Read only.
06	Interrupt Enable – Set under program control when it is desired to generate a transmitter interrupt request when the DLV11 is ready to accept a character for transmission. Reset under program control or by the BINIT signal. Read/write.
05-01	Not used. Read as 0.
00	Break – Set or reset under program control. When set, a continuous space level is transmitted. BINIT resets this bit. Read/write.



Transmitter Buffer Register (XBUF)

XBUF Bit Definitions

Bit	Function
15-08	Not used.
07-00	Contains five to eight right-justified data bits. Loaded under program control for serial transmission to a device. Write only.

DLV11-E ASYNCHRONOUS SERIAL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.0	0.15 (0.20 max.)	1.96	1	BC05C

Standard Address

RCSR	175610
RBUF	175612
XCSR	175614
XBUF	175616

NOTE

The DLV11-E is shipped configured for use with a modem.

Standard Vectors

Floating Configurable within the range of 300–770. Refer to Appendix B.

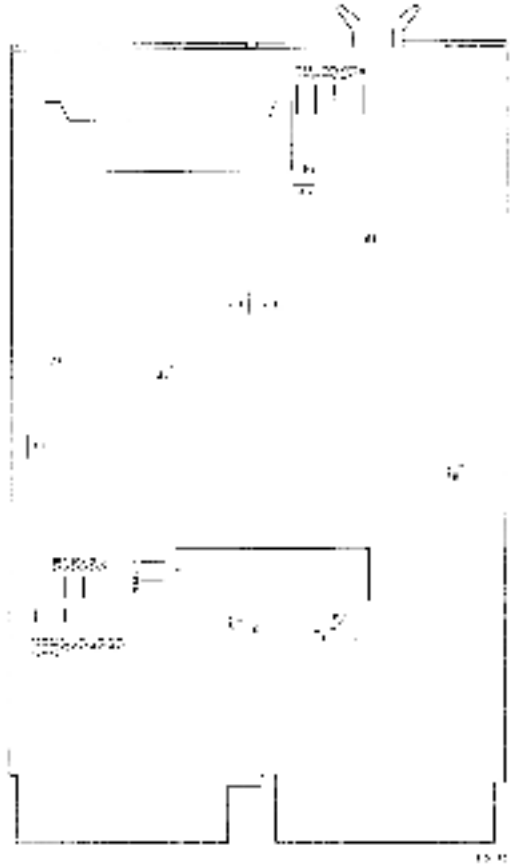
		MINC/DECLAB
Receiver Interrupt	300	330
Transmitter Interrupt	304	334

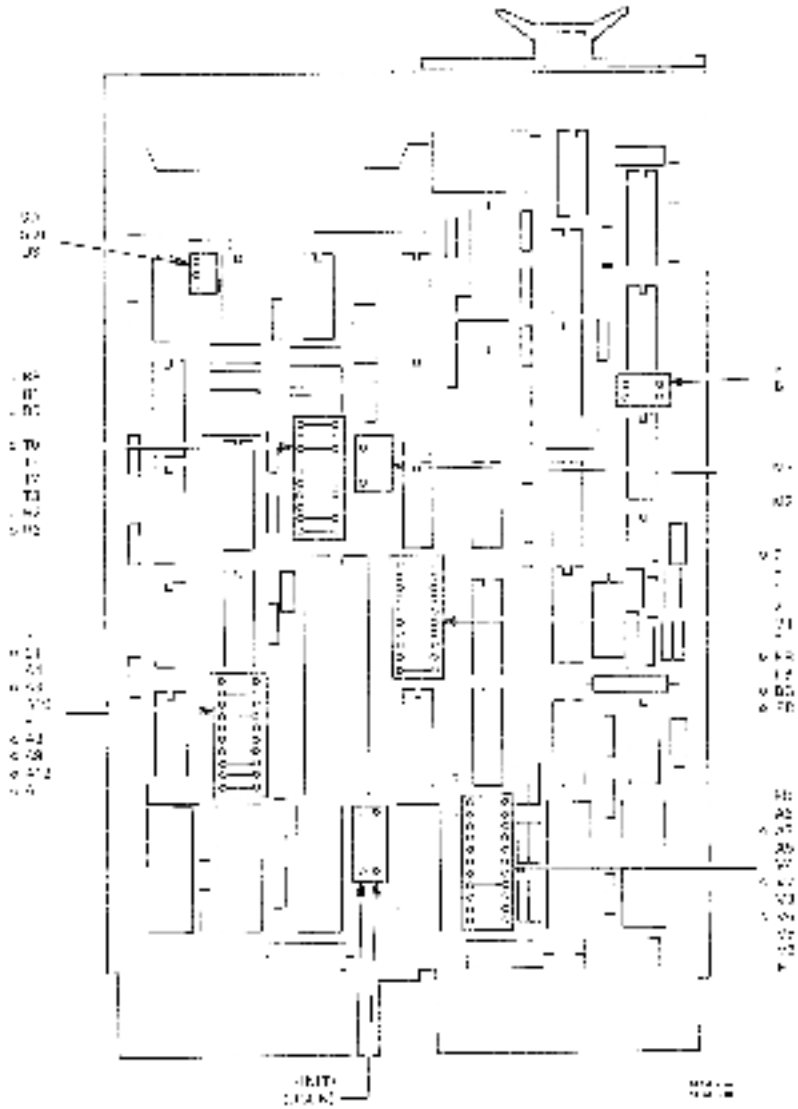
Diagnostic Programs

Refer to Appendix A.

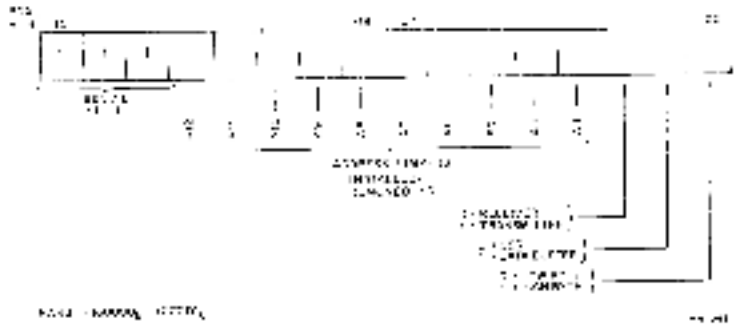
Related Documentation

DLV11-E and DLV11-F Asynchronous Line Interface User's Manual (EK-DLV11-UP)
Field Maintenance Print Set (MP00460)
Microcomputer Interfaces Handbook (EB-20175-20)

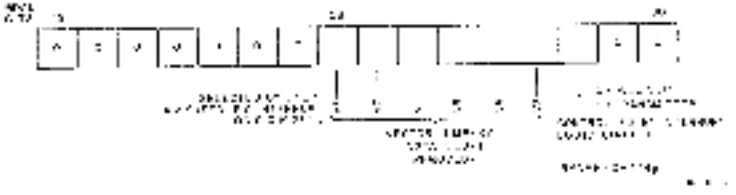

M8017 Revision C E.ch



M8017 Revision D Fitch



DLV11-E Addresses



DLV11-E Interrupt Vectors

Unit	Address	Address Jumpers A5	A4	A5	A6	A7	A8	A9	A10	A11	A12
Console	177560	R	I	I	I	R	I	I	I	I	
First Option	176500	R	R	R	I	R	I	R	I	I	I
Second Option	176510	I	R	R	I	R	I	R	I	I	I
Third Option	176520	R	I	R	I	R	I	R	I	I	I
Modem*	176610	I	R	R	R	I	I	I	R	I	I

*Factory configuration

Unit	Vector	Vector Jumpers V3	V4	V5	V6	V7	V8
Console	060	R	I	I	R	R	R
First Option	300	R	R	R	I	I	R
Second Option	310	I	R	R	I	I	R
Third Option	320	R	I	R	I	I	R
Modem*	300	R	R	R	I	I	R

*Factory configuration

Jumper Configuration When Shipped

Jumper Designation	Jumper State	Function Implemented
A3	I	Jumpers A3 through A12 implement a device address 175610. The least significant octal digit is hardwired on the module to address the four device registers as follows:
A4	R	
A5	R	
A6	R	
A7	I	
A8	I	X + 0 RCSR
A9	I	X + 2 RBUF
A10	R	X + 4 XCSR
A11	I	X + 6 XBUF
A12	I	
V3	R	This jumper selection implements interrupt vector address 300 for receiver interrupts and 304 for transmitter interrupts.
V4	R	
V5	R	
V6	I	
V7	I	
V8	R	
B0	I	The module is configured to receive at 110 baud (see "Baud Rate Selection" table, which follows).
B1	R	
B2	I	
B3	I	
T0	I	The transmitter is configured for 9600 baud if split speed operation is used.
T1	R	
T2	R	
T3	R	
BC		Break generation is enabled.

Jumper Configuration When Shipped (Cont)

Jumper Designation	Jumper State	Function Implemented
P	R	Parity bit is disabled.
E	R	Parity type is not applicable when P is removed.
1 2	R R	Operation with eight data bits per character (see "Data Bit Selection" table, which follows).
PB	R	Programmable baud rate function disabled.
C C1	R I	Programmable baud rate function disabled. Common speed operation enabled.
S S1	R R	Split speed operation disabled.
H	R	Halt on framing error disabled.
S R	R I	Scroll on framing error disabled.
-FD	I	The DATA TERMINAL READY signal is not forced continuously true.
-FR	I	The REQUEST TO SEND signal is not forced continuously true.
RS	I	The circuitry controlling the REQUEST TO SEND signal is enabled.
FD	R	The FORCE BUSY signal is disabled.
M M1	R R	Factory test jumpers. Not defined for field use.

Baud Rate Selection

	Bit	Bit	Bit	Bit	Bit	Baud Rate
Program Control	15	14	13	12	11*	
Receive Jumpers	R3	R2	R1	R0		
Transmit Jumpers	T3	T2	T1	T0		
	I	I	I	I		50
	I	I	I	R		75
	I	I	R	I		110
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600

I = jumper inserted = program bit cleared.
R = jumper removed = program bit set.

*Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Jumper P8 must be inserted to enable baud rate selection under program control.

Data Bit Selection

Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

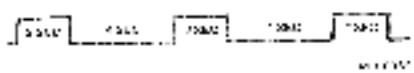
Jumper Definitions

Jumper	Function
A3–A12	These jumpers correspond to bits 3–12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3–V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding address bit on the LSI-11 bus.
R0–R5	Receiver and transmitter baud rate jumpers selected during common speed operation. Receiver-only baud rate select jumpers used during split speed operation.
T0–T3	Transmitter baud rate select jumpers used during split speed operation. Both receiver and transmitter baud rates used if maintenance mode is entered during split speed operation.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity; inserted for odd parity. Receive checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits.
PB	Jumper is inserted to enable the programmable baud rate capability.
C, C1	These jumpers are inserted for common speed operation. (Note that S and S1 must be removed when C and C1 are inserted.)

Jumper Definitions (Cont)

Jumper	Function
G, G1	Inserted for split speed operation. (Note that G and G1 must be removed when G and G1 are inserted.)
H	This jumper is inserted to assert BHALT L when a framing error is received (except when the maintenance bit is set). This causes the LSI-11 to halt mode.
B, B	Jumper B is inserted to negate BDCOK H when a RBI-AK signal or framing error is received, except when the maintenance bit is set. This causes the LSI-11 to reload the bootstrap. (Jumper -B must be removed when B is inserted.)
-DR	Jumper is removed to force DATA TERMINAL READY signal on.
-RR	Jumper is removed to force REQUEST TO SEND signal on.
RS	This jumper is inserted to enable normal transmission of the REQUEST TO SEND signal.
FB	Inserted to enable transmission of the FORCE BUSY signal (for Bell model 103F data sets).
M, M1	These are test jumpers used during the manufacturing of the module. They are not defined for field use.

DLV11-E RCSR Bit Assignments

Bit	Function
15	DATA SET INT (Data Set Interrupt) – This bit initiates an interrupt sequence provided that the DATA SET INT ENB bit (06) is also set. This bit is set whenever CAR DET, CLR TO SEND, or SEC REC changes state (i.e., on a 0-to-1 or 1-to-0 transition of any one of these bits). It is also set when ring changes from 0 to 1. Cleared by INIT or by reading the RCSR. Because reading the register clears the bit, it is in effect a 'read-once' bit.
14	Ring – When set, indicates that a RINGING signal is being received from the dataset. Note that the RINGING signal is not a level out on RIA control with the cycle time as shown below. Read only 
13	CLR TO SEND (Clear to Send) – The state of this bit is dependent on the state of the CLEAR TO SEND signal from the data set. When set, this bit indicates an ON condition; when clear, it indicates an OFF condition. Read only.
12	CAR DET (Carrier Detect) – This bit is set when the data carrier is received. When clear, it indicates either the end of the current transmission activity or an error condition. Read only.
11	RCVR ACT (Receiver Active) – When set, this bit indicates that the DLV11-E receiver is active. The bit is set at the center of the START bit, which is the beginning of the input serial data from the device. RCVR is cleared by the leading edge of R DONE H. Read only bit cleared by INIT or by R DONE H (b107).

DLV11-E RCSR Bit Assignments (Cont)

Bit	Function
10	SEC REC (Secondary Received or Supervisory Received Data) – This bit provides a receive capability for the reverse channel of a remote station. A space (−10 V) is read as a 1. (A transmit capability is provided by bit 05.) Read only.
9–8	Not used. Reserved for future use.
07	RCVR DONE (Receiver Done) – This bit is set when an entire character has been received and is ready for transfer to the LSI-11. When set, initiates an interrupt sequence, provided that RCVR INT ENB (bit 06) is also set. Cleared whenever the receiver buffer (RBUF) is accessed. Also cleared by INIT. Read only.
06	RCVR INT ENB (Receiver Interrupt Enable) – When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets.
05	DSET INT ENB (Data Set Interrupt Enable) – When set, allows an interrupt sequence to start when DATA SET INT (bit 15) sets.
04	Not used. Reserved for future use.
03	SEC XMIT (Secondary Transmitted or Supervisory Transmitted Data) – This bit provides a transmit capability for a reverse channel of a remote station. When set, transmits a space (+10 V). (A receive capability is provided by bit 10.) Read/write bit; cleared by INIT.
02	REQ TO SEND – A control lead to the data set which is required for transmission. Jumper on the DLV11-E lets this bit be REQ TO SEND or FORCE BUSY in the data set. Read/write bit; cleared by INIT.
01	DTR (Data Terminal Ready) – A control lead for the data set communication channel. When set, permits connection to the channel. When clear, disconnects the interface from the channel. Read/write bit; must be cleared by the program, not by INIT. The state of this bit is not defined after power-up.
00	Not used. Reserved for future use.

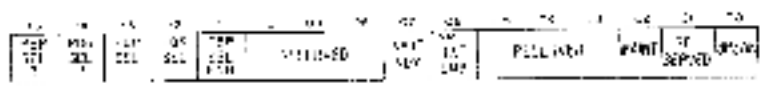
DLV11-E RBUF Bit Assignments

Bit	Function
15	Error – Used to indicate that an error condition is present. This bit is the logical OR of OR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes the error bit to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error-producing condition.

NOTE

Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.

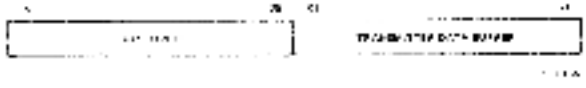
14	OR ERR (Overrun Error) – When set, indicates that reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read only; cleared by INIT.
13	FR ERR (Framing Error) – When set, indicates that the character that was read had no valid stop bit.
12	P ERR (Parity Error) – When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected. Read-only bit; cleared by INIT.
11–08	Not used. Reserved for future use.
07–00	Received Data Bits – Holds the character just received. If fewer than eight bits are selected, then the buffer is right-justified into the least significant bit positions. In this case, the higher unused bit or bits are read as 0s. Read-only bits, not cleared by INIT.



DLV11-E XCSR Bit Assignments

DLV11-E XCSR Bit Assignments

Bit	Function
15–12	PBR SEL (Programmable Baud Rate Select) – When set, these bits choose a baud rate from 50–9600 baud. Write only.
11	PBR ENB (Programmable Baud Rate Enable) – This bit must be set in order to select a new baud rate indicated by bits 12 to 15.
10–08	Not used. Reserved for future use.
07	XMIT RDY (Transmitter Ready) – This bit is set when the transmitter buffer (XDUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set. Read only bit; set by INIT.
06	XMIT INT ENB (Transmitter Interrupt Enable) – When set, allows an interrupt sequence to start when XMIT RDY (bit 07) is set. Read/write bits; cleared by INIT.
05–03	Not used. Reserved for future use.
02	MAINT Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when set if speed operation is enabled. Read/write bit; cleared by INIT.
01	Not used. Reserved for future use.
00	BREAK – When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.



DLV11-E XBUF Bit Assignments

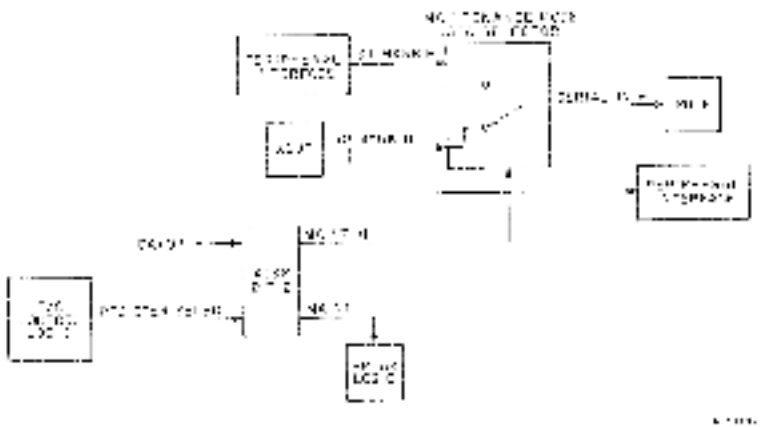
Bit	Function
15–08	Not used or defined. Not necessarily read as 0s.
07–00	Transmitter Data Buffer – Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so that it is right-justified in the low-order significant bits. Write-only bits; not necessarily read as 0s.

Maintenance Aids

The DLV11 is shipped with an EIA/CCITT modem test connector. This is plugged into the interface cable in place of a data set when maintenance programs are running.

Maintenance Mode Logic

In the maintenance mode, the DLV11-E and DLV11-F modules route their output data back to their input. To accomplish this, the computer program sets the maintenance bit in the XCSR. The latch holding this bit has two outputs. One goes to the break logic to prevent the generation of framing error signals during operation in the maintenance mode. The other output is applied to the maintenance mode data selector. The data selector normally routes the incoming data from the peripheral interface to the RBUF. In the maintenance mode, however, it switches its input to the output of the XBUF. This action loops the serial data out of the XBUF back into the RBUF and disconnects the peripheral interface's data. While in the maintenance mode, the serial output of the XBUF continues to go to the peripheral interface and out to the peripheral device.



Maintenance Mode Logic

DLV11-F ASYNCHRONOUS SERIAL LINE INTERFACE

DLV11-F (M8028) is a serial communication unit used to receive serial data, assemble it into parallel data, and send it to the LSI-11 bus. It also accepts parallel data from the bus and converts it to serial data for the peripherals. It also supports 20 mA current loops and EIA standard lines.

Amps		Bus Loads		Cables
0.5	4.12	AC	DC	BC08M for 20 mA
1.0	0.14	2.2	1.0	BC05C for EIA modem BC05C plus H3124 for EIA terminal

Standard Addresses

	Console	Second Terminal	Modem	MINC/DECLAB
RCSR	177560	176500	175610	175610
RBUF	177562	176502	175612	175612
XCSR	177564	176504	175614	175614
XBUF	177566	176506	175616	175616

Standard Vectors

Floating Configurable in the range of 000–770. Refer to Appendix B.

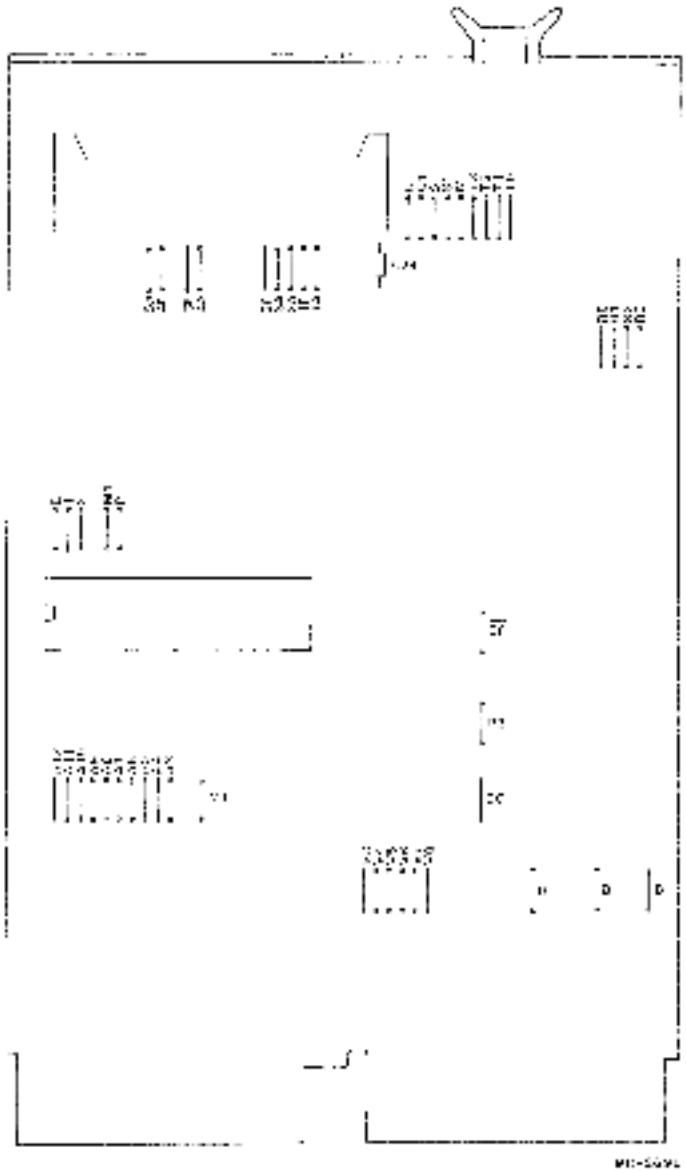
	Console	Second Terminal	Modem	MINC/DECLAB
Receiver	60	300	500	330
Transmitter	64	304	504	334

Diagnostic Programs

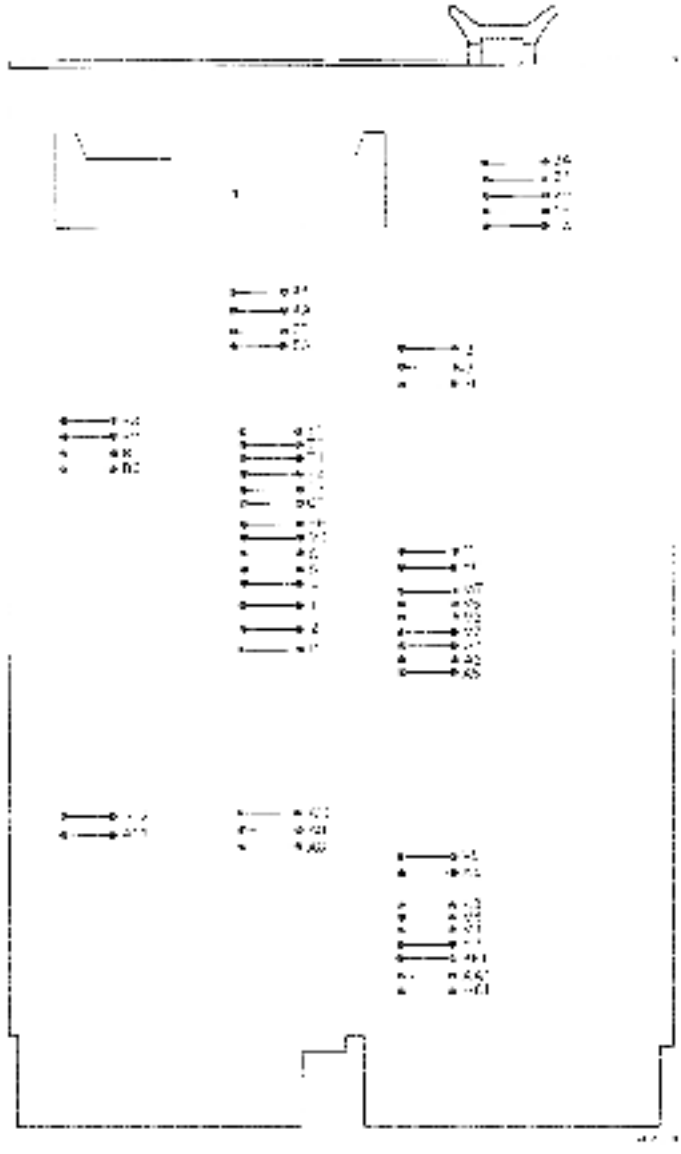
Refer to Appendix A.

Related Documentation

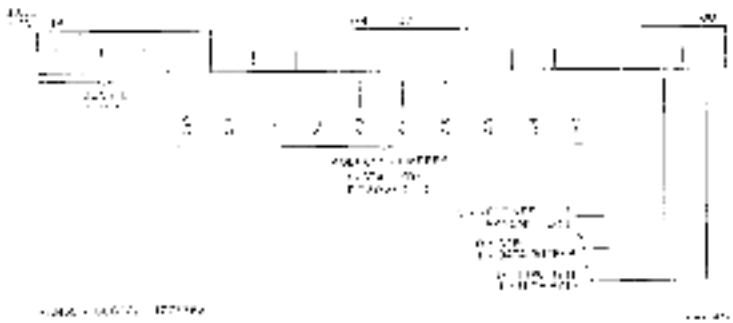
DLV11-E and DLV11-F Asynchronous Line Interface User's Manual (EK-DLV11-OP)
Field Maintenance Print Set (MP00461)
Microcomputer Interfaces Handbook (EB-20175-20)



DLV11-F Etch Rev B Jumper Locations



DLV11-F Etch Rev C Jumper Locations



DLV11-F Addresses

Address Jumpers

Unit	Address	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
Console	177560	I	I	I	I	I	R	I	I	I	R
First Option	176500	I	I	I	R	I	R	I	R	R	R
Second Option	176510	I	I	I	R	I	R	I	R	R	I
Third Option	176520	I	I	I	R	I	R	I	R	I	R

Etch Rev C

BD1	R
AA1	R
AD1	R

Vector Jumpers

Unit	Vector	V3	V4	V5	V6	V7	V8
Console	60	R	R	R	I	I	R
First Option	300	R	I	I	R	R	R
Second Option	310	R	I	I	R	R	I
Third Option	320	R	I	I	R	I	R

DLV11-F Interrupt Vectors

Jumper Configuration When Shipped

Jumper Designation	Jumper State	Function
A5	IN	Jumpers A5 through A12 implement device
A6	IN	address 17756X. The least significant octal
A7	IN	digit is hardwired on the module to address
A8	IN	the four device registers as follows:
A9	IN	
A10	IN	X — 0 RCSR
A11	IN	X — 2 RBUF
A12	IN	X — 4 XCSR
		X — 6 XBUF
V3	IN	This jumper selection implements interrupt
V4	IN	vector address 60 for receiver interrupts
V5	IN	and 64 for transmitter interrupts.
V6	OUT	
V7	OUT	
V8	OUT	
T0	IN	The transmitter is configured for 9600 baud
T1	OUT	if split speed operation is used.
T2	OUT	
T3	OUT	
BC	IN	Break generation is enabled.
P	IN	Parity bit is disabled.
E	OUT	Parity type is not applicable when P is removed

Jumper Configuration When Shipped (Cont)

Jumper Designation	Jumper State	Function
1	R	Operation with eight data bits per character.
2	R	(See "Data Bit Select on" table.)
FB	R	Programmable baud rate function disabled
C	I	Common speed operation enabled.
C1	I	
S	R	Split speed operation disabled
S1	R	
H	I	Halt on framing error enabled
B	R	Boot on framing error disabled.
B	I	
1A	I	The 20 mA current loop receiver is
2A	I	configured as an active receiver.
3A	I	
1P	R	
2P	R	
4A	I	The 20 mA current loop transmitter is
5A	I	configured for active operation
3P	R	
4P	R	
EF	I	Error flags disabled.
M	R	Factory test jumpers. Not defined for field use.
M1	R	
M	R	Maintenance bit disabled.

Baud Rate Selection

	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Baud Rate
Program Control Receive Jumpers Transmit Jumpers	R5 T5	R4 T4	R3 T3	R2 T2	R1 T1	
	I	I		I		50
	I	I		R		75
	I	I	R	I		110**
	I	I	R	R		134.5
	I	R	I	I		150
	I	R	I	R		300
	I	R	R	I		600
	I	R	R	R		1200
	R	I	I	I		1800
	R	I	I	R		2000
	R	I	R	I		2400
	R	I	R	R		3600
	R	R	I	I		4800
	R	R	I	R		7200
	R	R	R	I		9600
	R	R	R	R		19200

I — jumper inserted = program bit cleared.
R — jumper removed — program bit set.

* Bit 11 of the XCSR (write-only bit) must be set in order to select a new baud rate under program control. Also, jumper BR must be inserted to enable baud rate select bit under program control.

** When configured for 110 baud, the UART is set for two stop bits.

Data Bit Selection

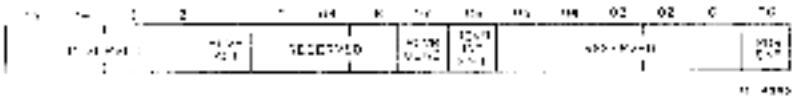
Jumpers		Number of Data Bits
2	1	
I	I	5
I	R	6
R	I	7
R	R	8

Jumper Definitions

Jumper	Function
A3–A12	These jumpers correspond to bits 3–12 of the address word. When inserted, they will cause the bus interface to check for a true condition on the corresponding address bit.
V3–V8	Used to generate the vector during an interrupt transaction. Each inserted jumper will assert the corresponding vector address bit on the UNIBUS.
RC, RS	Receiver and transmitter baud rate jumpers selected during common speed operation. Receiver-only baud rate select jumpers used during split speed operation.
TC, TS	Transmitter baud rate select jumpers used during split speed operation. Both receiver and transmitter baud rates used if maintenance mode is entered during split speed operation.
BG	Jumper is inserted to enable break generation.
P	Jumper is inserted for operation with parity.
E	Removed for even parity, inserted for odd parity. Receiver checks for appropriate parity and transmitter inserts appropriate parity.
1, 2	These jumpers select the desired number of data bits.
PB	Jumper is inserted in order to enable the programmable baud rate capability.

Jumper Definitions (Cont)

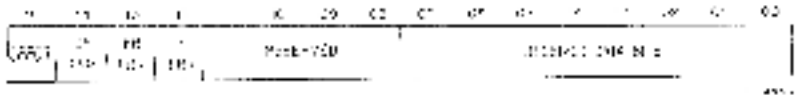
Jumper	Function
C, C1	These jumpers are inserted for common speed operation. Note that S and S1 must be removed when C and C1 are inserted.
S, S1	Inserted for split speed operation. Note that C and C1 must be removed when S and S1 are inserted.
H	This jumper is inserted to assert BHALT L when a framing error is received, except when the maintenance bit is set. This places the LSI-11 in the halt mode.
B, B	Jumper B is inserted to negate HDCOK H when a BREAK signal or framing error is received, except when the maintenance bit is set. This causes the LSI-11 to reload the bootstrap. (Jumper B must be removed when B is inserted.)
1A, 2A, 3A	These three jumpers are inserted to make the 20 mA and 3A current loop receiver active. (Jumpers 1P and 2P are removed when 1A, 2A, and 3A are inserted.)
1P, 2P	These jumpers are inserted to make the 20 mA current loop receiver passive. (Jumpers 1A, 2A, and 3A must be removed when 1P and 2P are installed.)
4A, 5A	Inserted to make the 20 mA current loop transmitter active. (3P and 4P must be removed when 4A and 5A are inserted.)
3P, 4P	Inserted to make the 20 mA current loop transmitter passive. (4A and 5A must be removed when 3P and 4P are inserted.)
RR	Jumper is removed to enable the error flags to be read in the high byte of the receiver buffer.
MT	When inserted, enables maintenance bit.
M, M1	These are test jumpers used during the manufacturing of the module. They are not defined for field use.



DLV11-F RCSR Bit Assignments

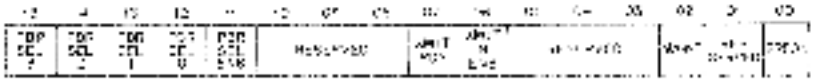
DLV11-F RCSR Bit Assignments

Bit	Function
15–12	Not used. Reserved for future use.
11	Receiver Active (RCVR ACT) – When set, this bit indicates that the DLV11-F interface receiver is active. The bit is set at the center of the start bit, which is the beginning of the incoming serial data from the device, and is cleared by the leading edge of RDONE H.
10–08	Not used. Reserved for future use.
07	Receiver Done (RCVR DONE) – This bit is set when an entire character has been received and is ready for transfer to the LSI-11 bus. When set, initiates an interrupt sequence provided RCVR INT ENB (bit 06) is also set. Read only bit; cleared whenever the receiver buffer (RBUF) is addressed or whenever RDR ENB (bit 00) is set. Also cleared by INIT.
06	Receiver Interrupt Enable (RCVR INT ENB) – When set, allows an interrupt sequence to start when RCVR DONE (bit 07) sets. Read/write bit; cleared by INIT.
05–01	Not used. Reserved for future use.
00	Reader Enable (RDR ENB) – When set, this bit advances the paper-tape reader in DIGITAL model 33 TTY units (LT33-C, LT33-A, -C) and clears the done bit (bit 07). This bit is cleared at the middle of the start bit, which is the beginning of the serial input from an external device. Also cleared by INIT. Write only.



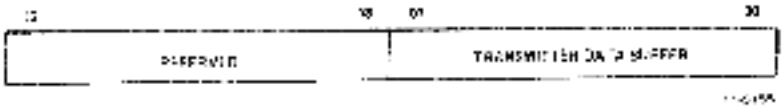
DLV11-F RBUF Bit Assignments

Bit	Function
15	Error – Used to indicate that an error condition is present. This bit is the logical OR of OVR ERR, FR ERR, and P ERR (bits 14, 13, and 12, respectively). Whenever one of these bits is set, it causes the error bit to set. This bit is not connected to the interrupt logic. Read-only bit; cleared by removing the error condition.
	NOTE Error indications remain present until the next character is received, at which time the error bits are updated. INIT clears the error bits.
14	Overrun Error (OP ERROR) – When set, indicates that the reading of the previously received character was not completed (RCVR DONE not cleared) prior to receiving a new character. Read-only bit; cleared by INIT.
13	Framing Error (FR ERR) – When set, indicates that the character just read had no valid stop bit. Read-only bit; cleared by INIT.
12	Parity Error (P ERR) – When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity is selected.
11–08	Not used. Reserved for future use.
07–00	Received Data Bits – Holds the character just read. If fewer than eight bits are selected, then the buffer is right-justified into the least significant bit positions. Then, the higher unused bit or bits are read as 0s. Read-only bits; not cleared by INIT.



DLV11-F XCSR Bit Assignments

Bit	Function
15-12	Programmable Baud Rate Select (PBR SEL) - When set, these bits choose a baud rate from 50 -9600 baud. Write only.
11	Programmable Baud Rate Enable (PBR ENB) - This bit must be set in order to select a new baud rate indicated by bits 12 to 15. Write only.
10-08	Not used. Reserved for future use.
07	Transmitter Ready (XMIT RDY) - This bit is set when the transmitter buffer (XBUF) can accept another character. When set, it initiates an interrupt sequence provided XMIT INT ENB (bit 06) is also set.
06	Transmitter Interrupt Enable (XMIT INT ENB) - When set, allows an interrupt sequence to start when XMIT RDY (bit 07) is set. Read/write bits; cleared by INIT.
05-03	Not used. Reserved for future use.
02	MAINT - Used for maintenance function. When set, connects the transmitter serial output to the receiver serial input while disconnecting the external device from the receiver serial input. It also forces the receiver to run at transmitter baud rate speed when split speed operation is enabled. Read/write bit; cleared by INIT.
01	Not used. Reserved for future use.
00	Break - When set, transmits a continuous space to the external device. Read/write bit; cleared by INIT.



DLV11-F XBUF Bit Assignments

Bit	Function
15–08	Not used. Not defined. Not necessarily read as 0's.
07–00	Transmitter Data Buffer. Holds the character to be transferred to the external device. If fewer than eight bits are used, the character must be loaded so that it is right-justified into the least significant bits.

M8043
DLV11-J SERIAL LINE UNIT

Amp		Bus Loads		Cables
5 V	+ 12 V	AC	DC	
1.0	0.25	1	1	BC21B-XX BC20N-XX (Heritage DLV11-KA) BC20M-XX

Standard Addresses

Configuration No. 1	Channel 0	Channel 1	Channel 2	Channel 3
RCSR	176500	176510	176520	176560
RBUF	176502	176512	176522	176562
XCSR	176504	176514	176524	176564
XBUF	176506	176516	176526	176566

Configuration No. 2

RCSR	176500	176510	176520	176530
RBUF	176502	176512	176522	176532
XCSR	176504	176514	176524	176534
XBUF	176506	176516	176526	176536

Standard Vectors

Configuration No. 1

Receiver	300	310	320	60
Transmitter	304	314	324	64

Configuration No. 2

Receiver	300	310	320	330
Transmitter	304	314	324	334

Diagnostic Programs

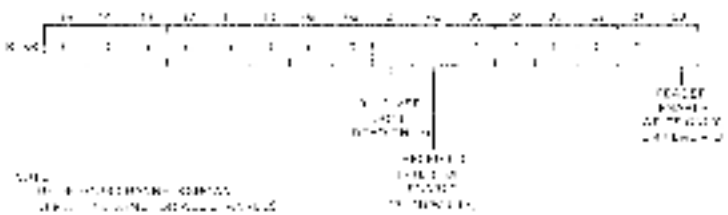
Refer to Addendum A

NOTE

This test requires that four H327C-A loopback plugs be inserted into the DLV11-J module in order for the diagnostic to run.

Related Documentation

DLV11-J User's Guide (EK-DLV1J-UG)
Field Maintenance Print Set (MP00586)
Microcomputer Interfaces Handbook (EB-20175-20)



RCSR Registers Bit Assignments

Word	Bit	Function
RCSR	8-15	Not used. On read — 0.
	7	Receiver Done – Set when an entire character has been received and is ready for input to the processor. This bit is automatically cleared when RBUF is read, when INIT is asserted (on power up or reset instruction), or when receiver enable bit is set. Read only. If receiver interrupt enable (bit 6) is set, the setting of receiver done starts an interrupt sequence.
	6	Receive Interrupt Enable – Set under program control when 1 is desired to allow a receiver interrupt sequence to occur when a character is ready for input to the processor (signified by receiver done being set). Cleared under program control or by INIT. Read/write.
	1-5	Not used. On read — 0.
	0	Reader Enable – Setting this bit advances the paper tape reader on an LT ASR terminal one character at a time and the setting of this bit clears receiver done (bit 7). Write only. The DLV11-KA 20 mA current loop option is required for operation of this bit.

RBUF Register Bit Assignments

Word	Bit	Function
RBUF	15	Channel Error Status – Logical OR of bits 14, 13, and 12. Read only.
	14	Overrun Error – When set, indicates that the receiving of the previously received character was not completed (RCVR done not cleared) prior to receiving a new character. The final character is "lost." Read only; cleared by INIT being asserted.

NOTE

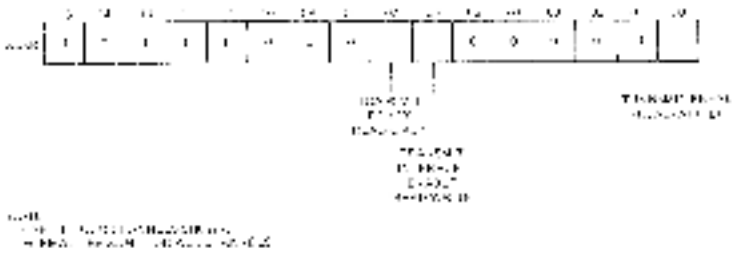
When back-to-back characters are received, one full character time is allowed from the instant when receiver done (bit 7) is set to the occurrence of an overrun error.

13	Framing Error – When set, indicates that the character read had no valid stop bit. This indicates that the currently received character and the next character are invalid. Read only; cleared by INIT.
12	Parity Error – When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no parity operation is configured for the channel. Read only.

NOTE

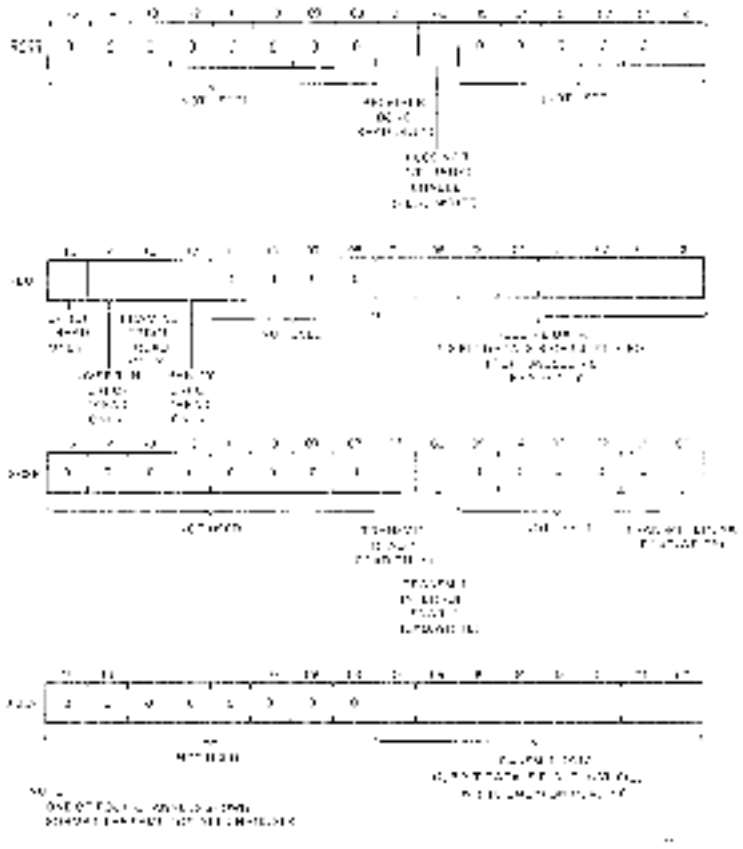
Error bits remain valid until the next character is received, at which time the error bits are updated.

8–11	Not used. On read = 0.
0–7	Data Bits – Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when seven data bits are enabled. Read only.



XCSR Registers Bit Assignments

Word	Bit	Function
XCSR	8–15	Not used. On read — 0
	7	Transmit Ready – Set when XBUF is empty and can accept another character for transmission. It is also set by INIT during the power-up sequence or during a reset instruction. If transmitter interrupt enable (bit 6) is set, the setting of transmit ready will start an interrupt sequence. Read only.
	6	Transmit Interrupt Enable – Set under program control when it is desired to generate a transmitter interrupt request (when transmitter is ready to accept a character for transmission). The bit is cleared under program control, during power up sequence, or reset instruction. Read/write.
	1–5	Not used. On read — 0.
	0	Transmit Break – Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt enable can still operate, allowing software timing of break. When not set, normal character transmission can occur. Read/write; cleared by INIT being asserted.

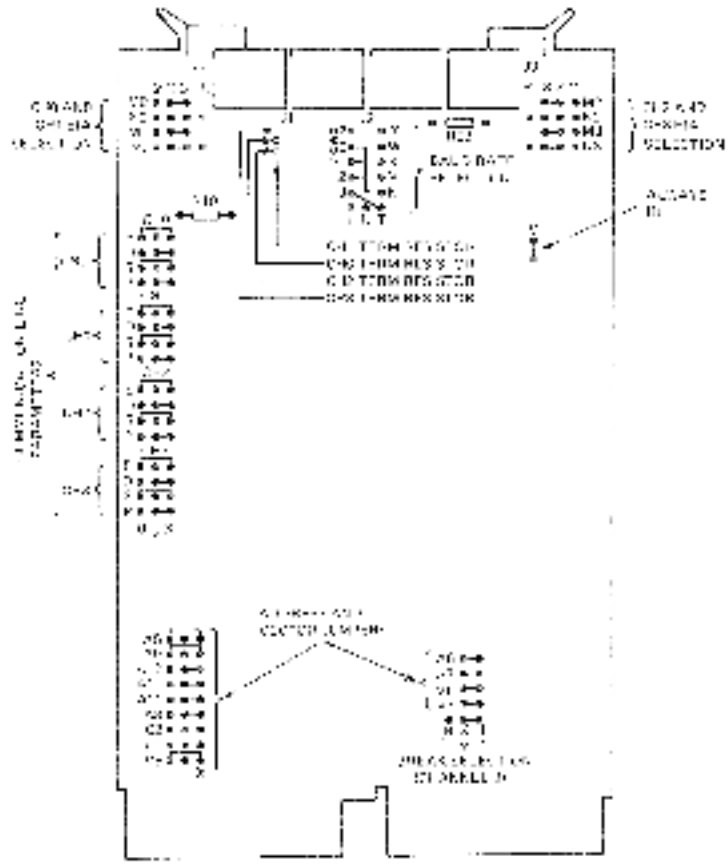


DLV11-J SLU Register Formats

XBUF Register Bit Assignments

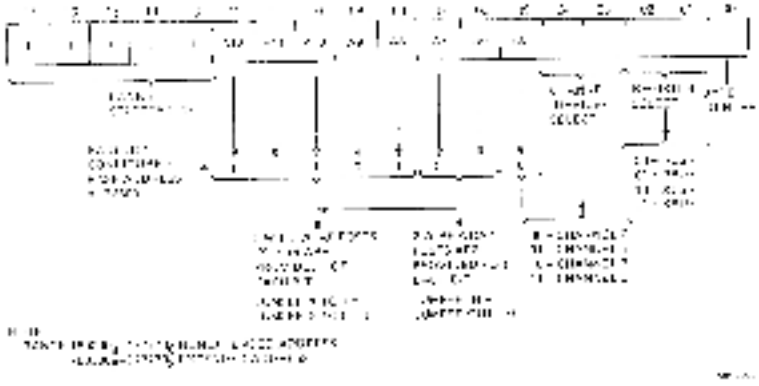
Word	Bit	Function
XBUF	8-15	Not used. On read = 0.
	0-7	Data bits - Contains seven or eight right-justified data bits loaded under program control for serial transmission. Write only.

Jumper Configurations



DLV11-J Component and Jumper Factory Configuration Summary

Address Selection



Device Register Address Format

It is possible to independently configure the last four addresses (channel 3) to the LSI-11 console device (addresses 777560–777566) when certain base addresses and console select jumpers* are installed. In this configuration, the preceding addresses (channels 0, 1, and 2) are not affected; they are normal offsets of the configured base device address as shown in the following table.

General Device Register Address Assignments (Without Console Selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA + 2	Channel 0 RBUF
BA + 4	Channel 0 XCSR
BA + 6	Channel 0 XBUF
BA + 10	Channel 1 RCSR
BA + 12	Channel 1 RBUF
BA + 14	Channel 1 XCSR
BA + 16	Channel 1 XBUF
BA + 20	Channel 2 RCSR
BA + 22	Channel 2 RBUF
BA + 24	Channel 2 XCSR
BA + 26	Channel 2 XBUF
BA + 30	Channel 3 RCSR
BA + 32	Channel 3 RBUF
BA + 34	Channel 3 XCSR
BA + 36	Channel 3 XBUF

*Console select jumpers G1 and G2 installed select channel 3 as console device.

General Device Register Address Assignments
(General Configuration With Console Selected)

Address	Device Register
Module Base Address (BA)	Channel 0 RCSR
BA — 2	Channel 0 RBUF
BA — 4	Channel 0 XCSR
BA — 6	Channel 0 XBUF
BA — 10	Channel 1 RCSR
BA — 12	Channel 1 RBUF
BA — 14	Channel 1 XCSR
BA — 16	Channel 1 XBUF
BA — 20	Channel 2 RCSR
BA — 22	Channel 2 RBUF
BA — 24	Channel 2 XCSR
BA — 26	Channel 2 XBUF
177560	Channel 3* RCSR
177562	Channel 3 RBUF
177564	Channel 3 XCSR
177566	Channel 3 XBUF

*Channel 3 is enabled as a console device.

Specific Device Register Address Assignments
(DLV11-J Configured With BA = 176500 and SV = 300
Without Console Selected)

Address	Register	Vector	Channel
176500	RCSR	300	Channel 0
176502	RBUF		
176504	XCSR	304	
176506	XBUF		
176510	RCSR	310	Channel 1
176512	RBUF		
176514	XCSR	314	
176516	XBUF		
176520	RCSR	320	Channel 2
176522	RBUF		
176524	XCSR	324	
176526	XBUF		
176530	RCSR	330	Channel 3
176532	RBUF		
176534	XCSR	334	
176536	XBUF		
177560	RCSR	60	Channel 4 Console Device
177562	RBUF		
177564	XCSR	64	
177566	XBUF		

NOTE
All addresses are in octal notation.

Vector Selection

When channel 3 is configured as the console device interface using console select jumpers C1 and C2, the interrupt vectors of the channel become 60 and 64. This is true regardless of the configured base vector of the module. It should be noted that the preceding channels (0, 1, and 2) are not affected and their vectors are normal offsets of the base vector configured, as shown in the following table.

General Vector Assignments
(Without Console Selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BA + 4	Channel 0 Transmitter
BA + 10	Channel 1 Receiver
BA + 14	Channel 1 Transmitter
BA + 20	Channel 2 Receiver
BA + 24	Channel 2 Transmitter
BA + 30	Channel 3 Receiver
BA + 34	Channel 3 Transmitter

General Vector Assignments
(With Console Selected)

Vector Offsets	Interrupt Vector
Module Base Vector (BV)	Channel 0 Receiver
BA + 4	Channel 0 Transmitter*
BA + 10	Channel 1 Receiver
BA + 14	Channel 1 Transmitter
BA + 20	Channel 2 Receiver*
BA + 24	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected

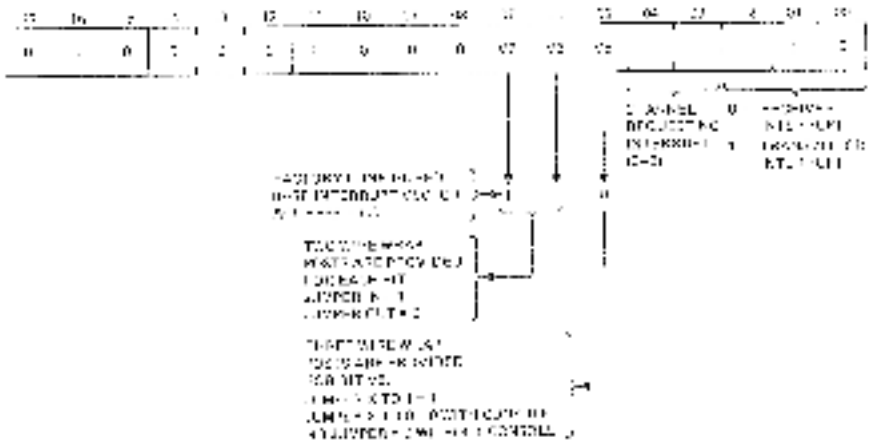
Specific Vector Assignments
(DLV11-J Configured With BV — 300
Without Console Selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
330	Channel 3 Receiver
334	Channel 3 Transmitter

Specific Vector Assignments
(Factory-Configured With BV — 300
With Console Selected)

Octal Vector	Interrupt Vector
300	Channel 0 Receiver
304	Channel 0 Transmitter
310	Channel 1 Receiver
314	Channel 1 Transmitter
320	Channel 2 Receiver
324	Channel 2 Transmitter
60	Channel 3 Receiver*
64	Channel 3 Transmitter*

*Console selected



Console device jumpers are used to select channels on the console interface. These jumpers (C1 and C2) will affect baudrate and vector selection.

Summary of Console Selection Jumper Configurations

Label	Console Selected	Console Not Selected
C1	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.
C2	Install jumper from wirewrap pins X to 1.	Install jumper from wirewrap pins X to 0.

Configuring Character Word Formats

Each DLV11-J SLU channel can be individually configured for number of data bits (7 or 8), even, odd, or no parity, 1 or 2 stop bits, and baud rate (described in the next section). A summary of possible character format jumper configurations is shown below.

Summary of Character Format Jumper Configurations

Label	UART Parameter	X to 0	X to 1	Comments
D	Number of data bits	7 bits	8 bits	LSB is transmitted first
S	Number of stop bits	1 bit	2 bits	
P	Parity inhibit	Parity generation and detection enabled	Parity generation and detection disabled	
E	Even parity enable	Odd parity enabled	Even parity enabled	Requires P jumper connected from X to 0

NOTE

E jumper must be connected to either 0 or 1, even if the parity bit is disabled. Two stop bits are generally used only with Teletype terminals.

CAUTION

To prevent hardware damage within the channel, the E jumper must ALWAYS be installed. This is true regardless of the configuration of the P (parity) jumper.

Baud Rate Selection

NOTE

A 110 baud rate clock generator circuit is contained on the optional DLV11-KA 20 mA option. When 110 baud operation is desired, do not connect the baud rate jumper on the DLV11-J module for that particular channel. The 110 baud rate will be supplied by the DLV11-KA option through the interface connector.

Configure baud rates (except 110 baud) by connecting a jumper from the appropriate baud rate generator output wirewrap pin to the baud rate clock input pin (labeled C-J). One jumper is required for each channel. Baud rate generator outputs are identified below.

Baud Rate Generator Outputs

Wirewrap Pin Label	Baud Rate (Bit/S)
U	150
T	300
V	600
W	1200
Y	2400
L	4800
M	9600
K	9600
Z	38400

NOTE

If more than one channel requires the same baud rate, the wirewrap jumpers may be daisy-chained.

Channel 3 Break Response

Channel 3 (normally used as the console device) can respond to a break condition on the receive line such as when an operator presses the BREAK key on the associated terminal. The BREAK key transmits a continuous space signal which is detected by the DLV11-J circuits as a framing error. If no operation is desired, do not connect jumpers to the B, X, and H wirewrap pins.

Channel 3 Break Operation Jumper Summary

Break Response Operation	Jumper Connection
Halt	Install jumper between wirewrap pins X and B.
Halt	Install jumper between wirewrap pins X and H.
No response	No jumper installed

Summary of Serial Channel Signal Level Compatibility Configurations

Serial Channel Signal Level

Serial Channel Signal Level Modifiers	EIA RS-422	EIA RS-232C and RS-423	20 mA Current Loop (Required DLV11-KA Option)
M0–3 jumpers	Connect wire-wrap pins X and 2	Connect wire-wrap pins X and 3	Connect wirewrap pins X and 3
N0–3 jumpers	Connect wire-wrap pins X and 2.	Connect wire-wrap pins X and 3.	Connect wirewrap pins X and R for program-controlled paper tape reader functionality
Terminator resistor (one per channel)	Install a 100 Ω, 1/4 W, non-wire-wound, fusible resistor.	No resistor installed	No resistor installed.
Wave shaping resistor pack per channel pair (channel pairs 0 and 1, 2 and 3).	Not required	Install resistor (see next table). 1/4 W non-wirewound.	Install 2K Ω non-wirewound resistor.

EIA RS-422 – To configure an SLU channel for EIA RS-422 signal levels, connect the M(M0–M3) and N(N0–N3) jumper wirewrap pin X of the desired channel to the respective wirewrap pin 2. Install (solder) a 100 ohm, 1/4 W fusible resistor (non-wirewound) into the termination resistor mounting pads for the channel being configured. The resistor must be removed for any configuration other than EIA RS-422.

EIA RS-423 and RS-232C – To configure an SLU channel to be compatible with both the EIA RS-423 and RS-232C (which on the DLV11-J are met simultaneously), connect each M(M0–M3) and N(N0–N3) jumper X wirewrap pin of the desired channel to the respective wirewrap pin 3.

Slew Rates The signal rise and fall time may be controlled on EIA RS-423 and RS-232C SLU channel configurations by installing (soldering) an appropriate value of non-wirewound, 1/4 W resistor into the wave-shaping resistor pads provided (R10 and/or R20). An appropriate resistor value can be selected by referring to the following table. The value of resistor R10 determines the slew rate of both channels 0 and 1 which are simultaneously set to the same value. Similarly, R20 controls the slew rate of both channels 2 and 3.

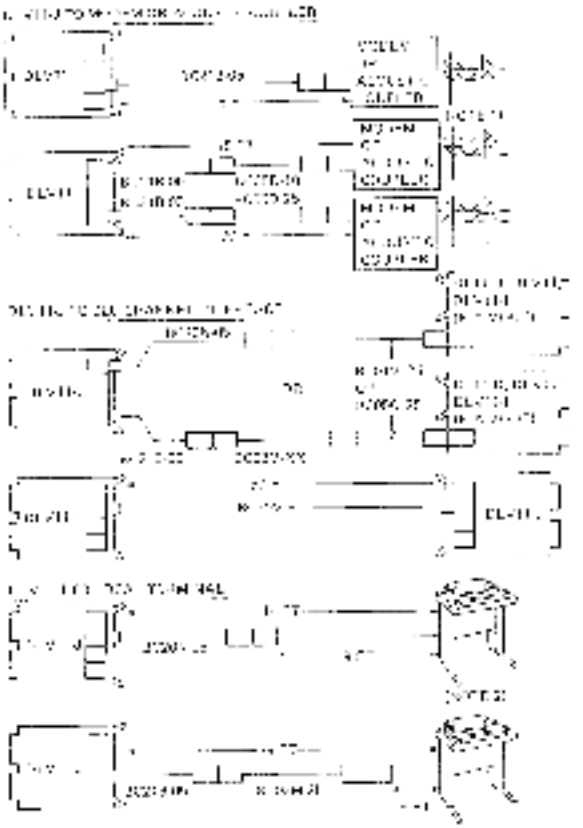
EIA RS-423 and RS-232C Wave-Shaping Resistor Values

Baud Rate	Wave-Shaping Resistor
38.4K	22 kΩ
19.2K	51 kΩ
9.6K	120 kΩ
4.8K	200 kΩ
2.4K	430 kΩ
1.2K	820 kΩ
600.0	1 MΩ
300.0	1 MΩ
150.0	1 MΩ
110.0	See Note.

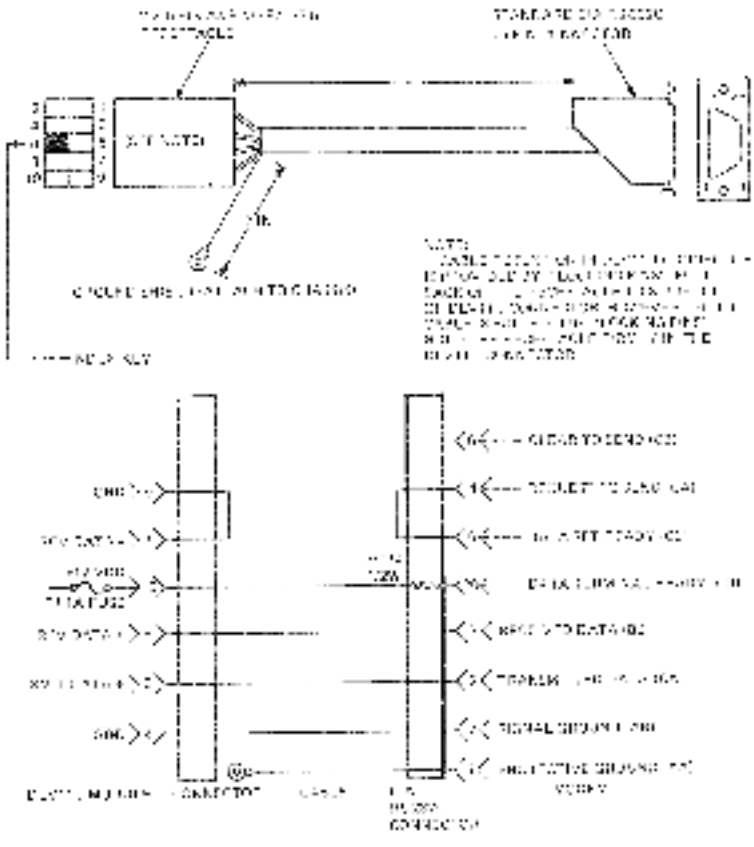
NOTE
Determined by other channel of the two-channel pair.

20 mA Current Loop – To configure an SLU channel for 20 mA current loop operation, connect the M(MC-M9) jumper pin X to pin S for the desired channel. If the 20 mA terminal contains a paper tape reader that can be program-controlled (such as a DEC-modified 11 KS Teletype or Teletype ASR-33 with LT33 MR modification kit), connect wirewrap jumper N(NO-N2) pin X to the respective pin R.

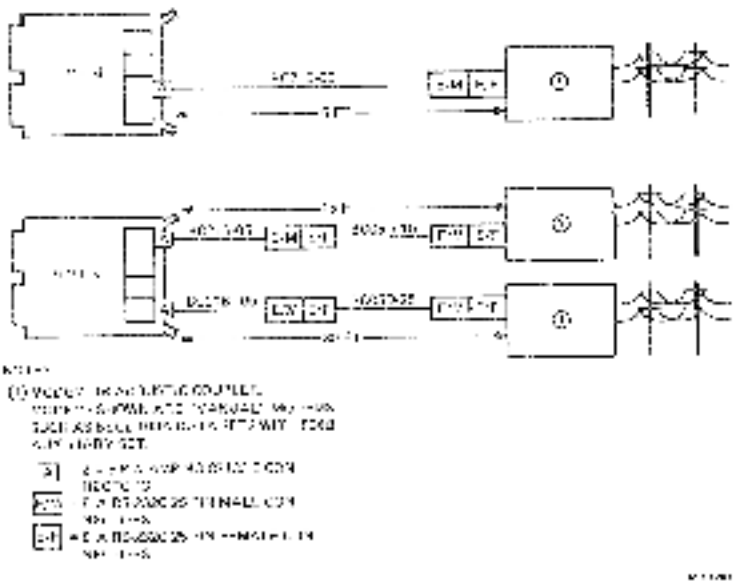
When the DLV11-KA 20 mA current loop option is connected to the channel interface connector, operating power for the option circuits is supplied by the DLV11-J. To configure a channel for 110 baud operation, enable the 110 baud rate clock on the DLV11-KA option and remove the baud rate selector jumper for the channel on the DLV11-J module. The clock needed by the DLV11-J is automatically supplied through the serial line connector cable.



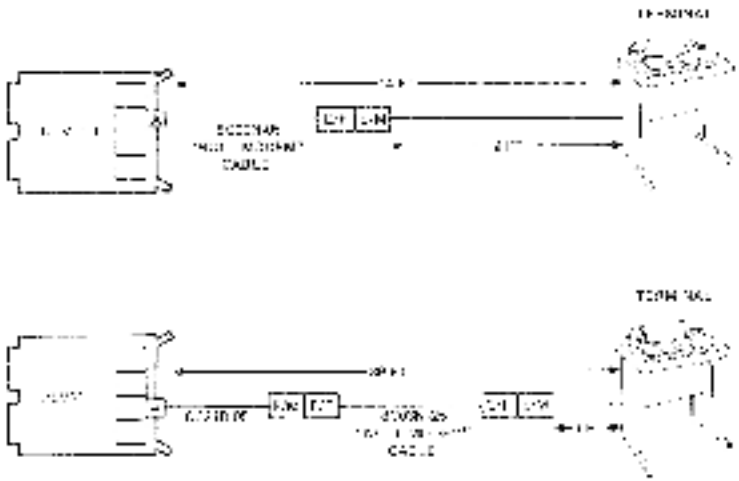
DLV11-J Cabling Summary



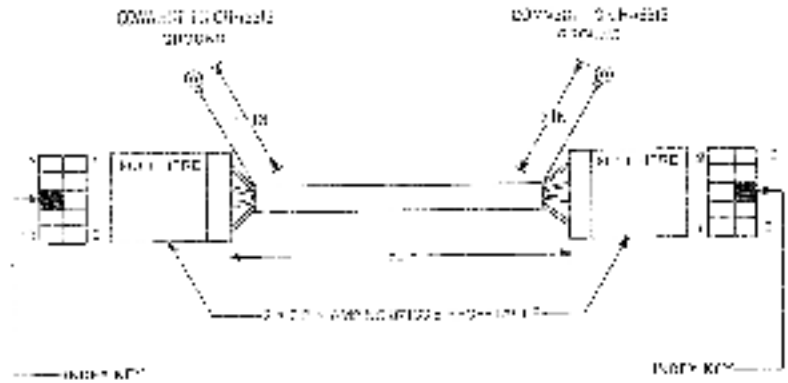
BC21S-03 Peripheral Device Cable



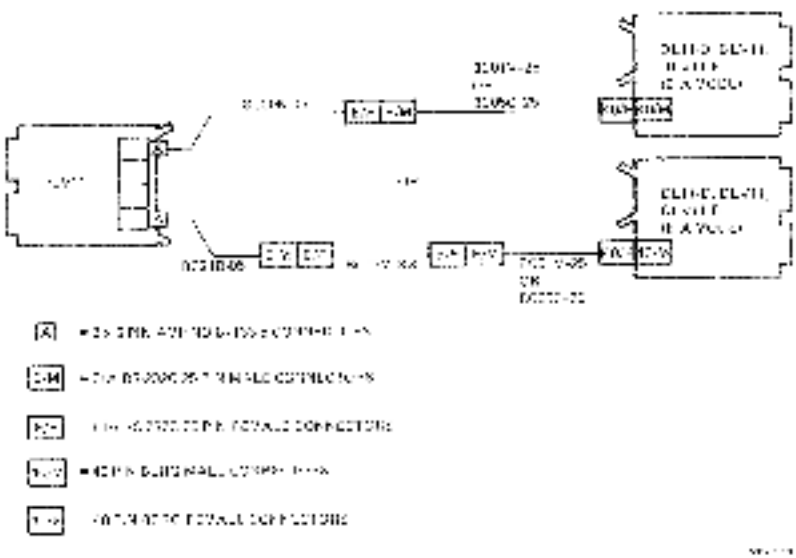
DLV11-J to Modem or Acoustic Coupler



Local Terminal Cabling



BC20M-50 DLV11-J to DLV11-J Cable



DLV11-J to SLU Modem Cabling

DLV11-KA EIA TO 20 MA CONTROLLER

Amps		Bus Loads		Cables
1.5	1.2	AC	DC	BC22A (to EIA
0	0	N/A	N/A	H3000-XX 20 mA

4 1.2 Vdc 0.275 max. (supplied by EIA SLU interface module).

Standard Addresses and Vectors, Diagnostic Programs

Not 6

Related Documentation

DLV11-KA EIA to 20 mA Installation Guide (EK-DLVKA-IN)
DLV11-KA Maintenance Print Set (MP00694)
Microcomputer Interfaces Handbook (EB-20175-20)

CONFIGURATION

General

The DLV11-K requires the configuration of 11 jumper wire connections and 1 capacitor connection. The configurations and functions of these jumpers are shown in the following table.

DLV11-KB Jumper Configurations

Function	Jumper In	Jumper Out
Passive 20 mA Receiver	W7, W9	W8, W6, W10
Active 20 mA Receiver*	W6, W8, W10	W7, W9
Passive 20 mA Transmitter	W2, W4	W1, W3, W5
Active 20 mA Transmitter*	W1, W3, W5	W2, W4
110 Baud Enabled*	W11	
110 Baud Disabled		W11
Noise Suppression	See following Note	See following Note.

*Factory configuration

NOTE

For use with an ASR-33 Teletype®, insert a 0.047 μF axial ceramic capacitor (DEC P/N 10-12784-00) in the location designated C. This capacitor is inserted for the factory configuration. For any other terminal there is nothing inserted in this location.

For proper operation of Teletype ASR-33 with DEC-supplied paper tape software, the SLU should be configured for eight data bits, two stop bits, and no parity. The Teletype models can be LT33-DC, LT33-DD, LT33-DE, or an ASR-33 Teletype with the LT33-MB modification kit installed.

DLV11-KB Jumper Locations

Installation Requirements

The DLV11-KA option can be installed in a system that requires conversion from EIA RS-232 standard to a 20 mA current loop. The DLV11-KA option consists of a DLV11-KB converter box and a BC21A-xx interface cable as shown in the preceding illustration. The BC21A-03 is a 0.9 m (3 ft) cable that interconnects the DLV11-KB to an EIA SLU interface module. The smaller connector (2 × 5 pin) connects to the SLU module and the larger connector (2 × 7 pin) connects to the DLV11-KB box. Keying is provided on both connectors, and cable retention is provided by "locking pins" on the SLU connector. To disengage, pull back on the connector and the connector will slide free. However, if the cable is pulled, the locking pins will hold the connector firmly in place. A BC05F-xx cable can be used to connect the DLV11-KB converter box to DEC 20 mA terminals, including the DEC-modified ASR-33 Teletype.

Cabling

Cables other than the DEC BC05F-XX can be used when installing the DLV11-KA option. However, any other cable must conform to the following parameters to meet the baud rate versus cable length specification.

1. Resistance – NMT 30 Ω/305 m (1000 ft) (NLT 22 AWG)
2. Capacitance to ground – NMT 50 pF/ft
3. Capacitance wire-to-wire – NMT 35 pF/ft

The BC05F-XX cable meets the above requirements. If the user desires to use shielded cable, the shield should be grounded to the chassis at the entry point and not to the DLV11-KA converter box. The user can fabricate custom cables for the 20 mA interface by using DEC connector, PN 12-09340-01 (AMP PN 1-480426-0), and pins PN 12-09575-03 (AMP PN 66506-4).

Baud Rate

The DLV11-KA option will operate up to a maximum of 9600 baud, provided that the interface module can accommodate these rates. However, the maximum operational baud rate is also limited by the length of cable. Maximum recommended cable lengths for the specific baud rates are given in the following table. These recommendations are conservative and will yield satisfactory operation for almost all applications. These guidelines may be exceeded, but this should only be done after reviewing the DLV11-KA specifications, the severity of the operating environment, and the error rate that can be tolerated.

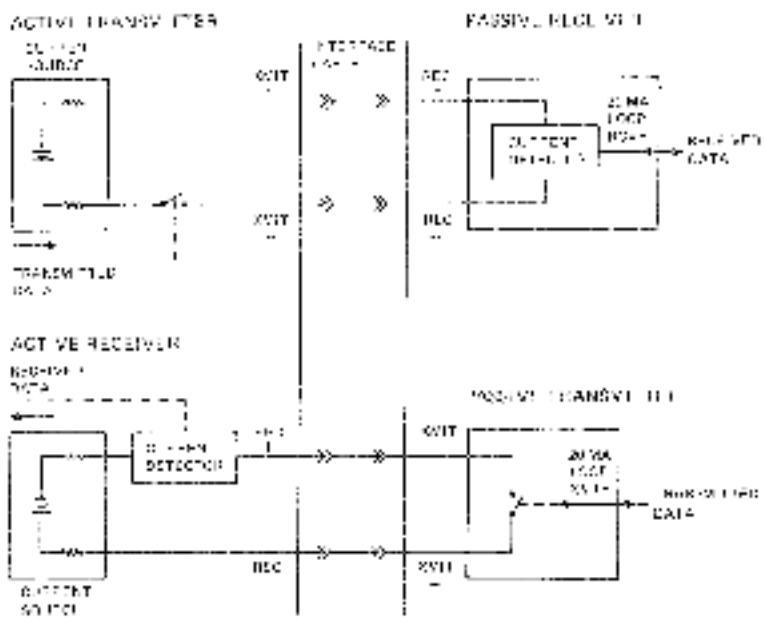
Baud Rate vs Cable Length

Baud Rate	Max. Cable Length
9600	30 m (100 ft)
4800	76 m (250 ft)
2400	152 m (500 ft)
1200	305 m (1000 ft)
600	610 m (2000 ft)
300	1220 m (4000 ft)
110	1220 m (4000 ft)

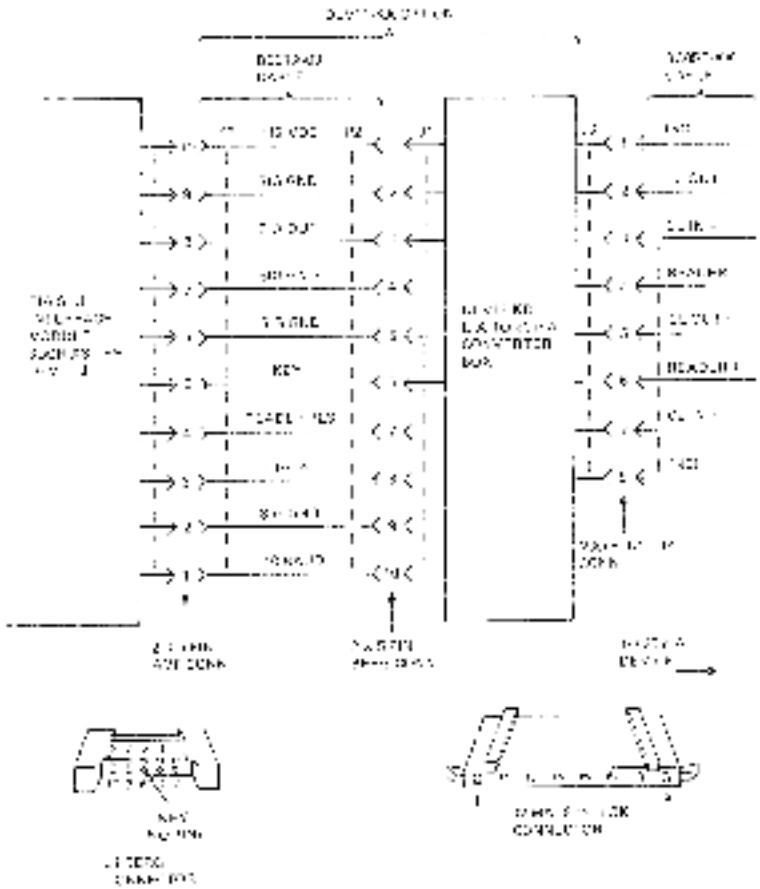
Terminal Recommendations

DIGITAL Terminals or SLUs	Active DLV11-KA Max. Cable Length (22 GA)	Max. Baud Rate	Passive DLV11-KA Max. Cable Length (22 GA)	Max. Baud Rate
DLV11	1220 m (4000 ft)	*	**	*
DLV11-J	1220 m (4000 ft)	*	**	*
DLV11-KA	1220 m (4000 ft)	9600	1220 m (4000 ft)	9600
MSRH	1220 m (4000 ft)	9600	**	9600
LA36	457 m (1500 ft)	300	457 m (1500 ft)	300
VT52	1220 m (4000 ft)	9600	**	9600
LA1600	1220 m (4000 ft)	*	NA	NA
LA120	1220 m (4000 ft)	*	671 m (2200 ft)	*
VT100	1220 m (4000 ft)	9600	**	9600
LA120	1220 m (4000 ft)	9600	**	9600
Televideo ASR-33	305 m (1000 ft)	110	NA	NA

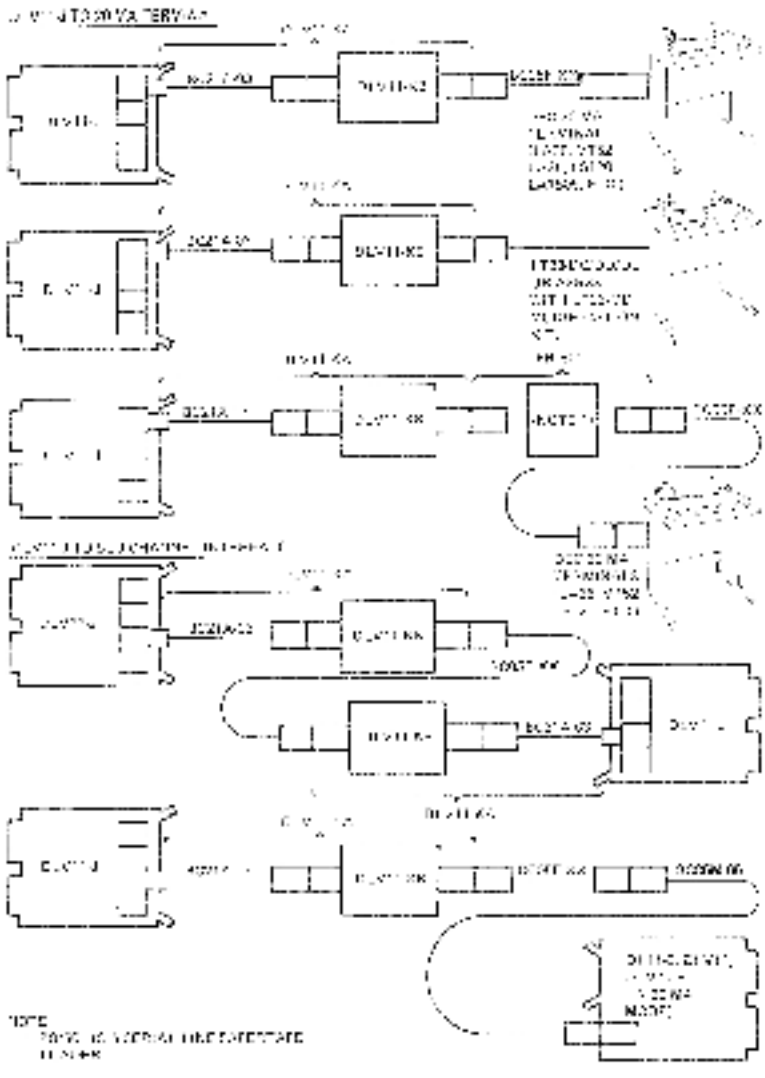
* Operation at 9600 baud only recommended for benign environments.
** Operation with more than 6 m (20 ft) of cable is not recommended



Standard Current Loop Interface



DLV11-KA Typical Installation



Typical Installation

DMV11 SYNCHRONOUS CONTROLLER

DMV11 OPTIONS

DMV11 Kits

Option	Interface	Line Speed (DMV11 Limitations)
DMV11-AA	EIA RS-232-C EIA RS-423-A	Up to 19.2K bits/s Up to 56K bits/s
DMV11-AB	CCITT V.35	Up to 56K bits/s
DMV11-AC	Integral modem	56K bits/s only

The DMV11-AA consists of:

1. An M8053-MA microcontroller/line unit
2. An H3254 (V.35 or integral modem) module test connector
3. An H3255 (RS-423-A/232-C) module test connector
4. A BC55H cable
5. An H325 and H3251 cable turnaround test connector.

The DMV11-AB consists of:

1. An M8053-MA microcontroller/line unit
2. An H3254 (V.35 or integral modem) module test connector
3. An H3255 (RS-423-A/232-C) module test connector
4. A BC05Z-25 cable
5. An H3250 and H3251 cable turnaround test connector.

The DMV11-AC consists of:

1. An M8064-MA microcontroller/line unit
2. An H3254 (V.35 or integral modem) module test connector
3. A BC05F cable
4. H3257 and H3258 terminators

DMV11/M8053,54

Power Requirements

Option	Voltage
DMV11-AA, AR	+5 V @ 3.1 A −12 V @ 0.280 A
DMV11-AC	+5 V @ 3.35 A −12 V @ 0.260 A

Bus Loads

	AC	DC
DMV11-AA	2	1
DMV11-AB	2	1
DMV11-AC	2	1

Address Assignments

Registers	Byte Address
BSEL0	16XXX0
BSEL1	16XXX1
BSEL2	16XXX2
BSEL3	16XXX3
BSEL4	16XXX4
BSEL5	16XXX5
BSEL6	16XXX6
BSEL7	16XXX7
BSEL10	76XX10*
BSEL11*	76XX11*

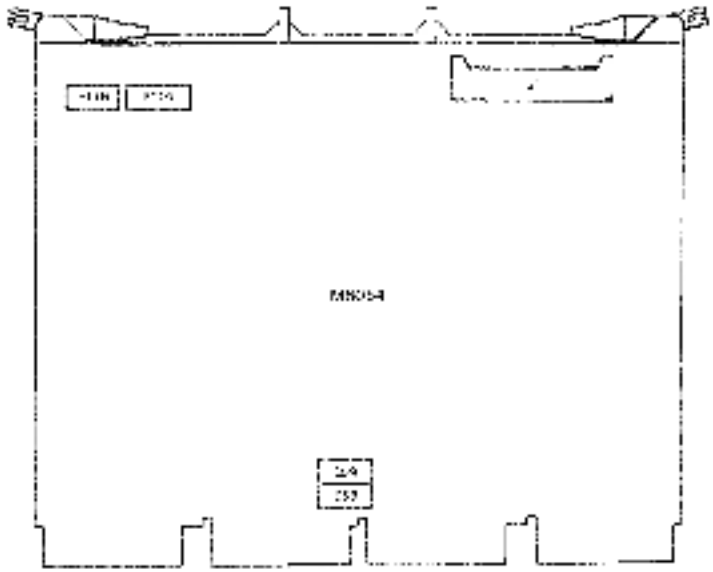
*22-bit addressing only

Diagnostics

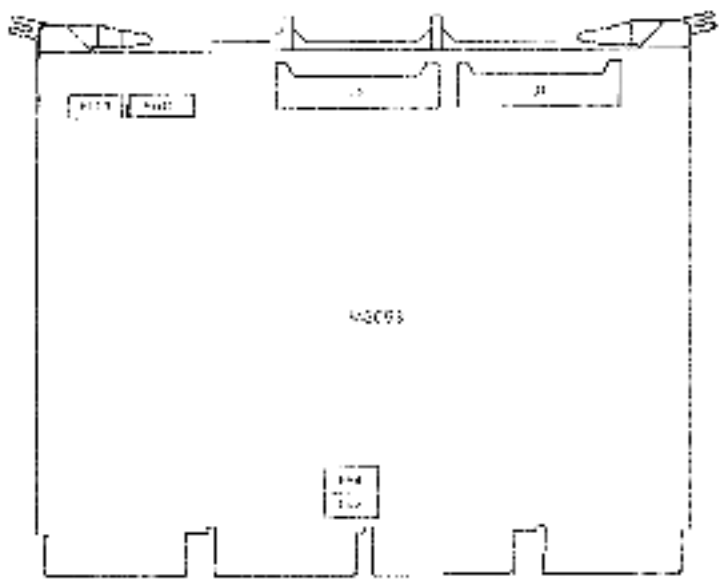
Refer to Appendix B.

Related Documentation

DMV11 Synchronous Controller User's Guide (EK-DMV11-UG)
Field Maintenance Print Set (MP-00942)



M8064 Switch Locations



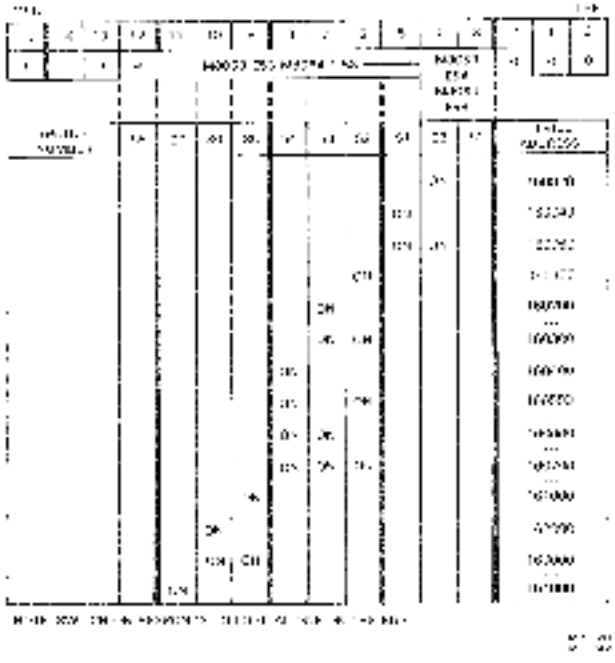
M8063 Switch Locations

CONFIGURATION

The DMV11 modules are configured by selecting switch positions on the switch packs. The user selects the address of the control status register, the interrupt vector address, DDCMP address register, and other general features.

Control Status Register

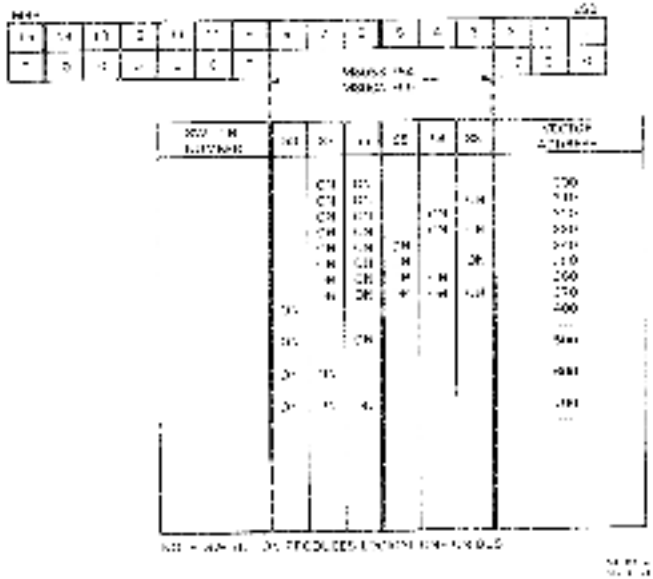
The address selected for the control status register (CSR) is the base line for all the module registers. The module has four 16-bit word registers or eight 8-bit byte registers when used in a 16 bit system. When used in a 22-bit system, an additional 16-bit register or two 8-bit byte registers are used. The M8053 module uses switch packs E50 and E54 for address selection and the M8054 module uses switch packs E55 and E49 for address selection. The switch positions required to select an address are as follows:



DMV11 Device Address Selection

Vector Address

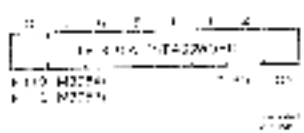
The vector address for the DMV11 is selected by using switch pack E54 on the M8053 module and switch pack E50 on the M8064 module. The switch requirements are as follows:



Vector Address Selection

DDCMP Address Register

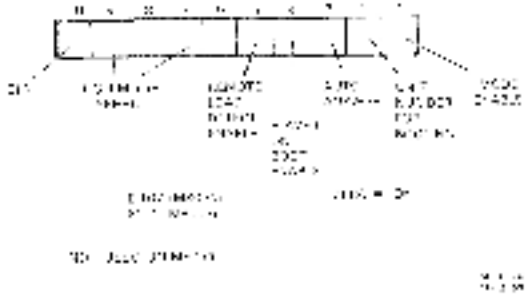
The DDCMP address register is set to represent the digital data communications message protocol data link password or tributary. The M8053 module uses switch pack E115 and the M8064 module uses switch pack E119. A logical one is selected by the switch in the off position and a logical zero is selected by the switch in the on position. The password bits selected by the switches are as follows:



DDCMP Address Register

General

The general features of the DMV11 are selected by switch pack E10? on the M8028 module and E10? on the M8054 module. A logical one is selected by the switch in the off position, and a logical zero is selected by the switch in the on position. The selectable features are as follows:



DMV11 Selectable Features

Mode of Operation – The operation mode is enabled when switch 1 is off to select a logical one and the feature is disabled by setting the switch on. The mode is selected by switches 6, 7, and 8 as follows.

Operating Modes

6	7	8	Switch Setting for the Mode of Operation
ON	ON	ON	HDX PT to PT DMC compatible
ON	ON	OFF	FDX PT to PT DMC compatible
ON	OFF	ON	HDX point to point
ON	OFF	OFF	FDX point to point
OFF	ON	ON	HDX control station
OFF	ON	OFF	FDX control station
OFF	OFF	ON	HDX tributary station
OFF	OFF	OFF	FDX tributary station

Unit Number – The unit number, either zero or one, must be selected for the host CPU to identify specific DMV11 for booting. A zero indicates the switch is on, and a one indicates the switch is off.

Auto Answer – The auto is selected by a one being selected and the switch is off.

Power On Boot Enable – To enable the power on boot feature at a remote station this switch must be set to a one; the switch is off.

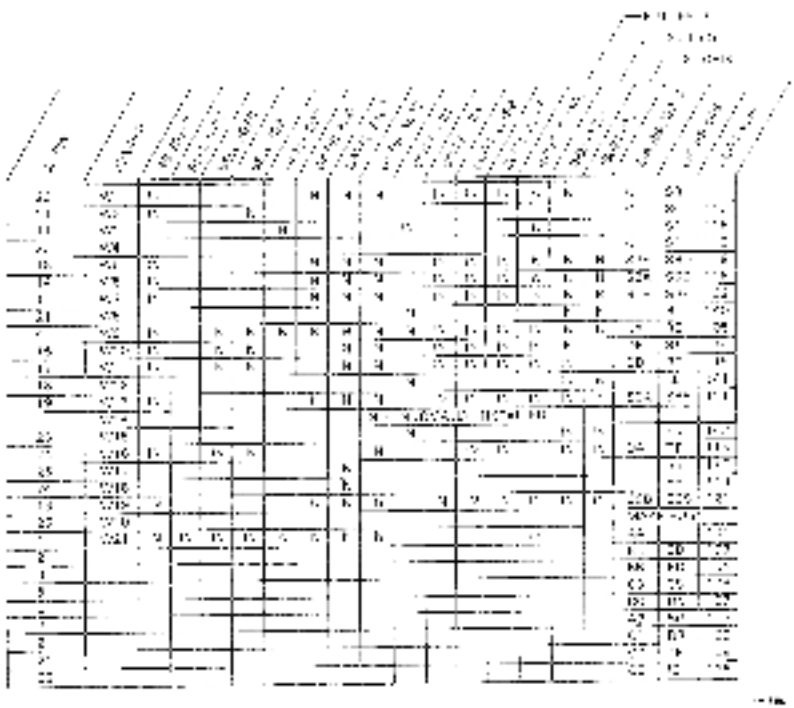
Remote Load Detect Enable – To enable the remote load detect feature of a remote station, this switch must be set to a one; the switch is off.

High Speed Switch – The high speed switch is enabled for integral modem or when running at/at 19.2K baud rate. The feature is enabled by being set to a one; the switch is off.

EIA – The EIA feature is only used on the M8053 module. The EIA mode is selected when the switch is off and the V.35 mode is selected when the switch is on.

Cables

The modules use a variety of cables dependent on the interface requirements. These are described in the following tables and the figures of cables and installation.



Module Option Jumper Functions

Cable Description

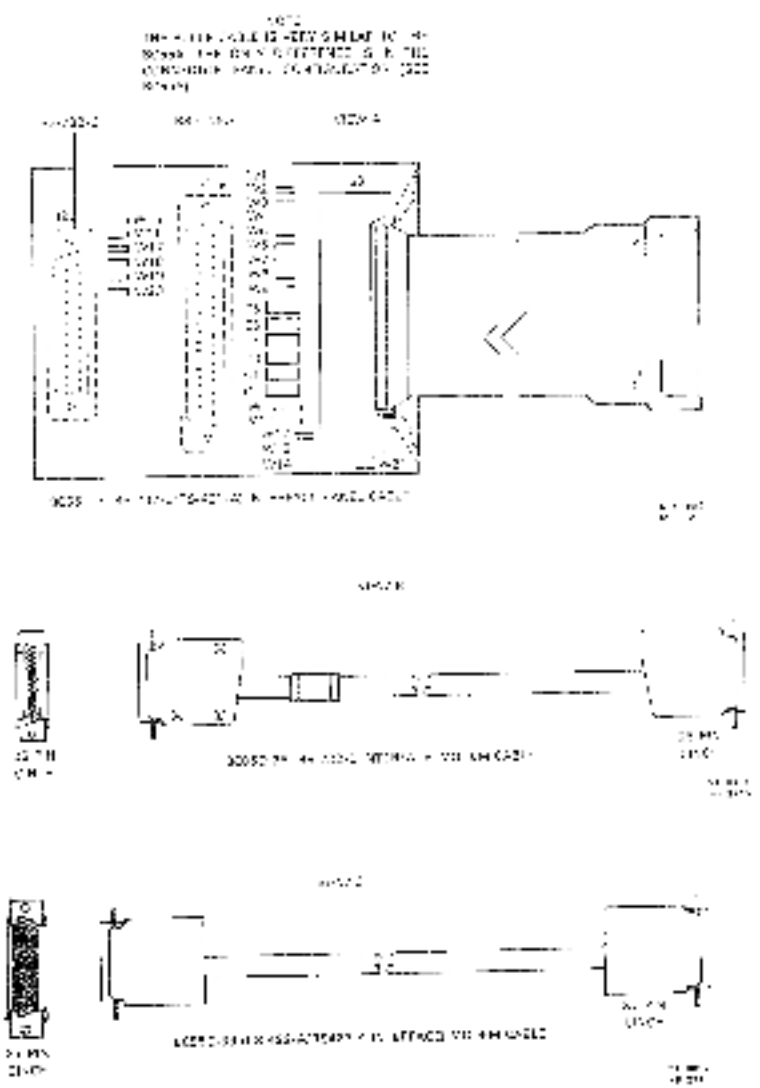
Interface	Cable	Module Connector	Test Connector	Description
RS-232-C	BC55R (DMV11 Cable Drawings View A)	J2 (M8053)	H325	A cable with a 40-pin Berg connector at one end. The other end has a panel that includes two different size connectors, J1 and J2. Connector J2 is used for RS-232-C to connect to the modem with external cable BC05D-25. The panel is mounted to a rear-mounted bulkhead to ensure proper grounding and ease of access to external cable connections.
	BC05D-25 (DMV11 Cable Drawings View B)		H325	A 7.6 m (25 feet) external cable that connects to J2 of the BC55C panel and an RS-232-C modem.
RS-422-A	BC55R-03 (DMV11 Cable Drawings View A)	J1 (M8053)	H325	Same cable as used for RS-232-C except that panel connector J1 is used with external cable BC06D-03 for connection to the modem. The panel is mounted to a rear-mounted bulkhead to ensure proper grounding and ease of access for external cable connections.

Cable Description (Cont)

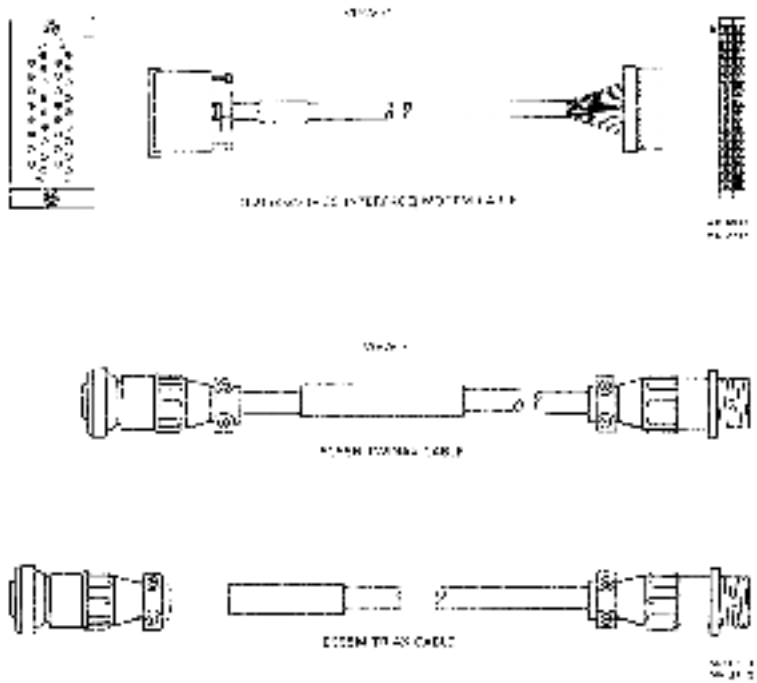
Interface	Cable	Module Connector	Test Connector	Description
	BC55D-33 (DMV11 Cable Drawings View D)		H3257	A 10.1 m (33 feet) cable that connects to J1 of the BC55H panel and an RS-449 modem
V.35	BC05Z-25 (DMV11 Cable Drawings View D)	J1 (M8053)	H3250	A 7.6 m (25 feet) modem cable with a 48-pin Berg connector at one end that connects to J1 of the M8053. A 34-pin Data Phone Digital Service (DDS) connector is installed at the other end and connects to the modem.
Integral Modem	BC55F (DMV11 Cable Drawings View D)	J1 (M8064)	Panel switch to NEXposition	A 0.9m (3 foot) cable with a 40 pin Berg connector at one end that plugs into J1 of the M8064. The panel assembly is installed at the rear mounted bulkhead for ease of external connections and to ensure proper grounding.
				Appropriate terminator connectors H3447 or H3253 must be used. See DMV Cable Drawings View F.

Cable Description (Cont)

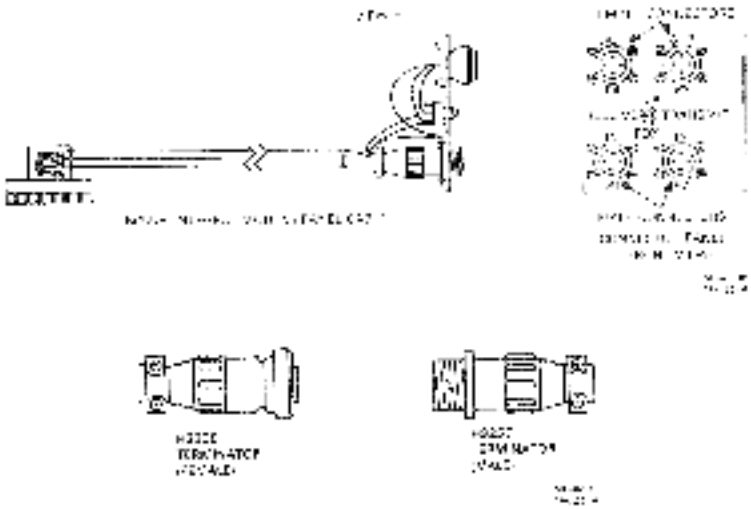
Interface	Cable	Module Connector	Test Connector	Description
Integral Modem	BC06N-30 (DMV11 Cable Drawings Vol E)	Local link BC05R panel	None	A 30.5 m (99 foot) external twinax cable used to interconnect a DMP11 or a DMV11 to a DMV11 system in a selected data rate of 56K bits/s.
	BC55M-30 (DMV11 Cable Drawings Vol E)	None	None	A 30.5 m (99 foot) external twinax cable used for the same purpose as the BC06N, but for data rates above 56K bits/s. The DMV11-AC supports data rates of 56K bits/s.



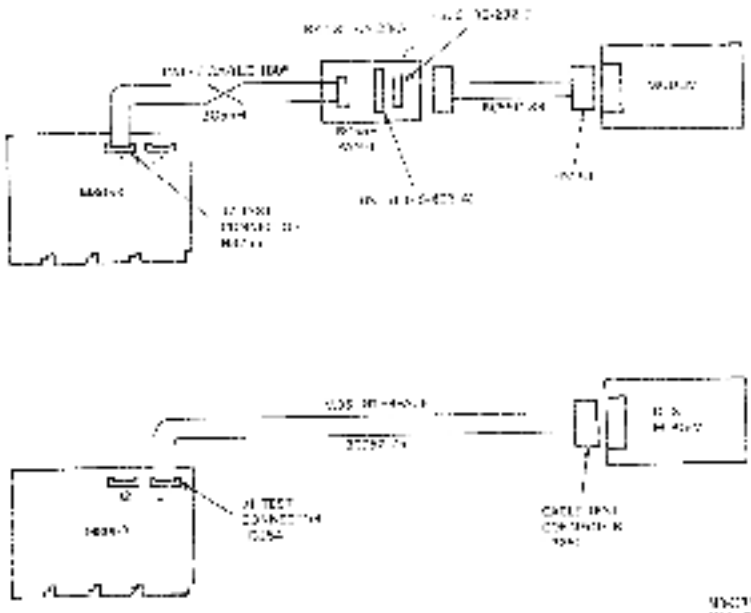
DMV11 Cable Drawings (Sheet 1 of 3)



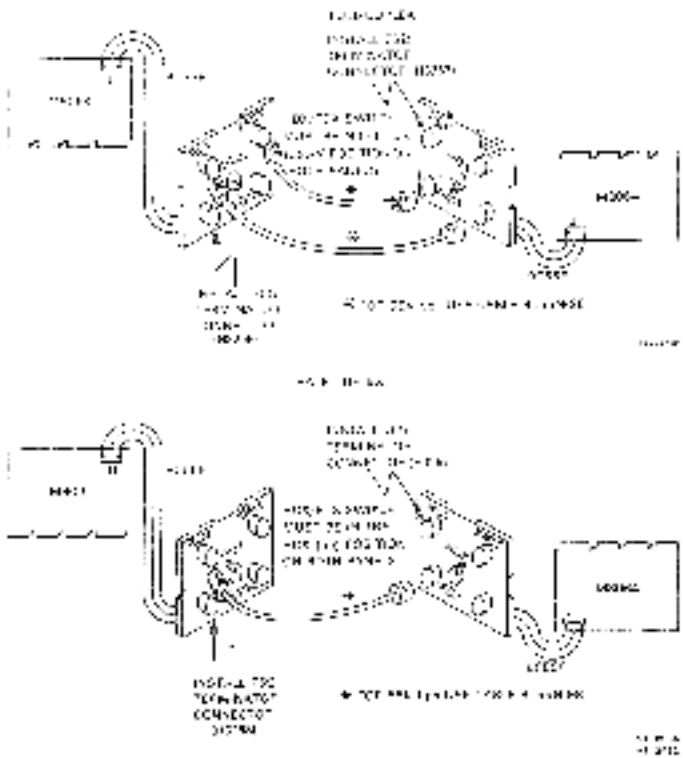
DMV11 Cable Drawings (Sheet 2 of 3)



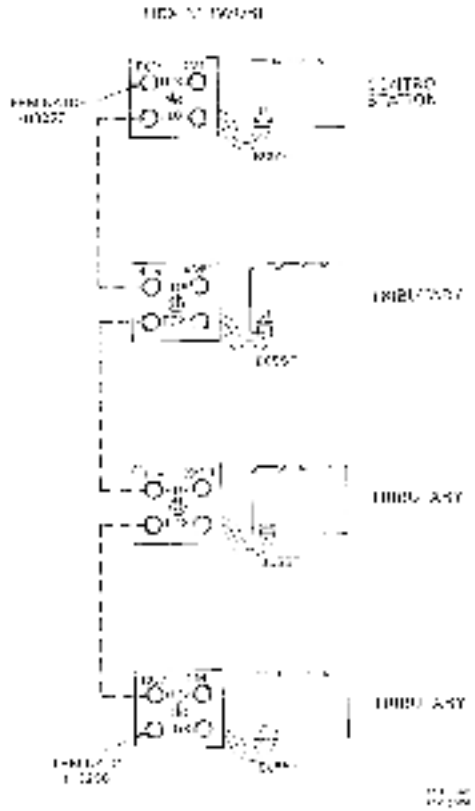
DMV11 Cable Drawings (Sheet 3 of 3)



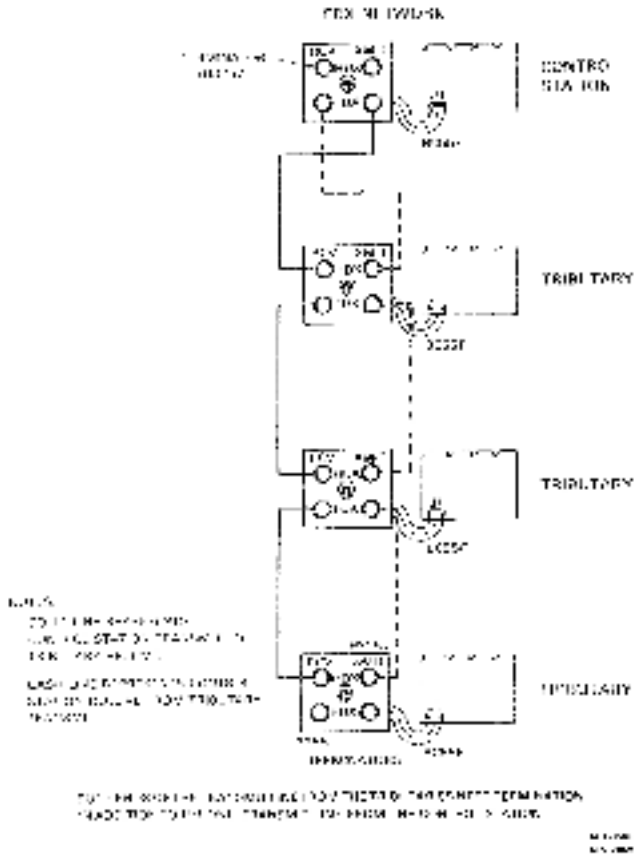
DMV11 Remote System Cabling Diagram



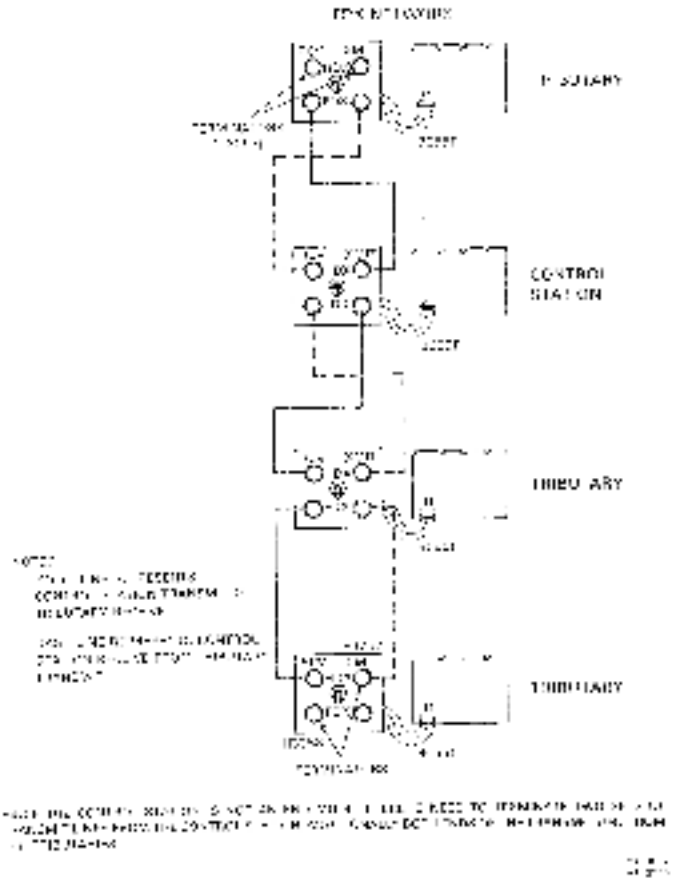
DMV11 to DMV11 Integral (Local) Modem Cabling Diagram
(Point-to-Point)



Half Duplex Multipoint Network (Control Station Error Node)



Full-Duplex Multipoint Network (Control Station End Node)



Full-Duplex Multipoint Network (Control Station Is Not Node)

CSR BITS

The module has eight 8-bit bidirectional registers for 16-bit address systems and ten 8-bit byte registers for 22-bit address systems. Registers BSEL0, BSEL2, and BSEL3 comprise the fixed format portion. BSEL1, BSEL5, BSEL6, and BSEL7 registers comprise the user program command and response portions. BSEL4 register is the control and maintenance command portion. The registers are as follows.

Fixed and Variable Formats

BSEL0 Bit Functions

Bit	Name	Description
00	Interrupt enable in (IEI)	When set, this bit enables the DMV11, upon asserting RDI (bit 04 of BSEL 0), to generate an interrupt to vector address XX0.
01-03	Reserved	
04	Interrupt enable out (IEO)	When set, this bit enables the DMV11, upon asserting RDO (bit 07 of BSEL 0), to generate an interrupt to vector address XX4.
05-06	Reserved	
07	Request in (RQI)	This bit is set by the user program to request access to the data port. It is cleared by the user program when the data port has been loaded, or when the port is no longer required for input anymore. The user program may leave RQI set if successive requests for the data port are pending.

CSEL1 Bit Functions

Bit	Name	Description
08	Maintenance request	When set along with master clear (bit 14 of CSR 4), this bit causes the DMV11 to enter the maintenance code section of the microcode.
09 10	Reserved	
11	Diagnostic mode	When set, this bit allows diagnostic programs to change the mode of operation of the DMV11 using the mode definition command to override the mode switches.
12	Reserved	
13	Invoke P/MOP boot	Invoke primary MOP mode. When set to one, this bit causes the DMV11 at this multipoint station to request that the control station initiate the primary MOP (maintenance operation protocol) boot procedure. In point-to-point networks, a DMV11 having this bit set requests the other station to initiate the primary MOP boot procedure.

NOTE

The master clear bit (bit 14) must also be asserted to use invoke P/MOP.

14	Master clear	When set, this bit initializes the DMV11. The clock is enabled and the RUN bit option is set. Master clear is self clearing.
15	Run	This bit controls running of the microprocessor. It is set by bus initialization or master clear. When run is cleared the microprocessor halts.

BSEL2 Bit Functions

Bit	Name	Description
00 02	Control/response code	These bits define the type of input command or output response as follows.

Bits	Description
2 1 0	
0 0 0	Buffer address/character count (RCV) command or buffer disposition (RCV complete) response
0 0 1	Control command or control response
0 1 0	Mode definition command or information response
0 1 1	Buffer disposition (RCV unused) response
1 0 0	Buffer address/character count (XMIT) command or buffer disposition (XMIT complete) response
1 0 1	Reserved
1 1 0	Buffer disposition (sent but not acknowledged) response
1 1 1	Buffer disposition (not sent) response

BSEL2 Bit Functions (Cont)

Bit	Name	Description
03	22-bit mode	When set, this bit indicates to the DMV11 that the buffer address is in the 22-bit format.
04	Ready in (RDI)	RDI is a DMV11 response to RQI, indicating to the user program that it may load the data ports (SEL 4 and SEL 6) and the command type code (BSEL 2 bits 00-03). It is cleared by the user program when the data port contains the input command. Clearing RDI returns control back to the DMV11.
05-06	Reserved	
07	Ready output (RDO)	RDO is asserted by the DMV11 to indicate that the data ports (SEL 4 and SEL 6) contain information for the output responses defined by bits 00-02 of BSEL 2. The user program must clear RDO when it reads this information. Clearing RDO returns the port to the DMV11.

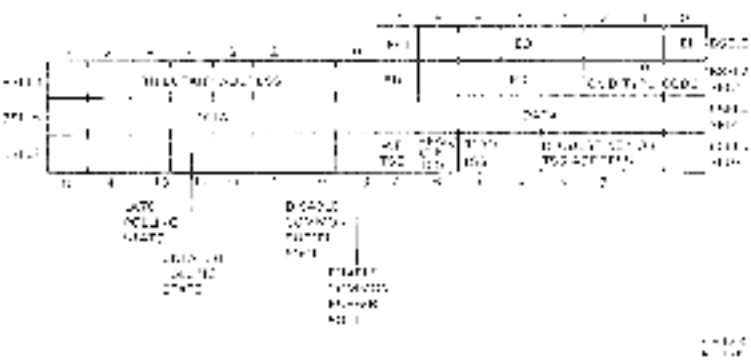
BSEL2 Bit Functions

Bits	Name	Description
[illegible]	Tributary address	Contains the address of the tributary modem

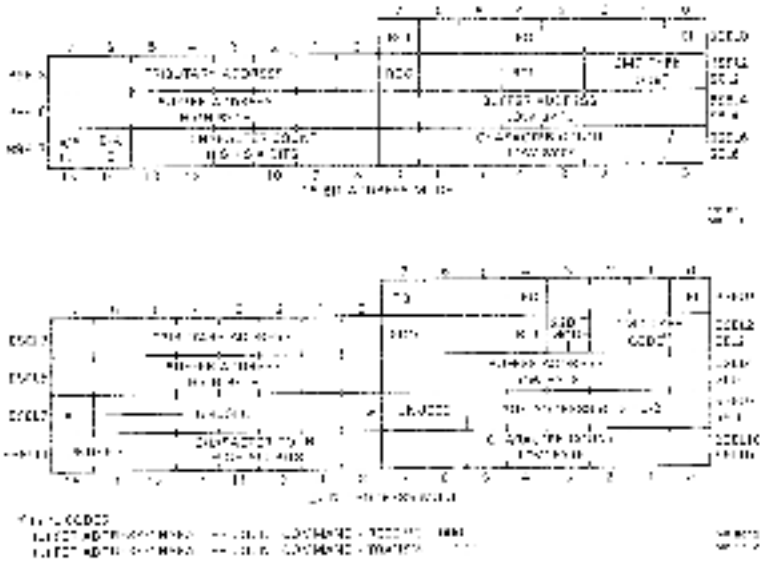
Command Functions

The program controlled command functions are extensive and will not be detailed. The register format will be described for each type of command function.

Mode Definition Command Format



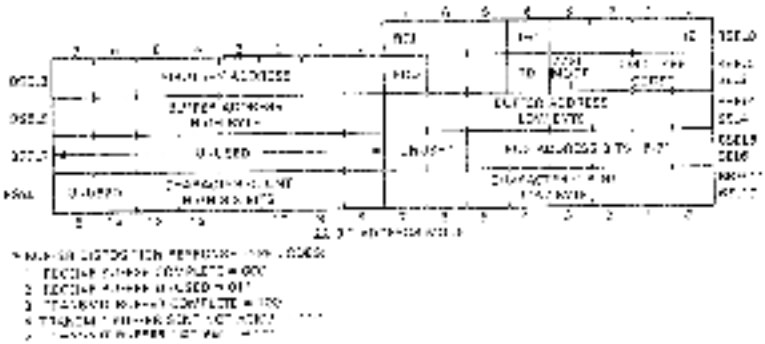
Control Command Format



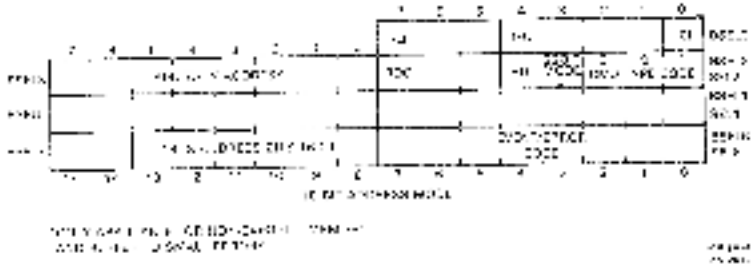
Buffer Address/Character Count Command Format

Response Functions

The program controlled output response functions are extensive and will not be detailed. The register format will be described for each type of response function.



Buffer Disposal on Response Format



Control Out Command Response Format

Information Response Format

DPV11 SERIAL SYNCHRONOUS INTERFACE

Power Requirements

[illegible] V (−5%) @ 0.3 A
[illegible] V (−5%) @ 1.2 A

Bus Loads

AC	DC
1	1

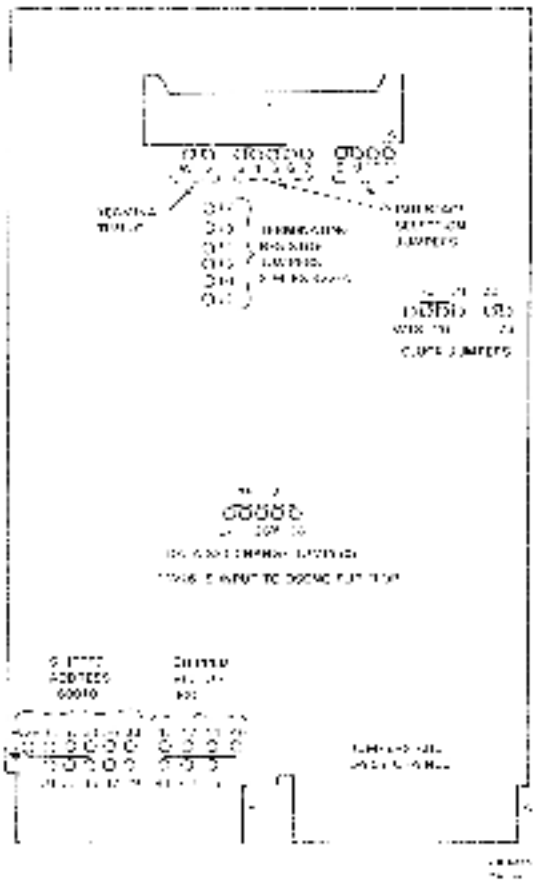
Cable

BC06L-25

Standard Addresses

Standard Address Assignments

Description	Mnemonic	Address	Status
Registers			
Receive control and status	RXCSR	160010	Read/write
Receive data and status	RDSR	160012	Read only
Parameter control/ Sync address	PCSAR	160014	Write only
Parameter control and Character length	PCSCR	160014	Read/write
Transmit data and status	TDSR	160016	Read/write
Vectors			
Break interrupt		300	



DPV11 Module Layout

Diagnostic Programs

Refer to Appendix A.

Related Documentation

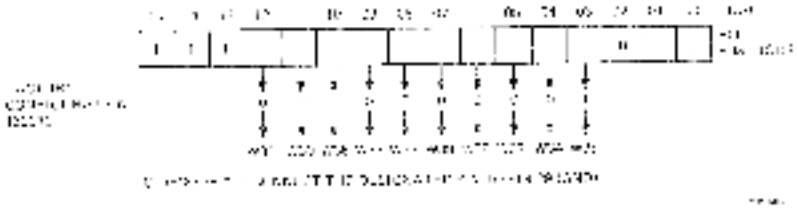
DPV11 User Manual (EK-DPV11-UG)
DPV11 Maintenance Reference Card (EK-DPV11-CQ)
Field Maintenance Print Set (M-000519)

CONFIGURATION

The DPV11 uses jumpers to select the device address, interrupt vector address, driver attenuation, interface selection, receiver termination, clock, and data set change. The normal configuration is typically RS-423-A compatible and the alternate is typically RS-422-A compatible.

Selecting DPV11 Device Address

The DPV11 device address is selected for the receive control and status register (RXCSR) by using the W29 to W31 jumpers. This allows the user to select the device address within the range of 160000 to 177770. The other registers are automatically assigned the next three addresses in increments of 2. Any jumper connected to W29 (ground) is decoded as a 1 in the corresponding bit position. The bit assignments for the jumpers are as follows.



DPV11 Device Address Format

Selecting DPV11 Interrupt Vector Address

The DPV11 generates an interrupt vector to the LSI-11 processor. An address can be selected within the range of 300 to 760 by using jumpers W40 to W48. Any jumper connected to W48 is decoded as a 1 in the corresponding bit position. The bit assignments for the jumpers are as follows.

DPV11 Vector Address Format

Driver Attenuation Jumper

The driver attenuation jumper is selected to bypass the attenuator resistor using jumpers W1 and W2 as follows.

Driver Attenuation Jumper

Driver	Normal Configuration	Alternate Option	Description
Terminal Timing	W1 to W2	Not connected	Bypasses attenuation resistor. Jumper must be removed for certain modems to operate properly

Interface Selection Jumpers

The interface selection jumpers are selected as follows using jumpers W3 to W11.

Interface Selection Jumpers

Input Signals	Normal Configuration	Alternate Option	Description
SQ/TM (PCSCH-5)	W5 to W6		Signal quality
		W7 to W6	Test mode
DM (DSR)	Not connected	W10 to W9	Data mode return for RS-422-A
SF/RL (RXCSH-6)	W3 to W4		Select frequency
		W4 to W3	Remote loopback
Local loopback	W8 to W9	Not connected	Local loopback
	Not connected	W8 to W11	Local loopback (alternate pin)

Receiver Termination Jumpers

The receiver termination jumpers are used for the RS-422-A compatible receiver termination, using jumpers W12 to W17 as follows.

Receiver Termination Jumpers

Receiver	Normal Configuration	Alternate Option	Description
Receive data	Not connected	W12 to W13	Connects terminating resistor for RS-422-A compatibility
Send timing	Not connected	W14 to W15	
Receive timing	Not connected	W16 to W17	

Clock Jumpers

The clock jumpers are used to provide a clock reference for the modem and use jumpers W19 to W23 as follows.

Clock Jumpers

Function	Normal Configuration	Alternate Option	Description
NULL MODEM CLK	W20 to W18		Sets NULL CLK MODEM CLK to 2 kHz
		W21 to W18	Sets NULL MODEM CLK to 505 kHz
Clock enable	W19 to W21 W22 to W23	W19 to W21 W22 to W23	Always installed except for factory testing

Data Set Jumpers

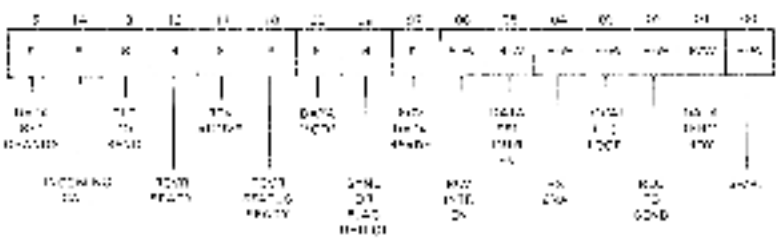
The data set jumpers are used to select the data mode and use jumpers W24 to W28 as follows.

Data Set Change Jumpers

Modem Signal Name	Normal Configuration	Alternate Option	Description
Data mode (DSR)	W26 to W24	Not connected	Connects the DSCNG flip-flop to the respective modem status signal for transition detection
Clear-to-send	W25 to W26	Not connected	
Incoming call	W26 to W27	Not connected	Note: W26 is input to DSCNG flip-flop
Receiver ready (carrier detect)	W26 to W28	Not connected	

RECEIVE CONTROL STATUS REGISTER (RXCSR)

The RXCSR is a read/write register and the bits are as follows.



Receive Control Status Register (RXCSR) Format

Receiver Control Status Register (RXCSR) Bit Assignments

Bit	Name	Description
15	Data set change (DSCNG)	This bit is set when a transition occurs on any of the following modem control lines. Clear-to-send Data mode Receiver ready Incoming call Transition detectors for each of these four lines can be disabled by removing the associated jumper. Data set change is cleared by reading either byte of the RXCSR or by device reset or BUS INIT. Data set change causes a receive interrupt if DSITEN (bit 06) and RXITEN (bit 06) are both set.
4	Incoming call (IC)	This bit reflects the state of the modem incoming call line. Any transition of this bit causes the data set change bit (bit 15) to be asserted unless the incoming call line is disabled by removing its jumper. This bit is read only and cannot be cleared by software.
13	Clear-to-send (CTS)	This bit reflects the state of the clear-to-send line of the modem. Any transition of this line causes the data set change bit to be set unless the jumper enabling the clear-to-send signal is removed. Clear-to-send is program read only and cannot be cleared by software.

Receiver Control Status Register (RXCSR) Bit Assignments (Cont)

Bit	Name	Description
12	Receiver ready (RR)	This bit is a direct reflection of modem receiver ready lead. It indicates that the modem is receiving a carrier signal. For external maintenance loopback, this signal must be high. If the line is open, RR is pulled high by the circuitry. Any transition of this bit causes the data set change bit to be asserted unless the jumper enabling the receiver ready signal is removed. Receiver ready is a read-only bit and cannot be cleared by software.
11	Receiver active (RXACT)	This bit is set when the USYNRT presents the first character of a message to the DPV11. It remains set until the receive data path of the USYNRT becomes idle. Receiver active is cleared by any of the following conditions: a terminating control character is received in bit-oriented protocol modes; an off transition of receiver enable (RXENA) occurs; or device reset or bus init is issued. Receiver active is a read-only bit that reflects the state of the USYNRT output pin five.
10	Receiver status ready (RSTARY)	This bit indicates the availability of status information in the upper byte of the receive data and status register (RDSR). It is set when any of the following bits of the RDSR are set: receiver end of message (REOM); receiver overrun (RCV OVRUN); receiver abort or go ahead (RABORT); error check (ERRCHK) if VRC is selected.

Receiver Control Status Register (RXCSR) Bit Assignments (Cont)

Bit	Name	Description
		Receiver status is cleared by any of the following conditions: reading either byte of the RDSR, clearing receiver enable (bit 04 of RXCSR), device reset, or RUN to 1. When set, receiver status ready causes a receive interrupt if receive interrupt enable (bit 06) is also set. Receiver status ready is a read-only bit that reflects the state of USYNRT pin seven.
09	Data mode (DM) (data set ready)	This bit reflects the state of the data mode signal from the modem. When this bit is on, it indicates that the modem is powered on and not in test, talk, or dial mode. Any transition of this bit causes the data set change bit (bit 15) to be asserted unless the data mode jumper has been removed. Data mode is a read-only bit and cannot be cleared by software.
08	Sync or flag detect (SFD)	This bit is set for one clock time when a flag character is detected with bit oriented protocols, or a sync character is detected with character oriented protocols. SFD is a read-only bit that reflects the state of USYNRT Pin four.

Receiver Control Status Register (RXCSR) Bit Assignments (Cont)

Bit	Name	Description
07	Receive data ready (RDATRY)	This bit indicates that the USYNPT has assembled a data character and that it is ready to present it to the processor. If this bit becomes set while receiver interrupt enable (bit 06) is set, a receive interrupt request will result. Receive data ready is reset when either byte of RDBR is read, receiver enable (bit 04) is cleared, device reset, or BUS INIT is issued. It is a read-only bit that reflected the state of USYNPT pin A4.
06	Receiver interrupt enable (RXTEN)	When set, this bit allows interrupt requests to be made to the receiver vector whenever RDATRY (bit 07) becomes set. The conditions that cause the interrupt request are the assertion of receive data ready (bit 07), receive status ready (bit 10), or data set change (bit 15) if MCINTEN is also set. RXITEN is program read/write and is cleared by device reset or BUS INIT.
05	Data set interrupt enable (DSITEN)	This bit, when set, along with RXITEN, allows interrupt requests to be made to the receiver vector whenever the data set change bit becomes set. DSITEN is a program read/write bit and is cleared by device reset or BUS INIT.

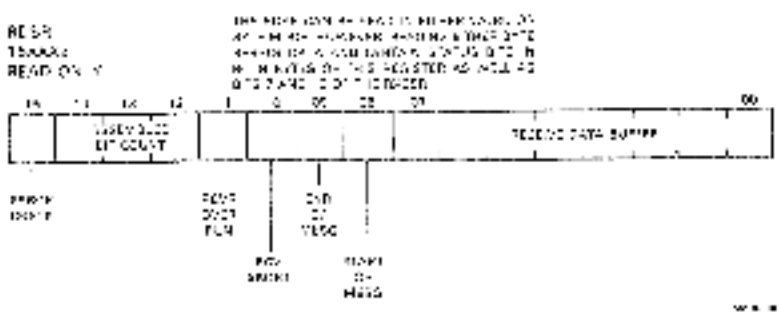
Receiver Control Status Register (RXCSR) Bit Assignments (Cont)

Bit	Name	Description
04	Receiver enable (RXENA)	This bit controls the operation of the receive section of the USYNRT. When this bit is set, the receive section of the USYNRT is enabled. When it is reset, the receive section is disabled. In addition to disabling the receive section of the USYNRT, resetting bit 04 reinitializes all but two of the USYNRT receive registers. The two registers not reinitialized are the character length selection buffer and the parameter control register.
03	Local loopback (LL)	Asserting this bit causes the modem connected to the DPV11 to establish a data loopback test condition. Clearing this bit restores normal modem operation. Local loopback is program read/write and is cleared by device reset or BUS INIT.
02	Request to send (RTS)	Setting this bit asserts the request to send signal at the modem interface. Request to send is program read/write and is cleared by device reset or BUS INIT.
01	Terminal ready (TR) (data terminal ready)	When set, this bit asserts the terminal ready signal to the modem interface. For auto dial and manual call origination, it maintains the established call. For auto answer, it allows handshaking in response to a ring signal.

Receiver Control Status Register (RXCSR) Bit Assignments (Cont)

Bit	Name	Description
00	Select frequency or remote loopback (SF/RL)	This bit can be wirewrap jumpered to function as either select frequency or remote loopback. When jumpered as select frequency (W3 to W4), setting this bit selects the modem's higher frequency band for transmission to the line and the lower frequency band for reception from the line. The clear condition selects the lower frequency for transmission and the higher frequency for reception. When jumpered for remote loopback (W3 to W5), this bit, (when asserted) causes the modem connected to the DPV11 to signal when a remote loopback test condition has been established in the remote modem. SF/RL is program read/write and is cleared by BUS INIT or device reset.

RECEIVE DATA AND STATUS REGISTER (RDSR)
The RDSR is a read only register and the bits are as follows.



Receive Data and Status Register (RDSR) Format

Receive Data and Status Register (RDSR) Bit Assignments

Bit	Name	Description
15	Error check (ERR CHK)	When set, this bit indicates a possible error. It is used in conjunction with the error detection selection bits of the parameter control sync/address register (bits 08–10) to indicate either an error or an all zeros state of the CRC register. With bit-oriented protocols, ERR CHK indicates that a CRC error has occurred. It is set when the receiver end of message bit (RDSR bit 09) is set. With character-oriented protocols, ERR CHK is asserted with each data character if all zeros are in the CRC register. The processor must then determine if this indicates an error-free message or not. If VRC parity is selected, this bit is set for every character that has a parity error. ERR CHK is cleared by reading the RDSR and clearing RXENA (RXCSR bit 04), device reset, or BUS INIT.
14–12	Assembled bit count (ABC)	Used only with bit-oriented protocols, these bits represent the number of valid bits in the last character of a message. They are all zeros unless the message ends on an unstated boundary. The bits are encoded to represent valid bits as follows. 14 13 12 **Number of Valid Bits** 0 0 0 All bits are valid 0 0 1 One valid bit 0 1 0 Two valid bits 0 1 1 Three valid bits 1 0 0 Four valid bits 1 0 1 Five valid bits 1 1 0 Six valid bits 1 1 1 Seven valid bits

Receive Data and Status Register (RDSR) Bit Assignments (Cont)

Bit	Name	Description
		These bits are presented simultaneously with the last bits of data and are cleared by reading the RDSR or by asserting RXENA (bit 04 of RXCSR).
13	Receiver overrun (RCV OVRUN)	This bit is used to indicate that an overrun situation has occurred. Overrun exists when the data buffer (bits 00 to 07 of RDSR) has not been serviced within one character time. As a general rule, the overrun is indicated when the last bit of the current character has been received into the shift register of the USYNRT and the data buffer is not yet available for a new character. Two factors exist that modify this general rule and apply only to bit-oriented protocols. The first factor is the number of bits inserted into the data stream for transparency. For each bit inserted during the formatting of the current character, the controllers maximum response time is increased by one clock cycle. The second factor is the result of termination of the current message. When this occurs, the data of the terminated message that is within the USYNRT is not overrunable. If an attempt is made to displace this data by the reception of a subsequent message, the data of the subsequent message is lost until the data of the prior message has been relieved.

Receive Data and Status Register (RDSR) Bit Assignments (Cont)

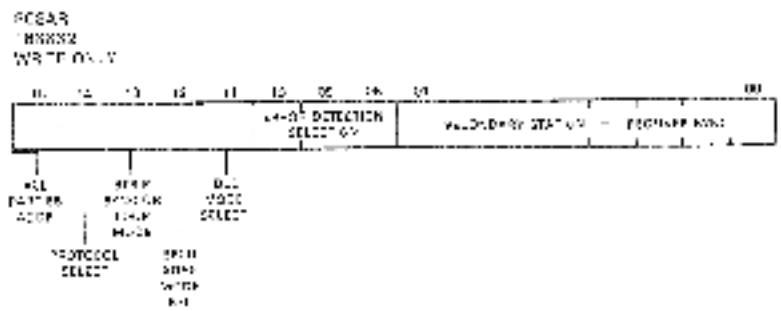
Bit	Name	Description
10	Receiver abort or go ahead (RABORT)	This bit is used only with bit oriented protocols and indicates that either an abort character or a go ahead character has been received. This is determined by the loop mode bit in the parameter control sync/address register (PCSAR). If the loop mode bit is clear, RABORT indicates reception of an abort character. If the loop mode bit is set, RABORT indicates a go ahead character has been received. The setting of RABORT causes receiver status ready (bit 10 of RXCSR) to become set. RABORT is reset when the RDSR is read or when receiver enable (bit 11 of RXCSR) is reset. The abort character is defined to be seven or more contiguous 1 bits appearing in the data stream. Reception of this bit pattern while loop mode is clear causes the receive section of the USYNRT to stop receiving and set RSTART. The abort character indicates abnormal termination of the current message. The go ahead character is defined as a zero bit followed by seven consecutive 1 bits. This character is recognized as a normal terminating control character when the loop mode bit is set. If loop mode is cleared, this character is interpreted as an abort character.

Receive Data and Status Register (RDSR) Bit Assignments (Cont)

Bit	Name	Description
09	Receiver end of message (REOM)	This bit is used only with bit-oriented protocols and is asserted if receiver active (bit 11 of RXCSR) is set and a message is terminated either normally or abnormally. When REOM becomes set, it sets RSTARY (bit 10 of RXCSR). REOM is cleared when the receive data and status register is read or when receive enable (bit 04 of RXCSR) is reset.
08	Receiver start of message (RSOM)	Used only with bit-oriented protocols. This bit is presented to the processor along with the first data character of a message and is synchronized to the last received flag character. Setting of RSOM does NOT set RSTARY. RSOM is cleared by device reset, BUS INIT, resetting receiver enable (RXCSR bit 04), or the next transfer into the receive data buffer (low byte of RDSR).
07-00	Receive data buffer	The low byte of the RDSR is the receive data buffer. The serial data input to the USYNRI is assembled and transferred to the low byte of the RDSR for presentation to the processor. When the RDSR receives data, receive data ready (bit 07 of RXCSR) becomes set to indicate that the RDSR has data to be picked up. If this data is not read within one character time, a data overrun occurs. The characters in the receive data buffer are right justified with bit 00 being the least significant bit.

PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAR)

The PCSAR register is a write only register with the same address as the RDDR register. The bits are as follows.



Parameter Control Sync/Address Register (PCSAR) Format

Parameter Control Sync/Address Register (PCSAR) Bit Assignments

Bit	Name	Description
15	All parties addressed (APA)	This bit is set when automatic recognition of the all parties addressed character is desired. The all parties addressed character is eight bits of 1s with necessary bit stuffing so as not to be confused with the abort character. Recognition of this character is done in the same way as the secondary station address (see bit 12 of this register) except that the broadcast address is essentially hardwired within the receive data path. The logic inspects the address character of each frame for the broadcast address. When the broadcast address is recognized, the USYNRT makes it available and sets receiver start of message (bit 05 of RDSR). If the broadcast address is not recognized, one of two possible actions occurs.

Parameter Control Sync/Address Register (PCSAR)
Bit Assignments (Cont)

Bit	Name	Description
		1. If the secondary address select mode bit (bit 12) is set, a test of the secondary station address is made. 2. If bit 12 is not set or the secondary station address is not recognized, the receive section of the USYNRT renews its search for synchronizing control characters.
14	Protocol select (PROT SEL)	This bit is used to select between character and byte count-oriented or bit oriented protocols. It is set for character and byte count-oriented protocols and reset for bit-oriented protocols.
13	Strip sync or loop mode (STRIP SYNC)	This bit serves two functions: strip sync (character oriented protocols) or loop mode (bit oriented protocols). 1. In character-oriented protocols all sync characters after the initial synchronization are deleted from the message and not included in the CRC computation if this bit is set. If it is cleared, all sync characters remain in the message and are included in the CRC computation. 2. With bit-oriented protocols, this bit is used to control the method of termination. If it is set, either a flag or go ahead character can cause a normal termination of a message. If it is cleared, only a flag character can cause a normal termination.

Parameter Control Sync/Address Register (PCSAR)
Bit Assignments (Cont)

Bit	Name	Description
12	Secondary address select (SEC ADR MDE)	This bit is used with bit-oriented protocols when automatic recognition of the secondary station address is desired. If it is set, the station address of the incoming message is compared with the address stored in the low byte of this register. Only messages prefixed with the correct secondary address are presented to the processor. If the addresses do not compare, the receive section of the USYNRT goes back to searching for flag or go ahead characters. When SEC ADR MDE is cleared, the receive section of the USYNRT recognizes all incoming messages.
11	Idle mode select (IDLE)	This bit is used with both bit- and character-oriented protocols. With bit-oriented protocols, IDLE is used to select the type of control character issued when either the transmit abort bit is set or a data underrun error occurs. If IDLE is set, flag characters are issued. If IDLE is clear, abort characters are issued. With character-oriented protocols, IDLE is used to control the method in which initial sync characters are transmitted and the action of the transmit section of the USYNRT when an underrun error occurs. IDLE is asserted to cause sync characters from the low byte of this register (PCSAR0) to be transmitted. When IDLE is cleared, the transmit data output is held asserted during an underrun error and at the end of a message

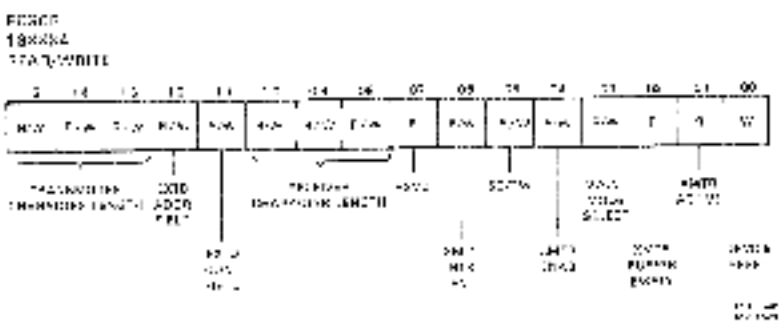
Parameter Control Sync/Address Register (PCSAR)
Bit Assignments (Cont)

Bit	Name	Description
10–08	Error detection selection (ERR DEL SEL)	These bits are used to determine the type of error detection used on received and transmitted messages. In bit-oriented protocols, the selection is independent of character length. In character- and byte-oriented protocols, CRC error detection is usable only with 8-bit character lengths; the maximum character length for VRC is seven. The bits are encoded as follows. 10 9 8 — CRC Polynomial 0 0 0 — $x^{16} + x^{12} + x^5 + 1$ (CRC CCITT) (Both CRC data registers in the transmit and receive sections are set to all ones prior to the computation.) 0 0 1 — $x^{16} + x^{15} + x^2 + 1$ (CRC CCITT) (Both CRC data registers set to all zeros.) 0 1 0 — Not used. 0 1 1 — $x^{16} + x^{15} + x^2 + 1$ (CRC 16) (Both CRC registers set to all zeros.) 1 0 0 — Odd VRC parity (A parity bit is attached to each transmitted character. It should be used only in character oriented protocols.)

Parameter Control Sync / Address Register (PCSAR)
Bit Assignments (Cont)

Bit	Name	Description
		10 9 8 CRC Polynomial 1 0 1 Even VRC parity (This is like odd VRC except that an even number of bits are generated.) 1 1 0 Not used. 1 1 1 All error detection is inhibited.
07-00	Sync character or secondary address	The low byte of this register (PCSAH) is used as either the sync character for character-oriented protocols or as the secondary station address for bit-oriented protocols. The bits are right justified with the least significant bit being bit 00.

PARAMETER CONTROL AND CHARACTER LENGTH REGISTER (PCSCR)
The PCSCR register is a read/write register. The bits are as follows.



Parameter Control and Character Length Register
(PCSCR) Format

Parameter Control and Character Length Register (PCSCR)
Bit Assignments

Bit	Name	Description
15-13	Transmitter character length	These bits can be read or written and are used to determine the length of the characters to be transmitted. They are encoded to set up character lengths as follows. 15 14 13 Character Length 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character (Bit-oriented protocol only) 1 0 0 Four bits per character (Bit-oriented protocol only) 0 1 1 Three bits per character (Bit-oriented protocol only) 0 1 0 Two bits per character (Bit-oriented protocol only) 0 0 1 One bit per character (Bit oriented protocol only) These bits can be changed while the transmitter is active, in which case the new character length is assumed at the completion of the current character. This field is set to a character length of eight by device reset or BUS INIT. When VRC error detection is selected, the default character length is eight bits plus parity.

Parameter Control and Character Length Register (PCSCR)
Bit Assignments (Cont)

Bit	Name	Description
12	Extended address field (EXADD)	This bit is used with bit-oriented protocols and affects the address portion of a message in receiver operations. When it is set, each address byte is tested for a one in the least significant bit position. If the LSB is zero, the received character is an extension of the address field. If the LSB is one, the current character terminates the address field and the next character is a control character. EXADD is not used with secondary address mode (bit 12 of PCSAR). EXADD is read/write and is reset by device reset or BUS INIT.
11	Extended control field (EXCON)	This bit is used with bit-oriented protocols and affects the control character of a message in receiver operations. When EXCON is set, it extends the control field from one 8-bit byte to two 8-bit bytes. EXCON is not used with secondary address mode (bit 12 of PCSAR). EXCON is read/write and is reset by device reset or BUS INIT.
10 08	Receiver character length	These bits are used to determine the length of the characters to be received.

Parameter Control and Character Length Register (PCSCR)
Bit Assignments (Cont)

Bit	Name	Description
		They are encoded to set up character lengths as follows:
		10 9 8 Character Length
		0 0 0 Eight bits per character
		1 1 1 Seven bits per character
		1 1 0 Six bits per character
		1 0 1 Five bits per character
		1 0 0 Four bits per character (Bit-oriented protocols only)
		0 1 1 Three bits per character (Bit-oriented protocols only)
		0 1 0 Two bits per character (Bit-oriented protocols only)
		0 0 1 One bit per character (Bit-oriented protocols only)
07	Reserved	Not used by the DPV11
06	Transmit interrupt enable (TXINTEN)	When set, this bit allows a transmitter interrupt request to be made to the transmitter vector when transmit buffer empty (TBEMTY) is asserted. Transmit interrupt enable is read/write and is cleared by device reset or BUS INIT.

Parameter Control and Character Length Register (PCSCR)
Bit Assignments (Cont)

Bit	Name	Description
05	Signal quality or test mode (SQ/TM)	This bit can be wirewrap jumpered to function as either signal quality or test mode. When jumpered for signal quality (W5 to W6), this bit reflects the state of the signal quality line from the modem. When asserted it indicates that there is a low probability of errors in the received data. When clear, it indicates that there is a high probability of errors in the received data. When jumpered for test mode (W1 to W7), this bit indicates that the modem has been placed in a test condition when asserted. The modem test condition could be established by asserting local loopback (bit 03 of RXCSR), remote loopback (bit 00 of RXCSR), or other means external to the DPV11. When SQ/TM is clear it indicates that the modem is not in test mode and is available for normal operation. SQ/TM is program read-only and can not be cleared by software.

Parameter Control and Character Length Register (PCSCR)
Bit Assignments (Cont)

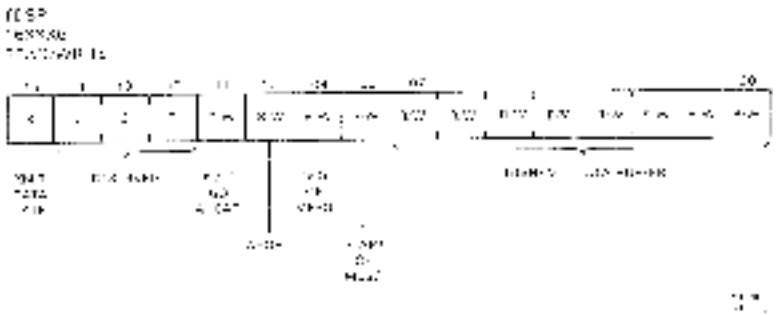
Bit	Name	Description
04	Transmitter enable (TXENA)	This bit must be set to initiate the transmission of data or control information. When this bit is cleared, the transmitter will revert back to the mark state once all requested sequences have been completed. TXENA should be cleared after the last data character has been loaded into the transmit data and status register. Transmit end of message (TEOM) should be asserted when TXENA is reset (if it is to be asserted at all) and remain asserted until the transmitter enters the idle mode. TXENA is connected directly to USYNRT pin 37. It is a read/write bit and is reset by device reset or BUS INIT.
03	Maintenance mode select (MM SEL)	When this bit is asserted, it causes the USYNRT's serial output to be internally connected to the USYNRT's serial input. The serial send data output line from the interface is asserted and the receive data serial input is disabled. Send timing and receive timing to the USYNRT are disabled and replaced with a clock signal generated on the interface. The clock rate is either 49.152K bits/s or 1.0368K bits/s depending on the position of a jumper on the interface board. Maintenance mode allows diagnostics to run in loopback without disconnecting the modem cable. MM SEL is a read/write bit and is cleared by device reset or BUS INIT. When it is cleared, the interface is set for normal operation.

Parameter Control and Character Length Register (PCSCR)
Bit Assignments (Cont)

Bit	Name	Description
02	Transmitter buffer empty (TBEMTY)	This bit is asserted when the transmit data and status register (TDSR) is available for new data or control information. It is also set after a device reset or BUS INIT. The TDSR should be loaded only in response to TBEMTY being set. When the TDSR is written into, TBEMTY is cleared. If TBEMTY becomes set while transmit interrupt enable is set, a transmit interrupt request results. TBEMTY reflects the state of USYNRT pin 34.
01	Transmitter active (TXACT)	This bit indicates the state of the transmit section of the USYNRT. It becomes set when the first character of data or control information is transmitted. TXACT is cleared when the transmitter has nothing to send or when device reset or BUS INIT is issued. TXACT reflects the state of USYNRT pin 34.
00	Device reset (RESET)	When a one is written to this bit all components of the interface are initialized. It performs the same function as BUS INIT with respect to this interface. Modem status (data mode, clear-to-send, receiver ready, incoming call, signal quality, or test mode) is not affected. RESET is write only; it cannot be read by software.

TRANSMIT DATA AND STATUS REGISTER (TDSR)

The TDSR register is a read/write register. The bits are as follows:



Transmit Data and Status Register (TDSR) Format

Transmit Data and Status Register Bit Assignments

Bit	Name	Description
15	Transmitter error (TERR)	This is a read-only bit that becomes asserted when the transmitter buffer empty (TBEMTY) indication has not been serviced for more than one character time. When TERR occurs in bit-oriented protocols, the transmit section of the USYNRT generates an abort or flag character based on the state of the IDLE bit (PCSAR bit 11). If IDLE is set, a flag character is sent. If it is reset, an abort character is sent. When TERR occurs in character-oriented protocols, the state of the IDLE bit again determines the result. If IDLE is set, the transmit serial output is held in the MARK condition. If it is cleared, a sync character is transmitted.

Transmit Data and Status Register Bit Assignments (Cont)

Bit	Name	Description
		TERR is cleared when TSOM (TDSR bit 08) becomes set or by device reset or BUS INIT. Clearing Transmit enable does not clear TERR, and TERR is not set with transmit end of message.
11-12	Reserved	Not used by the DPV11.
11	Transmit go ahead (TGA)	The function of this bit, when asserted, is to modify the bit pattern of the control character initiated by either transmit start of message (TSOM) or transmit end of message (TEOM). TSOM or TEOM normally cause a flag character to be sent. If TGA is set, a go ahead character is sent in place of the flag character. TGA is only used with bit-oriented protocols.
10	Transmit abort (TXABORT)	This bit is used only with bit oriented protocols and is used to abnormally terminate a message or to transmit filler information used to establish data link timing. When TXABORT is asserted, the transmitter automatically transmits either flag or abort characters depending on the state of the IDLE mode bit. If IDLE is cleared, abort characters are sent. If IDLE is set, flag characters are sent.

Transmit Data and Status Register Bit Assignments (Cont)

Bit	Name	Description
09	Transmit end of message (TEOM)	This control bit is used to normally terminate a message in bit oriented protocol. It also terminates a message in character-oriented protocols when CRC error detection is used. As a secondary function, it is used in conjunction with the transmit start of message bit to transmit a space sequence. Refer to the TSOM bit description (bit 05 of this register) for information regarding this sequence. With bit oriented protocols, asserting this bit causes the CRC information to be transmitted, if CRC is enabled, followed by flag or go ahead characters depending on the state of the transmit go ahead (TGA) bit. See bit 11 of this register. With character-oriented protocols asserting this bit causes CRC information, if CRC is enabled, to be transmitted followed by either sync characters or a MARK condition depending on the state of the IDLE bit. If IDLE is cleared, sync characters are transmitted. The character following the CRC information is repeated until the transmitter is disabled or the TEOM bit is cleared. A subsequent message may be initiated while the transmit section of the USYNRT is active. This is accomplished by clearing TEOM bit and supplying new message data without setting the transmit start of message bit. However, the CRC character for the prior message must have completed transmission.

Transmit Data and Status Register Bit Assignments (Cont)

Bit	Name	Description
08	Transmit start of message (TSOM)	This bit is used with either bit- or character-oriented protocols. As long as it remains asserted, flag characters (bit-oriented protocols) or sync characters (character-oriented protocols) are transmitted. With bit-oriented protocols, a close sequence of 16 zero bits can be transmitted by asserting TSOM and TEOM simultaneously, provided the transmitter is in the idle state and transmit enable is cleared. This should not be done during the transfer of data, and must only be done in byte mode. **NOTE** **When using the special space sequence function, all registers internal to the USYNRT must be written in byte mode.** Normally at the completion of each sync, flag, go ahead, or abort character, the TBEMTY indication is asserted. This allows the software to count the number of transmitted characters. In certain applications, the software may elect to ignore the service of the TBEMTY indication. Normally during data transfers, this would cause a transmit data late error. The TSOM bit asserted suppresses this error and provides the necessary synchronization to automatically transmit another flag, go ahead, or sync character.

Transmit Data and Status Register Bit Assignments (Cont)

Bit	Name	Description
07-00	Transmit data buffer	Data from the processor to be transmitted on the serial output line is loaded into this byte of the TDSR when transmitter buffer empty (TBFMTY) is asserted. If the transmit buffer is not loaded within one character time, an underrun error occurs. The characters are right-justified and bit 00 is the least significant bit.

DRV11 PARALLEL LINE UNIT

Amps		Bus Loads		Cables
+5	1.9	AC	DC	
0 V	0	2.80	1.0	(2) BC07D
(1.6 max.)				(2) BC08R

Standard Addresses

	First Device	Second Device	MINC/ DECLAB
DRCSR	167770	167760	171770
DRBUFOUF	167772	167762	171772
DRINBUF	167774	167764	171774

Vectors

Interrupt A	300	310	370
Interrupt B	304	314	374

Diagnostic Programs

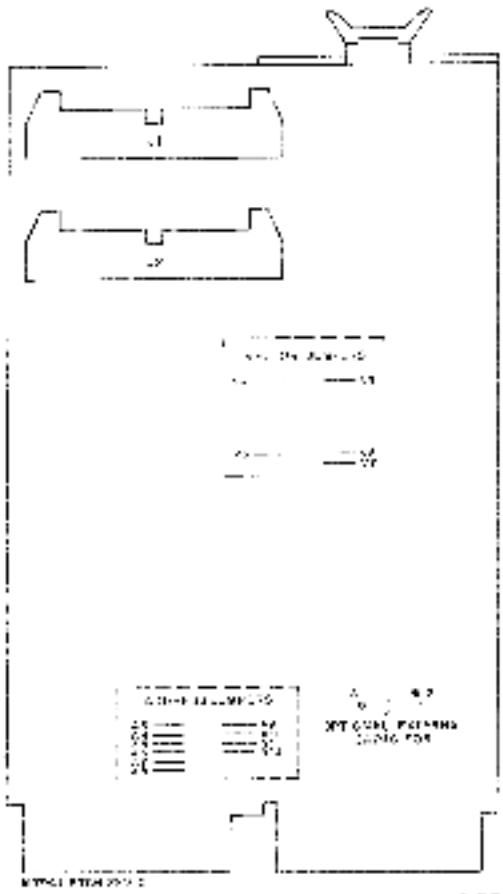
Refer to Appendix A.

NOTE

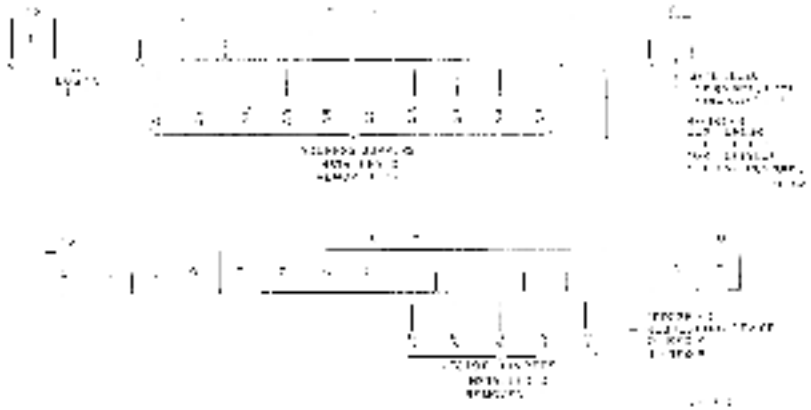
Full testing requires a BC08R wraparound cable for VRAF?? and DRA?.

Related Documentation

ADV11-A, AAV11-A, AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP00054)
Microcomputer Interfaces Handbook (EB-20175-20)



DRV11 (M7941) Jumpers



DRV11 PLU Factory Jumper Configuration

Jumper Designation	Jumper State	Function
A3	R	This arrangement of jumpers A3 through A12 assigns the device address 777776 to the PLU. This address is the starting address of a 16 word block in memory bank 7 which is recommended for user device address assignments. The least significant digit X is hardwired on the module to implement the three PLU device addresses as follows:
A4	R	
A5	R	
A6	R	
A7	R	
A8	R	
A9	R	
A10	R	
A11	R	
A12	R	X = 0, DR11B address X = 2, Output buffer address X = 4, Input buffer address
V3	R	This factory installed jumper configuration implements the two interrupt vector addresses 300 and 304 for use as defined by application requirements.
V4	R	
V5	R	
V6	R	
V7	R	
SL1	R	These jumper posts are provided for the installation of an external capacitor.
SL2	R	

External Capacitor

The pulse width of NEW DATA READY and DATA TRANSMITTED may be modified by installing an external capacitor. Note that the trailing edge of one of these two pulses must be used to clear interrupt requests.

Capacitor (μF)	Pulse Width (ns)
None (as shipped)	350
.0047	750
.01	1550
.02	2950
.03	4150

NOTE

Any system containing a REV11 and a DRV11 that has a capacitor to extend NEW DATA READY and DATA TRANSMITTED greater than 1500 ns may cause the REV11 to hang the system unless the REV11 is at ECO 5 level or greater (Circuit Schematic Rev K).

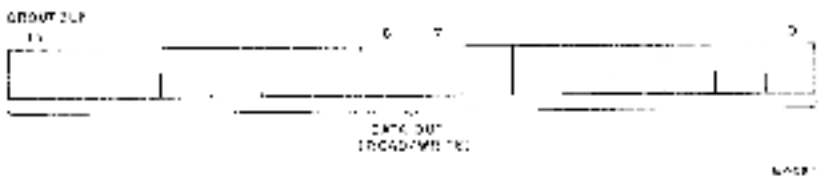
Control/Status Register

DRCSR Bit Definitions

Bit	Function
15	REQUEST B – This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.
14–08	Not used. Read as 0.
07	REQUEST A – Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Cleared by INIT when in maintenance mode. Read only.

DRCSR Bit Definitions (Cont)

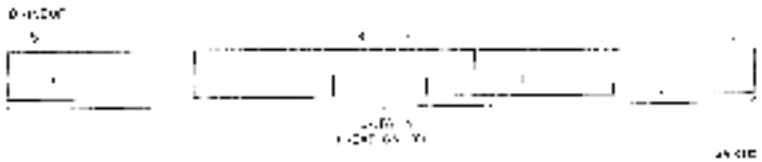
Bit	Function
06	INIT END A – Interrupt enable bit. When set, allows an interrupt request to be generated provided REQUEST A (bit 07) becomes set.
05	INIT END B – Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set.
04-02	Not used. Read as 0. Can be loaded or read by the program. Cleared by INIT. Read/write.
01	CSR1 – This bit can be loaded or read (under program control) and can be used for a user defined command to the device (appears only on connector no. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Can be loaded or read by the program. Cleared by INIT. Read/write.
00	CSR0 – Performs the same functions as CSR1 (bit 01) but appears only on connector no. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Cleared by INIT. Read/write.



Output Data Buffer Register (DROUTBUF)

DROUTBUF Bits 15–00
Output Data Buffer – Contains a full 16-bit word or one or two 8-bit bytes. High byte = bits 15–8, low byte = 7–0.

Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.



Input Data Buffer Register (DRINBUF)

DRINBUF Bits 15–00
Input Data Buffer Contains a full 16 bit word or one or two 8-bit bytes. The entire 16 bit word is read under a program-controlled DATI bus cycle.

DRV11-B GENERAL PURPOSE DMA INTERFACES

Amps		Bus Loads		Cables
−5	+12	AC	DC	
1.9	0	3.3	1.0	Two BC04Z Two BC05R

Standard Addresses

		MINC/ DECLAB
Word Count Register (WCR)	772410	171770
Bus Address Register (BAR)	772412	171772
CSR	772414	171774
DBR	772416	171776

Vector

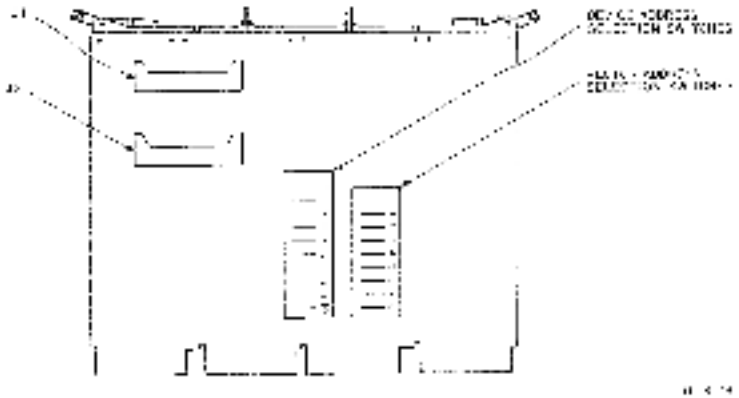
124 370

Diagnostic Programs

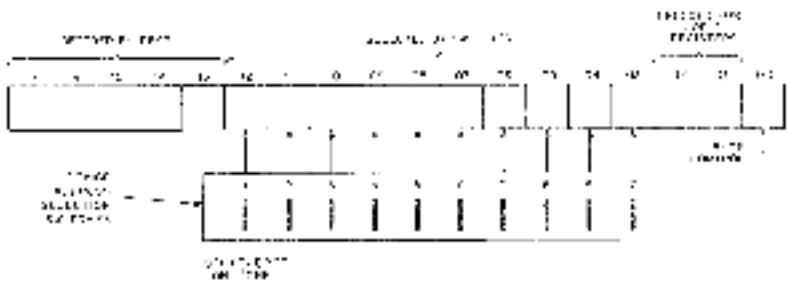
Refer to Appendix A.

Related Documentation

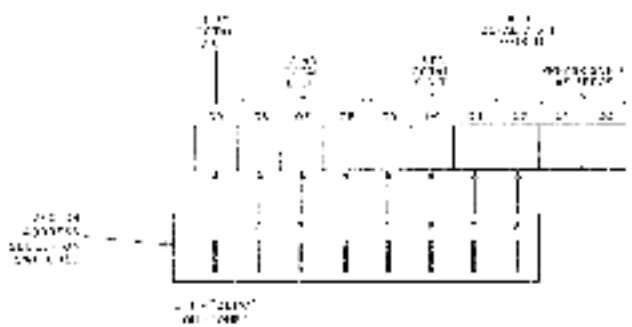
DRV11-B General Purpose DMA Interface User's Manual (EK-DRV1B-OP-001)
Field Maintenance Print Set (MP00160)
Microcomputer Interfaces Handbook (EB-20175-20)



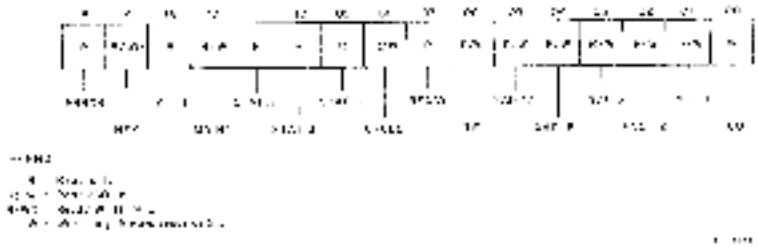
DRV11-B Switches



DRV11-B Device Address Select Format



DRV11-B Interrupt Vector Address Select Format



CSR Format (11 A1B6)

CSR Bit Functions

Bit	Function
00	Go - Write only. Always reads as 0. 1. Causes ready to be sent to the user's device, indicating that a command has been issued. 2. Allows DMA operation
01, 02, 03	FNCT 1, 2, 3 - Read/Write. 1. These outputs. 2. Cleared by INIT.
04, 05	XA(17-16) - Read/Write. Two bits used for extended addressing. Bits 04 and 05 increment with the address count when the BAR wraps around to 0.
06	IE - Read/Write. 1. Enables interrupts to occur when ready set. 2. Cleared by INIT
07	Ready - Read only. Indicates that the DRV11-B is able to accept a new command. Set by INIT, WDCFLG, ERROR; cleared by GO (bit 00)
08	Cycle - Read/write. Cycle is used to prime a DMA bus cycle. set by CYCLE REQUEST, cleared during DMA cycle. INIT.
09, 10, 11	STAT A, B, C - Read only. Three device status input bits that indicate the state of the DSTAT A, B, and C user signals.

CSR Bit Functions (Cont)

Bit	Function
12	MAINT – Read/write. Maintenance bit for use with the MAINDEC diagnostic.
13	ATTN – Read only. Indicates the state of the ATTN (user signal) sets ready, error.
14	NEX – Read/write to 0 bit. 1. Nonexistent memory: Indicates that as bus master, the DRV11-B did not receive DRPLY or that a DATO cycle was not completed. 2. Set error. 3. Cleared by INIT or by writing it to a 0.
15	Error – Read only. 1. Indicates one of the following special conditions: a. NEX (bit 14) b. ATTN (bit 13) 2. Sets ready (bit 7) and causes an interrupt if IE (bit 6) is set. 3. Cleared by removing the special condition as follows: a. NEX is cleared by writing bit 14 to a 0. b. ATTN is cleared by the user device.

DRV11-J GENERAL PURPOSE PARALLEL LINE INTERFACE

Amps	Bus Loads		Cables
+5 V	AC	DC	
1.3A	2	1	BC02D-XX BC08Y-XX H3116W-XX (For loopback half-twist connector)

Standard Addresses

	A	B	C	D
CSR	764160	764164	764170	764174
DBR	764162	764166	764172	764176

Standard Vectors

Software programmable in the range 000_8 - 774_8

Diagnostic Programs

Refer to Appendix A

NOTE

Both the XXDP+ diagnostics and the DEC/X11 module require the installation of a BC05W-XX loopback cable.

Related Documentation

DRV11-J Field Maintenance Print Set (MP-00886-00)
DRV11-J User Guide (EK-DRV11J-UG)

Technical, detailed information is beyond the scope of this manual. Additional information can be found in the *Microcomputer Interfaces Handbook* EB-20175-20.

Device Address

There are eight device registers on the M8049 module that can be individually addressed by the computer program. These registers are divided into four control status registers (CSR A, B, C, D), and four data buffer registers (DBR A, B, C, and D)

Addresses for the module are selectable from location 760000 octal through 777600 octal address range. When more than one DRV11-J is desired, the module's starting address must be assigned in descending order and separated by 20 octal addresses. Example: the first module will be 760060, the second 760040, and the third, 760020 octal.

Nine address jumpers (W1 through W9) are installed or removed to establish a base device register address. Note that address bits A13 through A15 are neither configured nor decoded by the module. These bits are decoded by the bus master module as the bank 7 select (BS7/L) bus signal. Address bit 0 is used by the program to select a high-byte or low-byte operation. Address bits 1 through 3 are used to select one of the eight device registers in the addressed module.

DRV11-J Device Address Format

DRV11-J Registers

Mnemonic	Description	Address (Octal)*
CSRA	Control Status Register A	7XXXX0
DBRA	Data Buffer Register A	7XXXX2
CSRB	Control Status Register B	7XXXX4
DBRB	Data Buffer Register B	7XXXX6
CSRC	Control Status Register C	7XXX10
DBRC	Data Buffer Register C	7XXX12
CSRD	Control Status Register D	7XXX14
DBRD	Data Buffer Register D	7XXX16

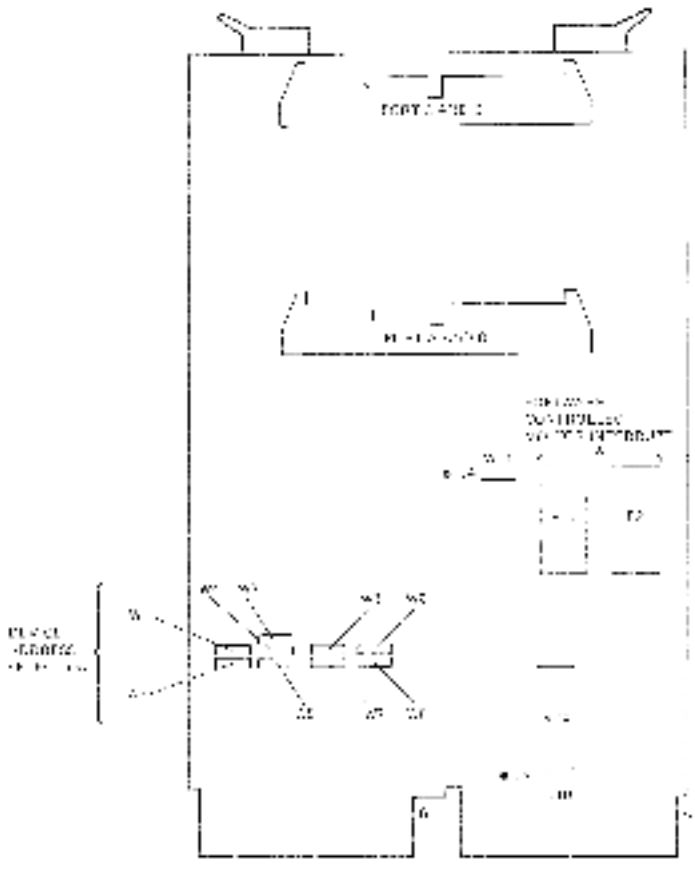
*XXXX is jumper selectable between 10000 and 77760 octal in 8 modules or 20 octal.

Interrupt Vector Addresses

The DRV11-J may be programmed to operate in systems requiring either vectored interrupts or polled interrupts. If the DRV11-J is used in a system that required vectored interrupts, the interrupt vector addresses must be programmed into a 64 x 8-bit RAM (vector address memory) contained in two interrupt controller chips (E2 and F10). Each interrupt controller chip may store a max mum of 32 interrupt vector addresses. CSRB bits D 07-00 are used in conjunction with CSRA bits 07-00 to program the 32 vector addresses for group 1 interrupt control. CSRD bits 07-00 are used in conjunction with CSRC bits to program the 32 vector addresses for group 2 interrupt control. Note that vector address bits V8 through V2 are programmed by CSRB or DSRD bits D7 through D0, respectively.

A total of 64 vector addresses in the 0000 through 1774 octal range may be stored in the vector address memory. To avoid device conflicts, refer to Appendix A of the *Microcomputer Interfaces Handbook*, EB-20174-20, when assigning vector addresses.

DRV11-J Vector Address Format

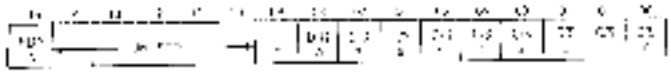


DRV11-J Jumper Locations

DRV11-J Factory Jumper Configuration

Jumper	Function	Jumper State*	Function
W1	A 2	R	This arrangement of jumpers W1 through W8 assigns the device address 764 (hex) to the first of eight contiguous bus registers. With a starting address of 764160 octal, the remaining bus registers are automatically assigned the following contiguous addresses:
W2	A 3	I	
W3	A10	R	
W4	A9	R	
W5	A8	R	CSRA 764130 DBRA 764132 CSRB 764134 DBRB 764136 CSRC 764170 DBRC 764172 CSRD 764174 DBRD 764176
W6	A7	R	
W7	A6	I	
W8	A5	I	
W9	A4	I	
W10		I	Reserved for future use.
W11	Group Vector Interrupts	I	DRV11-J monitors group 2 vectored interrupts using pin A1/C bits 11 CR and USER REPLY (A through 7) signals (default configuration).

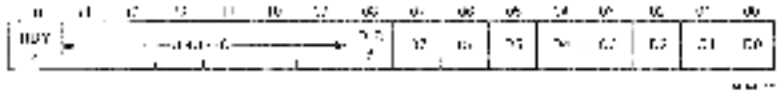
*R = removed = 0.
I = installed = 1.



CSRA Bit Assignments

CSRA Bit Function and Description

Bit	Function
07–00	C/S7–C/S0 These bits are used in conjunction with CSR3 bits (07–00) to program interrupt control group 1. They contain status information when read, and command words when written. Unaffected by BINIT. Read/write.
06	Direction A (DIR A) Used for controlling DSRA. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write
05	Interrupt Enable (IE) Enables the DRV11-J to generate processor interrupts when set. Used to enable both group 1 and group 2 interrupts. Cleared by BINIT. Read/write.
04–01	Unused. Read as 0s.
00	User Ready A (RDY A) Used for controlling DSRA. When read, yields the state of the USER RDY signal. A 0 equals negated and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.



CSR0 Bit Assignments

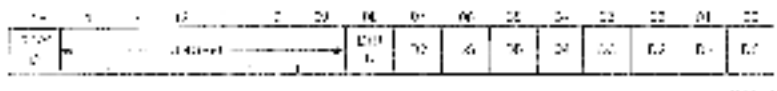
CSRB Bit Function and Description

Bit	Function
07–00	D7–D0 – These bits are used in conjunction with CSRA bits (07–00) to program interrupt control group 1. They contain interrupt vectors selected by the command word stored through CSRA. The registers available are the IRH, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. Read/write.
08	Direction B (DIR B) – Used for controlling DSRB. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14–09	Unused. Read as 0s.
15	User Ready B (RDY B) – Used for controlling DSRB. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.

CSRC Bit Assignments

CSRC Bit Function and Description

Bit	Function
C7–C0	C(S/ C/SC – These bits are used in conjunction with CSRD bits (07–00) to program interrupt control group 2. They contain status information when read and command words when written. Unaffected by BINIT. Read/write.
08	Direction C (DIR C) – Used for controlling DSRC. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14–09	Unused. Read as 0s.
15	User Ready C (RDY C) – Used for controlling DSRC. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT.



CSRD Bit Assignments

CSRD Bit Functions and Description

Bit	Function
07-00	D7-D0 – These bits are used in conjunction with CSRC bits (07–00) to program interrupt control group 2. They contain information selected by the command word loaded through CSRC. The registers available are the IRR, ISR, ACR, IMR and the vector address memory. Unaffected by BINIT. Read/write.
08	Direction D (DIR D) – Used for controlling DBRD. This bit, in conjunction with the USER RDY signal, controls the direction of data transfer. When the DIR bit is cleared, the DRV11-J RDY output signal is asserted and the DRV11-J is the input device. When set and the USER RDY signal is asserted, the DRV11-J is the output device. The negation of either DIR or USER RDY will cause the DRV11-J outputs to remain in their high impedance state. Cleared by BINIT. Read/write.
14-09	Unused. Read as 0s.
15	User Ready D (RDY D) – Used for controlling DBRD. When read, yields the state of the USER RDY signal. A 0 equals negated, and a 1 equals asserted. It is used in conjunction with the DIR bit to enable DRV11-J output operations. The user device asserts this signal when it desires the DRV11-J to output data. Unaffected by BINIT. Read only.

Data Buffer Register Bit Assignment

Data Buffer Registers

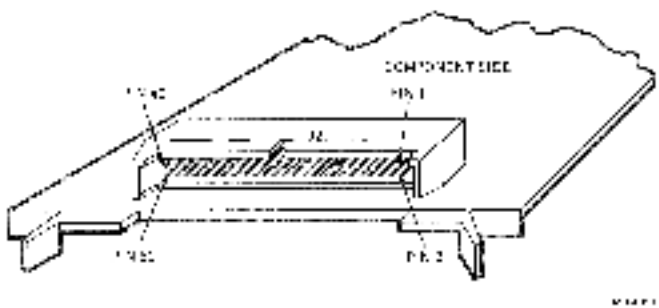
The data buffer registers (DBRA, DBRB, DBRC, and DBRD) are 16-bit word-addressable registers that contain output data when written and input data when read. In an output mode, reading the input register will yield the output buffer contents. The output buffers DBRA through DBRD are not cleared by initialize. The bit assignment is the same for all four registers.

Programmed Data Transfer

Input and output data transfers may be performed under program control by addressing the data buffer registers (DBRA, B, C, or D) and then reading or writing the data. Data is transferred on a 16-bit word-by-word basis by reading or writing the appropriate data buffer.

Interfacing to User's Device

Two board-mounted 50-pin male connectors (J1 and J2) interface the DRV11-J to the user device. Connector J1 is used to interface the port A and port B signals, while J2 is used for the port C and port D signals. Location of the connector pins is shown below with the interface signal names and their respective connector pins listed in the table that follows.



DRV11-J I/O Connector Pin Locations

I/O Connector Pin Functions

Signal Name	J1 Connector Pin	Signal Name	J2 Connector Pin
DRV11-J RDY A	J1-39	DRV11-J RDY D	J2-29
DRV11-J RPLY A	J1-33	DRV11-J RPLY D	J2-33
USER RDY A	J1-37	USER RDY D	J2-31
USER RPLY A	J1-27	USER RPLY D	J2-27
A I/O 15	J1-45	D I/O 15	J2-45
A I/O 14	J1-46	D I/O 14	J2-46
A I/O 13	J1-43	D I/O 13	J2-43
A I/O 12	J1-49	D I/O 12	J2-41
A I/O 11	J1-48	D I/O 11	J2-49
A I/O 10	J1-44	D I/O 10	J2-44

I/O Connector Pin Functions (Cont)

Signal Name	J1 Connector Pin	Signal Name	J2 Connector Pin
A I/O 9	J1-50	D I/O 9	J2-50
A I/O 8	J1-47	D I/O 8	J2-47
A I/O 7	J1-44	D I/O 7	J2-44
A I/O 6	J1-36	D I/O 6	J2-36
A I/O 5	J1-42	D I/O 5	J2-42
A I/O 4	J1-35	D I/O 4	J2-35
A I/O 3	J1-40	D I/O 3	J2-40
A I/O 2	J1-38	D I/O 2	J2-38
A I/O 1	J1-39	D I/O 1	J2-39
A I/O 0	J1-37	D I/O 0	J2-37
GND	J1-25	GND	J2-25
GND	J1-29	GND	J2-29
GND	J1-30	GND	J2-30
GND	J1-32	GND	J2-32
GND	J1-34	GND	J2-34
DRV11-J RDY B	J1-20	DRV11-J RDY C	J2-20
DRV11-J RPLY B	J1-24	DRV11-J RPLY C	J2-24
USER RDY B	J1-22	USER RDY C	J2-22
USER RPLY B	J1-18	USER RPLY C	J2-18
B I/O 15	J1-6	C I/O 15	J2-6
B I/O 14	J1-5	C I/O 14	J2-5
B I/O 13	J1-8	C I/O 13	J2-8
B I/O 12	J1-2	C I/O 12	J2-2
B I/O 11	J1-3	C I/O 11	J2-3
B I/O 10	J1-7	C I/O 10	J2-7
B I/O 9	J1-1	C I/O 9	J2-1
B I/O 8	J1-4	C I/O 8	J2-4
B I/O 7	J1-10	C I/O 7	J2-10
B I/O 6	J1-15	C I/O 6	J2-15
B I/O 5	J1-9	C I/O 5	J2-9
B I/O 4	J1-16	C I/O 4	J2-16
B I/O 3	J1-11	C I/O 3	J2-11
B I/O 2	J1-13	C I/O 2	J2-13
B I/O 1	J1-17	C I/O 1	J2-17
B I/O 0	J1-14	C I/O 0	J2-14
GND	J1-17	GND	J2-17
GND	J1-19	GND	J2-19
GND	J1-21	GND	J2-21
GND	J1-23	GND	J2-23
GND	J1-26	GND	J2-26

I/O Signal Functions

Signal Name*	Function
DRV11-J RDY [X]	This signal is asserted by the DRV11-J to inform the user that data may be placed on the I/O bus associated with the signal. It is asserted when the corresponding DIR bit is cleared.
DRV11-J RPLY [X]	This signal is asserted when the DRV11-J has accepted data (DRV11-J is the input device) by reading the corresponding data buffer with the associated DIR bit cleared, or when data is available for the user device (DRV11-J is the output device) by writing the corresponding data buffer with the associated DIR bit set.
[X] I/O <15:00>	These are the 16 three-state data buffer inputs and outputs.
USER RDY [X]	This signal is asserted by the user device to inform the DRV11-J that it requires input data (DRV11-J is the output device) and, in conjunction with the associated DIR bit, enables the DRV11-J three-state outputs.
USER RPLY [X]	This signal is asserted by the user device when data is accepted (DRV11-J is the output device) or when data is available (DRV11-J is the input device).

* [X] equals either A, B, C, or D.

Cables

The three types of cable used to connect the DRV11-J to a user device are described below.

Cable Description

Cable Type	Description	Max. Length**
BC02D-XX	Flat, 50 wires, shielded connectors (DEC P/N 12-11664) on both ends	1.00 m (3 ft)
BC05Y-XX	Round, 50-pin Berg to 50-pin Berg, 50 wires	1.82 m (6 ft)
BC05W-XX	Flat, 50 wires, shielded connectors (DEC P/N 12-11664) on both ends	7.6 m (25 ft)

* -XX in the cable denotes length in feet. For example, a 1.83 m (6 ft) BC02D cable would be ordered as BC02D-06.

** Maximum cable length is specified as being from DRV11-J to DRV11-J.

I/O Signal Specifications

All data buffer signals (I/O <15:00>) at the connectors (J1 and J2) are defined as being asserted (1) high (−3 V) and negated (0) low (GND). All protocol signals (DRV11-J RDY, DRV11-J BPLY, USER RDY and USER BPLY) at the connectors are defined as being asserted (1) low (GND) and negated (0) high (−3 V).

I/O Signal Loopback Connections

The DRV11-J signal pin assignments are arranged to permit loopback operation when a BC05W-XX cable is installed with a half twist connecting J1-1 to J2-50. With the cable installed in this manner, the proper connections are made to loopback the DRV11-J protocol signals.

DRV11-J Loopback Signal Connections

J1 Pin No.		Signal		Signal	J2 Pin No.	
Port B	1	B I/O 9	⟷	D I/O 9	50	Port D
	2	B I/O 12	⟷	D I/O 12	49	
	3	B I/O 11	⟷	D I/O 11	48	
	4	B I/O 8	⟷	D I/O 8	47	
	5	B I/O 14	⟷	D I/O 14	46	
	6	B I/O 15	⟷	D I/O 15	45	
	7	B I/O 10	⟷	D I/O 10	44	
	8	B I/O 13	⟷	D I/O 13	43	
	9	B I/O 5	⟷	D I/O 5	42	
	10	B I/O 7	⟷	D I/O 7	41	
	11	B I/O 6	⟷	D I/O 6	40	
	12	B I/O 1	⟷	D I/O 1	39	
	13	B I/O 2	⟷	D I/O 2	38	
	14	B I/O 0	⟷	D I/O 0	37	
	15	B I/O 3	⟷	D I/O 3	36	
	16	B I/O 4	⟷	D I/O 4	35	
	17	USER RPLY B	⟵	DRV11-J RPLY D	34	
	20	DRV11-J RDY B	⟶	USER RDY D	31	
	23	USER RDY B	⟵	DRV11-J RDY D	28	
	24	DRV11-J RPLY B	⟶	USER RPLY D	27	
Port A	27	USER RPLY A	⟵	DRV11-J RPLY C	24	Port C
	28	DRV11-J RDY A	⟶	USER RDY C	23	
	31	USER RDY A	⟵	DRV11-J RDY C	20	
	33	DRV11-J RPLY A	⟶	USER RPLY C	18	
	35	A I/O 4	⟷	C I/O 4	16	
	36	A I/O 6	⟷	C I/O 6	15	
	37	A I/O 8	⟷	C I/O 8	14	
	38	A I/O 9	⟷	C I/O 9	13	
	39	A I/O 1	⟷	C I/O 1	12	
	40	A I/O 3	⟷	C I/O 3	11	
	41	A I/O 7	⟷	C I/O 7	10	
	42	A I/O 5	⟷	C I/O 5	9	
	43	A I/O 13	⟷	C I/O 13	8	
	44	A I/O 10	⟷	C I/O 10	7	
	45	A I/O 15	⟷	C I/O 15	6	
	46	A I/O 14	⟷	C I/O 14	5	
	47	A I/O 0	⟷	C I/O 0	4	
	48	A I/O 11	⟷	C I/O 11	3	
	49	A I/O 12	⟷	C I/O 12	2	
	50	A I/O 2	⟷	C I/O 2	1	

Connector pins 17, 19, 21, 23, 25, 26, 28, 30, 32, 34 on J1 and J2 are grounds.

DRV11-P FOUNDATION MODULE

DRV11-P is a user configurable quad size, wirewrap module which provides adequate module area for mounting and connecting integrated circuits (IC's) or discrete components for a variety of device logic applications.

Amps		Bus Loads		Cables
+5	+ 12	AC	DC	
1.0		0.0	1.0	BC07A
Plus user's log c				BC07D
				BC08R
				BC04Z

Standard Addresses

No standard designated. Configurable within the range of 760000 - 777776. May conflict with DEC standard device addresses.

Vectors

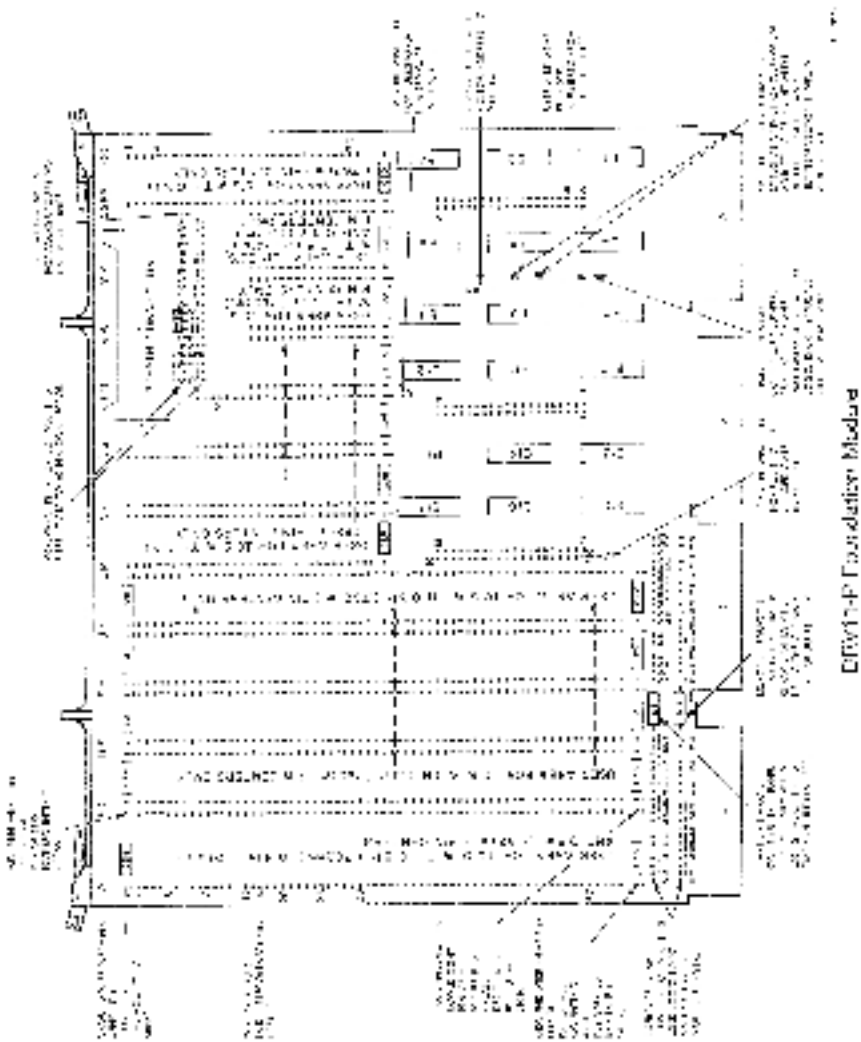
None assigned. Configurable within the range of 0-374. May conflict with DEC standard device vectors.

Diagnostic Program

None

Related Documentation

DRV11-P Foundation Module User's Manual
(EK-DRV11-OP)
Field Maintenance Print Set (MP00119)
Microcomputer Interfaces Handbook (EB-20175-20)

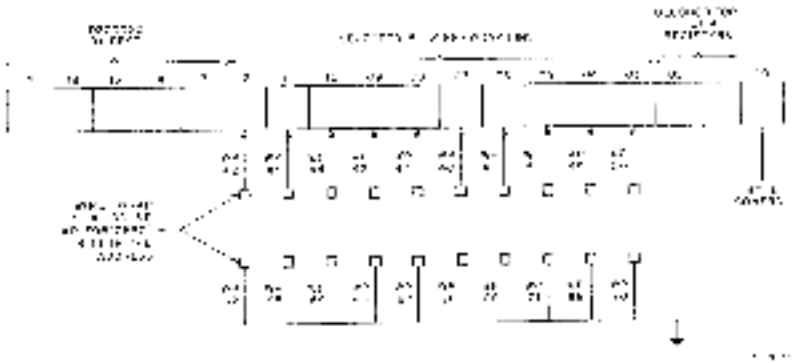


DRV11-P Foundation Module

Device Address Selection

The DRV11-P will respond to up to four consecutive addresses in the bank 7 area (addresses between 160000 and 177770). The register addresses are sequential by even numbers and are as follows:

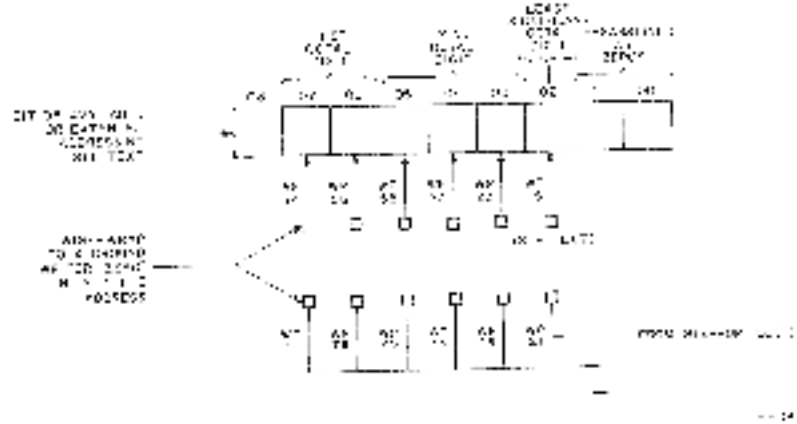
Register	BBS7	Octal Address
1	1	17xxx0
2	1	17xxx2
3	1	17xxx4
4	1	17xxx6



DRV11-P Device Address Select Format

Vector Address Selection

To cause separate vectors for an interrupt A and an interrupt B, jumper WP5 to WP21.



DRV11-P Vector Address Select Format

Bus Reply

The BRPLY L signal is normally issued within 65 ns (max.) of receiving either BDIN L or BDOUT L, depending on the bus cycle. If the user's interface requires more time before ending the bus cycle, the BRPLY L signal can be delayed up to a maximum of 1 µs by adding capacitor C39 across the solder lugs in the BRPLY delay circuit. The amount of capacitance required for various delays is given in the following table.

C39 R-C Delays for BRPLY

Resistor (Constant)	Capacitance (C39 Option)	Delay (Typical)*
680 Ω	0 pF	50 ns
680 Ω	100 pF	75 ns
680 Ω	120 pF	90 ns
680 Ω	470 pF	160 ns
680 Ω	560 pF	180 ns
680 Ω	650 pF	210 ns
680 Ω	1200 pF	340 ns

*Typical BRPLY delay with respect to BDOUT and BDIN

Maximum DRV11-P IC Density (All Areas)

IC Type	Max ICs
8 pin	122
8 pin	97
14 pin	61
16 pin	52
18 pin	44
20 pin	43
22 pin	6
24 pin	5
40 pin	3

User Wirewrap Pins

Wirewrap Pin	Function
WP1	SPARE IN – Spare input to the vector address multiplexer. This input can be used to read part of a control/status register.
WP2	SPARE IN – See WP1.
WP3	Ground for vector address bit V3. See WP28.
WP4	SPARE 1 – See WP1.
WP5	V2 – Vector address bit 02.
WP6	ENB CLK A H – ENB CLK A H is the clock input to the enable A flip-flop of the A interrupt logic. When ENB CLK A H goes high, ENB DATA A is clocked into the enable A flip-flop.
WP7	SPARE 2 – See WP1.
WP8	ENB B ST H – ENB B ST H is the status output from the enable B flip-flop of the B interrupt logic. When ENB B ST H is high, the enable B flip-flop is set.
WP9	BAKI L – Test point for the BIAK L bus signal. BIAKI L is the processor's response to BIRQ L and is daisy-chained such that the first requesting device blocks the signal propagation. Non-requesting devices pass the signal on as BIAKO L. The leading edge of BIAKI L causes BIRQ L to be unasserted by the requesting device.
WP10	D01 L – Test point for data/address bit one. Useful when testing the protocol logic. D01 is latched in the protocol logic at the asserted edge of BSYNC L. D01 and D02 are decoded to produce the SEL DEV outputs.
WP11	BWTBT L – Test point for the BWTBT bus signal, while BDOUT L is asserted. BWTBT L indicates a byte or word operation: BWTBT L asserted indicates byte operation; BWTBT L unasserted indicates word operation. BWTBT L decoded with BDOUT L and BDAL 0 L forms OUT LB L or OUT HB L.
WP12	R C X X – Test point for monitoring the delay of BRPLY.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP13	BSYNC H – Test point for the BSYNC L bus signal. BSYNC L indicates that the address is valid. At the assertion of BSYNC L, address information is trapped in four latches. While asserted, disables all outputs except the vector term of BRPLY. BSYNC L is held throughout the entire bus cycle.
WP14	DO0 H – One of 16 data or address lines from the transceivers for user applications. Address bit 00 is used for byte selection: 0 = low byte; 1 = high byte.
WP15	BDOUT L – Test point for the BDOUT L bus signal. BDOUT is a strobe signal to effect a data output transaction. BDOUT L is decoded with BWTBT L and BDAL0 to form OUT LB L and OUT HB L. BDOUT L also causes BRPLY L to be issued through the delay circuit.
WP16	IN WD L – In Word (IN WD) is used to gate input data from a selected register onto the LSI-11 bus. Enabled by BSYNC L and strobed by BDIN L.
WP17	DO1 H – One of 16 data or address lines from the transceivers for user applications.
WP19	INIT 0 L – An initialize signal (asserted low) for user applications.
WP18	INIT 0 H – An initialize signal (asserted high) for user applications.
WP20	BRPLY L – Test point for the BRPLY L bus signal. BRPLY L is generated by VECTOR H (vector term), or by BSYNC and DIN in combination with either BDIN L or BDOUT L. Capacitor C47 can be added by the user to extend the delay.
WP21	VEC HOST B H – Used to distinguish whether device A or device B is making a request. VEC HOST B H is asserted for device B requests and unasserted for device A requests.
WP22	V3 – Vector address bit 03. WP22 is used to select the state of vector address bit 03. When not wrapped to a ground pin, vector address bit 03 is a 1. When wrapped to WP3, vector address bit 03 is a 0.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP24	ENB DATA A H – Interrupt enable A data line. The level on this line, in conjunction with the ENB CLK A H (see WP8) line, determines the state of the A interrupt enable flip flop within the interrupt logic.
WP25	BIAKO L – Test point for the BIAKO L bus signal. BIAKO L is the daisy-chained signal that is passed by all devices not requesting interrupt service (see WP9).
WP26	ENB CLK B H – ENB CLK B H is the clock input to the enable B flip flop of the B interrupt logic. When ENB CLK B H goes high, ENB DATA B is clocked into the enable B flip-flop.
WP27	ENB DATA B H – Interrupt enable B data line. The level on this line, in conjunction with the ENB CLK B H (see WP 26) lines, determines the state of the B interrupt enable flip-flop within the interrupt logic.
WP28	RQST B H – When RQST B H is asserted, the bus request flip-flop for device B in the interrupt logic is enabled, and if BIRQ L becomes asserted if the interrupt enable flip-flop is set.
WP29	VECTOR H – Test point for VECTOR H. This signal causes BRPLY H (vector term) to be generated through a delay irrespective of BSYNC H and ENB H. VECTOR H also gates the vector address onto the LSI-11 bus via the vector address generator.
WP30	D02 L – Test point for data/address bit 2. Useful when testing the protocol logic. D02 is latched at the asserted edge of BSYNC H. D02 and D01 are decoded to produce the SEL DEV outputs.
WP31	ENB H – Test point for ENB H. This signal is the result of a comparison between the device address on the LSI-11 bus and the device address established by the user. When the addresses compare, ENB H is asserted and sent to the protocol logic.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP32	SEL DEV 1 L – One of four select signals that is true as a function of BDAL1 L and BDAL2 L if ENB H (see WP31) is asserted at the asserted edge of the RSYNC L. The four select signals indicate that a user's register has been selected for a data transaction. The select signals remain asserted until RSYNC L becomes unasserted.
WP33	SEL DEV 4L – See WP32.
WP34	SEL DEV 2L – See WP32.
WP35	SEL DEV 0L – See WP32.
WP36	OUT LB L – Out Low Byte is used to load (write) data into the low byte of a selected user register. See WP37.
WP37	OUT HB L – Out High Byte is used to load (write) data into the high byte of a selected user register. If used with OUT LB L, the higher, lower, or both bytes can be written. OUT HB L is enabled by BSYNC L and the decode of BWTBT L and BDAL0 L, and strobed by BDOUT L.
WP38	BIRQ L – Test point for the BIRQ L bus signal. This signal is asserted by a device needing interrupt service.
WP39	BDMGO L – This signal is generated by DMA devices as a result of arbitrating the BDMGI L line. Jumper W2 must be removed if the DRV11-P is to be used for DMA service.
WP40	BDMGI H – Used as a source for the BDMGI signal to drive the user's DMA request arbitration logic. See WP39.
WP41	ENB A ST H – ENB A ST H is the status output from the enable A flip-flop of the A interrupt logic. When ENB A ST H is high, the enable A flip-flop is set.
WP42	A12 – Used to select the user's device address along with WP45, 44, 43, 47, 48, 45, 51, 49, 50. When not wrapped to a ground pin, the particular device address bit will be a 1. When wrapped to a ground pin (WP42 for bit A12), the particular bit will be a 0.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP40	A09 – User's device address bit 09. The associated ground pin is WP63. See WP42.
WP44	A10 – User's device address bit 06. The associated ground pin is WP64. See WP42.
WP45	A11 – User's device address bit 08. The associated ground pin is WP65. See WP42.
WP46	A06 – User's device address bit 06. The associated ground pin is WP66. See WP42.
WP47	A08 – User's device address bit 08. The associated ground pin is WP67. See WP42.
WP48	A07 – User's device address bit 07. The associated ground pin is WP68. See WP42.
WP49	A04 – User's device address bit 04. The associated ground pin is WP69. See WP42.
WP50	A03 – User's device address bit 03. The associated ground pin is WP70. See WP42.
WP51	A05 – User's device address bit 05. The associated ground pin is WP17. See WP42.
WP52	SPARE 4 – See WP1.
WP53	V4 – Vector address bit 09. The associated ground pin is WP23. See WP 23.
WP55	V5 – Vector address bit 05. The associated ground pin is WP75. See WP23.
WP56	V6 – Vector address bit 06. The associated ground pin is WP76. See WP23.
WP57	IN03 H – One of 16 data or address lines to the transceivers for user applications.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP58	SPARE ENB 0 – SPARE ENB 0 and SPARE ENB 1 (WP59) both must be driven low to write data from SPARE inputs 0 through 7 to the LSI-11 bus via the transceiver. For 8 bit input applications, SPARE ENB 0 could be driven by one of the SEL DEV lines, while SPARE ENB 1 could be driven by IN WD L.
WP59	SPARE ENB 1 – See WP58.
WP60	IN00 H – See WP57.
WP61	D09 H – See WP17.
WP62	Ground for user's device address bit A12. See WP42.
WP63	Ground for user's device address bit A09. See WP42.
WP64	Ground for user's device address bit A10. See WP42.
WP65	Ground for user's device address bit A11. See WP42.
WP66	Ground for user's device address bit A08. See WP42.
WP67	Ground for user's device address bit A06. See WP42.
WP68	Ground for user's device address bit A07. See WP42.
WP69	Ground for user's device address bit A04. See WP42.
WP70	Ground for user's device address bit A03. See WP42.
WP71	Ground for user's device address bit A05. See WP42.
WP72	D04 H – See WP17.
WP73	Ground for vector address bit V4. See WP23.
WP74	Ground for vector address bit V5. See WP23.
WP75	Ground for vector address bit V6. See WP23.
WP76	Ground for vector address bit V7. See WP23.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP77	BBS7 H – Test point for the bank 7 select (BBS7) bus signal. This line is asserted by the bus master when an address in the upper 4K bank (28K–32K range) is placed on the LSI-11 bus.
WP78	SPARE 6 – See WP1.
WP79	D02 H – See WP17.
WP80	IN 02 H – See WP57.
WP81	D16 H – See WP17.
WP82	IN 13 H – See WP57.
WP83	D14 H – See WP17.
WP84	D15 H – See WP17.
WP85	D12 H – See WP17.
WP86	IN 12 H – See WP57.
WP87	D03 H – See WP17.
WP90	SPARE 7 – See WP1.
WP91	D13 H – See WP17.
WP92	IN 09 H – See WP57.
WP93	Not used.
WP94	TRANS ENB C L – Enables user's data to be placed onto the LSI-11 bus. Both TRANS ENB C and A (WP94 and WP120) and TRANS ENB D and B (WP95 and WP100) must be driven low prior to the processor's read data time.
WP95	TRANS ENB D L – See WP94.
WP96	IN 01 H – See WP57.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP97	VEC ENB H - Test point for VEC ENB H. This signal gates the vector address to the LSI-11 bus, provided that jumper W4 has not been removed. WP97 can be used as the source for VEC ENB H when adding an add l ess gate to the DRV11-P for vector address expansion up to 774
WP98	IN 05 H - See WP57.
WP99	IN 04 H - See WP17.
WP100	TRANS INB B L - See WP94.
WP101	IN 15 H - See WP57.
WP102	IN 14 H - See WP57.
WP103	Used to pull up the VEC ENB H line when jumper W4 is removed.
WP104	Not used.
WP105	Not used.
WP106	D08 H - See WP17.
WP107	D06 H - See WP17.
WP108	IN 11 H - See WP17.
WP109	D11 H - See WP57.
WP110	Not used.
WP111	Not used.
WP112	SPARE 5 - See WP1.
WP113	IN 08 H - See WP57.
WP114	Not used.

User Wirewrap Pins (Cont)

Wirewrap Pin	Function
WP110	BSYNC H – Test point for BSYNC P. At the asserted edge of this signal, address information is trapped in four latches. BSYNC H is the inverse of BSYNC L. See WP18.
WP116	Not used.
WP117	DO5 H – See WP17.
WP115	IN 07 H – See WP57.
WP119	IN 05 H – See WP57.
WP120	TRANS ENB A H – See WP94.
3 V	There are two 3 V source wirewrap pins on the DRV11-P. Each 3 V source can drive up to 3 TTL unit loads. These sources can be used for pulling up unused TTL inputs.

DUV11-DA SYNCHRONOUS SERIAL LINE INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.80	0.32	1.0	1.0	BC05C

Standard Addresses

Factory - Configurable in the range of 760000-777776. Refer to Appendix B.

Vector

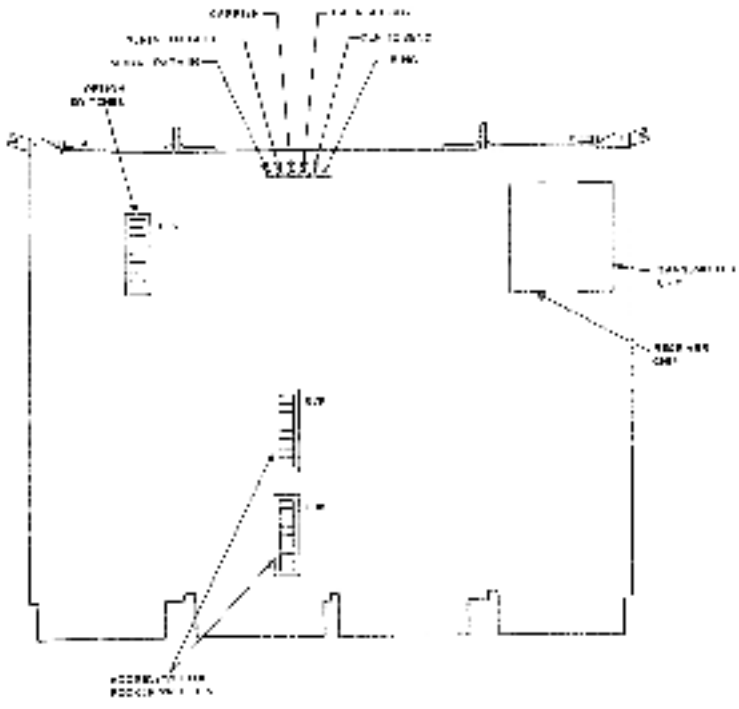
Factory - Configurable in the range of 300-770. Refer to Appendix B.

Diagnostic Programs

Refer to Appendix A.

Related Documentation

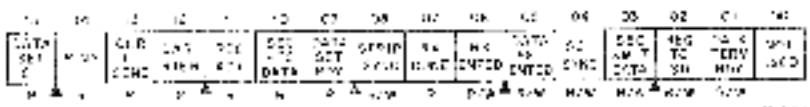
DUV11 User Interface Technical Manual (EK-DUV11-TM-001)
Field Maintenance Print Set (MP00287)
Microcomputer Interfaces Handbook (EB-20175-20)



DUV11-DA Switches

Guide for Setting Switches to Select Vector Address

Switch No. / Bit No.	3 / 3	4 / 7	5 / 6	6 / 5	7 / 4	8 / 3	Vector Address
		ON	ON				300
		ON	ON			ON	310
		ON	ON		ON		320
		ON	ON		ON	ON	330
		ON	ON	ON			340
		ON	ON	ON		ON	350
		ON	ON	ON	ON		360
		ON	ON	ON	ON	ON	370
	ON						400
	ON		ON				500
	ON	ON					600
	ON	ON	ON				700



Receiver Status Register (RXCSR)

Receiver Status Register Bit Description

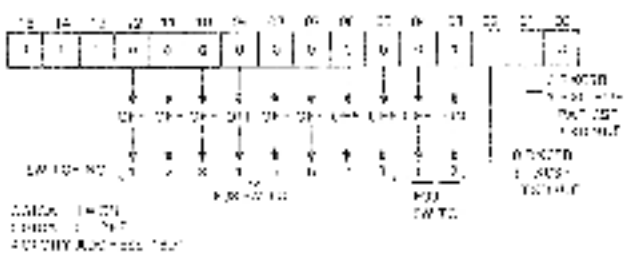
Bit	Function
15	Data Set Change (DAT SET CH) When set, this bit indicates a modem status change. This bit is set by a transition of any of the following lines. • Ring • Clear to send • Carrier • Secondary received data • Data set ready If bit 06 of this register is set, the setting of this bit will cause a RCVR interrupt. Read only; cleared by INIT, master reset, and the DT SEL 0 (RXCSR read strobe).

Receiver Status Register Bit Description (Cont)

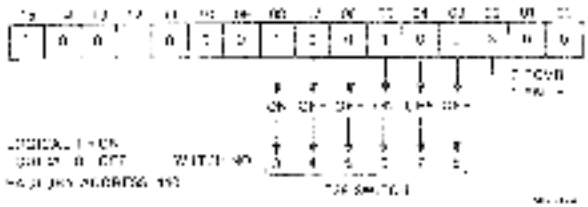
Bit	Function
14	Ring – This bit reflects the state of the modem ring line. When set, this bit indicates that a ring signal is being received from the modem. Read only.
13	Clear to Send (CLR TO SEND) – This bit reflects the state of the clear to send line from the modem. When set, this bit indicates that the modem is ready to accept data.
12	Carrier – This bit reflects the state of the modem carrier. When set, this bit indicates that the carrier is up. Read only.
11	Receiver Active (REC ACT) – When the internal synchronous mode is selected, this bit is set when the proper number of contiguous sync characters (either one or, normally, two) have been received. If external synchronous or asychronous mode is selected, this bit follows the state of the search sync bit (bit 04 of this register). Read only: cleared by INIT, master reset, and SCH SYNC (1) H (search sync) making 1 to 0 transition
10	Secondary Receive Data (SEC RCV DAT) – This bit reflects the state of the secondary receive data line from the modem. This bit provides a receive channel for supervisory data from the modem to the processor. Read only.
09	Data Set Ready (DAT SET RDY) – This bit reflects the state of the data line from the modem. When set, this bit indicates that the modem is powered up and ready. Read only.
08	STRIP SYNC – This bit determines whether sync characters received from the modem are to be presented to the program for reading. When this bit is set, received characters that match the contents of the sync register do not cause a RCVR interrupt provided no errors are detected, i.e., bit 15 of the RXDBUF is clear.
07	Receiver Done (RX DONE) – This bit is set when synchronization has been achieved and a character has been loaded into the RXDBUF, provided the STRIP SYNC bit is not set. If the STRIP SYNC bit is set and the received character is a sync character without errors, i.e., bit 15 of the RXDBUF is clear, this bit will not be set.

Switch Assignment for Option Switch Pack E55

Switch Number	Function
SW1	Optional clear – Switch ON enables CLR OPT, which is used to clear RXDBR bits 03, 02, and 01
SW2	Secondary transmit – Switch ON enables secondary data channel between the modem and DUV11.
SW3	Secondary receive – Switch ON enables secondary data channel between the modem and DUV11
SW4	Sync characters – Switch ON enables the receiver to synchronize internally upon receiving one sync character. The normal condition of receiving two sync characters exists when SW1 is off.
SW5	Special feature – Switch ON allows external clock to be internally generated, used when a modem is not being used.
SW6	Special feature – Optional feature is switched ON for programming control of data rate selection.
SW7	Maintenance clock – Switch ON enables the clock that is used for maintenance purposes only.
SW8	Not used



Device Address Selection



Interrupt Vector Selection

Guide for Setting Switches to Select Device Address

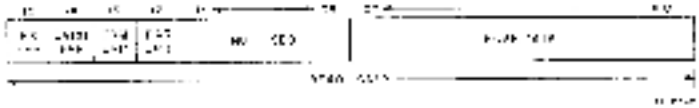
Module Switch No. / Bit No.	1 12	2 11	3 10	4 9	5 8	6 7	7 6	8 5	ESB 1 4	ESB 2 3	Device Address
										ON	760010
									ON		760020
									ON	ON	760030
								ON			760040
								ON		ON	760050
								ON	ON		760060
								ON	ON	ON	760070
							ON				760100
						ON					760200
						ON	ON				760300
					ON						760400
					ON		ON				760500
					ON	ON					760600
					ON	ON	ON				760700
				ON							761000
			ON								762000
			ON	ON							763000
		ON									764000

NOTE

ON means switch closed to respond to logical 1 on the bus.

Receiver Status Register Bit Description (Cont)

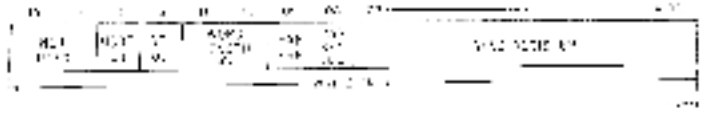
Bit	Function
06	Receiver Interrupt Enable (RX INTEN) – When set, allows a RCVR interrupt request to be generated when the RX done bit is set. Read/write; cleared by INIT and master reset.
05	Data Set Interrupt Enable (DAT SET INTEN) – When set, allows a RCVR interrupt request to be generated when the DAT SET CH bit is set.
04	Search Sync (SCH SYNC) – When set in the internal synchronous mode, enables the RCVR synchronization logic and causes the RCVR to start comparing incoming data bits to the contents of the sync register in an attempt to recognize a sync character. Read/write, cleared by INIT and master reset.
03	Secondary Transmit Data (SEC XMIT) – This bit reflects the state of the secondary transmit data line to the modem. This bit provides a transmit channel for supervisory data from the processor to the modem.
02	Request to Send (REQ TO SD) – When set, this bit causes the request to send line to the modem to be reasserted. The request to send line is a control lead to the modem. This line must be asserted before the interface can transmit data to the modem.
01	Data Terminal Ready (DATA TERM RDY) – When set, this bit indicates that the interface is powered up, programmed, and ready to receive data from the modem. Setting this bit causes the data terminal ready line to the modem to be asserted. The data terminal ready line is a control lead for the modem communication channel. When asserted, it permits the interface to be connected to the channel. Read/write; optionally cleared by INIT and master reset



Receiver Data Buffer (RXDBUF)

Receiver Data Buffer Bit Description

Bit	Function
15	Receiver Error (RX ERR) – This bit is set whenever one of the three receiver error bits is set (logical OR of bits 14, 13, and 12). Read only; cleared only when bits 14, 13, and 12 are cleared.
14	Overrun Error (OVRN ERR) – When set, this bit indicates that the processor has failed to service the RX DONE flag within the time required to load another character into the RXDBUF, .6 . (1/baud rate) X (bit/char) seconds. Hence, the previous character was overwritten (lost). This condition indicates the loss of at least one character. Read only; cleared by INIT, master reset, and DTI SEL 2 (RXDBUF read all/be)
13	Framing Error (FRM ERR) – When set, indicates that character received was not followed by a valid stop bit. This error only occurs in the isochronous mode of operation. Read only; cleared by INIT, master reset, and DTI SEL 2.
12	Parity Error (PAR ERR) – When set, indicates that the parity of the received character does not agree with the parity programmed (odd or even). If parity is not programmed, this bit is always cleared.
07-00	Receiver Data (RCVR DATA) – This register holds the received character for transfer to the program. The buffer is right justified for 5, 6, 7, or 8 bits. If parity is received it is also loaded into the buffer at the next vacant higher order bit position. Therefore, if a 5-bit character plus parity is framed by the RCVR, the parity bit would be loaded into bit position 05 in the RXDBUF and presented to the program for reading. If an 8-bit character plus parity is framed, the parity bit would not be presented to the program for reading. Read only buffer; cannot be cleared. INIT or master reset sets the buffer to all 1s. Reading the RDXBUF causes the RXDONE bit in the RXCSR to clear.



Parameter Status Register (PARCSR)

Parameter Status Register Bit Description

Bit	Function
13,12	Mode Select (MODE SEL) These bits control the mode of operation. Modes are selected as follows. Mode — Bit 13 — Bit 12 Internal Synchronous — 1 — 1 External Synchronous — 1 — 0 Isochronous — 0 — 0 Illegal (Not Used) — 0 — 1 Write only.
11, 10	Word Length Select (WORD LEN SEL) These bits control the length of characters received and transmitted by interface. Word length (not including parity) is selected as follows. Bit/Char — Bit 11 — Bit 10 5 — 0 — 0 6 — 0 — 1 7 — 1 — 0 8 — 1 — 1 Write only.
09	PAR ENB – If this bit is set, parity for each character is (parity enable) generated by the XMTR and checked by the RCVR. If character length is fewer than eight bits, the parity bit for received data is loaded into the RXDBUF for reading by the program. If bad parity is detected at the RCVR, the parity error flag is set (bit 12 of the RXDBUF). Write only.

Parameter Status Register Bit Description (Cont)

Bit	Function
05	Parity Sense Select (PAR SENSE) — When the parity enable bit (bit 08 of this register) is set, the sense of the parity (odd or even) is controlled by this bit. When this bit is set, even parity is generated by the XMTR and checked for by the RCVR (the program does not have to provide a parity bit to the XMTR). When this bit is cleared, odd parity is generated and checked. Write only.
07–00	Sync Register — This register contains the sync character. The sync character is used by the RCVR to detect received sync characters and thereby achieve synchronization. The sync character is used as a fill character by the XMTR when operating in the synchronous mode. Fill characters are operating in the synchronous mode. Fill characters are transmitted when the program fails to provide characters to the XMTR fast enough to maintain continuous transmission. I.e., (1 /baud rate) X (bit/char) seconds = 1/2 (bit time).

Transmitter Status Register (TXCSR)

Transmitter Status Register Bit Description

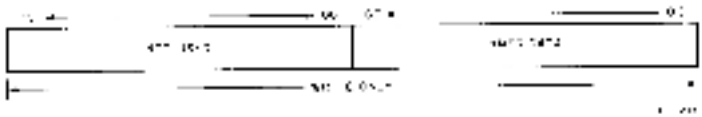
Bit	Function
15	Data Not Available (DNA) — This bit is set by the XMTR when a bit character is transmitted. This applies only to the synchronous mode of operation and is caused by the program response to a TX DONE interrupt request. The processor response to TX DONE must be within (1/Baud rate) X (bit/char) seconds = 1/2 (bit time), or not, the fill character is transmitted. It can be of this register is set; setting this bit causes an XMTR interrupt request. Read only; cleared by INIT, master reset, and DTI SEL 4 (TXCSR read strobe)

Transmitter Status Register Bit Description (Cont)

Bit	Function
14	Maintenance Data (MAINT DATA) – This bit is used in the internal loop and external loop maintenance. Read/write bit; cleared by INIT or master reset.
13	Single Step Maintenance Clock (SS CLK) – This bit is used in the internal loop and external loop maintenance modes by diagnostic program to simulate the XMTR and RCVR clocks. Read/write; cleared by INIT or master reset.
12, 11	Maintenance Mode Select 01 and 00 (MS01-MS00) – These bits are used to select the normal mode of operation or one of three maintenance modes. Modes are selected as follows. Mode / Bit 12 / Bit 11 Normal / 0 / 0 Internal Maintenance Loop / 0 / 1 External Maintenance Loop / 1 / 0 System Test / 1 / 1 Read/write; cleared by INIT and master reset.
10	Receiver Input (RX INP) – This bit monitors the RCVR input in the internal loop and external loop maintenance modes. Read only.
09	Master Reset (MSTRST) – This bit is used to generate a CLR (clear) pulse, which initializes the registers and the XMTR and RCVR and inhibits the BRPLY L (bus reply) signal. This bit remains set at 1 for only 3 µs after being set. Read/write.
07	Transmitter Done (TX DONE) – This bit is set by INIT and master reset and when the first bit of the character contained in the XMTR register is placed on the XMTR output line. If bit 06 of this register is set when this bit is set, an XMTR interrupt request is generated.
06	Transmitter Interrupt Enable (TX INTEN) – When set, this bit allows an XMTR interrupt request to be generated by the TX DONE bit.

Transmitter States Register Bit Description (Cont)

Bit	Function
05	Data Not Available Interrupt Enable (DNA INTEB) - When set, this bit allows a XMTR interrupt request to be generated by the DNA bit.
04	Send - When set, this bit enables the XMTR and transmission will start when a character is loaded into the TXDBUF. This bit must remain set until the entire message is transmitted. If not, transmission of the character currently in the XMTR register is completed and the XMTR will enter the idle state. Read/write: cleared by INIT and master reset.
03	Half Duplex (HALF DUP) - When this bit is set, operation will be in the half-duplex mode. In this mode, the RCVR is disabled whenever bit 04 of this register is set.
00	Break - When this bit is set, the serial XMTR output DS SERIAL DATA OUT H is held in the space (constant low) condition; otherwise, operation is normal. This bit is used by the diagnostic program in the internal loop or external loop maintenance modes to inhibit the XMTR output while inputting data to the RCVR via bit 14 of this register. Read/write: cleared by INIT and master reset.



Transmitter Data Buffer (TXDBUF)

Transmitter Data Buffer Bit Description

Bit	Function
07 - 00	Transmitter Data (XMTR DATA) - This register is loaded by the program with the character to be transmitted. Character length is from five to eight bits. The character is right justified. If a parity bit is enabled, it is generated by the transmitter. Write only. INIT or master reset places all 1s in this register.

DZV11 ASYNCHRONOUS MULTIPLEXER

The DZV11 (M7957) is a four line, asynchronous program controlled multiplexer with modem control on all lines.

Amps		Bus Loads		Cables
+5	1P	AC	DC	
1.15	0.39	1.26	1.0	BC11D

Standard Addresses

Floating Configurable within the range of 160000 - 177770.

Register	Mnemonic	Address
Control and Status Register	CSR	16XXX0
Receiver Buffer	RBUF	16XXX2
Line Parameter Register	LPR	16XXX2
Transmitter Control Register	TCR	16XXX4
Modem Status Register	MSR	16XXX6
Transmit Data Register	TDR	16XXX6

XXX — selected in accordance with floating device address convention. Refer to Appendix B.

Vectors

300 - 777 in accordance with floating interrupt vector assignments. Refer to Appendix B.

Diagnostic Programs

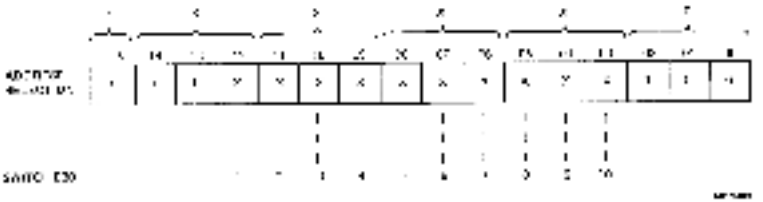
Refer to Appendix A.

Related Documentation

DZV11 Asynchronous Multiplexer Technical Manual (EK-DZV11-TM)
DZV11 Print Set (MP-00462-00)
Microcomputer Interfaces Handbook (EB-20175-20)

NOTES

1. Use H325 test connector to test individual lines.
2. Use H329 test connector to test module without cables.

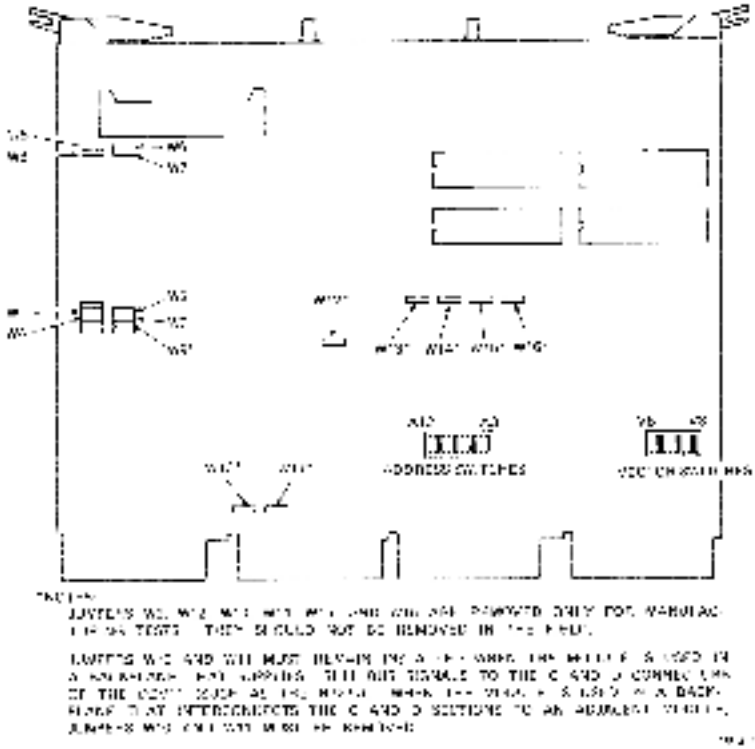


Address Switches

Vector Switches

Modem Control Jumpers

There are eight jumpers used for modem control. The jumpers labeled W1 through W4 connect Data Terminal Ready (DTR) to Request To Send (RTS). This allows the DZV11 to assert both DTR and RTS if using a modem that requires control of RTS. These jumpers must be installed to run the onsite and external test diagnostic programs. The remaining four jumpers: W5 through W8, connect the Forced Busy (FB) lines to the RTS leads. With these jumpers installed, the assertion of an RTS lead places an ON or BUSY signal on the corresponding forced busy lead. The forced busy jumpers (W5 through W8) are cut out unless the modem requires them.



M7957 Jumper Locations

Jumper Configuration

Jumper	Connection	Line
W1	DTR to RTS	05
W2	DTR to RTS	02
W3	DTR to RTS	01
W4	DTR to RTS	00
W5	RTS to FB	03
W6	RTS to FB	04
W7	RTS to FB	01
W8	RTS to FB	00

CSR Bit Assignments

CSR Bit Assignments

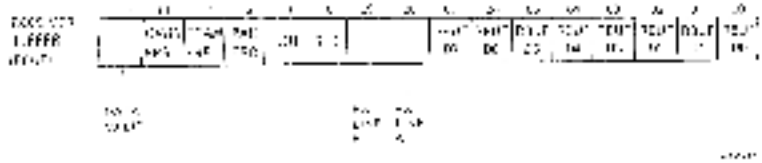
Bit	Function
00–02	Not used.
03	Maintenance – This bit when set loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. Read/write
04	Master Clear – When written to a 1, this bit generates "Initialize" within the DZV11. A read-back of the CSR with this bit set indicates initialize in progress within the device. This bit is self-clearing. All registers, silos, and UARTS are cleared with the following exceptions 1. Only bit 15 of the receiver buffer register (valid data) is cleared; the remaining bits, 00–14, are not. 2. The high byte of the transmitter control register is not cleared by master clear. 3. The modem status register is not cleared by master clear.
05	Master Scan Enable – This read/write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, transmitter ready (CSR 07) is inhibited from setting and the received character buffers (silos) are cleared.
06	Receiver Interrupt Enable – This bit, when set, permits setting CSR 07 or CSR 15 to generate a receiver interrupt request. Read/write

CSR Bit Assignments (Cont)

Bit	Function
07	Receiver Done – This is a read-only bit that sets when a character appears at the output of the first-in/first-out (FIFO) buffer. To operate in interrupt per character mode, CSR 06 must be set and CSR 12 must be cleared. With CSR 06 and CSR 12 cleared, character flag mode is indicated. Receiver done clears when the receiver buffer register (RBUF) is read or when master scan enable (CSR 05) is cleared. If the FIFO buffer contains an additional character, the receiver done flag stays cleared a minimum of one microsecond before presenting that character.
08–09	Transmitter Line – These read-only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when transmitter ready (CSR 15) is set, and are cleared when master scan enable is cleared. Bit 08 is the least significant bit.
10–11	Not used.
12	Silo Enable Alarm – This is a read/write bit. When set, it enables the silo alarm counter to keep count of the number of characters stored in the FIFO buffer. The counter is cleared when the silo alarm enable bit is cleared. Conditioning of this bit must occur prior to any character reception.
13	Silo Alarm – This is a read-only bit set by the hardware after 16 characters have been entered into the FIFO buffer. Silo alarm is held cleared when silo alarm enable (CSR 12) is cleared. This bit is reset by a read to the receiver buffer register and does not set until 16 additional characters are entered into the buffer. If receiver interrupt enable (CSR 06) is set, the occurrence of silo alarm generates a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the silo alarm bit.
14	Transmitter Interrupt Enable – This bit must be set for transmitter ready to generate an interrupt. Read/write.

CSR Bit Assignments (Cont)

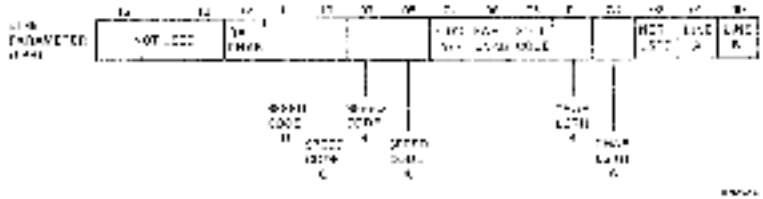
Bit	Function
15	Transmitter Ready – This bit is read only and is set by the hardware. This bit sets when the transmitter scan stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The transmitter number, specified in CSR 08 and CSR 09, is valid only when transmitter ready is set. Transmitter ready is cleared by any of the following conditions: a. when master scan enable is cleared b. when the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09 c. at the conclusion of the load instruction of the transmit data register (low byte only). If additional transmit lines require service, transmitter ready reappears within 1.4 microseconds from the completion of the transmit data register load instruction. The occurrence of transmitter ready with transmitter interrupt enable set, generates a transmitter interrupt request.



RBUF Bit Assignments

RBUF Bit Assignments

Bit	Function
00-07	Received Character – These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not known.
08-09	Received Character Line Number – These bits contain the line number upon which the received character was received. Bit 08 is the least significant bit.
10-11	Not used.
12	Parity Error – This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
13	Framing Error – This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
14	Overrun Error – This bit is set if the received character was processed by a character that was lost due to the inability of the receiver scanner to service the DART receiver holding buffer on that line.
15	Valid Data – This bit, when set, indicates that the data present in bits 00-14 is valid. This bit permits the use of a character handling program that takes characters from the FIFO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is 0.



LPR Bit Assignments

LPR Bit Assignments

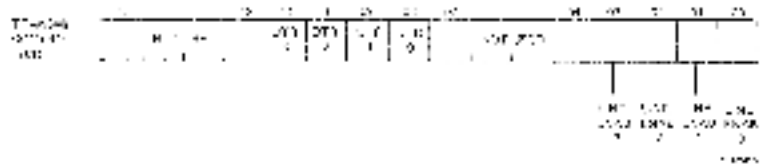
Bit	Function
00-01	Parameter Line Number – These bits specify the line number for which the parameter information (bits 0–12) is to apply. Bit 00 is the least significant bit.
02	Not used. Must always be written as a 0 when specifying the parameter line number. Writing this bit as a 1 extends the parameter line number field into nonexistent lines. Parameters for lines 00–03 are not affected.
03-04	Character Length – These bits are set to receive and transmit characters of the length (excluding parity) as shown below. 04 05 0 0 5 bit 0 1 6 bit 1 0 7 bit 1 1 8 bit
05	Stop Code – This bit sets the stop code length (0 = 1 unit stop; 1 = 2 unit stop or 1.5 unit stop if a five-level code is employed).
06	Parity Enable – If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
07	Odd Parity – If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line, and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.

LPR Bit Assignments (Cont)

Bit	Function
08–11	Speed Code. The state of these bits determines the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
	1	0	0	4800
	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Invalid

12	Receiver Enable. This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit is cleared following a BINIT or device master clear.
13–15	Not used.



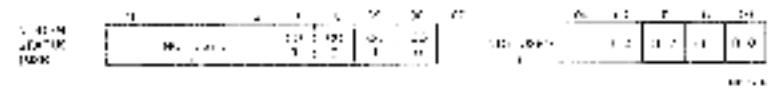
TCR Bit Assignments

The TCR bits are represented in bits 00–03. These bits are read/write and are cleared by BINIT or device master clear. Bits 04–07 are not used and read as 0.

The high byte of the TCR register contains the write-only modem control bits, the Data Terminal Ready (DTR). Bit designations are as follows.

Bit	Name
08	DTR line 00
09	DTR line 01
10	DTR line 02
11	DTR line 03
12–15	Unused, read as 0

Assertion of a DTR bit puts an ON condition on the appropriate modem circuit on that line. DTR bits are read/write and are cleared only by BINIT. Jumpers have been provided to allow the RTS circuits to be asserted with DTR assertions.

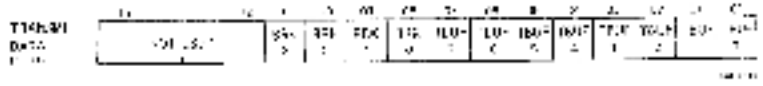


MSR Bit Assignments

Modem Status Register

The Modem Status Register (MSR) is a 16-bit read-only register. A read of this register results in the status of the readable modem control leads: ring and carrier. The ON condition of a modem control lead is interpreted as a logical 1. Bits 04–07 and 12–15 are unused and read as a 0. Remaining bit designations are as follows.

Bit	Name	Bit	Name
00	Ring line 00	08	Carrier line 00
01	Ring line 01	09	Carrier line 01
02	Ring line 02	10	Carrier line 02
03	Ring line 03	11	Carrier line 03
04–07	Unused; read as 0.	12–15	Unused; read as 0.



TDR Bit Assignments

Transmit Data Register

The Transmit Data Register (TDR) is a byte- and word-addressable, write-only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when transmitter ready (CSR 15) is set. The character that is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the TDR is designated as the break control register.

Each of the four multiplexer lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12 - 15 are unused. Setting a break bit forces that line's output to space. This condition remains until cleared by the program. This register is cleared by BINIT or device master clear. The break control register can be utilized regardless of the state of the device maintenance bit (CSR 03).

FPF11 FLOATING POINT PROCESSOR

GENERAL

The FPF11 is contained in one quad-height module, M8188, which becomes an integral part of the CPU when installed. The module is installed in the backplane slot adjacent to the CPU for systems using the PDP-11/23. It connects to the CPU by a ribbon cable that plugs into the socket designated for the optional floating-point processor chip. The FPF11 does not connect to the system bus, and therefore, has no effect on bus loading. The FPF11 can execute the entire PDP-11 floating-point instruction set.

Power Requirements

+5 V (±5%) at 5.5 A

Diagnostic Programs

Refer to Appendix A

Related Documentation

FPF11 Floating-Point Processor Technical Manual (EK-FPF11-TM)
Field Maintenance Print Set (MP01885)

CONFIGURATION

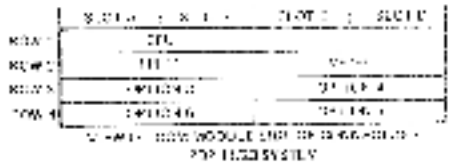
The FPF11 module is configured to operate in either an LSI-11 type bus or the Unibus backplane. The module jumpers and the jumper configuration for each bus follows. The position of the module in respect to the CPU is shown for different type systems and the interconnection of the 40-conductor cable is also shown.

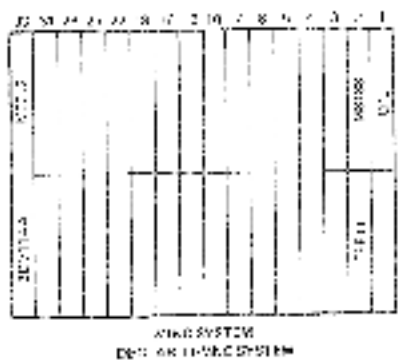
FPF11 Jumper Configurations

	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12
Unibus	R	R	I	S	R	I	I	I	I	R	I	I
LSI-11 bus	I	I	R	I	I	I	R	R	I	I	R	R

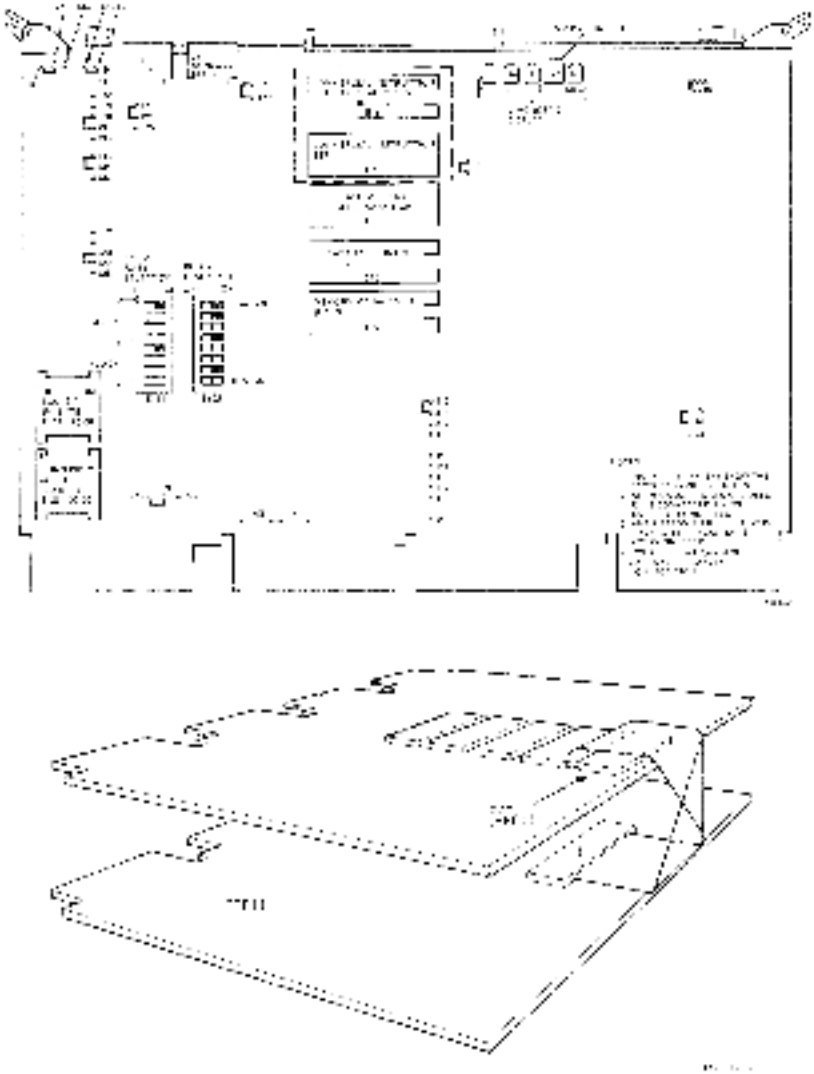
R — removed, I — installed

FPF11 Jumper Locations





FPF11 Module in Various Configurations

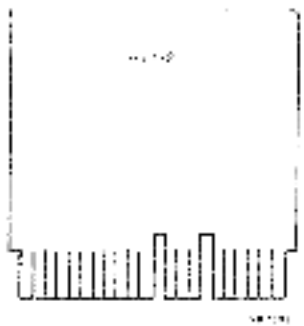


FPF11 Cable Layout

G7272/M8659 LSI-11 GRANT CARDS

G7272 GRANT CARD (Q-BUS)

The G7272 grant card is etched identically to that of the M8659 grant card and is identified with four notches and finger end shape. The G7272 grant card is installed into an open LSI-11 slot and is used to pass the bus grant signals on the Q-Bus.

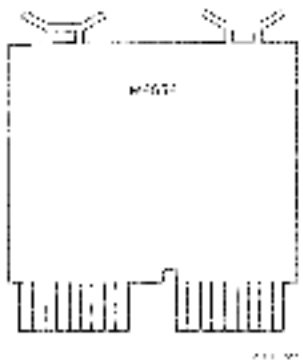


G7272 Grant Card

M8659 LSI-11 BUS GRANT CARD (VT71 GRANT CARD)

The M8659 grant card is inserted into an unoccupied backpane slot in a serial daisy chain backplane system.

The LSI-11 grant card is used to allow grant signals to pass on the LSI-11 bus, as open slots in a daisy-chained bus are not permitted. The H8659 grant card looks similar to a double-height module with handles with only the pins necessary to pass the grant signals on the C Bus.



H8659 Grant Card

IBV11-A LSI-11 INSTRUMENT BUS INTERFACE

Amps		Bus Loads		Cables
+5	+12	AC	DC	
0.3A (1.5 max.)	0	1.77	1.0	BN11A used from IBV11-A to first instrument. BNC1A used to any additional instruments.

Addresses

	Standard	MINC
IBS (Instrument Bus Status Register)	160160	174420
IBD (Instrument Bus Data Register)	160152	174412

Vectors

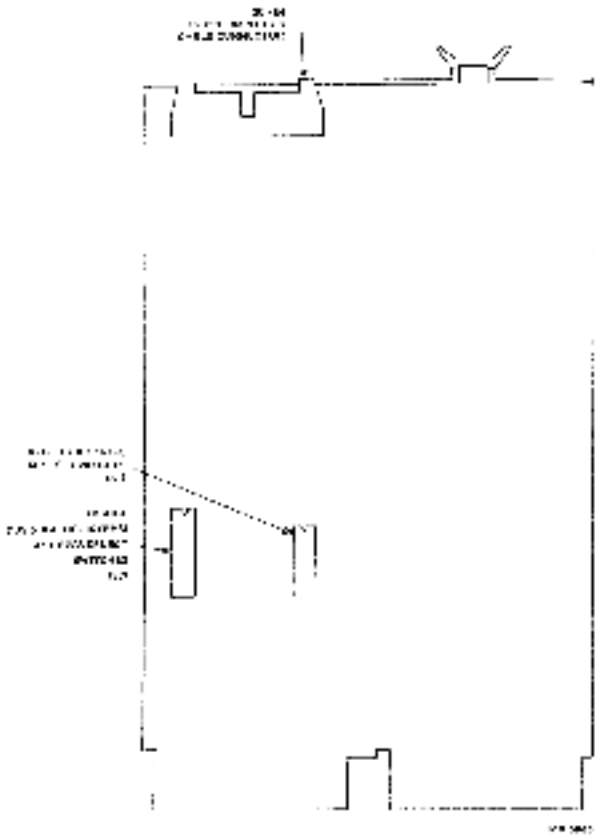
Error	420
Service request	424
Command and talker	430
Listener	434

Diagnostic Program

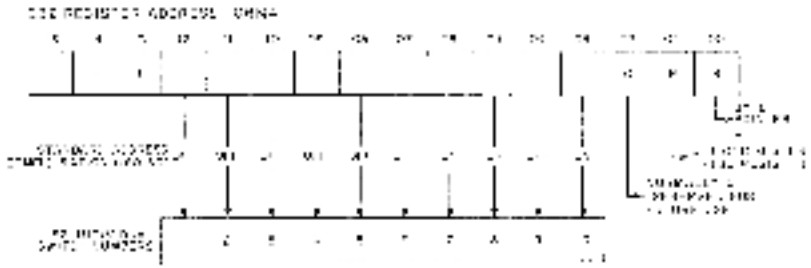
Refer to Appendix A.

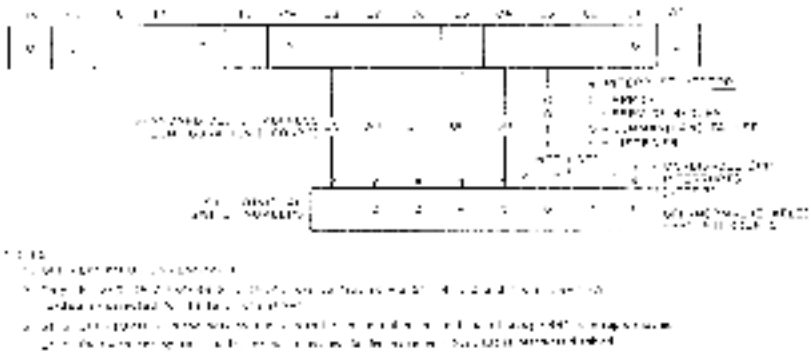
Related Documentation

IBV11-A LSI-11 Instrument Bus Interface User's Manual (EK-IBV11-UM)
Digital Interface for Programmable Instrumentation (IEEE Std. 488-1975)
Field Maintenance Print Set (MP00274)
Microcomputer Interfaces Handbook (EB-20175-20)



IBV11-A Address Hits





IBV11-A Interrupt Vector Addresses

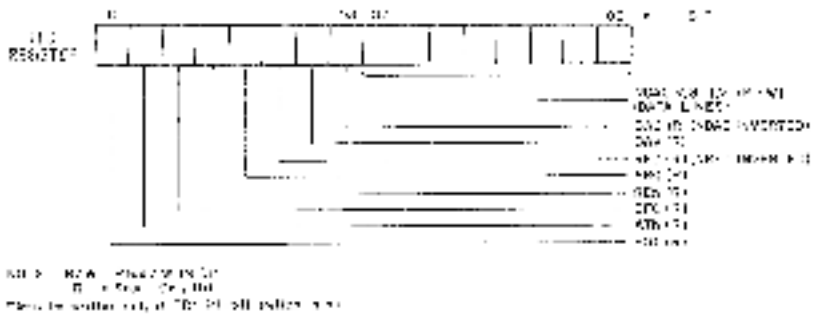
Instrument Bus Status Register

ISG Register Bits Description

Bit	Function
00	Take Control Synchronously (TCS) – Set and cleared under program control to enable or disable the IBV11-A controller-in-charge function by taking control synchronously or by requesting ATN. Setting TCS will cause NRFD to be asserted for at least 500 ns before DAV is checked. ATN is then asserted when DAV is not asserted. NRFD must be unasserted and CMD is set 500 ns (minimum) after ATN is asserted. TCS is cleared by BINIT L and IFC.
01	End or Poll (EOP) – Set and cleared under program control to assert or unassert the EOI line. EOP is cleared by BINIT L and IFC.
02	Remote On (REM) – Set and cleared under program control to assert or unassert the REM line. REM is cleared by BINIT L and IFC.
03	Interface Bus Clear (IBC) – When set, the leading edge of IBC produces IFC for 1.25 (approximately). At the end of IFC, TCS is automatically asserted and IBC is automatically cleared. IBC is cleared by BINIT L.
04	Listener On (LON) – Set or cleared by the program to enable or disable the IBV11-A listener function. When LON is set and the DAV line is asserted, the IRS LNR bit (bit 08) becomes set. When LON is cleared, the IBV11-A ignores DAV. LON is cleared by BINIT L and IFC.
05	Talker On (TON) – Set or cleared by the program to enable or disable the IBV11-A talker function. TON is cleared by BINIT L and IFC.
06	Interrupt Enable (IE) – Set and cleared by the program to enable or disable the IBV11-A talker function. TON is cleared by BINIT L and IFC.
07	Accept Data (ACC) – Set and cleared by the program. When ACC is cleared, reading a data byte from the DIO lines will automatically assert the DAC line and clear the LNR bit (bit 08). When ACC is set, the program must clear the low byte of the IBD register in order to clear the LNR status bit and assert the DAC line.

IBS Register Bits Description (Cont)

Bit	Function
08	Listener Ready (LNR) – When set, LNR indicates that the IBV11-A has a data or command byte that is ready for reading from the low byte of the IBD. LNR is set when LON is set and the DAV line becomes asserted. LNR is cleared by reading the IBD low byte if ACC is cleared, or by clearing the IBD low byte if ACC is set. LNR is also cleared when LON is cleared by the program and by BINIT L and IFC.
09	Talker Ready (TKR) – When set, TKR indicates to the LSI-11 processor that the IBV11-A is ready for the next data byte to be transmitted to the DIO lines via the low byte of the IBD register.
10	Command Done (CMD) – When set, CMD indicates to the LSI-11 processor that the IBV11-A is ready for the next command byte to be transmitted to the DIO lines via the low byte of the IBD register.
11	Not used. Read as 0.
12	Not used. Read as 0.
13	Error 1 (ER1) – Set whenever a conflict occurs between the instrument bus ATN, IFC, or REN lines and their IBV11-A control hardware. When set, ATN H is cleared and cannot be set. This condition can only be cleared by clearing the cause of the error. ER1 can occur when another system controller is connected to the instrument bus. The error can then be suppressed by setting the ER1 inhibit switch (S1-6) on the IBV11-A module to the ON position. If the IBV11-A is the only system controller, set S1-6 to the OFF position.
14	Error 2 (ER2) – Set when the IBV11-A tries to send a data or command byte while there is no active listener or command acceptor on the instrument bus. ER2 is cleared by clearing both the TCN and TCS bits.
15	Service Request (SRQ) – This bit always displays the status of the instrument bus SRQ line. It may be written (set and cleared) if the ER1 inhibit switch is set.



Instrument Bus Data Register

IBD Register Bit Description

Bit	Function
15–8	Instrument bus control line status. The program can look for the signal status of all eight control signals by reading this byte. Note that DAC (bit 08) and IRFD (bit 10) are inverted with respect to the actual instrument bus signal lines.
7–0	Instrument bus data input/output. The program can read or write to this register byte to receive or transmit command or data bytes over the instrument bus. Bits 7–0 correspond to DIO lines 8–1.

KD11 LSI-11 PROCESSOR MODULES

Processor option designations and processor module numbers do not have a one-for-one correspondence. This section describes processors both in terms of option designations (KD11-X) and module numbers (M7264-XX). When replacing chip sets, check both the number on the handle and chip revision on the board. The jumpers are defined in this section; however, the "Systems Configurations" section presents the general rules for configuring refresh reply. For details on differences between various revisions of the processor modules, refer to Appendix B of the *Microcomputer Processor Handbook*, EB-18461-20. For all commercial products systems, refer to the *DIGITAL Datasystem 320 Family Service Manual*, EK-DDS03-SV-001, available in hard copy or microfiche.

Processor Model Designations

KD11-F

Processor with 4K RAM:

M7264 Mostek 4096	M7264-EB Mostek 4027
M7264-AB Intel® 2104	M7264-FB TI-C 4027
M7264-GB Fujitsu 8224	M7264-HB Motorola 4027
M7264-DB Intel 2104-A	M7264-JB Fujitsu 8227

KD11-H (M7264-YA)

Processor without 4K RAM

EIS/FIS option can be added:
- Etch Revs C and D use KEV11
- Etch Rev D uses KEV11-H (EIS only)
- Etch Revs E and F use KEV11-A

KD11-L

Processor with on-board 4K RAM and EIS/FIS.
- Etch Rev C or D KD11-F plus KEV11 or
- Etch Rev E or F KD11-F plus KEV11-A

KD11-N

Processor without on-board 4K RAM and with EIS/FIS.
Etch Rev C or D KD11-H plus KEV11 or
Etch Rev E or F KD11-H plus KEV11-A

KD11-P

Processor with on-board 4K RAM and with CIS
Etch Rev E or F M7264-BB plus KEV11-CA

KD11-Q

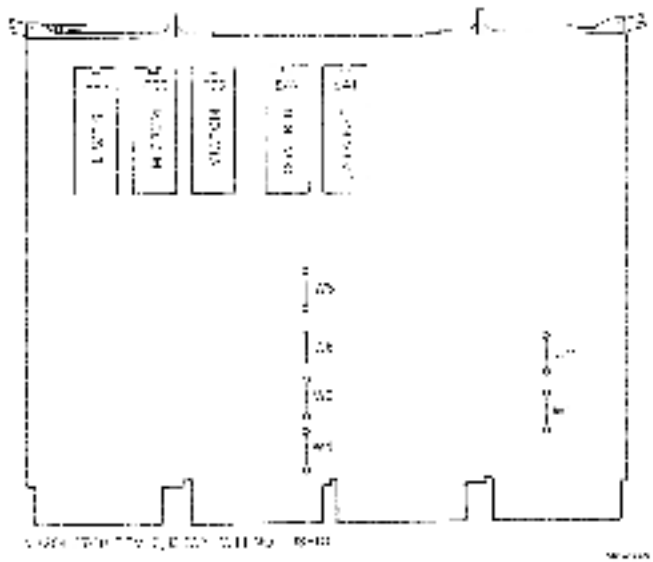
Processor without on-board 4K RAM and with CIS
Etch Rev E or F M7264-YB plus KEV11-CA

M7264 Specifications

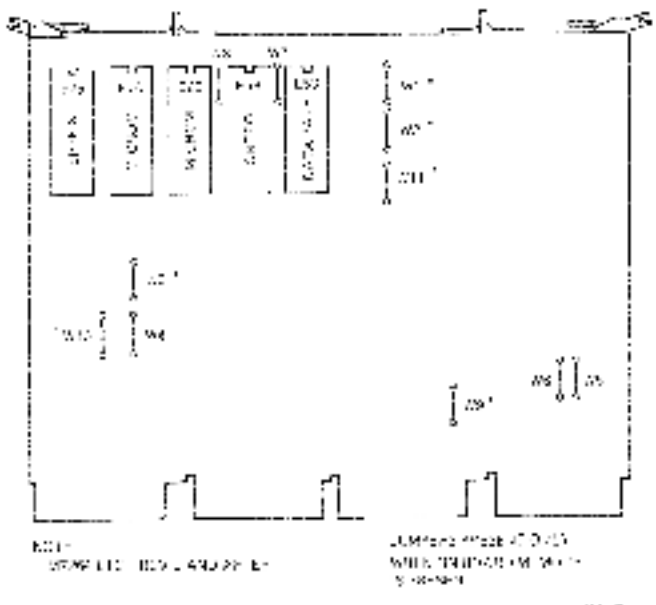
Size	Quad height module 26.6 cm (10.5 inches) × 22.8 cm (8.9 inches)
Power:	+5 V ±5%, 1.8 A; +12 V ±3%, 0.8 A
Bus Loads:	AC — 2.4 unit loads
	DC — 1 unit load
Environment:	DEC STD 102 Class C

Related Documentation

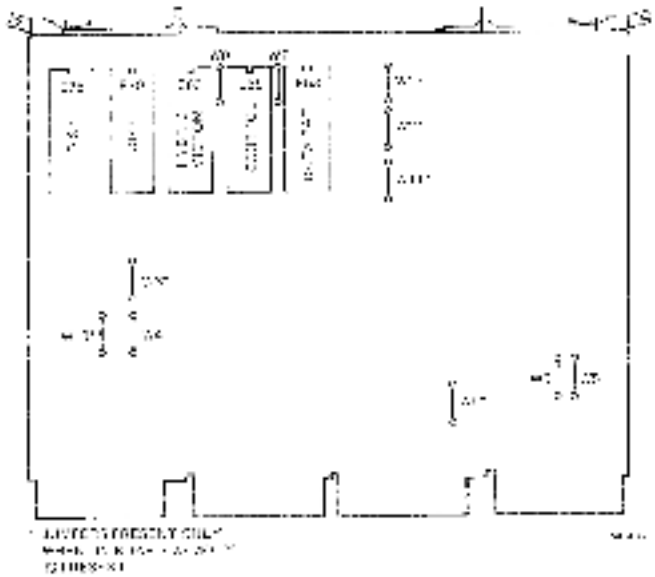
Microcomputer Processor Handbook (EB-18451-20)
KD11-F Field Maintenance Print Set (MP-00049-00)
KD11-H Field Maintenance Print Set (MP-00050-00)
KD11-P Field Maintenance Print Set (MP-00264-00)
KD11-Q Field Maintenance Print Set (MP-00357-00)
KD11-WA Field Maintenance Print Set (MP-00569-00)
LSI-11 Maintenance Card (EK-LSI11-MC)



M7264 Revisions C,D



M7264 Revision E



M7264-BB DIBOL Processor

M7264-BB Jumpers

Jumper	Function
W1	Insert to select resident memory bank 1
W2	Insert to select resident memory bank 0
W3	Remove to enable event line (LTC) interrupt.
W4	Remove to enable processor controlled memory refresh.
W5, W6	**Power-Up Modes** Jumpers Mode W6 W5 Mode Selected 0 R R PC at 24 and PS at 26, or halt mode 1 R I ODT microcode. 2 I R PC at 173000 for user bootstrap 3 I I Special processor microcode (not implemented).

M7254-BB Jumpers (Cont)

Jumper	Function
W7	Factory-selected biasing voltage. Installed for VDATA — VROM.
W8	Factory-selected biasing voltage. Installed for VCTL — VROM.
W9	Remove to enable reply from resident memory.
W10	Remove to enable reply from resident memory during refresh.
W11	Enable on-board memory select.

Processor Module Jumper States

	(LSI-11 With 4K On-Board Memory)		(LSI-11 Without On-Board Memory)	
Jumper	KD11-F, -L	KD11-P	KD11-H, -J, -M, -R, -S, -U	KD11-Q
W1	R	R	R	R
W2	I	I	R	R
W3	R	R	R	R
W4	R	I	I	I
W5	R	R	R	R
W6	R	I	R	I
W7	*	*	*	*
W8	*	*	*	*
W9	R	R	I	I
W10	R	R	R	R
W11	I	I	R	R

*May vary with ECO level. Do not alter.

Diagnostic Programs

The following diagnostic programs are for use with LSI-11 processors except for the limitations noted.

VKAA?? — LSI-11 basic instruction test.

VKAB?? — LSI-11 Extended Instruction Set (EIS) test. This program can only be run on LSI-11 CPUs with the KEV11 (EIS/FIS) or KEV11-CA (DIBOL instruction set) options installed.

VKAC?? — LSI-11 Floating Point Instruction (FIS) test. This runs only on LSI-11 CPUs that have the KEV11 (EIS/FIS) option (M7264BS).

NOTE

The KD11-F (or Q) supports EIS (DIBOL Instruction Set) and FIS (Extended Instruction Set) but not FIS (Floating Instruction Set). Therefore, FIS test (-VKACA0) will not run on a D322 or D324.

VKAD?? — LSI-11 traps test. This diagnostic auto-sizes for the EIS, FIS and DIBOL options.

- Older versions (Rev B1 and below) require the setting of a bit in the software switch register if EIS, FIS, or DIBOL is present.
- Rev A diagnostics will not run on D322 or D324 systems because of the DIS instructions.

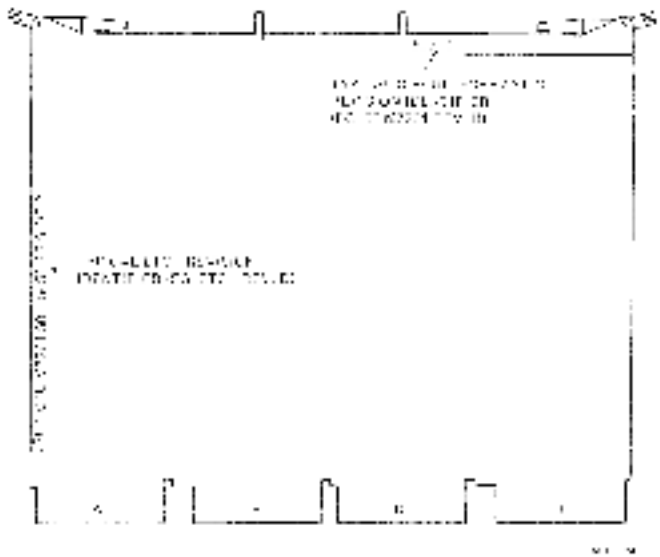
NOTE

See Appendix A for XXDP++ multimedia assignments.

VKAH?? — Basic system exercises. Tests serial line 0/1, memory, processor, RS-F-S, clock, and both floppy disks under various conditions. Software switch register must be set for options.

VKAI?? — DIS move and string instruction tests. This diagnostic tests the DIBOL instruction set. The CPU must have KEV11-CA (DIS) option installed. Not D322, 324.

VKAJ?? — DIS decimal instruction tests. This diagnostic tests the DIBOL instruction set. The CPU must have the KEV11-CA (DIS) option installed. Not D322, 324.



M7264 Revision Identifiers

M7264-YA Etch Rev C

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1511 B-51	21-11549-00	-5.1	
CONTROL	CP 1521 B-151	23-001C4-01	-5.1	2004 pattern
MICROM-0	CP 1531 B-3010	23-065A6-01	-5.1	Without ECO 2
	CP 1531 B-3010	23-065A6-01	-5.1	With ECO 2
MICROM-1	CP 1541 B-3007	23-067A6-01	-5.1	
DIS/FIS (Emergency)				
KEYS	CP1631 B-301 5	23-001A6-01	-5.1	
RAMs				
M7264	Mostek	21-11749	-9	Without ECO 2A
M7264-YA	None			With ECO 2A

M7264-AB, M7264-YA Etch Rev D

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-01	21-11049-00	−5.1	2004 pattern
MICROM-0	CP 1631 B-3010	23-08A5-01	5.1	
MICROM-1	CP 1631 B-3007	23-087A5-01	5.1	
RIS/FIS (if present)				
KEV11	CP 163[illegible] B-3015	23-01A5-01	−5.1	
KEV11-C (CIS only)	CP 1621 B-12	12-090A5-01	3.9	
RAMs				
M7264	Mostek	21-11748	−5	Without ECO 4
M7264	Mostek 4096	21-12726-00	−5.1	With ECO 4
M7264-AB	Intel 2104	21-12958-01	5.1	With ECO 7
M7264-YA	None			Not present

M7264-AB, M7264-YA Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 F-09	21-11549-0	3.9	
	PQ 1611 H	21-[illegible]579-00	3.9	With ECO 11
CONTROL 2004 pattern	CP 1621 B-17S	23-002C4	−3.9	With ECO 12
	CP 1621 B-18S	23-001C3	−3.9	Without ECO 12
MICROM-0	CP 1631 B-10S	23-001B5	3.9	
MICROM-1	CP 1631 B-07S	23-002B5	3.9	
RIS/FIS (if present)				
KEV11-A	CP 163[illegible] B	23-003B5	−3.9	
RAMs				
M7264	Mostek 4096	21-12726-00	−5.1	
M7264-AB	Intel 2104	21-12958-01	−5.1	
M7264-YA	None			Not present

M7264-SB, M7264-YB Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-51	21-11949	0.1	Without ECO 5
	CP 1611 B-39	21-11949-01	3.9	With ECO 5
	PC 1611	21-11949-00	3.9	With ECO 21
CONTROL				
2001 pattern	CP 1621 B-151	23-001CP-01	−5.1	With ECO 5
2007 pattern	CP 1521 B 480	23-001C5	−3.9	Without ECO 12
	CP 1621 H 173	23-002C1	3.9	With ECO 12
	CP 1621 H	23-003C5	3.9	With ECO 21*
MICROM-3/1	CP 1531 B-3010	23-003A5-01	5.1	Without ECO 16
		23-001H6	3.9	With ECO 16
		23-001B6	−3.9	With ECO 12
		23-001B6	−3.9	With ECO 16
DIS (KEV11-CA)				
DIS 2		23-001H5	3.9	5025 pattern
DIS 3		23-001B5	−3.9	5021 pattern
RAMs				
M7264-BB	Mostek 4036	21-12726-00	5.1	
M7264-YB	None			Not present

*This part of ECO 21 applies to M7264-BB and -YB variations only.

M7264-CB, M7264-DB Etch Rev E

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	-3.9	
	FO 1611 H	21-16579-00	-3.9	With ECO 21
CONTROL	CP 1621 B-173	23-00104	-3.9	2007 pattern
MICROM 0	CP 1651 B-103	23-00186	-3.9	
MICROM 1	CP 1651 B-073	23-00205	-3.9	
FIS/FIS (1 present) KEV11-A	CP 1651 B	23-00380	-3.9	
RAMs				
M7264-CB	Fujitsu 8224	21-13707-01	-3.9	
M7264-DB	Intel 2104A	21-13795-01	-3.9	

M7264, M7264-AB, -CB, -DB, -FB, -HB, -JB Etch Rev F

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CP 1611 B-39	21-11549-01	-3.9	
	FO 1611 H	21-16579-00	-3.9	With ECO 21
CONTROL	CP 1621 B-173	23-00204	-3.9	2007 pattern
MICROM 0	CP 1651 B-103	23-00186	-3.9	
MICROM 1	CP 1651 B-073	23-00205	-3.9	
FIS/FIS (1 present) KEV11-A	CP 1651 B-139	23-00380	-3.9	
RAMs				
M7264	Mostek 4096	21-12726-00		350 ns
M7264-AB	Intel 2104	21-12944-01		350 ns
M7264-CB	Fujitsu 8224	21-13707-01	-3.9	350 ns
M7264-DB	Intel 2104A	21-13795-01	-3.9	350 ns
M7264-FB	Mostek 4027	21-13733-01		200 ns
M7264-HB	DEC 4027	21-12914-01		200 ns
M7264-IB	Motorola 4027	21-14114-01		200 ns
M7264-JB	Fujitsu 8227	21-14475-01		200 ns

M7264-BC, M7264-YB Etch Rev F

Chip	Vendor Number	DEC Number	V_{BB}	Comments
DATA	CF 1611E-39	21-11949-01	−3.0	
	PQ [illegible] F	21-[illegible]	3.9	With ECO 21
CONTROL	CF 1621E-173	23-[illegible]CA	3.9	
	[illegible]	23-[illegible]CA	3.9	With ECO 21
MICROM 0	CF 1651E-101	23-[illegible]BC	3.9	
MICROM 1				Not present
DS				
KEY [illegible] CA				
DS 2		23-[illegible]AB	3.9	
DS 3		23-[illegible]AB	3.9	
RAMs				
M7264-BC	Mostek 4096	21-[illegible]6-CC	5.1	350 ns
M7264-YB	None			Not present

Circuit Schematic/ECO History

Etch Rev	CS Rev	ECO No.	Change
C	C		(Basic mode)
D	D	1	Change value of Cb in clock pulse generator circuit from 150 pF to 47 pF.
E	E	2	1. Logic changed to clock DPPLY into reply flip flop with trailing edge of timing signal. 2. Logic changed to disable BRSYN for the duration of HDMO L or BSACK L assertion. 3. BAUN L signal decoded and applied to backplane. 4. ECO 2A creates M7264-YA.
F	F	3	Logic changes for etch Rev C boards.
H	H	4	Circuit changes implemented to provide [illegible] V. Documentation updated by ECO 4A.

Circuit Schematic/ECO History (Cont)

Etch Rev	CS Rev	ECO No.	Change
F	J	5	New module layout. (DMA synchronization logic changed.) Add jumpers for read-only memory reply and refresh reply. Add factory jumpers for V_{BB} selection. Logic change to allow external selection of resident memory. Add factory adjustment (R16) for setting refresh clock to 1.5 ms. Terminate bus lines AA1, AR1, AC1, AD1, and BP1. Replace E53, E55, H61, E70 with −3.0 V chips.
E	K	6	1. Change DMA synchronization logic. 2. Terminate E46-12, −15 to −3 V.
E	L	7	Correct documentation errors.
E	M	8	Change R41 from 22Ω to 27Ω. Change R46 from 10Ω to 22Ω.
C	D1,E1	9	Logic change implemented to inhibit BBS7 L during memory refresh.
C	F1,J1		Canceled by ECO 16A.
F	N		
C D E	D2,F2 F2,J2 P	10	1. Logic change implemented to inhibit BBS7 L during memory refresh. 2. Removed DMA/refresh alternate cycle scheme. 3. Changed M7264-BB to −3.0 V (9) chips. 4. Documentation corrected by ECOs 16A and 16B.
E	R	11	Created M7264-YB.
F	S	12	Phased out 23-00180 CS control chip and replaced it with 23-00204.
F	T	13	Replaced 23-00180 microm with 23-00206.
F	U	14	1. Created M7264-CB, -DB.

Circuit Schematic/ECO History (Cont)

Etch Rev	CS Rev	ECO No.	Change
E	U	14	2. Operating frequency changed to 2.5 MHz min.–2.651 MHz max
E	V	15	Routed IF CLR to pin AF1 from CH1.
E	W	16	Replaced 23-002B5 microm with 23-003B6.
F	Y	17	Released etch Rev F.
			2. Refresh 625 ± 20 Hz adjustment.
			3. Pins 22 and 24 of E73 tied to phase 2 and phase 4 for WCS.
			4. SRUN buffered to CH1, AF1
			5. BPOK line deglitched
			6. Chip set changes (see data sheets).
			7. Documentation updated by ECO 17A.
G	DX,EX, FX,HX	18	Added resistors R24, R25, R26, and R27 to 0 pull up BDAL16 and BDAL17 (formerly BAD16 and BAD17). This ECO is normally required in systems using DRV11-Bs or MSV11-Ds.
F	Z	19	Created M7264-EB, -FB, -HB, and -JB.
F	AA	20	Create M7264-YC document changes
			Delete R50.
			2. Add R60.
F	AB	21	Use 1611H (21-15579-00) data chip instead of 1611A (21-14348-01).
			Use 23-002C3 control chip instead of 23-002C4
			Change R45 from 22Ω to 16Ω and clock frequency to 2.47 MHz for -YB and -DD only

KDF11-AX 11/23-A MICROCOMPUTER

The KDF11-A is a 16-bit, double-height, multilayered, microcomputer module. The processor (microcomputer) uses the existing LSI-11 bus. The KDF11 is backward compatible with existing LSI-11/2 processors and I/O interfaces. Memory management is included as a standard feature.

The KEF11-A option (not part of a standard system) is a floating point processor extension chip that mounts to a socket on the KDF11-A processor module. The chip option can execute the PDP-11/34 (FP11) floating point instruction set. These instructions supplement the integer arithmetic instructions (for example, MUL, DIV) in the basic instruction set.

Four 40 pin chip sockets mounted on the KDF11-A module are to accommodate the following chip functions.

- Memory Management Unit (MMU)
- Spare
- Floating point (optional)
- Data/control unit (the basic processor)

KDF11 Specifications

Identification:	M8186
Size:	Double-height module
Power Requirements:	5 V ± 5% 2.0 A −12 V ± 5% 0.2 A
Bus Loads:	AC 2 unit loads DC 1 unit load
Environmental:	DEC STD 102 Class C

Diagnostic Programs
The following diagnostic programs are used with the LSI-11/23 processor, except for the limitations noted.

JKOB8O	CPU trap and EIS diagnostics
JKDA8O	Memory Management Unit (MMU)
	Requires KEF11-A option (21-15542-00/01) installed in IC socket E57
JKDCAC	Floating point diagnostic - Part 1
JKDDAO	Floating point diagnostic - Part 2

The floating tests require the KEF11 option to be installed on the board. These diagnostics expect the CPU to be functional. Therefore, the JKDB?? diagnostic should be run before the floating point diagnostics.

NOTE
See Appendix A for multimedia assignments.

Related Documentation
Microcomputer Processor Handbook (EB-18451-20)
KDF11-A Field Maintenance Print Set (MP-00734-00)
LSI-11, PDP-11/23 Reference Card (EK-17598-20)

KEF11-A (Floating Point Option Installation)
The KEF11AA floating point option resides in two MOS/LSI chips contained on one 40-pin hybrid package (57-00001-01). The KEF11-AA requires the memory management chip to be present along with the base MOS/LSI chips, since all of the floating point accumulators and status registers are in the MMU chip. Chapter 10 in the *Microcomputer Processor Handbook*, EB-18451-20 covers the KEF11 in detail.

Early revision M8186 requires an ECO (M8186-S-0007) to accommodate the KEF11-AA option. Modules at hardware revision A0 (A etch) or C1 (C etch) and below, require this change.

Remove E57 (DEC PN 21-15542-00)
Install E57 (DEC PN 21-15542-01)
Remove E21 (DEC PN 57-00000-00)
Install E21 (DEC PN 57-00000-01)

NOTE
Mark Rev A0 or C2 on the module handle to indicate the new revision, depending on original etch rev.

After the ECO is installed, install the KDF11-AA option (57-00001-01) in IC socket position E39.

KDF11 Variations

AA -LSI-11/23 16-bit microcomputer with KTF11-AA memory management (M8186)

AB -KDF11-AA with KEF11-AA (floating point option)

AC -KDF11-AA without KTF11-A

CD -KDF11-AC with MXV11-AC and MSV11-CD (32K words)

HD -KDF11-AC with MSV11-DD (48K words)

HF -KDF11-AA with two MSV11-DD (64K words)

HH -KDF11-AA with three MSV11-DD (96K words)

HK -KDF11-AA with four MSV11-AA (128K words)

RE -KDF11-AA with MXV11-AC, MSV11-DD (48K words) and QJV13-DZ (RT-11 V 4.0, License only)

RF -KDF11-AA with MXV11-AC, two MSV11-DD (80K words) and QJV13-DZ

RL -KDF11-AA with MXV11-AC, three MSV11-DD (112K words) and QJV13-DZ

SE -KDF11-AA with MXV11-AC, MSV11-DD (48K words) and QJB42-DZ (RSX11-S V 2.2, license only)

SG -KDF11-AA with MXV11-AC, two MSV11-DD (80K words) and QJB42-DZ

SJ -KDF11-AA with MXV11-AC, three MSV11-DD (112K words) and QJB42-DZ

XA -KDF11-AA with two MSV11-ED (64K word) (parity)

XB -KDF11-AA with four MSV11-ED (128K word) (parity)

Data/Control (DC302, DC304) Hybrid
The data chip (DC302) contains the PDP-11 general registers, the processor status word (PS), several working registers, the arithmetic and logic unit (ALU), and conditional branching logic. The DC302 chip

- performs all arithmetic and logical functions
- handles all data and address transfers with the LSI-11 bus (except relocation, which is handled by the MMU)
- generates most of the signals used for interrupt communication and external system control.

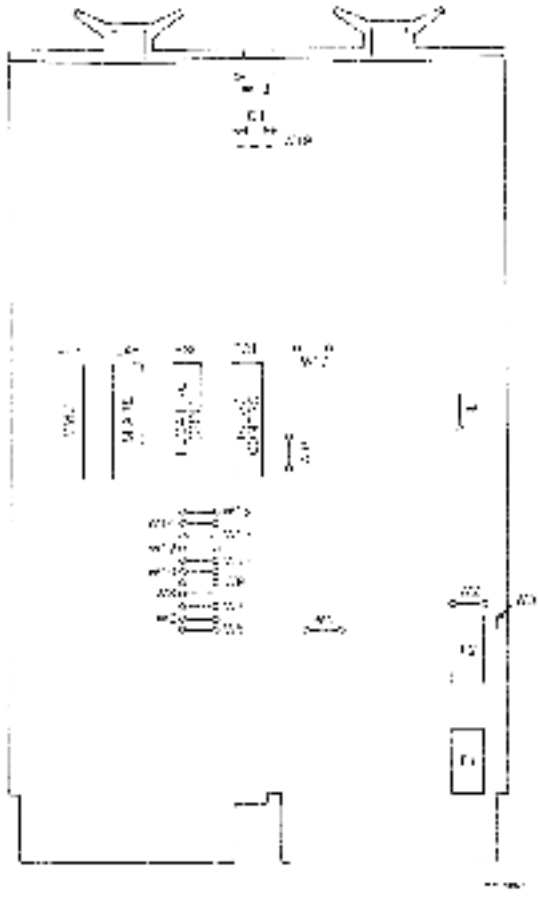
Control Chip
The control chip (DC303) contains the microprogram sequence logic and 640 words of microprogram storage in programmable logic arrays (PLA) and read only memory (ROM) arrays. The control chip accesses the appropriate microinstruction in the PLA or ROM and sends it along the MIB to the data and MMU chips for execution. The control chip accesses only its own storage.

MMU Chip
The MMU chip serves two purposes:

- It provides the memory management function.
- It provides storage for the KEF11-AA floating point accumulators and status registers.

This chip provides user and kernel mode address relocation of 18 bits. Sixteen-bit virtual addresses are relocated via mapping registers (PARs) to the appropriate 18-bit physical address for the transmission to the external system bus.

The MMU chip is controlled by information received on the microinstruction bus (MIB) from both the data chip and the control chip and by several discrete control inputs. The KDF11-AX can operate without the MMU chip; however, the memory would be limited to 32K words and the floating point registers would not be available.



KDF11-AA Rev A Jumpers

M8186 (Etch Rev A) Jumper Configurations

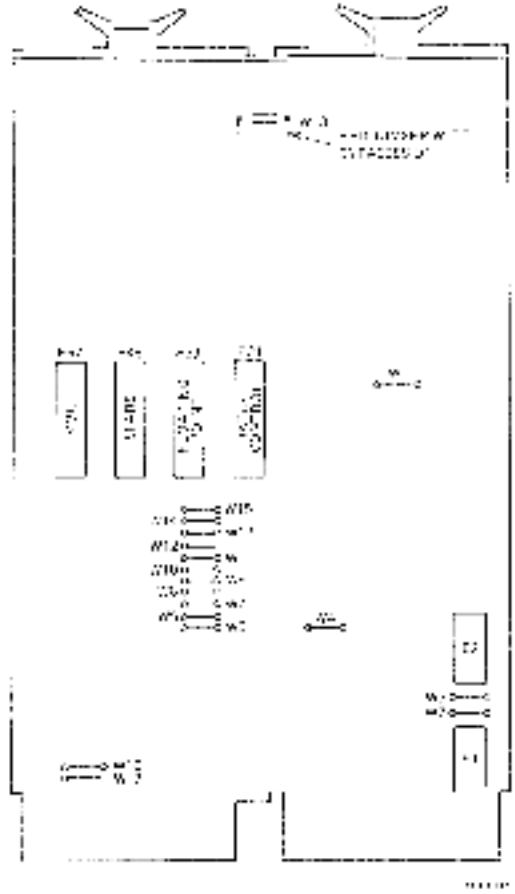
Jumper	Name	Function	Factory Set
W1	Master clock	In = enabled	In
W2	Reserved for DEC use	Removed = do not install	Out
W3	Reserved for DEC use	Installed = do not remove	In
W4	Event line enable	Out = enabled	In
W5, W6	Power-up mode	(*See footnote.)	W5 = In W6 = Out
W7	Halt/trap option	In = traps to 10_8 on HALT	In
		Out = enters console ODT on HALT	
W11	Bootstrap address	In = powers up to bootstrap address 173000_8	In
		Out = powers up to address specified by W9–W15	
W9–W15	User-selectable bootstrap address	W9–W15 correspond to address bits 9 through 15, respectively, in mode 2	W9–W15: In
		In = logic 1 Out = logic 0	

*Power-Up Mode Selection

Mode	Name	W5	W6
0	PC @ 24 (octal) ODT	Out In	Out Out
2	Bootstrap	Out	In
3	Extended microcode	In	In

M8186 (Etch Rev A) Jumper Configurations (Cont)

Jumper	Name	Function	Factory Set
W15	Reserved for DEC use	Factory-installed; do not remove	In
W17	Reserved for DEC use	Factory-installed; do not remove	In
W18	Reserved for DEC use	Factory-installed; do not remove	In



KDF11-A Rev C Jumpers

M8186 (Etch Rev C) Jumper Configurations

Jumper	Name	Function	Factory Set
W1	Master clock	In – Enabled	In
W2	Reserved for DEC use	Removed – do not install	Out*
W3	Reserved for DEC use	Installed – do not remove	In*
W4	Event line enabled	Out – enabled	In
W5, W6	Power-up mode	(**See footnote.)	W5 – In W6 – Out
W7	Halt/trap option	In – traps to 10_8 on HALT Out – enters console ODT on HALT	Out
W8	Bootstrap address	In – powers up to 173000_8 Out – powers up to address specified by W9–W15	In
W9–W15	User selectable bootstrap address	W9–W15 correspond to address bits 9 through 15, respectively In – logic 1 Out – logic 0	W9–W15 In

*Refer to EDC-MAINT-ROOOO

** Mode Name W5 W6

Mode	Name	W5	W6
0	PC @ 24 PS @ 26	Out	Out
1	Console ODT	In	Out
2	Bootstrap	Out	In
3	Extended arithmetic	In	In

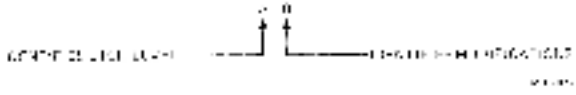
M8130 (Etch Rev C) Jumper Configurations (Cont)

Jumper	Name	Function	Factory Set
W16, W17	Reserved for DEC use	Factory-installed; do not remove	W16, W17 In
W18	Wake-up circuit	Out = disabled In = enabled	In

Hardware Revision System

All other modules have the etch revision level coded into the etch and the circuit schematic revision level coded on the module handle; the M8186 has both codes stamped on the module handle.

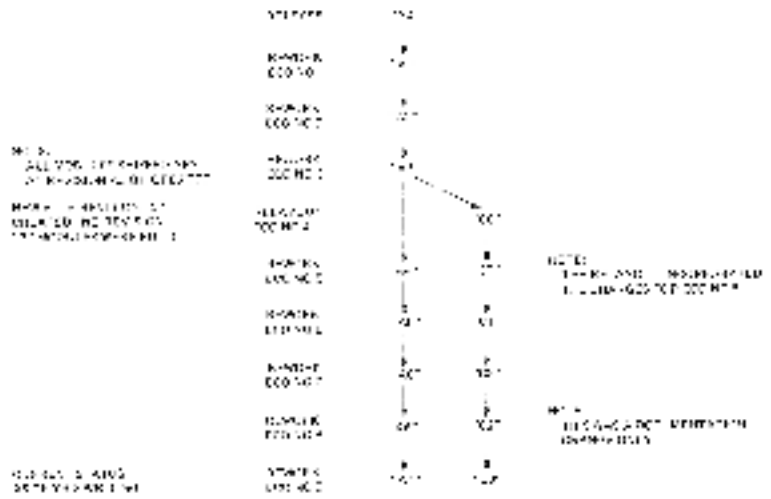
The revision identifier is a two-field alphanumeric designation. The first field indicates the etch revision. The second field indicates the modifications to the etch.



M8186 Revision Identifier

The M8186 started as hardware revision A0, as shown above; that is, etch revision "A" with no modifications or work. As ECOs were released calling for rework (not a new etch), the hardware revisions were released and the etch revision field was incremented from A to B to C. No etch revision "B" for the M8186 modules was built so the revision level appears to change from "A" to "C" via ECO no. 4. Etch revision "C" modules had ECO no. 5 incorporated on them before being released, therefore their hardware revision status did not change with ECO no. 5.

The hardware revision history of the M8186 is shown on page



M8186 ECO Summary

11/23 (M8186) ECO Summary

The following table details the ECOs issued since the first M8186 shipment. These ECOs are coded "M8186 M-UUUX", where "X" is the ECO number shown below.

ECO No.	Problem	Quick Verify
1	Too many wires and etch cuts; new etch needed. Note that the jumper locations change for each revision of "C".	Module handle will be stamped "C-" (where "-" refers to the ECO revision)
5	Possible parity errors when using parity memories (MSV11-E, etc.)	Check for etch cut to ET pins 16 and 18.

NOTE

Implementation of this ECO impacts configurations. This ECO is discussed in detail below.

6	The internal wake-up circuit defeats the sequencing provided by standard DEC power supplies. This ECO should be installed when the M8186 is used with same.	Red jumper wire is installed in parallel with J1.
7	CTL/DAT hybrid (57-00000-01) and MMU (54-10642-00) were not compatible with KEF11-AA floating point option. The FP registers in the MMU were inaccessible, and the CTL/DAT data path caused intermittent errors in floating point instructions.	CTL/DAT should be 57-00000-01 and MMU should be 54-10642-01 for floating point compatibility. *Coordinate with ECO M8186-0009.*
8	MMU (54-10642-01) was included as part of the M8186 module. It should have been specified as an option that could have added to the M8186 from the M8186. ECO KDF11A-0001 adds it back in as the option level (M8186-AB, KDF11-AA). This is a documentation change only.	Modules in systems may or may not have MMU depending upon which option they represent. Spares, however, are ordered as modules and will not have MMUs. MMUs must be ordered separately.

ECO No.	Problem	Quick Verify
9	1. No jumper table in print set (documentation change only).	1. Prints contain a jumper table.
	2. Metal oscillator may short to adjacent components	2. Oscillator has nylon spacer. Manufacturing change only. Do not retrofit in field.
	3. Possibility of worst case MMU timing violations. Change configuration of W2 and W3 to adjust timing. This ECO must be installed. a. when ECO M9186-0007 is call in b. when a microcode option (i.e., KEF11) is installed c. when a 40-pin IC (DTL/DAT, MMU or KEF11) is replaced d. whenever unexplained system crashes occur	3. Module will have W2 removed and W3 in. On etch Rev "A" modules, W3 is installed by soldering a jumper wire from E7 pin 3 to E2 pin 15.

ECO No. 5

A circuit was included in the KDF11-A to compensate for a design limitation in the MSV11-C and MRV11-C. That is, these devices do not use BBSY to deselect themselves. It is this limitation that causes the requirement to jumper deselect memory in the 28K–32K range on LSI-11s; otherwise the MSV11-C would respond to peripheral addresses. Unfortunately, the parity problem with MSV11-E could not be fixed except by disabling this circuit. As a result, after this ECO is installed (hardware revision "A4" and above, and all etch revision "C"), the MSV11-C cannot be configured in the 28K–32K (words) or in the 124K–128K (word) range. MRV11-C cannot be configured in the 24K–32K (word) range on mapped systems when used in the "direct" or "window" addressed modes. On unmapped systems (11/03 and KDF11-AC) it may be configured in the I/O page.

KDF11-BA 11/23-B MICROPROCESSOR

GENERAL

The KDF11-B is a 22-bit, quad-height microprocessor module. The module has a microprocessor, memory management unit (MMU), a line frequency clock, two serial line interface units, and a RDV11 compatible boot-strap/diagnostic ROM. Three 40-pin sockets are available for the KEF11-AA Floating Point option and the KDF11-BS Commercial Instruction set. The module can support up to 496K bytes of memory using the standard LSI-11 bus and up to 4 megabytes using the extended LSI-11 bus. The module uses a 4-level interrupt bus protocol.

Power Requirements

+5 V 5A, 4.5 A
+12 V 5A, 0.5 A

Bus Loads

AC 2 unit loads
DC 1 unit load

Environmental

DEC STD 102 Class C

Diagnostic Programs

Refer to Appendix A

CONFIGURING THE KDF11-BA

The module contains both wirewrap pins and soldered-in jumpers. It also has two switch packs used with the serial line units and the BDV11 type boot/diagnostic. The selectable functions are described as follows.

1. Test jumpers
2. CPU optional jumpers
3. Boot and diagnostic ROM jumpers
4. SLU jumpers
5. Bus grant continuity jumpers

Test Jumpers

This group of jumpers consists of manufacturing test, UART test, and Field Service test jumpers. The manufacturing test jumpers must be installed for normal operation.

KDF11-BA Jumper and Switch Locations

Manufacturing Test Jumpers

Jumper From	To	Function
J8	J7	Connects the system oscillator to the CPU and LSI-11 bus timing circuits.
J9	J8	Connects the phase signal to the input of the F11 chip clock driver.
J20	J21	Connects the baud rate crystal oscillator to the SLU baud rate generator and the −12 V charge pump circuit.

The UART test jumpers allow the UART to be cleared by power-up and system restart only.

CAUTION

Standard field service SLU diagnostics will fail if the reset disabled configuration is selected. Normal system and diagnostic operation requires that this feature not be selected.

UART Test Jumper

Jumper From	To	Function	Reset Disabled	Normal Operation
J33	J31	Connects LINITP(1) H to the console SLU UART reset input.	R	I
J32	J34	Connects DCOKCMBL to the console SLU UART reset input.	I	R

R = removed I = installed

The Field Service test jumper allows the checkout of the console terminal and cabling independent from the processor.

Field Service Test Jumper

Jumper From	To	Function	Field Service	Normal Operation
J27	J26	Connects the output of the console serial line driver to the console serial line output.	R	I
J26	J26	Connects the serial line input from the console connector to the console connector serial line output.	I	R

R — removed, I — installed

CPU Optional Jumpers

The CPU optional jumpers select the power-up mode as well as the bad-trap option.

Power-Up Mode Jumper Configurations

Jumper J18 to J19	Jumper J18 to J17	Mode	Name
R	R	0	PC@24, PS@26
R	I	1	Console ODT
I	R	2	Bootstrap
I	I	3	Extended microcode

R — removed, I — installed

Power-Up Mode 0 – This mode causes the microcode to fetch the contents of memory locations 24 and 26 and loads their contents into the PC and PS, respectively. The microcode then examines BHALT L. If BHALT L is asserted, the processor enters console ODT mode; if it is not, the processor begins program execution by fetching an instruction from the location pointed to by the PC. This mode is used when power-fail/auto-restart capability is desired, but is valid only when used with nonvolatile memory.

Power-Up Mode 1 – This mode causes the processor to enter console ODT (on-line debugging technique) mode immediately after power-up, regardless of the state of any service signals. This mode is useful in a program development or hardware debugging environment – the user has immediate control over the system after power up.

Power-Up Mode 2 – This mode causes the processor to generate internally a 16-bit bootstrap start address of 173000 (the conventional start address for DIGITAL systems). This address is loaded into the PC. The processor sets the PS to 340 (PS<7:0> = 7) to inhibit interrupts before the processor is ready for them. If HALT L is asserted, the processor enters console ODT mode; if it is not, the processor begins execution by fetching an instruction from the location pointed to by the PC. This mode is useful for turn-key applications where the system automatically begins operation without operator intervention.

Power-Up Mode 3 – This mode causes the microcode to jump to optional control chip number 37, location 76, and begin microcode execution. This mode is reserved for future microcode expansion by DIGITAL and is not recommended for customer use. If it is erroneously selected, the processor will treat it as a reserved instruction trap to location 10.

NOTE

In user mode a halt instruction execution will always result in a trap to location 10.

Halt/Trap Jumper Configuration

Jumper J18 to J16	Processor Mode	Function
R	Kernel	Processor enters console ODT microcode when it executes a halt instruction.
I	Kernel	Processor traps to location 10 when it executes a halt instruction.
X	User	Halt instruction decode results in a trap to location 10 regardless of the status of the halt/trap jumper.

R = removed, I = installed, X = don't care

Halt/Trap Option – If the processor is in kernel mode and decodes a halt instruction, BPOK H is tested. If BPOK H is negated, the processor will continue to test for BPOK H. The processor will perform a normal power-up sequence if BPOK H becomes asserted sometime later. If BPOK H is asserted after the halt instruction decode, the halt/trap jumper (J16) is tested. If the jumper is removed, the processor enters console ODT mode. If the jumper is installed, a trap to local address 10 will occur.

Bootstrap and Diagnostic Registers
The bootstrap and diagnostic logic contains three hardware registers that are software-addressable. One of the registers is a dual-purpose register, functioning as the configuration register when read and the display register when written. These three registers, along with the line clock register and the ROM expansion, can be disabled by inserting a jumper from J10 to J15.

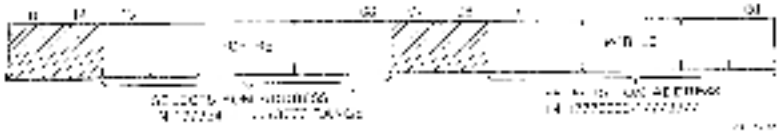
Register Address Assignments

Register	Read/ Write	Bit Size	Address
Page control	W	12	17777520
Read/write maintenance	R/W	16	17777522
Configuration*	R	8	17777524
Display*	W	4	17777524

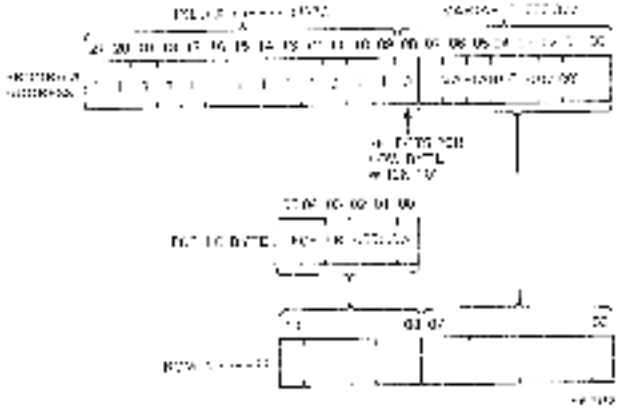
*Dual-purpose register

The page control register (PCR) is a write only register that is both word- and byte-addressable. Only bits <12:8> and <5:0> can be loaded. Whenever the KDF11-BA read-only memory is accessed, either the PCR high byte (bits <12:8>) or the PCR low byte (bits <5:0>) is used for the six most significant bits of the ROM address.

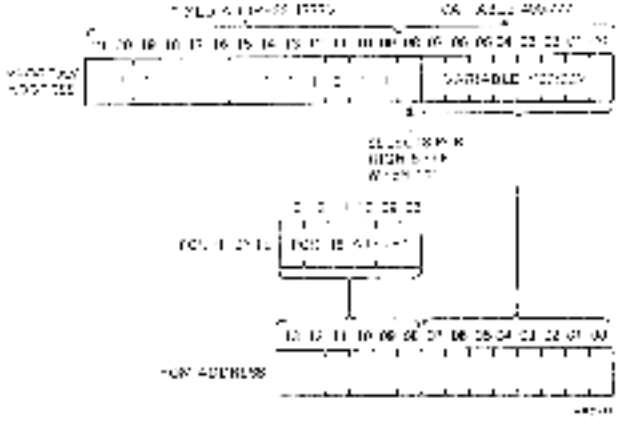
The read only memory addresses 17773000 through 17773377 are accessed by the low byte (bits 04:00). The read-only memory addresses 17773400 through 17773777 are accessed by the high byte (bits 13:05). The following figures show the format for the page control register, which is cleared by power-up or when the system is initialized.



Page Control Register Format



ROM Address Format Using PCR LO Byte



ROM Address Format Using PCR Hi Byte

The read/write maintenance register (R/W) is a 16-bit read/write register that is both word- and byte-addressable. It is used by the ROM diagnostics to test various read/write functions before accessing main memory. This register is cleared by power-up and by system reset.

The configuration and display register (CDR) is actually made up of two independent registers that share the same address. The read-only configuration register is accessed when the CDR is read. The write-only display register is loaded by a write transfer to the CDR.

Configuration register bits <15:8> always read as zero; bits <7:0> reflect the status of eight switches on the KDF11-BA module or location E102. The interpretation of these switches is determined by the ROM boot and diagnostic programs. Diagnostic/bootstrap program selection for the KDF11-BA is described in the following table.

Display register bits <3:0> allow for program control of a diagnostic LED display on the KDF11-BA module. Writing a 0 into one of these bits lights its corresponding LED. Writing a 1 into one of these bits turns its corresponding LED off. Display register bits <15:4> are not used. The display register is cleared (and the four LEDs are lit) by power up or system restart.

Bootstrap/Diagnostic Configuration Switches
Boot and diagnostic configuration register bits <7:0><0> reflect the status of the eight switches of the S1 switch pack (E102). Switches S1-1 through S1-4 are used to select a diagnostic and/or a bootstrap program. Switches S1-5 through S1-8 are used in conjunction with switches S1-3 and S1-4 to select the specific bootstrap program desired.

Diagnostic/Bootstrap Program Selection

Switch Number	Switch Position	Function
S1-1	ON	Execute CPU diagnostic upon power-up or restart.
S1-2	ON	Execute memory diagnostic upon power-up or restart.
S1-3	ON	DEC boot (S1-4 through S1-7 are arguments*).
S1-4	ON	Console test and dialog (S1-3 Off).
S1-5	OFF	Turn key boot displacement by S1-5 through S1-8 configuration (S1-3 Off).

*DEC boot arguments are:

Boot Device	Switch Positions S1-4	S1-5	S1-6	S1-7
DLV11	ON	X	X	X
DLV11-E	OFF	ON	X	OFF
DLV11-F	OFF	ON	X	ON

†DLV11-E CSR = 17775610
DLV11-F CSR = 17776500
DLV11 CSR = 176000[41] if there are no devices from 17760010 to 17760030

X = don't care

A bootstrap program other than the DECnet boots above are controlled by the bit patterns in switches S1-5 through S1-8. The bit patterns are described in the following table. If the console port is selected (S1-4 on, S1-3 off), the bootstrap program is controlled by a device mnemonic and unit number supplied by the console operator.

Bootstrap Program Selection

Device Mnemonic*	Switches: S1-5	S1-6	S1-7	S1-8	Program Selected
DKn (n < 8*	OFF	OFF	OFF	ON	RK05 boot
DLn (n < 4	OFF	OFF	ON	OFF	RL01 or RL02 boot
DDn (n < 2	OFF	OFF	ON	ON	TU58 (DD) at 776500 boot
DXn (n < 2	OFF	ON	OFF	OFF	RX01 boot
DYn (n < 2	OFF	ON	ON	OFF	RX02 boot

*n = unit number

The console ROM prompts the operator with:

```
XXXX.KW
START?
```

where XXXX is the decimal multiple of 1024 words of RAM found in the system when sized from 0 on in consecutive 1024-word increments. The first word of each 1024-word segment is read and written back to itself.

The console operator responses are a two character device mnemonic with a one-digit octal unit number or one of two special single-character mnemonics. If no one-digit unit number is specified, the unit 0 is selected. The response must be followed by a <CR>. The special single-character mnemonics are as follows:

Y Use switch settings to determine boot device.
N Halt – enter ODT microcode.

Bootstrap/Diagnostic ROM Jumpers

Two 24 pin sockets (E126 and E127) are provided for the installation of 2K x 8 ROMs or EPROMs. When EPROMs are inserted into the two ROM sockets, +5 V must be applied to pin 21 of each socket. For all other ROMs used in this option, BDV address bit 13 (BTRA 13 H) must be applied to pin 21. This pin is a chip select input for 2K ROMs.

ROM (or EPROM) Jumpers

Jumper From	To	Memory Type ROM	EPROM	Function
J24	J23	R	I	Connects BTRA 13 H to pin 21 of the two ROM sockets.
J22	J30	I	R	Connects +5 V to pin 21 of the two ROM sockets.

I = installed, R = removed

KDF11-BA LED Display

The KDF11-BA ROM programs use the four red LEDs to indicate which programs and program segments are running. If the program performs an error halt or if it hangs up waiting for data from a peripheral device, these LEDs serve as an error indication.

The four red LEDs present an octal number from 0 (all LEDs off) to 17 (all LEDs on). The most significant LED is separated from the other three LEDs by the green power on LED. An octal code of 0 indicates that the diagnostics and bootstrap programs have been successfully executed. Codes 1 and 2 are lit during the CPU and memory tests, respectively. Codes 3 and 4 are lit when the ROM programs are typing a message on the console device or waiting for a console input, respectively. Codes 5–12 are lit during various phases of the bootstrap routines. (Code 12 indicates a ROM bootstrap error and should never occur on the KDF11-BA which, unlike the BDV11, does not have sockets for additional ROM boot code.) If the memory diagnostic is disabled, the ROM code still verifies the existence of memory locations 0–6, indicating an error with LED code 13. Code 17 indicates that the ROM programs are unable to begin running, either because the halt switch is on, or because of a hardware failure. The KDF11-BA LED display table lists the errors indicated by their corresponding LED display pattern.

KDF11-BA LED Display

Display (Octal)	MSD Bit 3	Bit 2	LSD Bit 1	Bit 0	Type of Error
01	OFF	OFF	OFF	ON	CPU test error.
02	OFF	OFF	ON	OFF	Memory test error.
03	OFF	OFF	ON	ON	Waiting for console terminal transmitter ready flag.
04	OFF	ON	OFF	OFF	Waiting for console terminal receiver done flag.
05	OFF	ON	OFF	ON	Load device status error
06	OFF	ON	ON	OFF	Bootstrap code incorrect;
07	OFF	ON	ON	ON	DECnet waiting for response from host.
10	ON	OFF	OFF	OFF	DECnet waiting for message completion.
11	ON	OFF	OFF	ON	DECnet processing received message.
12	ON	OFF	ON	OFF	ROM bootstrap error (not used on KDF11-BA)
13	ON	OFF	ON	ON	Special memory test failure on locations 0–6. (Can occur when memory testing is disabled.)
17	ON	ON	ON	ON	System hung, HALT switch on, or not power-up mode 2.

NOTE

The errors indicated above are valid only if the KDF11-BA BDV ROMs (part numbers 23-339E2-00 and 23-340E2-00) are installed in ROM sockets E126 (low byte) and E127 (high byte).

KDF11-BA Error Halts

A failure in a diagnostic test or bootstrap program causes the error to be indicated by the display and an error halt instruction is carried out by the processor. When entering the halt mode, the processor outputs on the console terminal the PC address of the HALT of the error. The actual error address is one word less than the terminal printout. In halt mode, the processor responds to the console ODT commands and allows the operator to troubleshoot the error. The following table lists the error halts that can result when the KDF11-BA ROM diagnostics and bootstrap programs detect an error condition.

List of Error Halts

Address of Error	Display (Octal)	Cause of Error
173038	01	CP1ERR. R0 contains address of error
173060	05	SLU switch selection incorrect; error in switches.
173048	0b	SLU error. CSR address for selected device in error. Check CSR for selected device in floating CSR address area.
173200	02	ROM loader error: checksum on data block.
173232	02	Memory error 2, write address into itself. Test 0–30K words with MMU off if present. R1 — Address in error and expected data R0 — Failing data
173036	01	CP4ERR. R0 points to cause of error
173240	01	CP3ERR. R0 contains address of error
173061	03	Memory error 3; odd parity pattern (072507) using byte addressing. Failure in this test usually will indicate problem in byte logic. Test 0–30K words with MMU off if present. R1 Failing address R4 Expected data R5 — Failing data

List of Error Halts (Cont)

Address of Error*	Display (Octal)	Cause of Error
173817	07	Memory error in premenory data test for locations 000 776. R2 — Failing data R3 — Expected data R5 — Failing address (000 776)
173816	06	Memory error; bit is set in one of the parity CSRs (772100-772136). Failing memory should have parity error light on. R4 — Address of failing CSR (Contents of failing CSR identifies which 1K word bank of memory caused error.)
173854	12	ROM loader error; checksum on address block
173856	11	ROM loader error; jump address is odd.
173576	09	RL11/RL01 device error.
173852	05	RK05 device error.
173854	01	Switch mode halt; match was not made with switches.
173860	02	Memory error in 0000 (044K words of the 22-bit memory test. This is a common error halt for six different tests. If R0 = 0, there is an error in test 1 or R4 determines failing test. R4 — Expected data R5 — Failing data

List of Error Halts (Cont)

Address of Error	Display (Octal)	Cause of Error
		Contents of R4 / Test No. / Test Description
		000000–27776 / 1 / Address test bits 11–00
		177777 / 2 / Data test
		000000 / 3 / Data test
		052527 / 4 / Odd parity pattern test
		125125 / 5 / Byte addressing test
		For tests 1–5 (R3 = 0), determine 22-bit failing address as follows. R1 bits 11–00 = failing address bits 11–00 R2 bits 15–06 = failing address bits 21–12 Example: R2 = 123400 R1 = 007776 R2 = 1234XX R1 = XX7776 Ignore the upper two octal digits of R1 and the lower two octal digits of R2. Failing 22-bit address = 1234776
		Errors in address uniqueness test. Test checks address bits 21–06. Test 6. If R5 is not equal to 0, an error is in this test R4 = Expected data R5 = Failing data R2 = 22-bit failing physical address bits 21–06. Failing address bits 05–00 are always 0 Example: R2 = 021556 Failing address = 1021556000
17XXX4	05	Memory error in premaintenance address test for locations 000–776 R3 = Failing data R5 = Failing address and expected data

List of Error Halts (Cont)

Address of Error	Display (Octal)	Cause of Error
173670	01	Error CPU test 0; JSR R5 failed.
173700	01	Error CPU test 9; JSR PC failed
173704	05	RX011/RX02 device error.
173714	04	A NO typed in console terminal test.
173756	07	Memory error 1; data test failed. Test: 0–30K words with MMU bit 4 present. R1 — Failing address R4 — Expected data (either 0 or 177777) R5 — Failing data
173740	01	Error CPU test 9; RTS return failed.
173742	03/04	Console terminal test; no done flag.
173760	05	TU58 error halt

*Contents of R7 after halt

Device Selection Jumpers

The on-board peripheral device functions are selected by three jumpers that can be connected to ground via J10.

On-Board Device Selection Jumpers

Stake Number	Function
J10	This wirewrap stake provides a ground source for the other three wirewrap stakes in this group.
J19	When grounded, this signal disables the boot/diagnostic registers, the boot/diagnostic ROMs, and the line clock register.

On-Board Device Selection Jumpers (Cont)

Stake Number	Function
J11	When grounded, this signal forces the line clock interrupt enable flip-flop to be set and allows the LSI-11 bus BEVNT signal to request program interrupts unconditionally.
J14	When grounded, this signal disables the console serial line registers. When ungrounded, the device and vector addresses for the console SLU are as follows.

Device Addresses		Interrupt Vectors	
RCSR	17777560	Receiver	060
RBUF	17777562	Transmitter	064
XCSR	17777564		
XBUF	17777566		

NOTE

If J14 is grounded, the halt-on-break feature must also be disabled.

J13	When grounded, this signal disables the second serial line registers. When ungrounded, the device and vector addresses for the second SLU are determined by the status of the J12 jumper.
J12	When this jumper is not grounded, the second SLU device and its vector addresses are as follows.

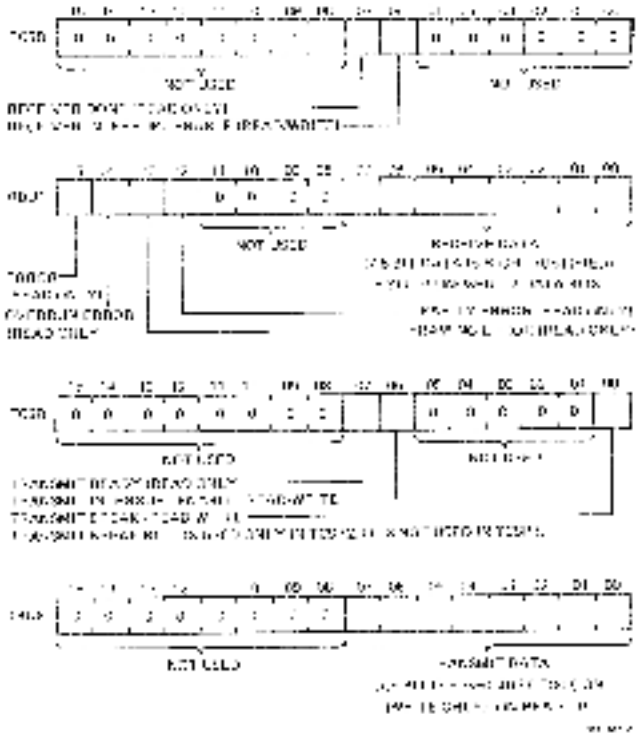
Device Addresses		Interrupt Vectors	
RCSR	17776500	Receiver	300
RBUF	17776502	Transmitter	304
XCSR	17776504		
XBUF	17776506		

When this jumper is grounded, the device and vector addresses are as follows.

Device Addresses		Interrupt Vectors	
RCSR	17776540	Receiver	340
RBUF	17776542	Transmitter	344
XCSR	17776544		
XBUF	17776546		

Register Bit Assignments

The bit formats for the SLU registers are described below.



SLU Register Bit Formats

RCSR1 and RCSR2 Bit Assignments

Bit	Mnemonic	Description
15-08		Unused. Read as zeros.
07	RX DONE	Receiver done. This read-only bit is set when an entire character has been received and is ready to be read from the RBUF register. This bit is automatically cleared when RBUF is read. It is also cleared by power-up and BUS INIT.
06	RX IE	Receiver interrupt enable. This read/write bit is cleared by power-up and BUS INIT. If both RCVR DONE and RCVR INT ENB are set, a program interrupt is requested.
05-00		Unused. Read as zeros.

RBUF1 and RBUF2 Bit Assignments

Bit	Mnemonic	Description
15	ERR	Error. This read only bit is set if any RBUF bit (14-12) is set. ERR is clear if all RBUF bits (14-12) are clear. This bit cannot generate a program interrupt.
14	OVR ERR	Overrun error. This read-only bit is set if a previously received character was not read before being overwritten by the present character.
13	FRM ERR	Framing error. This read-only bit is set if the present character had no valid stop bit. Also used to detect a break condition.
12	PAR ERR	Parity error. This read-only bit is set if received parity does not agree with expected parity. Always 0 if no parity is selected.

NOTE

Error conditions remain in effect until the next character is received, at which point, the error bits are updated. The error bits are cleared by power-up and BUS INIT.

RBUF1 and RBUF2 Bit Assignments (Cont)

Bit	Mnemonic	Description
11-08		Unused. Read as zeros.
07-00		Received data bits. These read-only bits contained the last received character. If less than eight bits are selected, the character will be right-justified with the most significant bit(s) reading zero.

TCSR1 and TCSR2 Bit Assignments

Bit	Mnemonic	Description
15-08		Unused. Read as zeros.
07	TX RDY	Transmitter ready. This read-only bit is cleared when TBUF is loaded and is set when TBUF can receive another character. XMT RDY is set by power up and by BUS INIT.
06	TX IE	Transmitter interrupt enable. This read/write bit is cleared by power-up and BUS INIT. If both XMT RDY and XMT INT ENB are set, a program interrupt is requested.
02-01		Unused. Read as zeros.
00	TX BRK	Break. When set, this read/write bit transmits a continuous space. This bit is cleared by power-up and SYSTEM INIT. This bit is used only in TCSR2; it is unused in TCSR1.

TBUF1 and TBUF2 Bit Assignments

Bit	Mnemonic	Description
15-08		Unused. Read as zeros.
07-00	TBUF	TBUF bits 07-00 are write-only bits used to load the transmitted character. If less than eight bits are selected, the character must be right-justified.

Console SLU Baud Rates

Switches 1–4 of the S2 switch pack (E111) select 1 of 16 possible SLU baud rates if the internal baud rate generator is used as the clock source. If the KDF11-BA is configured to operate the SLU with an external clock, the positions of these switches are meaningless. The SLU transmits and receives at the selected baud rate. Split baud operation is not provided.

Console SLU Baud Rate Selection

Switch Position S2-4	S2-3	S2-2	S2-1	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19200

Console SLU Character Formats

Five wirewrap stakes are used to select options for establishing the console SLU character format. The ground stake can be connected to any combination of the other four stakes to configure the character format for the following options.

1. One or two stop bits
2. Seven data bits plus parity
3. Eight data bits without parity
4. Odd or even parity

Character Jumper Configurations

Jumper From	To J38	Character Format Option
J39	IN	7-bit characters
	OUT	8-bit characters
J37	OUT	Two stop bits
	IN	One stop bit
J36*	IN	Parity check enabled
	OUT	Parity check disabled
J40	IN	Odd parity if J36 is in
	OUT	Even parity if J36 is in

NOTE: If 8 bit characters (J39 OUT) are selected, parity check must be disabled (J36 OUT).

Halt-on-Break Jumpers

Two jumpers enable and disable the halt-on-break feature. If this feature is enabled, the detection of a break condition by the console UART causes the processor to halt and enter the on-line debugging technique (ODT) microcode. If this feature is disabled, there is no response to the break condition.

Halt-on-Break Jumper Configuration

Jumper From	To	Function	Break Feature Enabled	Disabled
J5	J4	Connects ground to RQ HLT H.	R	I
J3	J1	Connects DL1 FE H to RQ HLT H.	I	R

R — removed, I — installed

Second SLU Baud Rates

Switches 5 through 8 of the S2 switch pack (E114) select 1 of 16 baud rates for the second SLU. If the internal baud rate generator is used as the clock source. The second SLU will transmit and receive at the selected baud rate.

Second SLU Baud Rate Selection

Switch Position S2-8	S2-7	S2-6	S2-5	Baud Rate
ON	ON	ON	ON	50
ON	ON	ON	OFF	75
ON	ON	OFF	ON	110
ON	ON	OFF	OFF	134.5
ON	OFF	ON	ON	150
ON	OFF	ON	OFF	300
ON	OFF	OFF	ON	600
ON	OFF	OFF	OFF	1200
OFF	ON	ON	ON	1800
OFF	ON	ON	OFF	2000
OFF	ON	OFF	ON	2400
OFF	ON	OFF	OFF	3600
OFF	OFF	ON	ON	4800
OFF	OFF	ON	OFF	7200
OFF	OFF	OFF	ON	9600
OFF	OFF	OFF	OFF	19200

Second SLU Character Formats

Five wirewrap jumpers are used to select options for establishing the second SLU character format. The ground stake can be connected to any combination of the other four stakes to configure the character format for the following options:

1. One or two stop bits
2. Seven data bits plus parity
3. Eight data bits without parity
4. Odd or even parity

Character Jumper Configurations

Jumper From	To J30	Character Format Option
J31	IN	7-bit characters
	OUT	8-bit characters
J29	OUT	Two stop bits
	IN	One stop bit
J28	IN	Parity check enabled
	OUT	Parity check disabled
J32	IN	Odd parity if J28 is in
	OUT	Even parity if J28 is in

Internal/External SLU Clock Jumpers

Two sets of jumpers are provided to select an internal or external clock for the console SLU and the second SLU. If the internal clock jumpers are installed, the SLU clocks are obtained from the internal baud rate generator. When the external clock jumpers are installed, external clocks are routed to the SLUs through pin 1 of the J1 and J2 SLU connectors.

Internal/External SLU Clock Jumper Configurations

Jumper From	To	Function	Selected Clock Internal	External
J42	J47	Connects internal baud rate generator to the console SLU UART. (Normal configuration)	I	R
J41	J43	Connects external clock to the console SLU UART.	R	I
J46	J48	Connects internal baud rate generator to the second SLU UART. (Normal configuration)	I	R
J44	J45	Connects external clock to the second SLU UART.	R	I

R = removed, I = installed

Bus Grant Continuity Jumpers

The jumpers provide continuity for the interrupt acknowledge (BIAK) and direct memory access grant (BDMG) LSI-11 bus signals.

Bus Grant Continuity Jumpers

Jumper[1]	Function
W1	Connects backplane pins CM2 and CN2, providing continuity for BIAK L.
W2	Connects backplane pins CR2 and CS2, providing continuity for BDMG L.

[1]Must be installed when the KDF11-BA is used in an A9/A8 or Q/Q bus backplane; otherwise, the jumper installation is optional.

FACTORY SWITCH AND JUMPER CONFIGURATIONS

Users may reconfigure the module jumpers and switches to select the KDF11-BA options required for the particular system application. All switches and all jumpers except those jumpers reserved for manufacturing and field service testing may be reconfigured. Therefore, the factory configuration as shipped is described below to assist users in determining the jumper and switch changes that are required to select the module options for their systems.

Factory Jumper Configurations

Jumper	Jumper State	Function
J1 to J7	I	Master clock, enables internal oscillator
J8 to J9	I	Phase; this connects signal to F11 chip clock drivers.
J20 to J21	I	XTAL; connects baud rate oscillator.
J33 to J34	I	LINIT (101); connects reset to console UART.
J33 to J34	O	Installed resets disabled test feature (only after removing jumper J35-J34)

Factory Jumper Configurations (Cont)

Jumper	Jumper State	Function
J27 to J26	I	Connects console SLU serial output to connector J1.
J26 to J25	R	Installed for Field Service wraparound testing (only after removing jumper J27-J26).
J19 to J18 J17 to J18	I R	Power up mode 2 (jumper J19-J18 installed; jumper J17-J16 removed) causes the processor to begin executing the bootstrap code at start address 173000
J16 to J18	R	Processor enters console ODT microcode when it executes a kernel mode halt instruction.
J11 to J10	R	LTC CKJ L BEVENT can request interrupts only if the processor program has set bit 6 of the line clock register (177775461)
J12 to J10 J13 to J10	R R	The second SLU is enabled with an RCSR address of 17776500 and interrupt vector addresses of 300 and 304.
J14 to J10	R	The console SLU is enabled.
J15 to J10	R	The KDV ROMs and registers, as well as the line clock register, are enabled.
J22 to J23		When ROMs are used, jumper J22-J23 is installed and jumper J24-J23 is removed.
J24 to J23		When PROMs are used, jumper J22-J23 is removed and jumper J24-J23 is installed.
J36 to J34	R	Console SLU parity check is disabled.
J37 to J35	I	Console SLU character contains one stop bit.
J38 to J34	R	Console SLU character contains eight bits.
J40 to J39	R	No effect; console parity already disabled.

Factory Jumper Configurations (Cont)

Jumper	Jumper State	Function
J3 to J4	R	
J5 to J1	I	Halt-on-break feature is disabled. The break key on the console SLU does not halt the processor. This feature may be enabled by removing jumpers J5-J4 and then installing jumpers J3-J4.
J29 to J30	R	Second SLU parity check is disabled.
J29 to J31	I	Second SLU character contains one stop bit.
J31 to J30	R	Second SLU character contains eight bits.
J32 to J33	R	No effect; second SLU parity already disabled.
J41 to J42	R	
J43 to J42	I	The on-board baud rate generator is connected to the console SLU. The external clock input from connector J1 is disabled.
J44 to J45	R	
J46 to J45	I	The on-board baud rate generator is connected to the second SLU. The external clock input from connector J2 is disabled.
W1	I	This provides bus grant continuity for the BIAK signal.
W2	I	This provides bus grant continuity for the BDMG signal.

Bootstrap/Diagnostic Factory Switch Configurations

Switch S1 Number	(E102) Position	Function
1	ON	Execute CPU diagnostic
2	ON	Execute memory diagnostic
3	OFF	DECnet boot disabled
4	ON	Console test and dialogue
5	OFF	
6	OFF	
7	ON	RL01/RL02 bootstrap program
8	OFF	

*With the switch configurations shown, the KDF11-BA upon power-up or restart, will execute the CPU diagnostic, the memory diagnostic and then enter the console test. If the operator wishes to terminate the memory diagnostic and immediately enter the console test, control-C must be entered on the console terminal.

SLU Baud Rate Factory Switch Configurations

Switch S2 Number	(E114) Position	Function
1	ON	Console SLU set for 9600 baud
2	OFF	
3	OFF	
4	OFF	
5	ON	Second SLU set for 9600 baud.
6	OFF	
7	OFF	
8	OFF	

KPV11-A (M8016) POWER FAIL/LINE TIME CLOCK
KPV11-B (M8016-YB) KPV11-A + 120 Ω TERMINATOR
KPV11-C (M8016-YC) KPV11-A + 250 Ω TERMINATOR

Amps 24 V		Bus Loads		Cables
5	12	AC	DC	
0.11	0.52	1.0	1.0	70-17704 (for remote operation)

Standard Address

LKR 177546

Standard Vector

LTC 100

Diagnostic Programs

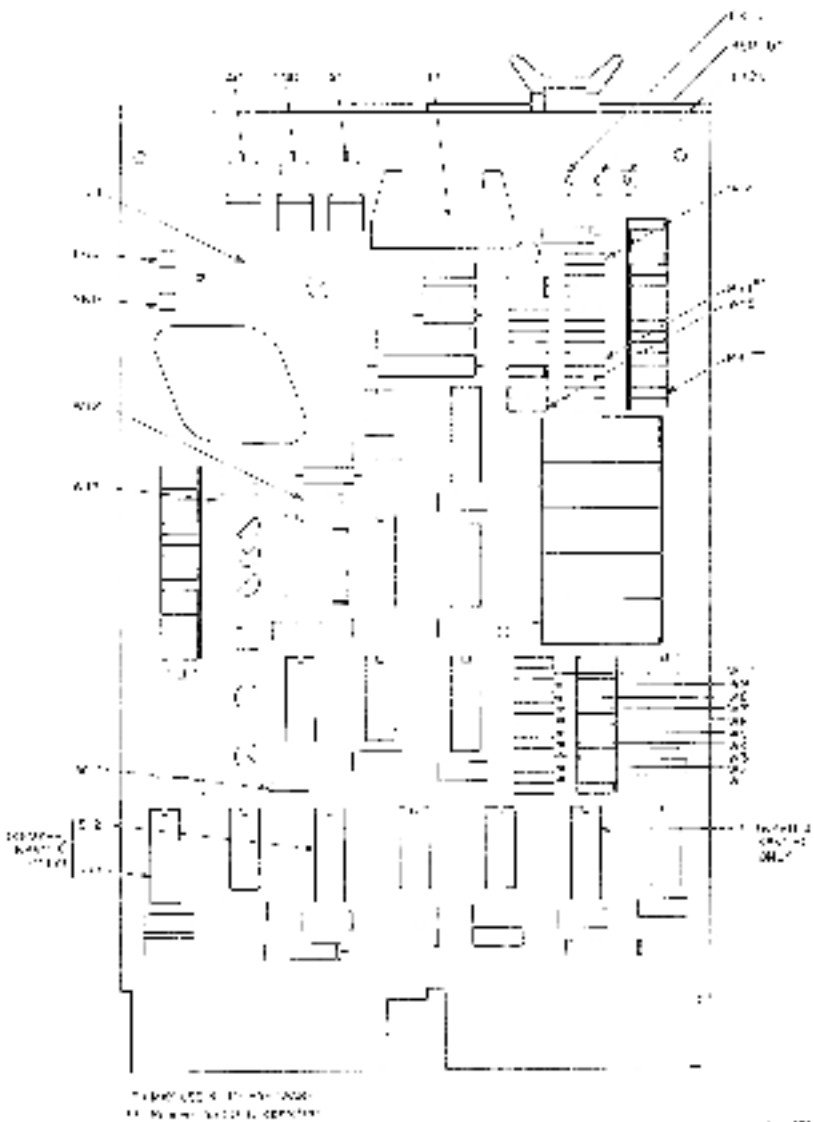
Refer to Appendix A.

Related Documentation

Field Maintenance Print Set (MP008041)
Microcomputer Interfaces Handbook (EB-20175-20)

Options to KPV11

DEC PN	Description
54-11606	Console panel printed circuit board assembly
70-11668	Console bezel (dress panel)
70-08012	Console signal/power cable (required for optional console panel use)



KPV11 Jumpers

KPV11 Factory Jumper Configuration

Jumper Designation	Jumper State	Function Implemented
W1	I	Sets address of line time clock status register (LKS) to 177546.
W2	I	
W3	I	
W4	I	
W5	I	
W6	H	
W7	I	
W8	I	
W9	H	
W10	H	
W11		Do not change. Must be installed for proper terminator function on KPV11-B and KPV11-C.
W12	R	Disables continuous or manual control of LTC interrupt request operation. Do not install when W13 is installed.
W13	I	LTC interrupt requests can be enabled and disabled by program. Do not install when W12 is installed.
W14	I	Console (optional) LTC ON/OFF switch enabled.
W15	I	LTC is set to count at the power line frequency.

NOTES

1. Line Time Clock (LTC) controls

Function	W12	W13
disable LTC	I	R
enable LTC and enable LTC program control	R	I
enable LTC and disable LTC program control	R	R

2. LTC Remote Console Switch

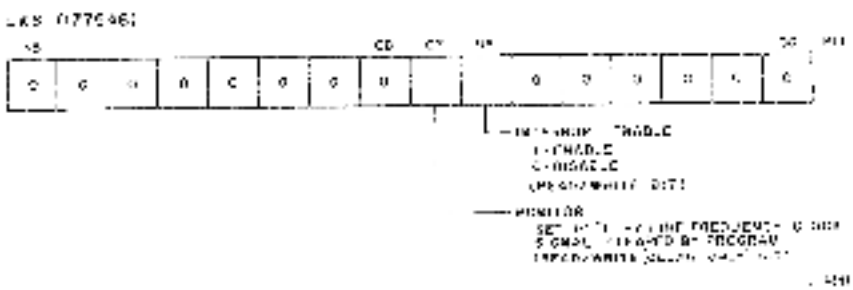
Function	W14
console switch enabled	I
console switch disabled	R

3. Select LTC Frequency

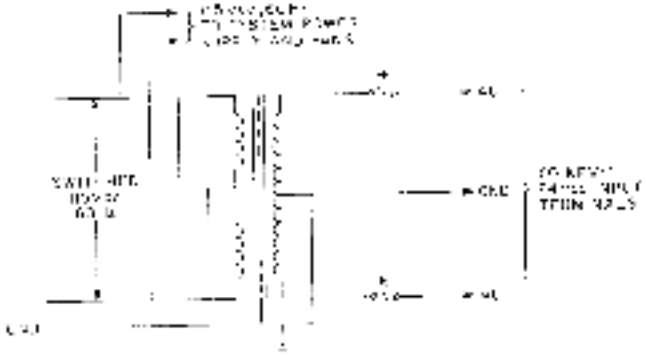
Function	W15
LTC signal occurs at line frequency	I
LTC signal occurs at frequency inserted at EXT TIME REF	R

4. External Transformer

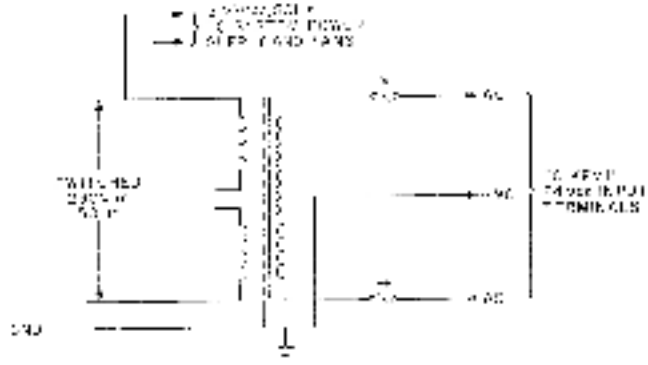
The user must supply a 24 Vac, 200 mA center tapped transformer to be connected to the two ac and the ground tabs on the top of the module. If a transformer capable of supplying more than 200 mA is used, current limiting in the form of a fuse must be used to protect the KPV11-A module.



Line Time Clock Status Register (LTCS)



(A) 115V CONNECTIONS (TYP CBL)



(B) 230V CONNECTIONS (TYP CBL)

Power Line Monitor Transformer Installation

KUV11-AA WRITABLE CONTROL STORE

Amps		Bus Loads		Cables
1.5	1.2	AC	DC	17-00124-00
0		1.4	1	17-00124-01 (maintenance)

Standard Addresses

CSR and RAM Address	177640
DATA I/O, bits 0-15	177642
DATA I/O, bits 16-21	177644

Standard Vectors

None

Diagnostic Program

Refer to Appendix A.

Related Documentation

LSI-11 WCS User's Guide (EK-KUV11-UG)
KUV11-AA Maintenance Print Set (MP00671-00)

NOTES

1. An M8018 can only be used with an M7264-YC LSI-11 processor.
2. To extend the M8018, the maintenance cable is required (17-00124-01).

Switch Configurations

The range of microcode addresses to which the WCS will respond on the microinstruction bus (MIB) (when the CSR enable bit is a 1) is determined by an 8-wire DIP switch (SW1) on the M8016 module.

Set switches S1 through S7 (S8 is not used) on SW1 as shown in the "WCS Address Mode Switch Settings" table to select one of the four modes of operation described below.

Mode I – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS correspondingly responds to microaddresses 2000 to 3777 on the MIB.

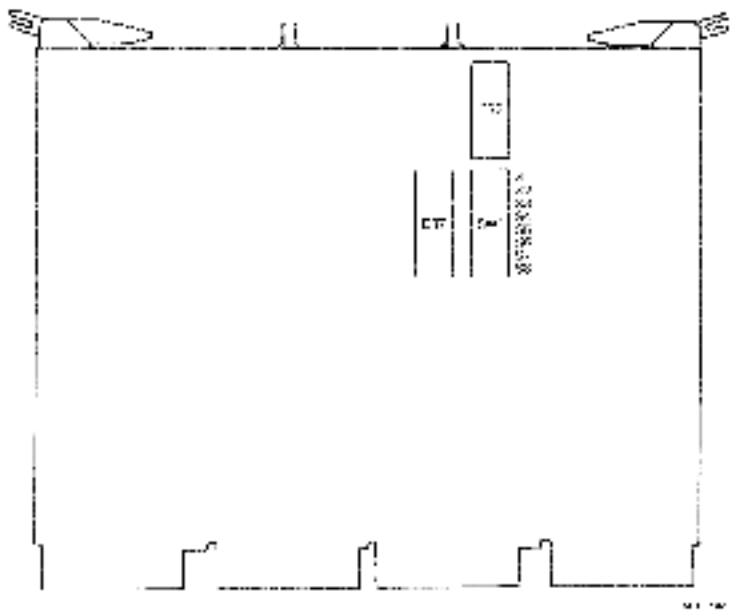
Mode II – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS initially responds to MIB microaddresses 2000 to 3777 from the first 512 words of RAM. If bits 21-16 of the microinstruction are coded to a 7 (octal) then the next microinstruction will be accessed from the second 512 words of RAM. A second 7 (octal) will toggle back to the first 512 words of RAM. This swapping between 512 word blocks for the same microaddress range is called "paging" and allows 1024 words of microcode to be implemented when only 512 microaddresses are available.

Mode III – This mode is the same as Mode I except that the two blocks of 512 words of RAM have been interchanged on the module. Addressing is identical to that of Mode I.

Mode IV – The microcode is loaded from the LSI-11 bus into WCS RAM locations 0 to 1777. The WCS correspondingly responds to MIB microaddresses 0 to 1777. This microaddress space is identical to MICROMs 0 and 1, which contain the base PDP-11 microcode for the LSI-11.

MODE	WCS RAM							
	2	3	4	5	6	7	8	
	ON	ON	ON	ON	OFF	ON	ON	
II	ON	ON	OFF	ON	OFF	OFF	ON	
III	ON	OFF	ON	ON	ON	ON	OFF	
IV	ON	ON	ON	ON	ON	ON	ON	

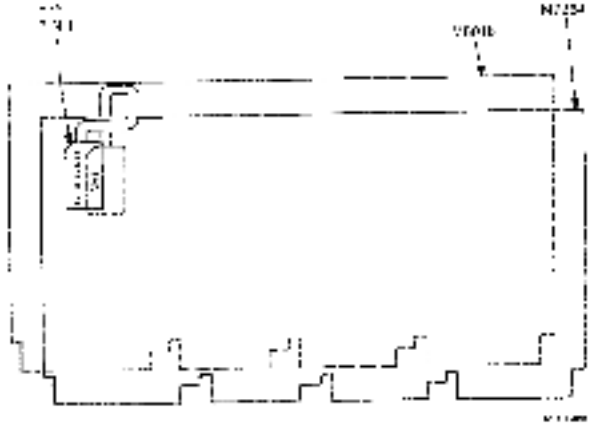
WCS Address Mode Switch Settings



Address Mode Switch Location

ITEM	QUANTITY			
	X			
	X	X	X	X
	X	X	X	X
		X	X	X
			X	X
			X	
				X

Items Supplied Per Configuration



W03 in CPU Installation

LSI-11 Bus Address Decode and Control
This logic does the LSI-11 bus interface, and responds to four device addresses which have the following meanings.

LSI-11 Address	Meaning
177640	Control/status register and RAM address
177642	Data input/output for RAM data word bits 0–15, or output for macro stack.
177644	Data input/output for RAM data word bits 16–21 and data input/output for two user bits.
177646	Unused (but still responds) A DIN will read all 1s.

NOTE
The address 177546 is the same address normally assigned to the KW11-L clock status register.

Read Back MUX
The read back MUX selects the source of the data to be output to the LSI-11 bus at the proper time during an LSI-11 DATAI bus cycle.

Control Status Register
The CSR consists of five control/status bits and a RAM address register. The control/status bits are described below.

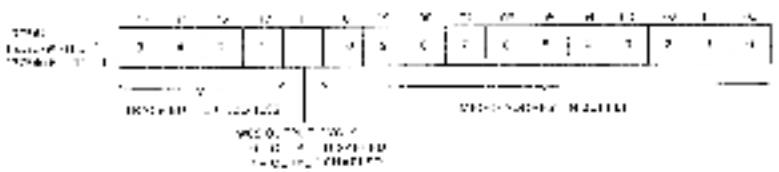
CSR Bit Descriptions

CSR Bit	Definition
15	When this bit is asserted, it resets the WCS module, in particular the trace feature.
14, 13, 11	These bits control the trace mode of the WCS.
12	When this bit (the enable bit) is asserted, the WCS is enabled to respond to the MB. When it is disabled, the WCS cannot respond to the MB.

After the enable bit is disabled in the CSR, the RAM can be accessed by writing an address (with enable bit = 0) to the CSR address. Then the lower 16 bits of that address of RAM (microcode bits 0-15) can be accessed (read or write) at the second device address, and the upper eight bits of the same address of RAM (the two user bits and microcode bits 16-21) can be accessed (read or write) at the third device address.

Control/Status and RAM Address Register

RAM Data Input/Output



Output for Trace Stack

RAM Data Input/Output, User Bits Data Input/Output

CSR Bit Assignments

KWV11-A PROGRAMMABLE REAL-TIME CLOCK

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.7A	0.01	3.41	1	BC04Z BC06R

Standard Addresses

CSR	170420
Buffer/Preset Register (BPR)	170422

Vector

440

Diagnostic Programs

Refer to Appendix A.

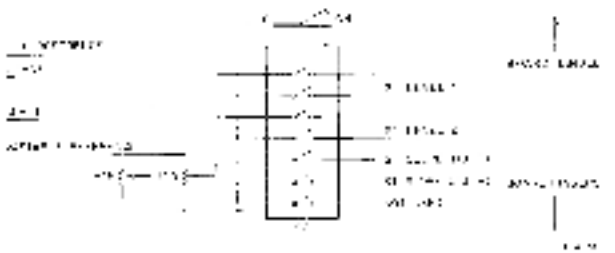
Related Documentation

ADV11-A, KWV11-A, AAV11-A, DRV11 User's Manual (EK-ADV11-OP)
Field Maintenance Print Set (MP002CC)
Microcomputer Interfaces Handbook (EB-20175-20)

KWV11-A Switches

KWV11-A CSR Address Switches (Set for 172420)

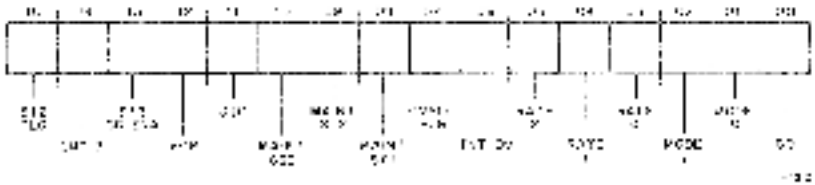
KWV11-A Vector Address Switches (Set for 300440)



KWV11-A Slope/Tolerance Level Selector Switches and Controls

NOTE

The user should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will not damage components, but will produce unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.



CSR Bit Assignment

CSR Bit Definitions

Bit	Function
15	ST2 Flag – Set by the firing of Schmitt trigger 2 or the setting of the MAINT ST2 bit in any mode while the go bit or the ST2 go enable bit is set. Cleared under program control. Also cleared at the rising transition of the go bit unless the ST2 go enable bit has previously been set. Must be cleared after servicing an ST2 interrupt to enable further interrupts. When cleared, any pending ST2 interrupt request will be canceled. If enabling interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority. Read/write to 0.
14	Interrupt on ST2 (INT 2) – Set and cleared under program control. When set, the assertion of ST2 flag will cause an interrupt. If set while ST2 flag is set, an interrupt is initiated. When cleared, any pending ST2 interrupt request will be canceled. Read/write.
13	ST2 Go Enable – Set and cleared under program control. Also cleared at the rising transition of the go bit. When set, the assertion of ST2 flag will set the go bit and clear the ST2 go enable bit. Read/write.
12	Flag Overrun (FOR) – Set when an overflow occurs and the overflow flag is still set from a previous occurrence, or when ST2 fires and the ST2 flag is already set. Cleared under program control and at the rising transition of the go bit. This bit provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software. Read/write.

CSR Bit Definitions (Cont)

Bit	Function
11	Disable Internal Oscillator (DIO) – Set and cleared under program control. For maintenance purposes, this bit inhibits the internal crystal oscillator from incrementing the clock counter. Used in conjunction with bit 10 below. Read/write.
10	MAINT OSC – Set under program control. Clearing is not required. Always read as a 0. For maintenance purposes, setting this bit high simulates one cycle of the internal 10 MHz crystal oscillator used to increment the clock counter. Write only.
09	MAINT ST2 – Set under program control. Clearing is not required. Always read as a 0. Setting this bit simulates the firing of Schmitt trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit. Write only.
08	MAINT ST1 – Set under program control. Clearing is not required. Always read as a 0. Setting this bit simulates the firing of ST1. All functions initiated by ST1 can be exercised under program control by using this bit. Write only.
07	OVFLO FLAG – Set each time the counter overflows. Cleared under the program control and at the 1-going transition of the go bit. If bit 6 is set, bit 7 will initiate an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If cleared while an overflow interrupt request to the processor is pending, the request is canceled. If enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority. Read/write bit.

CSR Bit Definitions (Cont)

Bit	Function
06	Interrupt on Overflow (INTOV) – Set and cleared under program control. When this bit is set, the assertion of OVFLO flag will generate an interrupt. Interrupt is also generated if bit 6 is set while OVFLO flag is set. If cleared while an overflow interrupt request to the processor is pending, the request is canceled. Read/write.
05, 04, 03	Rate – Set and cleared under program control. These bits select clock counting rate or source. 5 4 3 Rate 0 0 0 Stop 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 SCT 1 1 1 Line (50/60 Hz) Read/write to 0.
2, 1	Mode – Set and cleared under program control. 2 1 Mode 0: 0 0 Mode 1: 0 1 Mode 2: 1 0 Mode 3: 1 1 Read/write.
0	Go – Set and cleared under program control. Also cleared when the counter overflows in mode 0. Setting it to 1 initiates counter action as determined by the rate and mode bits. In modes 1, 2, and 3 it remains set until cleared. In mode 0 it clears itself when counter overflow occurs. Clearing bit 0 zeros and inhibits the counter. Read/write.

CSR Bit Settings for Mode 0, Single Interval

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of go bit. In version except when ST2 GO ENA has previously been set.
14-INT2	x	Set to 1 by program if interrupt on ST2 event is desired
13-ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit asserted.
12-FOR	(0)	
11-DIO	0	
10-MAINT OSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7-OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit asserted.
6-INT OV	x	Set to 1 by program for interrupt on counter overflow.
5-Rate 2	x	
4-Rate 1	x	See bit definitions.
3-Rate 0	x	
2-Mode 1	0	Set by program to 0.
1-Mode 0	0	Set by program to 0.
0-GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter overflows.

x — 0 or 1, depending on user requirements.
(0) — automatically cleared by go bit asserted (1).

CSR Bit Settings for Mode 1, Repeated Interval

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14-INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13-ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit assertion.
12 FOR	(0)	
11 0/C	0	
10-MAINT CSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7-OV-FLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit assertion.
6-INT OV	x	Set to 1 by program for interrupt on counter overflow.
5 Rate 2	x	
4 Rate 1	x	See bit definitions.
3 Rate 0	x	
2 Mode 1	0	Set by program to 1.
1-Mode 0	1	
0-GO	x	Same as for mode 0, except that bit is not cleared when counter overflows.

x — 0 or 1, depending on user requirements.
(0) — automatically cleared by go bit assertion

CSR Bit Settings for Mode 2, External Event Timing

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
15-ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of go bit assertion except when ST2 GO ENA has previously been set
14 INT2	x	Set to 1 by program if interrupt on ST2 event is desired.
13 ST2 GO ENA	x	Set to 1 by program if go is to be set by external signal to ST2. Cleared by leading edge of go bit assertion.
12-FOR	(0)	
11 DIO	0	
10 MAINT OSC	0	
9-MAINT ST2	0	
8-MAINT ST1	0	
7 OVFLO FLG	(0)	Will be set to 1 by counter overflow. Always cleared by leading edge of go bit assertion
6 INT OV	x	Set to 1 by program for interrupt on counter overflow.

x = 0 or 1 depending on user requirements.
(0) = automatically cleared by go bit assertion

CSR Bit Settings for Mode 2, External Event Timing (Cont)

Bit and CSR Name	Bit Condition as Written by Processor	Remarks
5–Rate 2	x	
4–Rate 1	x	See bit definitions.
3–Rate 0	x	
2 Mode 1	1	Set by program to 1.
1 Mode 0	0	
0 Go		Set by program to 1 unless ST2 GO ENA is set, remains 1 until written to 0 by program. Cleared when counter overflows.

x 0 or 1, according on user requirements.
(C) automatically cleared by go bit assertion.

Mode 3 (external event timing from 0 base) is identical to mode 2 except that the counter is zeroed after ST2 pulse. Counter continues to increment until go bit is set to 0.

KWV11-C PROGRAMMABLE REAL-TIME CLOCK

Power Requirement

−5 V ±5% @ 2.2 A
+ 12 V ±5% @ 10 mA

Bus Loads

AC	DC
1.0	1

Standard Addresses

Standard Address Assignments

Description	Mnemonic	Address
Registers		
Control/status	CSR	170420
Buffer preset	BPR	170422
Interrupt Vectors		
Clock overflow	CLK OV	440
Schmitt trigger 2	ST2	444

Diagnostic Programs

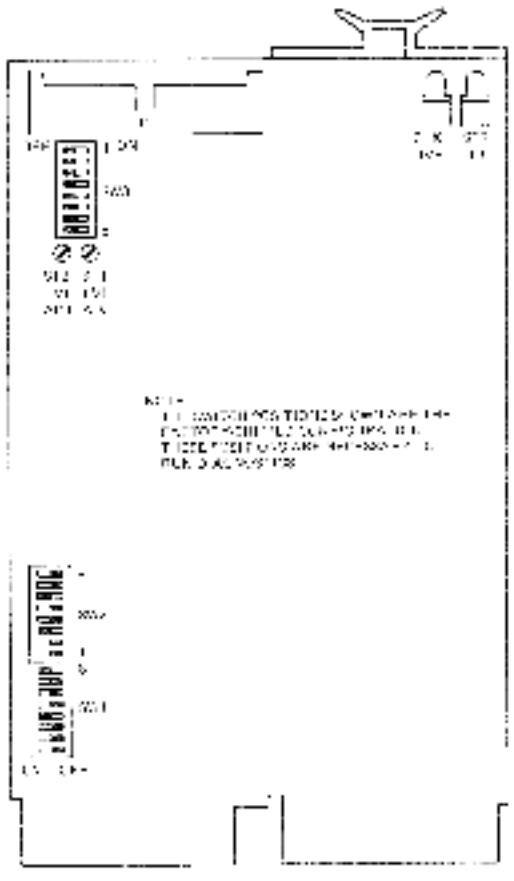
Refer to Appendix A.

Related Documentation

LSI-11 Analog System User's Guide (EK-AXV11-UG)
Field Maintenance Print Set (MP01950)

CONFIGURATION

The KWV11-C has two switch packs, SW1 and SW2, to set up its device address and interrupt vector address. It also has a switch pack, SW3, to select Schmitt trigger slope and level controls. For each of the two Schmitt triggers on the board, the user may select a fixed reference level for TTL logic or a variable reference level that permits setting the Schmitt trigger threshold to any point between −12 V and +12 V. The user may also select whether the Schmitt trigger fires on the positive or negative slope of the input waveform.



KWV11-C Module Layout

Selecting the KWV11-C Device Address

The KWV11-C device address is the base I/O address assigned to the control status register of the board. The device address is selected by means of two switch packs, SW1 and SW2. The switches allow the user to set the device address within the range of 170000 to 177774 in increments of 4. The device address is usually set at 170420. A switch in the on position decodes a 1 in the corresponding bit position; a switch in the off position decodes a 0.

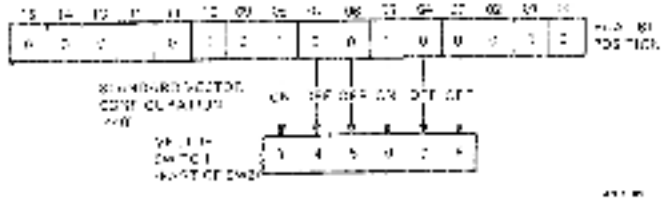
Selecting KWV11-C Device Address

Selecting the KWV11-C Interrupt Vector Address

The KWV11-C is capable of generating two interrupt vectors to the LSI-11 processor. These interrupts can occur when the clock counter overflows or the Schmitt trigger 2 fires.

The base interrupt vector is assigned to the clock overflow interrupt and can be assigned any address between 0 and 770 in increments of 10. It is usually set to 440 by SW2. A switch in the off position decodes a 0, a switch in the on position decodes a 1.

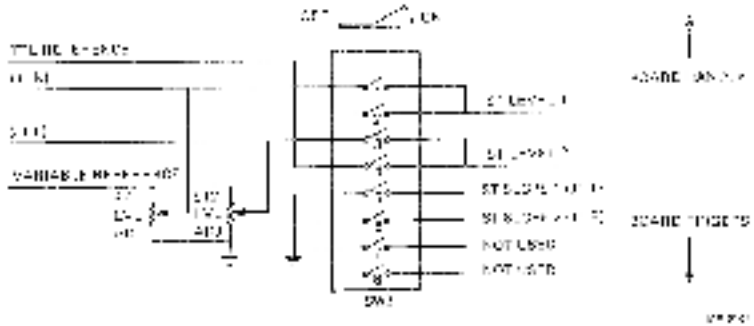
The interrupt vector for ST2 is automatically four address locations higher than the selected base interrupt vector.



Selecting KWV11-C Interrupt Vector Address

Selecting Schmitt Trigger Reference Levels and Slopes

The KWV11-C has two Schmitt triggers that condition the input waveforms to a form needed by the user. Both can be adjusted to trigger at any level in the ±12 V range (or at TTL fixed levels) and on either the positive or negative slope of the input signal. Each Schmitt trigger has three switches and a potentiometer. The use of these switches and potentiometers is described in the following table.

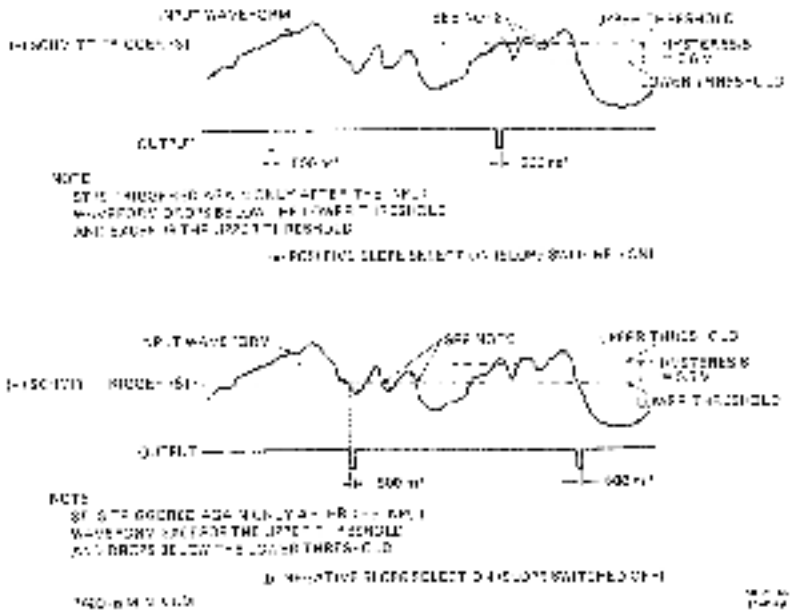


KWV11-C Slope and Reference Level Switches

Setting Schmitt Triggers on KWV11-C

SW3 Switch Number	Function
1	With this switch on and switch 2 off, ST1 fires at a level determined by the ST1 LVL ADJ potentiometer with a range of ±12 V. NOTE Switches 1 and 2 cannot be on together.
2	With this switch on and switch 1 off, ST1 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
3	With this switch on and switch 4 off, ST2 fires at a level determined by the ST2 LVL ADJ potentiometer within a range of ±12 V. NOTE Switches 3 and 4 cannot be on together.
4	With this switch on and switch 3 off, ST2 fires at a fixed reference level for TTL logic. The potentiometer has no effect.
5	When this switch is off, ST1 fires on the negative slope (high to low transition) of the input signal. When on, ST1 fires on the positive slope (low to high transition).
6	When this switch is off, ST2 fires on the negative slope of the input signal. When on, ST2 fires on the positive slope.
7, 8	Not used.

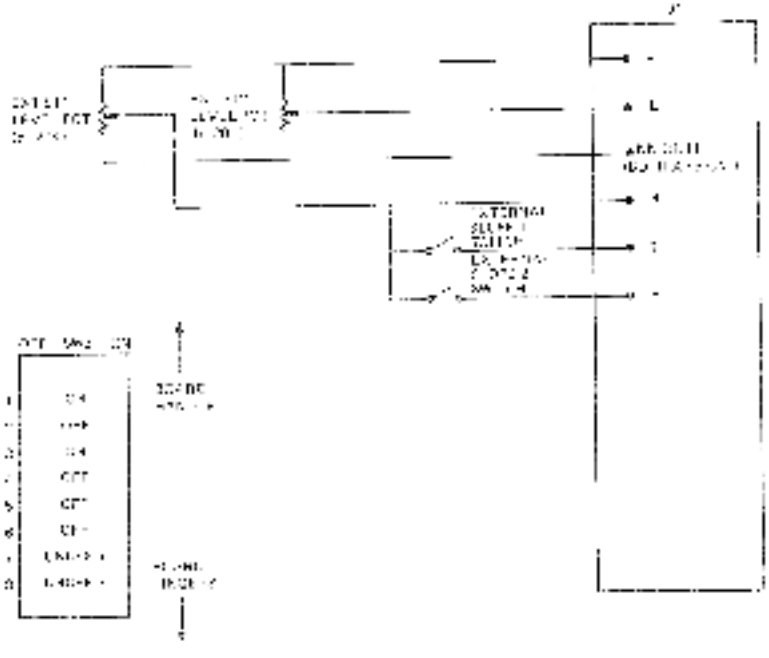
The following figure shows the relationship of an analog input signal to the Schmitt trigger output. Note that once the Schmitt trigger fires, it fires again only after the input signal moves past the opposite threshold and then again passes the user-selected threshold.



Input-to-Output Waveforms for Positive and Negative Slopes

External Control of Schmitt Triggers

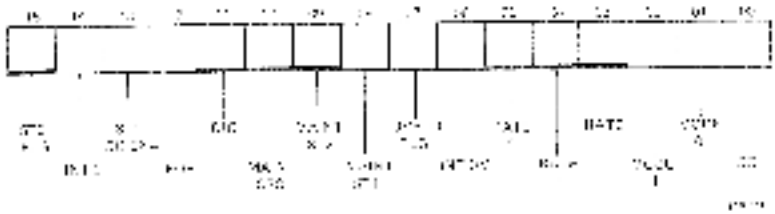
The connector J1 on the board allows the user to connect external slope and level controls for each Schmitt trigger. Connect external potentiometers and switches as follows. The value of the potentiometers should be between 5 kΩ and 20 kΩ. Selecting a potentiometer with more turns provides for a finer adjustment over the ±12 V range. SW3 on the KWV11-C must be set as follows.



Example Circuit for External Control of Schmitt Triggers

CSR BITS

The control status register is a read/write register that controls the operation of the KWV11-C. The CSR has bits to enable interrupts, mode selection, clock rate selection, and starting the counter (GO bit). The CSR monitors the counter overflow flag, flag overrun, and the Schmitt trigger flop (ST2). In addition, the CSR enables some maintenance operations. The following table describes these bits.



KWC11-C Control Status Register

KWV11-C Control Status Register Bit Definition

Bit	Name	Function	Set By/Cleared By
00	GO	(Read/write) – Setting this bit starts the counter at a rate determined by the rate bits 03–005.	The GO bit is set and cleared under program control. In modes 1, 2, and 3, this bit remains set until cleared by the program. In mode 0 this bit is cleared automatically when the counter overflows. Clearing bit 00 or a BUS INIT resets the counter and stops the counting.
01, 02	MODE	Read/Write 2 1 Mode 0 0 Mode 0 - Single interval 0 1 Mode 1 Repeated interval	The mode is set and cleared under program control and by BUS INIT.

KWV11-C Control Status Register Bit Definition (Cont)

Bit	Name	Function	Set By/Cleared By
		1 0 Mode 2 - External event timing 1 1 Mode 3 - External event timing from zero base	
05 04	RATE	Read/write - These bits select the clock rate or counting source for the counter. S 4 3 Rate 0 0 0 Stop 0 0 1 1 MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 external input 1 1 1 Line (50/60 Hz)	The rate is set and cleared under program control and by BUS INIT
06	INTOV (Interrupt on overflow)	Read/write - When this bit is set, the assertion of OVFLO FLAG generates an interrupt. Interrupt is also generated if bit 06 is set while OVFLO FLAG is set	This bit is set and cleared under program control. If either bit 06 or 07 is cleared while an overflow interrupt request to the processor is pending, the request is canceled.
07	OVFLO FLAG	Read/write to 0 - If bit 06 is set, setting bit 07 generates an interrupt. Bit 07 must be cleared after the interrupt has been serviced to enable further overflow interrupts. If two enabled interrupts are requested at the same time by bits 07 and 10, bit 07 has the higher priority.	This flag is set each time the counter overflows. It is cleared under program control, at the low-to-high transition of the CO bit, or by BUS INIT.

KWV11-C Control Status Register Bit Definition (Cont)

Bit	Name	Function	Set By/Cleared By
06	MAINT ST1	Write only – Setting this bit simulates the firing of ST1. All functions started by ST1 can be exercised under program control by using this bit.	This bit is set under program control. Clearing is not needed. It is always read as a 0.
05	MAINT ST2	Write only – Setting this bit simulates the firing of Schmitt trigger 2. All functions started by ST2 can be exercised under program control by using this bit.	This bit is set under program control. Clearing is not needed. It is always read as a 0.
04	MAINT OSC	Write only – For maintenance purposes, setting this bit simulates one cycle of the internal crystal oscillator used to increment the clock counter (Bit 11 must be set).	This bit is set under program control. Clearing is not needed. It is always read as a 0.
03	DISC (Disable internal oscillator)	Read/write – For maintenance purposes, this bit prevents the internal crystal oscillator from incrementing the clock counter. This bit is used with bit 04.	This bit is set and cleared under program control.
02	FOR (Flag overrun)	Read/write – Flag overrun provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the software.	This flag is set when an overrun occurs and the CWV11-C FLAG (bit 07) is still set from a previous occurrence, or when ST2 fires and the ST2 FLAG (bit 15) has been previously set. Bit 12

KWV11-C Control Status Register Bit Definition (Cont)

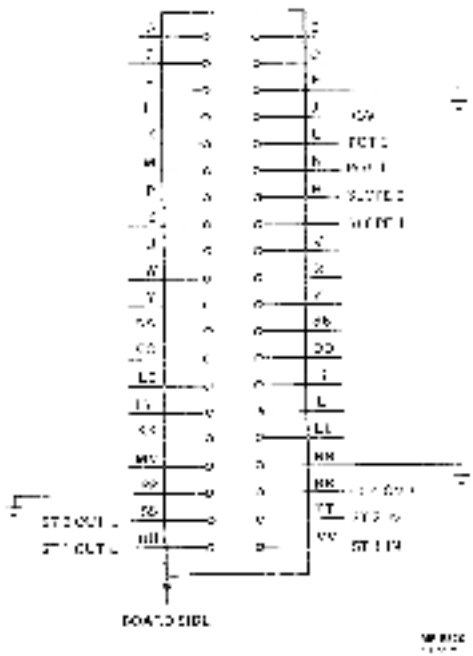
Bit	Name	Function	Set By / Cleared By
			is cleared under program control, at the low-to-high transition of the GO bit, or by BUS INIT.
13	ST2 GO ENABLE	Read/write. When set, the assertion of ST2 FLAG sets the GO bit and clears the ST2 GO ENABLE bit.	The ST2 GO ENABLE bit is cleared under program control, at the low-to-high transition of the GO bit, or by BUS INIT.
14	INT 2 (Interrupt on ST2)	Read/write. When set, the assertion of ST2 FLAG (bit 15) causes an interrupt. If set while ST2 FLAG is set, an interrupt request is generated.	This bit is set and cleared under program control and by BUS INIT. When either bit 14 or 15 is cleared, any pending ST2 interrupt request is cancelled.
15	ST2 FLAG	Read/write to 0. Setting this flag starts an interrupt request if bit 14 is set. Bit 15 must be cleared after servicing an ST2 interrupt to enable further interrupts. If two enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority.	The ST2 FLAG is set by the firing of Schmitt trigger 2 or the setting of the MAINT ST2 bit (in any mode) while the GO bit or the ST2 GO ENABLE bit is set. The ST2 FLAG is cleared under program control or at the low-to-high transition of the GO bit unless the ST2 GO ENABLE bit has previously been set. This bit is also cleared by BUS INIT.

BUFFER/PRESET REGISTER

The address of the buffer/preset register is the standard device address +2, or 172442. This register has two purposes. During mode 0 or 1 operation, this register is used to load the number of clock counts before the counter overflows. During mode 2 or 3 operation, this register is used to read the current count from the counter. Reading the BPR indirectly reads the counter.

I/O INTERFACE

The I/O interface signals use a 3M 4341-7040 connector and are defined in the following figure.



KWV11-C I/O Connector J1 Pin Assignments

KXT11-A SBC-11/21 SINGLE-BOARD COMPUTER

GENERAL

The SBC-11/21 is a single board computer on a dual-height board that interfaces with an LSI-11 bus and/or functions alone. On the board are a 16-bit microprocessor, two asynchronous serial-line units (SLUs), a 21-bit programmable parallel I/O interface, and four 28-pin sockets to accept 24- or 28-pin ROMs or static RAMs.

There are two versions of KXT11 or SBC-11/21 that are designated as revision C and revision D. The modules are interchangeable and each revision has a different printed circuit board layout that changes the designations of the configuration jumper pins. The *M8063 Falcon SBC-11/21 Single-Board Computer User's Guide* (EK-KXT11-UG) supports revision C of the module and the *SBC-11/21 Single Board Computer User's Guide* (EK-SBC11-UG) supports revision D of the module.

Power Requirements

Power Supply

+5.0 V ± 5%	2.1 A (Typical) 2.8 A (Maximum)
−12.0 V ± 5%	30 mA (Typical) used by on-board circuitry 1.1 A (Maximum) includes current supplied to outside world through pin 10 of the serial I/O connector

Battery Back-up

+5.0 V ± 5%	170 mA (Typical) 280 mA (Maximum)

NOTE

The +12.0 V typical current is measured with no connections at pin 10 of the serial I/O connectors (fused line).

Bus Loading

DC	AC
1.0	2.4

Diagnostics

Refer to Appendix A

Related Documentation

M8063 Falcon SBC 11/21 Single-Board Computer User's Guide (Revision C) (EK-KXT11-UG)

SBC 11/21 Single-Board Computer User's Guide (Revision D) (EK-SBC11-UG)

CONFIGURATION

Two versions of the KXT11 SBC exist, and the module should be identified before attempting to configure it. The C revision is identified by the circuit board number, 8014480, located on the module. The D revision is identified by the circuit board number, 8011448D, located on the module. The configuration of the wirewrap pins used to configure the module are different for each revision. Therefore, the configuration requirements for each revision are described separately. The module should be identified as either the C revision or D revision and configured to meet those specific requirements.

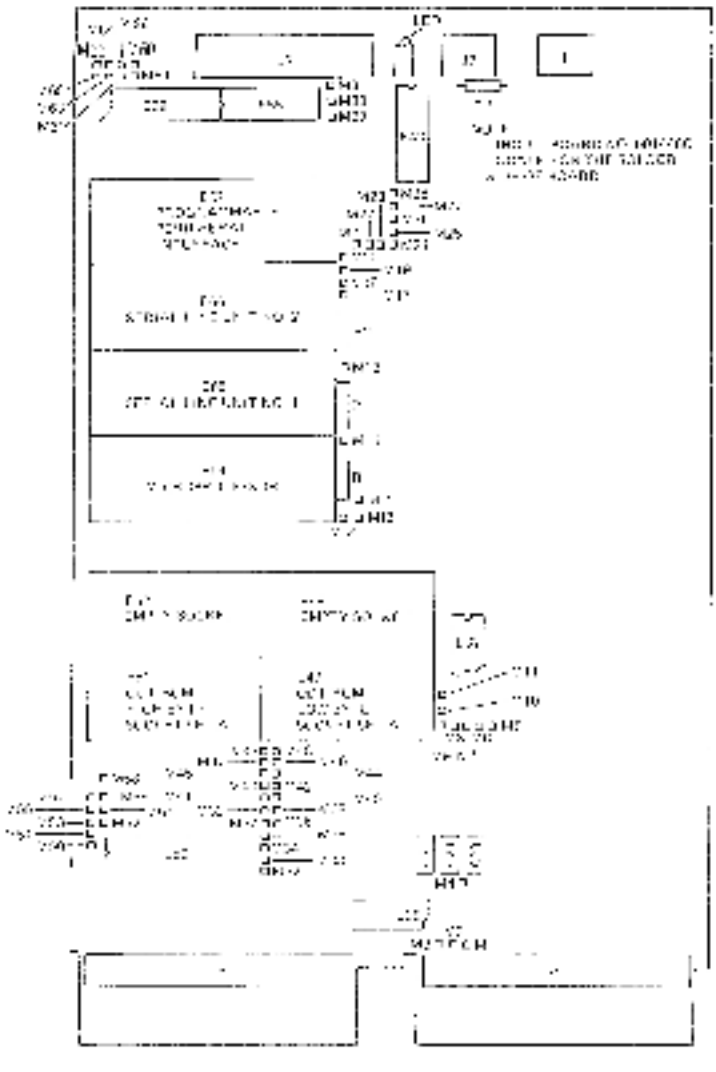
Configuration Requirements for the C Revision

The C revision of the KXT11 has 66 wirewrap pins that are used for configuration. Configuration is done by installing jumper wires between the pins. The pins and their functions are described in the following table.

NOTE

This maintenance information supports the field service configuration only. If the KXT11 is not set to the field service configuration, reconfiguration is necessary.

The KXT11 is usually found in the field service configuration. However, if the KXT11 is new or a replacement from the factory, it is set to the factory standard configuration. Before the KXT11 can run diagnostics, it must be reconfigured to the field service configuration.



KXT11 (SBC-11/21) Pin Layout (Rev C)

KXT11 Revision C Pins and Functions

Pins	Function
M1–M4	Battery backup
M5–M11	Nonmaskable interrupt and trap to the restart address
M12–M14	Serial line unit 1
M15, M16	Power-up
M17–M20	Real-time clock
M21–M24	Memory map decoder
M25–M26	Start address (mode register)
M29–M31	BHALT interrupt (level 7, maskable)
M32–M56	Memory
M58–M66	Parallel input/output

The differences between the field service and factory standard configuration exist in the start address and the line time clock. Both of these functions are reconfigured by removing two jumper wires and adding two. The changes necessary to reconfigure the KXT11 from factory standard to field service configurations are listed below.

For the line time clock:

Remove the wire between M17 and M19.
Place a new wire between M17 and M24.

For the start address:

Remove the wire between M24 and M26.
Place a new wire between M25 and M27.

The detailed field service wirewrap configuration is listed in the following table. No wirewrap jumpers are installed to the pins listed beside NO CONNECTIONS.

NOTE

Identify the module as revision C before configuring it to these requirements.

Field Service Revision C Configuration

Jumpers Between	Function
M1 and M2 M3 and M4	Standard LSI-11 bus power (no battery backup)
No jumpers	Power up circuit enabled
M25 and M26 M26 and M27 M27 and M28	Start address (mode register) Start address: 172000 Restart address: 172004
M22 and M23 M23 and M24	Memories: Memory map 0
M5 and M43 M5 and M54 M41 and M57 M56 and M36 M51 and M57 M32 and M58 M6 and M42 M6 and M52 M44 and M39 M47 and M32 M51 and M40	2K x 8 EPROM
M1 and M8 M7 and M8	Interrupts: Timeout traps to restart address except during LSI-11 bus IAK.
M10 and M14 M30 and M31	SLU 1 break asserts a BHALT signal which is received as a level 7 interrupt (vector 140).
M17 and M24	SLU 2 60 Hz line time clock
M59 and M60	Parallel I/O
M66 and M68	Port A receive data
M61 and M63	Port B transmit data (PC4 input)

Field Service Revision C Configuration (Cont)

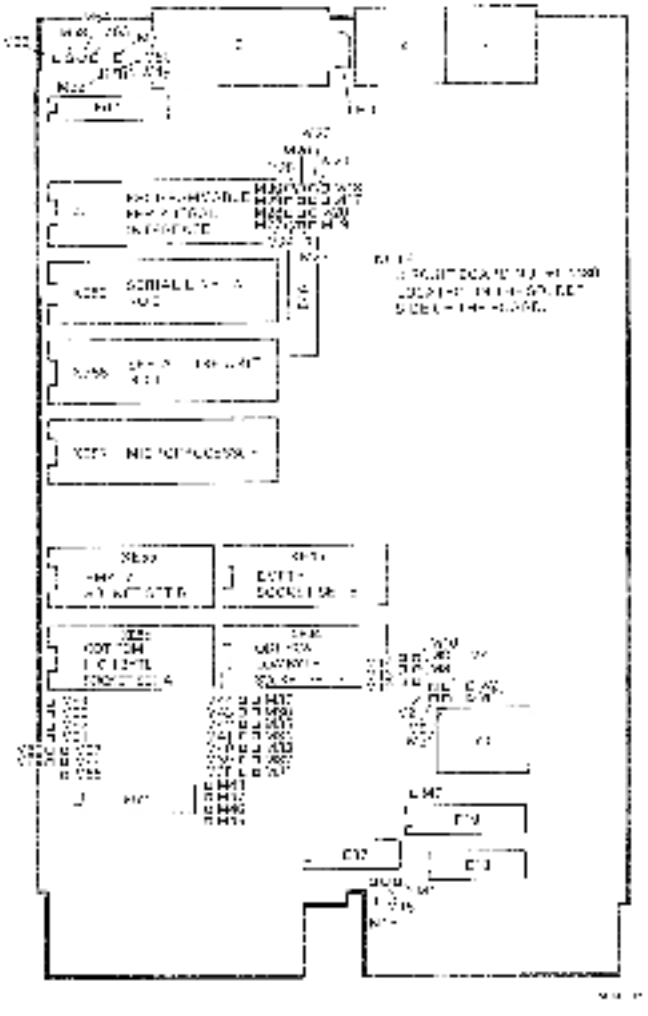
Jumpers Between	Function
M3, M10, M11, M12 M15, M16, M19, M19 M20, M21, M33, M35 M44, M45, M46, M47 M48, M50, M52, M53 M54, M55, M62, M64	NO CONNECTIONS

Configuration Requirements for the D Revision

The D revision of the KXT11 has 65 wirewrap pins that are used for configuration. Configuration is done by installing jumper wires between the pins. The pins and their functions are described below.

KXT11 Revision D Pins and Functions

Pins	Function
M2, M11	Clock oscillator
M1, M7, M15, M16	Battery backup
M5, M9, M10, M12, M13, M14	A nonmaskable interrupt and trap to the restart address
M17, M20, M24	Serial line unit 1
M4, M8	Power-up
M19, M23, M27, M28	Serial line unit 2
M18, M21, M25, M29	Memory map decoder
M18, M22, M26, M30	Start address (mode register)
M3, M5, M8	BHALT interrupt (level 7, maskable)
M31-M48, M50, M60 M57, M59, M60, M61 M62, M63, M64	Memory
M49-M54, M58, M65	Parallel input-output



KXT11 (SBC-11/21) Fin Layout (Rev 0)

NOTE

This maintenance information supports with the field service configuration only. If the KXT11 is not set to the field service configuration, reconfiguration is necessary

The KXT11 is usually found in the field service configuration. However, if the KXT11 is new or a replacement from the factory, it is set to the factory standard configuration. Before the KXT11 can run diagnostics, it must be reconfigured to the field service configuration.

The differences between the field service and factory standard configuration exist in the start address and the line time clock. Both of these functions are reconfigured by removing two jumper wires and adding two wires. The changes necessary to reconfigure the KXT11 from factory standard to field service configurations are as follows.

For the line-time clock:

Remove the wire between M23 and M19.
Place a new wire between M24 and M25.

For the start address:

Remove the wire between M26 and M29.
Place a new wire between M26 and M22.

The detailed field service wirewrap configuration is listed in the following table. No wirewrap jumpers are installed in the pins listed beside NO CONNECTIONS.

NOTE

Identify the module as revision D before configuring it to these requirements.

Field Service Revision D Configuration

Jumpers Between	Function
M1 and M15	Standard LSI-11 bus power (No battery backup)
No jumpers	Wake up circuit enabled
M30 and M26 M26 and M22 M22 and M18	Start address Start address 172000 Restart address 173004
	Memories:
M25 and M21 M21 and M20	Memory map 0
M61 and M40 M59 and M01 M41 and M38 M64 and M60 M46 and M47 M63 and M58 M60 and M62 M39 and M62 M24 and M32 M57 and M52	2K × 8 INTEL EPROM
	Interrupts:
M9 and M13 M14 and M10	Timeout traps to restart address except during LSI-11 bus IAK.
M29 and M17 M5 and M8	SLU #1 break asserts BHALT and BHALT is received as level 7 interrupt (vector 140)
M33 and M29	BEVENT Hz real time clock
M49 and M51 M50 and M52 M54 and M58	Parallel I/O in mode 1: Port A receive data, with STROBE A on PC4 Port B transmit data
M2, M3, M4, M6, M11, M12, M16, M19, M24, M27, M28, M31, M35, M36, M37, M39, M42, M45, M44, M48, M48, M53, M54, M55, M56, M57	No connections

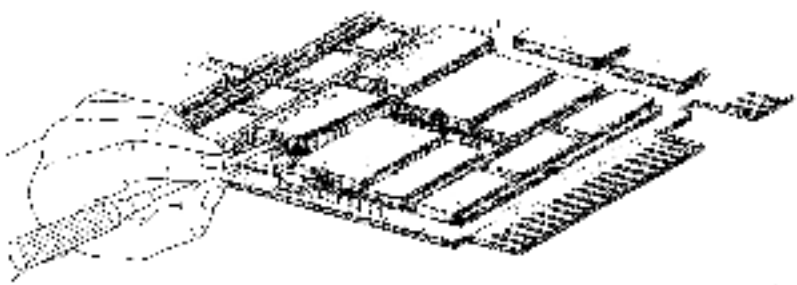
ODT ROMs

Part of the configuration procedure is to make sure that the ODT (on-line debugging technique) ROMs are positioned in the correct sockets. The KXT11 provides four sockets that may be used for ROM (or RAM). In the field service configuration, socket set B is not used. The two sockets that are used for the ODT ROMs are socket set A. The positioning of the ROMs is serious because the sockets have 28 pin locations, while the ROMs have only 24 pins. The ROMs must be placed in pin locations 3 through 26 of each socket. The number one pin of each ROM must be placed in pin location 3 of each socket. The two ODT ROMs are identified by their part numbers as follows.

1. Part number 23-322E2-00 (low byte) is placed in the low byte of socket set A.

2. Part number 23-323E2-00 (high byte) is placed in the high byte of socket set A.

If the KXT11 is new or a replacement from the factory, the ODT ROMs must be removed from the old KXT11 and put in the new. Place a small screwdriver under the chip and lift it gently. This method allows easy removal of both ODT ROMs.



ODT ROM Removal

ODT Self-Test

The ODT self-test is the only test that does not need the installation of the active loopback connector (KXT11-LP). The ODT self-test is automatically run when power is applied to the KXT11. There are two indications of successful completion of the ODT self-test.

1. The light emitting diode (LED) found between J2 and J3 on the KXT11 gives the first indication. While looking at the LED, apply power to the KXT11. If the ODT self-test is successful, the LED lights for approximately one second and then shuts off.

2. The second indication occurs after the autobaud routine. At the completion of the ODT self-test, the KXT11 looks for a carriage return. With the <CR> the KXT11 sets the baud rate and displays @ if the ODT self-test was successful.

If the ODT self-test fails, two indications appear.

1. The LED either lights or remains off and stays that way.
2. The @ is not displayed.

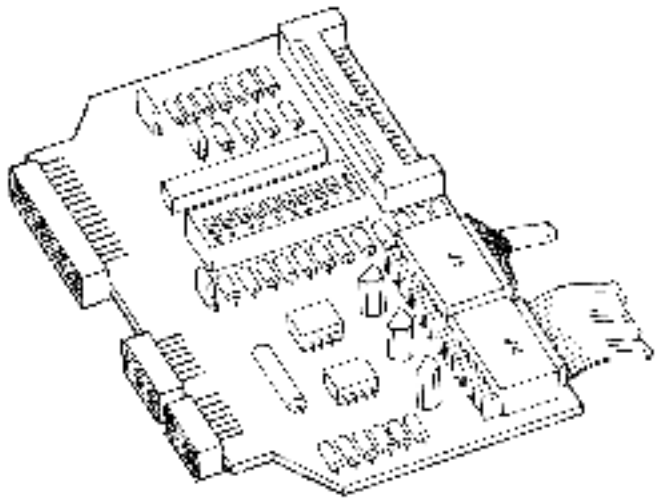
If an error was found during the ODT self-test, the KXT11 should be replaced.

ODT Extended Self-Test

Before the ODT extended self-test or the NKXAA/LH/C diagnostic tests can run, it is necessary to connect the active loopback connector (KXT11-LP). The KXT11-LP has nine switches in an 18-pin dual in-line package (DIP). These switches are used during the loading and running of the diagnostic tests.

CAUTION

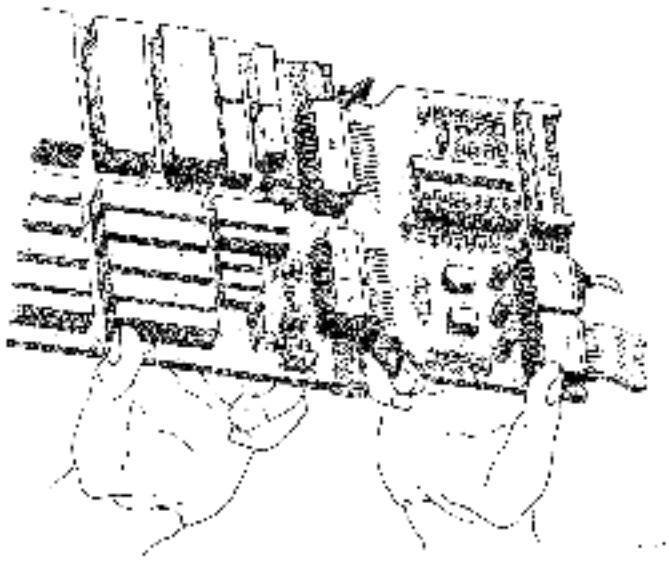
Power must be removed from the KXT11 before installing the KXT11-LP.



Active Loopback Connector (KXT11-LP)

To install the KXT11-LP:

1. Remove the connector from J1 (SLU 1) on the KXT11 and connect it to J5 on the KXT11-LP.
2. If there is a connector in J2 (SLU 2) on the KXT11, remove it and connect it to J4 on the KXT11-LP.
3. If there is a connector in J3 (parallel port) on the KXT11, remove it. This connector will not be reinstalled until testing is complete.
4. Position the KXT11-LP over J1, J2, and J3 on the KXT11, ensure correct alignment, and insert the KXT11-LP into the connectors.



KXT11-LP Installation

It is now necessary to configure the nine switches, found on the top of the KXT11-LP, for the ODT extended self-test.

ODT Extended Self-Test KXT11-LP Switch Configuration

Switch	1	2	3	4	5	6	7	8	9
Position	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF

ON — closed, OFF — open

The ODT extended self-test checks the peripheral parallel interface (parallel port) SLU 2, and the drivers and receivers for SLU 2. To run the ODT extended self-test, enter X on the terminal. If the test runs without errors 000000 is displayed. If an error is encountered during the ODT extended self-test an error message is displayed.

If an error was found during the ODT extended self-test, the KXT11 should be replaced.

ODT Extended Self-Test Error Messages

Message	Explanation		
	Parallel I/O Loopback Test	Internal Serial I/O Loopback Test	External Serial I/O Loopback Test
000000	Passed	Passed	Passed
000001	Failed	Passed	Passed
000010	Passed	Failed	Not performed
000011	Failed	Failed	Not performed
000100	Passed	Passed	Failed
000101	Failed	Passed	Failed