

LSI-11 Systems Service Manual

Volume III

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LAV11 PRINTER INTERFACE

Amperes		Bus Loads		Cables
+5	1.2	AG	DC	
0.5	0	1.8	1.9	3011S (for LA180)
				7009057 (for Communications line printer SM models 101, 101A, 101D, 102A, and 305)

Standard Addresses

LADB 177514

LADB 177516

Vectors

200

Diagnostic Program

Refer to Appendix A.

Related Documentation

LAV11 User's Manual (EK-LAV11-001001)

Field Maintenance Print Set (MP005034)

LA180 WFOprinter Maintenance Manual (EK-LA180-MM)

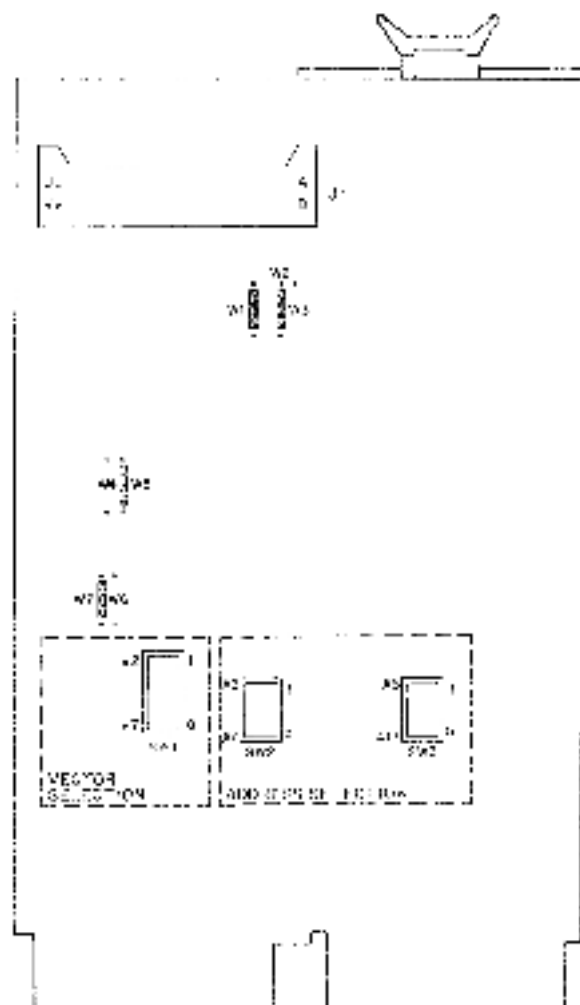
Minicomputer Interfaces Handbook (ED-20175-20)

CAUTIONS

1. **Switching** - Switching the LA180 off-line while the operating system is running a program may result in the computer hanging and crashing the program. If this occurs, type P to continue. This problem does not occur if the LPV11 is used in place of the LAV11.
2. **LA180 to LAV11 Cable** - The only acceptable cable for use between the LA180 and the LAV11 is the DC115. The end labeled P2 must attach to the LA180. The end labeled P1 must be attached to the LAV11.
3. **LA180 Modifications** - On the LA180 logic board (54-11023), jumper W6 must be inserted. This ensures +5 Vdc sense will read the LAV11. Failure to do so will result in a continued error condition in the LAV11 LACS buffer. W6 is located between J2 and J3 on the 54-11023 module.
4. **Miscellaneous Jumpers** - For an LA180, the following jumper configuration must be maintained.

Jumper	Condition	Function if inserted
W1	I	Transmit parity on line
W2	I	+5 Vdc sense from LA180
W3	R	+5 Vdc sense from LAV11
W4	R	DEMAND is asserted low
W5	I	DEMAND is asserted high
W6	R	P STROBE is asserted low
W7	I	P STROBE is asserted high

5. The field replacement for the LAV11 (M7949) is the LPV11 (M8027).



5.4. CASE COORDINATION

TABLE 2		
Category	Frequency	Percentage
Gender	Male	100
	Female	0
	Other	0
	Not specified	0
	Total	100
Age	18-24	100
	25-34	0
	35-44	0
	45-54	0
	Total	100
Education	High school or less	100
	Some college	0
	Bachelor's degree	0
	Master's degree	0
	Total	100

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JURISDICTION	YEAR	STATISTICS
WV	1997	1
MD	1997	2
MA	1997	2
MA	1998	2
MA	1999	2
MA	2000	2
MA	2001	2

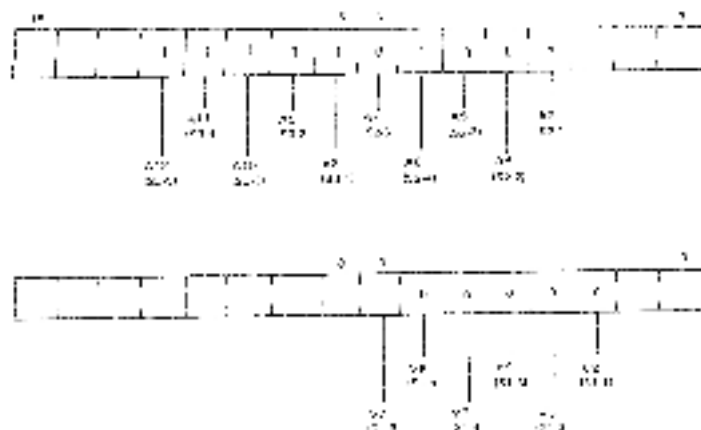
442

T. MEEHAN

2. 4220
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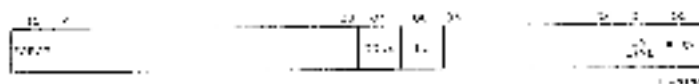
LAV11 Jupiter 9



LAV11 CONTROL REGISTER

DATA 24-2A: 00 00 00 00
 DATA 2B-2F: 00 00 00 00

M. 11.1



LAV11 Control/Status Register (LACS)

LACS Bit Definitions

Bit	Function
15	Error - The error bit is asserted (1) when an error condition (i.e., four or no paper) exists in the line printer. This is a read-only bit, which is reset only by manual correction of the error condition.
14-08	Reserved.
07	Done - The done bit is asserted (1) when the printer is ready to accept another character. This is a read-only bit, set by INT. The done bit is cleared by loading the ALH register. An interrupt sequence is started if IE (interrupt enable, bit 06) is in on act.

LACS Bit Definitions (Cont)

Bit	Function
06	IE - The interrupt enable bit is set or cleared (read or write bit) under program control. It is cleared by the INIT (initialization) signal on the LA11 bus. (INIT is caused by programmed RESET instruction, console start function, or a power-up or power-down condition.) When it is set, an interrupt sequence is started if either error or done is asserted.
05-02	Unused.
01	Online - The on line bit is asserted (1) when the LA180 printer (only) is on-line. Read only.
00	Busy - The busy bit is asserted (1) when the LA180 printer (only) is performing a print or paper advance operation.



LAV11 Data Buffer Register (LADB)

LADB Bit Definitions

Bit	Function
15-06	Unused.
07	Parity - The parity bit is loaded with the data word if the parity jumper is installed. Write only.
05-00	Data - The data comprises seven bits, with bit 06 being the most significant. This buffered 7-bit character will be transferred to the printer. These are all write only bits.

LPV11 LP05/LA180 INTERFACE MODULE

Amps		Bus Loads	Cables	
5	-12	40	DC	
0.8	0	1.4	1	60-118-25 for LA180 70-11212-25 for LP05

Standard Addresses

LP05	177514
LP05	177518

Standard Vector

Data or error interrupt 200

Diagnostic Programs

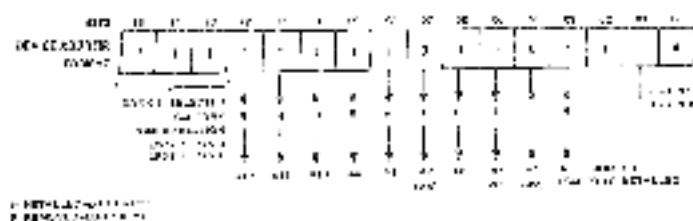
Refer to Appendix A.

Related Documentation

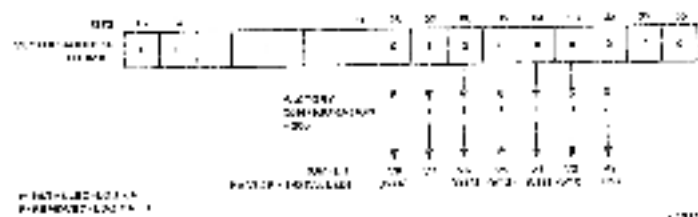
LP05 Line Printer Maintenance Guide (FR 0LP25-01)
LPV11 Printer User's Manual (EK-LPV11-01)
LA180 DECprinter I User's Manual (EK-LA180-01)
LA180 Field Maintenance Print Set (MP-LA150-00)
LA180 DECprinter I Maintenance Manual (EK-LA150-MM)
IBM Technical Manual, Model 2200 Line Printer (Data Products Corporation)
LPV11 V Field Maintenance Print Set (MP00157)
Microcomputer Interfaces Handbook (FR 20175-20)

NOTE

The LPV11 (M3027) is a direct replacement for the LAV11 (M7848).



LPV11 Interrupt Device Address Format and Jumpers



LPV11 Vector Address Format and Jumpers

LPV11 Jumper Definitions

Jumper Designation	Configuration When Shipped	Function
A12	R	Jumper wires W2, W3, and W4 are factory installed to negate address bits 4, 5, and 7, respectively.
A11	R	
A10	R	
A9	P	This sets 77514 as the base address.
A8	P	
A7	I	
A6	P	
A5	I	
A4	I	
A3	P	
V8	I	Jumper wires W5 through W14 are factory installed to negate vector bits 2, 3, 4, 5, 6, and 8.
V7	I	
V6	I	
V5	I	
V4	I	This sets 200 as the interrupt vector.
V3	I	
V2	I	

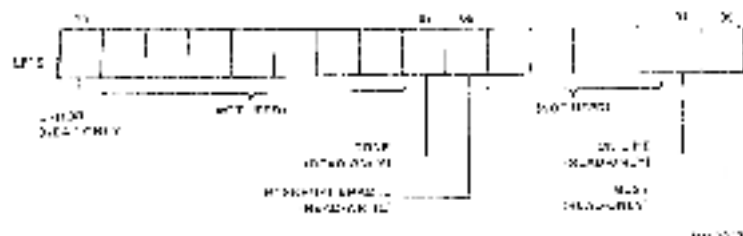
LPV11 Jumper Definitions (Cont)

Jumper Designation	Configuration When Shipped	Function											
D	I	W1 installed to delay BTRPLY L.											
T	R	Supports both uppercase and lowercase printing. For uppercase only, remove W7 and install I.											
W7	I												
		Do not configure the module with both jumpers W7 and T installed.											
P	R	Configured to transfer parity (bit 07) to printer											
W6	I												
<table><tr><th>Parity Option</th><th>Jumper W6</th><th>Jumper P</th></tr><tr><td>Normal parity bit</td><td>Installed</td><td>Removed</td></tr><tr><td>No parity, bit 07 low</td><td>Removed</td><td>Removed</td></tr><tr><td>No parity, bit 07 high</td><td>Removed</td><td>Installed</td></tr></table>			Parity Option	Jumper W6	Jumper P	Normal parity bit	Installed	Removed	No parity, bit 07 low	Removed	Removed	No parity, bit 07 high	Removed
Parity Option	Jumper W6	Jumper P											
Normal parity bit	Installed	Removed											
No parity, bit 07 low	Removed	Removed											
No parity, bit 07 high	Removed	Installed											
		Do not configure the module with both jumpers W6 and P installed.											

NOTE

If the LPV11 interface module is used with an LPOS printer equipped with the Direct Access Vertical Form Unit (DAVFU), it is recommended that the user remove jumper W6. The LPOS interface module does not support the DAVFU Function.

F	R	W6 is installed at F— to enable error filter operation with the LPOS.
F—	O	
		For operation without the error filter, remove W6 and install a jumper at F—.
		Do not configure the module with jumpers installed at both F— and F—.
		The LA180 automatically enables the error filter circuit regardless of the jumper configuration.



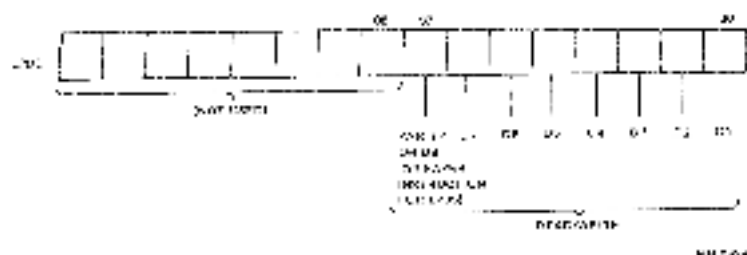
LPC11 Control/Status Register (LPCSR)

LPCS Register Bit Functions

Bit	Function
15	Error: Asserted (1) whenever an error condition exists in the line printer. Error conditions include the following: LPCB errors: • Power off • No paper • Printer drum gate open • Over temperature alarm • PRINT INHIBIT switch off • Printer off-line • Torn paper LA180 errors: • Fault (paper fault) • ON-LINE switch (in OFF position) Reset by manual correction of error condition. If LPOB bit (0) is not set, if bit 06 is set, bit 16 is reset by manual correction of the error and (1) reading the interrupt vector if the interface is "ready," or (2) after reading the LPOB if the interface is "not ready." Feed only.
14-13	Not used. Read as 0s.

LPCS Register Bit Functions (Cont)

Bit	Function
07	Done LPDS - Asserted (1) whenever printer is ready for next character to be loaded, and clears that previous function is either complete or has been started and continued to a point where the printer can accept the next command. This bit is set by the LSI-11 processor asserting HINIT L; inhibit CX is also set, an interrupt sequence is initiated. Also set by the printer when on-line and ready to accept a character. Cleared by loading (writing into) the LPDS register. Inhibited when bit 15 is set. Read only. LA180 - Asserted (1) when the printer is ready to accept another character. Done is set by the LSI-11 processor asserting HINIT L and is cleared by loading (output transfer to) the LPDS register. If the interrupt enable bit is set, setting done will initiate an interrupt request.
06	Interrupt Enable - Set or cleared by the program. Also cleared by the LSI-11 processor asserting BOUT L. When set, an interrupt sequence is initiated if either the error or done bit is set.
05-02	Not used. Read as 0s.
01	On-Line - Not supported and not required by DEC software.
00	Busy - Not supported and not required by DEC software. The following information is for reference only. LA180 - Set when the LA180 prints a line or advances paper. LPDS - Not used. Read as 0.



LPV11 Data Buffer Register (LPDB)

LPDB Register Bit Functions

Bit	Function
15-08	Not used. Read as 0s. Data written into these bits is lost.
07	Parity or Odd - Optional use. Read as 0. LA100 - Optional parity bit
	LP05 - Optional paper instruction bit. Not supported by the LPV11 (read as 0).
06-00	Data - Seven bit ASCII character register. Characters are sequentially output to the printer buffer via this register. Read as all 0s.

LSI-11/2 PROCESSOR MODULE DESIGNATIONS

KD11-HA Dual height LSI-11 processor without memory
 KD11-HB KD11-HA + MSV11-DD 8K word memory
 KD11-HC KD11-HA + MSV11-DD 16K word memory
 KD11-HD KD11-HA + MSV11-DD 32K word memory
 KD11-HF KD11-HA + MSV11-DA 4K word memory
 KD11-HJ KD11-HA + MSV11-A 4K word core memory
 KD11-HU KD11-HA + NRV11-BA

KD11-XA KD11-HA, 2 MSV11-ED 64K word memory (Heathkit)
 KD11-XB KD11-HA, 4 MSV11-ED 128K word memory (Heathkit)
 KD11-XC KD11-HA, 9 MSV11-ED 256K word memory (Heathkit)
 KD11-XD KD11-HA, 3 MSV11-DD (Heathkit)
 KD11-XH KD11-HA, 3 MSV11-DD (Heathkit)
 KD11-XJ KD11-HA, 3 MSV11-DD (Heathkit)

M7270 Specifications

Size: Dual-height module
 Dimensions: 12.34 cm (5.25 in.) x 72.6 cm (2.9 in.)
 Power: +5 Vdc = 1.6A
 +12 Vdc = 500 mA
 Bus Loader: AC = 1.7 unit loads
 DC = 1 unit load

Related Documentation

Microcomputer Processor Handbook (EB-10451-20)
 KD11-HA Print Set (MP-00406)
 LSI-11 Maintenance Card (EK-LS/11-MC)

Jumpers

W1	Always installed — master clock enabled.
W3	Removed — external event interrupt (line clock) enabled. Installed — external event interrupt disabled.

W5 — W5 Mode Selected

R ¹	0	PG at 24 and FS at 28, or halt mode (mode 0).
R	1	QDI microcode (mode 1).
I	0	PG at 1/0000 for user bootstrap (mode 2).
I	1	Special processor microcode; not implemented (mode 3).

Diagnostic Programs

The following diagnostic programs are for use with LSI-11 processors, except for the limitations noted.

VKA4??	LSI-11 basic instruction test.
VKA8??	LSI-11 Extended Instruction Set (EIS) test. This program can be run only on LSI-11 CPUs with the KEV11 (EIS/FIS) or KEV11-DA (DBOL instruction set) options installed.
VKA0??	LSI-11 Floating Point Instruction (FIS) test. This runs only on LSI-11 CPUs that have the KEV11 (EIS/FIS) option (23-0055).
VKA0??	LSI-11 traps test. This diagnostic auto sizes for the EIS, FIS, and DBOL options. - Older versions (Rev B1 and below) require the setting of a pin in the software switch register if EIS, FIS, or DBOL is present. - Rev A diagnostics will not run on D422 or D324 systems because of the D-B instructions.

NOTE

See Appendix A for XXDP+ multimedia assignments.

VKAH??	Basic system exercise. Tests serial line unit, memory, processor, EIS/FIS, clock, and both floppy disks under various conditions. Software switch register must be set for options.

*R = jumper removed; i = jumper installed.

Chip	Vendor Number	DEC Number	V _{DD}	Comments
DATA	CP 1631 B-39	21-11549-01 21-15579-00	0.9 0.9	With ECO's 2007 pattern
CONTROL	CP 1621 B-178	23-00204	0.9	
MICROM-0	CP 1631 B-103	23-00185	0.9	
MICROM-1	CP 1631 B-073	23-00285	0.9	
EIS/PIB (if present) KCV11-A	CP 1631 B-184	23-00385	0.9	

ECO's for Etch Rev E

CS Rev	ECO No	Change
A	1	1. Remove plinking pulse. 2. Generate clock driver V _{CL} from 4-12 V. 3. Move K1 MSTR L from E34-S to E34-A. 4. Rework board.
B	2	Change C31 and C32 from 10-10316-01 to 10-10279-0.
C	3	Change Argol socket to Dandy socket.
F	3A	Allow customer to remove C51.
H	4	Change R18 from 13-10817 to 13-10522.
I	5	Alternate part 11-14292-01 may be used to replace E37.
K	6	Change part E30 from 21-11549-01 to 21-15579-00.

MCV11-D CMOS READ/WRITE MEMORY**GENERAL****MCV11-D Modules**

Model	Memory Capacity	MOS Chips	Module	Number of Chips
MCV11-DA	2K bytes	2K $\times$ 8	MS631-A	4
MCV11-DC	32K bytes	2K $\times$ 8	MS631-C	16

Diagnostic Programs

Refer to Appendix A.

Related Documentation

MCV11-D User's Guide (EK-MCV1D-UG)
 MCV11-D Reference Card (EK-MCV1D-RC)
 Field Maintenance Print Set (MP-BDM6631)

MCV11-D Power

MCV11-DC (32K byte)			
Current and Power	Active Mode	Standby Mode	Data Retention Mode
Current: -5 V (Typ)*	1.20 A	1.22 A	0
-5 V (Max)*	2.16 A	2.15 A	0
-5 V BBU (Typ)†	1 mA	1 mA	9 mA
-5 V BBU (Max)†	2 mA	2 mA	11 mA
Power -5 V (Typ)	6.20 W	6.10 W	.045 W
-5 V (Max)	11.34 W	11.29 W	.073 W
MCV11-DA (8K byte)			
Current: -5 V (Typ)‡	1.20 A	1.19 A	0
-5 V (Max)*	2.09 A	2.08 A	0
-5 V BBU (Typ)†	1 mA	1 mA	9 mA
-5 V BBU (Max)†	2 mA	2 mA	11 mA
Power -5 V Typ	6.00 W	5.95 W	.045 W
-5 V Max	10.97 W	10.92 W	.073 W

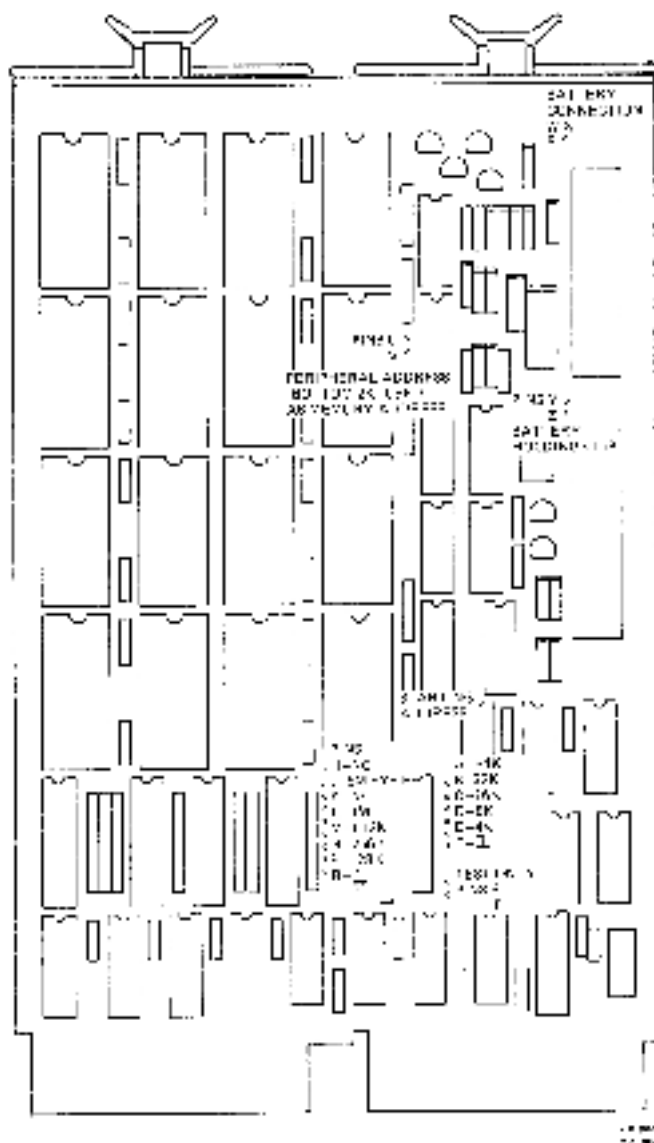
* The +5 V current is recorded with no +5 V BBU supply connected.

† The -5 V BBU current assumes +5 V = 4.75 V and -5 V BBU = 5.25 V. In the active and standby mode, a majority of current comes from the +5 V supply, so it appears as though very little current is required by the -5 V BBU supply. In the data retention mode, the -5 V supply is assumed to be at 0 V. The current supplied by +5 V BBU is used to trickle charge the batteries. If the batteries were disconnected, +5 V BBU would be typically 20 μ A.

CONFIGURING THE MCV11-D MEMORY MODULE

There are five groups of MCV11-D memory module jumpers

1. Module starting address jumpers
2. System selection jumper
3. Manufacturing test jumper
4. Memory I/O page address jumper
5. Memory module battery backup jumper



MCV21-D Module Layout

MCV11-D/M8631

Module Starting Address (MSA) Jumpers

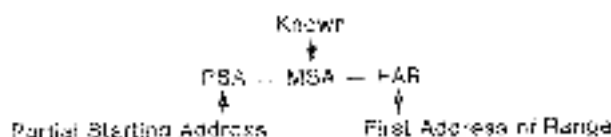
To configure the MSA jumpers, you need the module starting address. From the module starting address you can obtain the necessary data to configure the jumpers.

The first address of range (FAR) selects the first address of the 128K range the starting address falls in.

The partial starting address (PSA) selects which 4K boundary within a specific 128K range the starting address falls in.

You can find the memory module starting address (MSA) by determining how much memory the system has in decimal K words. This word value is the MSA.

To jumper the module starting address (MSA), proceed as follows:



First Address of Range (FAR)

Decimal (K)	Octal	Jumpers in (X) to Ground (R)			
		L	M	N	P
000-124	00000000-00760000				
128-260	01000000-01760000				X
256-388	02000000-02760000			X	
384-508	03000000-03760000			X	X
512-636	04000000-04760000		X		
640-784	05000000-05760000		X		X
788-892	06000000-06760000		X	X	
896-1020	07000000-07760000		X	X	X
1024-1148	10000000-10760000	X			
1152-1276	11000000-11760000	X			X
1280-1404	12000000-12760000	X		X	
1408-1532	13000000-13760000	X		X	X
1536-1660	14000000-14760000	X	X		
1664-1788	15000000-15760000	X	X		X
1792-1916	16000000-16760000	X	X	X	
1920-2044	17000000-17760000	X	X	X	X

Partial Starting Address (PSA)

Decimal (K)	Octal	Jumper to (X) To Ground (F)				
		A	B	C	D	E
0	00000000					
4	00020000					X
8	00040000				X	
12	00080000				X	X
16	00100000			X		
20	00120000			X		X
24	00140000			X	X	
28	00180000			X	X	X
32	00200000		X			
36	00220000		X			X
40	00240000		X		X	
44	00280000		X		X	X
48	00300000		X	X		
52	00320000		X	X		X
56	00340000		X	X	X	
60	00360000		X	X	X	X
64	00400000	X				
68	00420000	X				X
72	00440000	X			X	
76	00460000	X			X	X
80	00500000	X		X		
84	00520000	X		X		X
88	00540000	X		X	X	
92	00560000	X		X	X	X
96	00600000	X	X			
100	00620000	X	X			X
104	00640000	X	X		X	
108	00660000	X	X		X	X
112	00700000	X	X	X		
116	00720000	X	X	X		
120	00740000	X	X	X	X	
124	00760000	X	X	X	X	X

Module Starting Address (Example -- 352K Words)

Names	First Address of Range (FAR)				Partial Starting Address (PSA)				
Decimal k words Binary address	1Meg	512K	256K	128K	64K	32K	16K	8K	4K
Values									
BDAL	21	20	19	18	17	16	15	14	13
BDAL bits	0	0	1	0	1	1	0	0	0
Jumper pin names	L	M	N	P	A	B	C	D	E
Jumper pins	N to H				A to E, B to F				

System Selection Jumper

Small/large system select on is set by the condition of jumper pin J. Small systems use 16- or 18-bit addressing, with pin J open. Large systems use 22-bit addressing, with pin J wrapped to pin R.

Manufacturing Test Jumper

This jumper, when installed (pin T to pin S), allows addresses to start at 128K. The jumper is installed during manufacturing test. When the modules leave manufacturing test, the jumper is removed.

Memory I/O Page Address Jumper

When a customer wants to use the bottom 2K of the I/O space as a memory address, jumper U to V.

Memory Module Battery Backup Jumper

When you receive an MCV11-D memory, there will be two 1.5 V rechargeable nickel batteries. Pins Y and Z are the clip carrier pins (no electrical function); they should have a clip across them. Remove the clip and connect it across pins W and X. This installs module battery backup.

MRV11-AA READ-ONLY MEMORY

A PROM/ROM module will accept up to 16 customer-supplied addressable UV-PROMs, fusible Pk PROMs, or masked ROM devices.

Amps	Bus Loads		Cables	
	-5	-12	A0	B0
W/O PROMs (0.6 max.)	0.4	0	1.0A	1.0
With PROMs (4.1 max.)	2.0	0		

Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 addresses (0 - 777).

Vectors: Diagnostic Program, Exerciser Program

None

Related Documentation

Field Maintenance Print Set (MP00088)

Microcomputer Processor Handbook (E5-18451-20)

NOTES

1. Jumpers W8-W14 select chip set types (512 or 256).
2. Any row not populated with PROMs must have the BRFLY L jumper (W0-W7) removed.

MMIO 11-0A Address Wire Formats

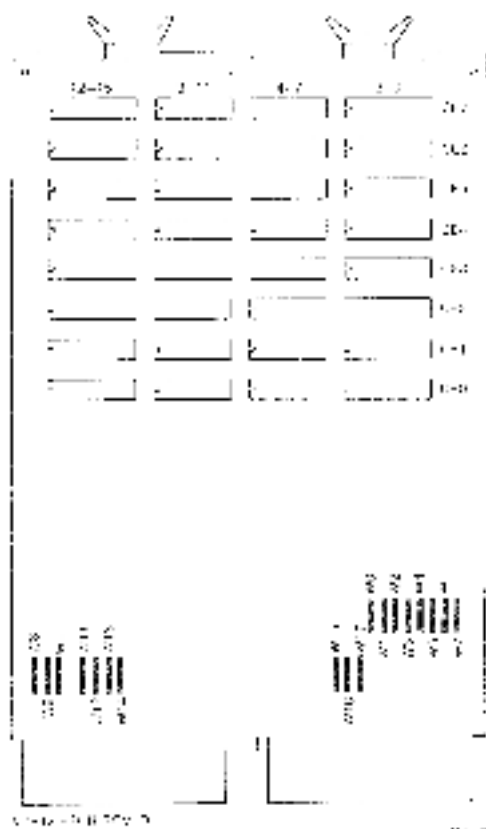
Bank	Bank Select		
	W15	W16	W17
0	1	1	1
1	1	1	R
2	1	R	1
3	1	R	R
4	R	1	1
5	R	1	R
6	R	R	
7	R	R	R

NOTE

Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.



MDM11-A Address Word Format



M7942 E1ch; Rev D

512 by 4-Bit PROM Addresses

Bank Address Jumpers			Word/Byte Address	Physical Row	BRPLY L Jumper
W15	W16	W17			
I	I	I	0-3777	CE0	W0
I	I	R	4000-3777	CE1	W1
I	R	I	4000-5777	CE2	W2
I	R	R	6000-7777	CE3	W3
R	I	I	10000-11777	CE4	W4
R	I	R	12000-13777	CE5	W5
R	R	I	14000-15777	CE6	W6
R	R	R	16000-17777	CE7	W7

256 by 4-Bit ROM Addresses

Bank Address Jumpers			Word/Byte Address		Physical Row	BRPLY L Jumper
W15	W16	W17	W13 Installed W14 Removed	W13 Removed W14 Installed		
I	I	I	0-7776	00000-10776	CE0	W0
I	I	R	10000-17776	11000-117776	CE2	W2
I	R	I	20000-27776	120000-127776	CE4	W4
I	R	R	30000-37776	130000-137776	CE6	W6
R	I	I	40000-47776	140000-147776	CE	W1
R	I	R	50000-57776	150000-157776	CE3	W3
R	R	I	60000-67776	160000-167776	CE5	W5
R	R	R	70000-77776	170000-177776	CE7	W7

BRPLY Select

Empty Row	Remove Jumper
CE0	W0
CE1	W1
CE2	W2
CE3	W3
CE4	W4
CE5	W5
CE6	W6
CE7	W7

MRV11-BA ULTRAVIOLET PROM-EPROM

The MRV11-BA is a high density multifunction module with two independently configurable, asynchronous serial lines which are compatible with RS232-C and RS-423.

	Amps		Bus Loads		Cables
	5	12	AC	DC	
W/O PROM	0.58 (0.67 max.)	0.54	2.5 (0.41 max.)	1.0	None
With PROMs	0.82 (0.744 max.)	0.5	(0.6 max.)		

Standard Addresses

RAMs 20000-20777
PROMs 140000-157777

Standard Vectors

None

Diagnostic Programs

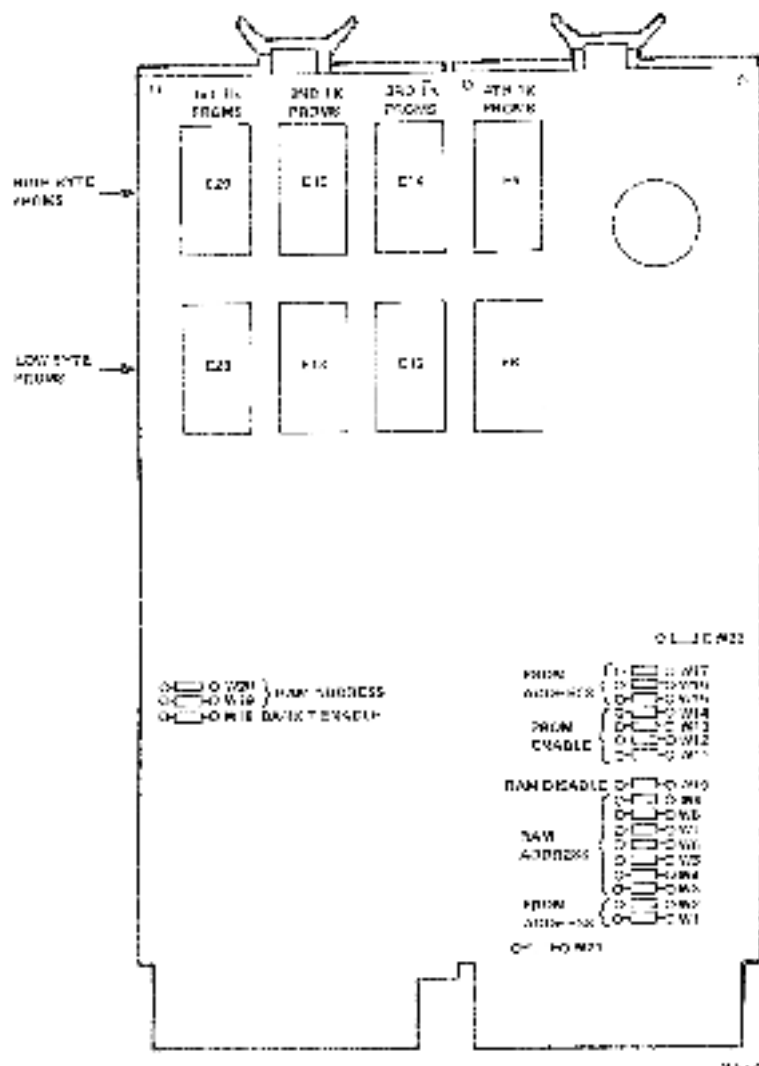
Refer to Appendix A.

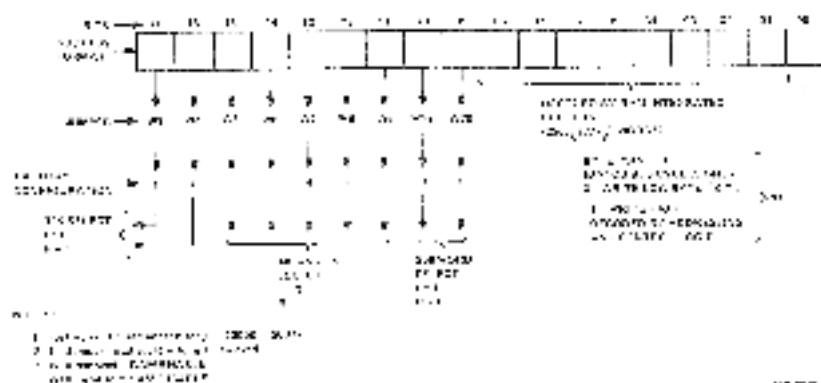
Related Documentation

MRV11-BA LSI-11 UV PROM-EPROM User's Manual (PK MRV11 TM)
Field Maintenance Print Set (MP00864)
Microcomputer Processor Handbook (EE-18451-20)

Recommended PROM Types

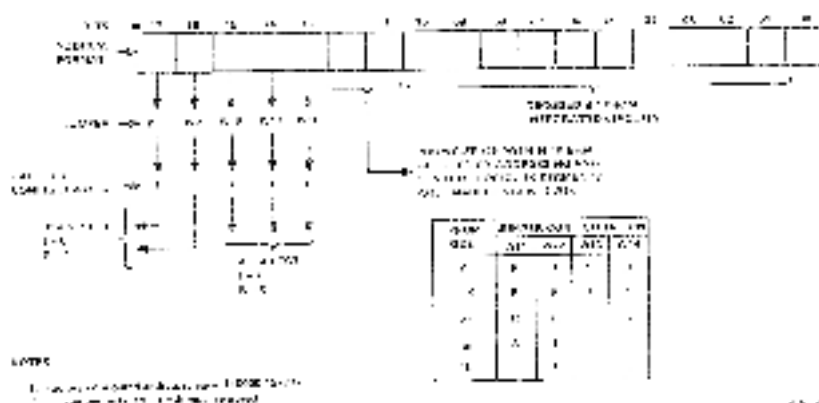
DEC MRV11-BA Intel 2708 1024 X 8-bit, MOS, 1st state, erasable,
(140000-157777) ultraviolet (24-pin DIP)





000000

MRV11-BA RAM Addressing



000000

MRV11-BA PHOM Addressing

RAM Addressing Summary

Address Range (Octal)	Memory Jumper Configuration (I—Installed, R—Removed)										
	Bank	W3	W4	W5	W6	W7	W8	W9	W10	W20	
000000-001777	0	I	I	I	I	I	I	I	R	R	
001000-001777	0	I	I	I	I	I	I	I	R	I	
002000-002777	0	I	I	I	I	I	I	I	I	R	
003000-003777	0	I	I	I	I	I	I	I	I	I	
004000-004777	0	I	I	I	I	I	I	R	R	I	
005000-005777	0	I	I	I	I	I	I	R	R	I	
006000-006777	0	I	I	I	I	I	I	R	I	I	
007000-007777	0	I	I	I	I	I	I	R	I	I	
010000-010777	0	I	I	I	I	I	R	I	I	R	
011000-011777	0	I	I	I	I	I	R	I	R	I	
012000-012777	0	I	I	I	I	I	R	I	I	I	
013000-013777	0	I	I	I	I	I	R	I	I	I	
014000-014777	0	I	I	I	I	I	R	R	R	I	
015000-015777	0	I	I	I	I	I	R	R	R	I	
016000-016777	0	I	I	I	I	I	R	R	I	R	
017000-017777	0	I	I	I	I	I	R	R	I	I	
020000-020777	1	I	I	I	I	R	I	I	R	R	
021000-021777	1	I	I	I	I	R	I	I	R	I	
022000-022777	1	I	I	I	I	R	I	I	I	R	
023000-023777	1	I	I	I	I	R	I	I	I	I	
024000-024777	1	I	I	I	I	R	I	R	R	I	
025000-025777	1	I	I	I	I	R	I	R	R	I	
026000-026777	1	I	I	I	I	R	I	R	I	R	
027000-027777	1	I	I	I	I	R	I	R	I	I	
030000-030777	1	I	I	I	I	R	R	I	R	R	
031000-031777	1	I	I	I	I	R	R	I	R	I	
032000-032777	1	I	I	I	I	R	R	I	I	R	
033000-033777	1	I	I	I	I	R	R	I	I	I	
034000-034777	1	I	R	I	I	R	R	R	R	R	
035000-035777	1	I	I	I	I	R	R	R	R	I	
036000-036777	1	I	I	I	I	R	R	R	I	R	
037000-037777	1	I	I	I	I	R	R	R	I	I	
040000-040777	2	I	I	I	R	I	I	I	R	R	
041000-041777	2	I	I	I	R	I	I	I	R		
042000-042777	2	I	I	I	R	I	I	I		R	
043000-043777	2	I	I	I	R	I	I	I		I	
044000-044777	2	I	I	I	R	I	I	R	R	R	
045000-045777	2	I	I	I	R	I	I	R	R	I	
046000-046777	2	I	I	I	R		I	R	I	R	
047000-047777	2	I	I	I	R		I	R	I	R	

RAM Addressing Summary (Cont)

Address	Memory Jumper Configuration (I—Installed R—Removed)									
	Bank	W3	W4	W5	W6	W7	W8	W9	W19	W20
000000-000777	2	I	I	I	R	I	R	I	I	I
001000-001777	2	I	I	I	R	I	R	I	R	I
002000-002777	2	I	I	I	R	I	R	I	I	R
003000-003777	2	I	I	I	R	I	R	I	I	I
004000-004777	2	I	I	I	R	I	R	R	R	R
005000-005777	2	I	I	I	R	I	R	R	R	I
006000-006777	2	I	I	I	R	I	R	R	I	I
007000-007777	2	I	I	I	R	I	R	R	I	I
008000-008777	3	I	I	I	I	R	I	I	I	R
009000-009777	3	I	I	I	I	R	I	I	R	I
010000-010777	2	I	I	I	I	R	I	I	I	R
011000-011777	3	I	I	I	I	R	I	I	I	I
012000-012777	3	I	I	I	I	R	I	I	I	I
013000-013777	3	I	I	I	I	R	I	R	R	R
014000-014777	3	I	I	I	I	R	I	R	R	R
015000-015777	3	I	I	I	I	R	I	R	R	I
016000-016777	3	I	I	I	I	R	I	R	R	I
017000-017777	3	I	I	I	I	R	I	R	R	I
018000-018777	3	I	I	I	I	R	I	R	R	I
019000-019777	3	I	I	I	I	R	I	R	R	I
020000-020777	3	I	I	I	I	R	I	R	R	I
021000-021777	3	I	I	I	I	R	I	R	R	I
022000-022777	3	I	I	I	I	R	I	R	R	I
023000-023777	3	I	I	I	I	R	I	R	R	I
024000-024777	3	I	I	I	I	R	I	R	R	I
025000-025777	3	I	I	I	I	R	I	R	R	I
026000-026777	3	I	I	I	I	R	I	R	R	I
027000-027777	3	I	I	I	I	R	I	R	R	I
028000-028777	3	I	I	I	I	R	I	R	R	I
029000-029777	3	I	I	I	I	R	I	R	R	I
030000-030777	3	I	I	I	I	R	I	R	R	I
031000-031777	3	I	I	I	I	R	I	R	R	I
032000-032777	3	I	I	I	I	R	I	R	R	I
033000-033777	3	I	I	I	I	R	I	R	R	I
034000-034777	3	I	I	I	I	R	I	R	R	I
035000-035777	3	I	I	I	I	R	I	R	R	I
036000-036777	3	I	I	I	I	R	I	R	R	I
037000-037777	3	I	I	I	I	R	I	R	R	I
038000-038777	3	I	I	I	I	R	I	R	R	I
039000-039777	3	I	I	I	I	R	I	R	R	I
040000-040777	3	I	I	I	I	R	I	R	R	I
041000-041777	3	I	I	I	I	R	I	R	R	I
042000-042777	3	I	I	I	I	R	I	R	R	I
043000-043777	3	I	I	I	I	R	I	R	R	I
044000-044777	3	I	I	I	I	R	I	R	R	I
045000-045777	3	I	I	I	I	R	I	R	R	I
046000-046777	3	I	I	I	I	R	I	R	R	I
047000-047777	3	I	I	I	I	R	I	R	R	I
048000-048777	3	I	I	I	I	R	I	R	R	I
049000-049777	3	I	I	I	I	R	I	R	R	I
050000-050777	3	I	I	I	I	R	I	R	R	I
051000-051777	3	I	I	I	I	R	I	R	R	I
052000-052777	3	I	I	I	I	R	I	R	R	I
053000-053777	3	I	I	I	I	R	I	R	R	I
054000-054777	3	I	I	I	I	R	I	R	R	I
055000-055777	3	I	I	I	I	R	I	R	R	I
056000-056777	3	I	I	I	I	R	I	R	R	I
057000-057777	3	I	I	I	I	R	I	R	R	I
058000-058777	3	I	I	I	I	R	I	R	R	I
059000-059777	3	I	I	I	I	R	I	R	R	I
060000-060777	3	I	I	I	I	R	I	R	R	I
061000-061777	3	I	I	I	I	R	I	R	R	I
062000-062777	3	I	I	I	I	R	I	R	R	I
063000-063777	3	I	I	I	I	R	I	R	R	I
064000-064777	3	I	I	I	I	R	I	R	R	I
065000-065777	3	I	I	I	I	R	I	R	R	I
066000-066777	3	I	I	I	I	R	I	R	R	I
067000-067777	3	I	I	I	I	R	I	R	R	I
068000-068777	3	I	I	I	I	R	I	R	R	I
069000-069777	3	I	I	I	I	R	I	R	R	I
070000-070777	3	I	I	I	I	R	I	R	R	I
071000-071777	3	I	I	I	I	R	I	R	R	I
072000-072777	3	I	I	I	I	R	I	R	R	I
073000-073777	3	I	I	I	I	R	I	R	R	I
074000-074777	3	I	I	I	I	R	I	R	R	I
075000-075777	3	I	I	I	I	R	I	R	R	I
076000-076777	3	I	I	I	I	R	I	R	R	I
077000-077777	3	I	I	I	I	R	I	R	R	I
078000-078777	3	I	I	I	I	R	I	R	R	I
079000-079777	3	I	I	I	I	R	I	R	R	I
080000-080777	3	I	I	I	I	R	I	R	R	I
081000-081777	3	I	I	I	I	R	I	R	R	I
082000-082777	3	I	I	I	I	R	I	R	R	I
083000-083777	3	I	I	I	I	R	I	R	R	I
084000-084777	3	I	I	I	I	R	I	R	R	I
085000-085777	3	I	I	I	I	R	I	R	R	I
086000-086777	3	I	I	I	I	R	I	R	R	I
087000-087777	3	I	I	I	I	R	I	R	R	I
088000-088777	3	I	I	I	I	R	I	R	R	I
089000-089777	3	I	I	I	I	R	I	R	R	I
090000-090777	3	I	I	I	I	R	I	R	R	I
091000-091777	3	I	I	I	I	R	I	R	R	I
092000-092777	3	I	I	I	I	R	I	R	R	I
093000-093777	3	I	I	I	I	R	I	R	R	I
094000-094777	3	I	I	I	I	R	I	R	R	I
095000-095777	3	I	I	I	I	R	I	R	R	I
096000-096777	3	I	I	I	I	R	I	R	R	I
097000-097777	3	I	I	I	I	R	I	R	R	I
098000-098777	3	I	I	I	I	R	I	R	R	I
099000-099777	3	I	I	I	I	R	I	R	R	I

RAM Addressing Summary (Cont)

Address	Memory Jumper Configuration (I—Installed, R—Removed)										
Range (Octal)	Bank	W3	W4	W5	W6	W7	W8	W9	W10	W11	
120000–120777	B	I	I	R	I	I	I	I	R	R	
121000–121777	B	I	I	R	I	R	I	I	R	I	
122000–122777	B	I	I	R	I	R	I	I	I	R	
123000–123777	B	I	I	R	I	R	I	I	I	I	
124000–124777	B	I	I	R	I	R	I	R	R	R	
125000–125777	B	I	I	R	I	R	I	R	R	I	
126000–126777	B	I	I	R	I	R	I	R	I	R	
127000–127777	B	I	I	R	I	R	R	I	R	R	
128000–128777	B	I	I	R	I	R	R	I	R	I	
129000–129777	B	I	I	R	I	R	R	I	R	I	
130000–130777	B	I	I	R	I	R	R	I	I	R	
131000–131777	B	I	I	R	I	R	R	I	I	I	
132000–132777	B	I	I	R	I	R	R	I	I	R	
133000–133777	B	I	I	R	I	R	R	I	I	I	
134000–134777	B	I	I	R	I	R	R	R	R	R	
135000–135777	B	I	I	R	I	R	R	R	R	I	
136000–136777	B	I	I	R	I	R	R	R	I	R	
137000–137777	B	I	I	R	I	R	R	R	I	I	
140000–140777	B	I	I	R	R	I	I	I	R	R	
141000–141777	B	I	I	R	R	I	I	I	R	I	
142000–142777	B	I	I	R	R	I	I	I	I	R	
143000–143777	B	I	I	R	R	I	I	I	I	I	
144000–144777	B	I	I	R	R	I	I	R	R	R	
145000–145777	B	I	I	R	R	I	I	R	R	I	
146000–146777	B	I	I	R	R	I	I	R	I	R	
147000–147777	B	I	I	R	R	I	I	R	I	I	
148000–148777	B	I	I	R	R	I	R	I	R	R	
149000–149777	B	I	I	R	R	I	R	I	R	I	
150000–150777	B	I	I	R	R	I	R	I	R	I	
151000–151777	B	I	I	R	R	I	R	I	R	I	
152000–152777	B	I	I	R	R	I	R	I	I	R	
153000–153777	B	I	I	R	R	I	R	I	I	I	
154000–154777	B	I	I	R	R	I	R	R	R	R	
155000–155777	B	I	I	R	R	I	R	R	R	I	
156000–156777	B	I	I	R	R	I	R	R	I	R	
157000–157777	B	I	I	R	R	I	R	R	I	I	
158000–158777	B	I	I	R	R	R	I	R	R	R	
159000–159777	B	I	I	R	R	R	I	R	R	I	
160000–160777	B	I	I	R	R	R	I	R	I	R	

*The bank 7 enable jumper W16 is factory installed to allow addressing in bank 7.

RAM Addressing Summary (Cont)

Address	Memory Jumper Configuration (1 = Installed; 0 = Removed)										
Range (Octal)	Bank	W3	W4	W5	W6	W7	W8	W9	W10	W20	
167000-167777	7*	1	1	0	0	0	1	0	1	1	
170000-170777	7*	1	1	0	0	0	0	1	0	0	
171000-171777	7*	1	1	0	0	0	0	1	0	1	
172000-172777	7*	1	1	0	0	0	0	1	1	0	
173000-173777	7*	1	1	0	0	0	0	1	1	1	
174000-174777	7*	1	1	0	0	0	0	0	0	0	
175000-175777	7*	1	1	0	0	0	0	0	0	1	
176000-176777	7*	1	1	0	0	0	0	0	1	0	
177000-177777	7*	1	1	0	0	0	0	0	1	1	

*The bank 7 enable jumper W10 is factory installed to allow addressing in bank 7.

NOTE

The following jumper configurations illustrate configuring the address range in banks above bank 7 (not implemented in present LSI-11 system configurations). WB, W3, W19, and W26 can be configured as shown in the preceding pages to select the desired segment within the bank.

Address Range (Octal)	Memory Jumper Configuration (I - Installed, R - Removed)					
	Bank	W3	W4	W5	W6	W7
200000-217777	10	I	R	I	I	I
220000-237777	11	I	R	I	I	R
240000-257777	12	I	R	I	R	I
260000-277777	13	I	R	I	R	R
280000-297777	14	I	R	R	I	I
300000-317777	15	I	R	R	I	R
320000-337777	16	I	R	R	R	I
340000-357777	17	I	R	R	R	R
360000-377777	20	R	I	I	I	I
400000-417777	21	R	I	I	I	R
420000-437777	22	R	I	I	R	I
440000-457777	23	R	I	I	R	R
460000-477777	24	R	I	R	I	I
480000-497777	25	R	I	R	I	R
500000-517777	26	R	I	R	R	I
520000-537777	27	R	I	R	R	R
540000-557777	30	R	R	I	I	I
560000-577777	31	R	R	I	I	R
580000-597777	32	R	R	I	R	I
600000-617777	33	R	R	I	R	R
620000-637777	34	R	R	R	I	I
640000-657777	35	R	R	R	I	R
660000-677777	36	R	R	R	R	I
680000-697777	37	R	R	R	R	R

PROM Addressing Summary

Address	Memory Jumper Configuration (I – Installed; R – Removed)					
	Bank	W1	W2	W15	W17	W18
000000–017777	0	I	I	R	Π	Π
020000–037777	1	I	I	R	Π	I
040000–057777	2	I	I	Π	I	R
060000–077777	3	I	I	Π	I	I
100000–117777	4	I	I	I	R	R
120000–137777	5	I	I	I	R	I
140000–157777	6	I	I	I	I	R
160000–177777	7*	I	I	I	I	I
200000–217777	10	I	R	R	Π	R
220000–237777	11	I	R	Π	R	I
240000–257777	12	I	R	R	I	R
260000–277777	13	I	R	R	I	I
300000–317777	14	I	Π	I	R	R
320000–337777	15	I	R	I	R	I
340000–357777	16	I	R	I	I	R
360000–377777	17	I	R	I	I	I
400000–417777	20	R	I	R	R	R
420000–437777	21	R	I	R	R	I
440000–457777	22	R	I	Π	I	R
460000–477777	23	R	I	R	I	I
500000–517777	24	R	I	I	R	R
520000–537777	25	R	I	I	R	I
540000–557777	26	R	I	I	I	R
560000–577777	27	R	I	I	I	I
600000–617777	30	R	R	R	R	R
620000–637777	31	R	R	R	R	I
640000–657777	32	R	R	R	I	Π
660000–677777	33	Π	R	R	I	I
700000–717777	34	R	R	I	R	R
720000–737777	35	R	R	I	R	I
740000–757777	36	R	Π	I	I	R
760000–777777	37	Π	R	I	I	I

*The bank 7 jumper on W18 is factory installed to allow addressing in Bank 7.

PROM Addressing

Address* Octal Binary	10 22	08 23	08 1	07 2	06 3	06 4	04 5	03 6	02 7	01 8	Address Bits PROM Pins
0 00000000000	L	L	L	L	L	L	L	L	L	L	Actual Logic Levels Required (1024 ₁₀ Locations)
2 00000000100	L	L	L	L	L	L	L	L	L	H	
4 00000001000	L	L	L	L	L	L	L	L	H	L	
6 00000001100	L	L	L	L	L	L	L	L	H	L	
10 00000010000	L	L	L	L	L	L	L	H	L	L	
12 00000010100	L	L	L	L	L	L	L	H	L	H	
14											
16											
3776 11111111110	H	H	H	H	H	H	H	H	H	H	

*Bit 9 address bit 0 is not used. Therefore, only even-numbered addresses are shown.

MRV11-C READ-ONLY MEMORY MODULE

The MRV11-C is a flexible, high-density ROM module used with the L51-11 bus. The module contains 128 wirewrap pins and 16 24-pin ROM chip sockets that use a variety of user-supplied ROM chips. Masked ROMs, bubble ROMs, and ultraviolet erasable PROMs are acceptable to use. The MRV11-C is shipped without jumpers installed.

Using 4K X 8 ROM chips, the total capacity of one M2048 module can be 64K bytes, accessible either by direct access or window mapping.

Amperes		Bus Loads		Cables
		AC	DC	
1.5 0.5	1-12	2	1	None

(plus ROM chip power)

Standard Addresses

Recommended window starting address 780000

Bootstrap starting address: 16-bit system 173000; 18-bit system 773000

Technical related information is beyond the scope of this manual. Additional information can be found in the *Minicomputer Processor Handbook*, EB-15451-20.

Related Documentation

MRV11-C Universal PROM Module User Guide (EK-MRV11-UG-001)

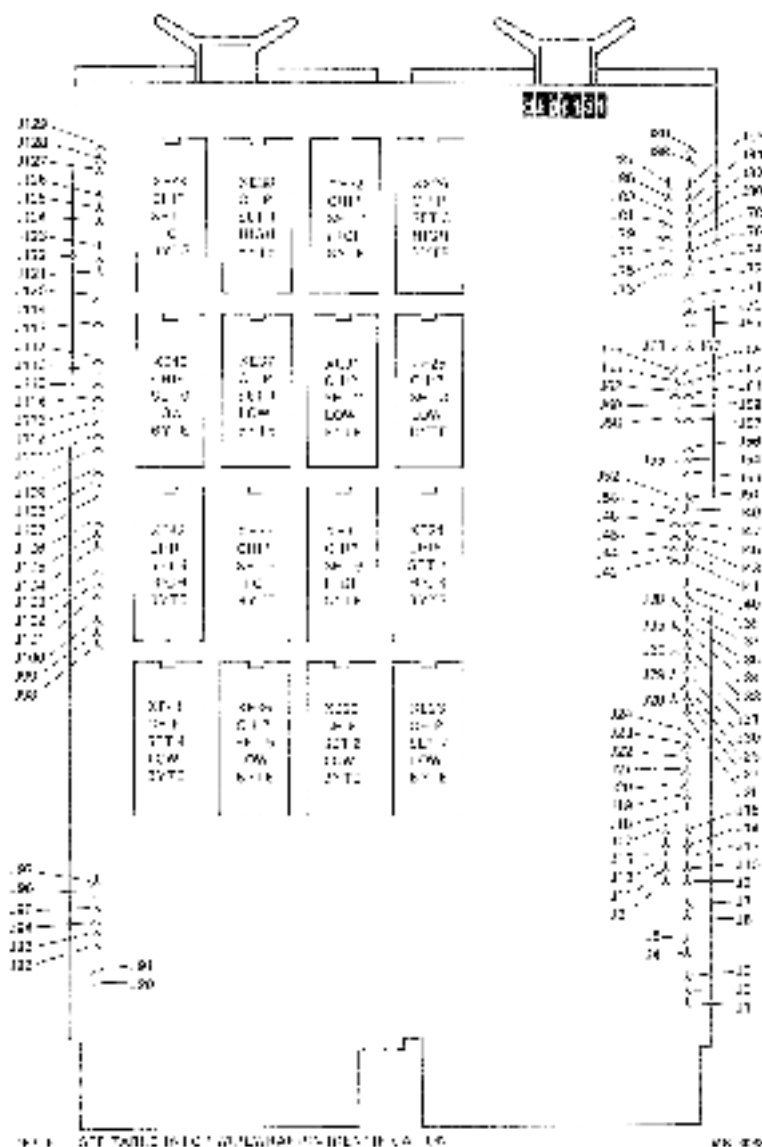
Field Maintenance Print Set (MP-00871)

Compatible UV PROMs (Ultraviolet)

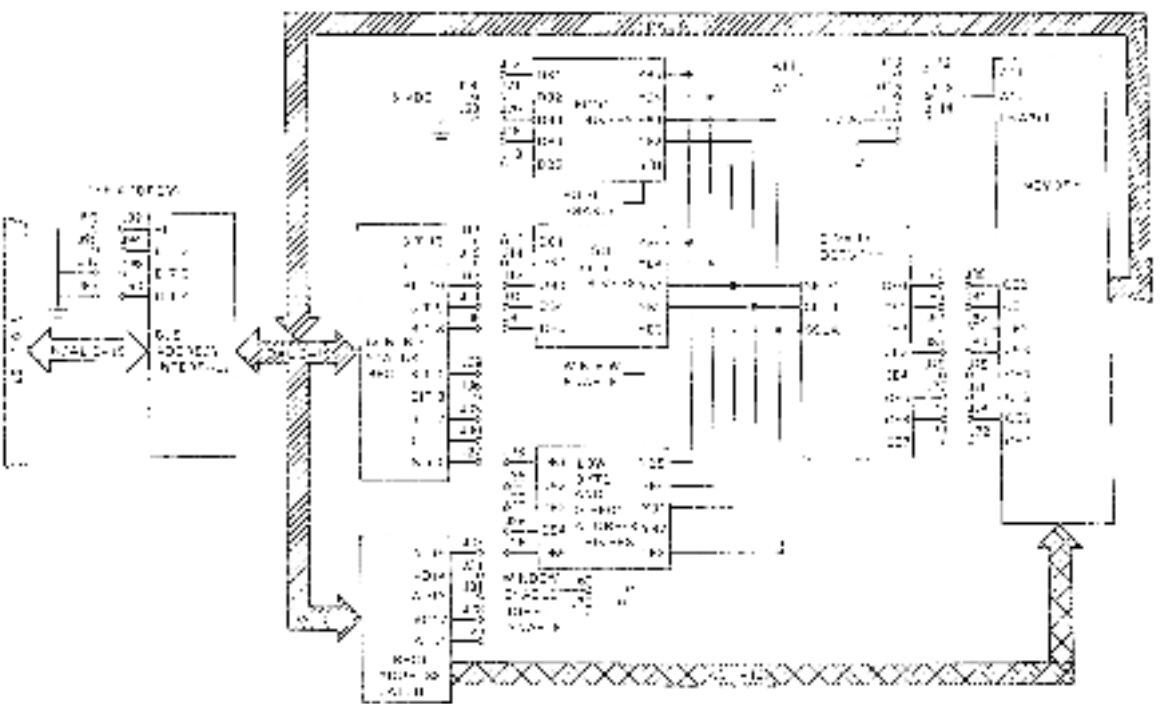
UV PROMs	Chip Array Size	Maximum Memory Size
Intel 2756	1K $\times$ 8	16K bytes
Intel 2716	2K $\times$ 8	32K bytes
Intel 2787	4K $\times$ 8	64K bytes
Mostek MK2716	2K $\times$ 8	32K bytes
TTL TMS 2616	2K $\times$ 8	32K bytes
TTL TMS 2637	4K $\times$ 8	64K bytes

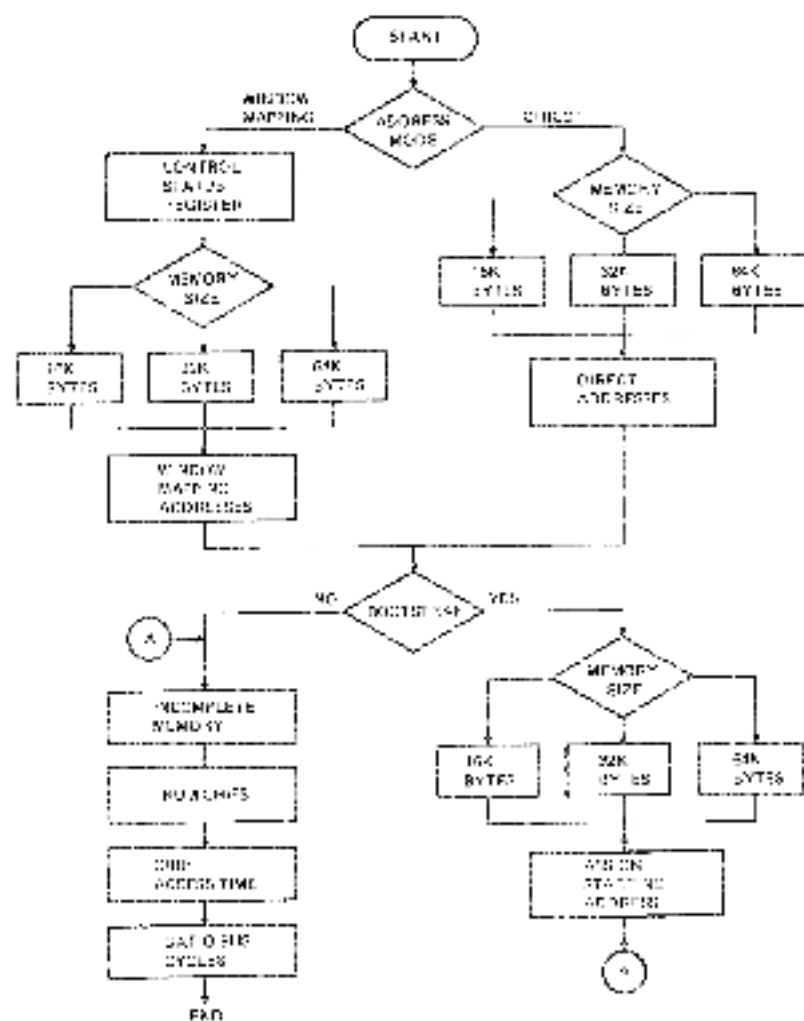
Compatible PROMs

PROM	Chip Array Size	Maximum Memory Size
Intel 3006	1K $\times$ 8	16K bytes
Signetics 829 2706	1K $\times$ 8	16K bytes
Signetics 829 181	1K $\times$ 8	16K bytes
Signetics 829 181	2K $\times$ 8	32K bytes



MRV11-C Wiring Pin Locations





Configuration Procedure

Wirewrap Pin Identification

Wirewrap Pin Designation	Function
J1	HXGX pull-up resistor
J2	HXGX optional capacitor
J3	HXGX signal
J4	LMATCH input for DDOUT control
J5	LMATCH for DDOUT control
J6	Window address enable ground
J7	Window address enable
J8	High byte chip enable bit A11
J9	CSR high byte bit 8 chip enable output
J10	High byte chip enable bit A12
J11	CSR high byte bit 9 chip enable output
J12	High byte chip enable least significant bit
J13	CSR high byte bit 10 chip enable output
J14	High byte chip enable intermediate bit
J15	CSR high byte bit 11 chip enable output
J16	High byte chip enable most significant bit
J17	CSR high byte bit 12 chip enable output
J18	Root address chip enable bit A11
J19	Root address chip enable bit A12
J20	Root address chip enable least significant bit
J21	Root address chip enable intermediate bit
J22	Root address chip enable most significant bit
J23	Root address chip enable ground reference
J24	Root address chip enable 5 V reference
J25	Direct address bit 1 chip enable output
J26	Low byte chip enable A11 bit
J27	CSR low byte bit 0 chip enable output
J28	Direct address bit 12 chip enable output
J29	Low byte chip enable A12 bit
J30	CSR low byte bit 1 chip enable output
J31	Direct address bit 13 chip enable output
J32	Low byte chip enable least significant bit
J33	CSR low byte bit 2 chip enable output
J34	Direct address bit 14 chip enable output
J35	Low byte chip enable intermediate bit
J36	CSR low byte bit 3 chip enable output
J37	Direct address bit 15 chip enable output
J38	Low byte chip enable most significant bit
J39	CSR low byte bit 4 chip enable output
J40	Reserved for future DIGITAL use
J41	Window address bit 16 compare ground
J42	Window address bit 16 compare input
J43	Window address bit 16 compare ground

Wirewrap Pin Identification (Cont)

Wirewrap Pin Designation	Function
J44	Window address bit 14 compare input
J45	Window address bit 14 compare ground
J46	Window address bit 15 compare input
J47	Window address bit 15 compare ground
J48	Window address bit 16 compare input
J49	Window address bit 16 compare ground
J50	Window address bit 17 compare input
J51	Window address bit 17 compare ground
J52	Window address bit 12 compare input
J53	Direct address 12K memory limit output
J54	Direct address 16K memory limit output
J55	Direct address memory limit input
J56	Direct address 8K memory limit output
J57	Direct address bit 17 compare ground
J58	Direct address bit 16 compare input
J59	Direct address bit 16 compare ground
J60	Direct address bit 17 compare input
J61	Direct address bit 15 compare ground
J62	Direct address bit 15 compare input
J63	Direct address bit 14 compare ground
J64	Direct address bit 14 compare input
J65	Direct address bit 13 compare ground
J66	Direct address bit 13 compare input
J67	CSR high byte bit 15 enable ground
J68	CSR high byte bit 15 enable input
J69	High byte chip enable window address function
J70	High byte chip enable direct address function
J71	High byte chip enable function select drivers
J72	Bit 7 chip select enable input
J73	Bit 7 chip enable decoder output
J74	Bit 6 chip select enable input
J75	Bit 6 chip enable decoder output
J76	Bit 5 chip select enable input
J77	Bit 5 chip enable decoder output
J78	Bit 4 chip select enable input
J79	Bit 4 chip enable decoder output
J80	Bit 3 chip select enable input
J81	Bit 3 chip enable decoder output
J82	Bit 2 chip select enable input
J83	Bit 2 chip enable decoder output
J84	Bit 1 chip select enable input
J85	Bit 1 chip enable decoder output
J86	Bit 0 chip select enable input

Wirewrap Pin Identification (Cont)

Wirewrap Pin Designation	Function
J057	Bit 0 chip enable decoder output
J060	Boot address enable ground
J063	Boot address enable
J065	DAL 4 CS# address select signal
J061	DAL 4 CS# address select ground
J062	DAL 1 CS# address select signal
J063	DAL 1 CS# address select ground
J064	DAL 2 CS# address select signal
J065	DAL 2 CS# address select ground
J066	DAL 3 CS# address select signal
J067	DAL 3 CS# address select ground
J068	Pin 18 input for chip set 5
J069	Chip wirewrap interconnection for chip set 5
J100	Pin 20 input for chip set 5 (chip enable 5)
J101	Pin 18 input for chip set 4
J102	Chip wirewrap interconnection for chip set 4
J103	Pin 20 input for chip set 4 (chip enable 4)
J104	Pin 18 input for chip set 3
J105	Chip wirewrap interconnection for chip set 3
J106	Pin 20 input for chip set 3 (chip enable 3)
J107	Pin 18 input for chip set 2
J108	Chip wirewrap interconnection for chip set 2
J109	Pin 20 input for chip set 2 (chip enable 2)
J110	Reserved for future DIGITAL use.
J111	ROM interconnection, ground reference
J112	Chip enable bit bus input
J113	Address bit A ¹⁰ , used as chip input A ¹⁰
J114	Chip interconnection, pop (to wirewrap pins)
J115	Address bit A ¹¹ , used as chip input A ¹¹
J116	Chip interconnection, pop for chip pin 21
J117	ROM interconnection, -5 Vdc voltage reference
J118	Pin 18 input for chip set 0
J119	Chip wirewrap interconnection for chip set 0
J120	Pin 20 input for chip set 0 (chip enable 0)
J121	Pin 18 input for chip set 1
J122	Chip wirewrap interconnection for chip set 1
J123	Pin 20 input for chip set 1 (chip enable 1)
J124	Pin 18 input for chip set 2
J125	Chip wirewrap interconnection for chip set 2
J126	Pin 20 input for chip set 2 (chip enable 2)
J127	Pin 18 input for chip set 3
J128	Chip wirewrap interconnection for chip set 3
J129	Pin 20 input for chip set 3 (chip enable 3)

Control and Status Register

Each MRV11-C board uses one 16-bit control and status register located in the system I/O page to determine mapping of ROM segments into windows in the window mapped mode. The default address for this CSR is 177000 (177000 in the PDP-11/23 system). The valid address range for CSRs is 177000 to 177035 (177000 to 177035 on PDP-11/23s).

The CSR contains a 5-bit read/write field for each window. The number stored in this field (0 to 31₁₀) selects the desired PKR register from the MRV11-C board to be associated with the window in question. CSR bits 0 through 4 control the mapping of the low address window, window 0. The low five bits of the upper byte (bits 8 through 12) control the mapping of window 1.

The MRV11-C optionally provides a window enable/disable capability. When bit 15 of 16 is selected, bit 15 of the CSR is used to enable or disable window responses under program control. When bit 15 is a 0, the board will respond to references to the CSR or DAT or DATC references to either of the windows. When bit 15 is a 1, only the CSR will respond. If the enable/disable option is not selected, bit 15 of the CSR will be read only and will always be 0. The enable/disable bit has no effect on direct mode addressing or the bootstrap window capability. If enable/disable option is used, bit 15 on system initializes, disabling the board.

Control and Status Register Addresses

CSR Address	Bit 4 J90 to J91	Bit 3 J96 to J97	Bit 2 J94 to J95	Bit 1 J92 to J93
177000*	R	R	R	R
177004	R	R	R	I
177008	R	R	I	R
17700C	R	R	I	I
177010	R	I	R	R
177014	R	I	R	I
177018	R	I	I	R
17701C	R	I	I	I
177020	I	R	R	R
177024	I	R	R	I
177028	I	R		R
17702C	I	R		I
177030	I	I	4	R
177034	I	I	R	I
177038	I	I		R
17703C	I	I		I

R = jumper removed I = jumper installed.

*Default address.

NOTE

Install J97 to J98 to allow the use of bit 15 of the CSR.

MRV11-C/M5048

MRV11-C Direct Addressing Starting Address

Starting Address	Bank	Bit 17 57 to 60	Bit 16 59 to 58	Bit 15 61 to 62	Bit 14 63 to 64	Bit 13 65 to 66
0	0	I	I	I	I	I
20000	1	I	I	I	I	R
40000	2	I	I	I	R	I
60000	3	I	I	I	R	R
100000	4	I	I	R	I	I
120000	5	I	I	R	I	R
140000	6	I	I	R	R	I
160000	7	I	I	R	R	R
200000	10	I	R	I	I	I
220000	11	I	R	I	I	R
240000	12	I	R	I	R	I
260000	13	I	R	I	R	R
300000	14	I	R	R	I	I
320000	15	I	R	R	I	R
340000	16	I	R	R	R	I
360000	17	I	R	R	R	R
400000	20	R	I	I	I	I
420000	21	R	I	I	I	R
440000	22	R	I	I	R	I
460000	23	R	I	I	R	R
500000	24	R	I	R	I	I
520000	25	R	I	R	I	R
540000	26	R	I	R	R	I
560000	27	R	I	R	R	R
600000	30	R	R	I	I	I
620000	31	R	R	I	I	R
640000	32	R	R	I	R	I
660000	33	R	R	I	R	R
700000	34	R	R	R	I	I
720000	35	R	R	R	I	R
740000	36	R	R	R	R	I
760000	37	R	R	R	R	R

R = jumper removed

I = jumper installed

Using Multiple Boards

Up to 16 MRV11-C boards may be configured in a single system. When multiple boards are present, each board has a unique control and status register address assigned in increasing order from 177000 (777000 in PDP-11/23 systems). Each board can have a unique 4Kb area of the physical address space set aside for its windows, but it is also possible to share one 4Kb area of the address space among all MRV11-C boards installed in the system. This is done by using the enable/disable capability discussed earlier. When enable/disable is implemented, the disable bit in the CSR will be set automatically by BINIT on the bus or by execution of the RESET instruction. Therefore, the initial state of the system will have all boards disabled. To access a particular segment of ROM in this multiboard configuration, the program must first enable the desired board and map the segment. When access to that segment is completed, the board is again disabled to allow another board to be selected some other time.

Chip Enable Jumpers

Sockets Enabled	Chip Enable Signal	Wirewrap Jumpers Pins
XE43, XE44	CE0	J80 to J87
XE37, XE38	CE1	J84 to J85
XE31, XE32	CE2	J82 to J83
XE25, XE26	CE3	J80 to J81
XE19, XE12	CE4	J78 to J79
XE15, XE16	CE5	J78 to J77
XE29, XE30	CE6	J74 to J75
XE23, XE24	CE7	J72 to J73

NOTE

J40 and J110 are unused at this time.

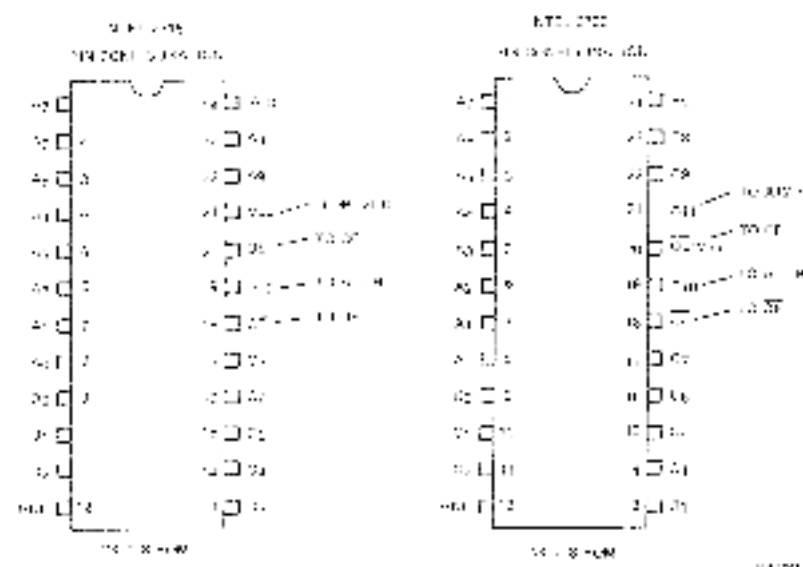
ROM Chips

The ROM is provided by the user and consists of up to 16 chips that are inserted into provided sockets. The chips will be either 1K $\times$ 5 bit, 2K $\times$ 8 bit, or 4K $\times$ 8 bit ROMs. When the MRV11-C is fully populated, the result will be either 16K, 32K, or 64K bytes of memory. These ROMs can be supplied by a variety of vendors and the basic configuration for many of the ROMs is standardized except for pins 15, 19, 20, and 21. The configuration of these pins will vary depending upon the size of the ROM and the vendor who supplies them. The user should verify the vendor's specifications in order to determine if a particular ROM can be used on the MRV11-C.

MRV11-C/M5048

The MRV11-C module is configured so that the user can select the signals that are applicable to pins 15, 18, and 21. The board provides wirewrap pins for the user to select the A11, A12, B Vdd, or ground. There are three individual loops that interconnect all chips and three wirewrap pins available for each individual chip. Wirewrap pin J1-12 interconnects pin 18 of all the chips and pin J1-16 interconnects pin 21 of all the chips; these are normally designated as the A10 or A11 inputs to the chips.

Wirewrap pin J1-14 interconnects wirewrap pins that are individually associated with each chip. Pin 10 of each chip is individually wired to a wirewrap pin and chip pin 20 is wired to the chip enable signal. Chip pin 20 is also individually wired to a wirewrap pin. The user must determine from the vendor's specifications which signals apply to which pins and must install jumper wires as needed to configure an operational module.



MRV11-C ROM Pin Configuration Sample

MRV11-D UNIVERSAL PROM MODULE

GENERAL

The MRV11-D is a flexible, high-density, dual-size module used with the IAS 11 bus. The module contains 41 jumper posts, 2 switch packs, and 16 28-pin memory chip sockets. A variety of user PROMs, such as fusible-link PROMs, ul. select erasable (UV-E) PROMs, and masked ROMs are accessible to use. The module is shipped from the factory with all jumpers installed.

The MRV11-D accepts several densities, up to and including 32K by 8; with 16 32K devices, memory capacity is 512K bytes.

Amperes Bits Loads

+5 -12	AC DC
1.5	2 -

plus ROM chip power

Standard Addresses

Recommended page mode

Window 0 is addressed between 17776000 and 17776775

Window 1 is addressed between 17776800 and 17776875

PCR address is fixed at location 1777520

Page mode PCR is used configured between 17777000 and 17777036.

Console octal debugging technique (ODT)

Terminal addresses used by console GDT addresses

16-bit addressing — 1777560 — 1777586

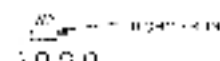
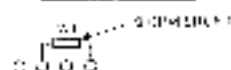
18-bit addressing — 777590 — 777595

22-bit addressing — 1777580 — 1777586

Detailed technical information is beyond the scope of this manual. For more information, refer to the Microcomputer Processor Handbook, PB 19451-23.

6. SATTETH (SOLAR) UNIT

JUMPER CONNECTION



START PULSE

24VDC OUTPUT OF THE SATTETH BACK PANEL
24VDC INPUT

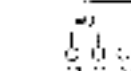
24VDC INPUT OF THE SATTETH BACK PANEL

NOTE:

INSTALLATION WITH A 24VDC SUPPLY

MRV11-D

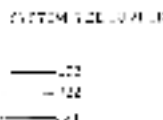
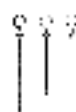
7. BATTERY UNIT (BATTERY)



BATTERY UNIT

24VDC INPUT OF THE BATTERY UNIT

24VDC OUTPUT OF THE BATTERY UNIT



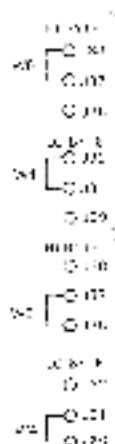
MRV11-D

8.

8. BATTERY SELECTION (BATTERY-SELECTION)

JUMPER CONNECTION

BATTERY SELECTION



THIS CONNECTION IS FOR THE BATTERY SELECTION
24VDC OUTPUT OF THE BATTERY SELECTION UNIT MUST BE
SELECTED IN THE BATTERY SELECTION UNIT

THIS CONNECTION IS FOR THE BATTERY SELECTION
24VDC OUTPUT OF THE BATTERY SELECTION UNIT MUST BE
SELECTED IN THE BATTERY SELECTION UNIT

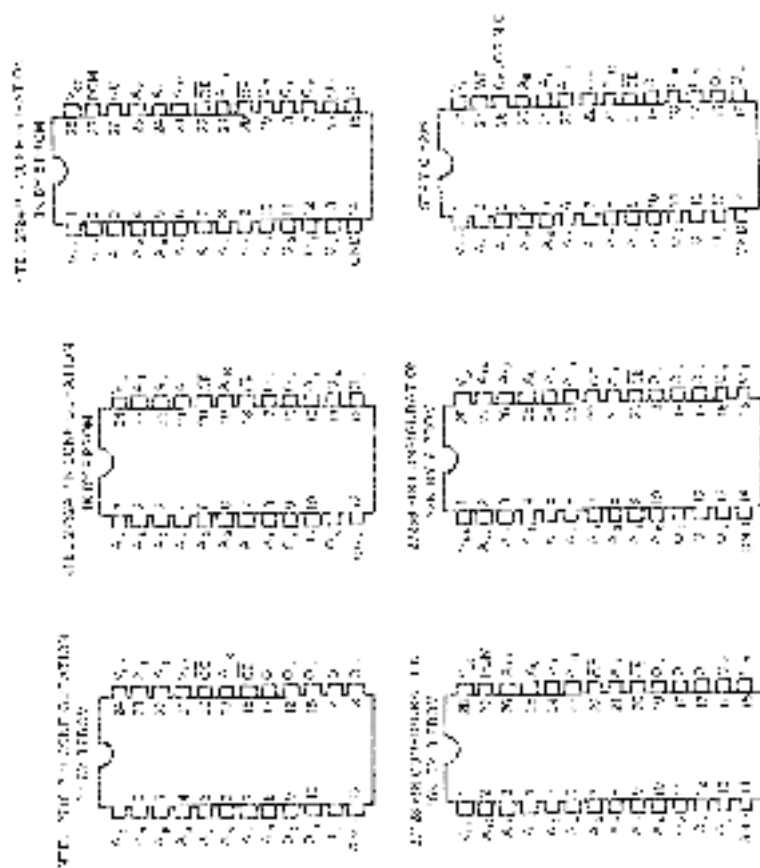
MRV11-D

Table 1
STARTING ADDRESS FOR EACH

		START	DATA FROM
	1	VCC	
	2	INT	
	3	A0	
	4	A1	
	5	A2	
	6	A3	
	7	A4	
	8	A5	
	9	A6	
	10	A7	
	11	A8	
	12	A9	
	13	A10	
	14	A11	
	15	A12	
	17	A13	
	18	A14	
	19	A15	
	20	A16	
	21	A17	
	22	A18	
	23	A19	
	24	A20	
	25	A21	
	26	A22	
	27	A23	
	28	A24	
	29	A25	

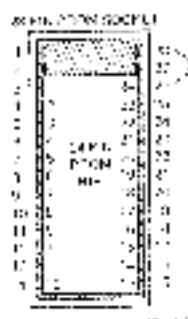
Pin 1

The basic differences on the 2784, 27128, 27256 and static RAM are in the functions of pins 26 and/or 27. The figure below shows these differences. For example, on the 16K by 8 PROM (27128), pin 26 is used as an address pin (A13). On the 32K by 8 PROM (27256), pins 26 and 27 are used as address pins (A13 and A14, respectively).



Compatible PROM Types

When installing a 24-pin PROM (2K by 8, 4K by 8) in a 26-pin socket, install it with the notch on top and bottom justified. Pin 1 of the PROM inserts into pin 3 of the socket. On 26-pin devices, pin 26 is the power pin. For 24-pin devices, pin 26 of the socket must be strapped to pin 23 of the socket to provide power to the device. The cover jumpers strap these pins together, as shown in the following figure.



Insertion of 24-Pin PROM Chips

NOTE

If you are using 24-pin devices such as the 2716 (2K by 8 PROM) on a revision C etch board, you must wire-wrap J13 (Vpp) to J40 (pin 26 of row 4). It is also necessary to jumper J40 to J41 (+5 V). However, you cannot use the jumper clip because a wire-wrap exists on J40. Therefore, you must wire-wrap, rather than jumper, J40 to J41. This procedure ensures proper read mode operation. On a revision D etch board, you can install 2K by 8 PROMs without wire-wrap.

Storage Capacity per ROM Chip Size and Number of Chips

Number of Chips Installed	Capacity Measured in Kbytes				
	2K by 8	4K by 8	8K by 8	16K by 8	32K by 8
2	4	8	16	32	64
4	8	16	32	64	128
6	12	24	48	96	192
8	16	32	64	128	256
10	20	40	80	160	320
12	24	48	96	192	384
14	28	56	112	224	448
16	32	64	128	256	512

Typical EPROMs

UV PROMs	Chip Array	Maximum Memory Array Size
	Size	
Intel 2716	2K by 8	32 Kbytes
Intel 2732	4K by 8	64 Kbytes
Intel 2764	8K by 8	128 Kbytes
Intel 27128	16K by 8	256 Kbytes
Masked ROMs		
Motorola M86700	8K by 8	128 Kbytes
Motorola 28128	16K by 8	256 Kbytes
NEC 52256	32K by 8	512 Kbytes
National 52384	8K by 8	128 Kbytes
Signetics 23128	16K by 8	256 Kbytes
Synertek 2365	8K by 8	128 Kbytes
Synertek 2365A	8K by 8	128 Kbytes
Synertek 23168	2K by 8	32 Kbytes
Synertek 2335 3	4K by 8	64 Kbytes

MSV11-B HEAD/WRITE MEMORY

Amps		Bus Loads		Cables
-5	+5	AC	DC	
0.8	0.8	1.00	1.0	none
(1.12 max.)	(0.7 max.)			

Standard Addresses

Module is shipped with all jumpers installed, selecting bank 0 (0-17776).

Vectors, DEC/X11 Exerciser Program

None

Diagnostic Programs

Refer to Appendix A

Related Documentation

Field Maintenance Print Set (MF10087)

Microcomputer Processor Handbook (ED-18451-00)

NOTES

1. Only one dynamic memory module in a system is needed to reply to the refresh bus functions initiated by the processor. The module selected should be the one with the longest access time (usually the module electrically furthest from the refreshing device).

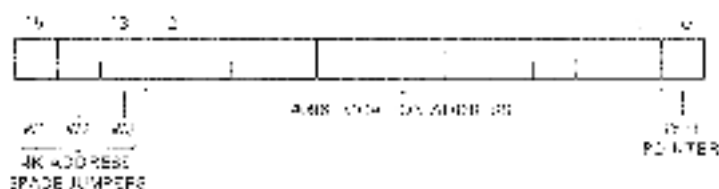
NOTES (Cont)

2. If a REV11 (M9400VA or YC) provides *refresh*, only the processor-resident memory (if present) should reply to *refresh*. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.
3. Refer to the Refresh Configuration Procedures in the "Systems Configurations" section.



M7944 Elsh Rev B

REAL BITS



Bit	Field	Value	Function
15	4K ADDRESS SPACE JUMPER	0	Normal operation
15	4K ADDRESS SPACE JUMPER	1	4K ADDRESS SPACE JUMPER
13	4K ADDRESS SPACE JUMPER	0	Normal operation
13	4K ADDRESS SPACE JUMPER	1	4K ADDRESS SPACE JUMPER
12	4K ADDRESS SPACE JUMPER	0	Normal operation
12	4K ADDRESS SPACE JUMPER	1	4K ADDRESS SPACE JUMPER
0	POLLER	0	Normal operation
0	POLLER	1	POLLER

NOTE: 1. The value 1 is not used.

M11-11

MSV11-B Address Format/Jumpers

NOTE

Because of addressing limitations, this module is not compatible with PDP-11/23 systems with more than 64K bytes of memory.

MSV11-B Address Format/Jumpers

Reply to Refresh

Function 004

Reply 0

Don't reply 1

MSV11-C MOS READ/WRITE MEMORY

Module	Model	Description
M7955-YA	MSV11-CA	4K by 16-bit read/write memory
M7955-YB	MSV11-CB	8K by 16-bit read/write memory
M7955-YC	MSV11-CC	12K by 16-bit read/write memory
M7955-YD	MSV11-CD	16K by 16-bit read/write memory

Amps		Bus Loads	Cables
+5	1.12	AC	DC
1.1	0.14	2.02	1
(2.0 max.)	(0.56 max.)		None

Standard Addresses

Module is shipped configured to start at bank 0.

Vectors

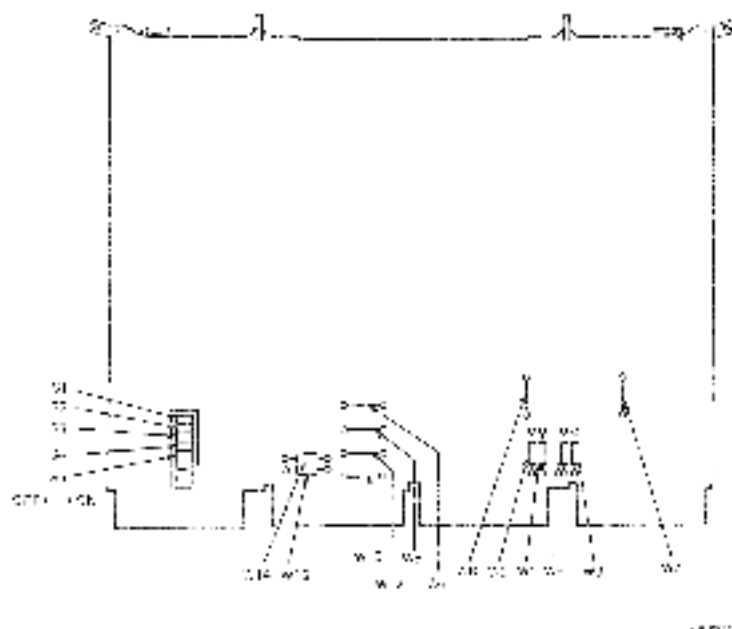
None

Diagnostic Programs

Refer to Appendix A.

Related Documentation

MSV11-C User's Manual (EX-MSV11-01)
Field Maintenance Print Set (MP00253)
Microcomputer Processor Handbook (EB-1845) (20)



M7955/MSV11-C Jumpers

NOTES

1. Only one dynamic memory module in a system is needed to reply to the refresh bus transactions initiated by the processor. The module selected should be the one with the longest access time.
2. If a REV11 (M9400-YA or M9400-YC) provides refresh, only the processor-resident memory (if present) should reply to refresh. If the processor board has no resident memory, the memory module electrically farthest from the REV11 should reply.
3. If MSV11-Cs are mixed with MSV11-Bs, the MSV11-Cs should use internal refresh. Again, the memory electrically farthest from the refreshing device should reply. Refer to the "Refresh Configuration Procedure" in the "Systems Configurations" section.

MSV11-C Jumper Configuration When Shipped

Jumper Name	Jumper State	Function Implemented												
W1 W2 W3 W5	I I I I	Battery backup power connected to system power												
		Battery backup power only. <table><tr><td>W1</td><td>W2</td><td>W3</td><td>W5</td></tr><tr><td>R</td><td>I</td><td>I</td><td>R</td></tr><tr><td>I</td><td>R</td><td>R</td><td>I</td></tr></table>	W1	W2	W3	W5	R	I	I	R	I	R	R	I
W1	W2	W3	W5											
R	I	I	R											
I	R	R	I											
		Battery backup power available but not desired for this MSV11-C module												
W6 W7	I I	Internal refresh enabled. Reply to refresh disabled												
		<table><tr><td>W6</td><td>W7</td></tr><tr><td>I</td><td>I</td></tr></table>	W6	W7	I	I								
W6	W7													
I	I													
		External refresh; no reply. <table><tr><td>W6</td><td>W7</td></tr><tr><td>R</td><td>I</td></tr></table>	W6	W7	R	I								
W6	W7													
R	I													
		External refresh; reply enabled. <table><tr><td>W6</td><td>W7</td></tr><tr><td>R</td><td>R</td></tr></table>	W6	W7	R	R								
W6	W7													
R	R													
W4 W8 W12 W10	* * * I	Factory configured to enable the memory banks appropriate to the memory model. These are normally not changed except for												
		1. Maintenance - Refer to chapter 4 of <i>MSV11-C User's Manual</i> , EX-MSV11-OP.												
		2. Configuring for 20K system: Remove W10 to disable upper 4K. See configuration rules in the 'System's Configurations' section												
W14	I	Bus grant continuity provided												
W15	I													

*Memory bank enable jumpers when supplied.

MSV11-C/M7955

Module Number	Option Designation	Memory Size	W6	W8	W12	W16
M7955-YD	MSV11-CD	16K	1	1	1	1
M7955-YG	MSV11-CC	12K	1	1	1	0
M7955-YH	MSV11-CB	8K	1	1	0	0
M7955-YA	MSV11-CA	4K	1	0	0	0

MSV11-CD Addressing Summary

Starting Address	MSV11-CD Banks	Address Range	Switch Setting				
			S1	S2	S3	S4	S5
0	0-3	0-77777	1	1	1	1	1
20000	1-4	20000-117777	0	1	1	1	1
40000	2-5	40000-137777	1	0	1	1	1
60000	3-6	60000-157777	0	0	1	1	1
100000	4-7	100000-177777	0	1	0	1	1
120000	5-10	120000-217777	0	1	0	1	1
140000	6-11	140000-237777	1	0	0	1	1
160000	7-12	160000-257777	0	0	0	1	1
200000	10-13	200000-277777	1	1	1	0	1
220000	11-14	220000-317777	0	1	1	0	1
240000	12-15	240000-337777	1	0	1	0	1
260000	13-16	260000-357777	0	0	1	0	1
300000	14-17	300000-377777	1	1	0	0	1
320000	16-20	320000-417777	0	1	0	0	1
340000	16-21	340000-437777	1	0	0	0	1
360000	17-22	360000-457777	0	0	1	0	1
400000	20-23	400000-477777	1	1	1	1	0
420000	21-24	420000-517777	0	1	1	1	0
440000	22-25	440000-537777	1	0	1	1	0
460000	23-26	460000-557777	0	0	1	1	0
500000	24-27	500000-577777	1	1	0	1	0
520000	25-30	520000-617777	0	1	0	1	0
540000	26-31	540000-637777	1	0	0	1	0
560000	27-32	560000-657777	0	0	0	1	0
600000	30-33	600000-677777	1	1	1	0	0
620000	31-34	620000-717777	0	1	1	0	0
640000	32-35	640000-737777	1	0	1	0	0
660000	33-36	660000-757777	0	0	1	0	0
700000	34-37	700000-777777	1	1	0	0	0
720000	x	x-x	0	1	0	0	0
740000	x	x-x	1	0	0	0	0
760000	x	x-x	0	0	0	0	0

NOTES

1. Switch setting:
1 -- ON
0 -- OFF
2. Each memory bank -- one 4K address space.
3. Switches 6, 7, and 8 are not used.

NOTE

When used in PDP-11/23 systems, the MSV11-C memory cannot be configured in the 56K-84K byte (28K-32K word) range or in the 248K-256K byte (124K-128K word) range.

MSV11-D,E MOS READ/WRITE MEMORY

Model	Memory Capacity	Module	Parity Bits
MSV11-DA	4K by 16 bits	M8044-DA	No
MSV11-DB	8K by 16 bits	M8044-DB	No
MSV11-DC	16K by 16 bits	M8044-CA	No
MSV11-DD	32K by 16 bits	M8044-DA	No
MSV11-DE	32K by 16 bits	M8045-DA	Yes

Amps		Bus Loads	Cables
1.5	+12	AC	DC
2.0	0.41	2	None

Standard Addresses

Module is shipped configured to start at bank 0.

Vectors

None

Diagnostic Programs

Refer to Appendix A.

NOTE

DEC diagnostic will not check parity.

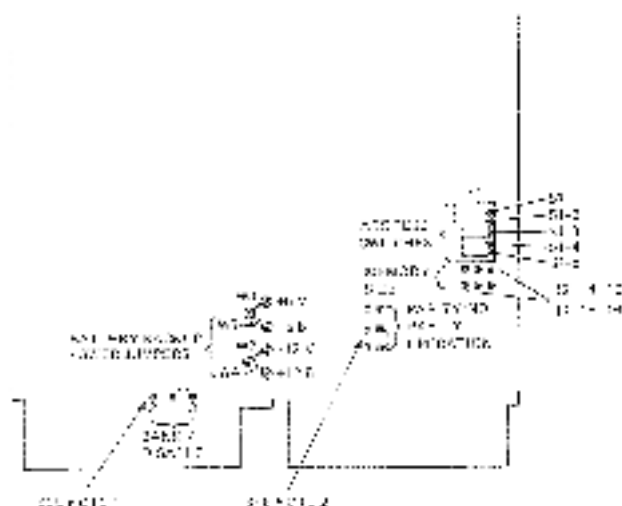
Related Documentation

MSV11-D, E User's Manual (EK-MSV1D-UP)
Field Maintenance Print Set (MP00269)
Microcomputer Processor Handbook (EE-1B451-20)

MSV11-D.E/M8C4.5

Address Selection

The MSV11-D or MSV11-E address can start at any 4K bank boundary. The address configured is the starting address for the contiguous portion of memory (1K, 8K, 16K, or 32K) contained on the module.



LETTERS

- [illegible]

444

MSX-100 MSX-100 Switch and Jumpers MB044-40

Set the switches to the desired starting address as listed in the table. Note that the module is designed to accommodate a 128K system addressing capability. However, the present addressing capability of the LSI-11 system including all PDP-11/08, PDP-11/05 and PDP-11/03 systems is 32K. PDP-11/28 systems, however, can address within the full 256K word range. By PDP-11 convention, the upper 4K address space is normally reserved for peripheral device and register addresses. Thus, with the present LSI-11 maximum addressing capability of 32K, bank 7 (addresses 160000-177777) normally should not be used for system memory.

Factory-configured modules will not respond to bank 7 addresses. In special applications (i.e., MINC), enable the use of the lower 2K portion of bank 7 for system memory (i.e., MINC). Enable the lower 2K portion of bank 7 by removing the jumper from pinwrap pins 1 and 3 and connecting a new jumper from 1 to 2.

NOTE

If 50K option is enabled, some diagnostics may not run.

Battery Backup Power

MSV11-D and MSV11-E modules are factory configured with power jumpers installed for normal system power only. If the system uses a battery backed power source, remove jumpers W2 and W5. Install new jumpers W4 and W6. (Two jumpers are removed and two new jumpers are installed.)

Parity

One jumper is factory installed for nonparity (MSV11-D) or parity (MSV11-E) operation, depending on the model. Do not reconfigure this jumper. Standard jumper configurations are listed below.

- All MSV11-D models: jumper installed from pin 7 to pin 5.
- All MSV11-E models: jumper installed from pin 6 to pin 5.

NOTE

This memory parity feature is not supported by DEC diagnostics or CPUs.

Memory Size

Two jumpers are factory installed to configure addressing logic for memory size (number and type of memory-integrated circuits). Do not reconfigure these jumpers. Standard jumper configurations are listed below.

Models	Jumpers (Two installed) Memory Select Pins	Memory Range Pins
MSV11-DA	From 12 to 14	From 17 to 15
MSV11-DB	From 12 to 14	From 17 to 15
MSV11-DC	From 16 to 14	From 18 to 15
MSV11-DD, ED	From 10 to 14	From 16 to 15

MSV11-D, MSV11-E Addressing Summary

Starting Address	Switch Settings					MSV11-DA, MSV11-EA	4K Memory Banks Selected			
	S1-1	S1-2	S1-3	S1-4	S1-5		MSV11-DB, MSV11-FB	MSV11-DC, MSV11-EC	MSV11-DD, MSV11-ED	
0	N	N	N	N	N	0	0-1	0-3	0-7	
20000	N	N	N	N	N	1	1-2	1-4	1-10	
40000	N	N	N	N	N	2	2-3	2-5	2-11	
60000	N	N	N	N	N	3	3-4	3-6	3-12	
80000	N	N	N	N	N	4	4-5	4-7	4-13	
120000	N	N	N	N	N	5	5-6	5-10	5-14	
140000	N	N	N	N	N	6	6-7	6-11	6-15	
160000	N	N	N	N	N	7	7-10	7-12	7-18	
200000	N	N	N	N	N	10	10-11	10-13	10-17	
220000	N	N	N	N	N	11	11-12	11-14	11-20	
240000	N	N	N	N	N	12	12-13	12-15	12-21	
260000	N	N	N	N	N	13	13-14	13-16	13-22	
300000	N	N	N	N	N	14	14-15	14-17	14-23	
320000	N	N	N	N	N	15	15-16	15-19	15-24	
340000	N	N	N	N	N	16	16-17	16-21	16-25	
360000	N	N	N	N	N	17	17-20	17-22	17-26	
400000	F	N	N	N	N	20	20-21	20-23	20-27	
420000	F	N	N	N	N	21	21-22	21-24	21-30	
440000	F	N	N	N	N	22	22-23	22-25	22-31	
460000	F	N	N	N	N	23	23-24	23-26	23-32	

MSV11-D, MSV11-E Addressing Summary (Cont)

Starting Address	Switch Settings							4K Memory Bank(s) Selected		
	S1-1	S1-2	S1-3	S1-4	S1-5	MSV11-CA, MSV11-FA		MSV11-DB, MSV11-EB	MSV11-DC, MSV11-EC	MSV11-DD, MSV11-ED
620000	F	N	F	N	N	24		24-25	24-27	24-33
520000	F	N	F	N	F	25		25-26	25-32	25-34
540000	F	N	F	F	N	26		26-27	26-31	26-35
560000	F	N	F	F	F	27		27-30	27-32	27-35
600000	F	F	N	N	N	30		30-31	30-33	30-37
620000	F	F	N	N	F	31		31-32	31-34	X
640000	F	F	N	F	N	32		32-33	32-35	X
660000	F	F	N	F	F	33		33-34	33-36	X
700000	F	F	F	N	N	34		34-35	34-37	X
720000	F	F	F	N	F	35		35-36	X	X
740000	F	F	F	F	N	36		36-37	X	X
760000	F	F	F	F	F	37		X	X	X

NOTES

- Switch settings:
N = ON
F = OFF
- In unmapped systems, bank 7 cannot be selected as factory configured; however, the user can enable the lower 2K portion of bank 7.
- X = Do not use.

MSV11-L MOS READ/WRITE MEMORY

GENERAL

MSV11-L Modules

Model	Memory Capacity	MOS Chips	Module	Number of Chips
MSV11-LF	128Kbytes	64K $\times$ 1	MB059-FA	10
MSV11-LK	256Kbytes	64K $\times$ 1	MB059-KA	36

MSV11-L POWER

Power Requirements

+5 V $\pm$ 5% Current (Amps)					-5 V $\pm$ 5% Power (Watts)			
Standby		Active		Standby		Active		
Type	Meas	Max	Meas	Max	Meas (-5 V)	Max (5.25 V)	Meas (-5 V)	Max (5.25 V)
64K (LF)	1.40	2.00	1.40	2.05	7.0	10.75	7.25	11.70
128K (LK)	1.40	2.05	1.80	2.05	7.5	10.75	8.0	10.75

Power Requirements (Cont)

+5 V BBU 5% Current (Amps)					+5 V BBU 5% Power (Watts)				
	Standby		Active		Standby		Active		
Type	Meas	Max	Meas	Max	Meas (-5 V)	Max (5.25 V)	Meas (-5 V)	Max (5.25 V)	
64K (LF)	0.9	1.26	1.35	1.55	4.5	6.62	11.75	8.11	
128K (LK)	1.0	1.33	1.40	1.67	5.0	7.26	7.0	10.34	
+5 V Total 5% Current (Amps)					+5 V Total 5% Power (Watts)				
	Standby		Active		Standby		Active		
Type	Meas	Max	Meas	Max	Meas (-5 V)	Max (5.25 V)	Meas (-5 V)	Max (5.25 V)	
64K (LF)	2.3	3.31	2.8	3.90	11.5	17.35	14.0	20.18	
128K (LK)	2.5	3.43	3.0	4.02	12.5	18.07	15.0	21.11	

Meas = measured

Max = maximum

NOTE

Use the total table above for power requirements for factory configured option modules.

Diagnostic Programs

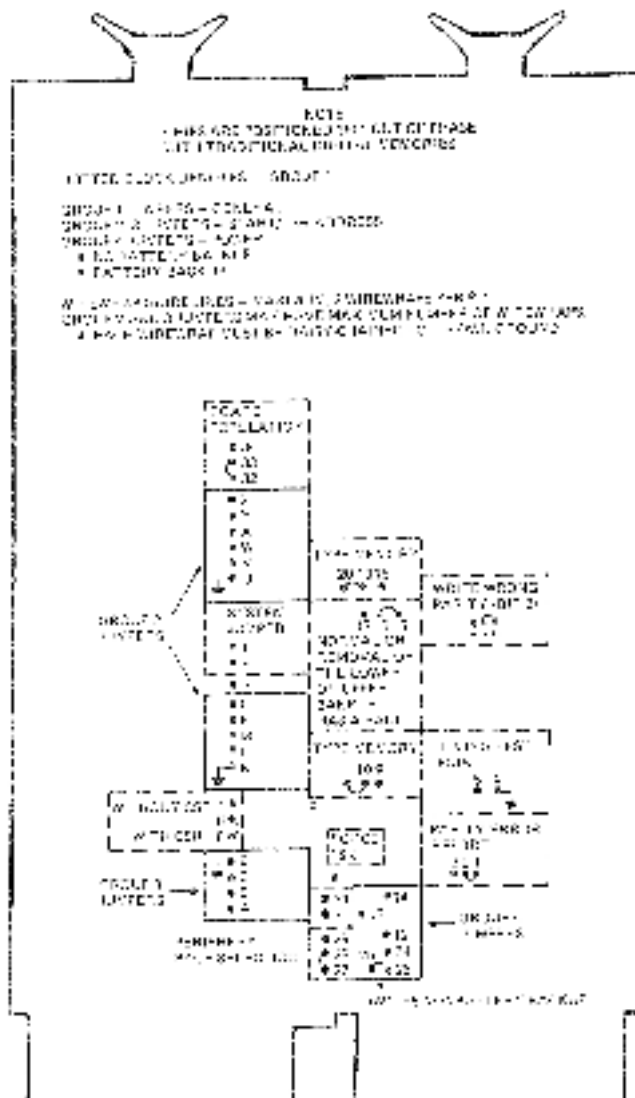
Refer to Appendix A.

Related Documentation

MSV11-L User's Guide (EK-MSV0L-UG)

MSV11-L Memory Module Configuration Guide (EK-MSV11-CG)

Field Maintenance Panel Set (MP-01239)



MSY114 Memory Module 1 2/2004

CONFIGURATION

There are four groups of jumpers that allow the memory operation for a specific system application. The jumper groups are named as follows:

- Group 1 - General jumpers
- Group 2 - Starting address jumpers
- Group 3 - CS# address jumpers
- Group 4 - Power jumpers

General Jumpers

The general configuration jumpers are described in the following table, and the normal or factory configuration is designated by being installed or removed.

General Jumpers (Group 1)

Function	Jumper Configuration	Normal Condition
Type Memory		
Nonparity	8 to 10	OUT
With parity	11 to 10	IN
Parity non-CS#	18 to 19	OUT
Parity with CS#	20 to 19	IN
Parity Error Report		
Reported BDAL 16 non-CS#	3 to 2	OUT
Reported BDAL 16 and BDAL 17 with CS#	1 to 2	IN
Write Wrong Parity		
Diagnostic bit for tester use.		
Disable	5 to 7	OUT
Enable	6 to 7	IN

General Jumpers (Group 1) (Cont)

Function	Jumper Configuration	Normal Condition
CSP Selection		
Non-CSP With CSP	J to H F to H	OUT IN
Peripheral Page Selection		
2K peripheral page 4K peripheral page	29 to 28 27 to 26	OUT IN
Full or Half Memory Selection		
Half memory selection Full memory selection	32 to 33 34 to 33	OUT IN
Removal of Lower or Upper Bank (with a Fault)		
Lower bank has failed Normal operation or upper bank has failed	17 to 16 5 to 16	OUT IN
Extended or Normal Memory Selection		
Small system normal operation (128K)	R to T	OUT
Large system extended operation (2 megawords)	H to I	IN

Starting Address Jumpers

Each MSV11-L memory module installed in a system is jumpered for its own starting address. The starting addresses are always on 4K boundaries. The module's starting address can be found by answering the question "how much memory does the system already have?" The value obtained is the module starting address in decimal k words. Module starting addresses and jumpers consist of two groups.

1. First address of the range (FAR) — Seals the first address of the 125K range that the starting address falls in.
2. Partial starting address (PSA) — Seals which 4K boundary within a specific multiple of 125K words the starting address falls in.

The module starting address (MSA) is determined by how much memory the system has in decimal k words. First address of the range plus partial starting address equals module starting address.

$$\begin{array}{ccc}
 & \text{Known} & \\
 & \downarrow & \\
 \text{PSA} = \text{MSA} - \text{FAR} & & \\
 \downarrow & & \downarrow \\
 \text{Partial Starting Address} & & \text{First Address of Range}
 \end{array}$$

First Address of Range (FAR)

Decimal (K)	Total	Jumpers in (X) to Ground (K)			
		P	R	M	L
000-124	00000000-00760000				
125-252	01000000-01760000				X
253-380	02000000-02760000			X	
381-508	03000000-03760000			X	X
509-636	04000000-04760000		X		
637-764	05000000-05760000		X		X
765-892	06000000-06760000		X	X	
893-1020	07000000-07760000		X	X	X
1021-1148	08000000-08760000	X			
1149-1276	09000000-09760000	X			X
1277-1404	10000000-10760000	X		X	
1405-1532	11000000-11760000	X		X	X
1533-1660	12000000-12760000	X	X		
1661-1788	13000000-13760000	X	X		X
1789-1916	14000000-14760000	X	X	X	
1917-2044	15000000-15760000	X	X	X	X

Partial Starting Address (PSA)

Decimal (K)	Octal	Jumpers in (X) to Ground (Z)					
		DAL Pins	17 Z	16 Y	15 X	14 W	13 V
0	00000000						X
4	00000000					X	
8	00040000					X	
12	00080000					X	X
16	00100000				X		
20	00120000				X		X
24	00140000				X	X	
28	00160000				X	X	X
32	00200000			X			
36	00220000			X			X
40	00240000			X		X	
44	00260000			X		X	X
48	00300000			X	X		
52	00320000			X	X		X
56	00340000			X	X	X	
60	00360000			X	X	X	X
64	00400000		X				
68	00420000		X				X
72	00440000		X			X	
76	00460000		X			X	X
80	00500000		X		X		
84	00520000		X		X		X
88	00540000		X		X	X	
92	00560000		X		X	X	X
96	00600000		X	X			
100	00620000		X	X			X
104	00640000		X	X		X	
108	00660000		X	X		X	X
112	00700000		X	X	X		
116	00720000		X	X	X		X
120	00740000		X	X	X	X	
124	00760000		X	X	X	X	X

Module Starting Address (Example - 32K Words)

Names	First Address of Range (FAR)				Partial Starting Address (PSA)				
Decimal k words	1Meg	512K	256K	128K	64K	32K	16K	8K	4K
binary address									
RF-AI values	21	20	19	18	17	16	15	14	13
RF-AI bits	0	0	1	0	1	1	0	0	0
Jumper pin names	P	N	M	L	Z	Y	X	W	V
Jumper pins	M to K				Z to Y, Y to U				

CSR Address Selection

There are three addresses reserved for the CSR. Every MSV11-L memory module has one CSR. By convention the CSR addresses are assigned as follows. The memory module with the lowest starting address should be jumpered for the lowest CSR address. The remaining memory modules will be jumpered in sequence.

CSR Address Jumpers (Group 2)

22-Bit CSR Address	18-Bit CSR Address	C	B	A
17772100	772100			
17772102	772102			X
17772104	772104		X	
17772106	772106		X	X
17772110	772110	X		
17772112	772112	X		X
17772114	772114	X	X	
17772116	772116	X	X	X

Note: To obtain any 1 of 8 CSR addresses, wirewrap daisy-chain fashion from pin C, which is grounded, to each successive pin labeled X for that address.

MSV11-L/MB059

Power Jumpers

Power jumpers allow the MSV11-L memory module to use battery backup or nonbattery backup power.

Power Jumpers (Group 4)

Voltage Connection	Jumper Configuration
5 V Nonbattery backup	26 to 26 (W1)
5 V Battery backup	24 to 26 (W2) 14 to 12 (W3)* or 12 to 12 (W1)*

*Availability for the +5 V battery backup.

CSR Bit Assignment

The CSR allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared by the assertion of BUS HLL (L). The CSR bit assignments are as follows:



CSR Bit Assignments

CSR Bit Descriptions

Bit	Name	Description
15	Parity error	If a parity error occurs on a DATI or DATO(5) cycle, this bit will be set to a 1. This is a read/write bit and is reset to 0 via a power up or BUS INIT. Bit 15 will remain set unless overwritten or initialized.
14	Extended CSR Read Enable	This bit is not used on 128K word machines. It will be read as a 0. Bit 14 can be set to a 1 in a 2048K word machine only. In a 2048K word machine bit 14 is a read 1 write bit and is reset to 0 by power up or BUS INIT. When set, bit 14 allows retrieval of failed address bits of A18 through A21 stored in CSR bits 08 through 05 respectively.
13, 12	Not used	
11-08	Error address	If a parity error occurs on a DATI or DATO(5) cycle then A17-A12 are stored in CSR bits 09-11 and bits A18-A21 are latched. The 128K word machines (18-bit address) require only one read of the CSR to obtain the failed address bits. CSR bit 14 = 0 allows the logic to pass A11-A17 to the LSI-11 bus. A 2048K word machine (20-bit address) requires two reads. The first read CSR bit 14 = 0 sends contents of CSR bits 09-11. Then the program must set CSR bit 14 = 1. This enables A18-A21 to be read from CSR bits 05-08. The parity error addresses locate the parity error to a 16K segment of memory. These are read/write bits and are not reset to zero via power up or BUS INIT. If a second parity error is encountered, the new failed address will be stored in the CSR.
04, 03	Not used	

CSR Bit Descriptions (Cont)

Bit	Name	Description
C2	Write wrong parity	If this bit is set to 1 and a DAT0 or DAT0B cycle to memory occurs, wrong parity data will be written into the parity MDS RAMs. This bit may be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable: 1. With bit C2 set, write entire memory with any pattern. 2. Read first location in memory. If bit C2 of the CSR is set, then a parity error indication will be detected on the LSI 11 bus and the failed address (location 0) will be stored in the CSR. 3. Read the CSR and obtain the failed address. CSR bit 14 = 1 implies A11-A17 on CSR bits 05-11. CSR bit 14 = 0 implies A18-A21 on CSR bits 05-08. Bit 09 is a read/write bit reset to zero on power up or BUS INIT.
C1	Not used	
C0	Parity error enable	If a parity error occurs on a DAT0 or DAT0B cycle to memory and bit C0 is set = 1, then BDAL 10 (L) or BDAL 16 (H) and DDAL 17 (L), jumper selectable, will be asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power up or BUS INIT.

MSV11-P MOS MEMORY

GENERAL

MSV11-P Modules

Model	Memory Capacity	MOS Chips	Module	Number of Rows	Number of Chips
MSV11-H-L	512K bytes	64K $\times$ 1	M8087-LA	8	72
MSV11-PK	256K bytes	64K $\times$ 1	M8087-KA	4	36
MSV11-PF	128K bytes	64K $\times$ 1	M8087-FA	8	72

MSV11-PF (Multivoltage MOS RAMs) M8087-Fx Power Requirements

Voltage	Standby Current(A)		Active Current(A)	
	Measure Typical	Maximum	Measure Typical	Maximum
+5 V Noncritical	1.40	2.21	1.40	2.21
+5 V BBU	1.15	1.55	1.20	1.55
Total +5 V	2.55	3.76	2.65	3.76
+12 V	0.10	0.12	0.35	0.53
Voltage	Standby Power(W)		Active Power(W)	
	Measure Typical	Maximum	Measure Typical	Maximum
+5 V Noncritical	7.00	11.08	7.25	11.60
+5 V BBU	5.75	8.14	8.00	8.14
Total +5 V	12.75	19.74	15.25	19.74
+12 V	1.20	1.51	4.20	6.36
Total Power	13.95	21.25	19.45	26.42

MSV11-PK (Single Voltage, Half Populated) M3067-KA Power

Voltage	Standby Current(A) Measure		Active Current(A) Measure	
	Typical	Maximum	Typical	Maximum
+5 V Noncritical	1.65	2.10	1.70	2.10
+5 V BBU	1.80	1.80	1.75	2.10
Total +5	3.00	3.80	3.45	4.20
Voltage	Standby Power(W) Measure		Active Power(W) Measure	
	Typical	Maximum	Typical	Maximum
(5.0)	(5.25)	(5.25)	(5.0)	(5.25)
+5 V Noncritical	8.25	11.00	8.50	11.0
+5 V BBU	8.75	9.45	8.75	11.0
Total Power	15.0	20.45	17.25	22.0

MSV11-PL (Single Voltage, Fully Populated) M3067-LA Power

Voltage	Standby Current(A) Measure		Active Current(A) Measure	
	Typical	Maximum	Typical	Maximum
+5 V Noncritical	1.65	2.10	1.70	2.10
+5 V BBU	1.45	1.90	1.85	2.20
Total +5 V	3.10	4.0	3.60	4.30
Voltage	Standby Power(W) Measure		Standby Power(W) Measure	
	Typical	Maximum	Typical	Maximum
(5.0)	(5.25)	(5.25)	(5.0)	(5.25)
+5 V Noncritical	8.25	11.0	8.50	11.00
+5 V BBU	7.25	10.0	9.25	11.55
Total +5 V	15.5	21.0	17.75	22.55

NOTE

Use the +5 V table (BOLD) for current requirements for factory configured modules.

Diagnostic Programs

Refer to Appendix A.

Related Documentation

MSV11-P User's Guide (UK-MSV0P-UG)

Field Maintenance Print Set (MP-C1239)

CONFIGURATION

The jumpers on the MSV11-P memory module are divided into the following five groups:

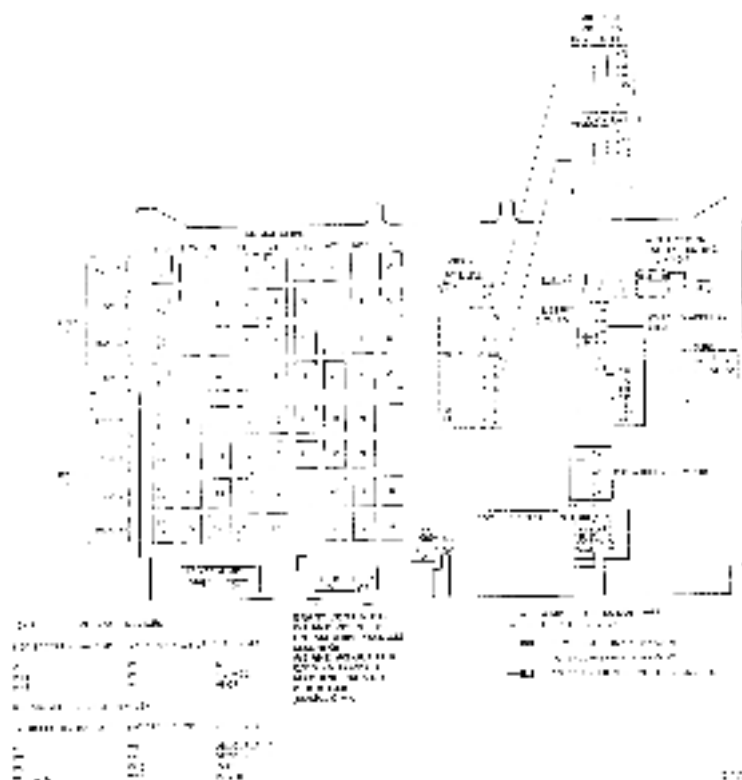
1. Starting address jumpers
2. CS# address jumpers
3. Power jumpers
4. Bus grant continuity jumpers
5. General jumpers

The location of the five jumper groups, four of which are enclosed in solid boxes and labeled, is shown in the following figure. The remaining jumpers are classified as general jumpers. The general jumpers are enclosed in dotted boxes.

Configuring the Starting Address

The starting addresses for each module in the system is always selected on 4K boundaries. The memory area of the system is determined first by its byte content. This determines the module starting address (MSA). The first address of range (FAR) selects the 256K word range the starting address will fall into. This selection is described under FAR selection. The partial starting address (PSA) selects the 8K boundary within the 256K range selected. The selection is described under the PSA selection. The following equation is used for selecting the FAR and PSA.

$$\begin{array}{ccc}
 & \text{Known} & \\
 & \downarrow & \\
 \text{PSA} - \text{MSA} & & \text{FAR} \\
 \downarrow & & \uparrow \\
 \text{Partial Starting Address} & & \text{First Address of Range}
 \end{array}$$



MSV11-P Memory Module Layout

FAR Starting Address Configurations (Part 6)

First Address Ranges (FAR)		Jumpers to Ground (Pin Y)		
Decimal K words	Octal K words	Pin X (A21)	Pin W (A20)	Pin V (A19)
000-248	00000000-01740000	OUT	OUT	OUT
256-504	02000000-03740000	OUT	OUT	IN
512-760	04000000-05740000	OUT	IN	OUT
768-1016	06000000-07740000	OUT	IN	IN
1024-1272	10000000-11740000	IN	OUT	OUT
1280-1528	12000000-13740000	IN	OUT	IN
1536-1784	14000000-15740000	IN	IN	OUT
1792-2040	16000000-17740000	IN	IN	IN

PSA Starting Address Configurations (Part 2)

Partial Starting Address (PSA)		Jumpers to Ground (Pin R)				
Decimal K	Octal	Pin P (A16)	Pin N (A17)	Pin M (A18)	Pin L (A19)	Pin T (A14)
0	00000000	OUT	OUT	OUT	OUT	OUT
8	00040000	OUT	OUT	OUT	OUT	IN
16	00100000	OUT	OUT	OUT	IN	OUT
24	00140000	OUT	OUT	OUT	IN	IN
32	00200000	OUT	OUT	IN	OUT	OUT
40	00240000	OUT	OUT	IN	OUT	IN
48	00300000	OUT	OUT	IN	IN	OUT
56	00340000	OUT	OUT	IN	IN	IN
64	00400000	OUT	IN	OUT	OUT	OUT
72	00440000	OUT	IN	OUT	OUT	IN
80	00500000	OUT	IN	OUT	IN	OUT
88	00540000	OUT	IN	OUT	IN	IN
96	00600000	OUT	IN	IN	OUT	OUT
104	00640000	OUT	IN	IN	OUT	IN
112	00700000	OUT	IN	IN	IN	OUT
120	00740000	OUT	IN	IN	IN	IN
128	01000000	IN	OUT	OUT	OUT	OUT
136	01040000	IN	OUT	OUT	OUT	IN
144	01100000	IN	OUT	OUT	IN	OUT
152	01140000	IN	OUT	OUT	IN	IN
160	01200000	IN	OUT	IN	OUT	OUT
168	01240000	IN	OUT	IN	OUT	IN
176	01300000	IN	OUT	IN	IN	OUT
184	01340000	IN	OUT	IN	IN	IN
192	01400000	IN	IN	OUT	OUT	OUT
200	01440000	IN	IN	OUT	OUT	IN
208	01500000	IN	IN	OUT	IN	OUT
216	01540000	IN	IN	OUT	IN	IN
224	01600000	IN	IN	IN	OUT	OUT
232	01640000	IN	IN	IN	OUT	IN
240	01700000	IN	IN	IN	IN	OUT
248	01740000	IN	IN	IN	IN	IN

Control Status Register (CSR) Jumpers

Each MSV11-P memory module has a control status register. The bus master can read or write the CSR via the LSI-11 bus. The CSR is a 18 bit register whose address falls in the top 4K of system address space.

Each memory module has four CSR jumper pins (A, B, C, and D) that can be easily chained to pin E (the ground pin). The jumpers allow logic to detect a specific CSR address that has been assigned to a CSR memory module. The user determines which type of bus the module is being installed and connects the jumpers for each address as described in the following table.

CSR Address Selection

Module Number	Extended LSI-11 Bus Address	LSI-11 Bus Address	Jumper to Ground (Pin E)			
			D	C	B	A
1	17772100	772100	OUT	OUT	OUT	OUT
2	17772102	772102	OUT	OUT	OUT	IN
3	17772104	772104	OUT	OUT	IN	OUT
4	17772106	772106	OUT	OUT	IN	IN
5	17772110	772110	OUT	IN	OUT	OUT
6	17772112	772112	OUT	IN	OUT	IN
7	17772114	772114	OUT	IN	IN	OUT
8	17772116	772116	OUT	IN	IN	IN
9	17772120	772120	IN	OUT	OUT	OUT
10	17772122	772122	IN	OUT	OUT	IN
11	17772124	772124	IN	OUT	IN	OUT
12	17772126	772126	IN	OUT	IN	IN
13	17772130	772130	IN	IN	OUT	OUT
14	17772132	772132	IN	IN	OUT	IN
15	17772134	772134	IN	IN	IN	OUT
16	17772136	772136	IN	IN	IN	IN

Power Jumpers

The power jumpers are divided into the following two groups.

- 16K multiple voltage devices (M8067-PA) with or without battery backup
- 64K single voltage devices (M8067-LA and M8067-KA) with or without battery backup

Power Jumpers

16K Multiple Voltage Devices

Nonbattery Backup	Battery Backup	Voltages
W4 W11 W15	W5 W10 W12	5 1 + 2 VDD + 5 CR

64K Single Voltage Devices

Nonbattery Backup	Battery Backup	Voltages
W1 W5 W9 W13/W16	W4 W6 W12 W14	Decouple +5 Decouple -5 -5 CH -5 VDD

Bus Grant Continuity Jumpers

To install W1 and W2 in your system, identify the backplane bus structure as AB/AB or AB/CD. The jumpers are installed for an AB type backplane and removed for a CD type backplane as described below.

Bus Grant Continuity

Backplane	Bus Type	W1	W2
H8270 (4 slot backplane)	AB/AB	IN	IN
H8275 (9 slot backplane)	AB/AB	IN	IN
H8276 (4 slot backplane)	AB/CD	OUT	OUT
H8276 (9 slot backplane)	AB/CD	OUT	OUT

General Jumpers

The general jumper group and their functions that have not yet been covered are described below.

General Jumpers

Pin Numbers	Function
6 to 7	In - write wrong parity
5 to 7	In - disable wrong parity
2 to Y	2 to Y out - 22-bit machine 2 to Y in - 16-bit machine
43 to 44	In - single voltage MOS RAM access time (150 ns device)
45 to 44	In - multiple voltage MOS RAM access time (200 ns device)
22 to 23	Not used
21 to 23	Not used
F to H	F to H in - connected to force the starting address to 16K F to H out - disables force function
3 to H	3 to B in - connected on 16K and 64K MOS chip
12 to 15	Connected on 16K and 64K MOS chip
4 to 10	Connected only on 64K MOS chip
14 to 16	Connected only on 64K MOS chip

CONTROL STATUS REGISTER (CSR) BIT ASSIGNMENT

The control status register (CSR) in the MSV11-P allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the LSI-11 bus. Some CSR bits are cleared by assertion of BUS INIT L. The CSR bit assignments are as follows.



(CSR) Bit Assignment

CSR Bit Descriptions

Bit	Name	Description
15	Parity error	This bit set indicates that a parity error has occurred. The bit then turns on a red LED on the module. This provides visual indication of a parity error. Bit 15 is a read/write bit. It is reset to zero via power-up or BUS INIT and remains set unless rewritten or initialized.
14	Extended CSR read enable	The use of this bit is explained in the error address description. Bit 14 = 0, always for 128K word machine Bit 14 = 0, first read on 2048K word machine Bit 14 = 1, second read on 2048K word machine
13, 12	Not used	

CSR Bit Descriptions (Cont)

Bit	Name	Description
11-05	Error address	If a parity error occurs on a DATA or DATO(B) cycle, then A11-A17 are stored in CSR bits 05-11 and bits A18-A21 are latched. The 128K word machines (18-bit address) require only one read of the CSR register to obtain the failed address bits. CSR bit 11 = 0 allows the logic to pass A11-A17 to the LSI 11 bus. A 2048K word machine (22-bit address) requires two reads. The first read CSR bit 14 = 0 sends contents of CSR bits 05-11. Then the program must set CSR bit 11 = 1. This enables A18-A21 to be read from CSR bits 05-09. The parity error addresses locate the parity error to a 1K segment of memory. These are read/write bits and are not reset to zero via power-up or BUS INIT. If a second parity error is encountered, the new failed address is stored in the CSR.
04, 03	Not used	
02	Write wrong parity	If this bit is set equal to 1 and a DATA or DATO(B) cycle to memory occurs, wrong parity data is written into the parity MOS RAMs. This bit can be used to check the parity error logic as well as failed address information in the CSR. The following diagnostic is applicable. 1. With bit 02 set, writes data to memory with any pattern. 2. Read first location in memory, if bit 00 of the CSR is set, then a parity error indication is detected on the LSI 11 bus, and the failed address (location 0) is stored in the CSR. 3. Reads the CSR and obtains the failed address: CSR bit 14 = 0 implies A11-A17 on CSR bits 05-11. CSR bit 14 = 1 implies A18-A21 on CSR bits 05-09. Bit 02 is a

CSR Bit Descriptions (Cont)

Bit	Name	Description
01	Not used	read/write bit reset to zero on power-up or BUS INIT.
00	Parity Error Enable	If a parity error occurs on a DATI or DATIO(2) cycle to memory, and bit 00 is set equal to 1, then BDAL 16 L and DDAL 17 L are asserted on the bus simultaneously with data. This is a read/write bit reset to zero on power-up or BUS INIT.

MXV11-AA,AC MULTIFUNCTION MODULE

The MXV11 is a multifunction option module used for the LSI-11, LSI-11/2, or LSI-11/20 systems. It contains read/write memory provisions for read-only memory, two asynchronous serial line interfaces, and a 60 Hz clock derived from a crystal oscillator.

Detailed technical information is beyond the scope of this document. Additional information can be found in the *Microcomputer Processor Handbook*, EB-15451-20.

Model Designations

- MXV11-AA contains 8K bytes of random access memory.
- MXV11-AC contains 32K bytes of random access memory.

Both models have two 24-pin sockets that provide for 1 to 2 read-only memories in which 1K $\times$ 8, 2K $\times$ 8, or 4K $\times$ 8 ROMs may be used. These sockets may also be used for 256 words of bootstrap code.

Amperes		Bus Loads		Cables
+5	1.2	AC	DC	BC20M-XX
1.2	0.1	2	2	BC20N-XX (Refer to DLV11-KA)
				BC21B-XX

Standard Addresses

RAM - Starts on any 8K boundary below 0400.

SLU	Channel 0	Channel 1
	178500	177560

To disable RAM:

MXV11-AC	Remove W4
MXV11-CA	Remove W5

Standard Vectors

SLU 000 00.

Diagnostic Programs

Refer to Appendix A.

Requires wraparound connectors to completely exercise SLU.

Related Documentation*MXV11-A Memory and Asynchronous Serial Line Interface User Guide (M5047)*

(FK-MXV1A-UB)

Field Maintenance Print Set (MF-30750)

Options

MXV11-AA and ROMs for PXB2, PXB1, or TUB

P/Ns: 23-13143-00, 23-13253-00

ROMsPower: -5 V $\pm$ 5%

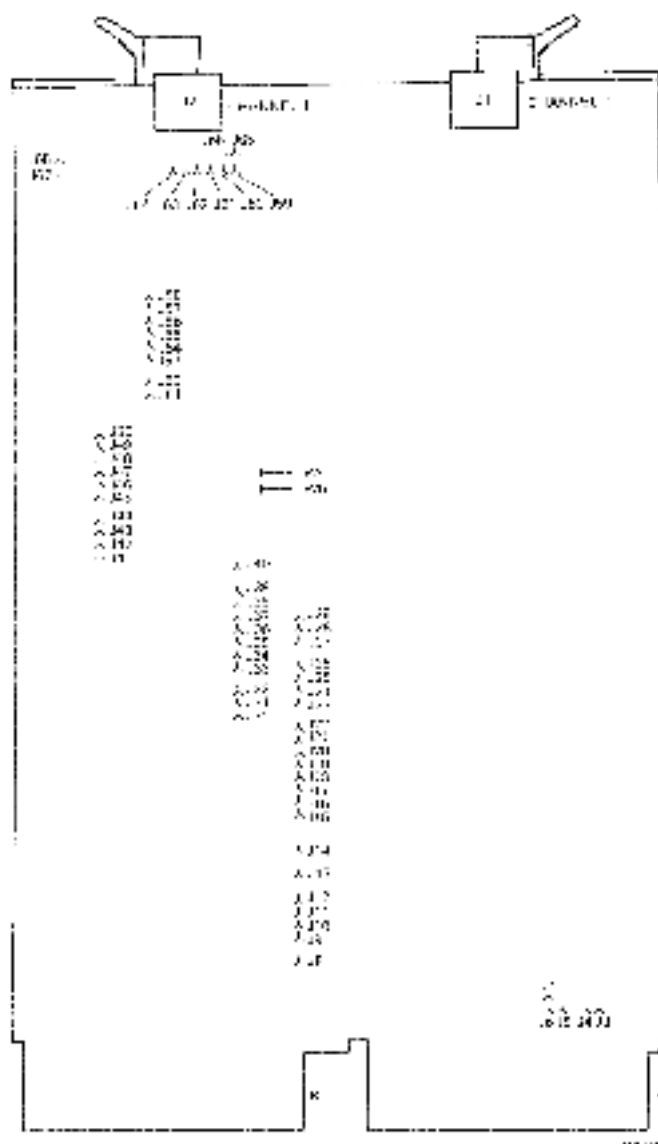
Pins: 24 Pin DIP

Access Time: Up to 450 nanoseconds

Array Size: 1K $\times$ 8, 2K $\times$ 8, or 4K $\times$ 8 bits

Type: Typical PROM types:

UV PROMs	Chip Array Size	Memory Size
Intel 2758	1K $\times$ 8 bits	1K words
Intel 2716	2K $\times$ 8 bits	2K words
Intel 2732	4K $\times$ 8 bits	4K words
Motorola MC2716	2K $\times$ 8 bits	2K words
T.J. TMS 2616	2K $\times$ 8 bits	2K words
T.J. TMS 2632	4K $\times$ 8 bits	4K words
Bipolar PROMs		
Intel 1820	1K $\times$ 8 bits	1K words
Signetics 82S 2708	1K $\times$ 8 bits	1K words
Signetics 82S 181	1K $\times$ 8 bits	1K words
Signetics 82S 191	2K $\times$ 8 bits	2K words



MXV11-AA Jumper Locations

MXV11-A Jumper Functions

Pin	Function	Option
J3	CLOCK. Open collector output of the clock. Connected to pin AE1 (SSpin 2). Wirewrap to J4 to implement the clock option.	60 Hz
J4	DEVNT L. Event interrupt (pin BF1) used for the clock option.	60 Hz
J5	BOOTCK H. BOOT (pin BA1) when high allows the processor to operate when low initializes the system. Connected to J11 to use the boot option.	Boot
J6	Framing Error. Open collector output of framing error from serial line one. Connected to pin AE1 (SSpin 1). Wirewrap to J5 to implement the boot option. Reset by bus initialize or reception of a valid character.	Break
J7	EHALT L. Halt (pin AF1) when low will stop program execution and cause the processor to enter GDT microcode. Connected to J6 to implement the halt option.	Halt
J8	GND. A ground signal that can be used to disable ROM by wirewrapping to J21 or to disable a serial line by wirewrapping to an address input pin (J20 or J24 for serial line B; or J25, J26, J27, or J28 for serial line C).	ROM
J9	A10 L. Address bit 10 asserted low. Wirewrap to J11 to select bank 1 with the ROM address decoder.	ROM
J10	A10 H. Address bit 10 asserted high. Wirewrap to J11 to select bank 0 with the ROM address decoder.	ROM
J11	A10 M. Address bit 10 input to the ROM address decoder. See J9 and J10. Used only if J20 is wirewrapped to J21.	ROM
J12	A03 H. Address bit 03 asserted high. Wirewrapped to the serial line address decoders (J23 or J24 for serial line B; J25, J26, J27, or J28 for serial line C) when address bit 03 is to be decoded as a 1.	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Action
J13	A04 H. Address bit 04 asserted high. Wirewrapped to the serial line one address decoder when address bit 04 is to be decoded as a 1.	SLU
J14	A05 H. Address bit 05 asserted high. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 1.	SLU
J15	A09 H. Address bit 9 asserted high. Wirewrapped to the serial line one address decoder when address bit 09 is to be decoded as a 1.	SLU
J16	A09 L. Address bit 09 asserted low. Wirewrapped to the serial line one address decoder when address address bit 09 is to be decoded as a 0.	SLU
J17	A05 L. Address bit 05 asserted low. Wirewrapped to the serial line one address decoder when address bit 05 is to be decoded as a 0.	SLU
J18	A04 L. Address bit 04 asserted low. Wirewrapped to the serial line one address decoder when address bit 04 is to be decoded as a 0.	SLU
J19	A03 L. Address bit 03 asserted low. Wirewrapped to the serial line address decoder when address bit 03 is to be decoded as a 0.	SLU
J20	ROM address. Output of the ROM address decoder. Connected to J21 when ROM is to be used in bank 0 or bank 1.	ROM
J21	ROM select. ROM address selection enable asserted high. Wirewrapped to J6 (GH0) to disable ROM, to J20 for bank 0 or bank 1, or to J22 for bootstrap.	ROM
J22	Root address. Output of the bootstrap address decoder. Connected to J21 when ROM is to be used in the bootstrap range from 173000-173776 (778000-778776 for L6H-11/23).	ROOT
J23	Serial line C address decoder input asserted high. May be wirewrapped to A03 H (J12), A03 L (J19), A04 H (J13), or A04 L (J18).	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option																																													
J24	Serial line 0 address decoder input asserted high may be wirewrapped to A02 or A04, whichever bit is not wired to J20. May be wirewrapped to GND (J8) to disable serial line 0.	SH																																													
J25 J26	Serial line 1 address decoder input asserted high. Four address decoder inputs to be connected to address bits A03, A04, A05, and A06. Whether the high or low assertion state of a bit is wirewrapped to an input determines if that bit is decoded as a 1 or a 0. See J12 through J19. May be wirewrapped to GND (J8) to disable serial line 1.	SH																																													
J29	ROM address bit 08 input. Wirewrapped to A09 H (J15) for normal ROM addressing and also for the MXV11-A2 option when the TUS3 bootstrap is desired. Wirewrapped to A09 L (J16) for the MXV11-A2 option when the disk bootstrap is desired.	ROM																																													
J30 J31	RAM starting address selection. These pins are wirewrapped to J33 (logic 0) or J34 (logic 1) to select the RAM starting address (see the following)	RAM																																													
	<table><tr><th>J32</th><th>J31</th><th>J30</th><th>Bank</th><th>Starting Address</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>000000</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>020000</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2</td><td>040000</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3</td><td>060000</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4</td><td>100000</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5</td><td>120000</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6</td><td>140000</td></tr><tr><td>1</td><td>1</td><td>1</td><td>7</td><td>160000</td></tr></table>	J32	J31	J30	Bank	Starting Address	0	0	0	0	000000	0	0	1	1	020000	0	1	0	2	040000	0	1	1	3	060000	1	0	0	4	100000	1	0	1	5	120000	1	1	0	6	140000	1	1	1	7	160000	
J32	J31	J30	Bank	Starting Address																																											
0	0	0	0	000000																																											
0	0	1	1	020000																																											
0	1	0	2	040000																																											
0	1	1	3	060000																																											
1	0	0	4	100000																																											
1	0	1	5	120000																																											
1	1	0	6	140000																																											
1	1	1	7	160000																																											
J33	GND. Logic 0 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.	RAM, ROM																																													
J34	+5 V. Logic 1 level signal used for selecting the RAM starting address and for enabling some ROM ICs in the ROM sockets.	RAM, ROM																																													

MXV11-A Jumper Functions (Cont.)

Pin	Function	Option
J35	A12 H. Address bit 12 asserted high. Used for addressing 64×8 bit ROMs. Wirewrapping to J37, J38 or J39, depending on the ROM used.	ROM
J36	A11 H. Address bit 11 asserted high. Used for addressing $2K \times 8$ and $4K \times 8$ bit ROMs. Wirewrapping to J37, J38, or J39, depending on the ROM.	ROM
J37	Pin 12 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for $+1.5$ V, to J85 for A12, or to J86 for A11.	ROM
J38	Pin 12 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for $+1.5$ V, to J35 for A12, or to J36 for A11.	ROM
J39	Pin 21 on both ROM sockets. Used for addressing or enabling ROM. Wirewrapped to J33 for ground, to J34 for $+5$ V, to J35 for A12, to J36 for A11, or to J40 for $+1.5$ V.	ROM
J40	$+1.5$ V. Used to power some ROMs on pin 21.	ROM
J41	Used for 150 baud. Wirewrapped to J45 for serial line 0, to J43 for serial line 1. (See following table.)	SLU
J42	Used for 1200 baud.	SLU
J43	Used for 300 baud.	SLU
J44	Used for 2400 baud.	SLU
J45	Clock 0. The clock input for serial line 0 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.	SLU
J46	Clock 1. The clock input for serial line 1 transmit and receive, 16 times the baud rate. Wirewrapped to either J41, J42, J43, J44, J47, J48, J49, or J50.	SLU
J47	Used for 4800 baud.	SLU
J48	Used for 9600 baud.	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J49	Used for 15.2K baud.	SLU
J50	Used for 38.4K baud.	SLU
J51	Vector 0. Vector enable for channel 0. Used to drive vector bits that pass the test: logic 1 for channel 0, and logic 0 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J56 for bit 05, to J56 for bits 06 and 07.	SLU
J52	Vector 1. Vector enable for channel 1. Used to drive vector bits that pass the test: logic 0 for channel 0 and logic 1 for channel 1. Wirewrapped to J53 for bit 03, to J54 for bit 04, to J55 for bit 05, to J56 for bits 06 and 07.	SLU
J53	Vector bit 03. Selects how bit 03 is to be driven for interrupt vectors. Wirewrapped to J51 if a logic 1 for channel 0 and a logic 0 for channel 1, to J52 if a logic 0 for channel 0 and a logic 1 for channel 1, to J53 if a logic 0 for both channel 0 and channel 1, or to J50 if a logic 1 for both channel 0 and channel 1.	SLU
J54	Vector bit 04. Selects how bit 04 is to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J55	Vector bit 05. Selects how bit 05 is to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J56	Vector bits 06 and 07. Selects how bits 06 and 07 are to be driven for interrupt vectors. Wirewrapped the same as J53.	SLU
J57	GND. Logic 0 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 0 for both serial line channels.	SLU
J58	+3 V. Logic 1 signal for configuring vector bits. Wirewrapped to J53, J54, J55 and/or J56 when the corresponding vector bit(s) will be logical 1 for both serial line channels.	SLU

MXV11-A Jumper Functions (Cont)

Pin	Function	Option
J59	Seven bit parity, eight bits no parity, channel 1. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity.	SLU
J60	Two stop bits. Selects one or two stop bits for channel 1. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits.	SLU
J61	Even parity. Selects odd or even parity for channel 1 when seven bits with parity (J61 wirewrapped to ground) is selected. Wirewrapped to ground (J65) for odd parity or to +3 V (J66) for even parity.	SLU
J62	Seven bit parity, 8 bits no parity, channel 0. Wirewrapped to ground (J65) for seven bits with parity or to +3 V (J66) for eight bits with no parity.	SLU
J63	Two stop bits. Selects one or two stop bits for channel 0. Wirewrapped to ground (J65) for one stop bit or to +3 V (J66) for two stop bits.	SLU
J64	Even parity. Selects odd or even parity for channel 0 when seven bits with parity (J64 wirewrapped to ground) is selected. Wirewrapped to logic 0 (J63) for odd parity or to logic 1 (J66) for even parity.	SLU
J65	Logic 0. Ground signal used for configuring peer station interfaces.	SLU
J66	Logic 1. +3 V signal used for configuring line interfaces.	SLU
J67	Clock in. Clock input for baud rates, memory refresh and negative voltage generator. Wirewrapped to J68. Not a user option.	SLU
J68	Clock out. Crystal oscillator output at 19.6608 Mhz. Wirewrapped to J67. Not a user option.	SLU

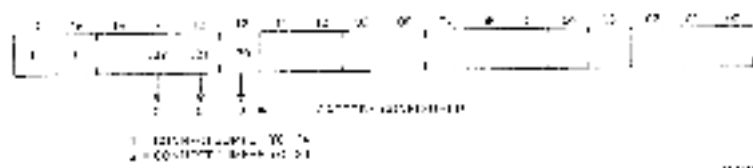
Standard Factory Configuration

Function	Wirewrap From	Pins To	Wirewrap Level
RAM Bank 0	J30 J32 J31	J31 J33 J32	L1 L1 L2
SLU Channel 0 Address 176500	J20 J24	J18 J19	L1 L1
SLU Channel 1 Address 177560	J28 J26 J25 J27	J13 J16 J14 J12	L2 L1 L1 L1
ROM Bootstrap (11552)	J27 J21 J34 J33 J29	J38 J32 J37 J39 J15	L1 L1 L2 L2 L2
SLU Vectors CH0 (800) CH1 (80)	J53 J64 J58 J54	J57 J52 J51 J55	L1 L1 L1 L2
SLU Parameters (8 Data Bits, No Parity, 1 Stop Bit)	J59 J62 J60 J61 J56 J63	J61 J64 J63 J62 J65 J66	L1 L1 L1 L2 L2 L2
Hard Rates CH0 (38.4K) CH1 (9600)	J45 J48	J50 J48	L1 L1
Break Generation (Halt Option)	J8	47	L1
Crystal Clock	J68	J67	L1

Configuring the RAM

The RAM can be configured to start on any 8KB boundary below 64KB. Because of this restriction, the MXV11 (2KB version) is not usable for memory above 56KB. The MXV11 can be used in 18-bit memory address systems, but it is restricted to being assigned to the memory area at or below 56KB.

Five wirewrap terminals, J50 through J54, select the starting address. The following figure shows the jumper configurations required to obtain the desired selected addresses.



EAT# Streaming Address Selection

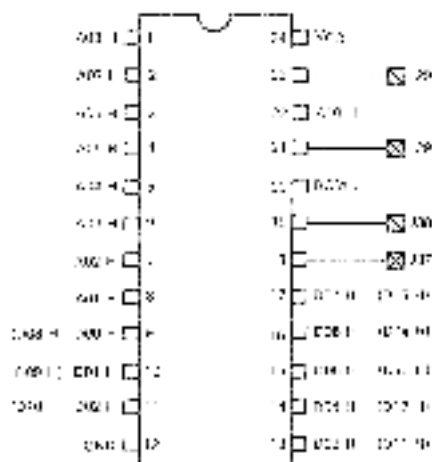
Configuring the ROM

Depending on the ROM type, the module's capacity is 1K, 2K, or 4K words using a pair of 1194×8 , 2048×8 , or 4096×8 -bit ROMs respectively. The J6801 configures jumpers on the module for the ROM type being used. The actual procedure for loading data into EPROMs, PROMs (or writing specifications for masked ROMs) will vary depending on the manufacturer, and is beyond the scope of this section. The user must refer to the manufacturer's data sheets and to the chapter, "Using PROMs" in the *Microcomputer Processor Handbook*, EB-18451 (2). The user must be aware of the relationship of the EPROM, PROM, or ROM pins to the LSI 11 data bus, and the relationship of the pins to the memory address bus. Refer to the following figure for ROM socket pin assignments. All ROMs used on the MSB11-A must conform to these pin assignments.

The factory configuration allows for using the MBV11 A2 bootstrap ROMs.

Configuring the Bootstrap ROM – The ROM can be configured to operate in the I/O page to support bootstrap programs. The address area contains 256 words from 1A000 to 1A378 (223000 to 223226 for the 1A11/20).

The MXV11-A is configured at the factory to allow for using the MXV11-A2 TUSB bootstrap. To reconfigure the MXV11-A to use the *d* sk bootstrap, remove jumper J29 to J10 and install jumpers J29 to J16.



NOTES:

1. Jumper J10 to J11 selects a bootstrap ROM.
2. Jumper J12 to J13 selects a bootstrap ROM.
3. Jumper J14 to J15 selects a bootstrap ROM.
4. Jumper J16 to J17 selects a bootstrap ROM.

FIGURE 1

MXV11-A ROM Socket Pin Assignment

ROM Bank Selection – If the MXV11-A sockets are used for program ROM instead of a bootstrap ROM, the memory must be selected by a jumper connecting J20 to J21. When main ROM memory is selected, the entire 4K word bank is enabled. If a 1K or 2K ROM is used, it will “wraparound” and give invalid data, depending on how the address lines are configured when the nonexisting ROM area is addressed. Main memory may be positioned in bank 0 or bank 1. To position the ROM in bank 0, jumper J10 to J11. To position the ROM in bank 1, jumper J16 to J17.

Configuring the Specific ROM Types – Additional jumpers must be connected depending on the type of ROM used. The “EPROM Address Jumpers” table describes the jumper configuration when using typical ROMs such as the Intel 2716 (2K \ 0) or 2732 (4K \ 16) EPROMs. The user must refer to the manufacturer’s data sheets when configuring jumpers for other ROM types.

The function of wirewrap pins J28, J30, J37, and J39 are shown in the following table. These pins are to be connected as required to pins J38 through J40.

ROM Upgrade Part Numbers

25-131F3-00
25-122F3-00

EPROM Address Jumpers

Function	From	2716 ROM		2732 ROM	
		Bank 0 to	Bank 1 to	Bank 0 to	Bank 1 to
Bank Enable	J20	J21	J21	J21	J21
Bit 09 Input	J29	J15	J15	J15	J15
Address or Enable	J36	J36	J36	J36	J36
Address or Enable	J37	J35	J35	J35	J35
Address or Enable	J39	J40	J40	J33	J34

CONFIGURING THE SERIAL LINE UNITS

Serial Line Register Address Selection

Four device registers (RCSR, RBUF, XCSR, and XBUF) are provided for each of the two serial lines. Jumpers are configured to establish separate base addresses for each serial line as shown.

- Serial port 0 may be assigned to one of the four starting addresses 176500, 176510, 176520, 176530.
- Serial port 1 may be assigned addresses in two ranges. The first range starts at 176500 and covers the eight starting addresses from 176500 to 176570. The second range starts at 177500 and also contains eight possible starting addresses, including the standard console address, 177560. Since several other standard DIGITAL devices use addresses in this second range, it is recommended that only the console address be used.

The format of an SLL address is shown in the following figure. Note that bits 12-17 are neither configured nor decoded by the MXV11-A module. These bits are decoded by the bus master module as the bank 7 select (B0S7 L) bus signal. This signal becomes active only when the I/O page is accessed. Bit 0 is used as the byte pointer.



MXV11-A SLL Address Format

Bits 1 and 0 select one of the four device registers within the addressed serial line. Bits 3 and 4 are used to select one of four possible device addresses for serial line 0. Bits 0, 4, 5, and 9 are used to select the device addresses in two ranges for serial line 1 (console). The following table describes the jumper combinations to select one of four device addresses for serial line 0 (I/O).

Serial Line 0 Address Jumpers

Address (Octal)	Jumper Posts	
	J23 to	J24 to
176500	J15 (Logic 0)	J18 (Logic 0) Factory Configuration
176510	J16 (Logic 0)	J12 (Logic 1)
176520	J13 (Logic 1)	J18 (Logic 0)
176530	J12 (Logic 1)	J19 (Logic 1)

NOTE

Logic 1

J13 (A04 H)

J12 (A03 H)

Logic 0

J18 (A04 L)

J19 (A03 L)

Serial line 1 may have 16 possible device addresses in two ranges. The following table describes the jumper combinations to select the eight device registers available in range 1. Only one device address is used in range 2.

Serial Line 1 Address Jumpers

Address (Octal)	Jumper Posts			
	J26 to	J25 to	J27 to	J28 to
176500	J16	J17	J18	J19
176510	J16	J17	J18	J19
176520	J16	J17	J19	J18
176530	J16	J17	J19	J18
176540	J16	J14	J18	J19
176550	J16	J14	J18	J19
176560	J16	J14	J18	J19
176570	J16	J14	J19	J18
Range 2				
177560	J15	J14	J13	J18

(See the following table.)

NOTE

Factory configurations use only one address in range 2 to avoid possible device conflicts. The remaining addresses are pre-assigned to other devices.

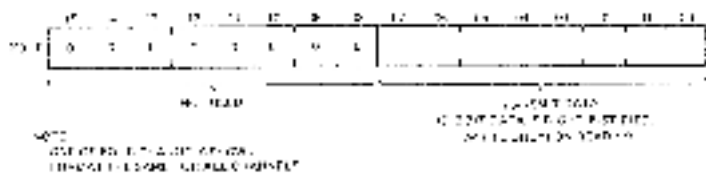
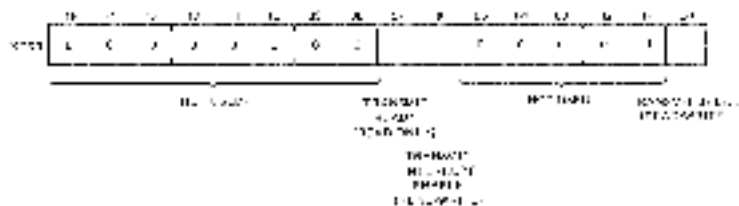
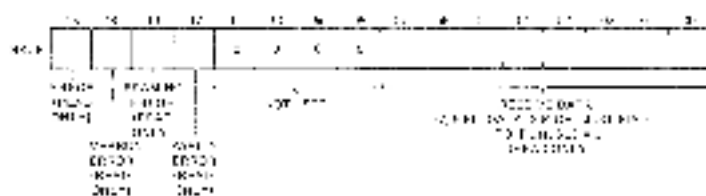
Logic 1	Logic 0
J15 (A09 H)	J16 (A09 L)
J14 (A08 H)	J17 (A08 L)
J13 (A04 H)	J18 (A04 L)
J12 (A03 H)	J19 (A03 L)

Control/Status Register

The MXV11-A has two control/status registers (CSRs) for each of its two serial lines. The following figure shows the control/status registers and the read/write data registers. Transmitter control/status registers 0 and 1 (XCSTR0 and 1) and receiver control/status registers 0 and 1 (RCSTR0 and 1) operate with serial lines 0 and 1, respectively.

Both serial lines have the same bit assignments. There are four registers for each serial line. They are sequential in this order: 0, receiver status; 2, receiver data; 4, transmitter status; and 6, transmitter data. All unused bits are read as 0.

MXV11-AA.AC/M8047



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MXV11-A SLU CSN Fy/Tala

Bit Assignments for the Receiver Status Register

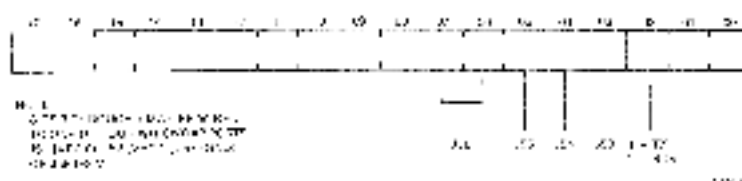
Bit	Function
6	Interrupt enable, read/write. A 1 enables receiver interrupts. A 0 disables interrupts. Cleared by initialize.
7	Receiver done, read only. A 1 indicates that the serial interface has received a character. If enabled by bit 6, receiver done will request an interrupt. Receiver done is cleared by reading the receiver data register or by initialize.
0-7	Data bits, read only. Bit 0 is the least significant bit and bit 7 is the most significant. If seven data bits plus parity is selected, bit 7 will always read as a 0.
12	Parity error, read only. A 1 indicates that the word being read in bits 0 through 6 has a parity error. Bit 12 will always read 0 when eight data bits and no parity are selected. Cleared when read, or by initialize.
13	Framing error, read only. A 1 indicates that a start bit was detected, but there was no corresponding stop bit. A framing error will be generated when a break is received. Cleared when read, or by initialize.
14	Overrun error, read only. A 1 indicates that a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read, or by initialize.
16	Error, read only. A 1 indicates that one or more of bits 12, 13, and 14 are 1. Cleared when read, or by initialize.

Bit Assignments for the Transmitter Status Register

Bit	Function
0	Break read/write. When set to a 1, bit 0 ceases the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when 1 is received and is regarded as a break. Cleared by writing a 0, or by bus initialize.
8	Interrupt enable, read/write. A 1 enables transmitter interrupts; a 0 disables interrupts. Cleared by initialize.
7	Transmitter ready, read only. A 1 indicates that the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 8, transmitter ready will request an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by initialize.
6-7	Data bits, write only. Bit 6 is the least significant bit and bit 7 is the most significant bit. If seven data bits plus parity are selected, bit 7 will not be transmitted. The transmitter data register will read all 0s.

Interrupt Vector Selection

Two consecutive interrupt vectors (one for receive and one for transmit) are provided for each of the two serial lines. The interrupt vector format is shown in the following figure. Each SLC port can be independently configured to operate in one of two ranges: 000 to 074, or 080 to 37E.



MXV11-A Interrupt Vector Format

The following table lists the vector addresses that may be assigned to the serial lines. Note that all vector addresses in the 000 to 074 range, except 000, are reserved vector locations. The jumper selectable bits are 0 through 4. Bits 5 and 7 are wired together.

Serial Line Vector Addresses

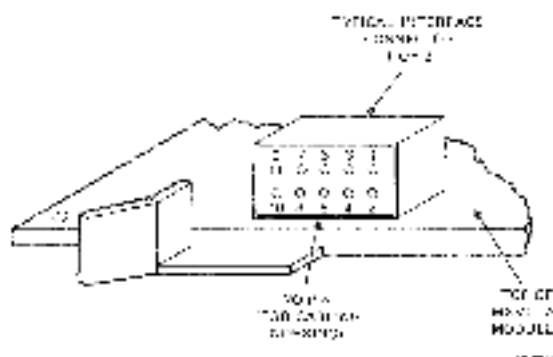
Serial Line 1 (Console)	Serial Line 0 (V/D)
000	000
010	010
020 DIGITAL Reserved	020
030 Digital Jan	030
040	040
050	050
060 Console	060
070 DIGITAL Reserved	070

The following example illustrates the procedure for configuring the vector addresses. Assume that 00 is the address for serial line 1 (console) and 010 is the address for serial line 0 (V/D). The example describes the relationship between the vector bases, vector address bits, and the jump points. The jumpers are configured using the following four rules:

1. If a bit = 1 in both vector bases, it is tied to J58 (vector 1).
2. If a bit = 0 in both vector bases, it is tied to J61 (vector 0).
3. If a bit = 1 for serial line 1 and a 0 for serial line 0, it is tied to J52 (vector 1).
4. If a bit = 0 for serial line 1 and a 1 for serial line 0, it is tied to J61 (vector 0).

Interface Connector Pins

Two 10-pin connectors (one for each serial line) are provided on the MXV11-A module. Connector pins and signal functions are described in the following table and shown in the following figure.



MXV11-A Connector Pins

MXV11-A I/O Connector Pin Functions

Pin	Signal	Function
1	UART CLOCK	The baud rate clock appears on this pin. When an internal baud rate is selected, this pin is a TTL output. When no baud rate is selected on the module, this is an external baud rate input. The high level for the clock is > 3.0 V.
2	GND	Transmitter output
3	XMIT+	
4	GND	
5	GND	Key pin not provided
6	NC	
7	RCV	
8	RCV	
9	GND	Receiver input most positive
10	-12 V	Power for the DLV11-KA option

Current Loop

The MXV11-A module can interface with 20 mA active or passive current loop devices when used with the DLV11-KA option. This option consists of a DLV11-KB (EIA to 20 mA current loop converter) and a RDP1A-03 interface cable. The MXV11-A does not have the capability to support the read-back portion of the DLV11-KA option. The DLV11-KA option is placed between the MXV11-A serial line output and the 20 mA current loop peripheral device.

MXV11-A Interface Cables

Cable	Application	Length
BC21B-05	EIA RS-232C modem cable to interface with modems and acoustic couplers (2 x 5-pin AMP female to RS-232C male).	1.5 m (5 ft)
BC20N-05	EIA RS-232C full modem cable to directly interface with a local EIA RS-232C terminal (2 x 5-pin AMP female to RS-232C female).	1.5 m (5 ft)
BC20M-50	EIA RS-422 or RS-423 cable for high speed transmission (15.2K baud) (2 x 5-pin AMP female to 2 x 5-pin AMP female).	15 m (50 ft)
BC05B-10	Extension cable used in conjunction with BC21B-05.	5 m (16 ft)
BC05B-25	Extension cable used in conjunction with BC21B-05.	7.6 m (25 ft)
BC05B-25	"Null modem" extension cable used in conjunction with BC21B-05.	7.6 m (25 ft)

NOTE

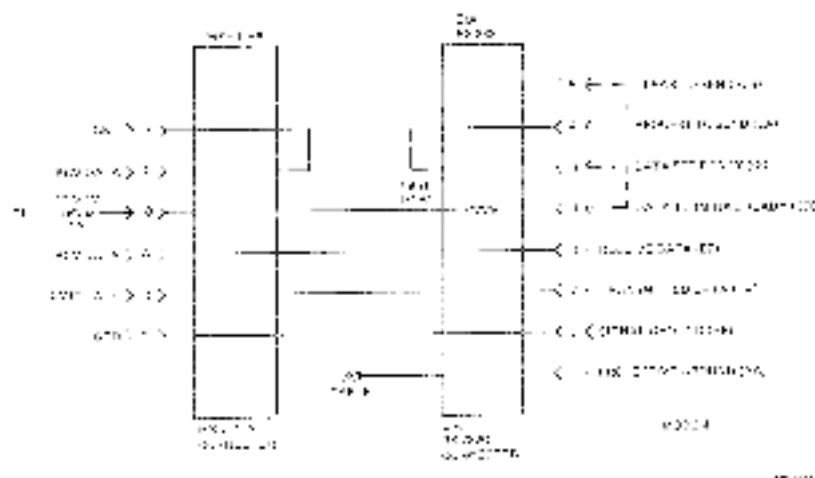
"Strapped" logic levels are provided on Data Terminal Ready (DTR) and Request To Send (RTS) for operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).

The MXV11-A may operate with several peripheral device cables and options for flexibility when configuring systems. A variety of cables and options, as well as the primary application of each, are shown with the MXV11-A.

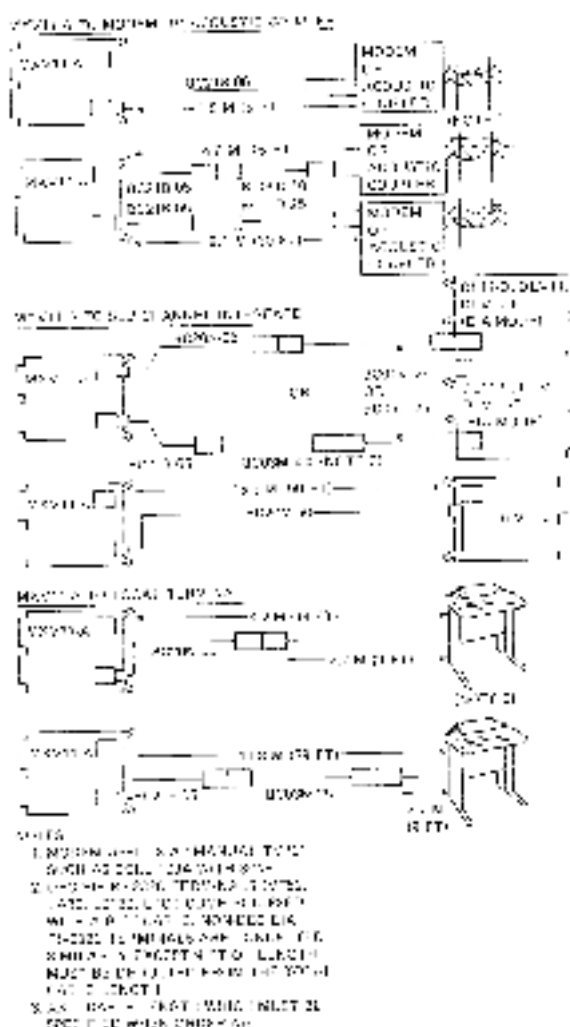
1. The receivers on the MXV11 have differential inputs. Therefore, when designing an RS-232C or RS-423 cable, receive data (pin 7 on the 2 × 5 pin AMP connector) must be tied to signal ground (pins 2, 6, or 8) in order to maintain proper EIA levels (see the following figure).
2. To connect directly to a local EIA RS-232C terminal, it is necessary to use a null modem. To design the null modem into the cable, one must switch received data (pin 2) with transmitted data (pin 3) on the RS-232C male connector as shown in the following figure.

To mate to the 2 × 5-pin connector block, the following parts are needed:

Cable Receptacle (QTY 1)	AMP PN 87133-5 DEC PN 12-14263-02
Locking Clip Connects (QTY 10)	AMP PN 87124-1 DEC PN 12-14267-00
Key Pin (pin 6) (QTY 1)	AMP PN 87179-1 DEC PN 12-15419-00



RJ45 to Modem Cable



MD211-A FLS Cable Configuration:

MXV11-B MULTIFUNCTION OPTION MODULE

GENERAL

The MXV11-B is a multifunction option module used with the PDP-11/23 and K11-1 processor systems. The MXV11-B read/write memory contains 129K bytes of dynamic MOS RAM without parity. The MXV11-B is configured from 84K SIPS (single in-line package). Four SPS provide 128K bytes (84K words) of memory storage. Battery backup is supplied when jumpers are configured to enable this feature and system supplied power is removed. This dual-height multifunction module option can operate on a 32-bit Q-Bus system, up to 81K words on an 18- and 16-bit Q-Bus system (1).

Features

- 19K MOS RAM memory
- 5 V battery backup for MOS RAMs
- Read only memory (ROM)
- ROM window map logic (page control register)
- Two asynchronous, serial, line ports (SL00 and SL01)
- Multiple I/O frequencies
- LPC diagnostic display register

Electrical Specifications

Power Requirements - The following voltages are used by this module.

Voltage	Tolerance	Pins
+5 V	±5%	AA3, BA2, DV+
+12 V	±5%	AD2, BD2
+5 VB	±5%	AV1

Power dissipated in each power supply configuration is as follows.

No battery backup

+5 V	+12 V	
Typ	17.25 W	Typ 0.87 W
Max	25.67 W	Max 0.71 W

Battery backup configuration

-5 V		+5 VB		+12 V	
Typ	12.90 W	Typ	4.95 W	Typ	3.57 W
Max	15.95 W	Max	8.65 W	Max	3.71 W

Data retention mode

VCC = 0 V, 12 V supply = 0

+5 VBI

Typ	4.25 W
Max	5.54 W

Related Documentation*MXV11-B Technical Manual (HK-MXV10-TM)**MXV11-B User Guide (HK-MXV10-UG)**MXV11-B2 ACist Set User Guide (EK-MXVB2-UG)**MXV11-B Multifunction Option Module User Guide (HK-MXV10-UG)**MXV11-B Field Maintenance Print Set (MP-01100-00)***Program Options and Defaults**

		Address/Vector
One MXV11-B	Channel 0	778500/320
	Channel 1	777580/60
Two MXV11-Bs	Channel 2	776510/310
	Channel 3	776520/320

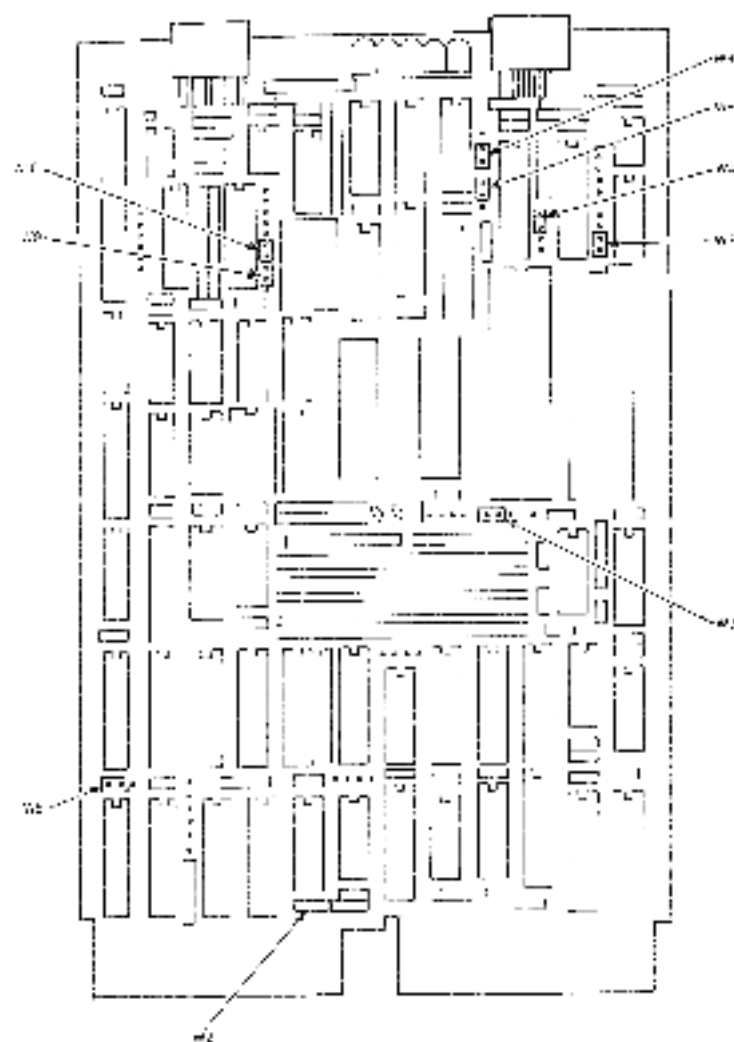
Diagnostic Programs

CMVX.BAO	Test Functions
	Serial lines ROM Clock option Page Control Register (PCR) Diagnostic Display Register (DDV) Random Access Memory (RAM)

MXV11-B/M7195

Definite jumpers

The delugli printers are as shown below:



Default Configuration of Push-On Connectors

Interface Connector Pins

Two 13-pin connectors, one for each serial line, are provided on the MXV11-B module. The connector pins and signal functions are described below.

MXV11-B I/O Connector Pin Functions

Pin	Signal	Function
1	8FDCLK	Baud rate clock. This output provides a clock signal at a frequency of 16 times the selected baud rate. This pin is used as an output from the MXV11-B and does not accept external clock inputs.
2	Ground	
3	XMIT-	Transmitter output
4	Ground	
5	Ground	
6	NC	Key, pin not provided
7	RCV-	Receiver input most negative
8	RCV+	Receiver input most positive
9	Ground	
10	+12 V	Power for the OLVI1-KA option

Jumpers are used to configure:

Console mode	Reboot
MXV11-B2 boot ROM set	Line time clock
System size	EVENT line
Root and diagnostic ROMs	Software programmed baud rates
Clock	Battery
Halt	User-supplied ROMs

Baud Rates

Each serial line can be software programmed or strapped to 300, 1200, 9600, or 38,400 baud and is compatible with EIA RS-422 or RS-232C signal levels.

When bit 06 is set, the BEVENT line clamp is removed and LTC is functional. The I/O address is 777546.

CAUTION

There should be only one source drive on the BEVENT line in any system. On most systems, the system power supply provides the bevent signal; this source must be disabled if the MXV11-B is used to drive the line clock.

This register is a write-only register, but generates a reply on DAT0 and DAT10 lines. The DDR resides in location 777524 on the I/O page and is enabled when the MXV11-B has its analog and console functions enabled.

Serial Line Unit Baud Rates

			SLU0 (See Note) J0A to GND (J10 to J9)	Baud Rates
J11	J0B	R	R	300*
J10	J0B	R		1200
J9	GND	I	0	9600
		I	I	38.4K
			SLU1 (See Note) J1B to GND (J7 to J6)	Baud Rates
J9	GND	R	0	9600*
J8	J1A	R	I	38.4K
J7	J1B	I	R	300
		I	I	1200

R = jumper removed

I = jumper inserted to ground

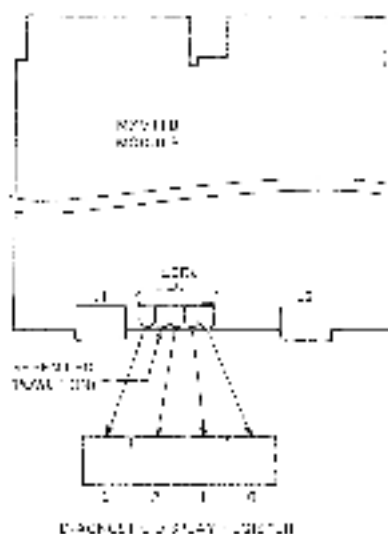
*Shipped configuration

NOTE

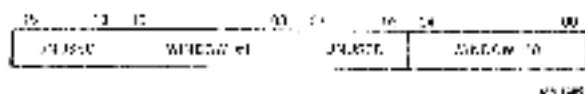
SOFT EN to GND jumper (J14 to J13) must be removed; otherwise these jumpers have no effect. If the SOFT EN to GND jumper (J14 to J13) is installed and FBRE bit 1 is set, baud rates are software controlled.

LED Diagnostic Display Register

The MXV11 has a diagnostic display register (DDR) which has four red LEDs to show system diagnostics and one green LED to indicate power-on.



MXV11-B Diagnostic Register (DDR)



Page Control Register

ROM Window Addresses for 16-, 18-, and 22-bit Q-Bus

Q-Bus	Window 1 Start Addr (octal)	End Addr (octal)	Window 0 Start Addr (octal)	End Addr (octal)
16-bit	165000	165777	173000	173377
18-bit	165000	165777	173000	173377
22-bit	17765000	17765777	17770000	17770377

ROM Window Map

Window Field	Normalized 9 ROM Address	
0	00000	
1	01000	
2	02000	
3	03000	
4	04000	
5	05000	
6	06000	
7	07000	Maximum address for 2K by 8 PROM
10	10000	
11	11000	
12	12000	
13	13000	
14	14000	
15	15000	
16	16000	
17	17000	Maximum address for 4K by 8 PROM
20	20000	
21	21000	
22	22000	
23	23000	
24	24000	
25	25000	
26	26000	
27	27000	
30	30000	
31	31000	
32	32000	
33	33000	
34	34000	
35	35000	
36	36000	
37	37000	Maximum address for 8K by 8 PROM

Receiver Status Register Bit Assignments (RCSR)

Bit		Description
15-12		Unused
11	RA Receiver active read only	A logic one indicates that the receiver is active. Set at the center of the start bit of the input serial data. Cleared at the expected center of the stop bit at the end of the data prior to the leading edge of RCV DUNE. Also cleared by power-up sequence.
10-8		Unused
7	RI	A logic one indicates that the serial interface has received a character. If enabled by bit 6, receiver done requests an interrupt. Receiver done is cleared by reading the receiver data register or by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables receiver interrupts. A zero disables interrupts. Cleared by initialization.
5-0		Unused

Receiver Data Buffer Bit Assignments (RBUF)

Bit		Description
15	ER Error read only	A logic one indicates that bit 13 and/or bit 14 is a one. Cleared when the bit is read or cleared by power-up sequence.
14	OE Overflow error read only	A logic one indicates a word in the receiver buffer had not been read when another word was received and placed in the receiver buffer. Cleared when read or by power-up sequence.
13	FE Framing error read only	A logic one indicates that a start bit was detected, but there was no corresponding stop bit. A framing error is generated when a break is received. Cleared when read or by power-up sequence.
12		Unused
11	RB Receiver break read only	This bit is set when serial-in (SI) signal goes from a mark to a space and stays in the space condition for 11 bit times after serial reception starts. This bit is cleared when the SI signal returns to the mark condition, or by power-up sequence.
10-8		Unused
7-0	DATA read only	These eight bits hold the most recent byte received. When a new byte is transferred to the data buffer, the RCVDONE in the RCSR is set. Bit 0 is the LSB and bit 7 is the MSB. Cleared by power-up sequence.

Transmitter Status Register Bit Assignments (XCSR)

Bit		Description
15-8		Unused
7	TX Transmitter ready read-only	A logic one indicates the serial interface is ready to accept a character into the transmitter data register. If enabled by bit 6, transmitter ready requests an interrupt. Transmitter ready is cleared when data is written into the transmitter data register. It is set by power-up sequence.
6	IE Interrupt enable read/write	A logic one enables transmitter interrupts. A logic zero disables interrupts. Cleared by initialization.
5-3	BR2-BR0 Programmable baud rate select read/write	When PBR-bit 1 in XCSR is set, these baud bits determine the baud rate (set by software if SOFT jumper connected to GND). If SOFT jumper is connected to OPEN, baud rate is obtained via extra wrap. Bits BR2-BR0 are cleared by PBR enable (SOFT Fx) or by power-up sequence.
2	MAINT Maintenance read/write	This bit facilitates a maintenance self-test. When the bit is set, the the (transmitter serial output) is connected to the receiver serial input; and the external serial input is disconnected. This bit is cleared by initialization.

* Read only as a zero when programmable baud rate inhibit (PBR) is asserted low. PBR is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J16). In this case, the baud rate is determined by the wrap-wrap jumpers (J7-J11). Otherwise, with SOFT EN to GND (J14-J12), the bit is read/write. This bit is cleared by power-up sequence or PBR (SOFT EN to OPEN jumper J14-J15).

Transmitter Status Register Bit Assignments (XC3S) (Cont)

Bit		Description
1	PBR* Programmable baud rate enable Read/write when software programmable baud rates enabled (SOFT EN to GND unassert); else read only as 0.	this bit switches between internal and external baud rate selection. When set (enable), the baud rate is determined by the PBR2-0 bits in this register. When clear (disable), the baud rate is determined by the J1, J0 wire-wrap pins. This bit is cleared by power-up sequence or SOFT EN to OPEN jumper connected (programmable baud rate inhibit (J14 to J15)).
0	BK Break read/write	When this bit is set, it causes the serial output signal to go to a space condition. A space condition longer than a character time causes a framing error when it is received and is regarded as a break. Cleared by bus initialization.

- * Read only as a zero when programmable baud rate inhibit (PBRi) is asserted low. PBRi is asserted low by connecting the SOFT EN to OPEN jumpers (J14 to J15). In this case, the baud rate is determined by the wire-wrap jumpers (J2-J11). Otherwise, with SOFT EN to GND (J14-J15), the bit is read/write. This bit is cleared by power-up sequence or PBRi (SOFT EN to OPEN jumper: J14-J15).

Transmitter Data Buffer Bit Assignments (XBUF)

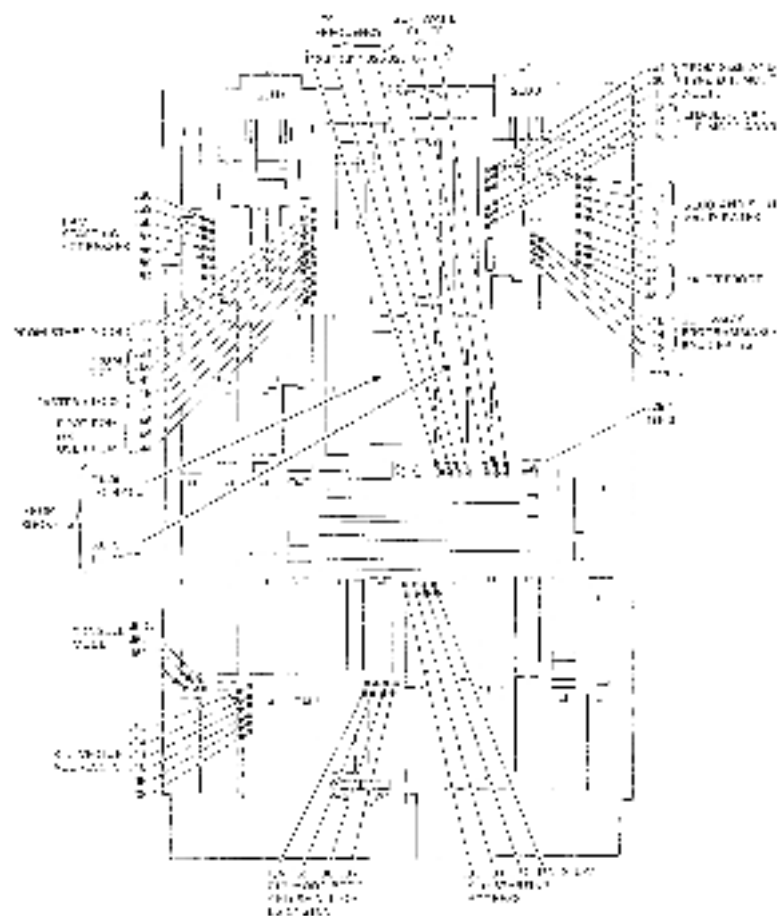
Bit	Description	
15-8	Unused	
7-0	XMIT DATA BUFFER residuals	Transmitter data buffer - this byte register holds a copy of the most recent byte written into it. When a byte is written into this register, the transmit ready (TR) bit in the XCSR register is cleared. This byte is copied into the transmitter serial output register whenever that register is empty and the bit is clear. The TR bit is set when a byte is copied from the transmitter data buffer into the serial output register. Flushing the contents of this register causes no other effect. Cleared by power up sequence.

Definition of Cables

Cable	Application	Length
BC21D-05	EIA RS-232D modem cable to interface with modems and acoustic couplers (2 × 5 pin AMP female to RS-232C male)	1.5 m (5 ft)
BC23N-05	EIA RS-232C null modem cable to directly interface with a local EIA RS-232C terminal (2 × 5 pin AMP female to RS-232C female)	1.5 m (5 ft)
BC29M-50	EIA RS-422 or RS-423 cable for high-speed transmission (15 × 0.01 in.) (2 × 5 pin AMP female to 2 × 5 AMP female)	15 m (50 ft)
BC05D-10	Extension cable used in conjunction with BC21B-05	3 m (10 ft)
BC05D-45	Extension cable used in conjunction with BC21B-05	7.6 m (25 ft)
BC03M-25	Null modem extension cable used in conjunction with BC21D-05	7.6 m (25 ft)

NOTE

Strapped logic levels are provided on data terminal ready (DTR) and request to send (RTS) to all operation of modems with manual provisions (such as Bell 103A data set with 804B auxiliary set).



MXV11-B Jumper Locations

Jumper Connections for MXV11-B Summary

Jumper	Name	Function	Connection*
J1	Connector for SLU0	SLU connectors	
J2	Connector for SLU1		
J3	RAI 1	Halt and reboot functions	POC (W3)
J4	GND		
J5	RR0001		
J6	OPEN		
J7	J10	Serial line unit baud rates	VW
J8	J16		
J9	GND		
J10	J06		
J11	J06		
J12	TP2	For engineering use	
J13	GND	Software programmable baud rates	POC (W4)
J14	SOFT EN		
J15	OPEN		
J16	GND	Enables or disables direct mode addressing	POC (W6)
J17	PC1/DIR H		
J18	OPEN		
J19	AL12H	PHOM size and type in direct mode addressing	POC (W5)
J20	NA12H		
J21	+5 V		
J22	LTC COMM	Line time clock frequency	VW
J23	50 Hz		
J24	60 Hz		
J25	800 Hz		
J26	OPEN	Software control of line time clock	POC (W7)
J27	LTC EN IN		
J28	LTC EN OUT		
J29	TP5	For engineering use	
J30	SLUA3	Serial line unit starting address	VW
J31	GND		
J32	SLUA2		
J33	SLUA1		

Jumper Connections for MXV11-B Summary (Cont)

Jumper Name		Function	Connection
J34	DIR MODE BOOT	Direct mode boot and small or large system	WW
J35	OPEN		
J36	GND		
J37	GM/LG		
J38	JL0	Serial line unit vector address	WW
J39	JL0		
J40	GND		
J41	JL1		
J42	JL2		
J43	JL3		
J44	BOOT L/PROM H	Boot ROM or user ROM	POC (W6)
J45	GND		
J46	OPEN		
J47	CLOCK IN	Master clock	POC (W10)
J48	CLOCK OUT		
J49	PROM 1	PROM size and PROM start address	WW
J50	PROM 2		
J51	GND		
J52	BSK1		
J53	BSK2		
J54	AJ13	RAM starting address	WW
J55	AJ14		
J56	AJ15		
J57	GND		
J58	AJ16		
J59	AJ17		
J60	AJ18		
J61	OPFR	Console mode	POC (W8)
J62	GND		
J63	CONSOLE		

*POC = Push-on connector

WW = Wire-wrap

NOTE

W1 and W2 are 0 ohm resistors associated with battery backup option. Either one may be inserted but not both. The module is shipped with W2 inserted.

Miscellaneous Jumper Configurations

Connector	Configuration	Description
J50 J52 J51	CONSOLE GND OPEN	GND to OPEN (J52 to J51)
J53 J52 J51	CONSOLE GND OPEN	CONSOLE to GND (J53 to J52)
J46 J45 J44	OPEN GND BOOT L/PROGRAM	BOOT L/PROGRAM to GND (J44 to J45)
J46 J45 J44	OPEN GND BOOT L/PROGRAM	Inserted when MXV11-B2 boot ROM set is installed in sockets XH18 and XH29. Enables the following registers to be addressed if the console GND to OPEN jumper (J52 to J51) is installed. Page control register Line time clock control Diagnostic display register
J46 J45 J44	OPEN GND BOOT L/PROGRAM	Inserted when ROMs are for user code (not bootstrap code). See Table A for addresses.
J37 J35 J35	SM/LG SYS GND OPEN	SM/LG SYS to GND (J37 to J35)
J37 J35 J35	SM/LG SYS GND OPEN	This is installed when the MXV11-B is connected in a Q2 bus backplane. Recognizes BDAL <2100> L. This jumper must be installed if RAM is addressed above 128K words.
J37 J35 J35	SM/LG SYS GND OPEN	Installed when the MXV11-B is connected to a 16- or 18-bit Q-BUS. Recognizes BDAL <1700> L only.
J36 J35 J34	GND OPEN DIRECT MODE BOOT	DIRECT MODE BOOT to OPEN (J34 to J35)
		Module not wired for direct mode boot

Miscellaneous Jumper Configurations (Cont.)

Connector	Connection	Description
J36 J35 J34	GND OPEN DIRECT MODE BOOT	DIR. MODE- BOOT to GND (J34 to J36)
J18 J17 J16	OPEN PG 1/DIR II GND	PG 1/DIR II to GND (J17 to J16)
J18 J17 J16	OPEN PG 1/DIR II GND	PG 1/DIR II to OPEN (J17 to J18)
J48 J47	CLOCK OUT CLOCK IN	CLOCK OUT to CLOCK IN (J46 to J47)
J3 J4 J5 J6	HALT GND /REBOOT OPEN	HALT to GND (J3 to J4)
J3 J4 J5 J6	HALT GND /REBOOT OPEN	HALT not con- nected to GND
J3 J4 J5 J6	HALT GND /REBOOT OPEN	REBOOT to GND

NOTE

HALT to GND (J3 to J4) and REBOOT to GND (J5 to J6) cannot be simultaneously jumpered.

Miscellaneous Jumper Configurations (Cont)

Connector		Connection	Description
J3	HAUT	GND to OPEN (J4 to J5)	Disables reboot function.
J4	GND		
J5	REBOOT		
J6	OPEN		
J26	OPEN	LTC EN IN to	Allows LTC to be software controlled. Enables control of BEVENT L on the bus via bit 06 of the LTC register. When bit 6 of LTC register is 0, BEVENT L will be asserted constantly low. This inhibits LTC interrupts. To address the LTC register (77548), the MXV11-B must be in boot mode (BOOT L/PRGM 1 to GND) (J44 to J45) and S/U1 must be the console port (CONSOLE to GND removed).
J27	LTC EN IN	LTC EN OUT	
J28	LTC EN OUT	(J27 to J28)	
J26	OPEN	LTC EN IN to OPEN (J27 to J28)	Prevents bit 06 of the LTC register from controlling the BEVENT L line.
J27	LTC EN IN		
J28	LTC EN OUT		
J29	LTC COMM	LTC COMM to 50 Hz (J22 to J23)	When installed, the BEVENT line is driven from a 50 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.
J23	50 Hz		
J24	50 Hz	LTC COMM to 60 Hz (J22 to J24)	When installed, the BEVENT line is driven from a 60 Hz crystal derived clock. If the line time clock jumper is installed, the clamp has to be turned off by the software for the clock to drive the BEVENT line.

CAUTION

LTC EN IN to LTC EN OUT (J27 to J28) should not be connected if the CPU has an LTC control register.

Miscellaneous Jumper Configurations (Cont)

Connector	Connection	Description
J25 800 Hz	J20 COMM to 800 Hz (J22 to J25)	When installed, the BEVENT line is driven from an 800 Hz crystal derived clock. If the line time clock jumper is installed, the stamp has to be turned off by the software for the clock to drive the BEVENT line.
J15 OPEN J14 SOFT EN J13 EN0	SOFT EN to GND (J14 to J13)	Enables software programmable baud rates for both SLU1 and SLU0 via the CSR. The baud rate jumpers in Table B have no effect if the PBRN bit is set.
J15 OPEN J14 SOFT EN J13 GND	SOFT EN to OPEN (J14 to J15)	Baud rates are selected from Table B.
W1	W1 (0 ohm resistor) connected	Battery backup. +5 V is supplied by user on backplane pin AV1. DIGITAL does not supply battery backup.
W2	W2 (0 ohm resistor) connected	No battery backup.
J21 +5 V J20 NA12H J19 BA12H	NA12H to +5 V (Normalized address 12) (J20 to J21) to (Buffered Address line 12)	Specifies 2K user UVROM's (2716) installed and direct mode addressing.
J21 +5 V J20 NA12H J19 BA12H	NA12H to BA12H (J20 to J19)	Specifies 4K or 8K user-supplied ROM in direct mode addressing.

NOTE

One of these jumpers (50, 60, or 800 Hz) should be installed: 1) if no external BEVENT source is provided in the system, and 2) if the user desires this source. Power supplies manufactured by DIGITAL normally supply BEVENT L to the backplane.

NOTE

There are cases where none of these jumpers (+5 V, NAAH, and AL12H) should be connected. In these cases, the push-on connector must be completely removed or must be connected to one of the outside pins to hold the connector. There is no open pin associated with these jumpers. For example, if 2K non UV PROMs or the MXV11-B2 ROM is to be installed, these jumpers are all disconnected.

Table A. Jumpers for PROM Starting Address

		BSK2 to GND (J53 to J51)	BSK1 to GND (J52 to J51)	User PROM Starting Address (octal) (bits)
J51	GND	R	R	000000*
J52	BSK1	R	I	020000
J53	BSK2	I	R	040000
	I	I	060000	

R = jumper removed

I = jumper inserted to ground

* Stopped configuration. Remove all jumpers from BSK1 (J52) and BSK2 (J53) if not in user mode.

NOTE

These addresses are for user supplied ROMs only. Jumpers BSK1 L/PROM H to GND (J44 to J46) and PG L/DIR H to GND (J17 to J18) must be removed.

Table B. Serial Line Unit Starting Address Jumpers

		SLUA3 to GND (J50 to J31)	SLUA2 to GND (J52 to J31)	SLU1 to GND (J33 to J31)	Starting Address SLUD	SLU1 (See Note)
J33	SLUA1	R	R	R	776500*	776510
J32	SLUA2	R	R	I	776510	776520
J31	GND	R	I	R	776520	776530
J30	SLUA3	R	I	I	776530	776540
		I	R	R	776540	776550
		I	R	I	776560	776560
		I	I	R	776560	776570
		I	I	I	776570	776580

R = jumper removed

I = jumper inserted to ground

*Shipped configuration

NOTE

If the GND to OPEN jumper (J52 to J61) is installed (console enabled), the SLU1 address is fixed at the standard console address of 777360 and this column does not apply.

Table C. Jumpers for SLU Vector Addresses

		J02 to GND (J39 to J40)	J01 to GND (J35 to J40)	JL2 to GND (J43 to J46)	JL2 to GND (J42 to J40)	JL1 to GND (J41 to J40)	SLU0	SLU1 (See Note)
J43	JL1	R	R	0	R	R	200*	310*
J42	JL2	R	R	0	R	I	210	320
J41	JL1	H	R	0	I	R	220	330
J40	GND	H	R	0	I	I	230	340
J39	J02	R	H	I	R	0	240	350
J38	J01	R	R	I	R	I	250	360
		R	R	I	I	R	260	370
		R	R	I	I	I	270	380
		R	I	0	R	H	300	410
		R	I	0	R	I	310	420
		R	I	0	I	R	320	430
		R	I	0	I	I	330	440
		R	I	I	R	R	340	450
		R	I	I	0	I	350	460
		R	I	I	I	R	360	470
		R	I	I	I	I	370	480
		I	R	R	R	R	400	510
		I	R	R	R	I	410	520
		I	R	R	I	H	420	530
		I	R	R	I	I	430	540
		I	R	I	R	R	440	550
		I	R	I	R	I	450	560
		I	R	I	I	0	460	570
		I	R	I	I	I	470	580
		I	I	R	H	R	500	610
		I	I	R	H	I	510	620
		I	I	R	I	R	520	630
		I	I	R	I	I	530	640
		I	I	I	0	R	540	650
		I	I	I	R	I	550	660
		I	I	I	I	R	560	670
		I	I	I	I	I	570	Undefined

I = jumper inserted from specified pin to ground. Where multiple connections are made, they are daisy-chained.

R = jumper removed

*Shipped configuration

NOTE

If the GND to OPEN jumper (J02 to J01) is installed (console enabled) SLU1 vector address is fixed at 60 and this column does not apply.

PROM Jumpers

		NA12H to BA12H (J20 to J21)	WA12H to +5 V (J20 to J21)	Description
J19	BA12H	R	P	Page mode – Boot ROM for 2K by 8 non-UV PROMs, 4K by 8 or 8K by 8 PROMs Direct mode – for 2K by 8, non-UV PROMs, 4k by 8, or 8K by 8 PROMs* Direct mode – for 2K by 8 UV PROMs
J20	NA12H	I	R	
J21	+5 V	R	I	

R – jumper removed

I – jumper inserted

*Shipped configuration

Jumpers to Configure PROM Size

		PROM 2 to GND (J50 to J51)	PROM 1 to GND (J49 to J51)	PROM Size
J51	GND	R	R	No PROMs†
J50	PROM 2	R	I	2K by 8
J49	PROM 1	I	R	4K by 8
			I	8K by 8†

R – jumper removed

I – jumper inserted

† Shipped configuration. Additional jumpers are required depending on user mode/buck mode and direct addressing page addressing. Refer to the last three tables in this section.

† If the MXV11-E2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND jumper (J50 to J49 to J51).

RAM Starting Address Jumpers

			AJ18 to GND (J58 to J57)	AJ17 to GND (J58 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J58 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
J50	AJ18	00	R	R	R	R	R	R	0"
J59	AJ17	01	R	R	R	R	R	I	4K
J58	AJ16	02	R	R	R	R	I	R	8K
J57	GND	03	R	R	R	R	I	I	12K
J56	AJ15	04	R	R	R	I	R	R	16K
J55	AJ14	05	R	R	R	I	R	I	20K
J54	AJ13	06	R	R	R	I	I	R	24K
		07	R	R	R	I	I	I	28K
		10	R	R	I	R	R	R	32K
		11	R	R	I	R	R	I	36K
		12	R	R	I	R	I	R	40K
		13	R	R	I	R	I	I	44K
		14	R	R	I	I	R	R	48K
		15	R	R	I	I	R	I	52K
		16	R	R	I	I	I	R	56K
		17	R	R	I	I	I	I	60K
		20	R	I	R	R	R	R	64K
		21	R	I	R	R	R	I	68K+
		22	R	I	R	R	I	R	72K+
		23	R	I	R	R	I	I	76K+
		24	R	I	R	I	R	R	80K+
		25	R	I	R	I	R	I	84K+
		26	R	I	R	I	I	R	88K+
		27	R	I	R	I	I	I	92K+
		30	R	I	I	R	R	R	96K+
		31	R	I	I	R	R	I	100K+
		32	R	I	I	R	I	R	104K+
		33	R	I	I	R	I	I	108K+
		34	R	I	I	I	R	R	112K+
		35	R	I	I	I	R	I	116K+
		36	R	I	I	I	I	R	120K+
		37	R	I	I	I	I	I	124K+
		40	I	R	R	R	R	R	128K+
		41	I	R	R	R	R	I	132K+
		42	I	R	R	R	I	R	136K+
		43	I	R	R	R	I	I	140K+
		44	I	R	R	I	R	R	144K+
		45	I	R	R	I	R	I	148K+
		46	I	R	R	I	I	R	152K+
		47	I	R	R	I	I	I	156K+

RAM Starting Address Jumpers (Cont)

	AJ18 to GND (J56 to J57)	AJ17 to GND (J58 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
50	I	R	I	R	R	I	160K†
51	I	R	I	R	R	I	164K†
52	I	I	I	R	I	R	185K†
53	I	I	I	R	I	I	172K†
54	I	I	I	I	R	R	176K†
55	I	R	I	I	R	I	160K†
56	I	R	I	I	I	R	184K†
57	I	R	I	I	I	I	168K†
60	I	I	R	R	R	R	192K†
61	I	I	R	R	R	I	196K†
62	I	I	R	R	I	R	200K†
63	I	I	R	R	I	I	204K†
64	I	I	R	I	R	I	208K†
65	I	I	I	I	R	I	212K†
66	I	I	R	I	I	R	216K†
67	I	I	R	I	I	I	220K†
70	I	I	I	R	I	R	224K†
71	I	I	I	R	R	I	228K†
72	I	I	I	I	I	R	232K†
73	I	I	I	R	I	I	236K†
74	I	I	I	I	R	R	240K†
75	I	I	I	I	R	I	244K†
76	I	I	I	I	I	R	248K†
77	I	I	I	I	I	I	252K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.

R = jumper removed

* Shipped configuration

† To use address above 64K words, SM/LC SYS TO GND jumper (J37 to J36) must be installed

NOTE

Be careful when configuring the MXV11-D RAM when ROM is used in the USER ROM address space. USER ROM address space is defined as bus addresses 0–16K, (00000–100000) on 4K boundaries. The RAM start address must be higher than the last location of the ROM or dual responses from both the RAM and ROM will occur. The chart below shows several examples of right and wrong ways of assigning RAM memory start addresses.

ROM Size	ROM Start	RAM Start	RAM End	Comments
8K	3K	4K	68K	Wrong, 4K overlap (4K–8K)
8K	4K	0K	64K	Wrong, 8K overlap (4K–12K)
4K	0K	4K	68K	Right, no overlap
4K	0K	12K	76K	Right, no overlap
8K	4K	12K	76K	Right

‡ Address space gap usually not recommended but up to user to decide depending on application.

Jumpers: Connections for PROM Sizes in User Mode

Jumpers	No PROMs	2K by 8	4K by 8	8K by 8
J16 (GND)	J17 to J18	J17 to J18	J17 to J18	J17 to J18
J17 (PG1/MP H)				
J18 (OPEN)				
J19 (HA12H)	J19 to J20	J20 to J21	J19 to J20	J19 to J20
J20 (RA12H)				
J21 (15 V)				
J44 (DOOT L/PROM H)	J45 to J46	J45 to J46	J45 to J46	J45 to J46
J45 (GND)				
J46 (OPEN)				
J49 (PROM1)	—	J49 to J51	J50 to J51	J49 to J50 to J51
J50 (PROM2)				
J51 (GND)				

NOTE

Jumpers connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J45 is connected to J46, and J49 is connected to J51.

Jumper Connections for PROM Sizes in Boot Mode (Page Addressing)

Jumpers	No. PROMs	2K by 8*	4K by 8	8K by 8
J16 (GND) J17 (PROM I/O) J18 (OPEN)	J17 to J18	J16 to J17	J18 to J17	J16 to J17
J19 (DA12H) J20 (RA12H) J21 (+5 V)	J19 to J20	-	J19 to J20	J19 to J20
J43 (BOOT L/PROM I/O) J44 (GND) J45 (OPEN)	J43 to J44	J44 to J45	J44 to J45	J44 to J45
J49 (PROM1) J50 (PROM2) J51 (GND)		J49 to J51	J50 to J51	J49 to J50 to J51

*2K by 8 UV PROM cannot be used in page mode.

NOTE

Jumper connections are indicated. For example, in the 8K by 8 PROM, J16 is connected to J17. J19 is connected to J20, J44 is connected to J45 and J49. J50 and J51 are connected.

Jumper Connections for PROM Sizes in Boot Mode (Direct Addressing)

Jumpers	No PROMs	2K by 8	4K by 8	6K by 8
J16 (GND) J17 (PG L/DIR H) J18 (OPEN)	J17 to J18	J17 to J18	J17 to J18	J17 to J18
J19 (BA12H) J20 (BA12H) J21 (H5 VI)	J19 to J20	J20 to J21	J19 to J20	J19 to J20
J44 (BOOT L/PROM H) J45 (GND) J46 (OPEN)	J45 to J46	J44 to J45	J44 to J45	J44 to J45
J49 (PROM1) J50 (PROM2) J51 (GND)	—	J49 to J51	J50 to J51	J49 to J50 to J51
J34 (DIR. MODE BOOT) J35 (OPEN) J36 (GND)		J34 to J35	J34 to J35	J34 to J35

NOTE

Jumper connections are indicated. For example, in the 2K by 8 PROM, J17 is connected to J18, J20 is connected to J21, J44 is connected to J45, J49 is connected to J51, and J34 is connected to J35.

RKV11-D BUS INTERFACE FOR RKV11-D DISK DRIVE CONTROLLER

Arms	Bus Loads		Cables
→ 5 18 max	12 0	AC 100% 1	(2) 8009L 1 M893 YA

Standard Address

RKDS	(Drive Status)	177400
RKER	(Error)	177402
RKCS	(Control/Status)	177404
RKWC	(Word Count)	177406
RKHA	(Data Address)	177410
RKDA	(Disk Address)	177412
RKDB	(Data Buffer)	177416

Vector

720

Diagnostic Programs

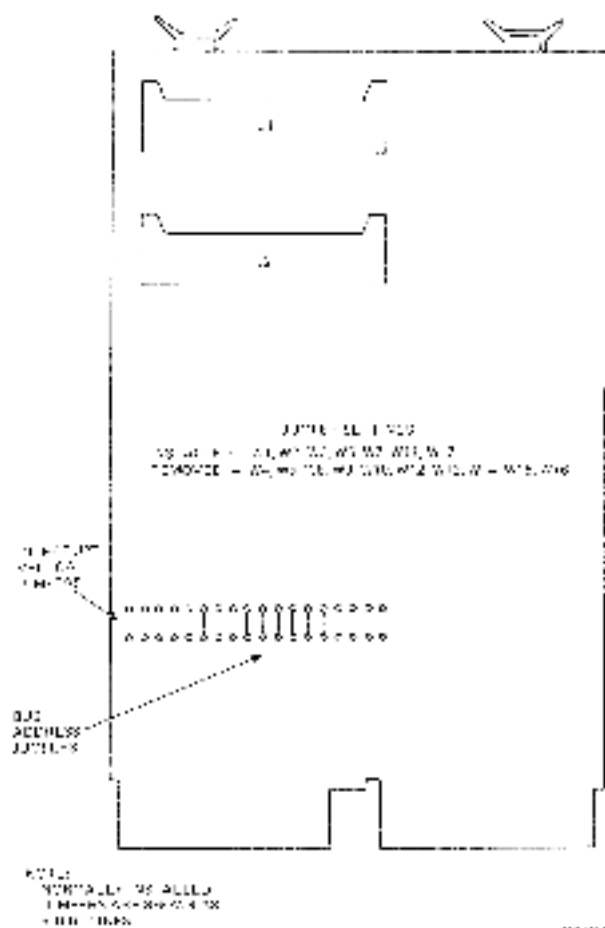
Refer to Appendix A

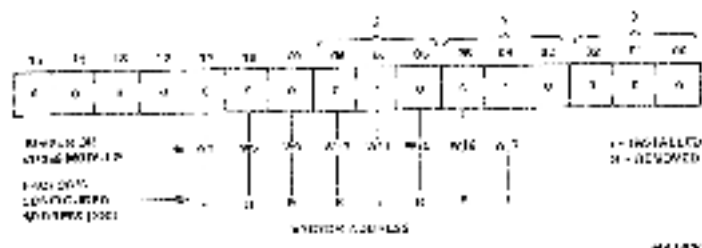
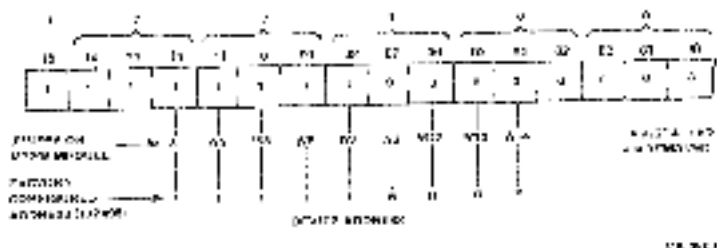
NOTE

The logic test programs should be run first, then the dynamic test, and finally the performance exerciser.

Related Documentation

RKV11-D Disk Drive Controller User's Manual (EK-RKV11-UP-001)
RKV11-D Disk Drive Controller Technical Manual (EK-RKV11-TM-001)
 Field Maintenance Print Set (MP00220)
RKDS/RKDSJ/RKDSF Disk Drive Maintenance Manual (EK-RKDSJF-MV-001)
RKDS/RKDSJ Disk Drive Preventive Maintenance Manual
 (EK-RKDSJ-PM-001)
RKDSF DEC Disk Drive Preventive Maintenance Procedure
 (ED-RKDSF-PM-001)
Microcomputer Interfaces Handbook (EB-30175-20)



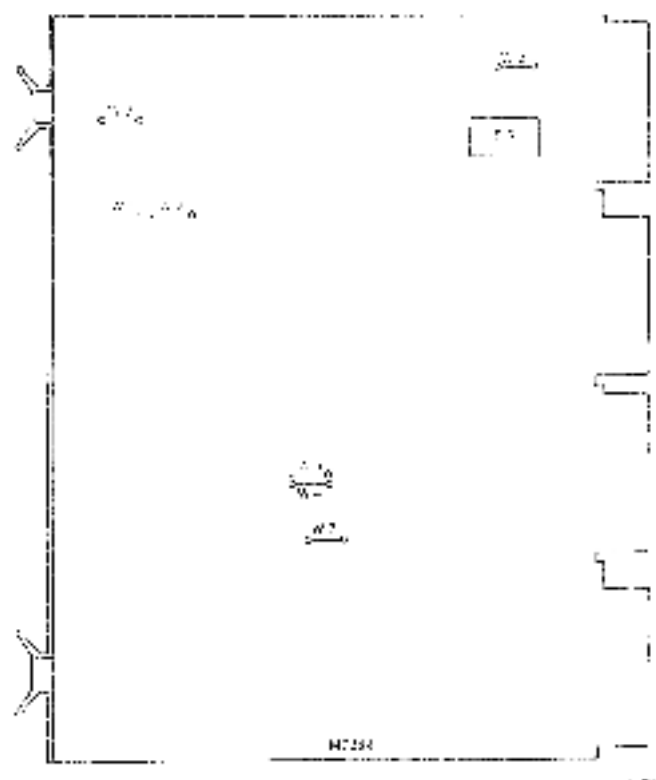


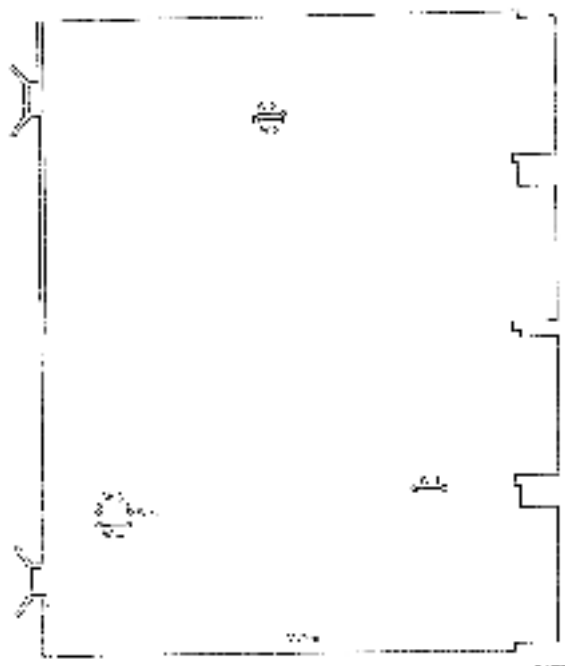
Jumpers on the three RKV11-D modules are identical to those in the standard RKV11-D configuration. A breakdown is given below for reference. There are no jumpers on M7268.

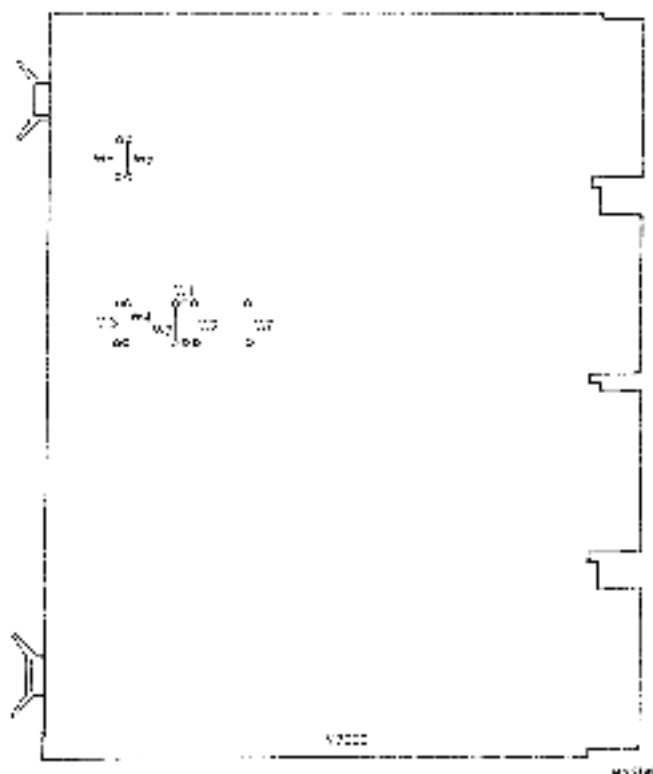
Module	Installed	Removed
M7264*	W1, W4, W6, W7	W2, W3, W5
M7265**	W1, W2, W6	W3, W4, W5
M7266	W2, W5, W7	W1, W3, W4, W6, W8

* Interrupt priority jumper (EP4-7) in socket F8 is not required since the RKV11-D was designed for single-line interrupt scheme only.

** 2.58 MHz crystal used DEC PN 16-10054-0.









RKV11-D Module Utilization

00000000

Drive Status Register (RDS)

Address = 77400

NOTE

This register is a read-only register, and contains the selected drive status and current sector address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECTOR ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SECTOR ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

00000000

Bit Definitions

Bit	Function
00-03	Sector Counter (SC) - These four bits are the current sector address of the selected drive. Sector address 00 is defined as the sector following the sector that contains the Index pulse.
04	Sector Counter Equals Sector Address (SC = SA) - Indicates that the disk heads are positioned over the disk address currently held in the sector address register.
05	Write-Protect Status (WPS) - Sets when the selected disk is in the write-protected mode.
06	Read/Write/Seek Ready (R/W/S RDY) - Indicates that the selected drive head mechanism is not in motion, and that the drive is ready to accept a new function.
07	Drive Ready (DRY) - Indicates that the selected disk drive complies with the following conditions.

Bit Definitions (Cont)

Bit	Function
	1. The drive is properly supplied with power. 2. The drive is loaded with a disk cartridge. 3. The disk drive door is closed. 4. The LOAD/RUN switch is set to RUN. 5. The disk is rotating at a proper speed. 6. The heads are properly loaded. 7. The disk is not in a DRU (DRU or RKDS) condition.
08	Sector Counter OK (SOK) - Indicates that the sector counter operating on the selected drive is not in the process of changing, and is ready for examination. If this bit is not set, the sector counter is not ready for examination, and a second attempt should be made.
09	Seek Incomplete (SIN) - Indicates that, due to some unusual condition, the seek function cannot be completed. Can be accompanied by RKER 16 (drive error). Cleared by a drive reset function.
10	Drive Unusable (DRU) - Indicates that an unusual condition has occurred in the disk drive, and it is unable to properly perform any operations. Reset by setting the RUN/LOAD switch to LOAD. If, when the switch is returned to RUN, the condition remains, an inoperative drive can be assumed, and corrective maintenance procedures should begin. Can be accompanied by RKER 16 (drive error).
11	RKDS Disk on Line (RKDS) - Always set to identify the selected disk drive as RKDS.
12	Drive Power Low (DPL) - Sets when an attempt is made to initiate a new function, or if a function is actively in process when the control senses a loss of power to one of the disk drives. Can be accompanied by RKER 16 (drive error). Reset by a BUS-INIT or a control reset function.
18-19	Ident Location of Drive (ID) - If an interrupt occurs as the result of a hardware polling operation, these bits will contain the binary representation of the logical drive number that caused the interrupt.

RKV11-D/M7269

Error Register (RKER)

Address = 177402

NOTE

This is a read-only register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	00
WCE	CSE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE	WCE

Bit Definitions

Bit	Function
00	Write Check Error (WCE) - Indicates that an error was encountered during a write check function as a result of a faulty bit comparison between disk data and memory data. Clears upon the initiation of a new function. This is a soft error condition.
01	Checksum Error (CSE) - Sets while performing a read function as a result of a faulty recalculation of the checksum. Cleared upon the initiation of any new function. This is a soft error condition.
02-04	Unused.

The remaining bits of the RKER are all hard errors, and are cleared only by a BUS INIT or a control reset function.

Bit Definitions

Bit	Function
05	Nonexistent Sector (NXS) - Indicates that an attempt was made to a sector address greater than 127.
06	Nonexistent Cylinder (NXC) - Indicates that an attempt was made to initiate a transfer to a cylinder address greater than 8127.
07	Nonexistent Disk (NXD) - Indicates that an attempt was made to initiate a function on a nonexistent drive.
08	Timing Error (TE) - Indicates that a loss of timing pulses for at least 5 μ s has been detected.

Bit Definitions (Cont.)

Bit	Function
09	Data Late (DLT) - Sets during a write or write check function when the multibuffer file is empty and the operation is not yet complete. Sets during a read function when the multibuffer file is filled and the operation is not yet complete.
10	Nonexistent Memory (NXM) - Sets if memory does not respond with a RPLY within 20 μ s of the time when the RKV11-D becomes bus master during a DMA sequence. Because of the speed of the RK05 disk drive, it is possible that NXM will be accompanied by RKER 09 (data late).
11	Programming Error (PGE) - Indicates that RKCB 10 (format) was set while initiating a function other than read or write.
12	Seek Error (SEE) - Sets if the disk head mechanism is not properly positioned while executing a normal read, write, read check, or write check function. The control checks 16 times before flagging this error. A simple jumper change will force the control to check just once.
13	Write Lockout Violation (WLO) - Sets if an attempt is made to write on a disk that is currently write protected.
14	Overrun (OVR) - Indicates that during a read, write, read check, or write check function, operations on sector 13 ₆ , surface 1 of cylinder address 512 ₆ were finished, and the RKWC has not yet overflowed. This is essentially an attempt to overflow out of a disk drive.
15	Drive Error (DRE) - Sets if a function is either initiated or in process, and a. one of the drives in the system senses a loss of either ac or dc power; or b. the selected drive is not ready, or is in some error condition.

RKV11-D/M7269

Control Status Register (RKCS)

Address 177404



Bit Definitions

Bit	Function																																						
GO	Go - This bit can be loaded by the operator and causes the control to carry out the function contained in bits 01-08 of the RKCS (function bits). Remains set until the control actually begins to respond to go, which may take from 1 us to 3.3 ms, depending on the current operation of the selected disk drive (to protect the format structure of the sector). Write only.																																						
01-08	Function - The function register or function bits, are loaded with the binary representation of the function to be performed by the control when a GO command is initiated. These bits are loaded by the program and cleared by BUS INIT. Read/Write. The binary codings are as follows.																																						
<table border="1"> <thead> <tr> <th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Operation</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>Control Reset</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>Write</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>Read</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>Write Check</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>Seek</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>Read Check</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>Drive Reset</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>Write Lock</td></tr> </tbody> </table>	Bit 3	Bit 2	Bit 1	Operation	0	0	0	Control Reset	0	0	1	Write	0	1	0	Read	0	1	1	Write Check	1	0	0	Seek	1	0	1	Read Check	1	1	0	Drive Reset	1	1	1	Write Lock			
Bit 3	Bit 2	Bit 1	Operation																																				
0	0	0	Control Reset																																				
0	0	1	Write																																				
0	1	0	Read																																				
0	1	1	Write Check																																				
1	0	0	Seek																																				
1	0	1	Read Check																																				
1	1	0	Drive Reset																																				
1	1	1	Write Lock																																				
09-23	Unused - The RKV11-D uses these bits. Since the PDP-11/05 bus structure has no provision for extended addressing, no connection is made to the bus from these bits on the RKV11-D. They will respond as two unused read/write bits in the status register but, like the RKV11-D they, will increment should the RKCS overflow.																																						

Bit Definitions (Cont)

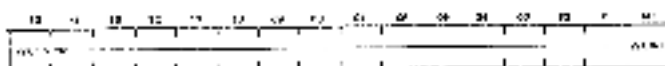
Bit	Function
06	Interrupt on Done Enable (IDE) - When set, causes the control to issue a bus request and interrupt to vector address 0000H if: a. a function has completed correctly b. a hard error is encountered c. a soft error is encountered and bit 08 of the RKCS (SSE) is set d. RKCS 07 (RDY) is set and go is not set Read/write.
07	Control Ready (RDY) - Indicates that the control is ready to perform a function. Set by INIT, a hard error condition, or by the termination of a function. Cleared by go being set. Read only.
08	Stop on Soft Error (SSE) - If a soft error is encountered when this bit is set: a. all control action will stop at the end of the current sector if RKCS 06 (IDE) is reset, or b. all control action will stop and a bus request will occur at the end of the current sector if RKCS 06 (IDE) is set Read/write.
09	Unused
10	Format (FMT) - FMT is under program control and must be used only in conjunction with normal read and write functions. Used to format a new disk pack or to reformat any sector erased due to control or drive failure. Alters the normal write operation, under which the header is rewritten each time the associated sector is rewritten, in that the head position is not checked for proper positioning before the write. Alters the normal read operation in that only one word, the header word, is transferred to memory per sector. For example, a three-word read function in format mode will transfer header words from three consecutive sectors to three consecutive memory locations for software checking. Read/write.
11	Int bit increment to the RKBA (IBA) - Inhibits the RKBA from incrementing during a normal transfer function. This allows data transfers to occur to or from the same memory location throughout the entire transfer operation. Read/write.
12	Unused

Bit Definitions (Cont)

Bit	Function
13	Search Complete (SCP) - Indicates that the previous interrupt was the result of some seek or drive reset function. Cleared at the initiation of any new function. Read only.
14	Hard Error (HE) - Sets when any of RKER 05-15 are set. Stops all control action, and processor reaction is dictated by RKCS 06 (IDE), until cleared, along with RKER 05-15, by INIT or a control reset function. Read only.
15	Error (ERR) - Sets when any bit of the RKER sets. Processor reaction is dictated by RKCS 06 and RKCS 08 (IDE and SSP). Cleared if all bits in the RKER are cleared. Read only.

Word Count Register (RKWC)

Address = 177406

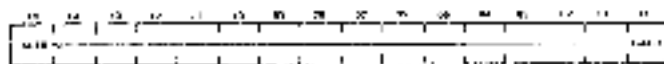


Bit Definition

Bit	Function
00-15	WCOO-WC15 - The bits in this register contain the 2's complement of words to be affected or transferred by a given function. The register increments by 1 after each word transfer. When the register overflows (all WC bits go to 0), the transfer is complete and RKV11-D operation is terminated at the end of the present disk sector. However, only the number of words specified in the RKWC are transferred. Read/write.

Current Bus Address Register (RKBA)

Address = 177410

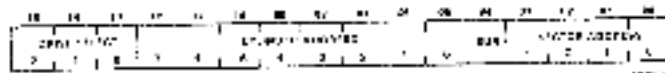


Bit Definition

Bit	Function
00-15	BA00-BA15 - The bits in this register contain the bus address to or from which data will be transferred. The register is incremented by two at the end of each transfer. Read/write.

Disk Address Register (RKDA)

Address - 177412



NOTE

This register will not respond to commands while the controller is busy. Therefore, RKDA bits are loaded from the bus data lines only in the control ready (RDY - bit 07 of the RKCS) state, and are cleared by BUS INIT and control reset. The RKDA is incremented automatically at the end of each disk sector.

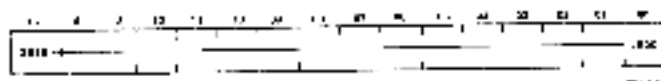
Bit Definitions

Bit	Function
00-03	Sector Address (SA) - Binary representation of the disk sector to be addressed for the next function. The largest valid address (or number) for the sector address is 12 ₈ .
04	Surface (SUR) - When set, enables the lower disk head so that operation is performed on the lower surface; when reset, enables the upper disk head.
05-12	Cylinder Address (CYL ADDR) - Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 212.
13-15	Drive Select (DR SEL) - Binary representation of the logical drive number currently being selected.

RKV11-D/M7269

Data Buffer Register (RKDB)

Address = 177416

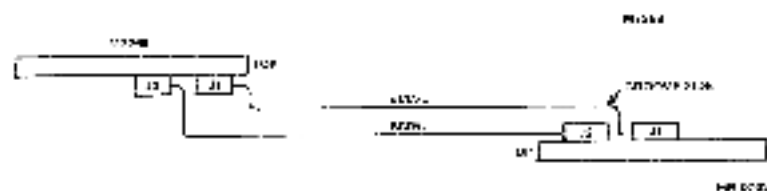
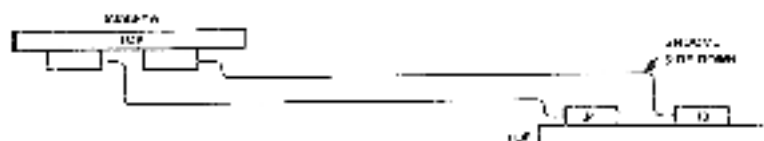
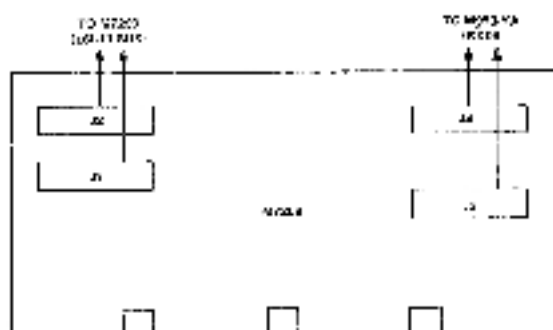


Bit Definition

Bit	Function
00-15	DB00-DB15 The bits of this register work as a general data handler in that all information transferred between the control and the disk drive must pass through this register. Loaded from the bus only while the RKV11-D is bus master during a DMA sequence. Read only.

NOTE

Address 177414 is unused.



RKV11-D Cable Connection

RLV11 CONTROLLER MODULES

Amps		Bus Loads		Cables
4.5	1.12	AC	DC	HGCR-XX
5.5	1.0	8.2	1	70-12122 (1 per drive)
Transition Bracket Assembly				70-12415-00
Terministor				70-12293-00

Standard Addresses

CSR	174400	Control Status Register
HAR	174402	Hardware Address Register
DAR	174404	Device Address Register
MPR	174408	Master Program Register

Standard Vectors

160

Diagnostic Programs

Refer to Appendix A.

70-12415-00 Transition Bracket Assembly

70-12293-00

70-12122

70-12415-00

70-12293-00

70-12122

70-12415-00

70-12293-00

70-12122

70-12415-00

70-12293-00

70-12122

70-12415-00

70-12293-00

70-12122

70-12415-00

70-12293-00

RLV11/M8013,4



Address Selection



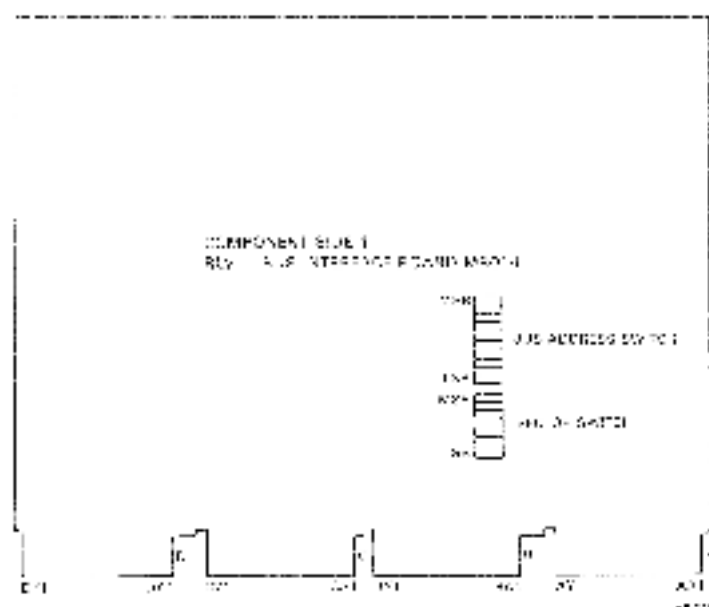
Vector Selection

Related Documentation

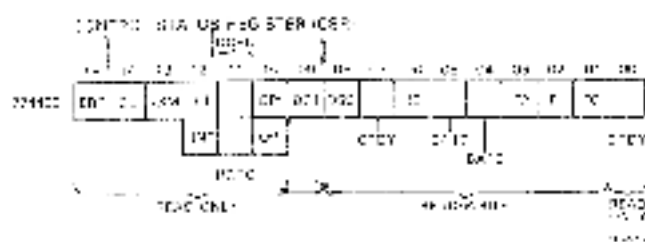
- RLV11 Controller Technical Description Manual* (EK-RLV11-TD)
- RLV11 Field Maintenance Print Set* (MP00636)
- RL01 Field Maintenance Print Set* (MP00347)
- RL02 Field Maintenance Print Set* (MP00553)
- RL01 Disk Drive IPB* (EK-ORL01-IP)
- RL02 Disk Drive IPB* (EK-ORL02-IP)
- RL01/RL02 User's Guide* (EK-RL012-UG)
- RL01/RL02 Pocket Service Guide* (EK-RL012-PG)
- Microcomputer Interfaces Handbook* (EE-20175-20)

NOTE

The M8013 must be installed above the M8014. The RLV11 controllers can only be used in a backplane built as an H9273 (slots A and B — LSI bus and slots C and D — interboard bus). The SA11-N box currently is the only box that contains an H9273 backplane.



RLV11 Bus interface Module (M8014)



Control Status Register

CSR Bit Definitions

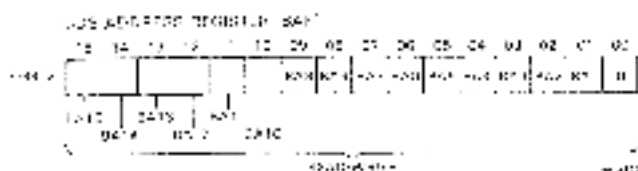
Bit	Function																																													
0	Drive Ready (RDY) - When set, this bit indicates that the selected drive is ready to receive a command (no seek operation in progress). The bit is cleared when a seek operation is initiated and set when the seek operation is completed.																																													
1-3	Function Code - These bits are set by software to indicate the command to be executed.																																													
	<table border="1"> <thead> <tr> <th>F2</th><th>F1</th><th>F0</th><th>Command</th><th>Octal Code</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>MAINTENANCE MODE</td><td>0</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>WRITE CHECK</td><td>1</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>GET STATUS</td><td>2</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>SEEK</td><td>3</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>READ HEADER</td><td>4</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>WRITE DATA</td><td>5</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>READ DATA</td><td>6</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>READ DATA WITHOUT HEADER CHECK</td><td>7</td></tr> </tbody> </table>	F2	F1	F0	Command	Octal Code	0	0	0	MAINTENANCE MODE	0	0	0	1	WRITE CHECK	1	0	1	0	GET STATUS	2	0	1	1	SEEK	3	1	0	0	READ HEADER	4	1	0	1	WRITE DATA	5	1	1	0	READ DATA	6	1	1	1	READ DATA WITHOUT HEADER CHECK	7
F2	F1	F0	Command	Octal Code																																										
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1	1	1	READ DATA WITHOUT HEADER CHECK	7																																										
	Command execution starts when RDY (bit 7) or the CSR is cleared by software. In a sense, bit 7 can be considered a negative go bit.																																													
4-5	Bus Address Extension Bits (BA16, BA17) - Two most significant bus address bits. Read and written as bits 4 and 5 of the CSR; they function as address bits 16 and 17 of the BAR.																																													
6	Interrupt Enable (IE) - When this bit is set by software, the controller is allowed to interrupt the processor at the assertion of RDY. This occurs at the normal or error termination of a command. Once an interrupt request is posted on the LSI bus, it is not removed until serviced even if IE is cleared.																																													

CSR Bit Definitions (Cont)

Bit	Function
7	Controller Ready (CRDY) - When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. Software cannot set this bit because no registers are accessible while CRDY is 0. When set, this bit indicates that the controller is ready to accept another command.
8-9	Drive Select (DS0, DS1) - These bits determine which drive will communicate with the controller via the drive bus.
10	Operation Incomplete (OPI) - When set, this bit indicates that the current command was not completed within the OPI timer period.
11	Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE) - If OPI (bit 10) is cleared and bit 11 is set, the CRC error occurred on the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error occurred on the header (HCRC). If OPI (bit 10) is cleared and bit 11 is set and the function command was a write check, a write check error (WCE) has occurred.
NOTE Cyclic redundancy checking is done only on the desired header. It is performed on the first and second header words, even though the second header word is always 0.	
12	Data Late (DLT) or Header Not Found (HNF Error) - When OPI (bit 10) is cleared and bit 12 is set, it indicates that a data late condition occurred on a read without header check operation. One of two conditions exists: Write Operation - The silo is empty, but the word count has not reached zero (bus request was ignored too long.) Read Operation - The silo is full (word being read could not enter the silo and the bus request was ignored too long.) When OPI (bit 10) is set and bit 12 is also set, it indicates that a timeout occurred while the controller was searching for the correct sector to read or write (no header; compare [HNF]).

CSR Bit Definitions (Cont.)

Bit	Function			
Error Summary				
Error	Bit 12	Bit 11	Bit 10	Comments
OPI	0	0	1	200 ms timeout
DCRC	0	1	0	
WCE	0	1	1	Function command is a write check.
RCRC	0	1	1	
DLT	1	0	0	
RNF	1	0	1	
13	Nonexistent Memory (NEM) - When set, this bit indicates that during a DMA data transfer, the memory location addressed did not respond within 14 ms.			
14	Drive Error (DE) - This bit is buffered from the drive error interface and, when set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a GET STATUS command. To clear the drive error bit, execute a GET STATUS command with bit 3 of the CARR.			
15	Composite Error (ERR) - When set, this bit indicates that one or more of the error bits (bits 10–14) is set. When an error occurs, the current operation terminates and an interrupt routine is initiated if the interrupt enable bit (bit 6 of the CSR) is set.			



Bus Address Register

BAR Bit Definitions

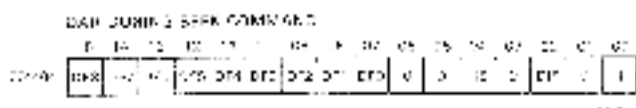
The Bus Address Register (BAR) is a 16-bit word-addressable register with an address of 774 402. Bits 0 through 15 can be read or written; bit 0 should normally be written 0. Expansion bits 16 and 17 are programmed via bits 4 and 5 of the CSR.

The bus address register indicates the memory location involved in the DMA data transfer during a read or write operation. The contents of the BAR are automatically incremented by 2 as each word is transferred between system memory and controller in either direction. Clear the BAR by executing a BUS INIT.

Disk Address Register (DAR)

The Disk Address Register (DAR) is a 16-bit read/write word-addressable register with an address of 774 40h. Its contents can have one of three meanings, depending on the function being performed. Clear this register by executing a BUS INIT.

DAR During a SEEK Command – To perform a seek function, it is necessary to provide address difference, head select, and head directional information to the selected drive.

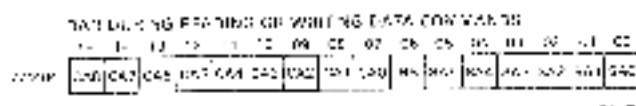


DAR SEEK Command

Bit Definitions

Bits	Function
0	Marker (MRK) – Must be a 1
1	Must be a 0, indicating to the drive that a SEEK command is being requested and that the remaining bits in the register will contain the seek specifications.
2	Direction (DIR) – This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (Bits 7–14).
3	Must be a 0
4	Head Select (HS) – Indicates which head (disk surfaces) is to be selected. Set = lower; clear = upper.
5–6	Reserved
7–14	Cylinder Address Difference (DF<0,0>) – Indicates the number of cylinders the heads are to move on a seek
15	Must be a 0

DAR During READ or WRITE DATA Command – For a read, write, or write check operation, the DAR is loaded with the address of the first sector to be transferred. Thereafter, as each adjoining sector is transferred, the DAR is automatically incremented by 1. If the DAR increments to the nonexistent sector address 505, an OPI timeout will occur. The drive must then seek to a new track if the transfer is to continue.

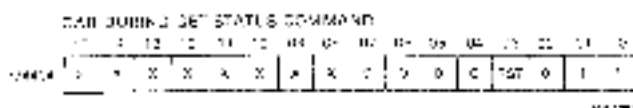


DAR READ/WRITE DATA Command

Bit Definitions

Bit	Function
0-5	Sector Address (SA<5:0>) – Address of one of the 40 sectors on a track. (Total range is 0 to 47.)
6	Head Select (HS) – Indicates which read (disk surface) is to be selected. Set = lower; clear = upper.
7-14	Cylinder Address (CA<7:0>) – Address of one of the 256 cylinders. (Total range is 0 to 255.)
15	Must be a 0.

DAR During a GET STATUS Command – After the GET STATUS command is deposited in the CSR, it is the DAR's responsibility to get the command transferred to the drive. Therefore, the DAR must also be programmed along with the CSR to do the GET STATUS command.



DAR GET STATUS Command

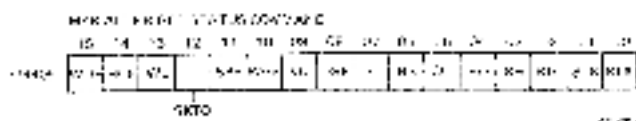
For a GET STATUS command, the DAR register bits must be programmed as follows.

DAR Register Bits for a GET STATUS Command

Bit	Function
0	Marker (MRKR) – Must be a 1.
1	Get Status (GS) – Must be a 1, indicating to the drive that its status word is being requested. At the completion of the GET STATUS command, the drive status word is read into the controller multipurpose (MP) register (output stage of FIFO). With this bit set, bits 8–15 are ignored by the drive.
2	Must be a 0.
3	Reset (RST) – When this bit is set, the drive clears its error register of soft errors before sending a status word to the controller.
4–7	Must be a 0.
8–15	Not used.

Multipurpose Register (MPR)

The MPR is two registers bearing the same base address. When writing into that location, the word counter accepts the data. When reading from that location, the FIFO output buffer provides the data.



MPR Status Word

MPR After a GET STATUS Command – When a GET STATUS command is executed and a status word is returned to the controller, the contents of the MPR (FIFO output stage) are defined as follows.

Bits C-2 - State < C:A> (ST<C:A>) - These bits define the state of the drive.

Bit			Definition
C	B	A	
0	0	0	Load Cartridge
0	0	1	Spin Up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek Track Counting
1	0	1	Seek Linear Mode (Lock On)
1	1	0	Unload Heads
1	1	1	Spin Down

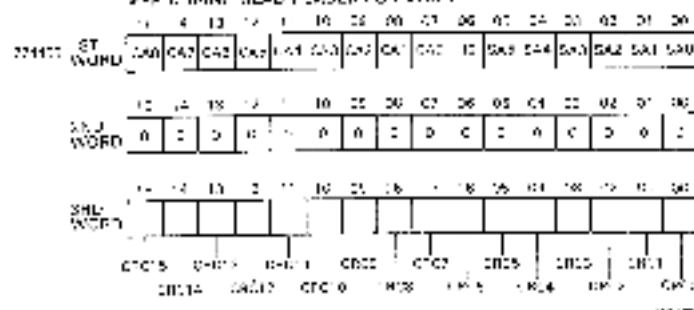
Bit Definitions

Bit	Function
0	Brush Home (BH) - Asserted when the brushes are not over the disk.
4	Heads Out (HO) - Asserted when the heads are over the disk.
5	Cover Open (CO) - Asserted when the cover is open or the dust cover is not in place.
6	Head Select (HS) - Indicates the currently selected head.
7	Drive Type (DT) - Set = lower; clear = upper. Set = RL02; clear = RL01.
8	Drive Select Error (DSE) - Indicates that multiple drive selection was detected.
9	Volume Check (VC) - VC is set every time the drive goes into load heads state. This asserts a drive error at the controller but not on the front panel. VC is an indication that the program does not really know which disk is present until it has read the serial number and had sector file. (The disk might have been changed while the heads were unloaded.)
10	Write Gate Error (WGE) - Indicates that the drive sensed that write gate was asserted when sector passed was asserted, or write gate was set with the drive not ready, or the drive was write locked.

Bit Definitions (Cont)

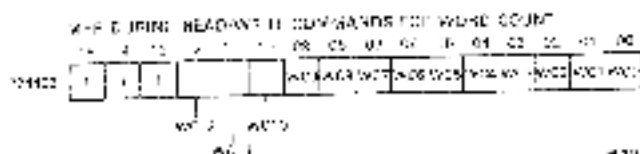
Bit	Function
11	Spin Error (SPE) - Indicates that the spindle did not reach speed in the required time; or indicates over speeding.
12	Seek time Out (SKTO) - Indicates that the heads did not come on track in the required time during a SEEK command or loss of "ready to read/write during lock on" mode.
13	Write Lock (WL) - Indicates write lock status of selected drive. Set = write protected.
14	Head Current Error (HCE) - Indicates that write current was detected in the heads when write gate was not asserted.
15	Write Data Error (WDE) - Indicates that write gate was asserted but no transitions were detected on the write data line.

MPR DURING READ HEADER COMMAND



MPR Three Header Words

MPR After a Read Header Command - When a READ HEADER command is executed, three words will be stored in the multipurpose register (FIFO output buffer). The first header word will contain sector address (SA0:SA5), head select (HS - set = lower; clear = upper), and cylinder address information (CA0:CA6). The second word will contain all 0s. The third word will contain the header CRC information. All three words are readable by the main program.



MPR Used As Word Counter

Bit Definitions

Bit	Function
0-12	Word Count (WOC < 2,025) - 2's complement of total number of words to be transferred.
13-15	Must be a 1 for word count in correct range.

MPR During READ/WRITE DATA Commands - When transferring data via DMA, the MPR functions as a word counter and is loaded by program with the 2's complement of the number of words to be transferred. It is then incremented by 1 by the controller as each word is transferred. The reading or writing operation generally is terminated when the word counter overflows. The word counter can keep track of from one data word to the full 40-sector count of 512H data words (decimal). The maximum number of words that can be transferred in a single operation is limited by the number of sectors available to be written in the track.

NOTE

The RLV11/RLV12 disk drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. Program the data transfer to terminate at the end of the last sector of the track.
2. Program a seek to the next track. This can be accomplished either by a head switch to the other surface but the same cylinder, or a head switch to move to the next cylinder.
3. Program the data transfer to continue at the start of the first sector on the next track.

RLV12 DISK CONTROLLER**Power Requirements**

+5 Vdc $\pm$ 5% at 5.0 A
 +12 Vdc $\pm$ 5% at 0.1 A

Bus Loads

DC	AC
1	2.7

Optional Drive Cables

Cable	Part No.	Length
BC20J-20	7012122-20	6 m (20 ft)
BC20J-40	7012122-40	12 m (40 ft)
BC20J-60	7012122-60	18 m (60 ft)

NOTE

Total length of cable(s) from controller to the last drive must not exceed 30 m (100 ft).

FCC Cable Information**Order Number**

RLV12-AP	Factory installed shielded cable and filler connector assembly, plus RLV12 option.
RLV12	Disk Controller option only.
CK-RLV1A-KA	Cabinet Kit for BA23/M-cro
CK-RLV1A-KB	Cabinet Kit for h3012/PDP-11/285
CK-RLV1A-KC	Cabinet Kit for R368/PDP-11/23-PI U.S.

RLV12/M8051

Standard Addresses

Standard Address Assignments

Device Address	16-Bit Addressing	18-Bit Addressing	22-Bit Addressing*
Starting address range	160000-177770	160000-177770	17760000-1777760
Starting address	174400	174400	17774400
Number of registers	4	4	8 (5 are used; 3 are not)
Registers used	CSR (174400) BAR (174402) DAR (174404) MPH (174406)	CSR (1774400) BAR (1774402) DAR (1774404) MPH (1774406)	CSR (17774400) BAR (17774402) DAR (17774404) MPH (17774406) BAE (17774410)
Interrupt Vector			
Vector range	0-774	0-774	0-774
Standard vector	160	160	160

*Factory configuration (TCO M8051-002)

Diagnostic Programs

Refer to Appendix A.

Related Documentation

RLV12 Disk Controller User's Guide (EK-RLV12-UG)
RL01 Field Maintenance Print Set (MP00347)
RL02 Field Maintenance Print Set (MP00353)
RL01 Disk Drive I/O (EK-0110-1P)
RL02 Disk Drive I/O (EK-0110-2P)
RL01/RL02 User's Guide (EK-RL01-2-UG)
RL01/RL02 Pocket Service Guide (EK-RL012-PG)

CONFIGURATION

The user or installer can configure and install the RLV12 in a 16-, 18-, or 22-bit LSI-11 bus. The user can select the device address, interrupt vector, and memory parity error abort feature.

Device Address Selection

Software control of the RLV12 is by means of four or five device registers — CSR, DAR, BAR, MPN, and BAE. Four registers are used for 16- or 18-bit addressing; five registers are used for 22-bit addressing. The bus address extension register (BAE) is added for upper address bit selection for 22-bit addressing. The usual device starting address is as follows.

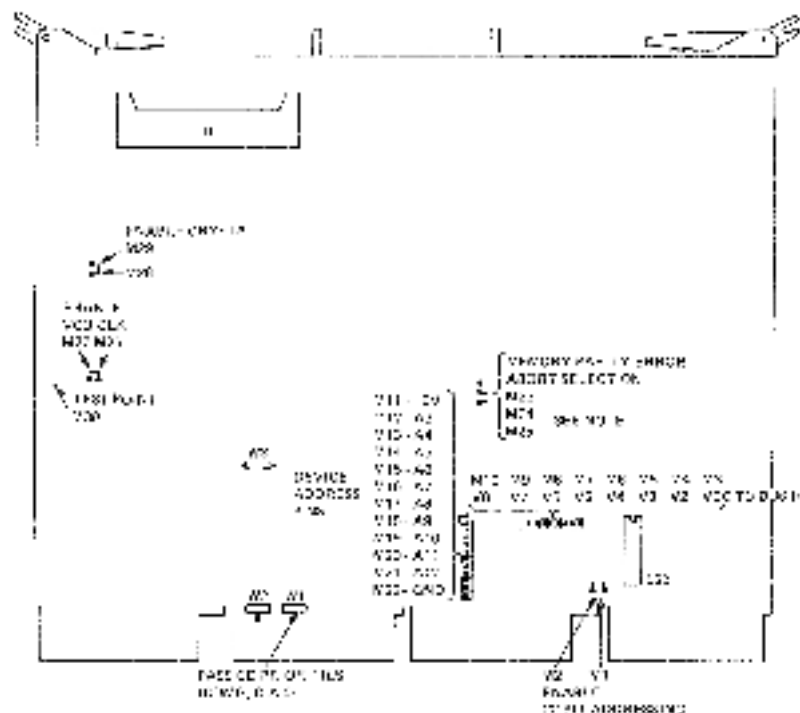
Device Starting Address	
Addressing Mode	Starting Address (Octal)
16-bit	174400
18-bit	774400
22-bit	17774400

The first register, the CSR, is assigned the starting address, and the other registers are incremented by 2.

The device starting address is selected by jumpers for bits 05 through 12. A jumper from the selected bit to ground (M22) decodes a 0; no jumper decodes a 1; and a jumper to +5 V (M11) decodes an X (don't care) condition. The following figure shows the RLV12 device starting address format.

NOTE

For 22-bit addressing, bit A3 is not decoded in the starting address.



NOTE:
 1. MEMORY PARTS LINEAR ADDRESS
 2. MEMORY PARTS LINEAR ADDRESS
 3. MEMORY PARTS LINEAR ADDRESS
 4. MEMORY PARTS LINEAR ADDRESS
 5. MEMORY PARTS LINEAR ADDRESS
 6. MEMORY PARTS LINEAR ADDRESS
 7. MEMORY PARTS LINEAR ADDRESS
 8. MEMORY PARTS LINEAR ADDRESS
 9. MEMORY PARTS LINEAR ADDRESS
 10. MEMORY PARTS LINEAR ADDRESS
 11. MEMORY PARTS LINEAR ADDRESS
 12. MEMORY PARTS LINEAR ADDRESS

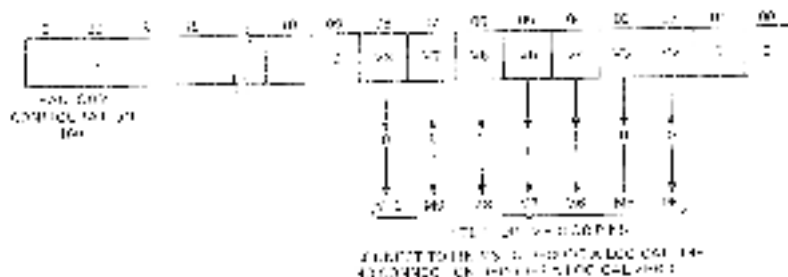
ADDRESS	FUNCTION
M00 - M04	MEMORY
M05 - M09	MEMORY

RLV12 Module Layout

RLV12/M3061

Interrupt Vector

The interrupt vector has a range of 0 to 774. The interrupt vector is preset at the factory to 180. The user may select another vector by changing the jumpers on pins V0-V8. A connection to M3 generates a 1 for that bit, no connection generates a 0. The RLV12 interrupt is at priority level 4.



RLV12 Interrupt Vector Format

Bus Selection

The RLV12 module can be used on 16-, 18-, or 22-bit SI-11 buses. When sent from the factory, the module operates on a 22-bit bus. Jumper M1 to M2 is installed, which enables bank select 7 (BRS7) to be determined by the upper address bits (10-21). When the jumper is removed, the RLV12 has an 18-bit mode bank select 7.

NOTE

The RLV12 may be used in a 16- or 18-bit system while configured in a 22-bit operation (factory-shipped configuration) provided it is the only RLV12 in the system.

Memory Parity Error Abort Feature

When reading the system's optional memory with parity error detection, a parity error will set GPI and NXM of the CSR. This is a unique error condition that aborts the current command to the RLV12. This error abort feature is possible only with memories that have parity data bits.

The RLV12 is sent from the factory with the memory parity error abort feature enabled. To disable parity error abort, remove the jumper between pins M24 and M25 and install a jumper between pins M20 and M24. This feature does not have to be disabled for nonparity memories, as parity errors are not generated. Parity error abort uses data bits 16 and 17.

Jumpers That Remain Installed

The module has two jumpers, W1 and W2, that enable priority signals to pass through the module. The module has these jumpers installed, and they should be left in.

Jumper	Signal
W1	CIACK to CIAKO
W2	CDMOI to CDMCO

One jumper, W3, enables the word count register to automatically increment during a DMA operation. This jumper is used for factory testing and should be left in.

Two jumpers on the module disable the crystal oscillator and the voltage-controlled oscillator (VCO) during factory testing. These jumpers should be left in.

Jumper	Oscillator
M21-M27	VCO
M28-M29	Crystal

CONTROL STATUS REGISTER (CSR)

The control status register is a 16-bit, word-addressable register with a standard address of 774400 for 16-bit addressing, and 17774400 for 32-bit addressing. Bits 01 through 08 can be read or written; the other bits can only be read. The bit functions are described in the following table.

When the LSI-11 bus is initialized with RINIT 1, bits 01-08 and 09-13 are cleared, and bit 07 (CRDY) is set. Bit 00 (RDY) is set when the selected drive is ready to accept a command; otherwise, this bit is cleared. Bit 14 (DE) is clear as long as there is no drive error. Otherwise, this bit is set and stays set until the drive error is corrected, or if bit 03 (drive reset) is set or the DAIR and the controller is sent a get status command, the DE bit is cleared.

Bit 15 (ERR) is set when there is a drive or controller error in bits 10-14.



Control Status Register (CSR)

RLV12 Control Status Register Bit Assignments

Bit	Name	Description																				
00	DRDY	Drive ready - When set, this bit indicates that the selected drive is ready to receive a command or supply valid read data. The bit is cleared when a seek or head select operation is started and set when the seek operation is completed.																				
01-03	F0-F2	Function code - These bits are the function code set by software to indicate the command to be executed. <table><tr><th>Function</th><th>Octal Code</th></tr><tr><th>F2 F1 F0 Command</th><th></th></tr><tr><td>0 0 0 Maintenance mode</td><td>0</td></tr><tr><td>0 0 1 Write check</td><td>1</td></tr><tr><td>0 1 0 Get status</td><td>2</td></tr><tr><td>0 1 1 Seek</td><td>3</td></tr><tr><td>1 0 0 Read header</td><td>4</td></tr><tr><td>1 0 1 Write data</td><td>5</td></tr><tr><td>1 1 0 Read data</td><td>6</td></tr><tr><td>1 1 1 Read data without header check</td><td>7</td></tr></table> Command execution starts when CRDY (bit 07) of the CSR is cleared by software. The function code is cleared by initializing the bus (BINIT L).	Function	Octal Code	F2 F1 F0 Command		0 0 0 Maintenance mode	0	0 0 1 Write check	1	0 1 0 Get status	2	0 1 1 Seek	3	1 0 0 Read header	4	1 0 1 Write data	5	1 1 0 Read data	6	1 1 1 Read data without header check	7
Function	Octal Code																					
F2 F1 F0 Command																						
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0 0 1 Write check	1																					
0 1 0 Get status	2																					
0 1 1 Seek	3																					
1 0 0 Read header	4																					
1 0 1 Write data	5																					
1 1 0 Read data	6																					
1 1 1 Read data without header check	7																					
04, 05	BA16, BA17	Extended address bits - These two bits are the upper-order bus address bits for 18-bit buses. These bits are read and written as bits 04 and 05 of the CSR. They function as address bits 16 and 17 of the BAE. Writing bits 04 and 05 of the CSR also writes bits 0 and 1 of the BAE.																				
06	IE	Interrupt enable - When CRDY is asserted, bit 06 allows the controller to interrupt the processor. This interrupt occurs at the termination of a command. Once an interrupt request is placed on the LSI-11 bus, it is not removed until acknowledged by the LSI-11 processor even if IE (bit 06) is cleared. This bit is cleared by initializing the bus.																				

RLV12 Control Status Register Bit Assignments (Cont)

Bit	Name	Description																		
07	CRDY	Controller ready - When cleared by software, this bit indicates that the command in bits 01-03 is to be executed. This bit is set by the controller at the completion of a command, at the detection of an error, or by initializing the bus. Software cannot set this bit because registers are not accessible while CRDY is 0.																		
08, 09	DS0, DS1	Drive select - These bits determine which drive will communicate with the controller via the drive bus. These bits are cleared by initializing the bus.																		
10-13	EO-EO	Controller status errors - These bits are the error code set by the controller to indicate one of the following errors.																		
		<table><tr><th>Error Code</th><th>Octal Code</th></tr><tr><th>E3 E2 E1 EO Error</th><th></th></tr><tr><td>0 0 0 1 Operation incomplete (OPI)</td><td>1</td></tr><tr><td>0 0 1 0 Data CRC (DORC)</td><td>2</td></tr><tr><td>0 0 1 1 Header CRC (HORC)</td><td>3</td></tr><tr><td>0 1 0 0 Data late (DLT)</td><td>4</td></tr><tr><td>0 1 0 1 Header not found (HNF)</td><td>5</td></tr><tr><td>1 0 0 0 Nonexistent memory (NXM)</td><td>10</td></tr><tr><td>1 0 0 1 Parity error abn (PAR ERR)</td><td>11</td></tr></table>	Error Code	Octal Code	E3 E2 E1 EO Error		0 0 0 1 Operation incomplete (OPI)	1	0 0 1 0 Data CRC (DORC)	2	0 0 1 1 Header CRC (HORC)	3	0 1 0 0 Data late (DLT)	4	0 1 0 1 Header not found (HNF)	5	1 0 0 0 Nonexistent memory (NXM)	10	1 0 0 1 Parity error abn (PAR ERR)	11
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0 0 1 0 Data CRC (DORC)	2																			
0 0 1 1 Header CRC (HORC)	3																			
0 1 0 0 Data late (DLT)	4																			
0 1 0 1 Header not found (HNF)	5																			
1 0 0 0 Nonexistent memory (NXM)	10																			
1 0 0 1 Parity error abn (PAR ERR)	11																			
		Operation incomplete indicates that the current command was not completed within the OPI timeout period of 550 ms.																		
		A data CRC error indicates that while reading the data field from the disk an error was found.																		
		A header CRC error indicates that while reading the header from the disk an error was found. The CRC check is performed on the first and second header words, although the second header word is always 0.																		
		Data late indicates that the FIFO RAM was more than half full and the controller was not able to read the next sequential sector. This error may occur during a read without header check command.																		

RLV12 Control Status Register Bit Assignments (Cont)

Bit	Name	Description
		Header not found indicates that an OPI timeout occurred while the controller was searching for the correct sector to read or write. A header compare did not occur.
		A non-existent memory error indicates that during a DMA transfer, the memory location addressed did not respond with PPLY within 10 µs.
		A memory parity error abort indicates that a parity error was detected while reading the system's optional memory that has parity error checking. If an error was detected, the current command to the RLV12 is aborted.
14	DE	Drive error - This bit is buffered from the drive error interface line. When set, it indicates that the selected drive has flagged an error, the source of which can be determined by executing a get status command. DE will not set FRR (bit 15) or GRDY (bit 07) until the usual occurrence of CRS.
15	ERR	Composite error - When set, this bit indicates that one or more of the error bits (bits 10-14) are set. When an error occurs, the current operation terminates and an interrupt routine is started if the interrupt enable bit (bit 06 of the CSR) is set.
		All error bits are cleared by initializing the bus by starting a new command, with the exception of DE and ERR if they were caused by a drive error.

BUS ADDRESS REGISTER (BAR)

The bus address register is a 18-bit, word-addressable register with a standard address of 774402 for 18-bit addressing, and 7774402 for 22-bit addressing. Bits 00 through 16 can be read or written; bit 00 is usually written as 0. The bus address register indicates the memory location for the DMA data transfer during a read or write operation. The register's contents are automatically incremented by 2 as each word is transferred between the system memory and the controller.

The bus address can be expanded for an 18-bit LSI-11 bus by using bits 114 and 05 (BA 16 and 17) of the CSR or by using bits 00 and 01 of the BAE register.

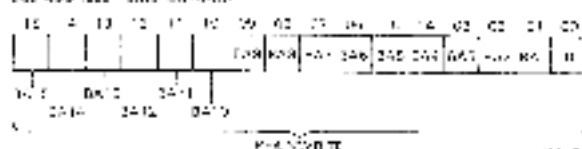
The bus address can be expanded for a 22-bit LSI-11 bus by using the BAE register (BAF 15-21).

NOTE

When using 22-bit mode, writing CSR bits 01 and 05 modifies BAE bits 00 and 01 and vice versa.

The BAE is cleared by initializing the bus (BINIT I).

DISK ADDRESS REGISTER (DAR)



Disk Address Register (DAR)

DISK ADDRESS REGISTER (DAR)

The disk address register is a 16-bit, read/write, word-addressable register with a standard address of 774404 for 18-bit addressing, and 17774404 for 22-bit addressing. Its contents have one of three meanings, depending on the command being performed.

Disk Address Commands

Command	DAR Function
Seek	Head selected, number of cylinders to move, direction.
Read data or write data	Head selected, cylinder address, sector address.
Get status	Send drive status to MPP; reset the error registers.

The DAR is cleared by initializing the bus (BINIT L).

DAR During a Seek Command

To perform a seek command, the program must provide the head selected (HS), direction to move (DIR), and the cylinder address difference (DF). The bits are as follows:

DAR BIT LOCATIONS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DF	DF	DF	DF	DF	DF	DF	DF	DF	0	0	HS	0	DIR	0	MRKR

MRKR (bit 00)

DIR (bit 02)

DAR During a Seek Command**DAR Seek Command Word Format**

Bit	Name	Description
00	MRKR	Marker - Must be a 1.
01	None	Must be a 0, indicating to the drive that a seek command is being issued and that the other bits in the register hold the seek specifications.
02	DIR	Direction - This bit indicates the direction in which the seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 07-15).
03	None	Must be a 0.
04	HS	Head select - Indicates which head (disk surface) is to be selected: 1 - lower, 0 - upper.
05, 06	None	Reserved.
07-15	DF	Cylinder address difference - Indicates the number of cylinders the heads are to move on a seek.

DAR During a Read, Write, or Write Check Command

For a read, write, or write check command, the DAR provides the head selected (HS) and the address of the first sector to be transferred (SA). The bits are described below. As each sector is transferred, the DAR sector address increments by 1.

DAR DURING READ OR WRITE OR WRITE CHECK

Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DAR	SA	SA	SA	SA	SA	SA	SA	SA	SA	HS	SA	SA	SA	SA	SA	SA

MLV12

DAR During a Read, Write, or Write Check Command**DAR Read/Write Data Command Word Format**

Bit	Name	Description
00-10	SA	Sector address - Address of one of the 40 sectors on a track. (Total range is 0 to 40.)
05	HS	Head select - Indicates which head (disk surface) is to be selected. 1 = lower; 0 = upper.
07-15	CA	Cylinder address - Address of one of the 256 cylinders for RL01 or 512 cylinders for RL02. (Total range is 0 to 777.)

DAR During a Get Status Command

Here the CSR and the DAR must be programmed to perform a get status command. Then a get status command is placed in the CSR. The DAR bits are as follows.

DAR DURING GET STATUS COMMAND

Bit	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DAR	X	0	0	X	X	X	X	0	0	0	0	0	AST	0	1	1

MLV12

DAR During a Get Status Command

DAR Get Status Command Word Format

Bit	Name	Description
bit	MARK	Marker - Must be a 1.
01	GS	Get status - Must be a 1, indicating to the drive to send its status word. At the completion of the get status command, the drive status word is read into the controller multipurpose register (MPR). With this bit set, bits C2-C5 are ignored by the drive.
C2	None	Must be a 0.
C3	RST	Reset - When this bit is set, the disk drive clears its error register of soft errors before sending a status word to the controller.
C4-C7	None	Must be a 0.
C8-15	None	Not used.

MULTIPURPOSE REGISTER (MPR)

The multipurpose register is a 16-bit, read/write, word-addressable register. It is accessed using the standard address of 774406 for 16-bit addressing, and 17774408 for 22-bit addressing. Following a read header command or a get status command, reading the MPR obtains sector header or drive status information.

Writing to the MPR is used to set the word count. The word count is cleared by initializing the bus (DINIT L).

Writing the MPR to Set the Word Count

Before starting a DMA transfer, the MPR is loaded with the word count. The program must load the MPR with the 2's complement of the number of words to be transferred. The bits are described below. As each word is transferred, the MPR is automatically incremented by 1. The reading or writing operation continues until a word count overflow occurs, indicating that all words have been transferred.

The word count can range from 1 to 5120 data words. The maximum word count is limited by the maximum number of sectors available (40) and the maximum words per sector (128).

NOTE

Once written, the word count cannot be read back. Reading the MPR does not change the word count.



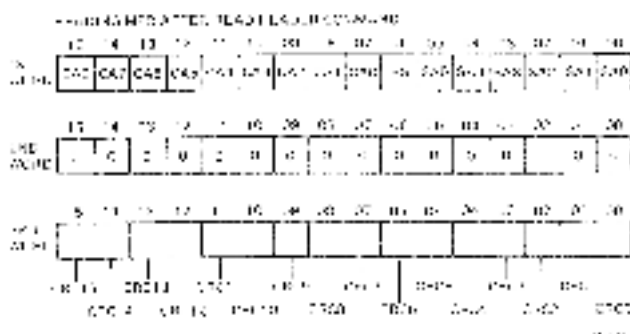
Writing the MPR to Set the Word Count

MPR Word Count Format

Bit	Header	Description
09-12	WC	Word count - This is the 2's complement of the total number of words to be transferred.
15-16	None	Must be all ones for word count in correct range.

Reading the MPR After a Read Header Command

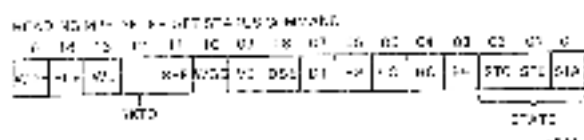
When a read header command is executed, three words can be sequentially read from the MPR, as the following figure shows. The first word includes the sector address, the head selected, and the cylinder address. The second word is all zeros. CRC information is the header for the third word.



Reading the MPR After a Read Header Command
(Three Header Words)

Reading the MPR After a Get Status Command

After a get status command is executed, a status word is stored in the MPR. The status word from the selected disk drive includes information on the functional state of the drive and any drive errors. The bits are described in the following table.



Reading the MPR After a Get Status Command

MPR Status Word Format

Bit	Name	Description																																				
00-11 ²	STA, STB, STC	These bits (A, B, and C) define the state of the drive as follows: <table><tr><th>C</th><th>B</th><th>A</th><th>State of Drive</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Load state</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Spin up</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Brush cycle</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Load heads</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Seek track counting</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Seek linear mode (look nn)</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Unload heads</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Spin down</td></tr></table>	C	B	A	State of Drive	0	0	0	Load state	0	0	1	Spin up	0	1	0	Brush cycle	0	1	1	Load heads	1	0	0	Seek track counting	1	0	1	Seek linear mode (look nn)	1	1	0	Unload heads	1	1	1	Spin down
C	B	A	State of Drive																																			
0	0	0	Load state																																			
0	0	1	Spin up																																			
0	1	0	Brush cycle																																			
0	1	1	Load heads																																			
1	0	0	Seek track counting																																			
1	0	1	Seek linear mode (look nn)																																			
1	1	0	Unload heads																																			
1	1	1	Spin down																																			
12	RII	Brush home - Asserted when the brushes are not over the disk.																																				
14	HIO	Heads out - Asserted when the heads are over the disk.																																				
15	GO	Cover open - Asserted when the cover is open or the dust cover is not in place.																																				
16	HS	Head select - Indicates the head selected: 1 - lower, 0 - upper.																																				

MPR Status Word Format (Cont)

Bit	Name	Description
07	DT	Drive type - Indicates the type of disk drive: 0 = RL01, 1 = RL02.
08	DSF	Drive select error - Indicates multiple drive selection is detected.
09	VC	Volume check - VC is set every time the drive goes into bad heads state. This asserts a drive error at the controller, but not on the front panel. VC is an indication that the program does not know which disk is present until it has read the serial number and bad sector file. (The disk might have been changed while the heads were unloaded.)
10	WGE	Write gate error - Indicates that the write gate was asserted when the drive was not ready, the sector pulse was asserted, or the drive was write locked.
11	EPE	Spin error - Indicates that the spindle did not reach full speed within a specific time, or that it is turning too fast.
12	SKTO	Seek time out - Indicates that the heads did not come onto track within a specific time during a seek command.
13	WL	Write lock - Indicates write lock status of selected drive: 0 = unlocked; 1 = protected.
14	HCE	Head current error - Indicates that write current was detected in the heads when write gate was not asserted.
15	WDE	Write data error - Indicates write gate was asserted, but no pulses were detected on the write data line.

BUS ADDRESS EXTENSION REGISTER (BAE)

The bus address extension register is a 16-bit read-write register used to drive address bits 18-21 for a 22-bit LSI-11 bus. The BAE has a standard address of 17774410 for 22-bit addressing. A write to the BAE loads TS DA0-11 into BAE 0-5. Reading the BAE enables bank select 7 (HRS7 L) to the LSI-11 bus. (A jumper must be connected between M⁺ and M⁻ on the controller to enable 22-bit addressing.) When address bits 18-21 are all ones, the RLV12 drives HRS7 L to direct data to the I/O page.

The two least significant bits of the BAE (bus address lines 18 and 19) are mirrored in bits 04 and 05 of the CSR. The same bits can be read or written as CSR bits 04 and 05 or BAE bits 00 and 01.

NOTE

Writing CSR bits 04 and 05 modifies BAE bits 0 and 1 and vice versa.

The BAE register is cleared by initializing the bus (BINIT L).

TABLE 12-20 LSI-11-45H001

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
BAE0-5 BAE6-11 BAE12-15															

BAE Register Word Format

RQDX1 AND EXTENDER CONTROLLER MODULE (RX50, RD51, RD52)

Amperage		Bus Loads	
+5 V	+12 Vdc	AC	UD
0.4 A	7.5 mA	0.5	1
0 A (max.)	10 mA (max.)		

Standard Addresses

Address Mode	Default Address
16-bit	172150
18-bit	172150
22-bit	17772150

Vectors

Software selectable (normally set to 104)

Diagnostic Programs

ZRQA??	RIN RQDX Performance Examiner
ZRQB??	RIN RQDX Formatter (R051)

Related Documentation

RQDX1 Field Maintenance Print Set (MF01731-01)
 UDAX0 Programmer's Document Kit (GP-005-02)
 RQDX0 Controller Modules User's Guide (RK RQDX0-UG)

RQDX1 Standard Address Jumper Configuration

Jumper	State	
A2	OUT	Address selector (7/2150)
A3	IN	
A4	OUT	
A5	IN	
A6	IN	
A7	OUT	
A8	OUT	
A9	OUT	
A10	IN	
A11	OUT	
A12	IN	

LOGICAL UNIT NUMBER SELECTION

The location of the RQDX1 controller module logical unit number jumpers is shown below. These jumpers are set to the lowest logical unit number assigned to any disk/diskette drive controlled by the module. The controller module automatically sizes the logical unit configuration during initialization to determine how many (or four possible units) are actually present. This automatic sizing eliminates the need for the reconfiguration of jumpers when units (RDS1 or RDS0 drives) are added to or removed from the controller module. The standard configuration for the logical unit number jumpers (selecting logical unit number 0) is listed. To configure the module for logical unit numbers beginning with other than unit number 0, use the format shown below to determine the appropriate jumper configuration.

LOGICAL UNIT Jumper from 10	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

OPTIONAL JUMPER 8
INSTALLED AT ANY
TIME
ALL JUMPER SETS TO
SELECTED UNIT
FROM 0-15

- 32 -

RQDX1 Logical Unit Number Jumper Format

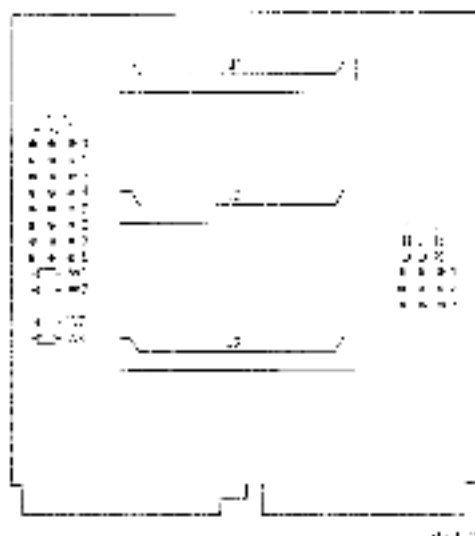
RQDX1 Standard Logical Unit Number Jumper Configuration

Jumper	State	
LUN1	OUT	Logical unit number (0)
LUN2	OUT	
LUN3	OUT	
LUN4	OUT	
LUN5	OUT	
LUN6	OUT	
LUN7	OUT	
LUN8	OUT	

This indicates that logical unit numbers 0-3 are assigned to this controller module. The controller will automatically determine if less than four logical units are present.

RQDX1-E Extender Module Jumper Configuration

The RQDX1-E extender module is a dual-height module that provides signal connectors and requires appropriate jumper configurations. The J2 connector receives signals from the RQDX1 controller module. The other connectors (J1 and J3) distribute those signals to the disk and diskette drives. Jumper functions for the RQDX1-E extender module, as well as the jumpers installed in the factory configuration, are listed.



RQDX1-E Extender Module Jumper Locations

RQDX1-E Extender Module Jumper Configuration

Jumpers	Functions	Factory Configuration*
W1-W4	Must be installed (Manufacturing use only)	W1-W4
JRD1-JRD3 JD1-JD3 JRX1-JRX3	Select the external drive to be connected to the J3 connector	JD1 to JRD1 JD2 to JRD2 JD3 to JRD3
JB1-JB6 JA-JA8 JC-JC8	Determine which connector (J2 or J0) the RD read/write will connect to	JA2 to JC2 JA2 to JC2 JA3 to JB3 JA1 to JB4 JA5 to JB5 JA6 to JB6 JA7 to JC7 JA8 to JC8

- * Factory configuration is set to connect an external RD51 disk drive to connector J3. To configure the module for an external RK50 (connected to J3), jumpers JD1 through JD3 are connected to JRX1 through JRX3 and jumpers JB1 through JB8 are connected to JB1 through JB8.

Interrupt Vector

The interrupt vector has a range of 0 to 774 and is software selectable. A vector selected by software must be greater than 0. The normal interrupt vector used by the RQDX1 controller module is 154.

Interrupt Request Level

The RQDX1 controller module interrupts at priority level 4 and are determined by C3, a D0009 chip.

RQDX1/M8639

RQDX1 CONTROLLER MODULE INSTALLATION

The RQDX1 module (M8639) is typically installed in the last occupied slot of the backplane. If empty slots are left between the other modules and the M8639 module, install grant cards (part no. 07272) in those empty slots to accommodate the interrupt and direct memory access structure of the backplane.

Before installing the module, make sure that the address and logical unit number jumpers are properly configured.

Install the 50-conductor signal cable (part no. RQX2U-10) to the J1 connector of the M8639 module. This cable must be connected to a signal distribution cable that will connect the appropriate signals to the RD51 and/or RX50 drives. An example of the MICRO/PDP-11 signal distribution cable connecting the M8639 module to an RD51 disk drive and an RX50 diskette drive is on the next page. The RD51 disk drive requires two signal cable connections. One is a 25-conductor cable (part no. 17-30282-00), the other is a 34-conductor cable (part no. 17-30283-00). The RX50 diskette drive requires a single 34-conductor signal cable (part no. 17-30285-00).

RQDX1-E EXTENDER MODULE OPTION

Typically, in the MICRO/PDP-11, the RQDX1 controller module is located in the same mounting box as the disk and/or diskette drives that it controls. However, if the system mounting box cannot hold all of these drives, the optional RQDX1-E extender module may be used to connect the RQDX1 controller module signals to any drive that is external from the system mounting box.

NOTE

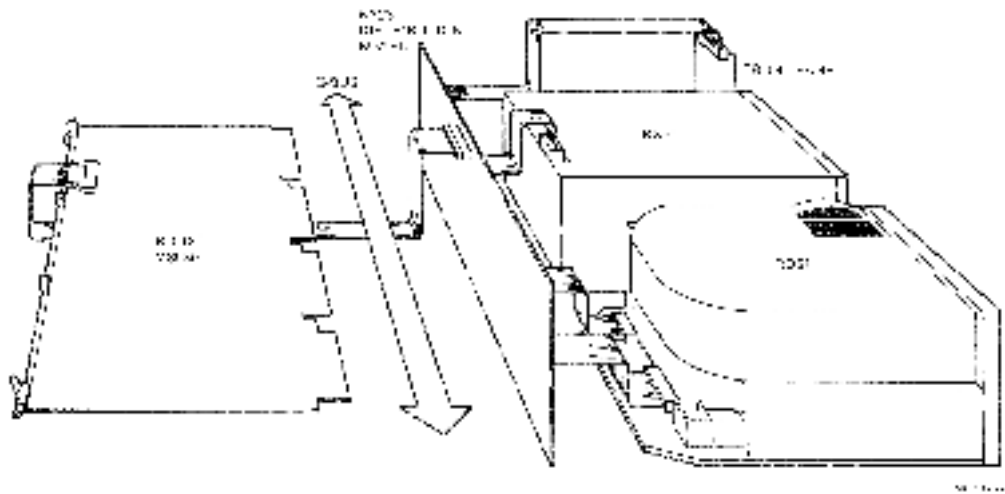
Jumpers selection (for configurations listed) is made by attaching two-position jumper clips (part no. 12-18783-00).

RQDX1-E EXTENDER MODULE INSTALLATION

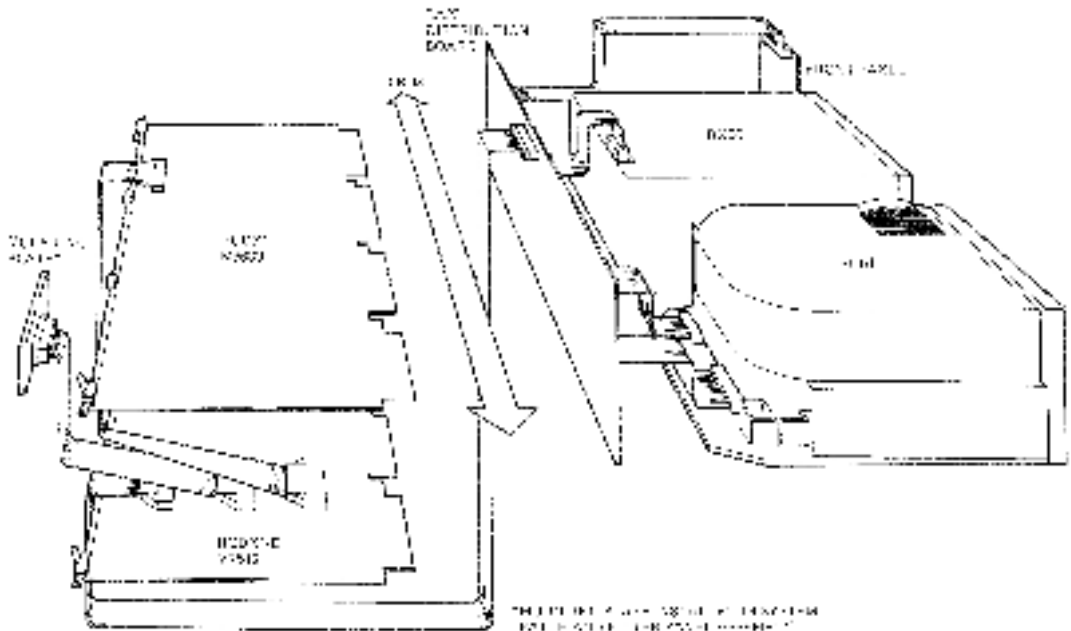
Installation of the RQDX1-E extender module option in the MICRO/PDP-11 system (B423 mounting box) is as follows. The V7512 dual-height module is installed in the backplane slot directly below the M8639 (RQDX1) module, in connectors A and B. A cable (part no. SC02D-04) connects the RQDX1 controller module to the RQDX1-E extender module through the J2 connector. Another cable (part no. 70-18562-01), attached to the J3 connector, connects the RQDX1-E extender module to a mounting plate (part no. 74-2868-01). This is mounted to the system's patch and filter band assembly. The entire cable and mounting plate assembly may be ordered as part number 70-20691-01. This external plate provides the signals to be sent to the external drive. A third cable (part no. RQX2U-10) attached to the J1 connector of the RQDX1-E extender module is connected to the signal distribution panel in the mounting box, providing signals to the disk or diskette drives that are installed in the system mounting box.

Cable Signals

RQDX1 controller module signals on the J1 connector.



RGJX Micro/PDP 11 Right Distribution Connectors



THE POWER JAR IS USED TO CONNECT
THE EXTENDER MODULE TO THE BASE UNIT.

4-1111

RQDX1 E Extender Module Connections

J1 Connector Signals

J1 Pin	Signal Name
1	MEMWRITDT1 (L) (RDS1 only signal)
2	MEMWRITDT1 (L) (RDS1 only signal)
3	GROUND
4	HEAD SEL 2 (L) (RDX only signal)*
5	GROUND
6	SP-ENGPI 1 (L) (RDS1 only signal)
7	RDI RTN (H) (RDS1 only signal)
8	WR. FAULT (L)
9	DRVDSG0E (L)
10	HEAD SEL 1 (L) (RDS1 only signal)
11	DXWPTLED (L) (RX50 only signal)
12	RDS RDY (H) (RDS1 only signal)
13	DXWPTLED (L) (RX50 only signal)
14	DRVSLDACK (L) (RDS1 only signal)
15	MEMRDJATO (H) (RDS1 only signal)
16	MEMRDJATO (L) (RDS1 only signal)
17	MEMRDJATO (H) (RDS1 only signal)
18	MEMRDJATO (L) (RDS1 only signal)
19	MEMRDJATO (H) (RDS1 only signal)
20	MEMRDJATO (L) (RDS1 only signal)
21	GROUND
22	REDUCWRTI (L)
23	RDWRTPRO (L) (RDS1 only signal)
24	DRV SPI 4 (L)
25	GROUND
26	INDEX (L)
27	HDSWR1 PRO (L) (RDS1 only signal)
28	DRV SEL 1 (L)
29	DRV SEL 2 (L)
30	DRV SPI 3 (L)
31	RX29PH (H) (L) (RX50 only signal)
32	RX MOTORON (L) (RX50 only signal)
33	GROUND
34	DIRECTION (L)
35	GROUND
36	STEP (L)
37	GROUND
38	RXWR1 DATA (L) (RX50 only signal)
39	GROUND

*Reserved for future use.

J1 Connector Signals (Cont)

J1 Pin	Signal Name
40	WRITE GATE (L)
41	GROUND
42	TRACK 00 (L)
43	RX3WPT_LED (L) (RX50 only signal)
44	PRVSLTACK (L) (RD51 only signal)
45	GROUND
46	HEAD DATA (L) (RX50 only signal)
47	GROUND
48	HEAD SELECT (L)
49	GROUND
50	READY (L)

RD51 Disk Drive J1 Signal Connector Pin Assignments

END Return Pin	Signal Pin	Signal Name
-	2	Reserved
3	4	Head select 2
5	6	Write gate
7	8	Seek complete
9	10	Track 0
11	12	Write fault
13	14	Head select 0
15	16	Reserved (to JP pin 7)
17	18	Head select 1
19	20	Index
21	22	Ready
23	24	Stop
25	26	Drive select 1
27	28	Drive select 2
29	30	Drive select 3
31	32	Drive select 4
33	34	Direction in

RDS1 Disk Drive J2 Signal Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	Drive selected
4	3	Reserved
6	5	Reserved
8	7	Reserved (to J1 pin 16)
	9, 10	Reserved
12	11	Blank
	13	-MFM write data
	14	-MFM write data
15	15	GND
	17	+MFM read data
	18	-MFM read data
20	19	GND

RDS1 Disk Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

RX50 Diskette Drive J1 Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
1	2	TK43L (controls write current level)
3	4	Reserved
5	6	Drive select 3 L
7	8	Index
9	10	Drive select 0 L
11	12	Drive select 1 L
13	14	Drive select 2 L
15	16	Motor on L
17	18	Direction (head movement direction)
19	20	Step L (head movement distance)
21	22	Write data L
23	24	Write gate L
25	26	Track 0 L
27	28	Write protect L
29	30	Head data L
31	32	Reserved
33	34	Ready L

RX50 Diskette Drive J3 Power Connector Pin Assignments

GND Return Pin	Signal Pin	Signal Name
2	1	+12 V
3	4	+5 V

RXV11 FLOPPY DISK INTERFACE

Amps		Bus Loads		Cables
1.6	1.12	AC	DC	
1.6 max	0	1.74	1	BC05L

Standard Addresses

	First Device	Second Device
RXDS	177170	177160
RXDR	177172	177162
Version	204	270

Diagnostic Programs

Refer to Appendix A

NOTE

Run DZRXB before DZRXA.

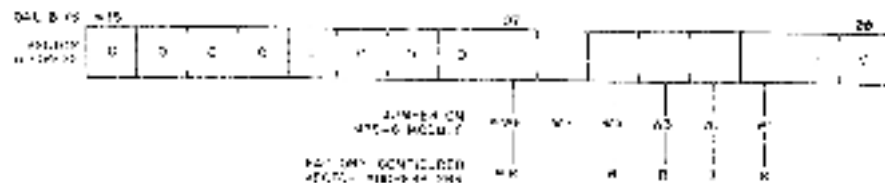
Related Documentation

RXV11 User's Manual (EK RXV11-OP-001)
Field Maintenance Print Set (MPC0024)
Microcomputer Interfaces Handbook (EB-20175-00)





Device Address



Vector Address

FIG. 1
 1. ADDRESS PREFIX (4 bits)
 2. ADDRESS SUFFIX (16 bits)
 3. ADDRESS

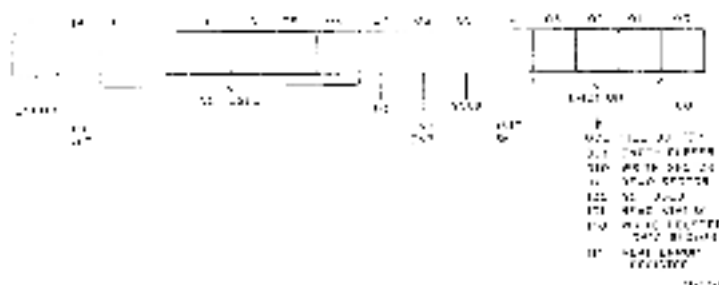
FIG. 2

Unit	Address	Address Jumpers										
		W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7
First (Drives C, 1)	177170	R	R	R	R	I	I	I	R	R	I	I
Second (Drives 2, 3)	177150	R	R	R	R	I	I	R	R	I	R	I

Unit	Vector	Vector Jumpers					
		W6	W5	W4	W3	W2	W1
First (Drives C, 1)	264	R	I	R	I	I	R
Second (Drives 2, 3)	270	R	I	R	R	R	I

NOTES

1. When inserting the cable in the RXV11 interface module, the red edge of the cable should be at the center of the module (near the pin A end of J1).
2. SUB INIT - install W18 to pass bus INIT to the RX01 as initialize.



Receiver Control/Status Register (RCRS)

Bit Definitions

Bit	Function
0	Go - Initiates a command to RX01. Write only.
1-3	Function Select - These bits code one of the eight possible functions. Write only.
4	Unit Select - This bit selects one of the two possible dies for execution of the desired function. Write only.
5	Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RXCS bit 6) is set. Read only.
6	Interrupt Enable - This bit is set by the program to enable an interrupt when the RX01 has completed an operation (done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by the I/O bus initialize (RINIT L) signal, but it is not cleared by the RXV11 initialize bit (RXCS bit 14). Read/write.

Bit Definitions (Cont)

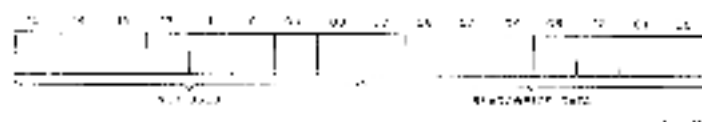
Bit	Function
7	Transfer Request - This bit signifies that the RXV11 needs data or has data available. Read only.
8-10	Unused.
11	RXV11 Initialize - This bit is set by the program to initialize the RXV11 without initializing all of the devices on the LSI-11 bus. Write only.
12	Upon setting this bit in the RXCS, the RXV11 will negate done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful initialize, the RX01 will zero the error and status register, set initialize done, and set HHS bit 7 (DRV RDY) when 0 is ready. It will a so read sector 1 of track 1 and drive 0.
13	Error - This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or by setting the initialize bit. When an error is detected, the RXES is automatically read into the RXDS.

The RXDS register serves as a general purpose data path between the RX01 and the RXV11 interface. It may represent one of five RX01 registers according to the protocol of the command function in progress. The RX01 registers include RXDS, RXTA, RXSA, RXES, and RXEI.

CAUTION

Violation of protocol in manipulation of this register may cause permanent data loss. Refer to *RXV11 User's Manual*.

RXDB-RX Data Buffer – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.



RXDB Format

RXTA-RX Track Address – This register is loaded to indicate on which of the 114 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



RXTA Format

RXSA-RX Sector Address – This register is loaded to indicate on which of the 32 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



RXSA Format

RXES-RX Error and Status – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDH upon completion of a function.



RXES Format

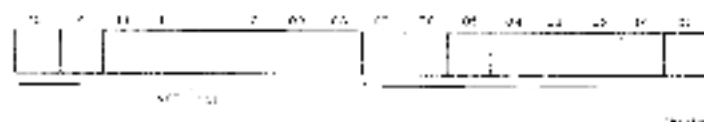
RXDB Bit Definitions

Bit	Function
0	CRC Error - A cyclic redundancy check error was detected on information was received from a data field of the diskette. The RXES is moved to the RXDB, and error and done are asserted.
1	Parity Error - A parity error was detected on command or on address information being transferred to the RXUI from the LSI-11 bus interface. A parity error indication means that there is a problem in the interface cable between the RXCI and the interface. Upon detection of a parity error, the current function is terminated, the RXES is moved to the RXDB, and the error and done are asserted.
2	Initialize Done - This bit is asserted in the RXES to indicate completion of the initialize routine, which can be caused by RXUI power failure, system power failure, or programmable or LSI-11 bus initialize.
3-5	Unused
6	Deleted Data Detected - During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready - This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTES

1. The drive ready bit is valid only when retrieved via a read status function or at completion of initialize when it indicates status of drive 0.
2. If the error bit was set in the RXCS but error bits are not set in the RXES, then specific error conditions contained in the RXER can be accessed from the RXDB via a read error register function.

RXER-RX Error - This register is located in the RXCI and contains specific RXCI error information. This information is normally accessed when the RXCS error bit is set but RXES error bits 0 and 1 are not set. This is a read only register.



OXEON Fuelcell

Decimal Code	Error Code Meaning
0010	Drive 0 failed to see home on initialize.
0020	Drive 1 failed to see home on initialize.
0030	Found home when stepping out 10 tracks for INIT.
0040	Tried to access a track greater than 77.
0050	Home was found before desired track was reached.
0060	Sed diagnostic error.
0070	Desired sector could not be found after moving at 82 heads (two revolutions).
0110	More than 40 microseconds and no SEP clock seen.
0120	A preamble could not be found.
0130	Preamble found but no I/O mark found within allowable time span.
0140	CRC error on a header; no flag.
0150	The header track address of a good header does not compare with the desired track.
0160	Too many tries for an ID address mark.
0170	Data mark not found in a cited time.
0200	CRC error on reading the sector from the disk. No code appears in the EPIEB.
0210	Parity error on some word from interface.

RXV21 FLOPPY DISK CONTROLLER

Amps		Bus Loads		Cables	
1.5	1.12	AC	DC		
1.8		5.0	1.0	DC051	16

Standard Addresses

	First Controller	Second Controller
RXC6	177170	177200
RXDR	177172	177202

Standard Vectors

264 270

Diagnostic Programs

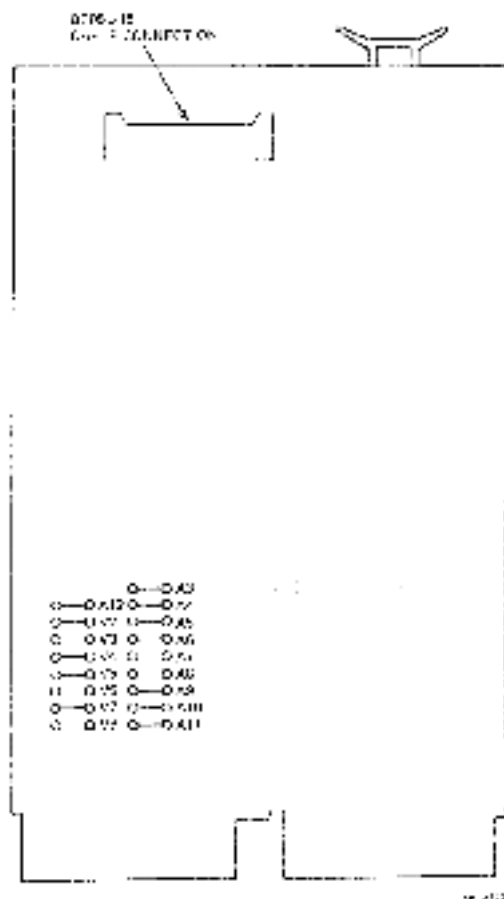
Refer to Appendix A

Related Documentation

RXV21 Field Maintenance Print Set (MP00628)
RX02 Floppy Disk System User's Guide (EK RX02-UG)
 RX01/RX02 Reference Card (FK-RX102-RC)
RX02 Technical Manual (EK DRX02-TM)
Minicomputer Interfaces Handbook (EB-2011/6-20)
 RX02 Field Maintenance Print Set (MP 00629-00)

CAUTION

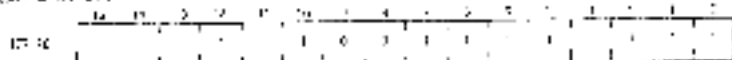
PDP-11/23 systems require the M8029 to be at C'S revision E1 or higher.



M8029 Module Address and Vector Jumpers

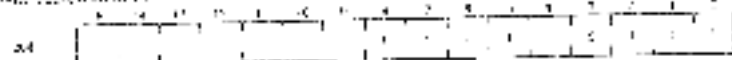
RXV21/M8029

READ ERROR ADDRESS



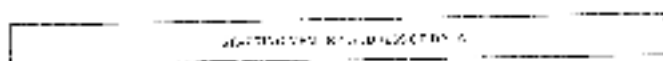
READ ERROR

READ ERROR VALUE ADDRESS

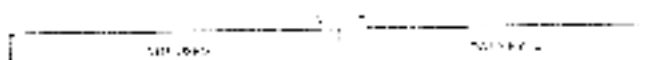


READ ERROR

READ ERROR



READ ERROR



RXV21 Error Codes

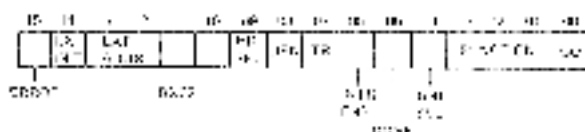
Error Codes

Error Reg

15 14 13 12 11 10 9 8	7	6	5	4	3	2	1	0
Track address DV	DV SEL	GEN DV1	HD LD	DER DVD				DER CMD
Target Sector	Target Track							
Current Track DV1	Current Track DVD							
Word Count Hdg	Error Code							

The following sequence is used to get definitive error information for doing a bootstrap operation. (It is assumed that the bootstrap program has halted and the CPU is in ODT.)

1. Examine Rn (Rn will contain RXP6 after an error)
2. Examine RXP6 by:
 - Loading the READ ERROR REGISTER command into RXP05 (77710/XXXXXXXX 17 0000)
 - Examining the four words of error information that will be transferred into locations 2000, 2002, 2004, and 2006.
 - Reading and decoding this information using the format shown below. The error code can be used to help identify the failing FRU.



RX2CS (Former RXV24)

Bit Definitions

Bit	Function																		
11	Go - Initiates a command to RX02. Write only.																		
1-10	Function Select - These bits code one of the eight possible functions described below. Write only. <table> <thead> <tr> <th>Code</th><th>Function</th></tr> </thead> <tbody> <tr> <td>000</td><td>Fill Buffer</td></tr> <tr> <td>001</td><td>Empty Buffer</td></tr> <tr> <td>010</td><td>Write Sector</td></tr> <tr> <td>011</td><td>Read Sector</td></tr> <tr> <td>100</td><td>Set Media Density</td></tr> <tr> <td>101</td><td>Read Status</td></tr> <tr> <td>110</td><td>Write Deleted Data Sector</td></tr> <tr> <td>111</td><td>Read Error Code</td></tr> </tbody> </table>	Code	Function	000	Fill Buffer	001	Empty Buffer	010	Write Sector	011	Read Sector	100	Set Media Density	101	Read Status	110	Write Deleted Data Sector	111	Read Error Code
Code	Function																		
000	Fill Buffer																		
001	Empty Buffer																		
010	Write Sector																		
011	Read Sector																		
100	Set Media Density																		
101	Read Status																		
110	Write Deleted Data Sector																		
111	Read Error Code																		
4	Unit Select - This bit selects one of the two possible disks for execution of the desired function. This bit is readable only when done is set, at which time it indicates the unit previously selected. Read/write.																		
5	Done - This bit indicates the completion of a function. Done will generate an interrupt when asserted if interrupt enable (RX2CS bit 6) is set. Read only.																		
6	Interrupt Enable - This bit is set by the program to enable an interrupt when the RX02 has completed an operation (done). The function of this bit is normally determined at the time a function is initiated. Read/write; cleared by initialize.																		
7	Transfer Request - This bit signifies that the RXV24 needs data or has data available. Read only.																		
8	Density - This bit determines the density of the function to be executed. This bit is readable only when done is set, at which time it indicates the density of the function previously executed. Read/write.																		

Bit Definitions (Cont)

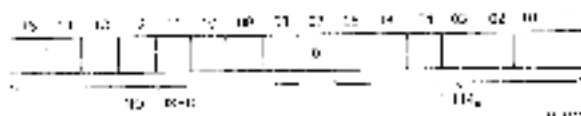
Bit	Function
9	Head Select - This bit selects one of two heads for position-sized operation, readable only when done is set. At that time the side that was previously selected is not valid.
10	Reserved for future use. Must be written as a 0.
11	RXC02 - This bit is set by the interface to inform the programmer that this is an RX02 system. Read only.
12-13	Extended Address - These bits are used to declare an extended bus address. Write only.
14	RXV21 Initialize - This bit is set by the program to initialize the RXV21 without initializing all devices on the UNIBUS. Write only.

CAUTION

Loading the lower byte of the RX2CS will also load the upper byte of the RX2CS.

Upon setting this bit in the RX2CS, the RXV21 will negate done and move the read position mechanism of both drives (if two are available) to track 0. Upon completion of a successful initialize, the RX02 will zero the error and status register, and set initialize done. It will also read sector 1 of track 1 on drive 0 into the buffer.

- 15 Error - This bit is set by the RX02 to indicate that an error has occurred during an attempt to execute a command. Read only; cleared by the initiation of a new command or an initialize.



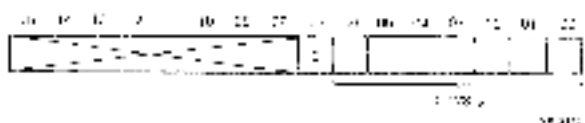
RX2TA Format (RXV21)

RX2TA (RX Track Address) - This register is loaded to indicate on which of the 114₀ (0-78₁₅) tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8-15 are unused and are ignored by the control.



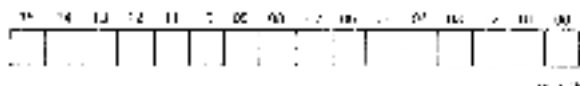
RX2SA Format (RXV21)

RX2SA (RX Sector Address) – This register is loaded to indicate on which of the 32₈ (1-25₅) sectors a given function is to operate. It can be addressed only under the protocol of the function in progress.



RX2WC Format (RXV21)

RX2WC (RX Word Count Register) – For a double density sector, the maximum word count is 128₈. For a single density sector the maximum word count is 64₈. If a word count is beyond the limit for the density indicated, the control asserts word count overflow (bit 10 of RX2ER). This is a write-only register. The actual word count, and not the 2's complement of the word count, is loaded into the register.



RX2BA and RX2DB Format (RXV21)

RX2BA (RX Bus Address Register) – This register specifies the bus address of data transferred during fill buffer, empty buffer, and read definitive error operations. Incrementation takes place after a memory transaction has occurred. The RX2BA, therefore, is loaded with the address of the first data word to be transferred. This is a 16-bit, write-only register.

RX2DB (RX Data Buffer) – All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.

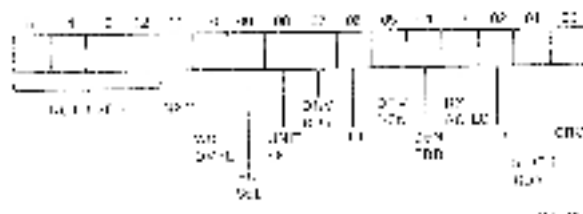
RX2DB (Data Buffer Register (17/172)) – This register serves as a general purpose data path between the RX02 and the interface. It may represent one of six RX02 registers according to the protocol of the function that is in progress.

RXV21/M8029

This register is read/write if the RXD2 is not in the process of executing a command; that is, it may be manipulated without affecting the RXD2 sub-system. If the RXD2 is actively executing a command, this register will only accept data if RX2CS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

CAUTION

Violation of protocol in manipulation of the data buffer register may cause permanent data loss.



RX2ES Format (RXV21)

RX2ES (RX Error and Status) – This register contains the current error and status conditions of the drive selected by bit 4 (unit select) of the RX2CS. This read-only register can be addressed only under the protocol of the function in progress. The RX2ES is located in the RXD2B upon completion of a function.

RXES bit assignments are as follows.

Bit Definitions

Bit	Function
0	CRC Error – A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The data collected must be considered invalid. The RX2ES is moved to the RXD2B, and error and done are asserted. It is suggested that the data transfer be tried up to 10 times, as most errors are recoverable (soft).
1	Side 1 Ready – This bit, when set, indicates that a double-sided diskette is mounted in a double-sided drive and is ready to execute a function. This bit is valid only at the termination of an initialize sequence or a maintenance READ STATUS command.

Bit Definitions (Cont.)

Bit	Function
2	Initialize Done - This bit is asserted in the RX2EG to indicate completion of the initialize routine which can be caused by RX02 power failure, system power failure, or programmable or hard initialize.
3	RX AC LO - This bit is set by the interface to indicate a power failure in the RX02 subsystem.
4	Density Error - This bit indicates that the density of the lunel on in progress does not match the drive density. Upon detection of this error the control terminates the operation and asserts error and done.
5	Drive Density - This bit indicates the density of the diskette in the drive selected (indicated by bit 6). The density of the drive is selected during read and write sector operations.
6	Deleted Data - This bit indicates that in the course of recovering data, the "deleted data" address mark was detected at the beginning of the data field. The DRV DFM bit indicates whether the mark was a single- or double-density colored data address mark. The data following the mark will be collected and transferred normally, as the deleted data mark has no further significance other than to establish drive density. Any alteration of files or actual deletion of data due to this mark must be accomplished by user software.
7	Drive Ready - This bit indicates that the selected drive is ready if bit 7 = 1 and all conditions for disk operation are satisfied, such as door closed, power OK, diskette up to speed, etc. The RX02 may be presumed to be ready to perform any operation. This bit is only valid when retrieved via a read status function or initialize.
8	Unit Select - This bit indicates that drive 0 is selected if bit 8 = 0. This bit indicates the drive that is currently selected.
9	Head Select - This bit indicates which side of a double-sided drive performed the last operation.
10	Word Count Overflow - This bit indicates that the word count is beyond sector size. The fill or empty buffer operation is terminated and error and done are set.
11	Nonexistent Memory Error - This bit is set by the interface when a DMA transfer is being performed and the memory address specified in RX2RA is nonexistent.

Function Codes

Following the strict protocol of the individual function, data storage and recovery on the RXV21 occur with careful manipulation of the RX2CS and RX2DB registers. The penalty for violation of protocol can be permanent data loss.

A summary of the function codes is presented below:

000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Set Media Density
101	Read Status
110	Write Deleted Data Sector
111	Read Error Code

The following paragraphs describe in detail the programming protocol associated with each function encoded and written into RX2CS bits 1-3 if code is set.

Fill Buffer (000) - This function is used to fill the RX2D data buffer with the number of words of data specified by the RX2WC register. Fill buffer is a complete function in itself; the function ends when RX2WC overflows, and if necessary, the control has zero-filled the remainder of the buffer. The contents of the buffer may be written on the disk by means of a subsequent WRITE SECTOR command or returned to the host processor by an EMPTY BUFFER command. If the word count is too large, the function is terminated, error and done are asserted, and the word count overflow bit is set in RX2EB.

To initiate this function the RX2CS is loaded with the function. Bit 4 of the RX2CS (unit select) does not affect this function since no disk operation is involved. Bit 3 (density) must be properly selected since this determines the word count limit. When the command has been loaded, the done bit (RX2CS bit 6) goes false. When the TR bit is asserted, the RX2WC may be loaded into the data buffer register. When TR is again asserted, the RX2BA may be loaded into the RX2DB. The data words are transferred directly from memory and when RX2WC overflows and the control has zero filled the remainder of the sector buffer, if necessary, done is asserted, ending the operation. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated. Any read of the RX2EB during the data transfer is ignored by the interface. After done is true, the RX2EB is loaded in the RX2DB register.

Empty Buffer (001) - This function is used to empty the contents of the internal buffer through the RXV21 for use by the host processor. This data is in the buffer as the result of a previous FILL BUFFER or READ SECTOR command.

The programming protocol for this function is identical to that for the **FILL BUFFER** command. The **RX2CB** is loaded with the command to initiate the function. (This function will ignore bit 4 **RX2CB**, not select.) **RX2CB** bit 6 (density) must be asserted to allow the proper word count limit. When the command has been loaded, the done bit (**RX2CB** bit 5) goes false. When the **TR** bit is asserted, the **RX2WC** may be loaded into the **RX2DB**. When **TR** is again asserted the **RX2BA** may be loaded into the **RX2DB**. The **RXV21** assembles one word of data at a time and transfers it directly to memory. Transfers occur until word count overflow, at which time the operation is complete and done goes true. If bit 8 (**RX2CB** Interrupt enable) is set, an interrupt is initiated. After done is true, the **RX2EB** is located in the data buffer register.

Write Sector (010) - This function is used to locate a desired sector on the diskette and fill it with the contents of the internal buffer. The initiation of the function clears **RX2EB**, **TR**, and done.

When **TR** is asserted, the program must load the desired sector address into **RX2UB**, which will drop **TR**. When **TR** is again asserted, the program must load the desired track address into the **RX2UR**, which will drop **TR**. **TR** will remain unasserted while the **RX02** attempts to locate the desired sector. The diskette density is determined at this time and is compared with the function density. If the densities do not agree, the operation is terminated; bit 4 **RX2CB** is set, **RX2CB** is moved to the **RX2DB**, error (bit 15 **RX2CB**) is set, done is asserted, and an interrupt is initiated, if bit 8 **RX2CB** (interrupt enable) is set.

If the densities agree but the **RX02** is unable to locate the desired sector within two diskette revolutions, the interface will again the operation, move the contents of **RX2CB** to the **RX2DB**, set error (bit 15 **RX2CB**), assert done, and initiate an interrupt if bit 8 **RX2CB** (interrupt enable) is set.

If the desired sector has been reached and the densities agree, the **RXV21** will write the 128₁₀ or 144₁₀ words stored in the internal buffer followed by a CRC character which is automatically calculated by the **RX02**. The **RXV21** ends the function by asserting done and, if bit 8 **RX2CB** (interrupt enable) is set, initiating an interrupt.

CAUTION

The contents of the sector buffer are not valid data after a power loss has been detected by the **RX02**. However, write sector will be accepted as a valid instruction and the (random) contents of the buffer will be written, followed by a valid CRC.

NOTE

The contents of the sector buffer are not destroyed during a write sector operation.

Read Sector (011) – This function is used to locate the desired sector and transfer the contents of the data field to the internal buffer in the control. This function may also be used to retrieve rapidly (5 ms) the current status of the drive servomotors. The initiation of this function clears RX2HS, TR, and done.

When TR is asserted the program must load the desired sector address into the RX2DH, which will drop TR. When TR is again asserted, the program must load the desired track address into the RX2DB, which will drop TR.

TR and done will remain negated while the RX02 attempts to locate the desired sector. If the RX02 is unable to locate the desired sector within two diskette revolutions for any reason, the RXV21/RX211 will abort the operation, set done and error (bit 15 RX2CS), move the contents of the RX2FS to the RX2DG, and if bit 6 RX2CS (interrupt enable) is set, initiate an interrupt.

If the desired sector is successfully located, the control reads the data address mark and determines the density of the diskette. If the diskette (drive) density does not agree with the function density the operation is terminated and done and error (bit 15 RX2CS) are asserted. Bit 4 RX2ES is set (density error) and the RX2FS is moved to the RX2DH. If bit 6 RX2CS (interrupt enable) is set, an interrupt is initiated.

If a legal data mark is successfully located, and the control and density agree, the control will read data from the sector into the internal buffer. If a deleted data address mark was detected, the control will set bit 8 RX2ES (DD). As data enters the internal buffer, a CRC is computed based on the data field and the CRC bytes previously recorded. A nonzero residue indicates that a read error has occurred and the control sets bit 0 RX2ES (CRC error) and bit 15 RX2CS (error). The RXV21 ends the operation by asserting done and moving the contents of the RX2FS into the RX2DH. If bit 6 RX2CS is set, an interrupt is initiated.

If the desired sector is successfully located, the densities agree and the data is transferred with no CRC error, done will be set and if bit 6 RX2CS (interrupt enable) is set, the RXV21 will also an interrupt.

Set Media Density (100) – This function causes the current diskette to be reassigned to a new density. Bit 11 RX2CS (density) indicates the new density. The control reformats the diskette by writing new data address marks (double or single density) and zeroing all of the data fields on the diskette.

The function is initiated by loading the RX2CS with the command. Initiation of the function clears HX2ES and done. When TR is set, an ASCII 0 (1111) must be loaded into the RX2DB to complete the protocol. This extra character is a safeguard against an error in loading the command. When the control recognizes this character it begins executing the format.

The control starts at sector 1, track 0 and reads the header information, then starts a write operation. If the header information is damaged, the control will abort the operation.

If the operation is successfully completed, done is set and bit 6 (RX2CS interrupt enable) is set, an interrupt is initiated.

CAUTION

This operation takes about 15 seconds and should not be interrupted. If for any reason the operation is interrupted, an illegal diskette will be generated which may have data marks of both densities. This diskette should be completely reformatted.

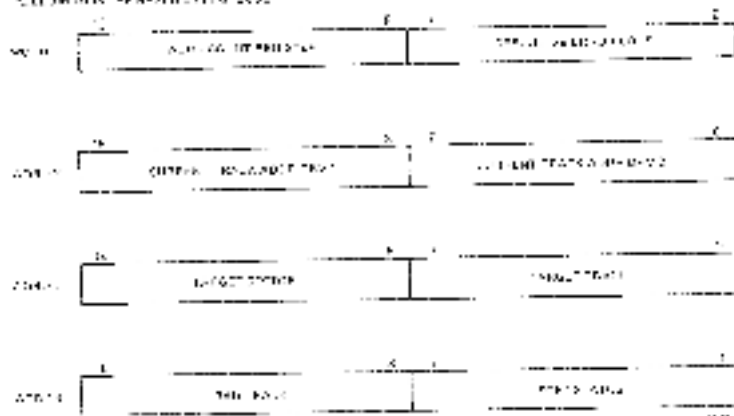
Maintenance Read Status (107) – This function is initiated by loading the HX2CS with the command. Done is cleared. The drive ready bit (bit 7 RX2ES) is updated by counting index pulses in the control. The drive density is updated by loading the head of the selected drive and reading the first data mark. The RX2ES is moved into the RX2DB. The RX2CS may be sampled when done (bit 6 RX2CS) is again asserted and if bit RX2CS (interrupt enable) is set, an interrupt will occur. This operation requires approximately 250 ms to complete.

Write Sector with Deleted Data (110) – This operation is identical to function 010 (write sector) with the exception that a deleted data address mark is written preceding the data rather than the standard data address mark. The density bit associated with the function indicates whether a single- or double-density deleted data address mark will be written.

Read Error Code (111) – The read error code function implies a read exception status. In addition to the specific error code, a dump of the control's internal scratch pad registers also occurs. This is the only way that the word count register can be retrieved. This function is used to retrieve specific information as well as drive status information depending upon detection of the general error bit.

The transfer of the registers is a DMA transfer. The function is initiated by loading the RX2CS with the command; then done goes false. When TR is true, the RX2BA may be loaded into the RX2DB and TR goes false. The registers are assembled one word at a time and are then transferred directly to memory.

SLEW/SEARCH - SEARCH FOR TRACK



Definitive Error Codes

- 10 Drive 0 failed to see home on initialize.
- 20 Drive 1 failed to see home on initialize.
- 40 Tried to access a track greater than 76.
- 50 Home was found before desired track was reached.
- 70 Desired sector could not be found after 57 tries.
- 110 More than 40 μ s and no SEP clock seen.
- 120 A preamble could not be found.
- 130 A preamble found but no ID mark found within allowable time.
- 150 The track address of a good header does not compare with desired track.
- 180 Too many tries for IDAM.
- 170 Data was not found in allotted time.
- 200 CRC on reading the sector from the disk.
- 220 Failed maintenance wraparound check.
- 230 Word count overflow.

240	Density error.
250	Incorrect key word on SET DENSITY command.

Register Protocol

Word 1<7:0>	Definitive error codes
Word 1<15:0>	Word count register
Word 2<7:0>	Current track address of drive 0
Word 2<15:8>	Current track address of drive 1
Word 3<7:0>	Target track of current disk access
Word 3<15:8>	Target sector of current disk access
Word 4<7>	Unit select bit*
Word 4<5>	Head load bit†
Word 4<8> <7>	Drive density bit or both drives*
Word 4<0>	Bitary of READ ERROR REGISTER command*
Word 4<10:8>	Track address of selected drive**

RX02 Power Fail or Initialize

When the RX02 control senses a loss of power within the RX02, it will un-load the head and short all control action. The RXACL line is asserted to indicate to the RXV21 that subsystem power has gone. The RXV21 asserts done and error and sets the RXACL bit in the RXES.

When the RX02 senses the return of power, it will remove done and begin a sequence to:

1. Move each drive head position mechanism to track 0
2. Clear any active error bits
3. Read sector 1 of track 1, on drive 0
4. Assert initialize done in the RXES

Upon completion of the power up sequence, done is again asserted. There is no guarantee that information being written at the time of a power failure will be retrieved; however, all other information on the disks will remain unaltered.

-
- * For DMA operation, the controller status soft register is sent to the interface at the end of the command. The four status bits are included in an 8-bit word. Unit select = bit 7; density of drive 1 = bit 6; head load = bit 5; density of drive 0 = bit 4; density of READ ERROR REGISTER command = bit 0.
 - ** The track address of the selected drive-error is only meaningful on a code 130 error. The register contains the address of the cylinder that the head reached on a seek error.

TSV05 TAPE TRANSPORT AND BUS INTERFACE/CONTROLLER

GENERAL

The TSV05 tape transport subsystem provides magnetic tape storage capabilities to computer systems using quad-sized LSI-11 bus backplanes. The subsystem reads or writes up to 160,000 bytes per second in ANSI standard format. Data is recorded by phase encoding 1600 bits per inch on nine-track tape. Reading and writing are performed at either 25 or 100 inches per second.* The TSV05 subsystem is hardware compatible with 18- and 22-bit addressing versions of the LSI-11 bus quad backplane. It is software compatible with system and application programs written for the TSV11 tape transport subsystem (as long as such programs use the DIGITAL-supplied device handler). Tape formatting, error detection and correction, and self-test diagnostics are included as integral components of the TSV05 subsystem.

Voltage	Bus Loads	
	AC	DC
+5 V _{cc} @ 5.6 A (max.)	3.0 (max.)	1

Standard Addresses

772620/772622	1st unit
772624/772626	2nd unit
772630/772632	3rd unit
772634/772636	4th unit

Vectors

094	1st unit
--	2nd unit
--	3rd unit
--	4th unit

* 100 IPS operating speed requires enabling special features and the appropriate software.

** Bank of 32 in one floating vector area starting at 300.

Diagnostic Programs

CVT5AA	Logic Test
CVT5BA	Advanced Logic Test
CVT5CA	Transport Test
CVT5DA	Advanced Transport Test
CVT5EA	Data Reliability Test
X15AA0	500-X11

Related Documentation

TSV05 Tape Transport Pocket Service Guide (EK-TSV05-PS)
Operation and Maintenance Instructions for Model F800 Tape Transport (799876-000)
TSV05 Tape Transport Subsystem Installation Manual (EK-TSV05-IM)
XXDP User Guide (AC 90931 MG)
TS05 Tape Transport Operation and Acceptance Preventive Maintenance Remove/Replace (CY-DQ142-P6)
 TSV05 Field Print Set (MF-01167)
TSV05 Subsystem Technical Manual (EK-TSV05-TM)
Microcomputers and Memories (CB-13451-20)
Microcomputer Interfaces Handbook (CB-17725-20)

TSV05 Hardware

T305 tape transport

M7106 LSI-11 bus interface/controller module

H9042-series cabinet, including 3/4 power controller and remote power control cable

Pair of 7010062 bus cables for connecting tape transport input and output to the bus interface/controller module

The bus interface/controller module plugs into the LSI-11 bus. The two cables connect the module with the tape transport.

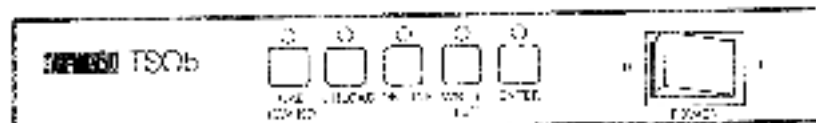
	Nominal, Vdc	Low Limit, Vdc	High Limit, Vdc
TSV05 5A	120	102	128
TSV05 5B	240	204	256
TSV05 5D	220	187	235

Electromagnetic Interference (EMI)

The TSV05 subsystem complies with FCC Part 15, Subpart J, Class A and is designed to comply with VDE 0871-D requirements.

NOTE

The TSV05 subsystem has been designed and tested to meet DIGITAL standards, including FCC requirements. The specifications in this chapter are based on this testing. DIGITAL cannot guarantee the TSV05 subsystem will meet these specifications if nontested equipment is installed into the TSV05 cabinet or the TSV05 cabinet is installed in nontested configurations.



Operator Front Panel

Controls and Indicators

Control/ Indicator	Type	Function
POWER	ON/OFF rocker switch and indicator	Switches the power ON and OFF.
LOAD REWIND	Tactile switch and indicator	1. Blinks when the tape drive is executing a load or unload sequence. 2. Lit continuously when the beginning of tape (BOT) marker is sensed. 3. Pressing the switch: a. Initiates load sequence and advances tape to load point. b. Rewinds the tape to load point.
UNLOAD	Tactile switch and indicator	1. Pressing the switch causes the tape to be unloaded regardless of tape position. 2. Blinks when the tape drive is executing an unload sequence. 3. Lit continuously when the tape drive has completed its unload sequence and the front access door is unlocked. At this time, the tape may be removed and another tape inserted into the drive. 4. Lit continuously after a successful power up, indicating a tape may be loaded.

Controls and Indicators (Cont)

Control/ Indicator	Type	Function
ON-LINE	Tactile switch and Indicator	1. Lit when drive is ready and on line 2. Pressing the switch: a. Takes the tape drive on-line and extinguishes the indicator. b. Puts the tape drive on-line and lights the indicator.
NOTE Pressing the switch during a load sequence puts the tape drive on-line when the SQT marker is sensed.		
TEST	Tactile switch	Operational only in the test mode. Selects alternative operational mode for other switches.
WRITE	Indicator	1. Lit when the write ring is installed and data may be written on tape. 2. When indicator is off, write ring is not installed and tape is file protected.
ENTER	Tactile switch	This control is used for manual loading and controlling the test mode.

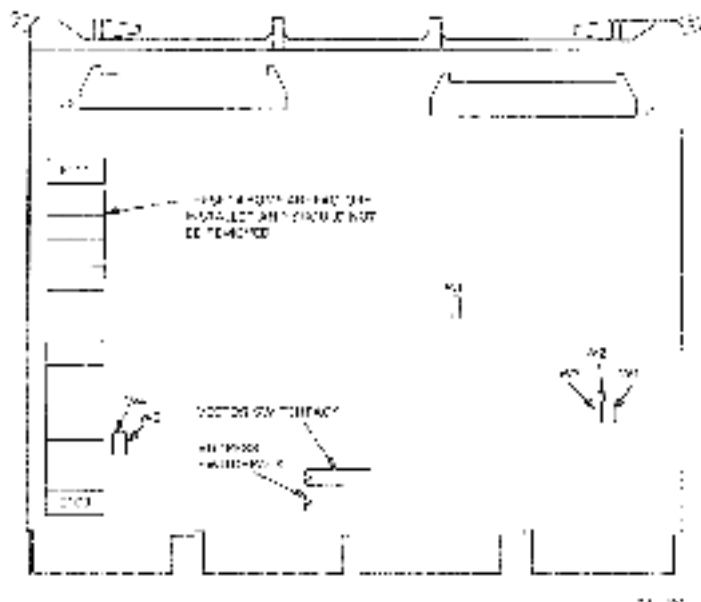


FIG. 1 - JUMPER IDENTIFICATION

	1	2	3	4	5	6	7	8	9	10	
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	SW

FIG. 2 - JUMPER IDENTIFICATION

	1	2	3	4	5	6	7	8	9	10	
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	SW

SW - JUMPER SWITCH
A1 - JUMPER 1

SW - JUMPER SWITCH
A1 - JUMPER 1

SW - JUMPER SWITCH

SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

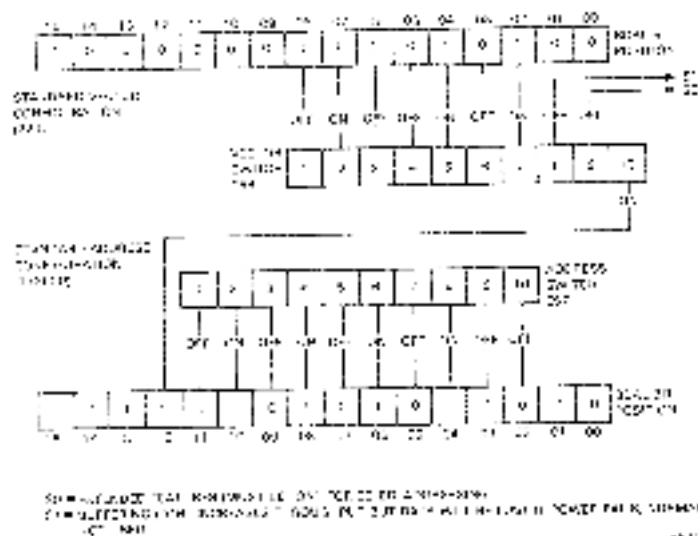
SW - JUMPER SWITCH

SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
SW	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10

SW - JUMPER SWITCH

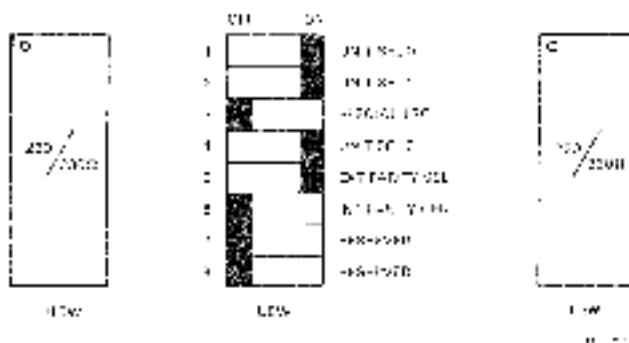
M7196 Switch and Jumper Identification

VARIABLES AND ADDRESS SWITCHES





TOP TIGHTENING UNIT SELECT GAGE



Transport Switch and Terminator identification

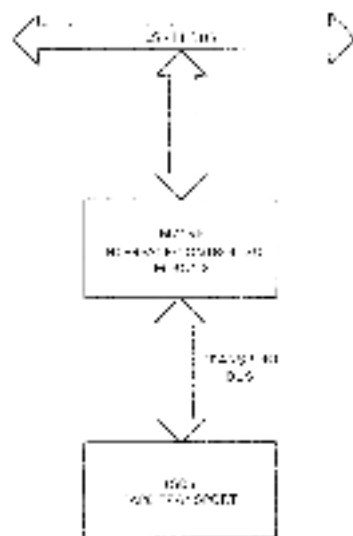
NOTE	PLUG	RECEPT	CABLE RECEPT
FIG. 10	LINE NEUTRAL GROUND	LINE NEUTRAL GROUND	LINE NEUTRAL GROUND

FIG. 10

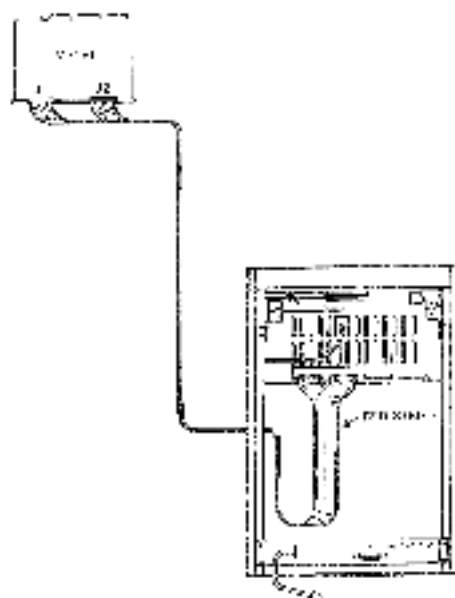
Power Line Connections

Power Line Connections

Power Cord Color Code		Pin connection	
Color	Function	L5-30P	6-15P
Brown	Hot	Brass	Brass 1
Blue	Neutral	Silver	Brass 2
Green/yellow	Ground	Ground	Ground

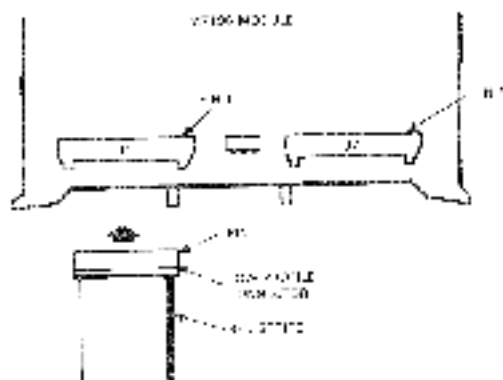


• 4. 214

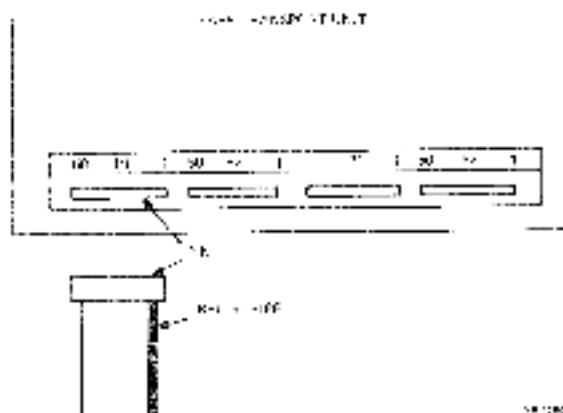


• **1990**

Matlab Interconnectivity



Cabling the M7196 Module



Cabling the Tape Transport

VSV11 RASTER GRAPHICS SYSTEM

GENERAL

The VSV11 raster graphics system is a basic O-Bus system designed for color graphics operation with LS-11 hosts.

This raster graphics module set is installed in a LS-11 bus and a Color console.

The first slot is reserved for either a CPU module or a connector which extends the O-Bus from another backplane. If slot 1 contains a CPU module, jumpers W1 and W2 must be removed in an H8273-A backplane used in a BA11-B mounting box. Rows C and D carry the video bus signals of the VSV11 system. This is modified for 22-bit bus addressing (backplanes H8273 and I-9276).

The basic module set includes:

- M7061-YA SYNC generator module
- M7062 image memory
- M7064 display processor module

Power Requirements

1. AC Power — The VSV11 system has one ac load, that being the M7064 (display process module), which is the only module in the VSV11 system that communicates with the CPU.
2. DC Power — To determine how many dc loads a VSV11 system has, count the number of VSV11 modules (M7061, M7062, M7064) that reside on the LS11 bus. The total number is the number of dc loads. For example, a VSV11-A11 consists of:

- 1-M7061
- 2-M7062
- 1-M7064

4=dc loads

VSV11/M7061,2,4

Module

M7061	-5 V @ 2.8 A -12 V @ 0.11 A
M7062	-5 V* @ 0.005 A 10 V @ 1.7 A +12 V @ 0.45 A
M7064	-5 V @ 6.0 A

Standard Device Address

767010

Vendor

722 (0016)

Diagnostic Program

GVVSA?

Related Documentation

VSV11 Raster Graphics System User Guide (EK-VSV11-UG)

DA11 Installation Guide (EK-DA11-A-IG)

VSV11 Field Maintenance Print Set (MP-0101?)

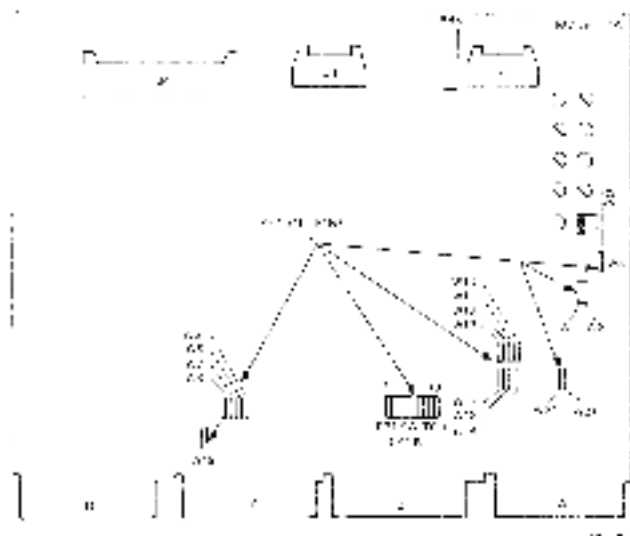
VT102 Hitachi Monitor Maintenance Manual

VT101 Series Technical Manual (EK-VT101-1M)

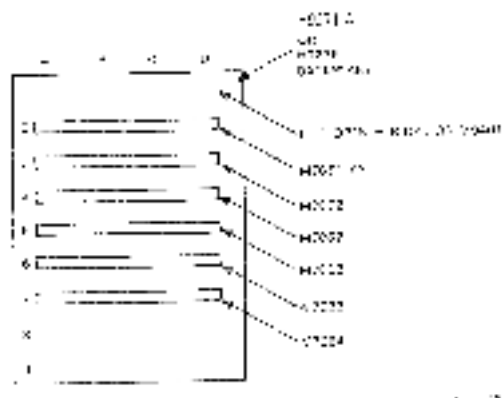
*Supplied by M7061 module

M7051-YA SYNC GENERATOR/CURSOR CONTROL BOARD

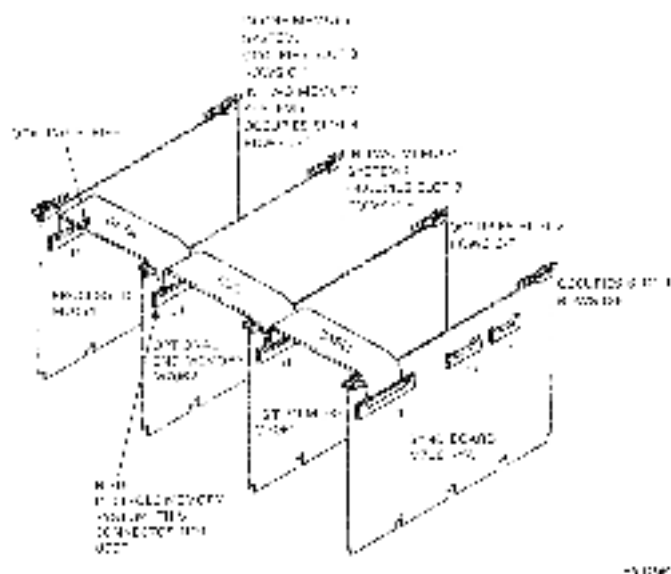
Jumpers and switches are configuration dependent and are located as shown.



M7051-YA Switches and Jumpers



Module Placement Example, Fair (Extended) Memory Systems

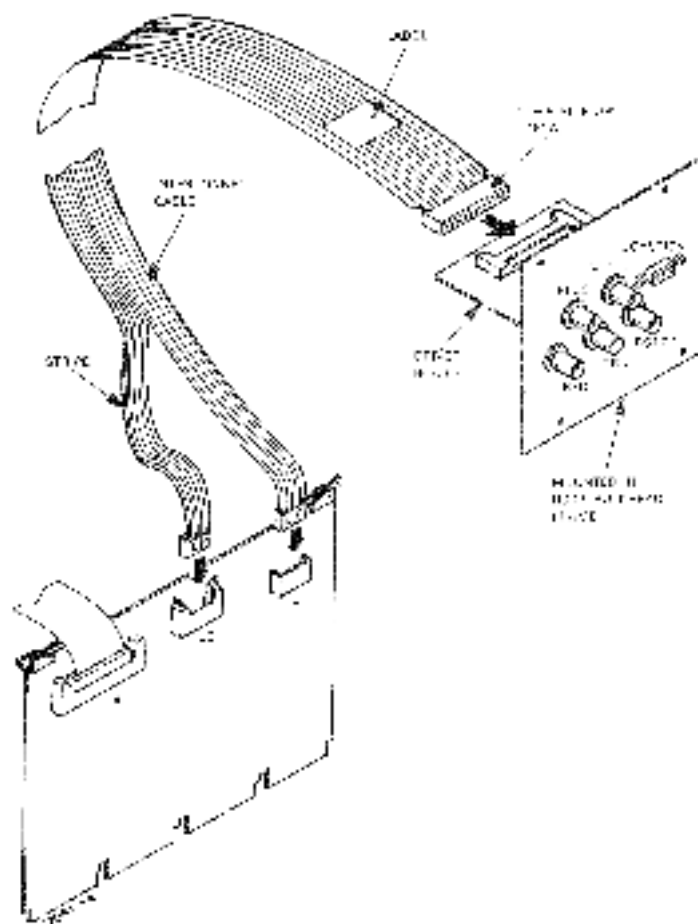


Intermodule Cabling Example, One of Two Memory Systems

M7061-YA Cable Connectors

The three cable connectors located on the M7061-YA module are:

- J1 - Accepts the drive board cable
- J3 - Accepts the driver board cable with the red stripe toward J4
- J4 - Accepts the beginning end of the daisy chain to memories and display processor.



M7061-YA Interconnecting Cable

1011

M7061: TA Switch Selections

Selection	Switch Settings		
	E21-1	E21-2	
50 Hz	OFF	ON	
60 Hz	ON	OFF	
Interlocked* Noninter-locked Special	E21-3	E21-8	
	OFF	ON	
	ON	ON	
Normal Scan* Special Scan	E21-4	E21-5	
	OFF	ON	
Master* Slave	E21-6		
	ON		
External Sync[] Internal Sync[]	E21-7	E21-9	E21-10
	ON	OFF	OFF
	OFF	ON	ON

*These are factory settings.

[] Use external sync when doing adjustments.

M7061-7A Jumper Selections

Selection	Jumper State			
	W19			
Master*	IN			
Slave	OUT			
	W6			
External Sync†	IN			
Internal Sync	OUT			
	W5	W5	W7	W9
Channel 0	OUT	IN	OUT	IN
Channel 1	OUT	IN	IN	OUT
Channel 2	IN	OUT	OUT	IN
Channel 3	IN	OUT	IN	OUT
	W10	W11		
White Cursor*	IN	IN		
Green and Blue Cursor	IN	OUT		
Green and Red Cursor	OUT	IN		
Green Cursor*	OUT	OUT		
	W16	W17		
Small Cursor*	IN	IN		
Large Cursor	OUT	OUT		
	W21	W22		
16 Shades/Colors	OUT	IN		
8 Shades/Colors	IN	OUT		

*These are factory settings.

VSV11/M7061,2,4

VSV11 Module M7051-7A ~ E21 Factory Switch Settings

Selection	E21 Switch No.										Customer Selection
	1	2	3	4	5	6	7	8	9	10	
60 Hz	OFF ON										
50 Hz	ON OFF										
Interfaced*			OFF							ON	
Noninterfaced			ON							ON	
Speeds			OFF							OFF	
Norm Scan†					OFF ON						
Special Scan					ON OFF						
Master†							ON				
Slave							OFF				
External Sync†							ON OFF		OFF		
Internal Sync							OFF ON		ON		

*These are factory settings

VSV11/M7061,2,4

VSV11 Module M7061-VA Factory Set Jumper W - States

Selection	Jumper W												Customer	
	3	5	6	7	8	10	11	16	17	19	21	22	Selection	
Master *										I				
Slave										O				
Extensl Sync	I													
Internal Sync		O												
Channel 0		O	I	O	I									
Channel 1		O	I	I	O									
Channel 2		I	O	O										
Channel 3		I	O	I	O									
White Cursor*						I	I							
Gr-HI Cursor						I	O							
Gr+Hd Cursor						O	I							
Green Cursor						O	O							
Small Cursor*								I	I					
Large Cursor								O	O					
16 Colors*											O	I		
8 Colors											I	O		

* These are factory settings

O = Out

I = In

**M7062 E40 and E55 Switch Settings* and
E78,77 Terminator Configuration**

SW	One Memory		Two Memories		Four Memories			
	Non-inter-laced	Inter-laced	1st	2nd	Channel 0		Channel 1	
			1st	2nd	1st	2nd	3rd	4th
1	OFF	ON	ON	ON	ON	ON	ON	ON
2	OFF	ON	ON	ON	ON	ON	ON	ON
3	ON	ON	ON	OFF	ON	OFF	ON	OFF
4	ON	ON	ON	OFF	ON	OFF	ON	OFF
5	ON	OFF	OFF	ON	OFF	ON	OFF	ON
6	ON	OFF	OFF	ON	OFF	ON	OFF	ON
7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
THM								
76	IN	IN	IN	OUT	IN	OUT	OFF	OFF
77	IN	IN	IN	OUT	N	OUT	OUT	OUT

*Note that both switches are set identically.

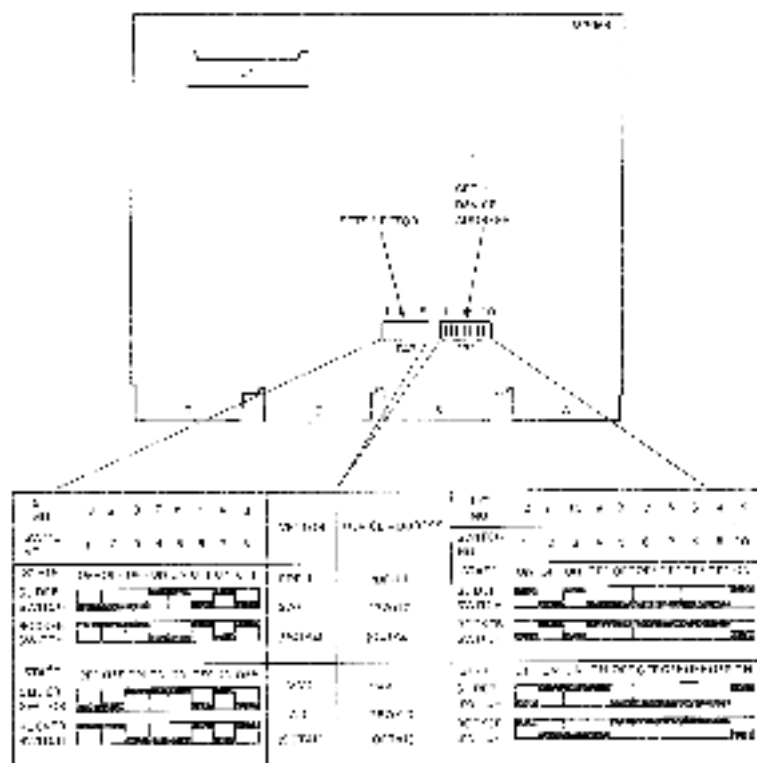
-Always remove end out pin 0 and re-install when IN.

M7062 Jumper Selections

W-	One Memory	Two Memories	Channel 0	Four Memories Channel 1
1	IN	IN	IN	IN
2	IN	IN	IN	IN
3	OUT	OUT	OUT	OUT
4	OUT	OUT	OUT	IN
5	IN	IN	IN	IN
6	IN	IN	IN	OUT

M7054 DISPLAY PROCESSOR MODULE

The M7064 display processor module controls transactions between the control logic and the LSI-11 bus logic. Switches on this module accommodate the host system.



Address and Vector Switch Settings for Module M7004

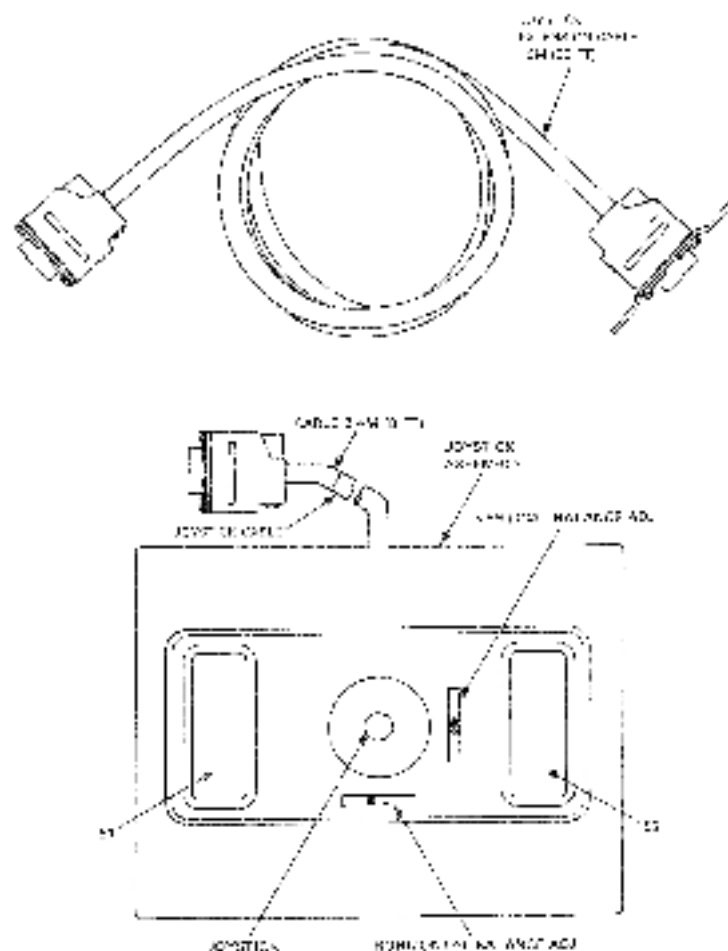
Install the sync generator module (M7061-YA) in slot 2 with either the GPU module or an M9401 bus extender card occupying slot 1. Next, insert the M7062 memory module(s) (up to 4). The last module to be inserted is the M7064 display processor module, next to the last memory module.

VSV11 Module M7064 - Switch Settings

Selection	System	Order	Switch Pack	No.	Factory Setting	Customer
Vector	PDP-11	320	E43	1	OFF	
				2	OFF	
				3	OFF	
				4	ON	
				5	ON	
				6	OFF	
				7	ON	
				8	OFF	
	VAX	720	E43	1	OFF	
				2	OFF	
				3	ON	
				4	ON	
				5	ON	
				6	OFF	
				7	ON	
				8	OFF	
Device Address	PDP-11	772010	E81	1	ON	
				2	OFF	
				3	ON	
				4	OFF	
				5	OFF	
				6	OFF	
				7	OFF	
				8	OFF	
				9	OFF	
				10	ON	
	VAX	787010	E81	1	OFF	
				2	ON	
				3	ON	
				4	ON	
				5	OFF	
				6	OFF	
				7	OFF	
				8	OFF	
				9	OFF	
				10	ON	

Task Module 5 – Joystick

The joystick is used in this system to move and mark the cursor on the screen. The equipment to be installed consists of the joystick itself, its cable, and an extension cable as shown below:

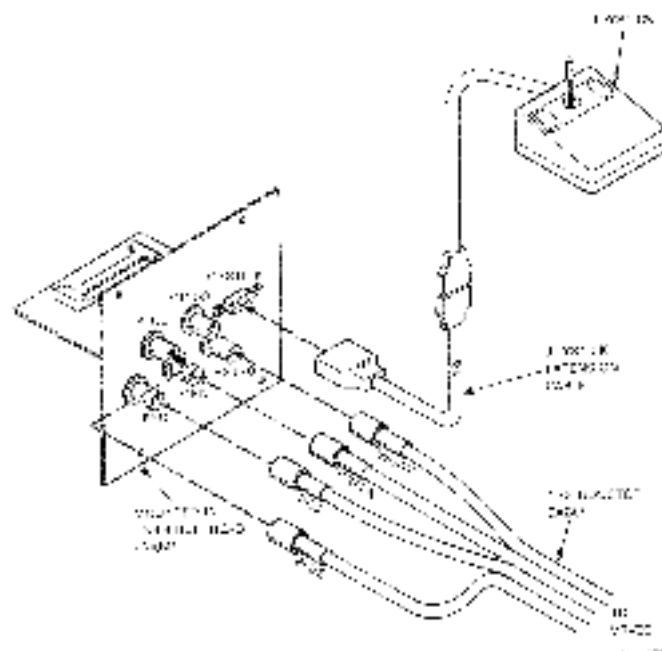


Joystick Components

CAUTION

Never connect the joystick to a system while power is on. To do this can damage the M7061-VA Sync Gen/Control Card module.

Shown below are the joystick and 4-conductor cable connections.



Joystick Installation and 4-Conductor Cable Connection

RC25 8-INCH DISK DRIVE SUBSYSTEM

GENERAL

The RC25 is a self-contained mass storage device that is used with a host to store up to 62 million characters on two, hard, 8-inch disk platters.

One disk platter is fixed and the other is removable. Both platters are mounted on the same spindle. The RC25 is available as a table top or rack mounted subsystem. The two types of RC25 units are the master and the slave. The disks on the master and slave units are interchangeable.

The master, containing the controller module, can drive two spindles (one master and one slave), and must be the first drive in a subsystem.

Related Documentation

RC25 Disk Subsystem User Guide (FK-0RC25-UG)

RC25 Slave Disk Drive Customer Installation Guide (FK-0RC25-IG)

RC25 Disk Subsystem Installation Guide (FK-0RC25-IN)

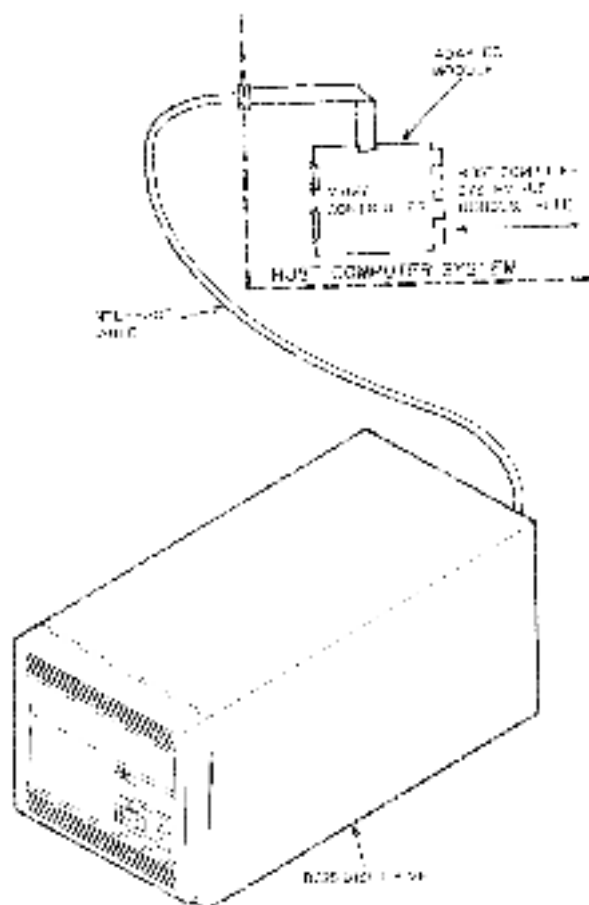
RC25 Disk Subsystem Pocket Service Guide (FK-0RC25-PG)

Illustrated Parts Breakdown (FK-0RC25-IP)

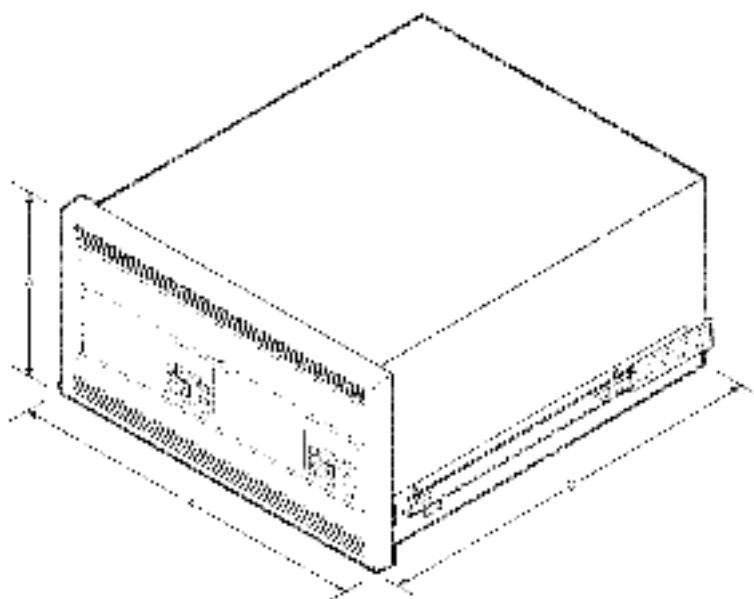
RC25 Field Maintenance Print Set (MF-01612-00)

MSCP Basic Disk Functions Manual (AA-1619A-FK)

Storage Systems IBM/ESA Port Descriptor (AA-1601A-FK)



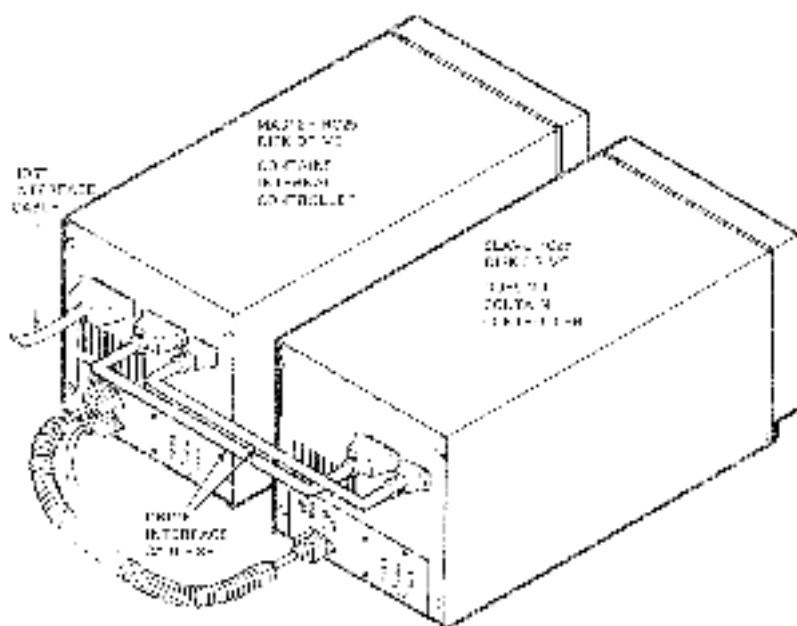
RC25 Disk Subsystem Components



UNIT WEIGHT	COMPONENTS	WEIGHT
1. RACK 1	222	17.5
2. RACK 2	14.5	11.1
3. RACK 3	96.7	7.7

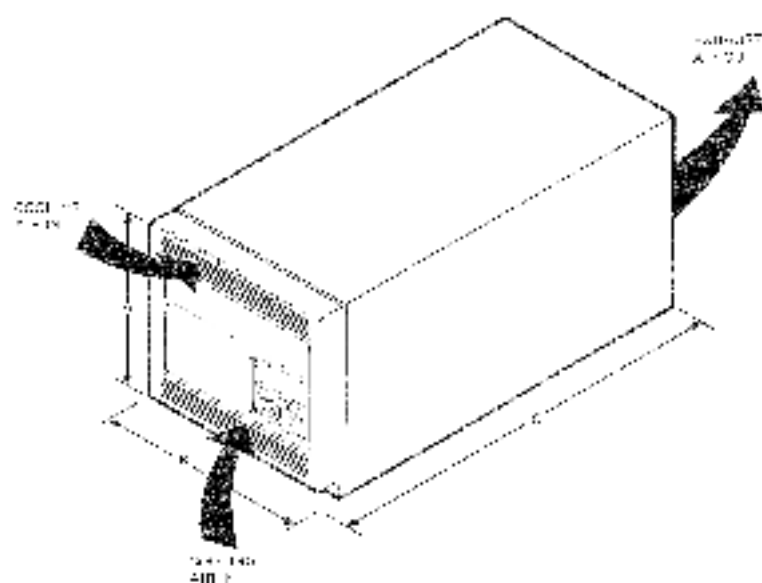
10-1001

Space Planning for the Rack Mount Unit



UP 201

RG25 Master and Slave Disk Drives



TABLETOP UNIT	DEPTH (IN)	WIDTH (IN)
A. 400001	20.0	20.0
B. 400002	20.0	20.0
C. 400003	20.0	20.0

Space Planning for the Tabletop Unit

SPECIFICATIONS

The following list defines the primary performance, design, and construction and physical characteristics of the RC25.

Size**Tabletop model**

Height	25.6 cm (10 1/8 in)
Width (master or slave)	25.4 cm (10 in)
Depth	52.1 cm (20 1/2 in)

Rackmount model

Height	26.5 cm (10 1/2 in)
Width	48.3 cm (19 in standard)
Depth	50.2 cm (19 3/4 in)

Weight**Laptop mode**

22.7 kg (50 lb)

Rackmount model

Single disk	25.5 kg (55 lb)
Dual disk	54.4 kg (120 lb)

Environment**Temperature**

Operating 13°–40°C (50°–104°F) ambient with a gradient of 10°C (18°F)/hr

Nonoperating (storage/shipping) –40°–66°C (–40°–151°F) ambient with a gradient of 20°C (36°F)/hr

Relative humidity (Operating) 10%–90% with maximum wet bulb temperature of 28°C (82°F) and a minimum dew point of 2°C (36°F) with no condensation

Nonoperating (storage/shipping) 5%–95% with no condensation

Altitude

Operating Sea level to 2.4 km (2000 ft)

Maximum operating temperature decreases by a factor of 1.8°C/(1000–1115)/1000 ft for operation above sea level.

Nonoperating (storage/shipping) Up to 9.1 km (30,000 ft) above sea level (actual or effective by means of cabin pressurization)

RC25

Shock	5 g peak at 7-10 ms duration in three axes mutually perpendicular (maximum)
Head Orientation	
Single disk drive	100° Rough
Dual disk drive	180° Rough
Noise level (single disk)	65 dB at 1 m
Electrical Voltage/frequency (single channel)	90-120 Vac, 6-8 A, 47-63 Hz 180-256 Vac, 3-5 A, 47-63 Hz
Power (operating):	
Single disk	320 W
Dual disk	535 W
Lead cord length (from end user)	1.83 m (6 ft)
Plug type 120 Vac 220-240 Vac	NEMA 5-15P NEMA 6-15P
Data Capacity (Formatted) Single disk drive	26,061,824 formatted disk 26,061,824 MB removable cartridge disk 52,123,648 MB total (50,902 512-byte blocks/platter)
Dual disk drive	52,123,648 MB fixed disk 52,123,648 MB removable cartridge disks 104,247,296 MB total (101,804 512-byte blocks/platter)
Media Fixed	One 20 cm (7.75 in) double-sided nonmagnetic disk platter per drive
Removable	One 20 cm (7.75 in) double-sided disk platter in cartridge per drive
Seek Time Average seek One track seek Maximum seek	30 ms maximum 10 ms maximum 30 ms maximum

Latency

Speed	2850 r/min ± 9 r/min
Average rotational latency	0.6 ms
Maximum rotational latency	21.0 ms
Average access	46.5 ms (overlapped seeks with double disk drive configuration)

Data Rates

Average long transfer rate	0.67 Mbytes typical

Spiral Read Time

Per track	51 ms typical
Per disk	60 s typical
Per drive	1 min, 40 s typical

Start/Stop Time

Start time	60 sec maximum (includes purge and seek test time)
Stop time	30 sec maximum

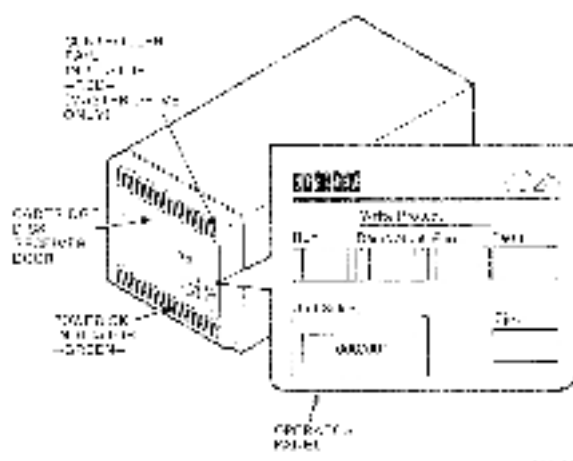
Safety precautions are listed with the following agencies:

UL	Underwriter Laboratories
CSA	Canadian Standards Association
VDE	Verband Deutscher Elektrotechniker (German Electrical Engineering Society)
IEC	International Electrotechnical Commission

Indicator States and Their Meaning

Run	Write Protect		Fault	Eject	Meaning
	Removable	Fixed			
OFF	-	-	OFF	ON	The drive is not running and the cartridge receiver door is unlocked.
Slow flash*	-	-	OFF	OFF	The disk platters are spinning up or down.
ON	-	-	OFF	OFF	The drive is ready to accept commands.
-	OFF	-	OFF	-	The removable disk cartridge is write enabled.
-	ON	-	OFF	-	The removable disk cartridge is in the read-only state. Writing is prevented.
-	-	OFF	OFF	-	The fixed disk platter is write enabled.
-	-	ON	OFF	-	The fixed disk platter is in the read-only state. Writing is prevented.
-	-	-	ON	-	The drive has detected a failure. Press FAULT briefly and refer to the fault codes in Chapter 5 to determine what went wrong.
-	-	-	slow flash*	-	The drive is in maintenance mode and is running a test.

*Slow flash is once per second.



RC25 Front View Showing Operator Panel

Cartridge Loading

The RC25 is designed to make correct loading easy. To load the cartridge disk, hold it label (writing) side up with the tapered end toward you. The opposite end has a small trap door through which the read/write heads enter. This end enters the cartridge receiver first.

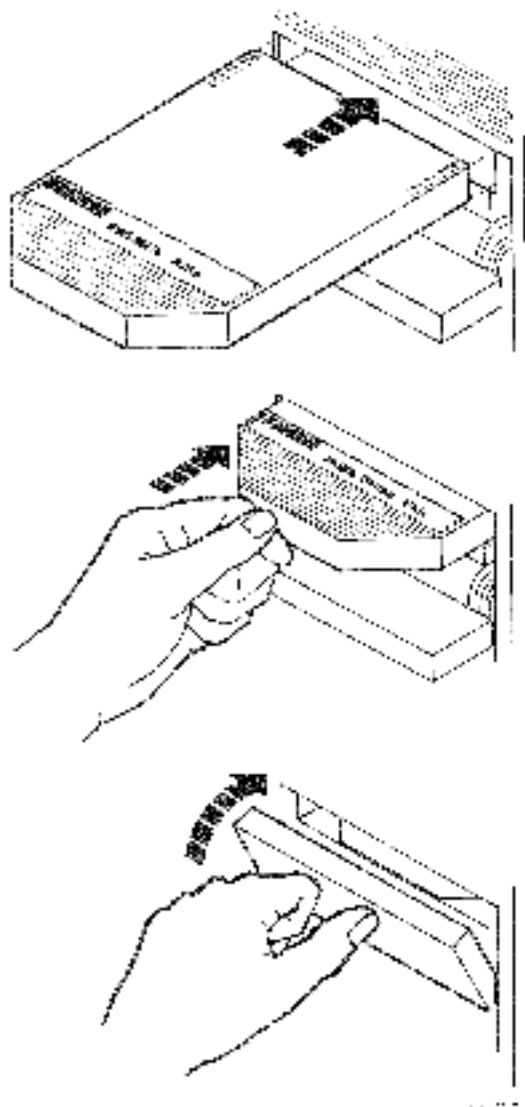
If the cartridge receiver door is not open, press the **EJECT** button. The door opens and swings down. Slide the cartridge straight in with a firm push until it locks into place. Close the receiver door firmly by swinging it back up and latching it into place.

Cartridge Unloading

Unloading the cartridge is as simple as loading. With the spindle stopped and the receiver door unlocked (**EJECT** indicator on), press the **EJECT** button. The door opens and the cartridge disk ejects. Once the door is open, grasp the cartridge and pull it straight out of the receiver.

NOTE

Keep the cartridge receiver door closed when not in use to prevent atmospheric contaminants from entering the disk enclosure.



Inserting the Disk Cartridge

Disk Operating Procedures

The procedures in this section are for starting and stopping the RC25.

Starting Procedure

Operator Action	Disk Drive Response
None.	Initial state of disk drive: RUN button is released (out). RUN indicator is off. EJECT indicator is on. Spindle is stopped.
Press EJECT.	Cartridge receiver door opens and disk cartridge partially ejects.
Reload cartridge or replace with new cartridge.	None.
Close cartridge receiver door.	None.
Set WRITE PROTECT buttons.	Corresponding WRITE PROTECT indicator lights or goes off.
Press RUN in to lock it in.	Receiver door locks. EJECT indicator goes off. RUN indicator flashes slowly. Disk platters spin up. RUN indicator lights continuously.
Disk is ready for operation.	

NOTE

A disk cartridge must be installed to spin up and operate the disk drive. The fixed disk does not spin up and run without a removable cartridge in place. The spin-up cycle takes approximately 1 minute. It involves spinning the disk platters up to operating speed, cleaning the internal air system, loading the read/write heads, and performing a self-test.

Stopping Procedure

Operator Action	Disk Drive Response
None.	Initial state of disk drive. RUN button is pressed in. Disk platters are spinning. RUN indicator is on. EJECT indicator is off.
Press RUN in to release it.	RUN indicator flashes slowly. Disk platters slow down. When disk platters stop spinning: RUN indicator goes off. EJECT indicator lights. Receiver door unlocks.
Press EJECT.	Receiver door opens partially. Push down door to eject cartridge fully.
Remove disk cartridge.	
Close receiver door.	

CAUTION

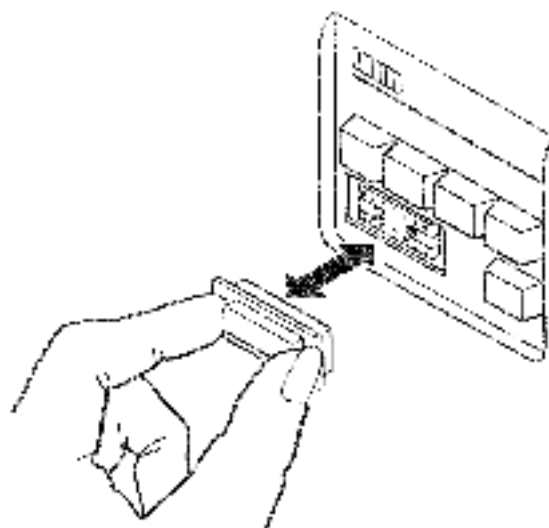
Do not try to open the receiver door until the EJECT indicator lights and the EJECT button is pressed; you can damage the disk drive and cartridge.

Unit Select Number

The host computer system (or computer network) locates a peripheral device via a unit select number. The RC25 can have any number pair from 0/n to 252/253. It has a pair of numbers because both disk platters have a unique number. The removable disk platter always has an even number and the fixed disk platter always has an odd number. The unit select number is chosen during installation, but may be changed any time thereafter.

The unit select number is determined by a factory-wired plug. This plug can be removed and replaced to change the number. However, the RC25 cannot function without a plug in place. The result is a fault indication. Two drives with the same unit select number also cause a fault.

Change the unit select number plug by grasping the plug handle and pulling it straight out of the operator panel. Install the new number plug by pushing it straight into the empty, recessed socket. When installing the new plug, be sure to hold it so the numbers are right side up. Do not try to force an up or down plug into the socket. This mistake creates a false number and destroys the electronic components inside the operator zone.

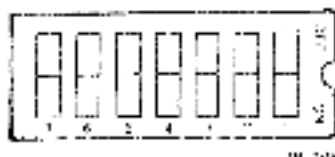


Changing the Unit Select Number Plug

HOW TO MODIFY THE UNIT SELECT NUMBER PLUG

If you want to use a unit select number pair of 8/9 or higher for your RC25, you must open and modify the unit select number plug. The procedure in this appendix shows you how to make the modification.

1. Remove the plug on the operator panel by grasping the plug handle and pulling it straight out.
2. The plug contains a small right position DIP switch. Remove this switch from the handle by spreading apart the two plastic restraining tabs and pulling straight out.
3. When working with the switch, hold it so the number 1 position is on the left, as shown below.



Unit Select Number Switch

4. Find the number pair you want and set the seven switches as indicated. Three different types of switches are used in the RC25: one slide switch and two types of rocker switches. It is important to identify which type of switch your drive has before trying to change the number. To change the number with a slide switch, push the switch tab to OFF or ON (up or down) as indicated in the table. To change the number with a rocker switch, press it on the corresponding side of the switch.
5. After setting the new number, press the DIP switch back into the plug handle and insert the plug back into the operator panel.

Unit Select Number Switch Settings

Unit Number	DIP Switch Position Number						
	1	2	3	4	5	6	7
0/1	ON	ON	ON	ON	ON	ON	ON
2/3	ON	ON	ON	ON	ON	ON	OFF
4/5	ON	ON	ON	ON	ON	OFF	ON
6/7	ON	ON	ON	ON	ON	OFF	OFF
8/9	ON	ON	ON	ON	OFF	ON	ON
10/11	ON	ON	ON	ON	OFF	ON	OFF
12/13	ON	ON	ON	ON	OFF	OFF	ON
14/15	ON	ON	ON	ON	OFF	OFF	OFF
16/17	ON	ON	ON	OFF	ON	ON	ON
18/19	ON	ON	ON	OFF	ON	ON	OFF
20/21	ON	ON	ON	OFF	ON	OFF	ON
22/23	ON	ON	ON	OFF	ON	OFF	OFF
24/25	ON	ON	ON	OFF	OFF	ON	ON
26/27	ON	ON	ON	OFF	OFF	ON	OFF
28/29	ON	ON	ON	OFF	OFF	OFF	ON
30/31	ON	ON	ON	OFF	OFF	OFF	OFF
32/33	ON	ON	OFF	ON	ON	ON	ON
34/35	ON	ON	OFF	ON	ON	ON	OFF
36/37	ON	ON	OFF	ON	ON	OFF	ON
38/39	ON	ON	OFF	ON	ON	OFF	OFF
40/41	ON	ON	OFF	ON	OFF	ON	ON
42/43	ON	ON	OFF	ON	OFF	ON	OFF
44/45	ON	ON	OFF	ON	OFF	OFF	ON
46/47	ON	ON	OFF	ON	OFF	OFF	OFF
48/49	ON	ON	OFF	OFF	ON	ON	ON
50/51	ON	ON	OFF	OFF	ON	ON	OFF
52/53	ON	ON	OFF	OFF	ON	OFF	ON
54/55	ON	ON	OFF	OFF	ON	OFF	OFF
56/57	ON	ON	OFF	OFF	OFF	ON	ON
58/59	ON	ON	OFF	OFF	OFF	ON	OFF
60/61	ON	ON	OFF	OFF	OFF	OFF	ON
62/63	ON	ON	OFF	OFF	OFF	OFF	OFF
64/65	ON	OFF	ON	ON	ON	ON	ON
66/67	ON	OFF	ON	ON	ON	ON	OFF
68/69	ON	OFF	ON	ON	ON	OFF	ON

Unit Select Number Switch Settings (Cont)

Unit Number	DIP Switch Position Number						
	1	2	3	4	5	6	7
70/71	ON	OFF	ON	ON	ON	OFF	OFF
72/73	ON	OFF	ON	ON	OFF	ON	ON
74/75	ON	OFF	ON	ON	OFF	ON	OFF
76/77	ON	OFF	ON	ON	OFF	OFF	ON
78/79	ON	OFF	ON	ON	OFF	OFF	OFF
80/81	ON	OFF	ON	OFF	ON	ON	ON
82/83	ON	OFF	ON	OFF	ON	ON	OFF
84/85	ON	OFF	ON	OFF	ON	OFF	ON
86/87	ON	OFF	ON	OFF	ON	OFF	OFF
88/89	ON	OFF	ON	OFF	OFF	ON	ON
90/91	ON	OFF	ON	OFF	OFF	ON	OFF
92/93	ON	OFF	ON	OFF	OFF	OFF	ON
94/95	ON	OFF	ON	OFF	OFF	OFF	OFF
96/97	ON	OFF	OFF	ON	ON	ON	ON
98/99	ON	OFF	OFF	ON	ON	ON	OFF
100/101	ON	OFF	OFF	ON	ON	OFF	ON
102/103	ON	OFF	OFF	ON	ON	OFF	OFF
104/105	ON	OFF	OFF	ON	OFF	ON	ON
106/107	ON	OFF	OFF	ON	OFF	ON	OFF
108/109	ON	OFF	OFF	ON	OFF	OFF	ON
110/111	ON	OFF	OFF	ON	OFF	OFF	OFF
112/113	ON	OFF	OFF	OFF	ON	ON	ON
114/115	ON	OFF	OFF	OFF	ON	ON	OFF
116/117	ON	OFF	OFF	OFF	ON	OFF	ON
118/119	ON	OFF	OFF	OFF	ON	OFF	OFF
120/121	ON	OFF	OFF	OFF	OFF	ON	ON
122/123	ON	OFF	OFF	OFF	OFF	ON	OFF
124/125	ON	OFF	OFF	OFF	OFF	OFF	ON
126/127	ON	OFF	OFF	OFF	OFF	OFF	OFF
128/129	OFF	ON	ON	ON	ON	ON	ON
130/131	OFF	ON	ON	ON	ON	ON	OFF
132/133	OFF	ON	ON	ON	ON	OFF	ON
134/135	OFF	ON	ON	ON	ON	OFF	OFF
136/137	OFF	ON	ON	ON	OFF	ON	ON
138/139	OFF	ON	ON	ON	OFF	ON	OFF

Unit Select Number Switch Settings (Cont)

Unit Number	DIP Switch Position Number						
	1	2	3	4	5	6	7
140/141	OFF	ON	ON	ON	OFF	OFF	ON
142/143	OFF	ON	ON	ON	OFF	OFF	OFF
144/145	OFF	ON	ON	OFF	ON	ON	ON
146/147	OFF	ON	ON	OFF	ON	ON	OFF
148/149	OFF	ON	ON	OFF	ON	OFF	ON
150/151	OFF	ON	ON	OFF	ON	OFF	OFF
152/153	OFF	ON	ON	OFF	OFF	ON	ON
154/155	OFF	ON	ON	OFF	OFF	ON	OFF
156/157	OFF	ON	ON	OFF	OFF	OFF	ON
158/159	OFF	ON	ON	OFF	OFF	OFF	OFF
160/161	OFF	ON	OFF	ON	ON	ON	ON
162/163	OFF	ON	OFF	ON	ON	ON	OFF
164/165	OFF	ON	OFF	ON	ON	OFF	ON
166/167	OFF	ON	OFF	ON	ON	OFF	OFF
168/169	OFF	ON	OFF	ON	OFF	ON	ON
170/171	OFF	ON	OFF	ON	OFF	ON	OFF
172/173	OFF	ON	OFF	ON	OFF	OFF	ON
174/175	OFF	ON	OFF	ON	OFF	OFF	OFF
176/177	OFF	ON	OFF	OFF	ON	ON	ON
178/179	OFF	ON	OFF	OFF	ON	ON	OFF
180/181	OFF	ON	OFF	OFF	ON	OFF	ON
182/183	OFF	ON	OFF	OFF	ON	OFF	OFF
184/185	OFF	ON	OFF	OFF	OFF	ON	ON
186/187	OFF	ON	OFF	OFF	OFF	ON	OFF
188/189	OFF	ON	OFF	OFF	OFF	OFF	ON
190/191	OFF	ON	OFF	OFF	OFF	OFF	OFF
192/193	OFF	OFF	ON	ON	ON	ON	ON
194/195	OFF	OFF	ON	ON	ON	ON	OFF
196/197	OFF	OFF	ON	ON	ON	OFF	ON
198/199	OFF	OFF	ON	ON	ON	OFF	OFF
200/201	OFF	OFF	ON	ON	OFF	ON	ON
202/203	OFF	OFF	ON	ON	OFF	ON	OFF
204/205	OFF	OFF	ON	ON	OFF	OFF	ON
206/207	OFF	OFF	ON	ON	OFF	OFF	OFF
208/209	OFF	OFF	ON	OFF	ON	ON	ON

Unit Select Number Switch Settings (Cont.)

Unit Number	DIP Switch Position Number						
	1	2	3	4	5	6	7
210/211	OFF	OFF	ON	OFF	ON	ON	OFF
212/213	OFF	OFF	ON	OFF	ON	OFF	ON
214/215	OFF	OFF	ON	OFF	ON	OFF	OFF
216/217	OFF	OFF	ON	OFF	OFF	ON	ON
218/219	OFF	OFF	ON	OFF	OFF	ON	OFF
220/221	OFF	OFF	ON	OFF	OFF	OFF	ON
222/223	OFF	OFF	ON	OFF	OFF	OFF	OFF
224/225	OFF	OFF	OFF	ON	ON	ON	ON
226/227	OFF	OFF	OFF	ON	ON	ON	OFF
228/229	OFF	OFF	OFF	ON	ON	OFF	ON
230/231	OFF	OFF	OFF	ON	ON	OFF	OFF
232/233	OFF	OFF	OFF	ON	OFF	ON	ON
234/235	OFF	OFF	OFF	ON	OFF	ON	OFF
236/237	OFF	OFF	OFF	ON	OFF	OFF	ON
238/239	OFF	OFF	OFF	ON	OFF	OFF	OFF
240/241	OFF	OFF	OFF	OFF	ON	ON	ON
242/243	OFF	OFF	OFF	OFF	ON	ON	OFF
244/245	OFF	OFF	OFF	OFF	ON	OFF	ON
246/247	OFF	OFF	OFF	OFF	ON	OFF	OFF
248/249	OFF	OFF	OFF	OFF	OFF	ON	ON
250/251	OFF	OFF	OFF	OFF	OFF	ON	OFF
252/253	OFF	OFF	OFF	OFF	OFF	OFF	ON
ILLEGAL	OFF	OFF	OFF	OFF	OFF	OFF	OFF

RD51 11 Mb WINCHESTER DISK DRIVE SUBSYSTEM

GENERAL

The RD51 fixed Winchester single element disk subsystem, found inside the MICRO/PDP-11 and the MICRO VAX, can be attached to an existing 22-bit MICRO, MICRO VAX, or a PDP-11/23 PLUS system.

The RD51 controller interface is used for both the RD51 and the RX50 disk and diskette drives.

Related Documentation

MICRO/PDP-11 Technical Manual (EK-OLCPS-1M)
MICRO/PDP-11 Owner's Manual (EK-OLCPS-OM)
MICRO/PDP-11 Unpacking and Installation (EK-OLCPS-1N)
RQBX1 Controller Module User Guide (EK-OLCPS-UG)
MICRO/PDP-11 System Option Manual (EK-OLCPS-OD)
HPS02 Rack Mount Adapter Kit Instruction Manual (EK-LEP00-1K)

RD51 Subsystem Component Specification

On-Storage Capacity

11 megabytes (formatted data) 18 sectors

Power Supply Assembly

Inputs	
Switchable line voltage	100-120 Vac (normal) 200-240 Vac (remote)
line frequency	47-63 Hz either input range
line current	120 Vac @ 2 A RMS (max) 240 Vac @ 1 A RMS (max)
Output:	
Power	65 watts (max)
DC Voltage	+12A Vdc $\pm 5\%$ 1 A min. (4.5 A max.)
	+12B Vdc $\pm 10\%$.12 A (max.)
	+5 Vdc $\pm 5\%$ @ .3 A min to 2 A (max.)

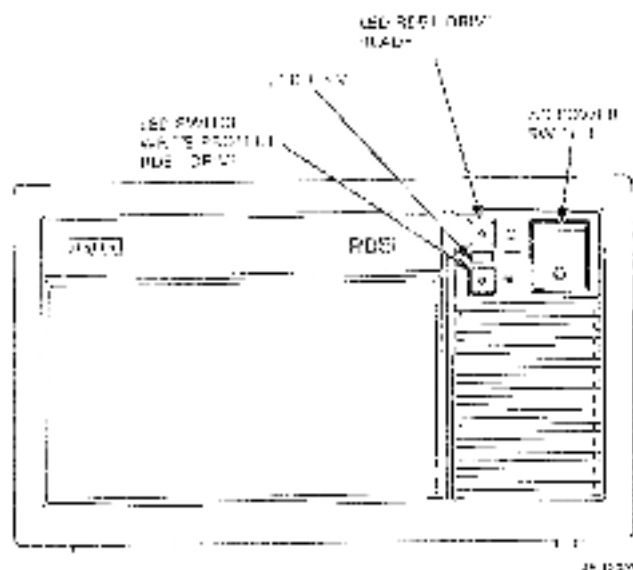
RD51

Dimension	12 in long
	9 in wide
	3 1/2 in high
Weight	14 lbs

Controls and Indicators

Switch ON/OFF in or by rocker switch - connects ac power to the subassemblies internal dc power supply.

Front Panel LEDs	Lit	Not Lit
Top Green LED	RD51 ready	RD51 not ready
Middle Green LED	DC power present	DC power not present
Amber LED	RD51 write protect	RD51 not write protected

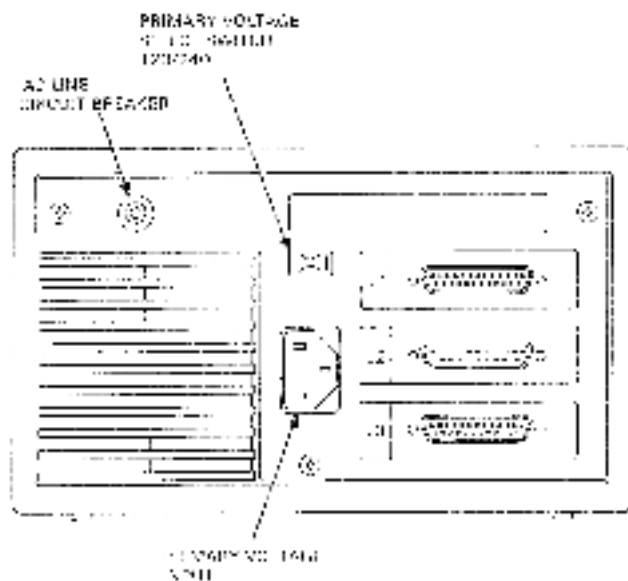


Front Panel, Controls and Indicators

Rear Panel Connectors

J1	DU0
J2	DU1
J3	DU2

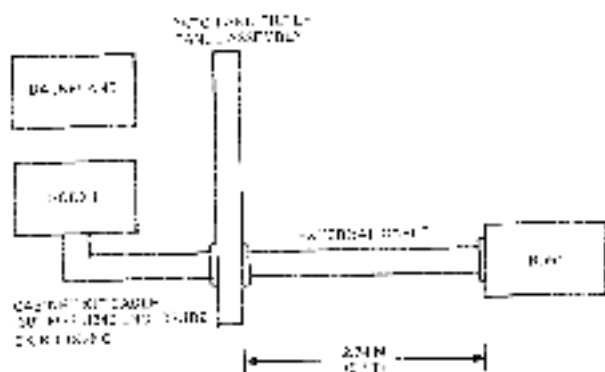
Inside the BA23 system chassis (VLSI-40(FDP-1) and MICRO VAX 1) an RDX1 drive controller, RDX1 E extender module and cdb 89 are used. (Cable kit C-K RDX1-KA)



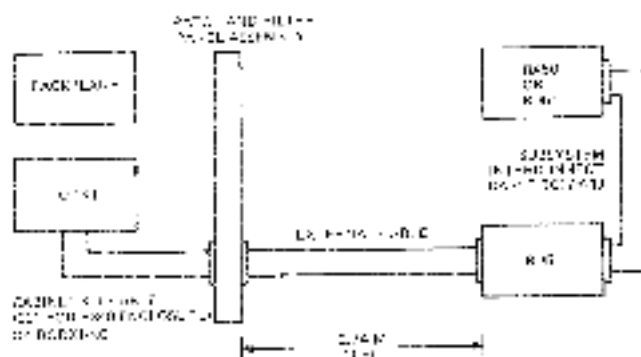
Rear Fender Assembly:

RD51

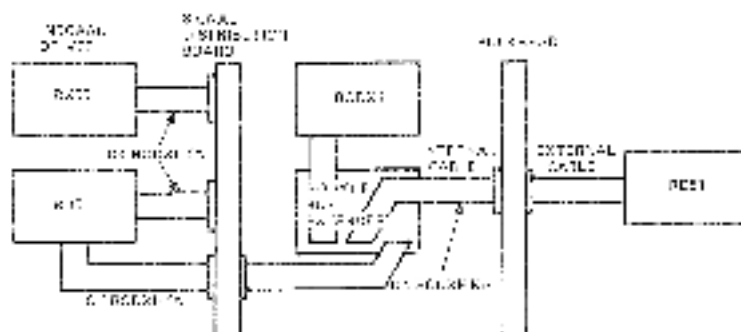
VARIOUS CONFIGURATIONS FOR EXPANSION OF THE RD51



Single Expansion Configuration



Double Expansion Configuration



Maximum Expansion Configuration

J1, J2 and J3 Pin Numbers and Signal Names

Connectors J1, J2 and J3 have identical signal names and pin numbering.

Pin No.	Signal Name	Pin No.	Signal Name
J1-01	MEMWRTDT1 (I)	J1-42	INDEX (I)
J1-24	MEMWRTDT1 (L)	J1-29	RD(WRT)FRQ (L)
J1-18	GROUND	J1-16	DRV SEL 1 (L)
J1-02	HEAD SEL 2 (L)	J1-43	DRV SEL 2 (L)
J1-35	GROUND	J1-27	DRV SEL 3 (L)
J1-19	SERKOPLT	J1-41	RX3WPTLED (I)
J1-03	RDI RDY (H)	J1-44	RXMOTORON (L)
J1-38	WPT FAULT (I)	J1-28	GROUND
J1-30	GROUND	J1-12	DIRECTION (L)
J1-04	READ SEL 1 (L)	J1-45	GROUND
J1-37	RXOWPTLED (L)	J1-23	STEP (I)
J1-21	RDD RDY (H)	J1-13	GROUND
J1-05	RX1WPTLED (I)	J1-46	RKWRDATA (L)
J1-36	DRVGLOADK (L)	J1-30	GROUND
J1-22	MEMRDDBA10 (I)	J1-14	WRT GATE (L)
J1-06	MEMRDDBA10 (L)	J1-47	GROUND
J1-32	MEMWRTDT0 (I)	J1-31	THACK 00 (L)
J1-23	MEMWRTDT0 (L)	J1-19	RX3WPTLED (I)
J1-07	MEMRDDBA1 (H)	J1-48	DRVSLACK (L)
J1-40	MEMRDDBA1 (L)	J1-02	GROUND
J1-24	GROUND	J1-15	READ DATA (L)
J1-03	HEADWRTDT (I)	J1-49	GROUND
J1-11	RD(WRT)FRQ (L)	J1-33	HEAD SEL 0 (L)
J1-25	DRV SEL 4 (L)	J1-17	GROUND
J1-08	GROUND	J1-40	READY (L)

Power Supply Connectors

AC Power Input Connector

Pin No.	Signal
1	Ground
2	ac phase
3	ac neutral

DC Power Output Connector

Pin No.	Signal
1	+5 V
2	+5 V
3	+5 V
4	Return
5	Return
6	Return
7	Return
8	12 VA
9	12 VA
10	12 VB
11	No pin
12	No connection

RD51

Logical Unit Number Selection

The logical unit number (LUN) selection is set by jumpers on the RQDX1 Controller module. These jumpers are set to the lowest LUN assigned to any RD51 or RX50 drive subsystem that is controlled by the RQDX1. The RQDX1 module automatically senses the logical unit configuration during initialization of the system to determine how many of the four possible units are actually present.

The LUN jumper format allows only one jumper to be installed at a time, and each individual jumper spanned a group of four logical units as follows.

LUN Jumper	LUNs Specified
No jumper installed	0-3
1	4-7
2	8-11
3	12-15
4	16-19
5	20-23
6	24-27
7	28-31
8	32-35

Within the context of RQDX1 configurations as shown below, if number 4 jumper is connected and using configuration number 2, then:

- 16 = unit 0
- 17 = unit 1
- 18 = unit 2
- 19 = unit 3

Configuration	External subsystem disk drives	Logical numbers for disk drives
1	One RD51, one RX50	Unit 0 = RD51 Units 1, 2 = RX50
2	Two RX50s	Units 0, 1 = RX50 Units 2, 3 = RX50
3	Two RD51s, one RX50	Unit 0 = RD51 Unit 1 = RD51 Units 2, 3 = RX50
4	Two RD51s	Unit 0 = RD51 Unit 1 = RD51
5	One RX50	Units 0, 1 = RX50

Expansion

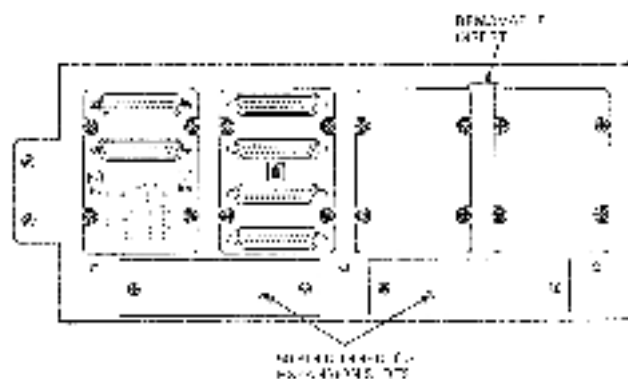
MICRO/PDP 11 and MICRO VAX I systems contain inboard RD51-A and RK50-AA drives and both systems are housed in BA23 enclosures. Each system also contains an RQDX1 controller. The controller has a capacity of four LUNs, three of which are used internally. Thus, only one RD51 drive can be added externally to the MICRO/PDP-11 and MICRO VAX I.

A BA23 enclosure (MICRO/PDP-11 and MICRO VAX I) prior to any add-on RD51, contains:

- 1 RQDX1 controller
- 1 CK-RQDX1-KA cabinet kit
- 1 RD51-A (drive only)
- 1 RK50-AA (drive only)

To accommodate an external add-on drive, an RQDX1-F bus extender and cable must be added internally and connected to the patch and filter panel assembly.

A PDP-11/23 PLUS system, to accommodate external add-on drives, requires internally an RQDX1 controller and a cabinet key cable CK-RQDX1-KC connected to the H349 distribution panel.



BA23 Patch and Filter Panel Assembly

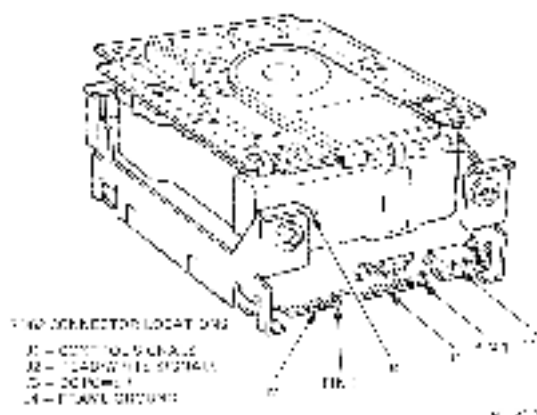
RD52 31 MB WINCHESTER DISK DRIVE SUBSYSTEM

GENERAL

The RD52 fixed disk drive uses an RDX1 controller and contains three non-magnetic 5-1/4 inch disks as storage media. The three 5-1/4 inch disks can store up to 31 megabytes of formatted data.

The interface between the disk drive and the host controller consists of four connectors:

- 11 - Control Signals
- 12 - Read/Write Signals
- 13 - DC power
- 14 - Frame ground



RD52 Connector Locations

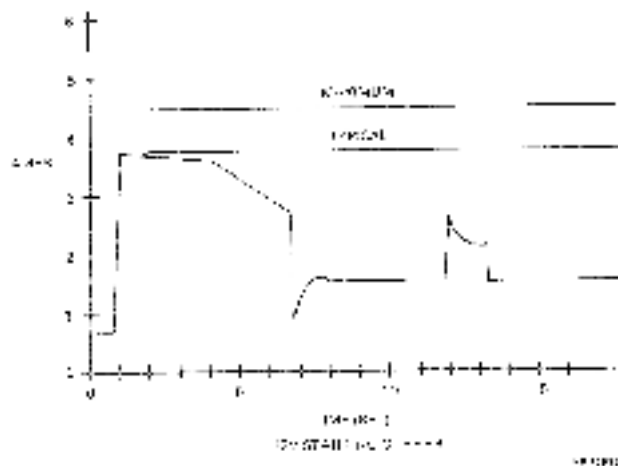
Power Requirement

+5 Vdc 15% (@ 1.0 A)

+12 Vdc -5% (@ 2.5 A (4.5 A max.))

ENV. TEMP.	MAX. C. JCT.	TEMP. STABILITY	TEMP. COEFF. REG.	TEMP. COEFF. REG.	MAX. MAXIMUM RATED	TEMP. STABILITY	TEMP. COEFF. REG.
5	1.0 A	0.01%	0.01%	0.01%	1.0 A	0.01%	0.01%
112	0.0 A	0.01%	0.01%	0.01%	0.0 A	0.01%	0.01%

CURRENT - CURRENT 5



+12 Vdc Steady Current

Related Documentation

R052-0.0 Disk Drive Subsystem Owners Manual (EK-LEP03-0M)

Physical Size

Height - 3.25 in

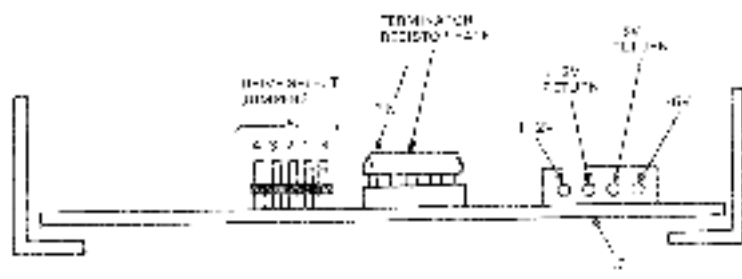
Width - 5.75 in

Depth - 8.0 in

Weight - 14 lbs

Connectors

- J1 - 34 pin - control signal
- J2 - 20 pin - ± 12 Vdc data signals
- J3 - 4 pin +5 Vdc dc power
- J4 - single lug - frame ground

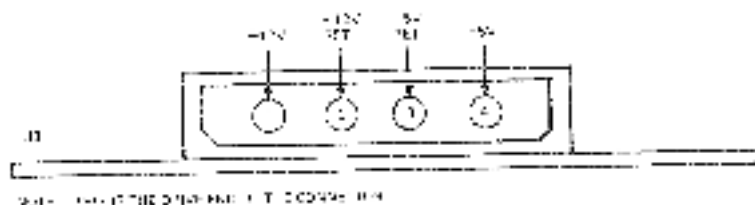


RD52 Power Connector (J3)

CAUTION

Damage will occur to the drive if the +5 V and ± 12 V connections are reversed.

CAUTION - DAMAGE WILL OCCUR TO THE DRIVE IF THE ± 12 V AND +5 V CONNECTIONS ARE REVERSED.



Selectable Address Internal

NOTE

This is the drive end of the connector.

8052

Environmental Limits

Operating temperature	10° to 50 ° C
Non operating temperature	-40° to 60° C
Operating humidity	10 % to 80%
Non operating humidity	5% to 95%
Maximum wet bulb	25° C (Non-condensing)
Thermal gradient	10°C per hour
Operating altitude	0 to 10,000 feet
Operating vibration	.5 G at 10-500 Hz
Non operating shock	30 Gs

Capacity Unformatted (+10 sps/cr cylinders)

Per drive	33.87 MB
Per surface	6.61 MB
Per track	10.416 KB

Capacity Formatted (+10 Spare Cylinders)

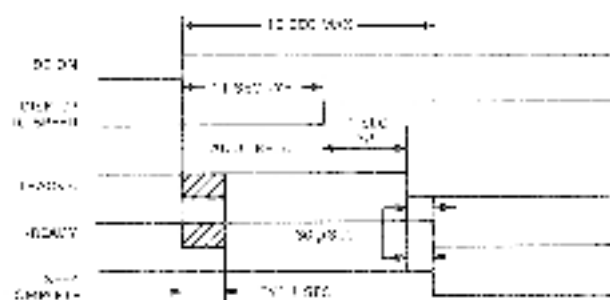
Per drive	26.00 MB
Per surface	5.20 MB
Per track	6.192 KB
Per sector	256 bytes
Sectors/Track	32
Transfer rate	5 Mbytes/sec

Seek Time

Track to track	3.0 ms
Average	30.0 ms
Maximum	60.0 ms
Settling	3.0 ms
Average latency	8.33 ms
Start time	1% sec

Functional Summary

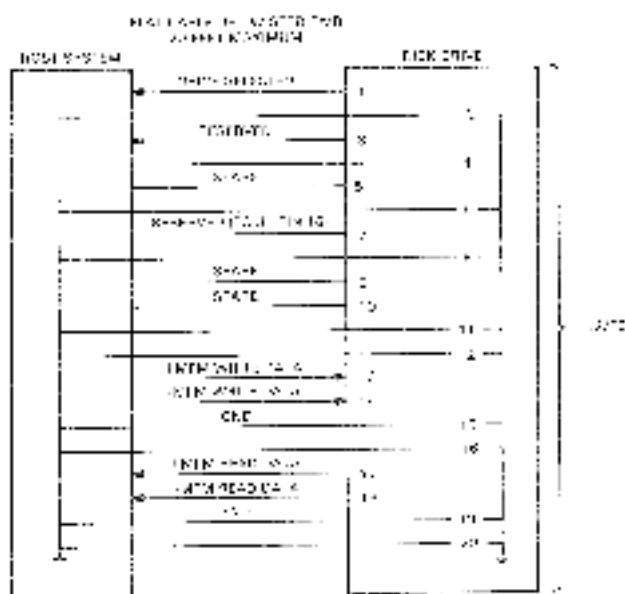
Rotation +1%	3600 rpm
Recording max	8780 bpi
Flux density	8780 m
Track density	800 tpi
Data cylinders	645
Tracks	2175
R/W heads	5
Disks	3
Index	1



NOTE: -- ONLY AUTO-LOCK CONTROL AVAILABLE IN STATION 1 OF THE PROGRAM --
 L. STATION -- NOT SELECTED

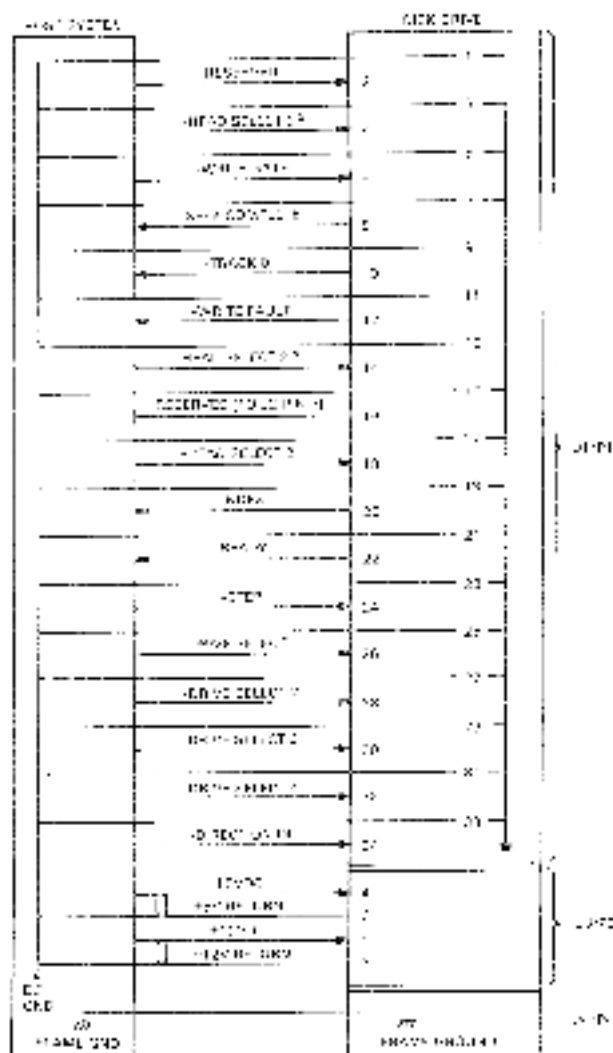
10.000 MHz

Power-Up Sequence

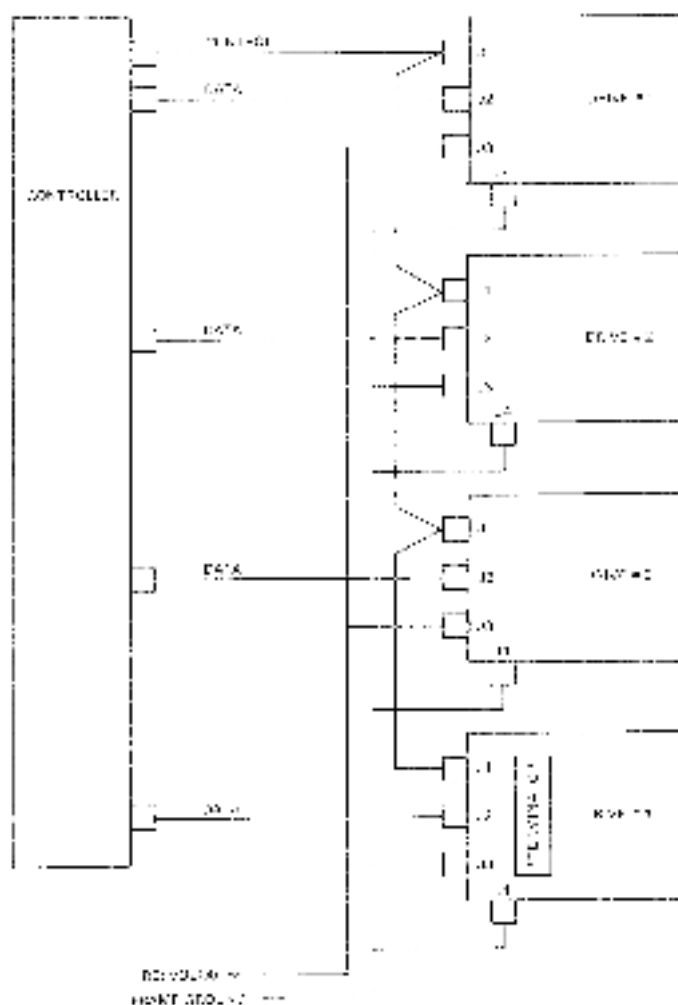


Data Signals

TABLE 100-0000-0000-0000-0000-0000-0000-0000



Control Signals

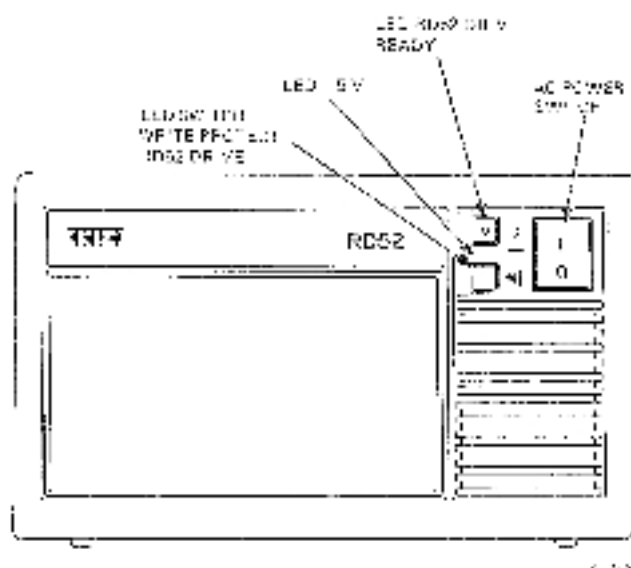


* THE LAST OF ONLY ONE OF THE CONTROL CABLES MUST HAVE A SHORT TO TERMINATE OR
 BRIDGE TO GROUND AT THE END OF THE CABLE TO PREVENT REFLECTIONS.

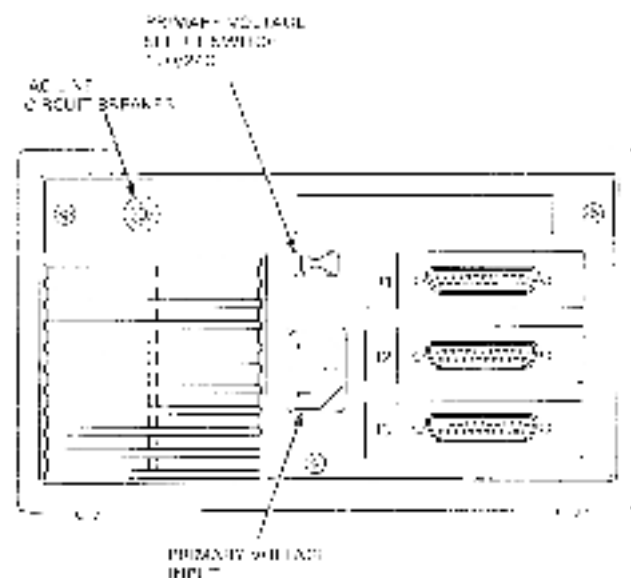
FIGURE 1

Typical Connection, Four Drivers

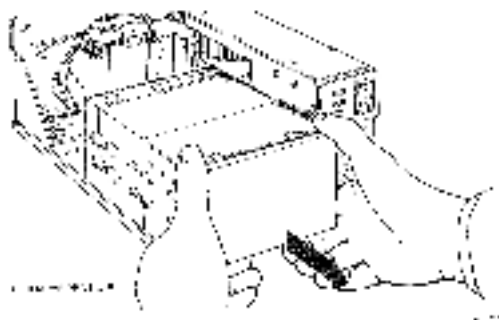
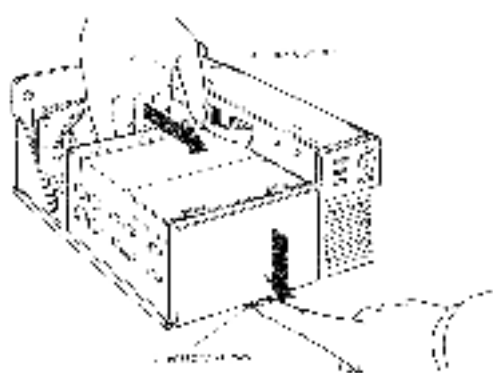
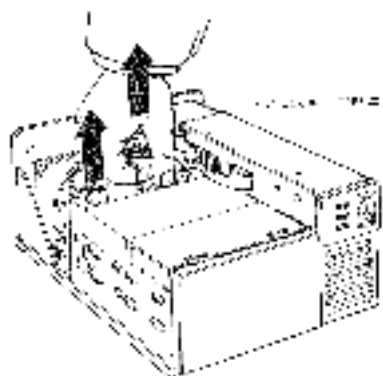
RD52



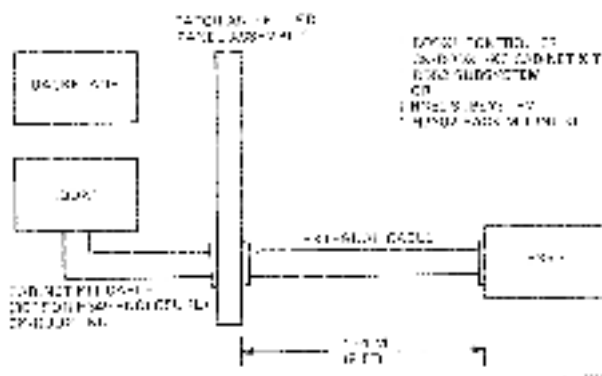
Front Panel, Switches and Indicators



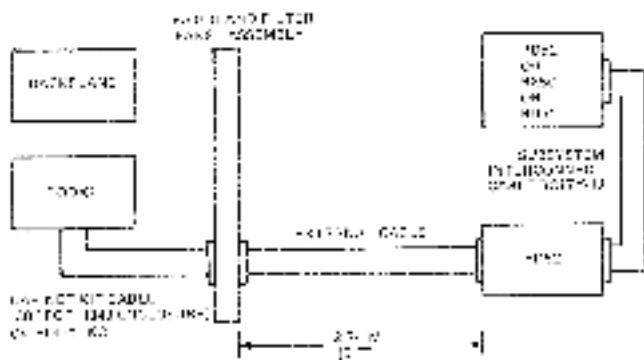
Rear Panel



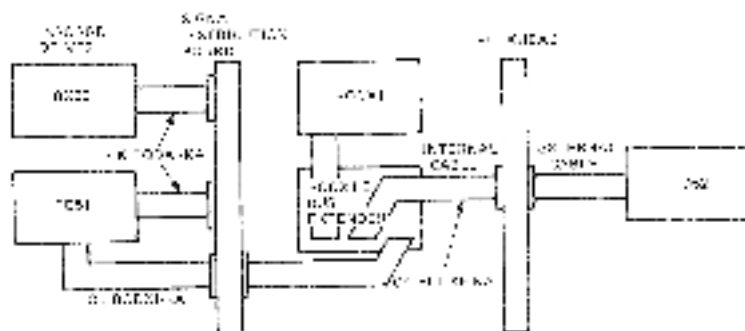
Removal of Flexible Disk Drive Signal and Power Cables



One Subsystem Add On to a PDF-11/23 PLUS



Two Subsystem Add Ons to 11349 Distribution Panel



Maximum Expansion Configuration

RK05 DISK DRIVE SUBSYSTEM

RK05 Disk Drives

The RK05-J disk drive uses a removable disk cartridge and the RK05-F uses a fixed, dual-density disk cartridge. Both drives are interfaced by the RKV11-D option. The RKV11-D is set at address 177400 and vector 220. Applicable diagnostic programs are found in Appendix A.

Related Documentation

RKV11-D Field Maintenance Print Set (MP-00223-00)

RK05-J Field Maintenance Print Set (MP-00RK05-CJ)

RK05-F Field Maintenance Print Set (MP-00RK05-DF)

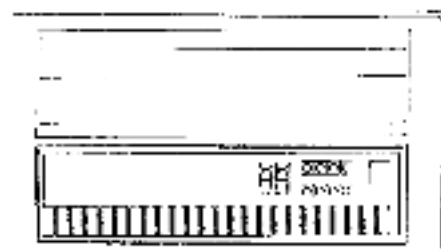
RKV11-D User's Guide (EK-RKV11-0P)

Microcomputer Interfaces Handbook (EH-20110-20)

RK05 Disk Drive User's Guide (EK-00RK05-0P)

RK05/JBJ/DSF Maintenance Manual (EK-RK05J-MM)

RK05 Exerciser Maintenance Manual (EK-RK05X-MM)



RK05 Disk Drive

Controls and Indicators for the RK05, RK05-J, and RK05-F

Controls and Indicators	Description
RUN/LOAD (Rocker Switch)	Placing this switch in the RUN position (provided that all interlocks are safe): - opens the drive front door - accelerates the disk to operating speed - loads the read/write heads - lights the RUN indicator. Placing this switch in the LOAD position: - unloads the read/write heads - stops the disk rotation - unlocks the drive front door when the disk has stopped - lights the LOAD indicator.
CAUTION Do not switch to the LOAD position during a write operation; this results in erroneous data being recorded.	
WT PROT (Pusher Switch, Spring-Loaded Off)	Placing this momentary contact switch in the PROT position lights the WT PROT indicator and prevents a write operation; it also turns off the FAULT indicator, if that is lit. Depressing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation.
PWR (Indicator)	Lights when operating power is present. Goes off when operating power is removed.
RDY (Indicator)	Lights when: - the disk is rotating at the correct operating speed - the heads are loaded - no other conditions are present (all interlocks safe) to prevent a seek, read, or write operation Goes off when the RUN/LOAD switch is set to LOAD.

Controls and Indicators for the RK05, RK05-J, and RK05-F (Cont)

Controls and Indicators	Description
ON CYL (Indicator)	Lights when: a. the drive is in the ready condition b. a seek or restore operation is not being performed c. the read/write heads are positioned and settled Goes off during a seek or restore operation.
FAULT (Indicator)	Lights when: a. erase or write current is present without a write gate b. the linear positioner transducer lamp is inoperable Goes off when the WT PROT switch is pressed, or when the drive is recycled through a run/load sequence.
WT PROT (Indicator)	Lights when: a. the WT PROT switch is pressed b. the operating system sends a WRITE PROTECT command. Goes off when the WT PROT switch is pressed a second time, or when the drive is recycled through a run/load sequence.
LCAD (Indicator)	Lights when the read/write heads are fully retracted and the spindle has stopped rotating.
WT (Indicator)	Lights when a write operation occurs. Goes off when the write operation terminates.
RD (Indicator)	Lights when a read operation occurs. Goes off when the read operation terminates.

Performance Specifications

Storage Medium

Type	Single-disk magnetic cartridge (RK05, RK05J – removable; RK05F – nonremovable)
Disk Diameter	5.25 cm (2 inches)

Magnetic Heads

Number	2

Bit Transfer

Transfer Code	Double frequency, NRZ recording
Transfer Rate	1.44 mb/s

Electrical Requirements

Voltage	115/230 Vac @ 60/50 Hz $\pm$ 0.5 Hz
Power	260 VA
Starting Current	Power only: 1.9 A Start spindle: 10 A (for 2 seconds)

Model Designation

RK05-AA, RK05J-AA, RK05F-AA, RK05F-FA 85 – 100 Vac @ 60 $\pm$ 0.5 Hz
 RK05-AD, RK05J-AB, RK05F-AB, RK05F-FB 290 – 260 Vac @ 60 $\pm$ 0.5 Hz
 RK05-BA, RK05J-BA, RK05F-AC, RK05F-FC 35 – 130 Vac @ 50 $\pm$ 0.5 Hz
 RK05-BB, RK05J-BB, RK05F-AD, RK05F-FD 130 – 260 Vac @ 50 $\pm$ 0.5 Hz

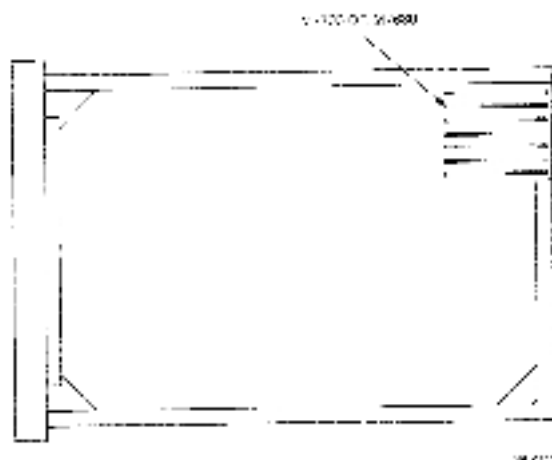
Dimensions and Weight

Width	45 cm (18 in)
Depth	67 cm (26.5 in)
Height	27 cm (10.6 in)
Weight	50 kg (110 lb)

RK05

Unit Selection

An RK05 disk drive may be configured to respond to a desired unit designation by selecting the appropriate setting on a rotary switch. The rotary switch is located on the second module in the card cage. The circuit cards are located behind the profiler, and may be accessed by removing the rear cover panel on the bottom side of the disk drive unit. In the RK05-J, the rotary switch is on the M7700 module. In the RK05-F it is on the M7680.



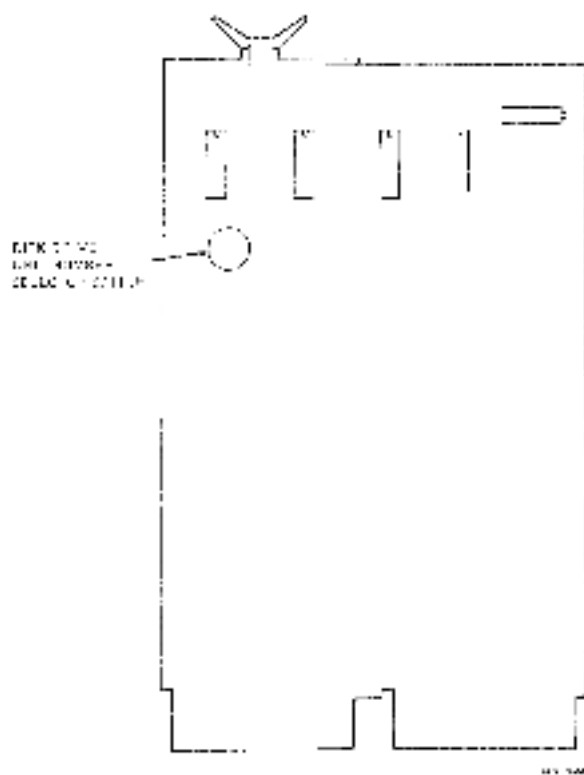
M7700 or M7680 Placement

Bootstrap Program for RK05

If an RK05 is used in a system that has no hardware bootstrap module, the disk drive may be booted by entering the following program manually.

```
@R0/000000 000000<CR>*  
@R1/000000 177404<CR>  
@1000/000000 000005<LF>  
00/002/000000 010081<LF>  
00/004/000000 000006<LF>  
00/006/000000 012701<LF>  
00/010/000000 177400<LF>  
00/012/000000 000002<LF>  
00/014/000000 012711<LF>  
00/016/000000 000006<LF>  
00/020/000000 106711<LF>  
00/022/000000 000006<LF>  
00/024/000000 000007<CR>  
@100000
```

*0 = 0 for drive 0; 2 for drive 1; and 4 for drive 2.



Control for Switches

RL01/RL02 5.2/10.4 Mb CARTRIDGE DISK DRIVE UNIT

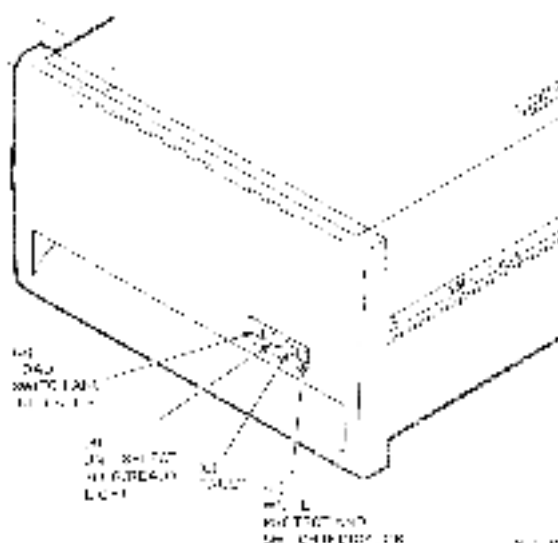
RL01/RL02 Disk Drive

The RL01 is a 5,000,000 byte disk drive that uses a modified, removable, 5¼" style cartridge (RL01K-DC). The RL02 is a dual density version of the RL01. The RL02 uses an RL02K-DC cartridge. Both the RL01 and RL02 use the RLV11 interface module. Up to four drives of either type in any combination can be connected to an RLV11 interface. The RLV11 is normally configured for a bus address of 77400 octal with a vector address of 160 octal. For more in-depth information, refer to the RLV11 (M9013/9014) section. Additional information can be found in the following manuals:

RL01/RL02 Disk Drive Technical Manual (EK-RL012-TM)
RLV11 Technical Description (EK-RLV11-TD)
RL01/RL02 Pocket Service Guide (EK-RL012-PG)
RL01/RL02 Disk Subsystem User's Guide (EK-RL012-UG)
RL01 Illustrated Parts Breakdown (EK-CRL01-IP)
RL02 Illustrated Parts Breakdown (EK-CRL02-IP)
 RL01 Field Maintenance Print Set (MF-00577-00)
 RL02 Field Maintenance Print Set (MF-00694-00)
 RLV11 Field Maintenance Print Set (MF-00636-00)
Minicomputer Interface Handbook (ED-20175-20)

Specifications RL01/RL02**Medium**

Type:	Single platter, top-load ½ cartridge (similar to RM 5440). Embedded servo information.
Capacity:	RL01K-DC — 5.2 Mb RL02K-DC — 10.4 Mb
Cylinders:	RL01 — 256 RL02 — 512
Sectors:	40
Heads:	2



RL01/RL02 Controls and Indicators

Data Transfer

MRM (Miller coding) recording 244 ns bit time; 4.1 megabytes/s (4.9 μ s/word)

RL01/RL02 Bootstrap

Ensure that the heads are over cylinder 0 and head 0 is selected by releasing the LOAD switch, waiting for the LOAD indicator to light, then depressing the LOAD switch. After the drive is ready, initialize the controller with a system initial ze. Perform a bit test, is clear. Load the following program into memory.

LOC	Contents	Comments
10000	012707	Load CSR
10002	000014	
10004	174400	
10006	000001	Wait

Start the program at 10000 and allow it to run for a few seconds, halt the program and restart at 00000.

RL01/RL02 Controls and Indicators

Switches	Function
Power ON/OFF Circuit Breaker (located in the rear of the drive)	In the OFF position, no power is removed from the drive. In the ON position, no power is supplied to the drive.
(A) LOAD	This is a PUSH/PUSH alternating action switch. When depressed, the RL01/RL02 begins a "cycle up" sequence, provided that: • the RL01/RL02 cartridge is installed • the cartridge cover is in place • the access door is closed • all ac and dc voltages are within spec • the R/W heads are retracted • the brushes are in the "home" position. When released, the RL01/RL02 will begin a "cycle down" sequence.
(B) UNIT SELECT PLUG	This is a non-operated switch that is activated by inserting a numbered, domed button. The switch contacts are binary encoded so that the drive assumes the logical unit number that is printed on the button.
(C) WRITE PROTECT	This is an alternating action PUSH/PUSH switch. When depressed, the drive assumes a write protect status (during a write operation). When released the drive is no longer write protected.

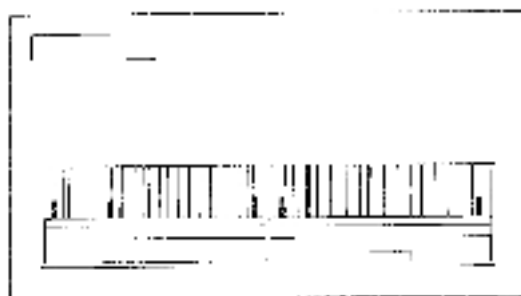
RL01/RL02 Controls and Indicators (Cont)

Indicators	Function
(A) LOAD (Yellow)	Indicates that the drive is ready to have a cartridge loaded (or unloaded). The LOAD indicator will light when: - the spindle is stopped - the R/W heads are "home" - the brushes are "home."
(B) READY (White)	When lit, indicates a "drive ready" condition; i.e., the heads are loaded and oriented.
(C) FAULT (Red)	Indicates when one of the following has occurred: - drive select error - seek timeout error (1.5 second) - write current in heads during "sector time" - loss of system clock from R/W U - write data error (no track data) - spin error (over speed or 40 sec timeout) - write gate error (attempting to write when not ready, when write protected, or during sector time)
(D) WRITE PROTECT (Yellow)	Indicates that drive is write protected, that is, write operations to the cartridge will be inhibited (and the FAULT indicator will light).

RX01 FLOPPY DISK DRIVE

RX01 Floppy Disk Drive

The RX01 floppy disk drive is part of the RXV11 floppy disk system, and is interfaced by the RXV11 interface module (M/948). The disk system uses address 177170 and vector 204 for the first option, and address 177174 and vector 270 for a second option.



RX01 Floppy Disk

Model Designations

RXV11-AA Single Drive System, 110 V/60 Hz
 RXV11-AC Single Drive System, 115 V/50 Hz
 RXV11-AD Single Drive System, 230 V/50 Hz
 RXV11-BA Dual Drive System, 115 V/60 Hz
 RXV11-BD Dual Drive System, 115 V/50 Hz
 RXV11-BD Dual Drive System, 230 V/50 Hz

Related Documentation

RXV11 User's Manual (EK-RXV11-00)

RX01/RX02/RX11 Floppy Disk System Maintenance Manual (EK-RX01-MM)

RXV11 Field Maintenance Print Set (MP-00024-00)

RX01 Field Maintenance Print Set (MP-00296-00)

RX01/RX02 Reference Card (EK-RX01-RC)

Microcomputer Interfaces Handbook (ER-00175-00)

NOTE

50 Hz versions are available in voltages of 105, 115, 220, and 240 Vac by field-pluggable conversion. Refer to the *RX01/RX02/RX11 Floppy Disk System Maintenance Manual* for complete input power modification details.

AC Power

The RXV11 floppy disk system is available in the following three ac voltage/mode configurations:

Models	Voltage/Frequency						
RXV11-AA, -BA	100 Vac-150 Vac, 60 Hz						
RXV11-AC, -BC	100 Vac-150 Vac, 50 Hz						
RXV11-AD, -BD	160 Vac-264 Vac, 50 Hz, in one of two voltage ranges. The actual voltage range is user-selected by installing the appropriate power harness during system installation, as follows.						
	<table> <tr> <th>Voltage Range</th><th>Power Harness PN</th></tr> <tr> <td>150-240</td><td>7C-10686-04</td></tr> <tr> <td>200-264</td><td>7C-10686-03</td></tr> </table>	Voltage Range	Power Harness PN	150-240	7C-10686-04	200-264	7C-10686-03
Voltage Range	Power Harness PN						
150-240	7C-10686-04						
200-264	7C-10686-03						

Power Consumption

RX01
 3 A at 24 V (dual), 75 W;
 5 A at 5 V, 25 W

RXV11 interface (M7246)
 Power input (ac)
 Not more than 1.5 A at 5 Vdc
 4 A at 115 Vac
 2 A at 230 Vac

RX01

Boostraps for Manual Entry

Full Length Version

```

001000/000000 12702<LF>
001002/000000 *00707<LF>*
001004/000000 12701<LF>
001006/000000 171170<LF>
001008/000000 130211<LF>
001010/000000 1776<LF>
001012/000000 1776<LF>
001014/000000 112010<LF>
001016/000000 7<LF>
001020/000000 10103<LF>
001022/000000 10223<LF>
001024/000000 402<LF>
001026/000000 12710<LF>
001030/000000 1<LF>
001032/000000 8203<LF>
001034/000000 100402<LF>
001036/000000 112711<LF>
001040/000000 111023<LF>
001042/000000 32011<LF>
001044/000000 1778<LF>
001046/000000 100758<LF>
001050/000000 103766<LF>
001052/000000 105711<LF>
001054/000000 100771<LF>
001056/000000 5000<LF>
001060/000000 22710<LF>
001062/000000 240<LF>
001064/000000 1047<LF>
001066/000000 122702<LF>
001070/000000 247<LF>
001072/000000 5500<LF>
001074/000000 1007<CR>

```

*r = 1 for unit 0

n = 0 for unit 1

<LF> = Line Feed

<CR> = Carriage Return

Starting address = 1000

Abbreviated Version (Drive 0 Only)

```

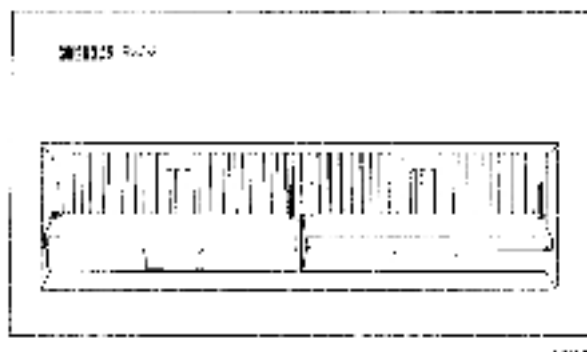
001000/000000 5000<LF>
001002/000000 12701<LF>
001004/000000 177170<LF>
001006/000000 105711<LF>
001010/000000 1776<LF>
001012/000000 12711<LF>
001014/000000 3<LF>
001016/000000 6711<LF>
001020/000000 1776<LF>
001022/000000 100405<LF>
001024/000000 105711<LF>
001026/000000 100004<LF>
001030/000000 116120<LF>
001032/000000 2<LF>
001034/000000 770<LF>
001036/000000 0<LF>
001040/000000 1007<CR>

```

RX02 FLOPPY DISK DRIVE

RX02 Floppy Disk Drive

The RX02 is part of the RXV11-RX floppy disk system. The RXV21-DX options use the RX02 in double-density mode with the RXV21 (M3029) interface module. The RXV21-DX options use the RX02 in single-density mode with the RXV21 (M7946) interface module.



Front View of the Floppy Disk System

The density mode of the RX02 is selected by switches on the M7744 controller module. This module is located in the RX02 floppy disk drive. The following switch settings define the mode of the RX02.

Controller Configuration Switch Settings
(Located on M7744 Module)

Interface	S1-1	S1-2
RXV11/RXV21	OFF	ON
RX0E/RX11/RXV11	ON	OFF
RX20	OFF	OFF

NOTE

The subject of the RX02 as used in a PDP-8 system is beyond the scope of this document.

General configuration and diagnostic information is contained in this manual. Refer to the section covering the applicable interface (M7946 or M3029).

RX02

Related Documentation

RX02 Floppy Disk System User's Guide (FK 6RX02-UG)
RX01/RX02 Reference Card (EK-RX102-RC)
Microcomputer Interface Handbook (EK 20175-20)
RX02 Print Set (MP 00009-00)

Module Designations

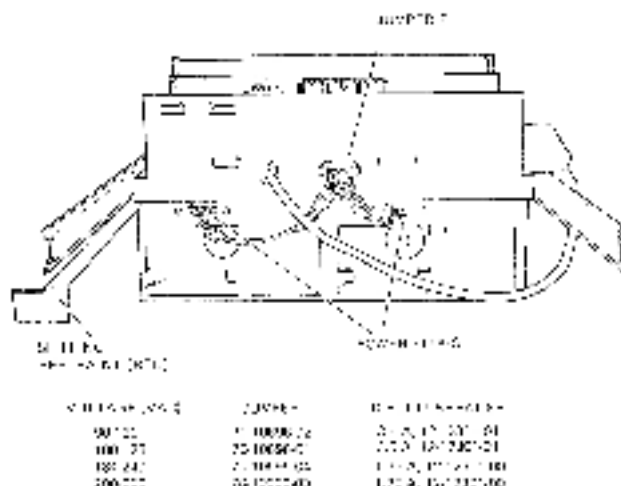
HXV21	-DA	M7948	RX02-DA	115 V, 60 Hz
	-DC	M7946	RX02-DC	115 V, 60 Hz
	-DD	M7946	RX02-DD	230 V, 60 Hz
	-BA	M8026	RX02-BA	115 V, 60 Hz
	-BC	M8024	RX02-BC	115 V, 60 Hz
	-BD	M8027	RX02-BD	230 V, 60 Hz

Power Requirements

The RX02 is designed to use either a 60 Hz Vac or a 50 Hz power source. The 60 Hz version will operate from 90 Vac - 125 Vac, without modification, and will use less than 4 A operating. The 60 Hz version will operate within four voltage ratings and will require field verification on/off calibration to ensure that the correct voltage option is selected. The voltage ranges of 90 Vac-120 Vac and 164 Vac-240 Vac will use less than 4 A operating. The voltage ranges of 100 Vac-120 Vac and 200 Vac-250 Vac will use less than 2 A. Both versions of the RX02 will be required to receive the input power from an ac source (e.g., 561 power control) that is controlled by the system's power switch.

Input Power Modification Requirements

The 60 Hz version of the RX02 uses the H771-A power supply and will operate on 90 Vac-125 Vac, without modification. To convert to operate on a 60 Hz power source in the field, the H771-A supply must be replaced with an H771-C or -D and the drive motor belt and drive motor pulley must be replaced. The H771-C operates on a 90 Vac-120 Vac or 100 Vac-125 Vac power source. The H771-D operates on a 134 Vac-240 Vac or 200 Vac-250 Vac power source. To convert the H771-C to the higher voltage ranges or the H771-D to the lower voltage ranges, the power harness and circuit breaker must be changed. The appropriate jumper and circuit breaker are shown in the following figure.



RX02

RX02/RXV21 (M8029)

60000/XXXXXXXX	12701<LF>
6002/XXXXXXXX	177170<LF>
6004/XXXXXXXX	17700<LF>
6006/XXXXXXXX	100240<LF>
6010/XXXXXXXX	5002<LF>
6012/XXXXXXXX	12705<LF>
6014/XXXXXXXX	200<LF>
6016/XXXXXXXX	12704<LF>
6020/XXXXXXXX	401<LF>
6022/XXXXXXXX	12703<LF>
6024/XXXXXXXX	177172<LF>
6026/XXXXXXXX	3001<LF>
6030/XXXXXXXX	1776<LF>
6032/XXXXXXXX	100470<LF>
6034/XXXXXXXX	12711<LF>
6036/XXXXXXXX	401<LF>
6040/XXXXXXXX	3001<LF>
6042/XXXXXXXX	1776<LF>
6044/XXXXXXXX	100431<LF>
6046/XXXXXXXX	110413<LF>
6048/XXXXXXXX	804<LF>
6052/XXXXXXXX	30011<LF>
6054/XXXXXXXX	1776<LF>
6056/XXXXXXXX	112413<LF>
6060/XXXXXXXX	304<LF>
6062/XXXXXXXX	30011<LF>
6064/XXXXXXXX	1776<LF>
6066/XXXXXXXX	1100470<LF>
6070/XXXXXXXX	12711<LF>
6072/XXXXXXXX	403<LF>
6074/XXXXXXXX	30011<LF>
6076/XXXXXXXX	1776<LF>
6100/XXXXXXXX	100413<LF>
6102/XXXXXXXX	10513<LF>
6104/XXXXXXXX	30011<LF>
6106/XXXXXXXX	1776<LF>
6110/XXXXXXXX	10040<LF>
6112/XXXXXXXX	10213<LF>
6114/XXXXXXXX	5052<LF>
6116/XXXXXXXX	60502<LF>
6120/XXXXXXXX	100470<LF>
6122/XXXXXXXX	12043<LF>
6124/XXXXXXXX	7<LF>

RX02/RXV2-1 (MSG28) (Cont)

2128/XXXXXX	3737<LF>
2130/XXXXXX	5000<LF>
2132/XXXXXX	5007<LF>
2134/XXXXXX	0<CR>
222000	

RX50 FLOPPY DISK DRIVE SUBSYSTEM

GENERAL

The RX50 R/D track or disk module uses an RQDX1 controller interface which controls up to four logical units. The RX50 uses two logical units and the RD51 uses one logical unit. With a system using an RQDX1 controller, the maximum configuration that can be used is two RX50 disk drive units or one RX50 and one RD50 disk unit, expandable by one RD51 drive and by using an RQDX1-E bus extender option.

RX50 Flexible Disk Drives - 120 Vac or 240 Vac Voltage Selectable

Power Supply

	-12 Av	0v	+12 Battery voltage
Minimum	1 A	.3 A	3 A
Maximum	1.3 A	5.0 A	12 A

RX50 Voltage

Maximum	3 A	3 A	.2 A
Minimum	1.3 A	5 A	.2 A
Standby	0.1 A	5 A	.2 A

Capacity (diskette)

800K bytes

Related Documentation

MICRO/PDP-11 Systems, Technical Manual (EK-OLCPS-TV)
MICRO/PDP-11 Systems, Owner's Manual (EK-OLCPS-OM)
MICRO/PDP-11 Systems, Unpacking and Installation Guide (EK-OLCPS-IN)
MICRO/PDP-11 System Option Manual (EK-OLCPS-OD-001)
RQDX1 Controller Module User's Guide (EK-RQDX1-UG)
 (includes RQDX1-E Bus Extender)
HS302 Rack Mounting and Installation Manual (EK-HS302-IN)

Compatibility

RX50 R/D units are used as add-ons in the PDP 11/30 PLUS, MICRO/PDP-11, MICRO VAX I, and other Q-BUS hosts.

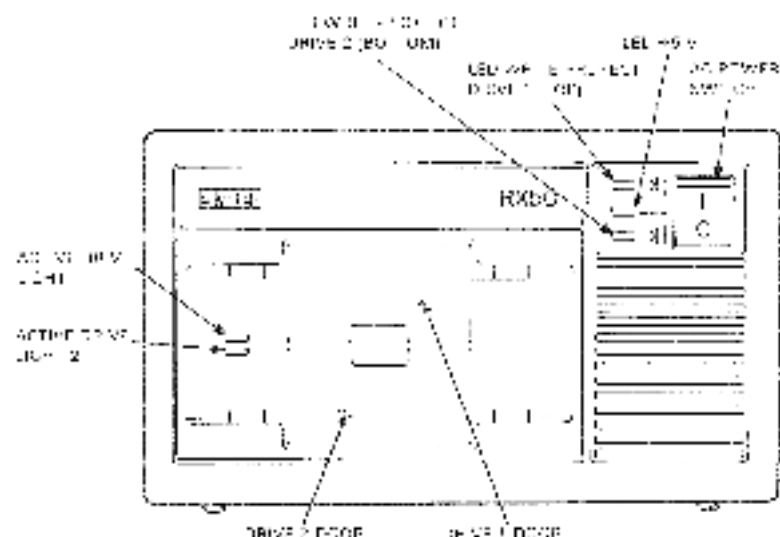
Front Panel Controls and Indicators

AC power ON/OFF switch – connects AC power to the internal power supply.

TOP THREE LEDs:	L11
1st (yellow) LED	When top drive is write protected
2nd (green) LED	+5 Vdc is being supplied to the drive
3rd (yellow) LED	When bottom drive is write protected

NOTE

Never open a disk drive door when either drive's light is on (active drive).



RX50-111

Front Panel, Switches and Indicators

RX50

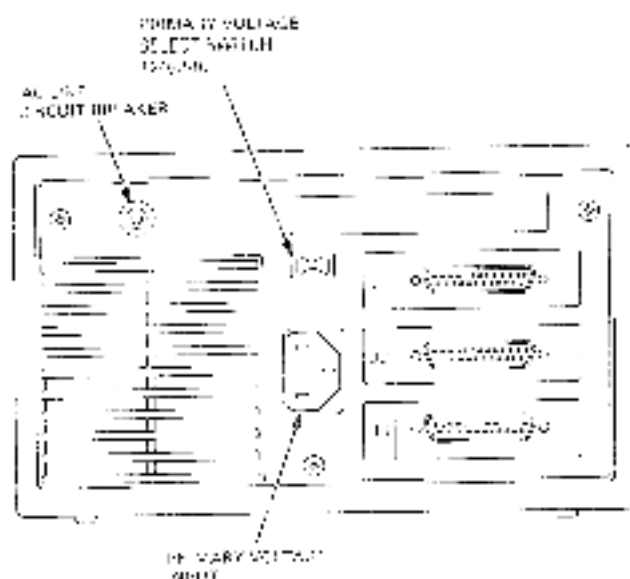


FIGURE 1

RX50 Near View

RX60 Subsystem Dimensions and Weights

Dimensions

Desk top configuration and
rack mount configuration

Approximately 12 inches long 9
inches wide, 6-1/2 inches high

Weights

Desk top configuration and
rack mount configuration

Approximately 14 pounds

The hardware requirements for the BAC3 enclosure are:

- 1 RQDX1 Controller
- 1 OR RQDX1-KA cabinet kit
- 1 RX50-D subassembly
or
- 1 RX50-F subassembly
- 1 H5302 rack adapter kit

RX50

The hardware requirements for the BA20 enclosure are:

- 1 RQDX1 controller
- 1 CK-RQDX1-KA cabinet kit

The two subsystems can be either:

- 2 RD51-U subsystems or 2 RD51-R with 1 H9302 adapter kit or
- 1 RD51-D or -R with 1 H9302
- 1 RX50-D or -R with H9302
- 1 BC17Y-U subsystem interconnection cable

The hardware requirements for the H349 enclosure are:

- 1 RQDX1 controller
- 1 CK-RQDX1-KG cabinet kit

and the two subsystems can be either:

- 2 RD51-D subsystems or 2 RD51-R with 1 H9302 rack adapter kit or,
- 1 RD51-D or 1 RD51-R with 1 H9302 rack adapter kit
- 1 RX50-D or H800-R
- 1 BC17Y-U subsystem interconnection cable.

The hardware requirements are:

- 1 RQDX1-C RQDX1 extender
- 1 CK-RQDX1-KA cabinet kit R.D./R.X. controller EXT BA20
- 1 RD51-U or
- 1 RD51-R with 1 H302 rack adapter kit

SYSTEM AND EXTERNAL SUBSYSTEM INTERCONNECT

System enclosures such as the BA25 and H319 have a piston and fiber panel assembly attached to the rear of the unit. This panel has an unused area that can be used for system expansion. The internal system cabling for the external subsystem is contained in the cabinet kits and will be connected to a proper connector on the internal side of the piston panel. The subsystem user can simply connect to the external connector of the port used.

J1, J2 and J3 Pin Numbers and Signal Names

Connectors J1, J2 and J3 have the same signal names and pin numbering.

Pin Numbers	Signal Names	Pin Numbers	Signal Names
J1-01	MEMWRTDT* (H)	J1-25	DRV SEL 4 (L)
J1-04	MEMWRTDT* (L)	J1-09	GROUND
J1-18	GROUND	J1-42	INDEX (L)
J1-02	HEAD SET 2 (L)	J1-29	RDWRTTRPO (L)
J1-05	GROUND	J1-10	DRV SEL 1 (L)
J1-19	SEFREQ* *	J1-43	DRV SEL 2 (L)
J1-03	RD1 RDY (H)	J1-27	DRV SEL 3 (L)
J1-28	WRT FAIL1 (L)	J1-11	EXWPTLED (L)
J1-20	GROUND	J1-44	EXMOTORON (L)
J1-04	READ SEL 1 (L)	J1-28	GROUND
J1-07	EXWPTLED (L)	J1-12	DIRECTION (L)
J1-21	RD0 RDY (H)	J1-45	GROUND
J1-05	EXWPT HD (L)	J1-23	STEP (L)
J1-28	DRVSL JACK (L)	J1-13	GROUND
J1-22	MEMRD DATA (H)	J1-46	EXWRTDATA (L)
J1-06	MEMRD DATA (L)	J1-30	GROUND
J1-39	MEMWRTDT0 (H)	J1-14	WRT GATE (L)
J1-23	MEMWRTDT0 (L)	J1-47	GROUND
J1-37	MEMRD DATA1 (H)	J1-31	TRACK 00 (L)
J1-40	MEMRD DATA1 (L)	J1-15	EXWPT HD (L)
J1-24	GROUND	J1-48	DRVSL JACK (L)
J1-08	RD0WRT (L)	J1-32	GROUND
J1-41	RD0WRTTRPO (L)	J1-16	READ DATA (L)
		J1-49	GROUND
		J1-35	HEAD SET 0 (L)
		J1-17	GROUND
		J1-50	READY (L)

RX50

Power Supply Connectors

AC Power Input Connector

Pin No.	Signal
1	Ground
2	AC phase
3	AC neutral

DC Power Output Connector

Pin No.	Signal
1	+5 V
2	+5 V
3	+5 V
4	Return
5	Return
6	Return
7	Return
8	12 VA
9	12 VA
10	12 VB
11	No pin
12	No connection

Logical Unit Number Selection

The logical unit number (LUN) selection is set by jumpers on the RQDX1 controller module. These jumpers are set to the lowest LUN logical unit number assigned to any HDS1 or RX50 drive subsystem that is controlled by the RQDX1. The RQDX1 module automatically senses the logical unit configuration during initialization of the system to determine how many of the four possible units are actually present.

The LUN jumper format allows only one jumper to be installed at a time, and each individual jumper specifies a group of 4 logical units as follows:

LUN Jumper	LUNs Specified
No jumper installed	0-3
1	4-7
2	8-11
3	12-15
4	16-19
5	20-23
6	24-27
7	28-31
8	32-35

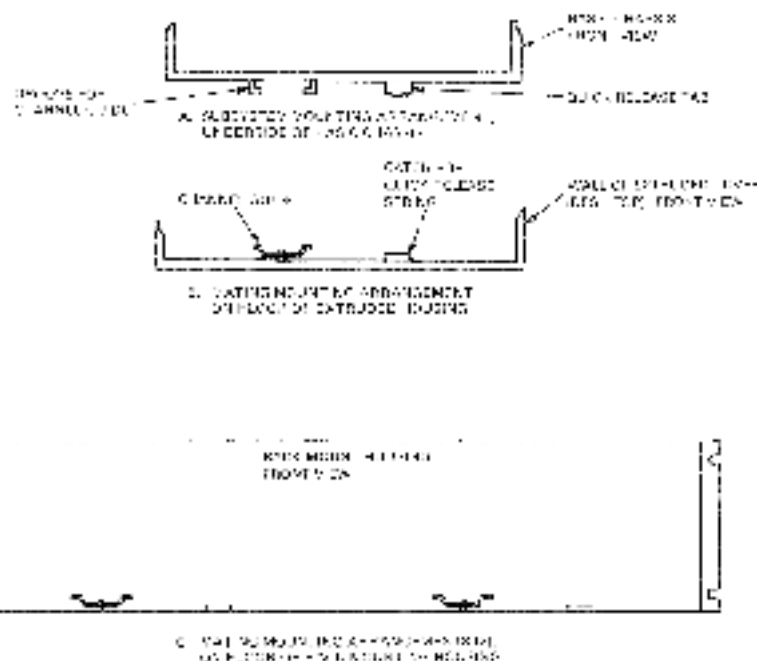
Within the context of RDX1 configurations as shown below, if the number 4 jumper is connected and configuration number 2 is being used, then:

- 16 = unit 0
- 17 = unit 1
- 18 = unit 2
- 19 = unit 3

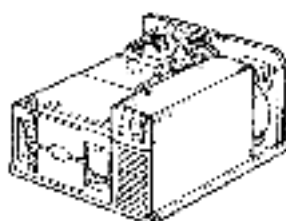
Configuration Number	External Subsystem Disk Drives	Logical Unit Numbers for Disk Drive
1	One RD51, one RX50	Unit 0 = RD51 Units 1, 2 = RX50
2	Two RX50s	Units 0, 1 = RX50 Units 2, 3 = RX50
3	Two RD51s, one RX50	Unit 0 = RD51 Unit 1 = RD51 Units 2, 3 = RX50
4	Two RD51s	Unit 0 = RD51 Unit 1 = RD51
5	One RX50	Units 0, 1 = RX50
6	One RD51	Unit 0 = RD51

System Controller Options

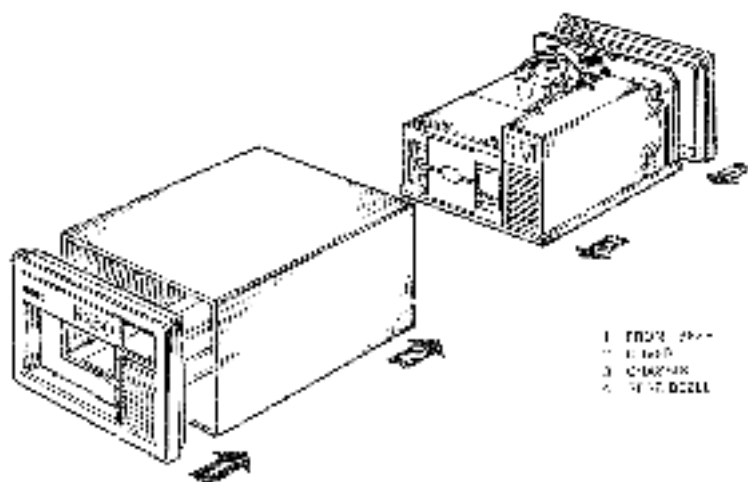
Model	Description	
RQDX1	Controller/Interface, MSOP Q-BUS	RX50 and/or RD51 MSOP controller. One controller handles up to four logical units. No more than two RX50s per controller. One RX50L is equal to two LUNs.
RQDX1-E	Bus EXTENDER w/cable	Enables external drive (RX50, RD51) to connect to MICRO/PDP-11 internal controller-to-drive bus. Allows either one external RX50 or one external RD51 to be connected to the MICRO/PDP-11 controller depending on the RQDX1 configuration guidelines.
CK-RQDX1-KA	Cabinet kit for installing the RQDX1 controller in a DA25 enclosure (MICRO/PDP-11).	
CK-RQDX1-KC	Cabinet kit for installing the RQDX1 controller with the H548 I/O panel (PDP 11/23 PLUS).	
CK-RQDX1-E KA	Cabinet kit for installing the RQDX1-E extender in a HA23 enclosure (MICRO/PDP 11).	
RQDX1-C	Country kit: Doc. for RQDX1 Controller and Extender	
RQDX1-D	Country kit: Doc, Labels, Diagnostic for RX50-D, -D.	
RD51-E	Country kit: Doc, Labels for RD51-D, -D.	



Mounting Channel and Quick Release Latch



A. RX50 - RACK MOUNTING HOUSING

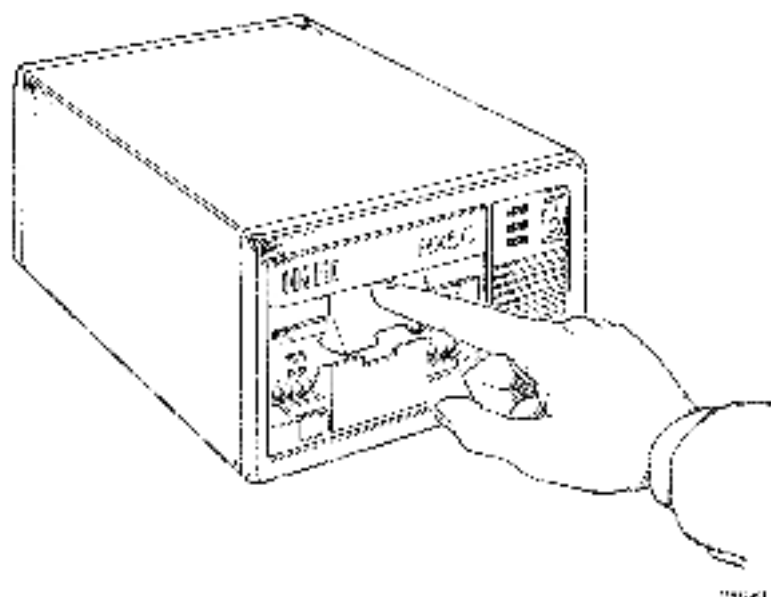


F. RX50 Desk-Top MOUNTING HOUSING

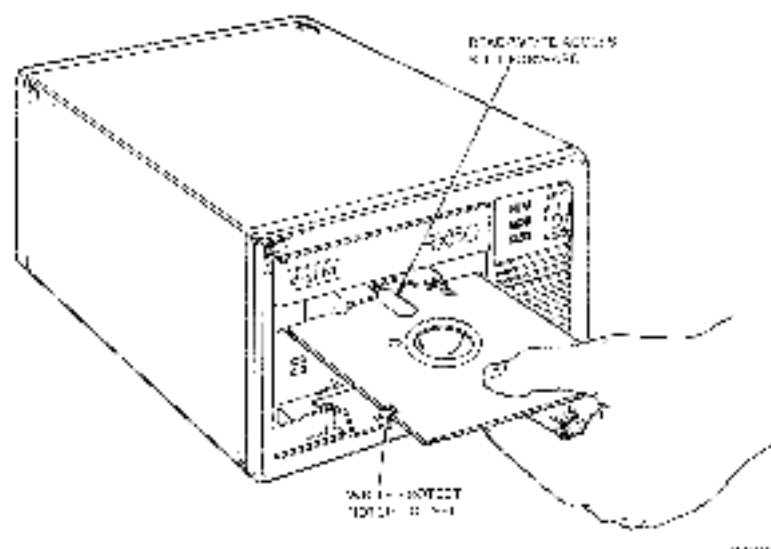
1. FRONT PANEL
2. LENS
3. CHASSIS
4. REAR BEZEL

100-1000

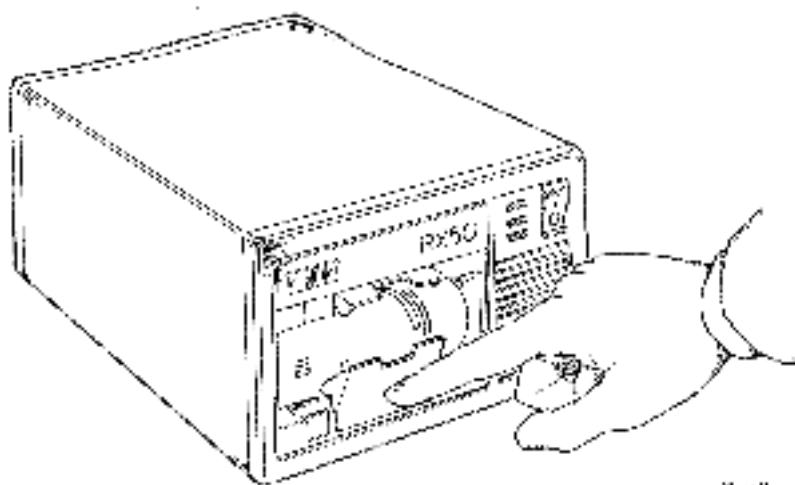
RX50 Desk-Top and Rack Mounting Housing



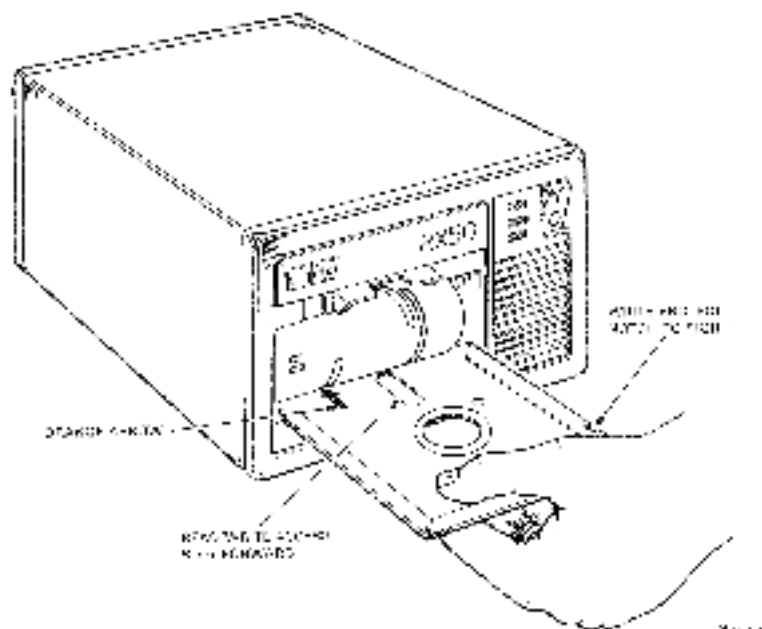
Opening the Drive 1 Door



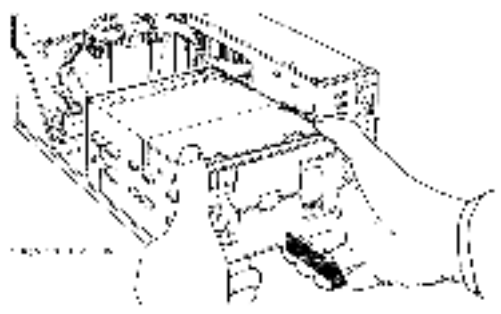
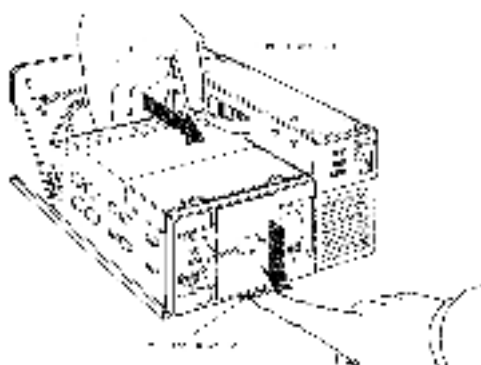
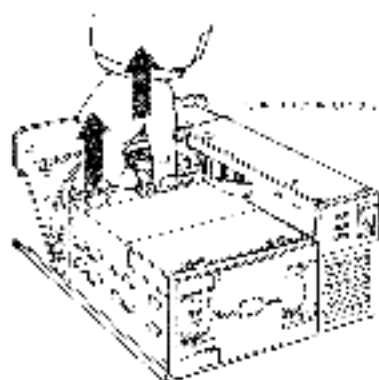
Inserting a Flexible Disk in Drive 1



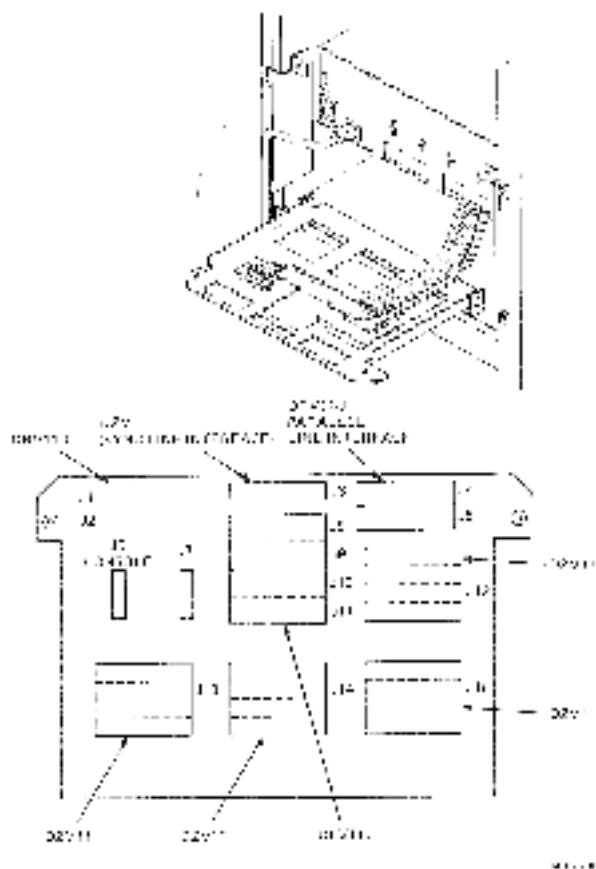
Opening the Drive 2 Door



Inserting a Flexible Disk in Drive 2



Removal of Flexible Disk Drive Signal and Power Cable



H340 Distributor Cable

TU58 TAPE CASSETTE UNIT

GENERAL

The TU58 Microtape II is a random access, fixed length block, mass storage tape unit. Tape cartridges are DIGITAL's proprietary reel to reel packages containing 42.7m (140 ft) long by 0.914mm (0.036 in) wide tape. The TU58 processor consists of an 8085 processor, supported by firmware in a 2Kb, read only memory (ROM).

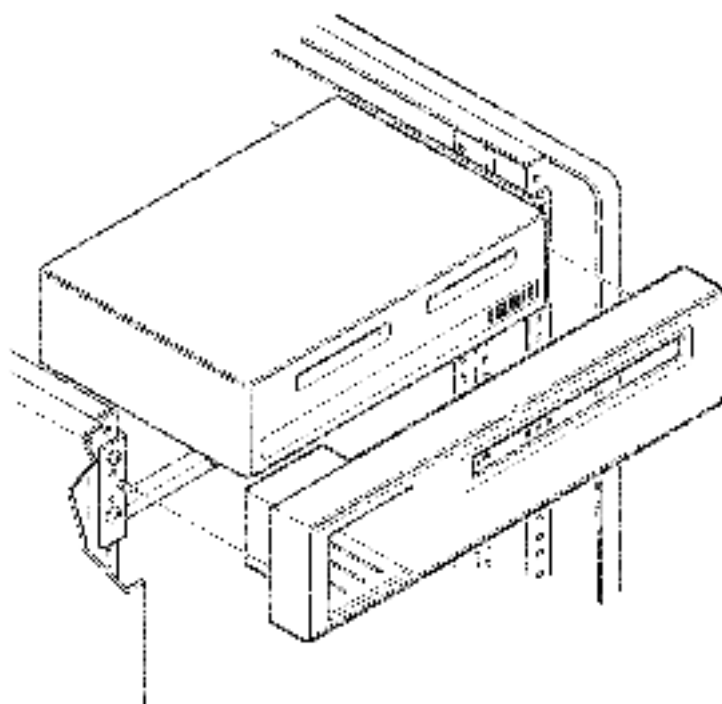
Power Consumption

Esomd plus 1 and 2 drives

- 11 W typical, drive running
- +5 V $\pm$ 5% @ 0.75 A (max)
- +12 V $\pm$ 10, $\pm$ 5% @ 1.2 A, peak
- 0.6 A average I/Oing
- 0.1 A idle

Backmount

- 80-120 Vac 180-250 Vac
- 47-63 Hz, 35 W (max)



Installing the Bazel

TU56

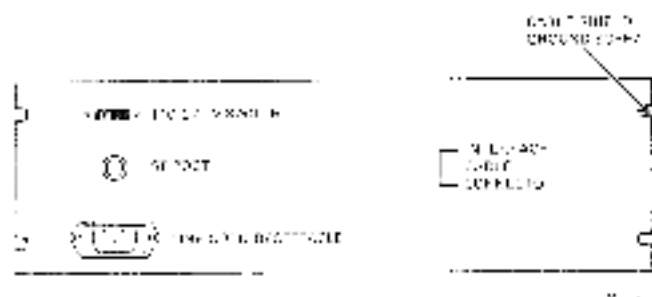
Related Documentation

TU56 Declass II User's Guide (LN-DTU56-UG)
TU56 Declass II Pocket Service Guide (PK-DTU56-PS)
TU56 Declass II Technical Manual (TK-DTU56-TM)
TU56 Declass II Maintenance Parts List (PL-DTU56-IP)
Field Maintenance Print Set (MP00747-15A)
Field Maintenance Print Set (MP01014-6A)
Field Maintenance Print Set (MP01013-VA)
Field Maintenance Print Set (MP01003-DD)

Model Distinctions

CA Rackmount

- Large chassis
- Two drives
- Serial interface controller board
- Switch selectable 120/240 Vac
- Detachable line cord
- 2 cartridges
- Host ROM for M111
- Two I/O cables (BC17A/R10) (2 16)
- Diagnostic kit (ZJ279-HA)



TU56-CA Rear Panel

CA Rackmount

Tabletop chassis

TU58-CA features with additional accessory assembly hardware kit (70-16753-00)

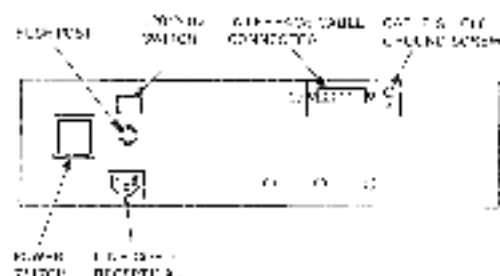


Figure 1

TU58-CA Rear Panel

CA Tabletop

Two drives

Serial interface controller board

E2 Tabletop

Two drives

Serial interface controller board

Two I/O cables (DC-7A-18/ BC17B-18)

Boot ROM for MV11-BA

Accessory assembly hardware kit (70-16753-00)

Field Maintenance Print Set (MF01014)

VA Tabletop

Two drives

Serial interface controller

DC Power cable (70-17569-00)

I/O interface cable (70-17568-17)

Two cartridges

MKV11-A2 boot ROM

Field Maintenance Print Set (MF01013)

Accessory assembly hardware kit (70-16753-01)

Accessories**TU58-DE**

Backmount kit for laptop versions

TU58-FC

Accessory kit with detachable line cord for hardware kit (70-16753-00)
User's guide
Field Maintenance Print Set (MP01014)

TU58-ED

Accessory kit with 120V/240V detachable line cord
Fuse for 230 Vac
Two cartridges
Two I/O cables (70-BC174-1B/BC178-1B)
Boot ROM for MR11-BA
Accessory assembly hardware kit (70-16753-00)
User guide
Field Maintenance Print Set (MP01014)

TU58-VE

Accessory kit with dc power cable (70-17569-1C)
I/O cable (70-17569-1F)
Two cartridges
MXV11-A2 boot ROM
User's Guide
Field Maintenance Print Set (MP01013)
Configuration Guide

TU58

Serial Interface Standards

To interface with the TU58, working with their appropriate cables are listed below. In accordance with RS422 (balanced) and RS423 (unbalanced) signal standards, the TU58 is compatible with devices complying with RS232-C.

NOTE

BC220-10 replaces BC17A-18 and BC17B-18. The new cable has an improved shield connection to comply with FCC regulations.

DL11 or DLV11	5.4 m (18 ft) 10 to 40 pin connector	BC17A-18
DLV11-J or MXV11	5.4 m (18 ft) 10 to 10 pin connector — BC17B-18 5.4 m (18 ft) 10 to 10 pin connector — BC20M-50	
FA	1.5 m (5 ft) 10 pin to DB25S female — BC20K-05 (null modem cable) 1.5 m (5 ft) 10 pin to DB25P male — BC21B-05 (Modem cable)	

TU58:POP-11 Toggle-In Port

This board drives 0 only.

1000/012701	1021/000012	1050/000000
1002/175500	1026/012700	1052/100711
1004/010701	1030/000004	1054/100375
1006/178304	1032/005761	1056/116123
1010/010100	1034/000007	1060/000002
1012/005212	1036/012700	1062/022703
1014/106712	1040/000020	1061/001000
1016/100370	1042/010062	1066/101371
1020/000000	1044/000002	1070/000007
1022/001305	1046/001352	

APPENDIX A DIAGNOSTIC MEDIA AVAILABILITY

Module Number	Option Name	Diagnostic and DEC/K11 File Names	Notes	Diagnostic and DEC/K11 Module Titles	Listing and Paper Tape PNs	R	R	R	R	R
						X	X	X	X	X
						0	0	0	0	0
						1	2	5	1	2
V4002 XX	V4001-0	V4WA99.B10	17, 19, 20, 21	K11-A Diagnostic	AC-82220-MC AK-82250-MC	4	13	19	19	20
V4204 XX	K01-H1 K01-H1W (LSI-11)	V4AA77.B17		LSI-11 Basic Instruction Test (Listing)	AC-81030-MC	4	18	18	19	20
				(Binary PT)	AK-81080-MC					
		V4AB77.B17		LSI-11 FIS Instruction Set Test (Listing)	AC-8180A-MC	4	18	18	19	20
				(Binary PT)	AK-8192A-MC					
		V4AC77.B17	0	LSI-11 FIS Instruction Set Test (Listing)	AC-81940-MC	4	✓	18	19	20
				(Binary PT)	AK-81970-MC					
		V4AD77.D10	5	LSI-11 Traps Test (Listing)	AC-81050-MC	4	10	10	9	20
				(Binary PT)	AK-81100-MC					
		V4AE77.B10		LSI-11 EK System Extender (Listing)	AC-8210A-MC	4	10	10	9	20
				(Binary PT)	AK-8212A-MC					
		V4AF77.B17	8	LSI-11 DIS Move & String Test (Listing)	AC-08140-MC	4	15	16	19	20
				(Binary PT)	AK-0217A-MC					
		V4AJ77.B17	8	LSI-11 DIS Decimate Instructions (Listing)	AC-8216A-MC	4	15	18	19	20
				(Binary PT)	AK-8227A-MC					
		V4AL77.B17	0	LSI-11 Trap Test (30K — FIS) (Listing)	AC-F012A-MC	4	12	15	16	20
				(Binary PT)	AK-F014A-MC					
		V4CP99.Q03		DEC/K11 Processor Test Module (Listing)	AC-F6R40-MC					
				(Binary PT)	AK-F6R50-MC					
		V4CR77.C01		DEC/K11 E/S Exercise Module (Listing)	EC-88R70-MC	1	14	18	19	20
				(Binary PT)	AK-88R80-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles	Listing and Paper Tape PNs	A	B	C	D	E
						X	X	X	X	X
						0	0	0	0	0
						1	2	3	4	5
M7340	DLV11	VKA577.BW	15, 16	DLV11 Test	(Listing) (Binary PT)	AC-0303B-MC	4	13	16	19 20
		XDLA77.OBJ	10	DEC/X11 DLV11 Exerciser Module	(Listing) (Binary PT)	AK-0305B-MC AK-E7100-MC	5	14	15	18 20
M7341	DRV11	VKA777.BW	3	DRV11 Test	(Listing) (Binary PT)	AC-6209D-MC	4	15	16	19 20
		XDRAP7.OBJ	13	DEC/X11 DRV11 Exerciser Module	(Listing) (Binary PT)	AK-F654D-MC AK-F655D-MC	5	15	16	19 20
M7342	MDV11-AA	NA								
M7344	MSV11-B	ZKMA77.BW	44	MO5: Core 0-124K Exerciser	(Listing) (Binary PT)	AC-8350F-MC AK-8351F-MC	4	18	19	15 20
		ZGMC77.BW	46	0-124K Memory Exerciser (10K)	(Listing) (Binary PT)	AL-8045F-MC AK-8046F-MC	12	13	2	15 20
M7810	RXV11	ZHXA77.BW	7, 14	RXV11 System Reliability TEST	(Listing) (Binary PT)	AC-9334B-MC AK-9337B-MC	7	10	10	19 20
		ZRXD77.DW	7	RXV11 Interface Diagnostic	(Listing) (Binary PT)	AC-9335F-MC AK-9344B-MC	7	10	16	18 20
		XRXA77.OBJ	7	DEC/X11 RXV11 Exerciser Module	(Listing) (Binary PT)	AC-E736E-MC AK-E737E-MC	3	16	18	19 20
M7946	DRV11-P	NA								

[illegible]

Module Number	Option Name	Diagnostic and DEC VAX11 File Names		Notes	Diagnostic and DEC VAX11 Module Titles	Listing and Paper Tape PNs	R	R	S	R	R	
		Z	X				K	L	L			
		O	O				O	O	O			
							1	2	5	1	2	
V7852	KWW11-A	VKWW02.PP	17, 18, 19, 20, 21		KWW11-A Diagnostic (Listing)	AC-95220-MOM	4	13	19	19	20	
						(Binary PT)	AK-A0750-MO					
		ZKWW07.05d			DEC VAX11 KWW11-A Exerciser Module (Listing)	AK-50905-MO	5	14	18	19	20	
					(Binary PT)	AK-50918-MO						
V7864	BVB11-A	VIBA02.BIT	22, 23, 24		BV11-A Diagnostic (Listing)	AC-A880A-MO	6	15	9	9	20	
						(Binary PT)	AK-A882A-MO					
		VBR02.BIT	22, 23, 24		BV11-A (20K) Diagnostic (Listing)	AC-F015A-MO	12	15	16	18	20	
						(Binary PT)	AK-F017A-MO					
		XIBA07.05d	25		BV11-A Exerciser Module (Listing)	AC-F914D-MO	5	4	18	19	20	
					(Binary PT)	AK-F915D-MO						
V7865	MBV11-C	ZKMB11.BIT	45		MC02 Core 0-124K Exerciser (Listing)	AC-B850F-MO	4	10	10	19	20	
						(Binary PT)	AK-B854F-MO					
		ZQB022.DIT	45		0-124K Memory Exerciser (16K) (Listing)	AC-9045F-MO	10	13	16	18	20	
					(Binary PT)	AK-9045F-MO						
V7867	DZV11	VDZ002.PP	26, 27		DZV11-4 Line Asynch MUX - OF 2 (Listing)	AC-A0777-MO	5	15	16	16	20	
						(Binary PT)	AK-A079A-MO					
		VDZ022.BIT	26, 27		DZV11-4 Line Asynch MUX - OF 2 (Listing)	AC-A080A-MO	5	15	16	16	20	
						(Binary PT)	AK-A080A-MO					
		VDZ076.BIT	26, 27		DZV11 Cable and Echo Test (Listing)	AC-A041A-MO	5	15	16	16	20	
					(Binary PT)	AK-A041A-MO						

Module Number	Option Name	Diagnostic and DEC-V11 File Names		Diagnostic and DEC-V11 Module Titles	Listing and Paper Tape PNs	A D I	K U 2	R O 5	R O 1	H L L
M8012	RDV11 AA	VLZD??BIF	28 22 30	DZV11 Overdrive for IDEF (Listing)	AK-A056A-MC	9	15	18	19	20
		XDZB??LOB		DZC11X11 DZV11 Exerciser Module (Listing)	AK-A057A-MC	5	17	18	19	20
		VMBA??BIF		RDV11-44 Diagnostic (Listing)	AK-E811C-MC	8	13	15	19	20
		XDMD??ODJ		DZC11X11 DZV11 Exerciser (Binary PT)	AK-D050C-MC	1	17	18	19	20
M8013- M8014	RLV11	VRLA??BIF	7 34 36	RLV11 RLO1 Diskette Test (Listing)	AK-F060C-MC	10	17	18	19	20
		ZRLB??BIF		RLV11 RLV11 Controller Test 1 (Listing)	AK-B109a-MC	10	17	18	19	20
		ZRLB??BIF		RLV11 RLV11 Controller Test 2 (Listing)	AK-F111D-MC	10	17	18	19	20
		ZRLI??BIF		RLO1-02 Drive Test 1 (Listing)	AK-F112B-MC	10	17	18	19	20
		ZRLI??BIF		RLV11-02 Drive Test 2 (Listing)	AK-F119C-MC	10	17	18	19	20
		ZRLK??BIF		RLV11-02 Performance Exerciser (Binary PT)	AK-F116C-MC	10	17	18	19	20
		ZRLM??BIF		RLV11-02 Performance Exerciser (Binary PT)	AK-F122B-MC	10	17	18	19	20
		ZRLN??BIF		RLO1-02 Drive Compatibility Test (Listing)	AK-F124B-MC	10	17	18	19	20
		ZRLM??BIF		RLO1-02 Drive Compatibility Test (Binary PT)	AK-F131B-MC	11	17	18	19	20
		ZRLM??BIF		RLO1-02 Bad Sector File Test (Listing)	AK-F128B-MC	11	17	18	19	20
		ZRLM??BIF		RLO1-02 Bad Sector File Test (Binary PT)	AK-F135B-MC					

Module Number	Option Name	Diagnostic and DEC/X11 File Names	Notes	Diagnostic and DEC/X11 Module Titles	Listing and Paper Tape PNs	R X 0 1	R X 0 2	R K 0 5	R L 0 1	R L 0 2
MB016	KPV11-X	ZRLV??BI?	7,39-40	RLO102 Drive Test 3	(Listing) (Binary PT)	AC-F843A-MC	11	17	18	19 20
		XRLA??OBJ	7	RL110RLV110RLD1-R, DP Exerciser	(Listing) (Binary PT)	AC-E955D-MC	6	10	13	18 20
		VKDA??R?	41,42,43	KPV11-A Diagnostic	(Listing) (Binary PT)	AK-A056D-MC	3	18	18	19 20
MB017	DIV11-E	VQVA??BI?	11a	GV11-E On-Line Test	(Listing) (Binary PT)	AC-B107B-MC	6	10	13	18 20
		XELA??OBJ	11b	DEC/X11 DI 11 Exerciser Module	(Listing) (Binary PT)	AC-E709J-MC	5	14	18	18 20
		VKHA??DI?	44	KUV11-AA (LSI WOS) Diagnostic	(Listing) (Binary PT)	AC-E108A-MC	4	13	18	19 20
MB020	DPV11-XX	XKUA??OBJ	45	DEC/X11 KUV11-AA Exerciser Module	(Listing) (Binary PT)	AC-E104E-MC	5	14	18	19 20
		VDPV??BI?		DPV11 Functional Diagnostic	(Listing) (Binary PT)	AC-E883B-MC	4	13	18	19 20
		XDPV??OBJ		DPV11 Module		AC-S5329-MC	4	13	18	19 20
MB021	MDV11-BA	VMDA??DI?		LSI11 UVPRONRAM (MDV11 PA) Test	(Listing) (Binary PT)	AC-B103A-MC	3	15	18	19 20
		ZKMA??R?	46,46	MOS1 Core 0-124K Exerciser	(Listing) (Binary PT)	AC-B105A-MC	4	13	18	19 20
		ZDNCV??BI?	46,46	0-124 K Memory Exerciser (10K)	(Listing) (Binary PT)	AC-B654E-MC	12	13	18	19 20

Module Number	Option Name	Diagnostic and DFC/X11 File Name(s)	Notes	Diagnostic and DFC/X11 Module Titles	Listing and Paper Tape PNs	R X 0 1	R X 0 2	R K 0 3	R L 0 1	R L 0 2
M6044- M6045	MEV11-DX/ MEV11-FX	ZCMV99.B1?	4a	MOS/ Core 0-124K Exerciser	(Listing) AC-8850I-MC	4	13	18	19	20
		ZCMC??DI?	4b	0-124K Memory Exerciser (16K)	(Binary PT) AK-8854I-MC (Listing) AC-8045F-MC (Binary PT) AK-8045F-MC	12	13	18	19	20
M6047	MXV11-AX	VMXA??B1?	4c	MXV11-AX Diagnostic	(Listing) AC-F656A-MC (Binary PT) AK-F656A-MC	12	15	18	19	20
		ZKMA97.B?	4d	MOS/ Core 0-124K Exerciser	(Listing) AC-8850F-MC (Binary PT) AK-8850F-MC	4	8	18	19	20
		ZCMC??B1?	4e	0-124K Memory Exerciser (16K)	(Listing) AC-8045F-MC (Binary PT) AK-8045F-MC	12	13	0	18	20
		XDLAT? DEJ	4f	DFC/X11 DCL1 Exerciser Module	(Listing) AC-8703J-MC (Binary PT) AK-8710J-MC	5	14	16	18	20
M6048	MDV11-C	NA								
M6049	DMV11-J	VDMC??B1?	4g	DMV11 Diagnostic Test Part 1	(Listing) AC-F756A-MC (Binary PT) AK-F757A-MC	8	15	18	19	20
		VDMD??B1?	4h	DMV11 Diagnostic Test Part 2	(Listing) AC-F756A-MC (Binary PT) AK-F760A-MC	8	15	18	19	20
M6052	DMV11	VDMA??B1 VDMB??B VDMC??B VDMD??B		DMV11 MOTOROL Diagnostic No. 1 DMV11 MOTOROL Diagnostic No. 2 DMV11 Line Unit Diagnostic No. 1 DMV11 Line Unit Diagnostic No. 2						

Module Number	Option Name	Diagnostic and DEC-X11 File Names	Notes	Diagnostic and DEC-X11 Module Titles	Listing and Paper Tape PNs	R X 0 1	R X 0 2	R X 0 5	R L 0 1	R L 0 2
MSV1	MSV111	VM5A??B ZKM4??B		Memory Exerciser MOS 0.104K Exerciser	AC-8735A-MC AK-8436A-MC AC-8650F-MC AK-8854F-MC					
KB120	KBF11-A	JKD4??B? JKD6??B? JKD0??B? JKD0??B? KCPA??OBJ KCP5??OBJ KFP4??OBJ	30 31	KTF11-AA Diagnostic KBF11-AA Diagnostic KBF11-AA Diagnostic No. 1 KBF11-AA Diagnostic No. 2 DEC-X11 Processor Test Module DEC-X11 BUS Exerciser Module DEC-X11 I/P11 Exerciser Module	(Listing) (Binary PT) (Listing) (Binary PT) (Listing) (Binary PT) (Listing) (Binary PT) (Listing) (Binary PT) (Listing) (Binary PT)	AC-F139C-MC AK-F106C-MC AC-F141C-M1 AK-F137C-MC AC-F244B-MC AK-F240B-MC AC-F244B-MC AK-F242B-MC AC-C864G-MC AK-C865G-MC AC-F867J-MC AK-F869J-MC AC-F749C-MC AK-F740C-MC	0 0 1 1 0	13 15 15 14 14 13	18 19 19 19 19 19	20 20 20 20 20 20
MS135	FPE11	JFPA??B? JFPB??B?		FLT PNT Diagnostic No. 1 FLT PNT Diagnostic No. 2	AC-F405C-MC AK-F406C-MC AC-5445A-MC AK-5445A-MC					

Module Number	Option Name	Diagnostic and DSC-X11 File Names	Notes	Diagnostic and DSC-X11 Module Titles	Listing and Paper Tape PNs	P X 0 1	R X 0 2	R K 0 5	R L 0 7	R L 0 2
AD12	ADV11-A	VADA000R	1	ADV11 Performance Test	(Listing) (Binary PT) (DSC-PT PT-0)	AC-B174D-MC AK-B176D-MC ZJ76D-RS	8	13	16	19 20
		XAD07700R	2,3	DSC-X11 ADV11 Exerciser Module	(Listing) (Binary PT)	AC-B323R-MC AK-B324R-MC	1	14	16	19 20
AD026	ADV11-C	VADA775R		ADV11 Diagnostic Test						
AD001	ADV11-A	VADA728R		ADV11 Diagnostic Test	(Listing) (Binary PT) (DSC-PT R11)	AC-B138A-MC AK-B172A-MC ZJ249-RS	8	15	16	19 20
		XAD0000R		DSC-X11 ADV11 Exerciser Module	(Listing) (Binary PT)	AC-F317B-MC AK-F318C-MC	1	14	16	19 20
AD008	ADV11-C	VADA775R		ADV11-C Diagnostic Test						
AD002	ADV11-C	VADA775R		ADV11-C Diagnostic Test						
DB027 B003	BMV11-A	ZBMA075BR	4a	MB01 Core 0-124K Exerciser	(Listing) (Binary PT)	AC-B850F-MC AK-B854F-MC	4	10	18	2 20
		ZQMC075B	4b	0-124K Memory Exerciser (16K)	(Listing) (Binary PT)	AC-9C45F-MC AK-9C48G-MC	12	13	18	19 20

Notes

1. Wraparound test and sub-tests require Berg test connector ZH-12834-00.
2. Requires an analog ground on any channel to be tested.
3. May be run asynchronously if KVVH is present in system. If run asynchronously, XKWE??OBJ must be deselected from the DEC/X menu.
- 4a. Memory space under test should be contiguous and read/write. For systems having noncontiguous memory, the memory boundaries must be defined by the operator before running the program. This diagnostic requires 5K of memory space to run in.
- 4b. This test will run successfully only on an i1334 processor with a minimum of 128K of memory.
5. LTC must be disabled.
6. VKA???.BI? and VKA???.BI? should be run on the CPU prior to running this test.
7. Scratch media must be mounted in drives to be tested before starting the diagnostic.
8. ZRKJ???.BI?, ZRKK???.BI?, ZRKL???.BI?, and ZRKI???.BI? (if needed) should be run on subsystem before running this test.
9. ZRKJ???.BI? should be run on the subsystem before running this test.
10. ZRKJ???.BI? and ZRKK???.BI? should be run on the subsystem before running this test.
- 11a. A wraparound test connector must be installed to run this test if the connector is not available from stock. The F.E. must make one up himself. The following instructions (excerpted from Tech Tip PDP-11/38 TT-11) tell how this is done. The following items are required:

1 Berg connector	(12-13915-15)
4 Berg pins	(12-13309-07)
#22 wire	(90-07350-00)

Crimp a short length of wire between two Berg pins. Make up two sets of these. Install one set from pin F to pin J, and one set from pin E to pin M of the Berg connector.

- 11b. To completely exercise the modem control portion of the DLV11-E, a special wraparound connector (H215) must be installed on the modem end of the I/F cable. This test connector connects certain control lines as well as the data lines.

12. The test has baud rate dependent configuration requirements.

Baud Rate	No. of Stop Bits	No. of Bits

110	2	8

All others	1	8

13. Requires DCCDR test cable for full test of module's data lines.
14. ZHX272.BIT should be run on the subsystem before running this test.
15. If a REV11 is in the system, DMA refresh must be disabled and CPU refresh must be enabled.
16. EBITA connector required for external feedback testing.
17. If customer hardware is connected to the KVV11 which could inject signals on ST1, ST2 or slave in inputs, it must be disconnected from the inputs.
18. All switches in switch pack 2 should be left off unless you are instructed otherwise.
19. I/O signal test no. 1 (ST1 in, ST2 out): install a jumper between J1-SS (ST2 out) to J1-VV (ST1 in)

Switch Pack 2

Switch	State
1	Off
2	On
3	Off
4	Off
5	On
6	On
7	Not used.

Use a program starting address of 210

20. I/O signal test no. 2 (clock overflow tests): install a jumper between J1-RP (clock overflow) to J1-TT (ST2 in).

Switch Pack 2

Switch	State
1	Off
2	Off
3	Off
4	On
5	Off
6	On
7	Not used

Use a program starting address of 214.

21. I/O signal test no. 3 (ST1 out, ST2 in): install a jumper between J1-UU (ST1 out) to J1-TT (ST2 in).

Switch Pack 2

Switch	State
1	Off
2	Off
3	Off
4	On
5	On
6	On
7	Not used.

Use a program starting address of 220.

22. Test may be run with a "known good module" in the system for comparison. The good module should be inserted second (also initially) on the bus, with a cable connecting it and the module under test.

"known good module" address = 760100
"known good module" vector = 860

23. Starting restrictions:

If a free running clock, such as 100 Hz from the power supply, is attached to the DEYNT bus line on ACV C/D/E systems, an interrupt to location 100 will occur when using the "GO" and "IL" commands. This will happen prior to the program executing the first instruction. This program cannot disable the DEYNT bus line by inhibiting interrupts.

User systems requiring a free-running clock attached to the IBV11-A can temporarily avoid this situation by setting the PSW to 200, loading the PC with the starting address, and then using the "P" command instead of using the starting address and the "G" command.

Before using the "P" command, the PSW can be set to 200 to inhibit interrupts after loading the absolute loader.

24. Possible program bombs:

The first two tests check to see if the IBV11-A responds to the address the program thinks it is at. If not, a bus error occurs.

Bus errors may alter the present contents of location 4 before the trap is executed. Program control may be transferred to an area of the program which is not set up to handle the trap. Or, control may be passed to some totally unknown and irrelevant piece of code residing accidentally in memory. If this occurs, the program will most probably bomb, and it may also revert to parts of itself. In this occurrence, the program must be reloaded before proceeding.

25. If the IB bus cable is not removed from the module under test, any errors which are detected could be from some device out on the IB bus and not necessarily from the IBV11-A.

26. If run in staggered maintenance mode, an H329 staggered turn-around connector is required.

27. If run in external maintenance mode, an H325 cable turn-around connector is required on all lines which have been selected to be tested.

28. This test assumes that the module under test resides in the same backplane where the line time clock is generated.

29. Test 3 assumes that switch no. 5 of E21 is in the ON position.

30. For the rocker switch test, the operator should specify the configuration for the module under test.

31. VRLA??RI? should be run on the subsystem before running this test.

32. VRLA??EI? and ZRLO??BI? should be run on the subsystem before running this test.

33. A 300V11 programmable line clock is required to run test no. 34.

34. VRLA??BI?, ZRLG??BI?, and ZRLH??BI? should be run on the subsystem before running this test.
35. A KWW11 programmable line clock is required for some tests.
36. VRLA??HI?, ZRLG??BI?, ZRLH??BI?, and ZRLI??BI? should be run on the subsystem before running this test.
37. VRLA??BI?, ZRLG??BI?, ZRLH??HI?, ZRLI??BI?, ZRLJ??BI?, and ZRLN??HI? should be run on the subsystem before running this test.
38. VRLA??BI?, ZRLG??HI?, ZRLH??BI?, ZRLI??HI?, ZRLJ??BI?, ZRLK??BI, and ZRLN??BI? should be run on the subsystem before running this test.
39. VRLA??HI?, ZRLG??BI?, ZRLH??HI?, ZRLI??BI?, and ZRLJ??HI? should be run on the subsystem before running this test.
40. A KWW11 programmable line clock is required for tests 1 and 4.
41. To check the power fail circuitry, nonvolatile memory must be in the first 4K of memory.
42. Power up option no. 1 should be selected on the CPU module for power fail testing.
43. The module should be in the standard factory configuration.
Jumpers in: W1-W5, W7, W8, W11, W13-W15
Jumpers out: W6, W9, W10, W12
44. If the test is to be run in all address modes, then an extender card and a special test cable (17-00124-01) are required.
45. The exerciser may be run with the module in address modes 1 or 3 only.
46. This test may be run only if RAM is present on the board.
47. All channels must be configured to the same bit word length.
48. A wraparound connector (H3270) is required for the data wraparound tests for each of the lines to be tested.
49. Require a RG59W-92 cable to be installed between the Serp connectors. The cable should have a tight twist in it.

- 50. J4D0??BP should be run on the first 19K of memory before running this test.
- 51. JK00??BP should be run on the module before running this test.

Media Availability

No.	Media Package Identifier	Title	Notes	Media P/Ns	Documentation Media Kit P/Ns
1	CZZGG??	DXDP + 71 DEC/X11 EXEC 1	1	AS-96457-M?	ZJ271-RY
2	CZZGL??	DXDP + 71 DEC/REFRKT1		AS-96507-M?	
3	CZZGO??	DXDP + 81 RX11 DAG		AS-96509-M?	
4	CZZGY??	DXDP + 85 LSI/FLP 1	1	AS-96637-M?	ZJ271-RY
5	CZZOZ??	DXDP + 85 DEC/X11 EXEC 2	1	AS-96874-M?	ZJ271-RY
6	CZZHD??	DXDP + 90 DEC/X11 EXEC 3	-	AS-96689-M?	ZJ271-RY
7	CZZHE??	DXDP + 91 LSI/FLP 2	1	AS-96889-M?	ZJ271-RY
8	CZZHG??	DXDP + 98 LSI/FLP 3	1	AS-96719-M?	ZJ271-RY
9	CZZHQ??	DXDP + 18 LSI/FLP 4	1	AS-96847-M?	ZJ271-RY
10	CZZH2??	DXDP + 50 HIC2/DAG no. 1	1	AS-96479-M?	ZJ271-RY
11	CZZH3??	DXDP + 50 HIC2/DAG no. 2	1	AS-97530-M?	ZJ271-RY
12	CZZH4??	DXDP + 50 LSI/FLP 5	1	AS-98049-M?	ZJ271-RY
13	CZZMC??	DYDP + 8 LSI/FLP no. 1	2	BA-F0217-M?	ZJ271-RX
14	CZZMD??	DYDP + 4 DEC/X11 no. 1	2	BA-F0229-M?	ZJ271-RX
15	CZZMT??	DYDP + 20 LSI-11 no. 2	2	BA-F0489-M?	ZJ271-RX
16	CZZMU??	DYDP + 31 DEC/X11 no. 2	2	BA-F0487-M?	ZJ271-RX
17	CZZMA??	DYDP + 26 LSI-11 no. 3	2	BA-F0489-M?	ZJ271-RX
18	CZZZD??	-SI-11 DYDP - Diagnostic PKG		AN-98357-M?	ZJ278-RY
19	CZ71A??	FLP -- (HIC1) Diagnostic PKG no. 1		AX-C0809-M?	ZJ272-RQ
20	CZ71N??	FLP -- (HIC2) Diagnostic PKG		BC-F9169-M?	ZJ274-RQ

Notes

1. Documentation/media kit ZJ271-RY contains all of these offerings as well as all of the applicable documentation.
2. Documentation/media kit ZJ271-RX contains all of these offerings as well as a set of the applicable documentation.

APPENDIX B FLOATING ADDRESSES / VECTORS

FLOATING ADDRESSES

The conventions for the assignment of floating addresses for modules on the LSI-11 bus are the same as UNIBUS devices. UNIBUS devices are used to explain the ranking sequence.

The floating-address convention used for communications and for other devices that interface with the PDP-11 series of products assigns addresses sequentially starting at x60 000 (or 100 000) and proceeds upward to 768 776 (or 163 776). For the sake of compatibility with UNIBUS conventions, addresses are expressed as consisting of 18 bits (7XX XXX) rather than 16 bits (XXX XXX).

Floating addresses are assigned in the following sequence:

Rank	UNIBUS Device	LSI-11 Device
1	DJ11	
2	DH11	
3	DQ11	
4	DI11	DUX11
5	DUP11	
6	LK11A	
7	DMC11	
8	DZ11	DZV11
9	KWD11	
10	RT11 (extra)	RLV11 (extra)

FLOATING VECTORS

The conventions for the assignments of floating vectors for modules on the LSI-11 bus will adhere to those established for UNIBUS devices. UNIBUS devices are used to explain the priority ranking for floating vectors and are included in the subsequent table of trap and interrupt vectors as a guide for the user.

The floating vector convention used for communications and for devices that interface with the PDP-11 series of products assigns vectors sequentially starting at 300 and proceeding upward to 777. (Some LSI-11 bus modules, such as the DLV11 and DRV11, have an upper vector set of 377.) The following table shows the sequence for assigning vectors to modules. It can be seen that the first vector address, 300, is assigned to the first DLV11 in the system. If another DLV11 is used, it would then be assigned to a 11th DLV11e (up to a maximum of 32). addresses are then assigned consecutively to each unit of the next, higher-ranked device (DRV11 or DLV11-E, and so forth), then to the other devices according to their rank.

Ranking for Floating Vectors
(Start at 300 and proceed upward.)

Rank	UNIGUS	LSI-11 Bus
1	DC11	DLV11, -F, -J
2	KL11, DL11-A, -B	
3	DP11	
4	DM11-A	
5	DN11	
6	DM11-BB	DNV11-B DNV11
7	DN11-A	
8	DN11-C	
9	PA611 Reader	
10	PA611 Punch	
11	DT11	DLV11-E
12	DX11	
13	DL11-C, -D, -E	
14	DJ11	
15	PH11	
16	BT40	KWV11 DLV11
17	IPS11	
18	DO11	
19	KW11-W	
20	DU11	

APPENDIX C

LSI-11 BUS SPECIFICATION

GENERAL

NOTE

This is not the complete LSI-11 bus specification, but is included to permit users to design and implement typical interfaces to the LSI-11 bus.

The processor, memory, and I/O devices communicate via 36 bidirectional signal lines that constitute the LSI-11 bus. Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are functionally divided as follows:

- 19 Data/address lines – BDA[0-17,00]
- 6 Data transfer control lines – HRSZ, RDIN, DDOUT, DAPLY, BSYNC, BWTBT
- 4 Direct memory access control lines – DDMG, DDMG, BBACK
- 6 Interrupt control lines – DCVNT, BIAK, DACK, SIRQ5, BIRQ6, BIRQ7
- 5 System control lines – DDCLK, BHALT, BINIT, BPOK, BREF

Most LSI-11 bus signals are bidirectional and use terminations for a negated (high) signal level. Devices connect to these lines via high-impedance bus receivers and open-collector drivers. The asserted state is produced when a bus driver asserts the line low. Although bidirectional lines are electrically bidirectional (any point along the line can be driven or received), certain lines are functionally unidirectional. These lines communicate to or from a bus master (or signal source), but not both. Interrupt acknowledge (B-ACK) and direct memory access grant (DDMG) signals are physically unidirectional in a daisy-chain fashion. These signals start at the processor output signal pins. Each is received on device input pins (BIAK) or (DDMGi) and conditionally retransmitted via device output pins (BIAKO or DDMGO). These signals are received from higher priority devices and are retransmitted to lower priority devices along the bus.

Master/Slave Relationship

Communication between devices on the bus is asynchronous. At master/slave relationship exists throughout each bus transaction. At any time, there is one device that has control of the bus. This controlling device is called the "bus master." The master device controls the bus when communicating with another device on the bus, called the slave. The bus master (typically the processor or a DMA device) initiates a bus transaction. The slave device responds by acknowledging the transaction in progress and by receiving data from, or transmitting data to, the bus master. LSI-11 bus control signals transmitted or received by the bus master or bus slave device must complete the sequence according to bus protocol.

The processor controls bus arbitration (i.e., who becomes bus master at any given time). A typical example of this relationship is the processor as master, fetching an instruction from memory (which is always a slave). Another example is a disk as master, transferring data to memory as slave. Theoretically, any device can be master or slave, depending on the circumstances. Communication on the LSI-11 bus is interlocked so that for each control signal issued by the master device, there must be a response from the slave in order to complete the transfer. It is this master/slave signal protocol that makes the LSI-11 bus asynchronous. The asynchronous operation precludes the need for synchronizing with clock pulses.

Since bus cycle completion by the bus master requires response from the slave device, each bus master must include a timeout error circuit that will abort the bus cycle if the slave device does not respond to the bus transaction within 10 microseconds.

The actual time before a timeout error occurs must be longer than the reply time of the slowest peripheral or memory device on the bus.

The signals and pin assignments are tabulated as shown below. The pin nomenclature is for reference and is only required when examining DIGITAL modules and circuit schematics. A functional description of the LSI-11 bus pins and signals is also found below.

Categories of LSI-11 Bus Signal Lines

Number of Pins	Functional Category	DIGITAL's Nomenclature		(Name) (Pin)			
10	Data/Address	DDA03, A02	DDA04, A03	DDA05, D02	DDA06, D03	DDA07, A04	DDA08, A05
3	Unit Control	DDCHT, A09	DDCHY, A07	DDIN, A08	DDFMO, A02	DDTEST, A09	DDRST, A09
6	Interrupt Control	RI003, R01	RI006, A01	RI005, A01	RI004, A02	RIAK0, A02	RIAK1, A02
4	DMA Control	SDMR, A01	SDHGO, A02	SDMGI, A02	SDACK, B01		
6	System Control	EH-ALT, A01	BRE-*, A01	LOCK, A01	LOCK, A01	DDVMI, B01	RINIT, A02
8	5 Vdc	AA2, BA2, D01					
2	12 Vdc	A02, D02					
2	12 Vdc	A02, B02					
2	-12 V*	A01, B01					
1	0 V*	A01, A02, A03 (pin 40)					
8	GRU	A02, A03, A04, A05, A06, B02, B01, B01, B01					
8	0-READER	A01, A06, A01, A01, B01, B01, B01, B01					
7	MEMORIES	A01, A01, B01, B01, B01, B01, B01					
2	PEPARES	A01, B01					

* Railcay

Functional Descriptions

Bus Pin	Signal Name(s)	Signal Function
AA1	DIRP5 L	Interrupt request priority level 5
AB1	DIRP6 L	Interrupt request priority level 6
AD1	BDA116 L	Address line 16 during addressing protocol; memory error line during data transfer protocol
AD1	BDA117 L	Address line 17 during addressing protocol; memory error enable during data transfer protocol
As1	SSPARP1 (alternate: +5 B)	Special spare – not assigned or used in DIGITAL cable or backplane assemblies; available for user connection. Optionally, this pin may be used for +5 V battery (+5 B) backup power to keep critical circuits alive during power failures. A jumper is required on LSI-11 bus options to open (disconnect) the +5 B circuit in systems that use this line as SSPARP1.
AF1	SSPARC2	Special spare – not assigned or used in DIGITAL cable or backplane assemblies; available for user interconnection. In the highest priority device slot, the processor may use this pin for a signal to indicate its RUN state.
AH1	SSPARC3 RUN	Special spare – not assigned or used in DIGITAL cable or backplane assemblies; available for user interconnection.
AJ1	GND	Ground – System signal ground and dc return
AK1 AL1	MSPARCA MSPARCB	Maintenance Spare – Normally connected together on the backplane at each option location (not buses connection).
AM1	GND	Ground – System signal ground and dc return

Functional Descriptions (Cont)

Bus Pin	Signal Mnemonic	Signal Function
AA1	HDMH	Direct memory access (DMA) request – device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYMT.L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO.L. The device responds by negating BDMR.L and asserting BSACK.L.
AP1	DIHALT.L	Processor halt – When DIHALT.L is asserted, the processor responds by going into console ODT mode.
AR1	BREF.L	Memory refresh – used to refresh dynamic memory devices. The LSI-11 processor microcode features automatic refresh control. BREF.L is asserted during this time to override memory bank selection encoding. Interrupt requests and SaaS are blocked out during this time.
AS1	+5 V or -12 V (battery)	-12 or +5 Vdc battery backup power to keep critical circuits alive during power failures. This signal is not used to AS1 in all DIGITAL backplanes. A jumper is required on all LSI-11 bus boards to open (disconnect) the backup circuit from the bus in systems that use this line at the alternate voltage.
AT1	GND	Ground – system signal ground and so return.
AU1	PSPARE*	Power spare #1 (not assigned a function, not recommended for use) – If a module is using +12 V (or SRP) and if the module is accidentally inserted back wrong in at the backplane, +12 Vdc appears on pin AU1.
AV1	+5 V	+5 V battery power – secondary +5 V power connection. Battery power can be used with certain devices.

Functional Descriptions (Cont.)

Bus Pin	Signal Mnemonic	Signal Function
BA1	DOCKOK_H	DC power OK - Power supply-generated signal that is asserted when there is sufficient dc voltage available to sustain reliable system operation.
BD1	HPCK_H	AC power OK - Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BD1 BD1 BD1 BD1 BD1	SSPARE 4 SSPARE 5 SSPARE 6 SSPARE 7 SSPARE 8	Special spares - not assigned or used in DIGITAL's cable and backplane assemblies available for user interconnections. Caution: These pins may be used as test points by DIGITAL in some options.
BJ1	GND	Ground - system signal ground and dc return.
DK1 DL1	MSPARE0 MSPARE0	Maintenance spares - manually connected together on the backplane at each option location (not a bus-to-bus connection).
BM1	GND	Ground - system signal ground and dc return.
DN1	BSACK_L	This signal is asserted by a DMA device in response to the processor's BDMG0_L signal, indicating that the DMA device is bus master.
HP1	BRQ7_1	Interrupt request priority level 7.
DR1	SEVNT1_1	General event interrupt request - When the processor latches the leading edge and arbitrates as a level 6 interrupt. A typical use of this signal is a line clock interrupt.
BS1	-12 B	-12 Vdc battery backup power (not used to AS1 in all DIGITAL backplanes).
BJ1	GND	Ground - system signal ground and dc return.
BU1	PSPARE2	Power spare 2 (not assigned a function, not recommended for use) - If a module is using -12 V (on pin AB2) and if the module is accidentally inserted backwards in the backplane, -12 Vdc appears on pin BU1.

Functional Descriptions (Cont)

Bus Pin	Signal Mnemonic	Signal Function
AV1	V ₁₅	15 V power – Normal +5 Vdc system power
AA2	V ₁₅	15 V power – Normal +5 Vdc system power
AB2	V ₁₂	12 V Power – +12 Vdc (optional) power for devices requiring this voltage.
AC2	GND	Ground – system signal ground and dc return
AD2	V ₁₂	-12 V Power – -12 Vdc system power
AE2	BDOUT L	Data Output – BDOUT, when asserted, implies that valid data is available on BDAL (+0.5) L and that an output transfer with respect to the bus master device is taking place. BDOUT L is deasserted with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	Reply – BRPLY L is asserted in response to BDIN L or BDOUT L and during IAK transaction. It is generated by a slave device to indicate that it has placed its data on the HDAL bus or that it has accepted output data from the bus.
AH2	BDIN L	Data Input – BDIN L is used for two types of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response (BRPLY L). BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring. The master device must deassert input data from BRPLY L.

Functional Descriptions (Cont)

Bus Pin	Signal Mnemonic	Signal Function
AJ2	BSYNC L	Synchronize - BSYNC L is asserted by the bus master device to indicate that it has placed an address on the bus. The transfer is in process until BSYNC L is negated.
AJ2	BWIDT L	Write/Data - BWIDT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATA or DATOH), rather than an input sequence. 2. It is asserted during BDCOUT L in a DATA bus cycle, for byte addressing.
AJ2	BR04 L	Interrupt request priority level 4
AM2 AN2	DIACK L DIAKO L	Interrupt acknowledge - In accordance with interrupt protocol, the processor asserts DIAKO L to acknowledge the numbering of an interrupt. The bus transmits this to DIAKI L of the next priority device (electrically closest to the processor). This device accepts the interrupt acknowledge under two conditions: 1. The device requested the bus by asserting an interrupt, and 2. The device has the highest priority interrupt request on the bus at that time. If these conditions are not met, the device asserts DIAKO L to the next device on the bus. This process continues in a daisy-chain fashion until the device with the highest interrupt priority receives the interrupt acknowledge (IAKI) signal.
AP2	BB57 L	Bank 7 select - The bus master asserts this signal to reference the I/O page (including that portion of the I/O page reserved for non-existent memory). The address is BDAL 0 12 L when BB57 L is asserted in the address within the I/O page.

Functional Descriptions (Cont)

Bus Pin	Signal Mechanics	Signal Function
AR2 AS2	BDMAS L BDMAS L	Direct memory access grant – The bus arbitrator asserts this signal to grant bus mastership to a requesting device, according to bus mastership protocol. The signal is passed in a daisy chain from the arbitrator (ss BDMOS L) through the bus to BDMAS L of the next priority device (electrically closest device on the bus). This device accepts the grant only if it requested to be bus master (by a BDMO L); if not, the device passes the grant (asserts BDMOS L) to the next device on the bus. This process continues until the requesting device acknowledges the grant.
AT2	DINIT L	Initialize – This signal is used for system reset. All devices on the bus are to return to a known, initial state; i.e., registers are reset to zero, and logic is reset to state 0. Exceptions should be completely documented in programming and engineering specifications for the device.
AV2	BDAL0 L	Data/address line 00.
AV2	BDAL1 L	Data/address line 01.
BA2	+5	+5 Vdc power.
BB2	+12	+12 Vdc power (optional, not required for DIGITAL I/O-11 hardware options).
BL2	GND	Power supply return.
BD2	+12	+12 Vdc power.
BE2	BDAL2 L	Data/address line 02.
BF2	BDAL3 L	Data/address line 03.
BH2	BDAL4 L	Data/address line 04.
BJ2	BDAL5 L	Data/address line 05.

Functional Descriptions (Cont)

Bus Pin	Signal Mnemonic	Signal Function
0K2	BDAL6 L	Data/address line 06.
BL2	BDAL7 L	Data/address line 07.
BM2	BDAL8 L	Data/address line 08.
DN2	BDAL9 L	Data/address line 09.
SP2	BDAL10 L	Data/address line 10.
BR2	BDAL11 L	Data/address line 11.
BS2	BDAL12 L	Data/address line 12.
BT2	BDAL13 L	Data/address line 13.
BU2	BDAL14 L	Data/address line 14.
BV2	BDAL15 L	Data/address line 15.

DATA TRANSFER BUS CYCLES

Data transfer bus cycles are as follows:

Bus Cycle Mnemonic	Description	Function (with respect to the bus master)
DAT	Data word input	Read
DATO	Data word output	Write
DATOB	Data byte output	Write byte
DAT O	Data word input/output	Read modify-write
DATOB	Data byte input/byte output	Read modify-write byte

These bus cycles, executed by bus master devices, transfer 16-bit words or 8-bit bytes to or from slave devices. The following bus signals are used in a data transfer operation:

Mnemonic	Description	Function
BDAL<17:0> [1]	18 Data/address lines	BDAL<17:0> [1] L are used for word and byte transfers. BDAL<17:16> [1] L are used for extended addressing, memory parity error, and memory parity error enable functions.
BSYNC [1]	Synchronize	Strobe signals
BDIN [1]	Data input strobe	
BDOUT [1]	Data output strobe	
BIRPLY [1]	Reply	
BWTR [1]	Write/byte control	Control signals
BBS [1]	Bank select 7	

Data transfer bus cycles can be reduced to three basic types: DAT, DATOB and DATOB. These transactions occur between the bus master and one slave device selected during the addressing portion to the bus cycle.

Bus Cycle Protocol

Before initiating a bus cycle, the previous bus transaction must have been completed (BSYNC [1] negated) and the device must become bus master. The bus cycle can be divided into two parts, an addressing portion and a data transfer portion. During the addressing portion, the bus master outputs the address for the desired slave device (memory or device register). The selected slave device responds by latching the address bits and holding this condition for the duration of the bus cycle (until BSYNC [1] becomes negated). During the data transfer portion, the actual data transfer occurs.

Device Addressing

The device addressing portion of a data transfer bus cycle comprises an address setup and deassert time and an address hold/deassert time. During the address setup and deassert time, the bus master does the following:

- Asserts $\overline{BDAL}<17:00>L$ with the desired slave device address bits
- Asserts $\overline{BBS7}L$ if a device in the I/O page is being addressed
- Asserts $\overline{BWTBT}L$ if the cycle is a DATQ(B) bus cycle
- Asserts $\overline{BSYNC}$ at least 150 ns after $\overline{BDAL}<17:00>L$, $\overline{BBS7}L$, and $\overline{BWTBT}L$ are valid.

During this time the address, $\overline{BDS7}L$ and $\overline{BWTBT}L$ signals are asserted at the slave bus receiver for at least 75 ns before $\overline{BSYNC}$ goes active. Devices in the I/O page ignore the five high-order address bits $\overline{BDAL}<17:13>L$ and instead decode $\overline{BBS7}$ along with the 13 low-order address bits. An active $\overline{BWTBT}L$ signal indicates that a DATQ(B) operation follows, while an inactive $\overline{BWTBT}L$ indicates a DATI or DATQ(B) operation.

The address hold/deassert time begins after $\overline{BSYNC}L$ is assertion. The master must hold the address at $\overline{BDAL}$ at least 100 ns after the assertion of $\overline{BSYNC}$.

The slave device uses the active $\overline{BSYNC}L$ bus receiver output to clock $\overline{BDAL}$ address bits, $\overline{BDS7}L$ and $\overline{BWTBT}L$ into its internal logic. $\overline{BWTBT}L$, $\overline{BBS7}L$, and $\overline{BDAL}<17:00>L$ will remain active for a minimum of 25 ns after the $\overline{BSYNC}L$ bus receiver goes active. $\overline{BSYNC}L$ remains active for the duration of the bus cycle.

Device selected logic must be reset at the end of the current bus cycle. The device should not wait until the next $\overline{BSYNC}L$ signal to reset the device selected logic.

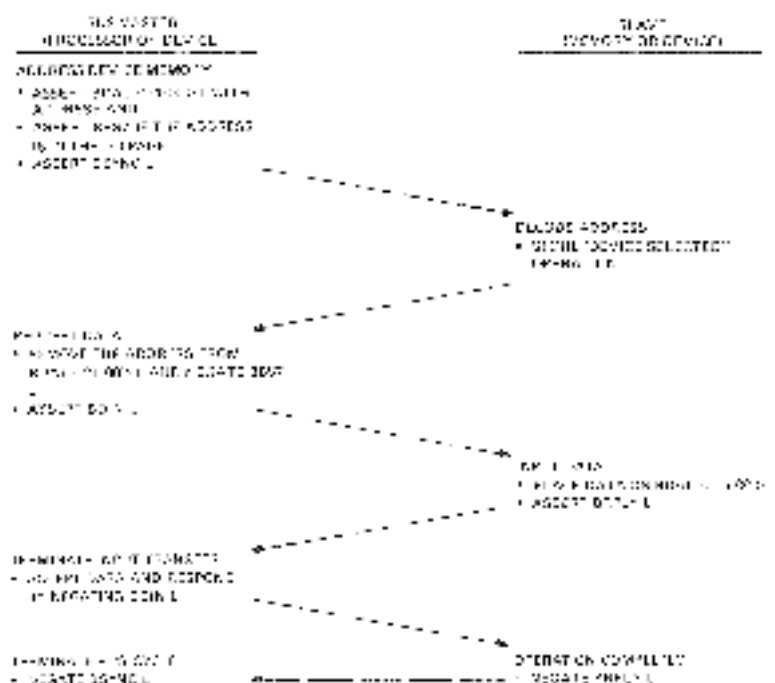
Memory and peripheral devices are addressed similarly, except for the way the slave device responds to $\overline{BBS7}$. Addressed peripheral devices must not decode address bits $\overline{BDAL}<17:13>L$. Addressed peripheral devices may respond to a bus cycle only when $\overline{BDS7}$ is asserted (low) during the addressing portion of the cycle. When asserted, $\overline{BDS7}L$ indicates that the device address resides in the I/O page (the upper 4K address space). Memory devices generally do not respond to addresses in the I/O page; however, some system applications may permit memory to reside in the I/O page for use as DMA buffers, read-only-memory bootstraps, or diagnostics, etc.

DATI

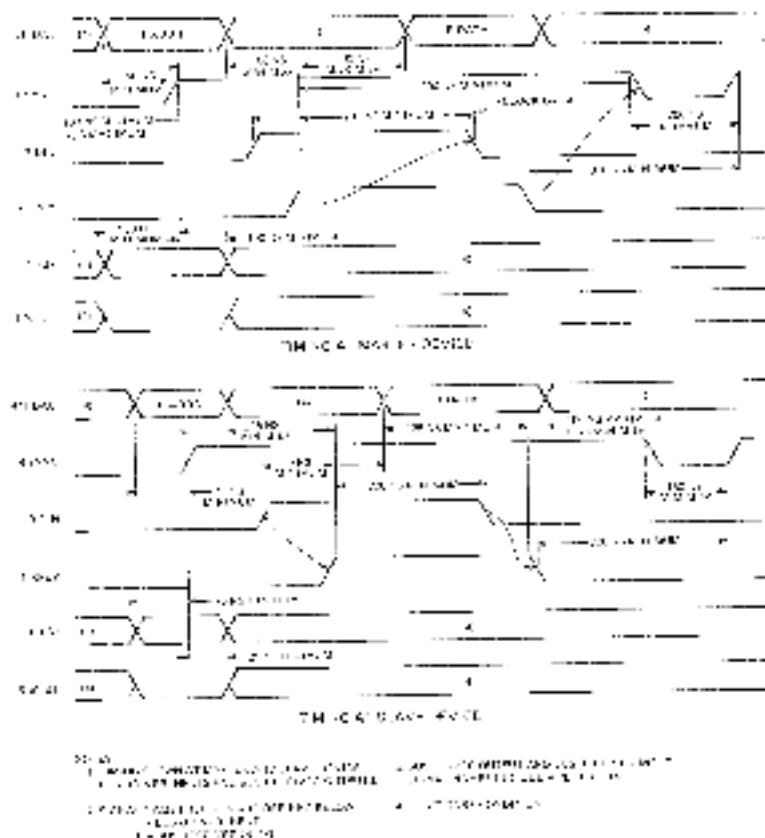
The DATI bus cycle is a read operation. During DATI, data is input to the bus master. Data consists of 16-bit word transfers over the bus. During the data transfer portion of the DATI bus cycle, the bus master asserts **BDIN L** 100 ns minimum, 8 ns maximum, after **DATAVNC L** is asserted. The slave device responds to **BDIN L** active in the following ways:

Asserts **BRPLY L** after receiving **BDIN L** and 125 ns (maximum) before **BDAL** bus driver data bits are valid.

Asserts **BDAL** 1700 ns L with the addressed data and error information.



DATI Bus Cycle



IAT1 Bus Cycle Timing

When the bus master receives **DRPLY L**, it does the following:

Waits at least 200 ns deassert time and then accepts input data at **BDAT<17:00>L** bus receiver. **RDAT<17:16>L** are used for transmitting parity errors to the master.

Negates **BDEN L** no less than 150 ns and no more than 2 microseconds after **DRPLY L** goes active.

the slave device responds to B[10:0] negation by negating BRPLY L, and removing read data from B[10:0] bus drivers. BRPLY L must be negated no more than 100 ns prior to removal of read data. The bus master responds to the negated BRPLY L by negating BSYNC L.

Conditions for the next BSYNC L assertion are as follows:

BSYNC L must remain negated for 200 ns (minimum)

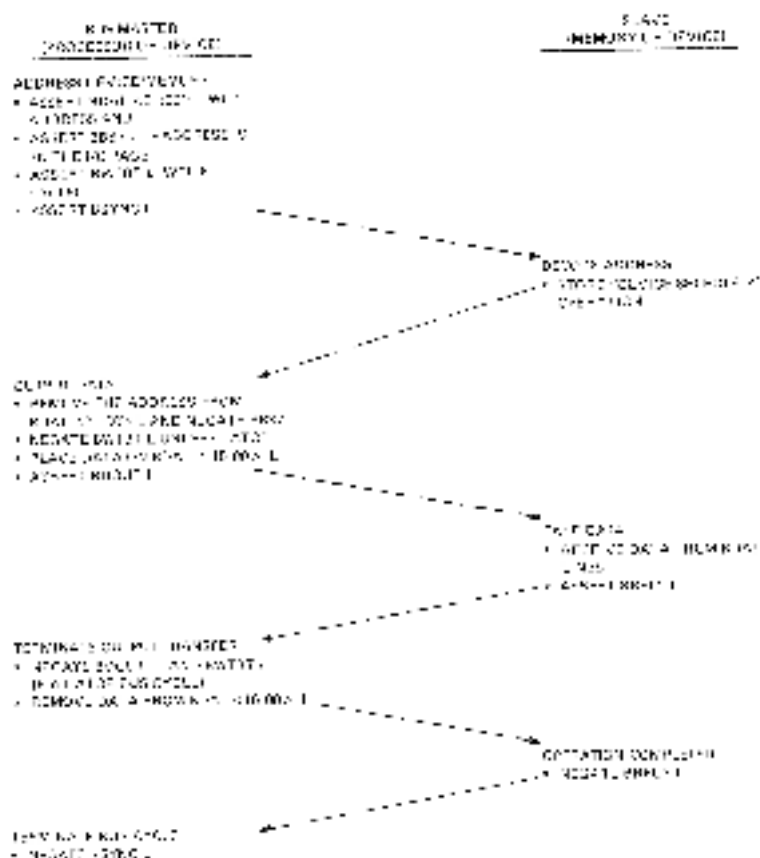
BSYNC L must not become asserted within 300 ns of previous BRPLY L negation.

NOTE

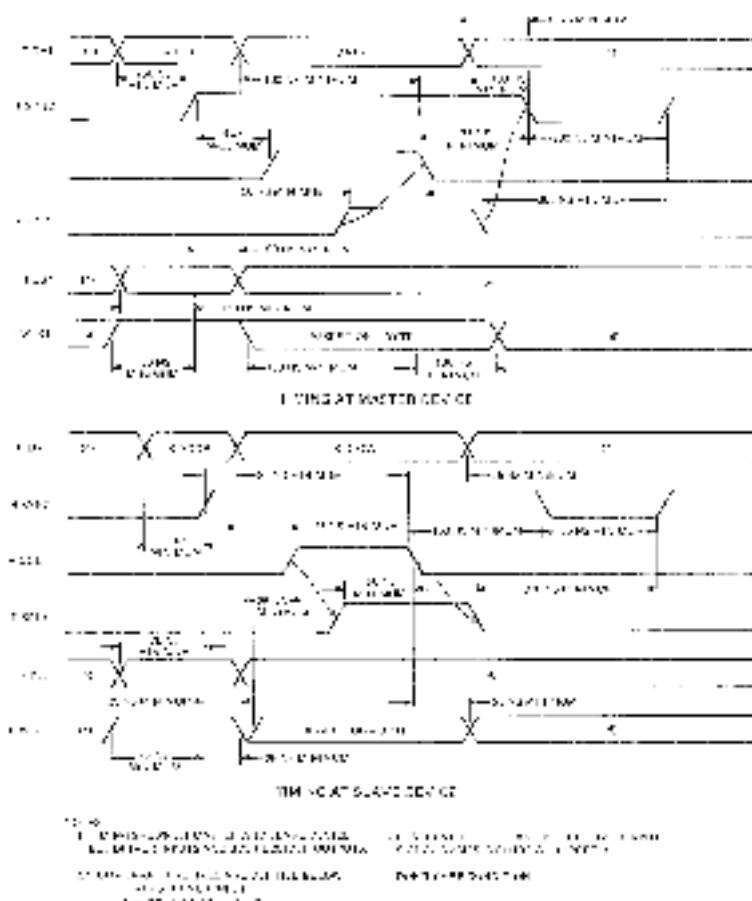
Continuous assertion of BSYNC L retains control of the bus by the bus master, and the previously addressed slave device remains selected. This is done for DATQ(B) bus cycles where DATQ or DATOR follows a DATI without BSYNC L negation and a second device addressing operation. Also, a slow slave device can hold off data transfers to itself by keeping BRPLY L asserted, which will cause the master to keep BSYNC L asserted. Exceeding 15 µsec hold time will cause loss of memory if bus refresh is being used.

DATOB

DATOB is a write operation. Data is transferred in 16-bit words (DATO) or 8-bit bytes (DATOB) from the bus master to the slave device. The data transfer output can occur after the addressing portion of a bus cycle when DWTBT = 1, had been asserted by the bus master, or immediately following an input transfer part of a DATOB bus cycle.



DATO or DATOB Bus Cycle



DAT0 or DAT0S Bus Cycle Timing

The data transfer portion of a DAT0R bus cycle comprises a data set-up and deslew time and a data hold and deslew time.

During the data set-up and deslew time, the bus master outputs the data on BDA[1:16]L at least 100 ns after BSYNCL is asserted. If it is a word transfer, the bus master negates BWTSTL at least 100 ns after BSYNCL assertion and BWTSTL remains negated for the length of the bus cycle. If the transfer is a byte transfer, BWTSTL remains asserted. 1:1 is the output of a DAT0S. BWTSL becomes asserted and lasts the duration of the bus cycle. During a byte transfer,

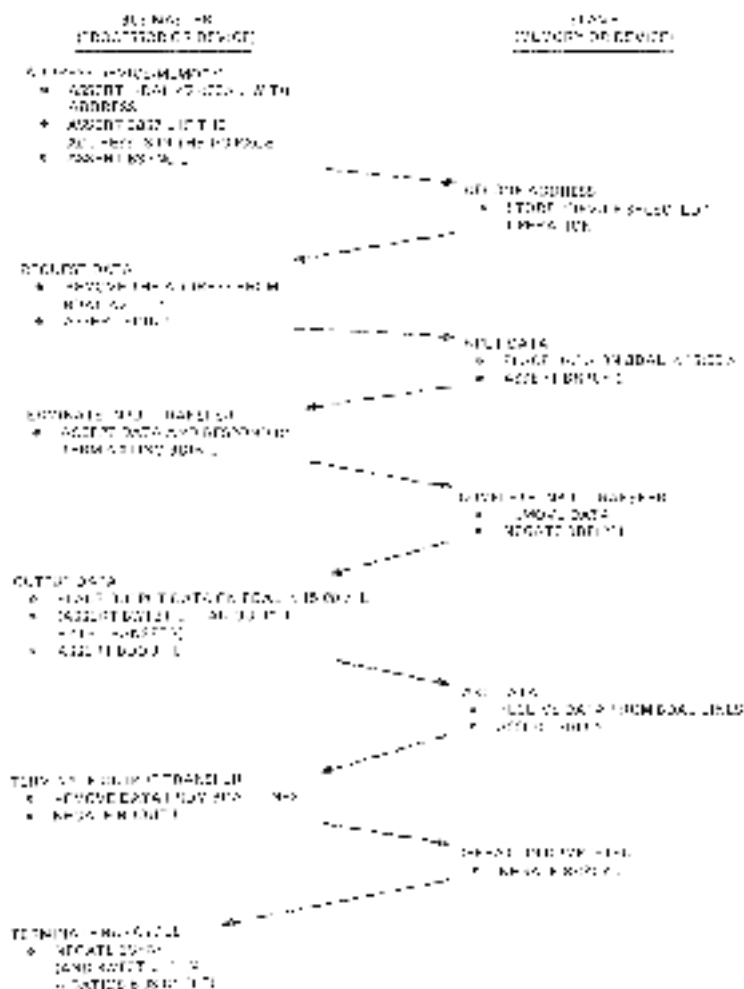
BDAL 00 L selects the high or low byte. This occurs while in the addressing portion of the cycle. If asserted, the high byte (BDAL<15:08> L) is selected; otherwise, the low byte (BDAL<07:00> L) is selected. An asserted BDAL 16 L at this time will force a parity error to be written into memory if the memory is a parity-type memory. BDAL 17 L is not used for write operations. The bus master asserts BDCOUT L between 100 ns and 0 ns after BDAL and BWDAT L bus drivers are stable. The slave device responds by asserting BRPLY L within 10 microseconds to avoid bus timeout. This completes the data setup and deassert time.

During the data hold and deassert time, the bus master receives BRPLY L and negates BDCOUT L. BDCOUT L must remain asserted for at least 150 ns from the receipt of BRPLY L before being negated by the bus master. BDAL<15:00> L bus drivers remain asserted for at least 100 ns after BDCOUT L negation. The bus master then registers RDAL inputs.

During this time, the slave device senses BDCOUT L negation. The data is accepted and the slave device negates BRPLY L. The bus master responds by negating BSYNC L; however, the processor will not negate BSYNC L for at least 175 ns after negating BDCOUT L. This completes the DATOD bus cycle. Before the next cycle BSYNC L must remain unasserted for at least 200 ns.

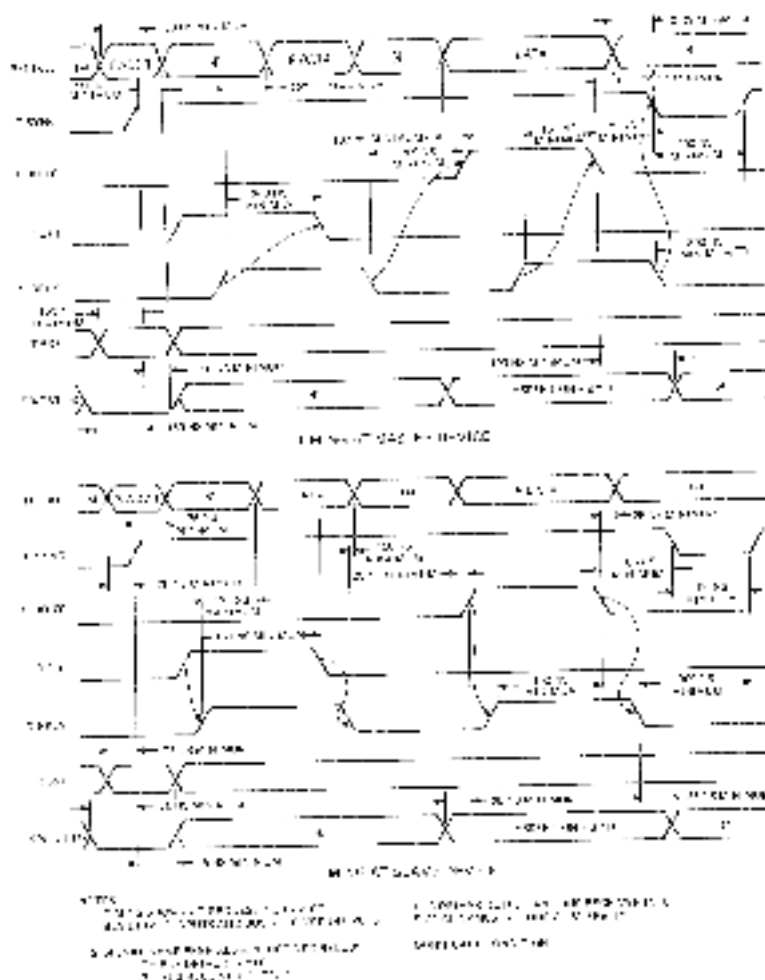
NATION

The protocol for a DAT00 bus cycle is identical to the addressing and data transfer portions of the DAT01 and DAT02 bus cycles. After addressing the device, a DAT01 cycle is performed as explained above; however, RSYNC L is not negated. RSYNC L remains active for an output word or byte transfer (DAT02). The bus master maintains at least 200 ns between RSPFL L negation during the DAT01 cycle and RDOUL L assertion. The cycle is terminated when the bus master negates RSYNC L, which is the same as described for DAT02.



DATID or DATIDB Bus Cycle

22



DAT10 or DAT10B Bus Cycle Timing

Parity Protocol

The KDP11-AA recognizes memory parity errors and traps to location 114h if one occurs. A parity error detection occurs during every DAT10 or DAT10B portion of a DAT10B cycle. The processor samples BDAL 16 L and BDAL 17 L after the 200 ns REPLY deassert time similar to BDAL 15.DX L. BDAL 16 L is interpreted as a parity error signal from memory and BDAL 17 L is interpreted as a parity error enable signal from an external parity controller module. BDAL 17 L is used by

software to enable parity detection which is done by addressing a parity status register on the LSI-11 bus. Parity status register hardware then asserts BDAL 17 L during the BDIN L portion of DATA cycles to inform the processor or bus master that detection is enabled. BDAL 16 L is used to indicate a parity error and is asserted by the selected memory at REPLY time. Upon system power-up, memory may contain random data and erroneous parity error signals may be used (BDAL 16 L asserted). Until known data is written into memory, software keeps BDAL 17 L negated, to avoid false traps. After known data and correct parity have been written into memory, software can enable parity detection in the parity status register. If both BDAL 16 L and BDAL 17 L are asserted at REPLY time, an abort and trap to location 1146 will occur. The assertion of BDAL 16 L during BDOUT L will cause memory to write wrong parity as a diagnostic tool for maintenance purposes.

Direct Memory Access

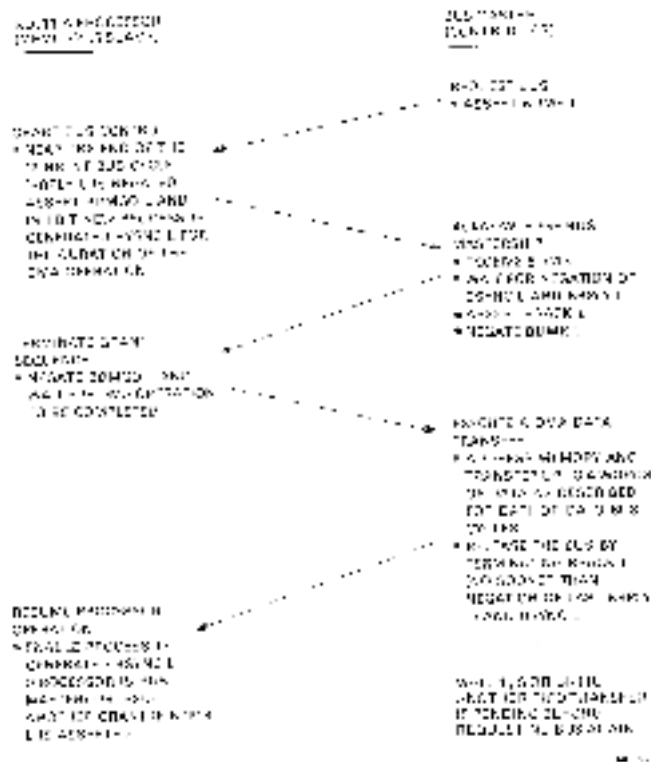
The direct memory access (DMA) capability allows direct data transfers between I/O devices and memory. This is useful when using mass storage devices (e.g., disks) that move large blocks of data to and from memory. A DMA device only needs to know the starting address in memory, the starting address in mass storage, the length of the transfer, and whether the operation is read or write. When this information is available, the DMA device can transfer data directly to (or from) memory. Since most DMA devices must perform data transfers in rapid succession or one data, DMA devices are provided the highest priority.

DMA is accomplished after the processor (formally the bus master) has passed bus mastership to the highest priority DMA device that is requesting the bus. The processor arbitrates all requests and grants the bus to the DMA device located electrically closest to the processor. A DMA device remains bus master indefinitely until it relinquishes its mastership. The following control signals are used during bus arbitration:

BDMCI L	DMA Grant Input
BDMCO L	DMA Grant Output
BDMR I	DMA Request Line
BSACK I	Bus Grant Acknowledge

DMA PROTOCOL

A DMA transaction can be divided into three phases: the bus mastership acquisition phase, the data transfer phase, and the bus mastership relinquish phase.



DMA Request/Grant Sequence

During the bus mastership acquisition phase, a DMA device requests the bus by asserting **BDMR L**. The processor arbitrates the request and initiates the transfer of bus mastership by asserting **BDMGO L**. The maximum time between **BDMR L** assertion and **BDMGO L** assertion is DMA latency. This time is processor-dependent. **BDMGO L**/**BDMGO H** is one signal that isaisy-chained through each module in the backplane. It is driven out of the processor on the **BDMGO L** pin, enters each module on the **BDMGI L** pin, and exits on the **BDMGO L** pin. Propagation delay from **BDMGI L** to **BDMGO L** must be less than 500 ns per LSI-11 bus slot. Since this delay directly affects system performance, it should be kept as short as possible. This signal passes through the modules in descending order of priority until it is stopped by the requesting device. The requesting device blocks the output of **BDMGO L** and asserts **BSACK L**. If **BRPLY L** and **BSYNC L** are negated. Propagation delay from **BDMGO L** to **BSACK L** must be less than 500 ns.

During the data transfer phase, the DMA device continues asserting **BSACK L**. The actual data transfer is performed as described in the sections on **DAT L**, **DAT H**, and **DAT O**.

NOTE

If multiple-unit transfers are performed during this phase, consideration must be given to the use of the bus for other system functions, such as memory refresh (if required).

The DMA device can assert **BSYNC L** for a data transfer no less than 250 ns after it receives **BDMGO L** and its **BSYNC L** and **BRPLY L** become negated.

During the bus mastership relinquish phase the DMA device relinquishes the bus by negating **BSACK L**. This occurs after completing (or aborting) the last data transfer cycle (**BRPLY L** negated). **BSACK L** may be negated no more than 300 ns before negating **BSYNC L**.

INTERRUPTS

The interrupt capability of the LSI-11 bus allows any I/O device to temporarily suspend (interrupt) current program execution and divert processor operation to service the requesting device. The processor inputs a vector from the device to start the service routine (handler). Like the device register address, hardware fixes the device vector or interrupts within a designated range (below location 001000). The vector is used as the first of a pair of contiguous addresses. The content of the first address is read by the processor and is the starting address of the interrupt handler. The content of the second address is a new processor status word (PS). The new PS can raise the interrupt priority level, thereby preventing lower level interrupts from breaking into the current interrupt service routine. Control is returned to the interrupt program when the interrupt handler is ended. The original (interrupted) program's address (PC) and its associated PS are stored on a stack. The original PC and PS are restored by a return from interrupt (RTI or RTU) instruction at the end of the handler. The use of the stack and the LSI-11 bus interrupt scheme can allow interrupts to occur within interrupts (nested interrupts), depending on the PS.

Interrupts can be caused by LSI-11 bus options. Interrupt operations can also originate from within the processor. These interrupts are called traps. Traps are caused by programming errors, hardware errors, special instructions, and maintenance features.

The LSI-11 bus signals that are used in interrupt transactions are as follows:

SIR04 L	Interrupt request priority level 4
SIR05 L	Interrupt request priority level 5
SIR06 L	Interrupt request priority level 6
SIR07 L	Interrupt request priority level 7
IRACK L	Interrupt acknowledge input
IRACK O	Interrupt acknowledge output
SDAL<15:00> L	Data/address lines
SDIN L	Data input strobe
SRFLV L	Ready

There are two classes of LSI-11 CPUs. One, the 11/23 CPU class, treats all interrupts as level 4. The other, the 11/29 CPU class, can distinguish between the four interrupt levels.

Device Priority

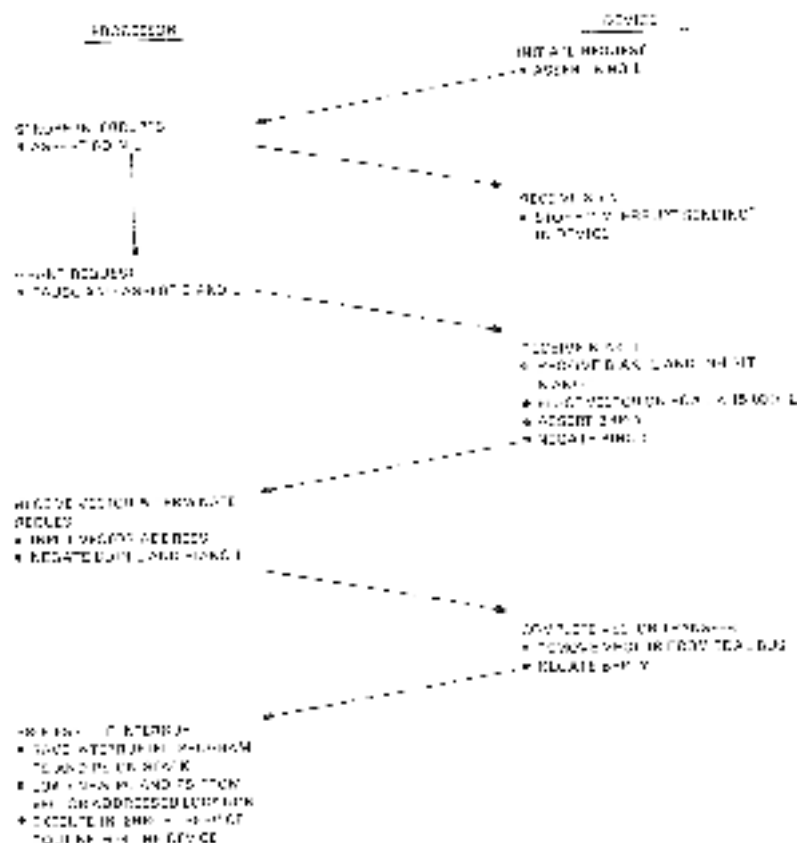
The LSI-11 bus supports the following two methods of device priority:

Distribution arbitration – Priority arbitration is implemented in logic on the interrupting device based on request priority information on the bus. When devices of equal priority level request an interrupt, priority is given to the device electrically closest to the processor.

Position-defined arbitration Priority is determined solely by electrical position on the bus. The closer a device is to the processor, the higher its priority is.

Interrupt Protocol

Interrupt protocol has three phases: interrupt request phase, interrupt acknowledge and priority arbitration phase, and interrupt vector transfer phase.



Interrupt Request/Acknowledge Sequence

The interrupt request phase begins when a device meets its specific conditions for interrupt requests. For example, the device is ready, done, or an error has occurred. The interrupt enable bit in a device status register must be set. The device then initiates the interrupt by asserting the interrupt request line(s). IRQ04 L is the lowest hardware priority level and is asserted for all interrupt requests for compatibility with previous LSI-11 processors. The event a device is configured at must also be asserted. A special case exists for level 7 devices which must also assert event 6. See item 2 of the arbitration discussion involving the 4-level scheme (below) for an explanation.

Interrupt Level	Lines Asserted by Device
4	IRQ04 L
5	IRQ04 L, IRQ05 L
6	IRQ04 L, IRQ06 L
7	IRQ04 L, IRQ06 L, IRQ07 L

The interrupt request line remains asserted until the request is acknowledged.

During the interrupt acknowledge and priority arbitration phase the processor will acknowledge interrupts under the following conditions:

On the 11/03 class processors, the PS bit 7 is cleared. On 11/23 class processors, the device interrupt priority is higher than the PS=07.05.

The processor has completed instruction execution and no additional bus cycles are pending.

The processor acknowledges the interrupt request by asserting BDIR L, and no less than 225 ns later asserting BIAK0 L. The device electrically closest to the processor receives the acknowledge on its BIAK0 L bus receiver.

At this point, the two types of arbitration must be discussed separately. If the device that receives the acknowledge uses the 4-level (distributed) interrupt scheme it reacts as described below:

1. If not requesting an interrupt, the device asserts BIAK0 L and the acknowledge propagates to the next device on the bus.
2. If the device is requesting an interrupt it must check to see that no higher level device is currently requesting an interrupt. This is done by monitoring higher level request lines. The table below lists the lines that need to be monitored by devices at each priority level.
3. In addition to asserting levels 4 and 7, level 7 devices must drive level 6. This is done to simplify the monitoring and arbitration by level 4 and 6 devices. If

this protocol, level 4 and 5 devices need not monitor level 7, since level 7 devices assert level 6. Level 4 and 5 devices will become aware of a level 7 request since they monitor the level 5 request.

Device Priority Level	Line(s) Monitored
4	BIACK ₀ , BIACK ₆
5	BIACK ₆
6	BIACK ₇
7	—

- If no higher level device is requesting an interrupt, the acknowledge is blocked by the device (BIACK₀ is not asserted). Arbitration logic within the device uses the leading edge of DDIN₀ L to clock a flip-flop that blocks BIACK₀ L. Arbitration is won and the interrupt vector transfer phase begins.
- If a higher level request (and is active), the device disqualifies itself and asserts BIACK₀ L to propagate the acknowledge to the next device along the bus.

Signal timing must be carefully considered when implementing 4-level interrupts. Refer to the previous figure for interrupt protocol timing.

If a single-level (position defining) device receives the acknowledge, it reacts as follows:

- If not requesting an interrupt, the device asserts BIACK₀ L and the acknowledge propagates to the next device on the bus.
- If the device was requesting an interrupt, the acknowledge is blocked using the leading edge of DDIN₀ L and arbitration is won. The interrupt vector transfer phase begins.

The interrupt vector transfer phase is enabled by DDIN₀ L and BIACK₀ L. The device responds by asserting BRPLY₀ L and its BDAL<15:00> L bus driver inputs with the vector address bits. The BDAL bus driver inputs must be stable no more than 125 ns after BRPLY₀ L is asserted. The processor then inputs the vector address and negates DDIN₀ L and BIACK₀ L. The device then negates BRPLY₀ L and no more than 100 ns later removes the vector address bits. The processor then enters the device's service routine.

NOTE

Propagation delay from BIACK₀ L to BIACK₆ L must be no greater than 500 ns per LSI-11 bus slot.

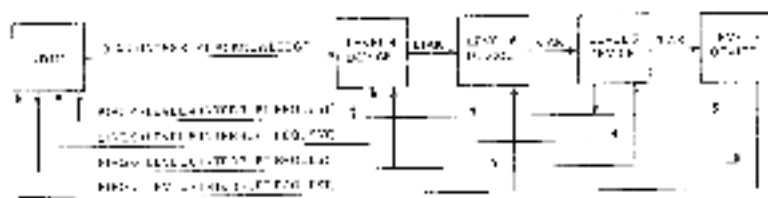
The device must assert BRPLY₀ L no more than 10 microseconds after BIACK₀ L is asserted at the input to the module. Since the magnitude of

both these times directly affects system performance, they should be kept as short as possible. Typical DIGITAL designs have less than 55 ns propagation delay from $\overline{\text{DMAK}}_L$ to $\overline{\text{DMAK}}_H$.

4-Level Interrupt Configurations (LSI-11/21)

Users who have high speed peripherals and desire better software performance can use the 4-level interrupt scheme. Both position-independent and position-dependent configurations can be used with the 4-level interrupt scheme.

The position-independent configuration is shown below. This allows peripheral devices that use the 4-level interrupt scheme to be placed in the backplane in any order. These devices must send out interrupt requests and monitor higher level request lines as described above. The level 4 request is always asserted by a requesting device regardless of priority, to allow compatibility if an LSI-11/2 or LSI-11 processor is in the same system. If two or more devices of equally high priority request an interrupt, the device physically closest to the processor will win arbitration.



Position-Independent Configuration (LSI-11/23)



Position-Dependent Configuration (LSI-11/23)

The position-dependent configuration is shown above. This configuration is simpler to implement. A constraint is that peripheral devices must be inserted with the highest priority device located closest to the processor and the remaining devices placed in the backplane in decreasing order of priority, with the lowest priority devices furthest from the processor. With this configuration, each device only has to assert its own level and level 4 (for compatibility with an LSI-11 or LSI-11/2). Monitoring higher level request lines is unnecessary. Arbitration is achieved through the physical positioning of each device on the bus. Devices which use the position-dependent scheme must be placed on the bus behind all position-independent devices and in order of decreasing priority.

CONTROL FUNCTIONS

The following J54-11 bus signals provide control functions.

REFR $\bar{L}$	Memory refresh
HALT $\bar{L}$	Processor halt
INIT $\bar{L}$	Initialize
POK $\bar{H}$	Power OK
GOODOK $\bar{H}$	DC power OK

Memory Refresh

If REFR $\bar{L}$ is asserted during the address portion of a bus data transfer cycle, it causes all dynamic MOS memories to be simultaneously addressed. The sequence of addresses required for refreshing the memory is determined by the specific requirements for each memory. The complete memory refresh cycle consists of a series of refresh bus transactions. A new address is used for each transaction. The effect of multiple data transfers by DMA devices must be carefully considered since they could delay memory refresh cycles.

Halt

Assertion of HALT $\bar{L}$ stops program execution and forces the processor unconditionally into console DDT mode.

Initialization

Devices along the bus are initialized when INIT $\bar{L}$ is asserted. The processor can assert INIT $\bar{L}$ as a result of executing a RESET instruction or as part of a power-up sequence. INIT $\bar{L}$ is asserted for approximately 10 μ s when RESET is executed.

Power Status

Power status protocol is controlled by two signals, POK $\bar{H}$ and GOODOK $\bar{H}$. These signals are driven by some external device (usually the power supply) and are defined as follows.

GOODOK $\bar{H}$

The assertion of this line indicates that dc power has been stable for at least 3 ms. The negation of this line indicates that only 5 μ s of dc power reserve remains. Once GOODOK $\bar{H}$ is negated it must remain in this state for at least 1 μ s before being asserted again. GOODOK $\bar{H}$ may be pulsed low for a minimum of 1 μ s to cause the CPU to restart.

POK $\bar{H}$

The assertion of this line indicates that there is at least an 8 ms reserve of dc power and that GOODOK $\bar{H}$ has been asserted for at least 30 ms. Once POK $\bar{H}$ has been asserted, it must remain asserted for at least 3 ms. The negation of this line indicates that power is fading and that only 4 ms of dc power reserve remains.

Power-Up/Down Protocol

Power-up protocol begins when the power supply applies power with BDCCK H negated. This forces the processor to assert BINIT L. When the dc voltages are stable, the power supply or other external device asserts BDCCK H. The power supply asserts EPDK H no less than 70 ms after BDCCK H is asserted. The processor then performs its power up sequence. Normal power must be maintained at least 3 ms before a power down sequence can begin.

A power-down sequence begins when the power supply negates DPDK H. The current bus master, if not the processor, should relinquish the bus as soon as possible (maximum 1 ms). When the current instruction is completed, the processor traps to a power-down routine. The processor traps to location J4a, which contains the PC that points to the power down routine. The end of the routine is terminated with a HALT instruction to avoid any possible memory corruption as the dc voltages decay. The power fail routine has 4 ms to execute and HALT from the time RPDK L is negated.

BUS ELECTRICAL CHARACTERISTICS

This section contains information about the electrical characteristics of the LSI-11 bus.

AC Load Definition

AC load is a unit of measure of capacitance between a signal line and ground, as specified below. A unit load is defined as 9.25 pF of capacitance.

DC Load Definition

DC load is a unit of measure of the dc current flowing in a signal line. A unit load is defined as 100 μ A flowing into a device when the signal line is in the high state.

120 Ohm LSI-11 Bus

The electrical conductors interconnecting the bus device slots are treated as transmission lines. A uniform transmission line, terminated in its characteristic impedance, will propagate an electrical signal without reflections. Insofar as bus drivers, receivers and wiring connected to the bus have finite resistance and nonzero reactance, the characteristic line impedance becomes nonuniform, and thus introduces distortions into pulses propagated along it. Passive components of the LSI-11 bus (such as wiring, cabling and etched signal conductors) are designed to have a nominal characteristic impedance of 120 ohms.

The maximum length of interconnecting cable, excluding wiring within the back plane, is limited to 4.68 m (15 ft).

Bus Drivers

Devices driving the 120 ohm LSI-11 bus must have open collector outputs and meet the following specifications:

AC Specifications

Output low voltage when sinking 70 mA of current: 0.7 V maximum

Output high leakage current when connected to 3.0 Vdc: 25 μ A (even if no power is applied to them, except for BDCOK II and BPOK II)

These conditions must be met at worst-case supply voltage, temperature, and input signal levels.

AC Specifications

Bus driver output pin capacitive load: Not to exceed 10 pF

Propagation delay: Not to exceed 35 ns

Slew (difference in propagation time between slowest and fastest gate): Not to exceed 25 ns

Rise/Fall Times: Transition time from 10 percent to 90 percent for positive transition, and from 90 percent to 10 percent for negative transition, must be no faster than 10 ns and no slower than 1 μ s.

Bus Receivers

Devices that receive signals from the 120 ohm LSI-11 bus must meet the following requirements.

DC Specifications

Input low voltage (maximum): 1.2 V

Input high voltage (minimum): 1.7 V

Maximum input current when connected to 3.2 Vdc: 80 μ A even if no power is applied to them.

These specifications must be met at worst-case supply voltage, temperature, and output signal conditions.

AC Specifications

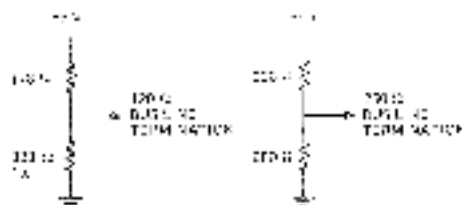
Bus receiver input pin capacitance load: Not to exceed 10 pF

Propagation delay: Not to exceed 35 ns

Slew (difference in propagation time between slowest and fastest gate): Not to exceed 25 ns

Bus Termination

The 120 ohm LSI-11 bus must be terminated at each end by an appropriate terminator. This is to be done as a voltage divider with its Thévenin equivalent equal to 120 ohms and 2.4 V nominal. This type of termination is provided by an REVM11-A refresh/byte terminator, or the RLM11-A4.



Bus Line Terminations

Each of the several LSI-11 bus lines (all signals whose nomenclature start with the letter D) must see an equivalent network with the following characteristics at each end of the bus:

- Input impedance (with respect to ground): $Z = 120 \pm 10\%$ ohms
- Open circuit voltage: 3.4 vdc $\pm 5\%$
- Capacitance (max): Not to exceed 20 pF

NOTE

The resistive termination may be provided by the combination of two modules (i.e., the processor module supplies 220 ohms to ground). Both of these two terminators must be physically resident within the same backplane.

Bus Interconnecting Wiring

This section contains the electrical characteristics of the bus transmission lines.

Backplane Wiring

The wiring that interconnects all device interface slots on the LSI-11 bus must meet the following specifications:

1. The conductors must be arranged such that each line exhibits a characteristic impedance of 120 ohms (measured with respect to the bus common return).
2. Crosstalk between any two lines must be no greater than 5 percent. Note that worst-case crosstalk is manifested by simultaneously driving all but one signal line and measuring the effect on the undriven line.
3. DC resistance of signal path, as measured between near-end terminator and far-end terminator module (including all intervening connectors, cables, backplane wiring, connector-module etc.) must not exceed 2 ohms.
4. DC resistance of common return path, as measured between near-end terminator and far-end terminator module (including all intervening connectors, cables, backplane wiring, connector-module etc., etc.) must not exceed an equivalent of 2 ohms per signal path. Thus, the composite signal return path dc resistance must not exceed 2 ohms divided by 40 bus lines, or 50 milliohms. Note that although this common return path is nominally at ground potential, the conductance must be part of the bus wiring; the specified low impedance return path must be provided by the bus wiring as distinguished from common system or power ground path.

Intra-Backplane Bus Wiring

This wiring method interconnects the bus connector slots within one contiguous backplane as part of the overall bus transmission line. Due to implementation constraints, the nominal characteristic impedance of 120 ohms may not be achievable. Distributed wiring capacitance in excess of the amount required to achieve the nominal 120 ohm impedance may not exceed 60 pF per signal line per backplane.

Power and Ground

Each bus interface slot has connector pins assigned for the following dc voltages.*

- +5 Vdc – Three pins (4.5 A maximum per bus device slot)
- +12 Vdc – Two pins (3.0 A maximum per bus device slot)
- Ground – Eight pins (shared by power return and signal return).

NOTE

Power is not used between backplanes on any interconnecting bus cables.

* The maximum allowable current per pin is 1.5 A. +5 Vdc must be regulated to $\pm 5\%$; maximum ripple: 100 mV p-p. +12 Vdc must be regulated to $\pm 3\%$; maximum ripple: 200 mV p-p.

SYSTEM CONFIGURATIONS

LSI-1 bus systems can be divided into two types:

Systems containing one backplane

Systems containing multiple backplanes

Before configuring any system, three characteristics for each module in the system must be known. These characteristics include

Power consumption: +5 Vdc and -12 Vdc current requirements

AC bus loading: the amount of capacitance a module presents to a bus signal line. AC loading is expressed in terms of ac loads where one ac load equals 5.05 pF of capacitance.

DC bus loading: the amount of dc leakage current a module presents to a bus signal when the line is high (driven). DC loading is expressed in terms of dc loads where one dc load equals 105 microamperes (nominal).

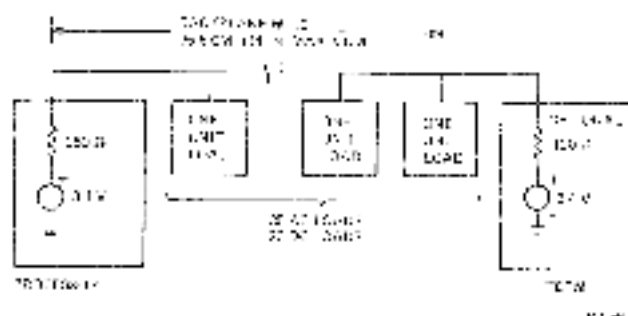
Power consumption, ac loading, and dc loading specifications for each module are included in the Microcomputer Handbook Series.

NOTE

The ac and dc loads and the power consumption of the processor module, terminator module, and backplane must be included in determining the total loading of a backplane.

Rules for Configuring Single Backplane Systems

1. The bus can accommodate modules that have up to a total of 20 ac loads (total) before an additional termination is required. The processor has on-board termination for one end of the bus. If more than 20 ac loads are included, the other end of the bus must be terminated with 120 ohms.
2. A single backplane, terminated bus can accommodate modules comprising up to a total of 55 ac loads.
3. The bus can accommodate modules up to a total of 20 dc loads.
4. The bus signal lines on the backplane can be up to 30.5 cm (14 in) long.



Single Backplane Configuration

Rules for Configuring Multiple Backplane Systems

1. Up to three backplanes may comprise the system. The signal lines on each backplane can be up to 25.4 cm (10 in) long.
2. Each backplane can accommodate modules that have up to a total of 20 pin loads. Unused pin loads from one backplane may not be added to another backplane. It is desirable to load backplanes equally, or with the highest pin loads in the first and second backplanes.
3. DC loading of all modules in all backplanes cannot exceed a total of 20 loads.
4. Both ends of the bus must be terminated with 120 ohms. This means that the first backplane must have an impedance of 120 ohms (obtained via the processor 220 ohm terminations and a separate 220 ohm terminator), and the last backplane must have a termination of 120 ohms.
5. The cables used to connect the backplanes should adhere to the following rules:
 - a. The cable(s) connecting the first two backplanes is 51 cm (2 ft) or greater in length.
 - b. The cable(s) connecting the second backplane to the third backplane is 22 cm (4 ft) longer or shorter than the cable(s) connecting the first and second backplanes.
 - c. The combined length of both cables cannot exceed 4.88 m (16 ft).
 - d. The cables used must have a characteristic impedance of 120 ohms.

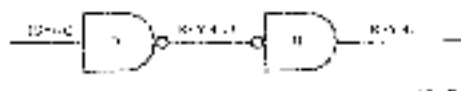
Power Supply Loading

Total power requirements for each backplane can be determined by obtaining the total power requirements for each module in the backplane. Obtain separate totals for +5 V and +12 V power. Power requirements for each module are specified in the Microcomputer Handbook Series.

When distributing power in multiple backplane systems, do not attempt to distribute power via the I S-B-T bus cables. Provide separate, appropriate power wiring from each power supply to each backplane. Each power supply should be capable of asserting BPOR-H and BDCOR-H signals according to bus protocol; this is required if automatic power fail/restart programs are implemented, or if specific peripherals require an orderly power-down halt sequence. The proper use of HPOR-H and HDOOR-H signals is strongly recommended.

NOTE

Timing diagrams reference signals at driver inputs (eg. TSYNC) and receiver outputs (eg. RSYNC). However, the accompanying text refers to the signals' names in their bus specific form (eg. BSYNC). The relationship between the three signal names are shown below. Most timing numbers indicated in the text are given with respect to the R and T versions of the signals shown in the timing diagrams; in all cases the timing diagrams are the overriding authority.



Signal Naming Conventions

APPENDIX D

FCC INFORMATION

GENERAL

To meet Federal Communications Commission (FCC) and Vordend Deutscher Elektroniktechnik (VDE) emission requirements, it is necessary to prevent excessive electromagnetic interference from escaping from a computer system's enclosure.

DIGITAL has designed the LSI-II cabinet kit system options to reduce interference by shielding cabinets and cables.

Grandfathered Items

Products produced before October 1, 1983 and which would normally fall into the FCC vertical category (commercial, industrial, and/or business use) were given "Grandfather Status", which means that they could continue to be built and labeled "untested" through September, 1983. Units built after September, 1983 must meet the applicable technical electromagnetic interference (EMI) limits of the FCC regulations, and must be labeled as such.

Date of Manufacture

The date of manufacture for FCC purposes, is the date on which a product completes its volume build, receives its identity and labels, and moves into the finished goods category.

It is not necessary that all products be fully configured as they would be shipped in order to comply with the date of manufacture (DOM) requirements.

For instance, if a PDP 11/23 processor could be inventoried as a basic machine, after October, 1983 additional communications options, memory and floating point processor (FPP) might be added.

Exempt

Exempt means that when a computing device is intended for several end-user applications, the device is exempt from part 15J testing/labeling/marketing rules. There are no exemptions from general prohibitions against interfering with licensed communications, both existing and proposed.

Mixed Systems

Individual products maintain their identity and FCC label status in a mixed system. FCC rules applying to each individual product will apply.

When DIGITAL sells a product or products which create a mixed system, either as a sale or field addition to another DIGITAL product, DIGITAL is responsible for the ability for each DIGITAL Class A or B product involved to continue to apply.

Interconnection of DIGITAL products with non-DIGITAL products is the responsibility of the purchaser of the products.

Specific FCC Related Labels

Class B Certified

These labels are for use on products marketed for use in the home or in residential areas.

Unlabeled

These labels are used on "Grandfather" units. The use of these labels ends 83 September 1983, which is when production of all "Grandfather" products must cease.

Class A Verified

These labels are used on products marketed for and use in industrial, commercial, and business applications.

Class B Verified

Can be used on the same types of products as above (Class A Verified), if the product passed the stricter test limits of Class B.

FCC Module List

The FCC does not require labeling of subassemblies, modules, cables, etc. They do require that manufacturers inform their customers of "the interference potential" of such products. The method used to determine this information at the point of sale is to separate the products by generating a list for those which have successfully been integrated into Class A or Class B products.