

P R E L I M I N A R Y

W4301 BOOTSTRAP TERMINATION
MAINTENANCE MANUAL

The information in this document is subject to change without notice and should not be construed as a commitment by Digital Equipment Corporation. Digital Equipment Corporation assumes no responsibility for any errors that may appear in this manual.

M93B1 MAINTENANCE MANUAL

CONTENTS

1.0	PREFACE
2.0	INTRODUCTION
2.1	General Description
2.2	Features
2.3	Physical Description
2.4	Electrical Specification
2.4.1	Power Consumption
2.4.2	Electrical Interfaces
2.4.3	External Electrical Interfaces
2.4.4	Electrical Prerequisites
2.4.5	Power and Ground Pinouts
2.4.6	Modified UNIBUS Pin Assignments
2.4.7	Timing
2.5	Operating Environmental Specifications
2.5.1	Temperature Range
2.5.2	Relative Humidity
3.0	HARDWARE DESCRIPTION
3.1	Introduction
3.1	Definition of Terms
3.3	Overview
3.4	Power Up Booting Logic
3.5	External Boot Circuit
3.6	Power Up Transfer Detection - Logic
3.7	Power Up Clear
3.8	Address Detection Logic
3.9	Address Offset Switch Bank
3.10	Rom Memory
3.11	M93B1 Terminator

Contents (Con't)

4.0	M9301 VARIATIONS
4.1	Overview
4.2	M9321=0
4.3	M9321=YA and M9301=YB
4.3.1	Physical Differences from M9321=0
4.3.2	Program Memory Maps
4.3.2.1	CPU Diagnostics
4.3.2.2	Register Display Routine
4.3.2.3	Memory Diagnostics
4.3.2.4	Bootstrap Programs
	RX11 Diskette
	Tall Cassette
	PC11 Paper Tape
	Disks
	Magnetape
	Console Emulator
4.3.2.5	Program Flows
	M9321 YA
	M9301 YB
4.3.3	Installation
4.3.3.1	Reboot Enable
4.3.3.2	Low Rom Enable
4.3.3.3	Boot Switch Selection
4.3.3.4	External Boot Switch
4.4	M9301=YC
4.4.1	Memory Map
4.4.2	General Description
4.4.3	Diagnostic test Descriptions
4.4.4	11/70 Bootstrap
4.4.5	Installation
4.4.6	Starting Procedure
4.4.7	Errors
5.0	EXTENDED ADDRESSING
5.1	Extended Addressing (Definition)
5.2	Definition of Virtual and Physical addresses
5.3	Address Mapping without Memory Management
5.4	Address Mapping with Memory Management
5.5	Creation of a Virtual address
5.6	Memory Management Registers
5.7	Address Assignments
6.0	M9301=YD
6.1	Purpose
6.2	Functionality
6.3	Using the M9301=YD
6.4	Program Listing
7.0	APPENDIX

1.3 PREFACE

This manual describes the M9321 Bootstrap/Terminator module and its various versions. Complete understanding of its contents requires that the user have a general knowledge of digital circuitry and a basic understanding of PDP-11 computers. The following related documents may be valuable as references.

PDP11 Peripherals Handbook
 PDP11 Processor Handbooks
 PDP-11/34, 11/39, USERS MANUAL

2.0 INTRODUCTION

2.1 General Description

The M9301 Bootstrap/Terminator is a double height extended module which plugs into a terminator slot on most PDP11 computers (see Installation Section 4). It contains a complete set of UNIBUS termination resistors along with 512 words of Read-Only memory which can be used for bootstrap programs. The module also provides circuitry for initiating bootstrap programs either on power up or from an external or logic level switch closure. See Figure 1 for photo of module.

2.2 Features

- Combines UNIBUS termination and bootstrap capability on one double height module.
- Can be used in all PDP11 machines which can handle an extended length module in the terminator slots.
- Bootstrap programs can be initiated by the following means:
 1. Direct program jumps to the memory space occupied by the bootstrap.
 2. Programmer console Load address and start sequence.
 3. Power restarts (See Section 3.3)
 4. External Boot switch closure
- Provides capability of enabling or disabling boots on power restarts.
- Provides 512 words of user memory space which can be programmed by the user or purchased with standard patterns provided by DEC. (See sections 3.12 and 4.2).

Module Photo

To Be Supplied

Figure 1

2.3 Physical Description

The M9381 is a double height extended (P 1/2 x 5 1/2 inches) FLIP-CHIP module which plugs into the A and B terminator slots on the APPI1 backplane. External connections are made via three FAST ON (TP1, TP2, and TP3) tabs provided at the handle end of the module.

2.4 Electrical Specification

2.4.1 Power Consumption

+5V DC ~ 2.2 Amperes typical

2.4.2 Electrical Interfaces

The UNIBUS interface is standardized using 8037 and 8680 receivers and 8881 drivers.

2.4.3 External Electrical Interfaces

The external interface consists of three FAST ON tabs (TP1, TP2 and TP3), each having the following loading and usage constraints.

- | | |
|-----|--|
| TP1 | Represents one standard TTL load with a 1K ohm pull-up. Input should be stable during a power up. Refer to Section 3.3 for TP1 usage. |
| TP2 | Represents two standard TTL loads with a 1K ohm pull-up resistor. Input signals should be limited to a 120ns minimum pulse width with all switch bounce noise restricted to a 5ms maximum duration. Note that triggering is initiated upon release of an input low (logic "0") pulse. On all power-ups, triggering is disabled until approximately 120ms after power returns (See Section 3.7) assuming that +5 VDC will be available from the power supply within 20ms. It is also important to realize that this input has no over voltage protection capability and adequate filtering must be provided when removing this input outside the standard DEC computer enclosure. Refer to Section 3.5 for TP2 usage. |
| TP3 | Should be used as a ground return for external switches attached to TP1 and TP2. Note that there is no protection for large voltage spikes on this input so proper filters should be externally installed to guarantee adequate isolation. |

2.4.4 Electrical Prerequisites

Refer to Section 4.2 for system constraints on specific version being used;

2.4.5 Power and Ground Pinouts

+5VDC:	pin AA2, BA2
GND:	PINS AC2, AT1, BC2, BT1

2.4.6 M9301 MODIFIED UNIQUE Pin Assignments

See TABLE 1.

2.4.7 Timing

Figure 2 shows important timing constraints for the M9301. Values shown are typical.

FIGURE 2
M9301 TIMING

2.5 Operating Environmental Specifications

2.5.1 Temperature Range 0 c to 70 c

2.5.2 Relative Humidity = 20% to 95%
(with out condensation)

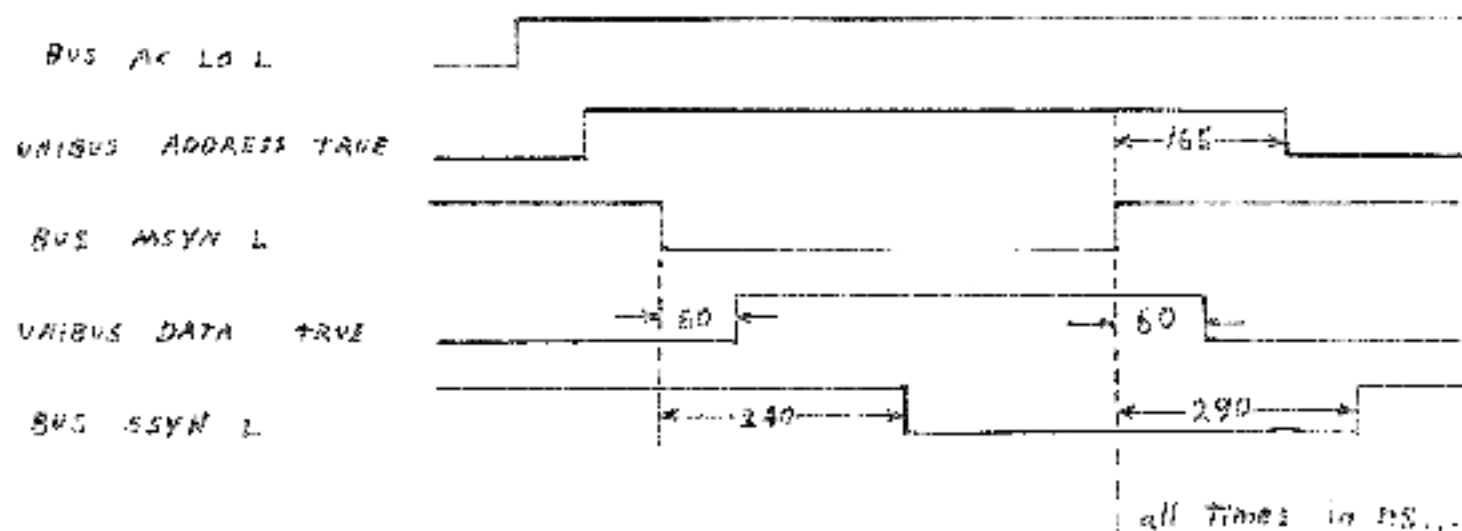


FIGURE 2
M9301 TIMING

TABLE 1

M9301 MODIFIED UNIBUS PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
AA1	BUS INIT L	BA1	SPARE
AP2	POWER (+5V)	BA2	POWER (+5V)
AB1	BUS INTR L	BP1	SPARE
AB2	TEST POINT	BB2	TEST POINT
AC1	BUS DC0 L	BC1	BUS BR 5L
AC2	GROUND	BC2	GROUND
AD1	BUS DC2 L	BD1	BAT-BACKUP +5V
AD2	BUS DC1 L	BD2	BR 4L
AE1	BUS DC4 L	BE1	INT. SSYN.
AE2	BUS DC3 L	BE2	PAR. DET.
AF1	BUS DC6 L	BF1	BUS ACLO L
AF2	BUS DC5 L	BF2	BUS DCLO L
AH1	BUS DC8 L	BM1	BUS A01 L
AH2	BUS DC7 L	BM2	BUS A00 L
AJ1	BUS D12 L	BJ1	BUS A03 L
AJ2	BUS DC9 L	BJ2	BUS A02 L
AK1	BUS D12 L	BK1	BUS A05 L
AK2	BUS D11 L	BK2	BUS A04 L
AL1	BUS D14 L	BL1	BUS A07 L
AL2	BUS D13 L	BL2	BUS A06 L
AM1	BUS PA L	BM1	BUS A09 L
AM2	BUS D15 L	BM2	BUS A08 L
AN1	P1	BN1	BUS A11 L
AN2	BUS PB L	BN2	BUS A12 L
AP1	PA	BP1	BUS A13 L
AP2	BUS BB8V L	BP2	BUS A12 L
AR1	BAT BACKUP +15V	BR1	BUS A15 L
AR2	BUS BACK L	BR2	BUS A14 L
AS1	BAT. BACKUP +15V	BS1	BUS A17 L
AS2	BUS NRR L	BS2	BUS A16 L
AT1	GROUND	BT1	GROUND
AT2	BUS GR 7L	BT2	BUS C1 L
AU1	+20V	BU1	BUS SSYN L
AU2	BUS GR 6L	BU2	BUS CO 1
AV1	+20V	BV1	BUS SSYN L
AV2	+20V	BV2	+5V

3.2 HARDWARE DESCRIPTION

3.1 Introduction

The following is a detailed circuit description of the M9321 Bootstrap/Terminals module. Various segments of this module will be analyzed separately for clarity. M9301 circuit schematics will be referenced throughout the description. (CS M9321-0-1).

3.2 Definition of Terms

3.2.1 Bootstrap Program

A bootstrap program is any program which loads another (usually larger) program into computer memory from a peripheral device.

3.2.2 Boot

Boot is a verb which means to initiate execution of a bootstrap program.

3.2.3 Bootstrap

Bootstrap and bootstrap program are used interchangeably.

3.3 Overview

Typically all PDP11 computers perform what is referred to as a power up sequence each time power is applied to their CPU module(s). This sequence is as follows:

3.3 Overview continued

+5VDC COMES TRUE

BUS DC LD L RELEASED
BY POWER SUPPLY

BUS AC LD L RELEASED
BY POWER SUPPLY

PROCESSOR ACCESSES MEMORY
LOCATION 24(8) FOR NEW PC

PROCESSOR ACCESSES MEMORY
LOCATION 26(8) FOR NEW PSW

PROCESSOR BEGINS RUNNING PROGRAM
AT NEW PC CONTENTS

WITH AN M9301 BOOTSTRAP/TERMINATOR IN THE PDP11 computer system, on power up the user can optionally (a switch on the M9301 can enable or disable this feature) force the processor to read its new PC from a ROM memory location (unibus location 773020(8)) and offset switch bank on the M9301. A new PSW will also be read from a location (UNIBUS Location 773026(8)) in the M9301 memory. This new PC and PSW will then direct the processor to a program (typically a bootstrap) in the M9301 ROM (UNIBUS memory locations 773000 thru 773776).

If booting on power up is disabled an external switch or logic level and be used to force the processor to execute a boot program. Programs in the M9301 can also be initiated by program jumps to their starting addresses or through the START switch feature of a programmer's switch console if one is available in the system.

3.4 Power Up Booting Logic

AC LD and DC LD

The status of every PDP11 power supply is described by the two UNIBUS control lines BUS AC LD L and BUS DC LD L. The condition of these two lines in relation to the +5 volt output of the power supply is defined by UNIBUS specifications as summarized in Figure 3.

Figure 3 Power fail Sequence

Power Up or Power Down

On the MP101, Power up sequences are detected by the circuitry shown in Figure 4. When +5 volts first becomes true, both BUS AC LO, and BUS DC LO are asserted low. Assuming the POWER UP REBOOT ENABLE switch (S1-2) is closed on, flip flop E24 will then be set. When BUS DC LO L goes high followed by BUS AC LO L, this flip-flop is then cleared generating a low-to-high transition on the output of E27 (pin 13). This transition triggers the one-shot E21 which asserts UNIBUS address lines BUS A29 L, BUS A10 L, and BUS A12 L thru BUS A17 L for 300 ns.

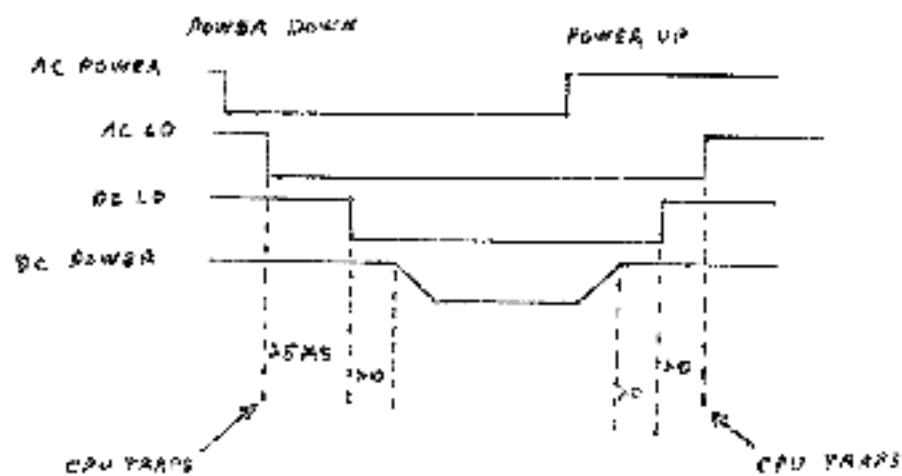


FIGURE 3 Power Fail Sequence

FIGURE 0
POWER UP BOOT LOGIC

Processor reads new program counter

During the 300 ms timeout of E21, the central processor will be performing its power up sequence. When the processor attempts to read a new program counter (PC) address from memory location 24(8), the address bits enabled by the one-shot are logically ORed to generate the address 773024(8). This location happens to be an address in the M9301 ROM space which contains the starting address of a specific (see Section 3.9) boot routine.

Processor reads new status word

Having obtained a new PC from location 773024(8), the processor then attempts to read a new Processor Status Word (PSW) from memory location 25(8). The address bits enabled by one-shot E21 are logically ORed to generate the address 773025(8) which is also in the M9301 ROM address space. Once this transfer is completed the removal of XSYN from the bus will generate a ADDR CLR L signal (See Section 3.8) which clears the one-shot (E21) timeout removing address bits BUS A09, BUS A10, and BUS A12 thru BUS A17. The 300 ms timeout length of E21 was chosen to guarantee enough time for all PDP11 processors to complete the two memory transfers described before releasing the address lines.

POWER UP REBOOT ENABLE

The POWER UP RESET ENABLE switch (S1-2) can be used to disable the logic shown in Figure 4. With this switch open, the clear input to the flip-flop 829 will always be low, preventing it from ever being set on power restarts. FAST ON tap TP1 is provided to allow switch S1-2 to be removed external to the module. Note that when an external switch is used, S1-2 must be left in the off position.

3.5 External Boot Circuit

The processor can be externally activated by grounding the FAST ON tap TP2 input, as shown in FIGURE 5. This low input sets flip-flop E13 which then generates a BUS AC LD L signal on the DATABUS. Upon seeing this

FIGURE 5
EXTERNAL BOOT CIRCUIT

DATABUS SIGNAL EVERY PDP-11 processor will begin a power down routine anticipating a real power failure. After completing this routine, the processor will then wait for the release of BUS AC LD L at which time it will perform a power up sequence through location 773224 and 773226.

When the EXTERNAL BOOT input is released, the one-shot E21 is triggered causing an 8 ms timeout, and the set input to flip-flop E13 removed. At the end of the one-shot timeout, flip-flop E13 is clocked low releasing the BUS AC LD L line and firing the 300 ms one-shot (E21) mentioned in Section 3.4. The processor then is forced to read its new PC and P&W from location 773224 and 773226 respectively as described in Section 3.4.

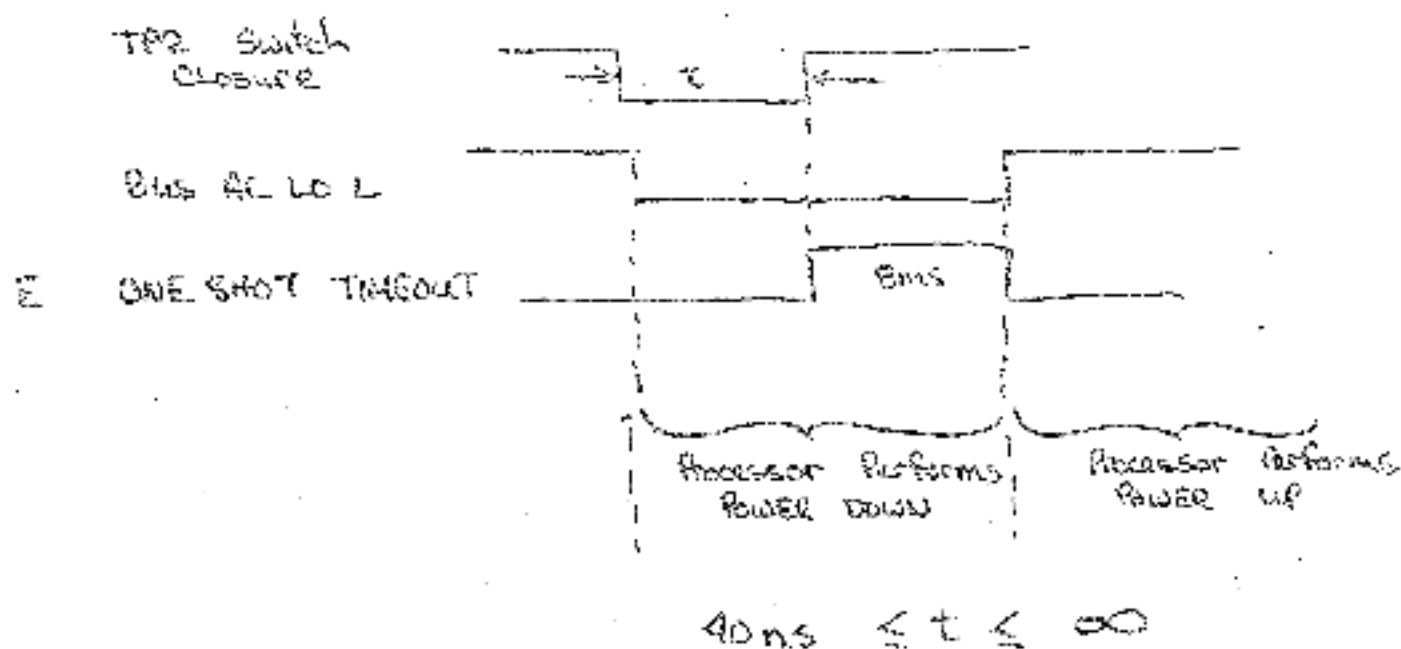


FIGURE 6
EXTERNAL BOOT TIMING

3.6 Power Up Transfer Detection Logic

FIGURE 7
TRANSFER DETECTION LOGIC

After BUS AC LO L and BUS BC LO L have performed their power up sequence as described in Section 3.4, the logic shown in Figure 7 counts the first two DATA transfers on the UNIBUS and generates a 75 ns pulse on the CLR ADDR L line. The two UNIBUS transfers performed will be to obtain a new PC and PSN as previously described. The CLR ADDR L pulse resulting will be used to clear the one shot E21 shown in Figure 4 releasing bus address line BUS A29, BUS A18, and BUS A12 thru BUS A17.

3.7 Power Up Clear

The circuit shown in Figure 8 is included on the M9301 to guarantee that specific storage elements on the module are cleared when power is first applied. The PWR CLR L signal will be held low for approximately 70 ns after the +5VDC has returned assuming the +5V supply has a rise time of less than 20ns. The exact period of time for holding PWR CLR L is a function of the rise time of the +5VDC power supply.

FIGURE 8
POWER UP CLEAR LOGIC

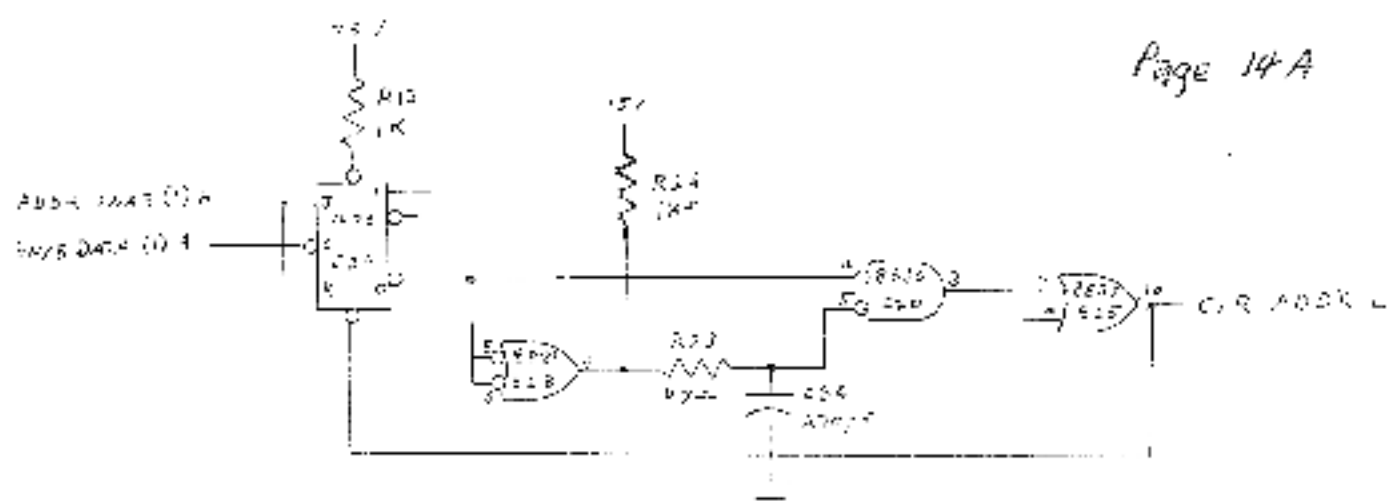


TABLE 5. DETECTION LOGIC

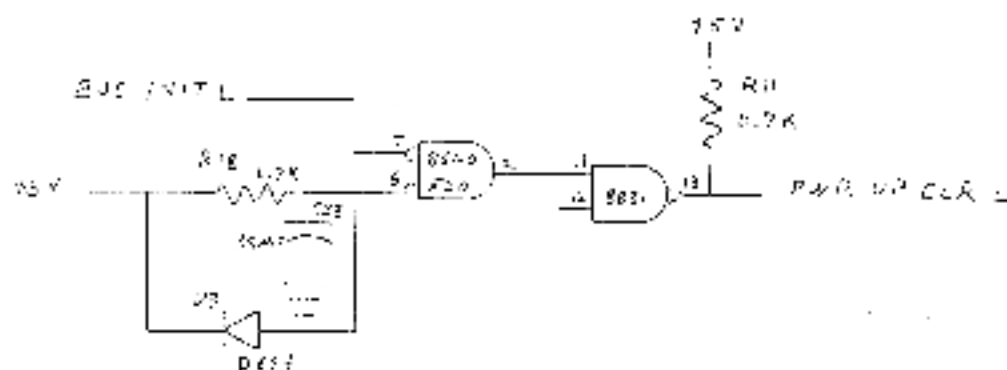


FIG. 8
Pattern of $CLPn2$ in G10

3.8 Address Detection Logic

H9321 Address Space

Figure 4 shows the complete UNIBUS address detection logic on the H9321. The purpose of this circuitry is to detect UNIBUS addresses within the address space of the H9301 $773270(8) \sim 773777(8)$ and $765220(8) \sim 765777(8)$, and recognize the specific addresses $773224(8)$ and $773226(8)$ for the power up circuit previously described in Sections 3.4, and 3.5.

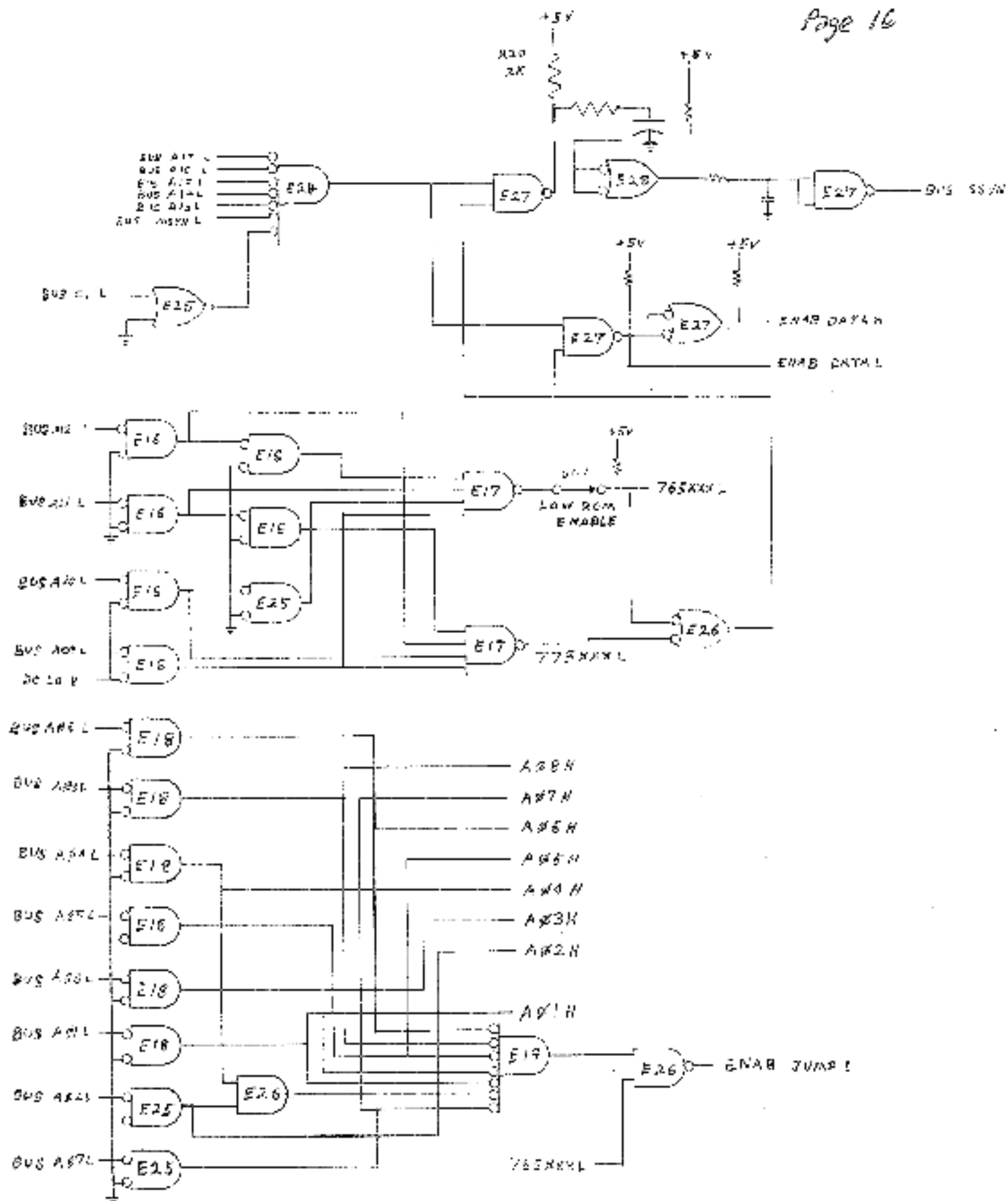


FIG. 9
ADDRESS DECODER LOGIC

M9301 Memory Access Constraints

The circuitry shown in Figure 9 determines when the M9301 ROM address space is being accessed. Upon receiving a recognized UNIBUS address, and BUS MSYN, the ROM data outputs are enabled onto the UNIBUS data lines (BUS D00 L + BUS D15 L) and BUS SSYN L is enabled 200 ns later. Conditions which must be met before enabling the ROM data and returning BUS SSYN are as follows:

1. Detection of the UNIBUS address 765XXX (dependent on position tns of L ROM ENABLE switch S1=1) or 773XX7 where XXX is redundant.
2. Transfer being performed is a DATA operation where BUS C1 L is not asserted.
3. A BUS MSYN L control signal has been obtained.

Low ROM Enable Switch

LOW ROM ENABLE switch (S1=1) shown in Figure 9 allows the user to disable the M9301 detection of UNIBUS addresses 765000 thru 765777. These addresses would normally represent the lower 256 words of the M9301 memory space. Disabling the detection of these addresses S1=1 is set to OFF position) becomes essential when that memory space is being used by other peripheral devices in the system. For M9301 modules containing standard DEC programs, users should note what program features will be eliminated by disabling M9301 address locations 765000 thru 765777.

ROM Address Generation

Logic shown in the lower half of Figure 9 performs two functions. First it receives the nine address inputs for the M9301 ROM memory (765XXX L and A01M thru A78M). Second it detects the UNIBUS address 773024 and generates the offset switch enable signal (See Section 3.9) EN48 JUMP L.

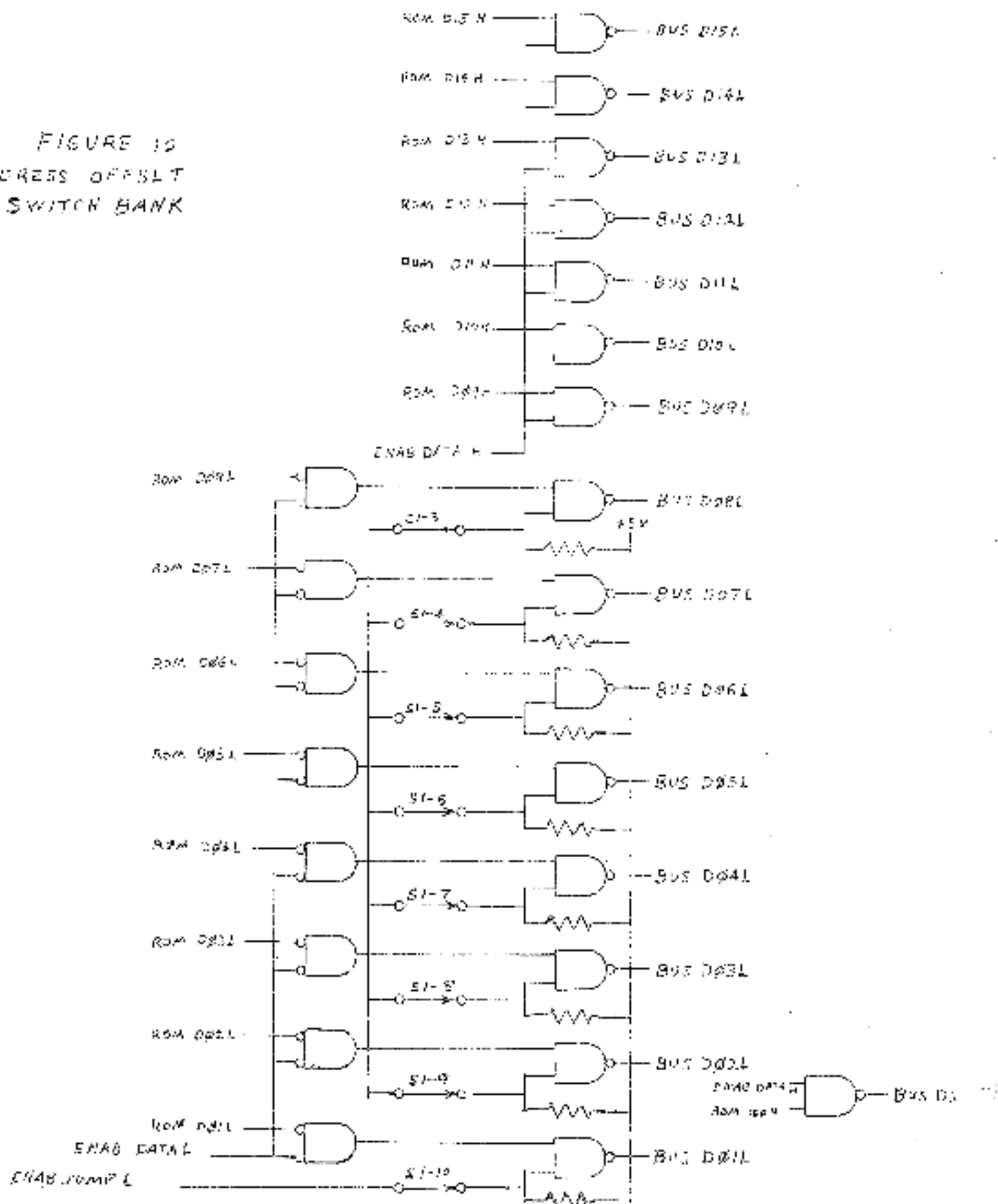
3.9 Address Offset Switch Bank

As previously mentioned in Section 3.4, on all boots, the M9301 processor obtains its new PC from location 773024(8) instead of location 24(8). When the M9301 address detection logic (Section 3.8) decodes the address 24(8), it enables (via EN48L JUMP L) the address offset switch bank (Figure 10) shown below. The contents of these switches, combined with the contents of the specified address in M9301 ROM memory, produce a new PC for the CPU. This new PC will point the processor to the starting address of a specific program (usually a bootstrap routine) in the M9301 memory. Several programs can be included in the M9301 memory with any one being user selectable through the address offset switch selection.

Example:

49301 ROM address 773024 contains ==	173003
Offset Switch Bank contains	254
	=====
New PC read by CPU	173254

FIGURE 12
ADDRESS OFFSET
SWITCH BANK



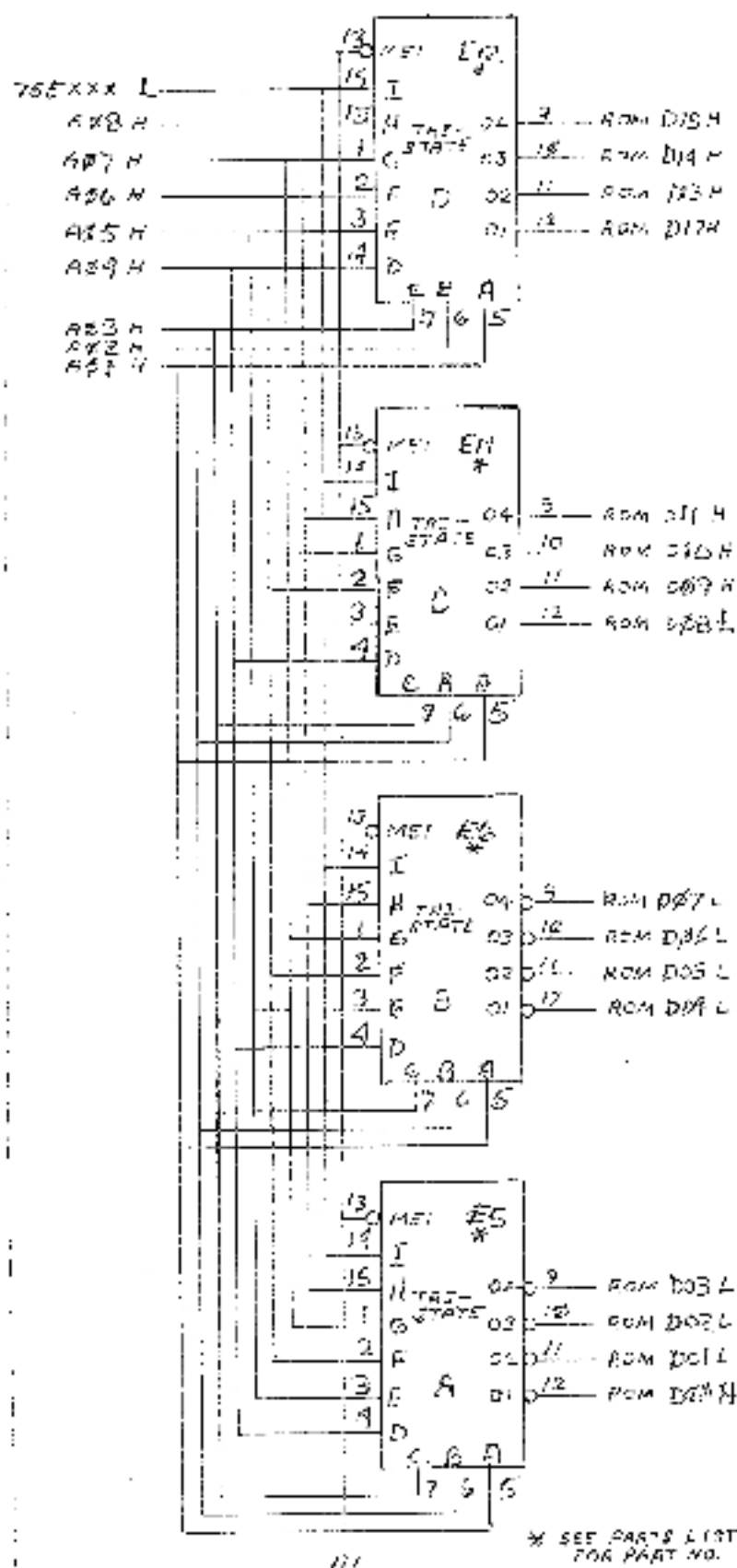
3.13 ROM Memory

The heart of the M9301 is the 512 word ROM (Read Only Memory) shown in Figure 11. It is composed of four 512 x 4 bit Tristate ROMS organized in a 512 x 16 bit configuration. All four units share the same address lines and produce 16-bit PDP-11 instructions for execution by the processor.

All four ROM outputs are always enabled, so any change in Address inputs will result in a change in the UNIBUS data lines when the ENAB DATA signals in Figure 9 are enabled. For further information on M9301 compatible ROMS, CONSULT THE ROM Specifications shown in the Appendix.

M9301 users that program their own PROMS should note the following programming constraints.

1. There is no address or data output translation required.
2. UNIBUS address locations 773200(8) thru 773776(8) are located in the lower 256 words of PROM word space and UNIBUS address locations 765000(8) thru 765776(8) are resident in the upper 256 words.
3. When coding PROM patterns data bits D01 thru D06 must always contain the inverse of the data required to compensate for the extra inversion logic available in the M9301 Offset Switch Circuitry.



3.11 M9301 TERMINATOR

The terminator section of the M9301 consists of four resistor pack circuits each containing the required pull-up and pull-down resistors for proper UNIBUS termination. Since PDP11/04 and PDP11/14 computers incorporate BUS GRANT pull-up resistors on the processor modules, space has been left on the M9301 for five jumpers (W1 thru W5) which allow the user to select whether to include BUS GRANT pull-up resistors. TABLE 2 indicates which versions of the M9301 have BUS GRANT jumpers installed.

Caution should be taken when inserting M9301 modules in various PDP11 (PDP11/05, 11/10, 11/35, 11/43) computers. If the processor in question does not have BUS GRANT pull-ups on the CPU, jumpers W1 through W5 on the M9301, should be inserted or the M9301 should be positioned at the end of the UNIBUS furthest from the CPU.

4.0 M9321 VARIATION

4.1 Overview

The M9321 Bootstrap/Terminator presently comes in five variations as described in the following sections. Table 2 summarizes the differences between each variation.

	M9301				
	-0	-YA	-YB	-YC	-YD
EXTERNAL BOOT SWITCH RESTART	*	YES	YES	NO	YES
POWER UP REBOOT ENABLE RESTART	*	YES	YES	NO	YES
PROGRAMMER'S CONSOLE STANDARD WITH COMPUTER	*	NO	NO	YES	YES
READ ONLY MEMORY (ROM)	NO	YES	YES	YES	YES
SOCKETS SUPPLIED FOR PROGRAMMABLE (ROM/PRGM)	YES	NO	NO	NO	NO
BUS GRANT PULL-UP TERMINATOR RESISTOR (W1 YHRU #5)	YES	NO	NO	YES	NO
SWITCH SELECTABLE BOOTING	*	YES	NO	YES	NO
STANDARD DEC BOOTSTRAPS AND MASSBUS DEVICE BOOTS	NO	NO	YES	NO	NO
STANDARD DEC BOOTSTRAPS	NO	YES	NO	NO	NO
FDP 11/70 USER PROGRAM	NO	NO	NO	YES	NO
DDCMP USER PROGRAM	NO	NO	NO	NO	YES

* INDICATES USER SELECTABLE

TABLE 2

M9301 VARIATION FEATURES

M9301 Variation Usage

General:

None of the following M9301 variations will function in a PDP11 system containing a UNIBUS repeater, unless the M9301 is inserted in a terminator position on the processor side of the repeater.

M9301 = 0 = Can be used in any PDP11 computer that accepts an extended length terminator. The user defines the bootstrap or program available in M9301 Rom space.

M9301 = YA = Used in most PDP11/34, and 34 OEM machines but is program compatible with all PDP11 machines that will accept an extended length terminator. Note however, that in other machines having CPUs which do not contain BUS GRANT pull up resistors, the M9301-YA must be placed at the end of the UNIBUS furthest from the CPU.

M9301 = YB = Same as the M9301-YA except it is intended for end user machines in the PDP11/34, and 34.

M9301 = YC = For use in only PDP11/74 machines.

M9301 = YD = Can be used in any PDP11 machine. Caution should be taken, however, when inserting the M9301 in some PDP11 computers. If the processor in question does not have BUS GRANT pull-up resistors on the CPU, jumpers J1 thru J5 on M9301 should be inserted or, the M9301 should be placed at the end of the UNIBUS furthest from the processor. (See Section 3.11).

4.2 M9301=0

The M9301=0 has been created as a universal bootstrap device which allows the user to program and install customized 512 x 4 bit ROMs. This module version comes with four 16-pin IC (integrated circuit) sockets in place of the Rom normally inserted on other module versions. For pinout and access time constraints on Roms used, consult the Rom Specification shown in the appendix. When configuring Rom bit patterns for the M9301=0, care should be taken to arrange them to meet the address and data output pinouts on the module. (See section 3.10)

4.3 M9301-YA and M9301-YB versions

Two versions of the M9301 have been created for use in the PDP 11/34, and 34, computers. One version, designated M9301-YA, is for OEM (original equipment manufacturer) use and the other designated M9301-YB is for end users. Both units contain basic CPU and memory ROMs and 80 diagnostics along with specific sets of bootstrap programs as shown in Table 3 and Table 4.

4.3.1 Physical Differences from the M9321=0

The only physical difference between the M9301=YA/M9301=YB modules and the M9301=0 previously described, is that specially programmed Tel State 512 x 4 bit ROMs are inserted in the four locations occupied by 16-pin DIP sockets on the M9301=0.

4.3.2 M9301=YA and M9321=YB Program Memory Map

Table 5 is a program memory map of the M9321=YB and M9301=YB modules and briefly lists the nature of each diagnostic test in the ROMs.

4.3.2.1 Basic CPU Diagnostics

TEST 1 = SINGLE OPERAND TEST

This test executes all single operand instructions using destination mode 3. The basic objective is to verify that all single operand instructions operate; it also provides a cursory check on the operation of each instruction, while ensuring that the CPU decodes each instruction in the correct manner.

TEST 1 brings the test destination register through its three possible states: zero, negative, and positive. Each instruction operates on the register contents in one of four ways:

1. Data will be changed via a direct operation, i.e., increment, clear, decrement, etc.
2. Data will be changed via an indirect operation, i.e., arithmetic shifts, add carry, and subtract carry.
3. Data will be unchanged, but operated upon, via a direct operation, i.e., clear a register already containing zeros.
4. Data will be unchanged via a non-modifying instruction (TEST).

Note that when operating upon data in an indirect manner, the data is modified by the state of the appropriate condition code. Arithmetic shifts will move the "C" bit into or out of the destination. This operation, when performed correctly, implies that the "C" bit was set correctly by the previous instruction. There are no checks on the data integrity prior to the end of the test. However, a check is made on and the result of the data manipulation. A correct result implies that all instructions manipulated (or, did not manipulate) the data in the correct way. If the data is incorrect, the program will hang in a program loop until the machine is halted.

TEST 2 = DOUBLE OPERAND, ALL SOURCE MODES,

DESTINATION MODE 0

This test verifies all double operand general and logical instructions--each in one of the seven modes (excludes mode 01). Thus, two operations are checked the correct decoding of each double operand instruction, and the correct operation of each addressing mode for the source operand.

Each instruction on the test must operate correctly in order for the next instruction to operate. This interdependence is carried through to the last instruction (bit test) where, only through the correct execution of all previous instructions is a data field examined for a specific bit configuration. Thus, each instruction prior to the last serves to set up the pointer to the test data.

Two checks on instruction operation are made in TEST 2. One check, a branch on condition, is made following the compare instruction, while the second is made as the last instruction in the test sequence.

Since the GROUND GU test resides in a ROM memory, all data manipulation (modification) must be performed in destination mode 0 (register contains data). The data and addressing constants used by TEST 2, are contained within the ROM.

It is important to note that two different types of operations must execute correctly in order for this test to operate:

1. Those instructions that participate in computing the final address of the data mask for the final bit test instruction.
2. Those instructions that manipulate the test data within the register to generate the expected bit pattern.

Detection of an error within this test results in a program loop.

TEST 3 - JUMP TEST MODES 1, 2, AND 3

The purpose of this test is to ensure correct operation of the Jump instruction. This test is constructed such that only a Jump to the expected instruction will provide the correct pointer for the next instruction.

There are two possible failure modes that can occur in this test:

1. The jump addressing circuitry will malfunction causing a transfer of execution to an incorrect instruction sequence or non-existent memory.
2. The jump addressing circuitry will malfunction in such a way as to cause the CPU to loop.

The latter case is a logical error indicator. The former, however, may manifest itself as an alternate test error. For example, if the jump causes control to be given to other routines within the #4301, the inter-dependent instruction sequences would probably cause a

failures to eventually occur. In any case, the failing of the Jump instruction will eventually cause an out of sequence or "illogical event" to occur. This in itself is a meaningful indicator of a malfunctioning CPU.

This test contains a JUMP, MODE 2. This instruction is not compatible across the PDP-11 line. However, it will operate on any PDP-11, within this test, due to the unique programming of the instruction within TEST 3. Before illustrating the operation, it is important to understand the difference of the JUMP MODE 2 between machines.

On the PDP-11/20, 11/05, and 11/12 processor, for the Jump Mode 2 (JMP (R)+1) the register (R) is incremented by 2 prior to execution of the Jump. On the PDP-11/40 and 11/35, (R) is used as the Jump address and incremented by 2 after execution of the Jump.

In order to avoid this incompatibility, the Jump (R)+1 is programmed with (R) pointing back on the Jump itself. On 11/20, 11/05, and 11/12 processors, execution of the instruction would cause (R) to be incremented to point to the following instruction, effectively continuing a normal execution sequence.

On the PDP-11/40 and 11/35 processors, the use of the initial value of (R) will cause the Jump to "loop" back on itself. However, correct operation of the auto-increment will move (R) to point to the next instruction following the initial Jump. The Jump will then be executed again. However, the destination address will be the next instruction in sequence.

TEST 4 - SINGLE OPERAND, NON-MODIFYING, BYTE TEST

This test focuses on then one unique single operand instruction, the TST. TST is a special case in the CPU execution flow since it is a non-modifying operation. TEST 4 also tests the byte operation of this instruction. The TSTB instruction will be executed in Mode 1 (register deferred) and Mode 2 (register deferred, auto increment).

The TSTB is programmed to operate on data which has a negative value most significant byte and a zero (not negative) least significant byte.

In order for this test to operate properly, the TSTB on the LSB must, first, be able to access the even addressed LSB, then set the proper condition codes. The TSTB is then re-executed with the auto-increment facility. After the auto-increment, the addressing register should be pointing to the MSB of the test data. Another TSTB is executed on what should be the MSB. The "N" bit of the condition codes should be set by this operation.

Correct execution of the last TSTB implies that the auto-increment recognized that a byte operation was requested, thereby only incrementing the address in the register by one, rather than two. If the correct condition code was not set by the associated TSTB instruction, the program will loop.

TEST 5 - DOUBLE-OPERAND, NON-MODIFYING TEST

These are two non-modifying double-operand instructions - the compare (CMP) and bit test (BIT). These two instructions operate on test data in source modes 1 and 4, and destination modes 2 and 4.

The BIT and CMP instructions will operate on data consisting of all ones (1777777). Two separate fields of ones are used in order to utilize the compare instructions, and to provide a field large enough to handle the autoincrementing of the addressing register. Since the compare instruction is executed on two fields containing the same data, the expected result is a true "Z" bit, indicating equality.

The BIT instruction will use a mask argument of all ones against another field of all ones. The expected result is a non-zero condition (Z).

Test failures will result in a one instruction loop.

4.3.2.3 Register Display Routine - The register display routine prints out the actual contents of the CPU registers R0, R4, R5 and old PC on the console terminal. This sequence will be followed by a prompt character (\$) on the next line.

Example of a typical printout.

	XXXXXX	XXXXXX	XXXXXX	XXXXXX
\$				
Prompt	R0	R4	R5	Old PC Program Counter
Character			(Stack Pointer)	

1. Where X signifies an octal number (X=7).
2. Whenever there is a power up routine or the BOOT SWITCH is released on PDP11/34 and PDP11/34 machines, the PC at this time will be stored in R5. The contents of R5 are then printed as the OLD PC shown in the example.

The prompting character string indicates that diagnostics have been run and the processor is operating.

4.3.2.3 Memory Modifying CPU Diagnostics

TEST 6 - DOUBLE OPERAND, MODIFYING, BYTE TEST

The objective of this test is to verify that the double-operand, modifying instructions will operate in the byte mode. TEST 6 contains three subtests:

1. Test source mode 2, destination mode 1, odd and even bytes.
2. Test source mode 3, destination mode 2.

3. Test source code 0, destination mode 3, even byte.

The move byte (MOV8), bit clear byte (BIC8), and bit set byte (BIS8) are used within TEST 6 to verify the operation of the modifying double-operand functions.

Since modifying instructions are under test, memory must be used as a destination for the test data. TEST 6 uses location 500(8) as a destination address. Later, in TEST 7 and the Memory Test, location 500 is used as the first available storage for the stack.

Note that, since TEST 6 is a byte test, location 500(8) implies that both 500(8) and 501 are used for the bytes test (even and odd, respectively). Thus, in the word of data at 500 add and even bytes are caused to be all zeroes and all ones throughout the test. Each byte is modified independently of the other.

TEST 7 - JSR TEST

The JSR is the first test in the 60-40 60 sequence that utilizes the stack. The Jump Subroutine command (JSR) is executed in codes 1 and 6. After the JSR is executed, the subroutine which was given control, will examine the stack to ensure that the correct data was placed in the correct stack location (500(8)). The routine will also ensure that the line back register points to the correct address. Any errors detected in this test will result in a halt.

TEST 8 - MEMORY TEST

Although this test is intended to test both core and MOS memories, the data patterns used are designed to exhibit the most taxing operation for MOS. Before the details of the test are described, it would be appropriate to discuss the assumptions placed upon the failure modes of the MOS technology.

This test is intended to check for two types of problems that may arise in the memory.

1. Solid Element or Sense Amp failures.
2. Addressing Malfunctions external to the chip.

The simplest failure to detect is a solid read or write problem. If a cell fails to hold the appropriate data, it is expected that the Memory Test will easily detect this problem. In addition, the program attempts to saturate a chip in such a way as to cause marginal sense amp operation to manifest itself as a loss or pickup of unexpected data. The 64 x 1 cells used in the memory consists of a 64 x 64 matrix of MOS storage elements. Each 64 bit section is tied to a common sense amplifier. The objective of the program is to saturate the section with, at first all zeroes and one "1" bit. This "1" bit is then floated through the chip. At the end, the data is complemented, and the test repeated.

For external addressing failures, it is assumed that if two or more

locations are selected at the same time, and a write occurs, it is likely that both locations will assume the correct state. Thus, prior to writing any test data, the background data is checked to ensure that there was no crosstalk between any two locations. All failures will result in a program halt as do failures in tests 6 and 7. After the halt, it is expected that the operator will depress the BDC switch causing RD (Expected Data), RU (Received Data), SP (failing Address), and PC (PC indicating memory failure) to be displayed.

NOTE

If the expected and received data are the same, it is highly probable that an intermittent failure has been detected (i.e., timing or margin problem). The reason the expected and received data can be identical is that the test program re-reads the failing address after the initial noncompare is detected. Thus, a failure at CPU speed is detected, and indicated by the reading of the failing address on a single reference (not at speed) operation.

4.3.2.4 Bootstrap Programs Supported by the M9301-YA and M9301-YB - Peripheral devices whose bootstraps are supported by the M9301-YA and M9301-YB are listed in TABLE 3 and TABLE 4. Each of these bootstraps is compatible with standard DEC boots and operates as follows.

4.3.2.4.1 RX11 DISKETTE - Loads the first 64 words (226 bytes) of data from track one, sector one into memory location 2 -177 beginning at location 0. Once loaded the contents of location 0 is checked. If it contains 242, operation is transferred to the routine beginning in location 0. If location 0 does not contain 242, the boot is restarted. Restarts will occur 2000 times before the machine is halted automatically.

4.3.2.4.2 T111 CASSETTE - This bootstrap is identical to that of the RX11 except that data is loaded from the cassette beginning at the second block.

4.3.2.4.3 PC11 PAPER TAPE READER - Loads an Absolute Loader formatted tape into the upper memory locations XXX746 to XXX777 (XXX is dependent on memory size). Once loading is completed, the boot transfers operation to a routine beginning at location XXX752. In systems containing an M9321-YA which is set up not to run diagnostics

TEST 1 thru TEST 5, XXX will become 017 not the lower part of memory;

4.3.2.4.4 = DISKS (excluding RX11) = Load 1220 words (2000 bytes) of data from the disk into memory locations 0-1776.

4.3.2.4.5 MAGTAPE = TX11 = Loads second record (1020 bytes maximum size) from the magtape into memory location 0-777. T2015 = Load second record (2020 bytes maximum size) from magtape into memory locations 0-1777.

4.3.2.4.6 CONSOLE EMULATOR = When this routine is used in conjunction with the user's terminal, functions quite similar to those found on the programmer's console of traditional PDP11 family computers are generated, as shown in the summary below. The description of the operation that follows assumes that the user's K9301 module is configured to enter the console emulator routine (CIP switch settings for emulator are shown in TABLE(3) on PCXER 1.0 or whenever the BDDT switch is depressed.

A SUMMARY OF THE CONSOLE EMULATOR FUNCTIONS

LOAD =	This function loads the address to be manipulated into the system
EXAMINE =	Allows the operator to examine the contents of the address that was loaded and or deposited.
DEPOSIT =	Allows the operator to write into the address that was loaded and/or examined
START =	Initializes the system and starts execution of the program at the address loaded
BDDT =	Allows the booting of a specified device by typing in a two character code and unit number.

Console Emulator Operation

The console emulator allows the user to perform load, examine, deposit, start, and boot operations by typing in appropriate code on the keyboard. The combination of the console emulator routine and the keyboard will be referred to as "The Console Emulator".

Discussion of the Simplified Operator's Flow Chart

Introduction

The simplified operator's flow chart of the console emulator routine (which will be referred to as the Operator's Flow Chart) is presented at this point in the text, to give the reader a unified picture of the console emulator routine.

Detailed discussions of each aspect of the chart are presented in Sections in the following paragraphs.

Symbols

Rectangle

Rectangles indicate automatic operations which are performed by the machine. There is only one entrance and one exit on a rectangle.

Diamond

A diamond indicates an automatic operation which can take either of two paths depending on how the question stated within the diamond is answered.

Circle

A circle indicates operator action, and the moving of a switch or the typing of keys.

0000-9222/87/0001-0000\$7.50/0



CR

CR is the symbol for the carriage return key.

Using the Console Emulator

After The S =

Once the system has been powered up or booted, and R0, R4, SP, PC and A have been printed, the console emulator routine can be used.

Keyboard Input Symbols

The discussion of keyboard input format uses the following symbols:

Space Bar : (SB)

Carriage Return Key : (CR)

Any Number 0 - 7

(Octal Number)key : (X)

Keyboard Input Format: Load = Examine deposit start. All character keys shown in the following discussion represent themselves with the exception of those in parenthesis.

FUNCTION	KEYBOARD STROKES
Load Address	L (SB) (X) (X) (X) (X) (X) (X) (CR)
Examine	E (SB)
Deposit	D (SB) (X) (X) (X) (X) (X) (X) (CR)
Start	S (CR)

Order of Significance of Input Keys

The first character that is typed will be the most significant character. Conversely, the last character that is typed is the least significant character.

Leading Zeros

When an address or data word contains leading zeros, these zeros can be omitted when loading the address or depositing the data.

Example Using the Load, Examine, Deposit, and Start Functions

Assume that a user wishes to:

1. Turn on power
2. Load address 700
3. Examine location 700
4. Deposit 777 into location 700
5. Examine location 700
6. Start at location 700

USER	TERMINAL DISPLAY
1. TURNS ON POWER	XXXXXX XXXXXX XXXXXX XXXXXX
2. L(SB) 700 (CR)	\$ L700
3. E(SB)	\$ E 002700 XXXXXX
4. D(SB) 777(CR)	\$ D 777
5. E(SB)	\$ E 000700 200777
6. S(CR)	\$ S

Even Addresses Only

The console emulator routine will not work with odd addresses. Even numbered addresses must always be used.

Successive Operations

Examine

Successive examine operations are permitted. The address is loaded for the first examine only. Successive examines cause the address to increment and will display consecutive addresses along with their contents.

Example of Successive Examine Operation

Examine Addresses 500 - 506

Operator INPUT	Terminal DISPLAY
L(SB 500 CR	L 500
E(SB)	\$E 000500 XXXXXX

E(SB)	SE 200502	XXXXXX
E(SB)	SE 200524	XXXXXX
E(SB)	SE 200506	XXXXXX

Deposit

Successive deposit operations are permitted. The procedure is identical to that used with examine.

Example of Successive Deposit Operations

Deposit 62 into Location 500
 2 into Location 502
 4 into Location 504

Operator Input	Terminal Display
L(SB) 500 CR	SL 500
D(SB) 60 CR	SD 60
D(SB) 2 CR	SD 1
D(SB) 4 CR	SD 4

Alternate Deposit - Examine Operations

This mode of operation will not increment the address. The address will contain the last data which was deposited.

Example of Alternate Deposit - Examine Operations

Load address 500, deposit the following numbers with examine after every deposit 1000, 2000, 5420.

Operator Input	Terminal Display
L(SB) 500 (CR)	SL 500
D(SB) 1200 (CR)	SD 1200
E(SB)	SE 002500 001200
D(SB) 2020 (CR)	SD 2020
E(SB)	SE 002500 002020
D(SB) 5420 (CR)	SD 5420
E(SB)	SE 002500 005420

Alternate Examine - Deposit Operations

If an examine is the first instruction after a load sequence, and is alternately followed by deposits and examines, the address will not be incremented, and the address will contain the last data which was deposited. (The above example applying to this operation, with the exception of the order of examine and deposit, the end result is the same).

Limits of Operation

The M9301 console emulator routine can directly manipulate the lower 28K of memory and the 4K I/O page. See section 5. for an explanation of techniques required to access addresses above the lower 28K.

Booting From The Keyboard

Once the \$ symbol has been displayed in response to system power coming up, or the boot switch being depressed, the system is ready to load a bootstrap from the device which the operator selects.

Console Emulator Boot Procedures

1. Find the two character boot command code on either Table 3 or Table 4, that corresponds to the peripheral to be booted.
2. Load papertape, magtape, disc, etc., into the peripheral to be booted if required.
3. Verify that the peripheral indicators signify that the peripheral is ready (if applicable).
4. Type two character code obtained from the table.
5. If there is more than one unit of a given peripheral, type the unit number to be booted (0 = 7) if no number is typed, the default number will be 0.
6. Type (CR), this initiates the boot.

Before Booting...

Always Remember:

1. The medium (Paper tape, disc, magtape, cassette, etc.) must be placed in the peripheral to be booted prior to booting.
2. The machine will not be under the control of the console emulator routine after booting.
3. The program which is booted in must:

1) be self starting or 2) allow the user to load another program by using the CONT function or 3) be prestartable after the console emulator is recalled.

3. Actuating the boot switch will always abort the program being run. The contents of the general registers (R0-R7) will be destroyed. There is no way to continue with the program which was aborted. Some programs are designed to be restartable.

Example: Booting the High Speed Reader Using the Console Emulator

An operator wishes to load the CPU Diagnostic for an 11/32 computer system. The system has a high speed reader.

Procedure:

1. Place the HALT/CONT switch in the CONT position.
2. Obtain a 8bye
 - a. Turning on system power
 - b. Actuating the boot.

(R0, R4, 3P, and PC will be printed prior to the 8.)
3. Place the absolute loader paper tape (coded leader section) in the high speed reader.
4. Type: PR (CR)

The absolute loader tape will be loaded, and the machine will halt.
5. Remove the absolute loader and place the leader of the program, in this case a CPU Diagnostic, in the reader.
6. Move the HALT/CONT switch to HALT and then return it to CONT. The diagnostic will be loaded and the machine will halt (normal for this programming; non-diagnostic programs could be self starting).
7. If program is not self starting activate the BOOT/EXIT switch; this will restart the console emulator routine.
8. Using the console emulator, deposit desired functions into the Software Switch Register (a memory address) location. See the diagnostic for the software switch register's actual location and significance.)

9. Using the console emulator, load the starting address, and start the program as described earlier in this section.

Example of Booting A Disc Using the Console Emulator

A user wishes to boot the system's RKII Disk, which contains the CPU Diagnostic which the user wants to run.

Procedures:

1. Verify the the HALT/CDMT switch is in the CDMT position and the write lock switch on the RKII peripheral is in the ON position.
2. The user turns on system power. The system terminal displays R0, R4, SP and PC which are random binary numbers. Followed by a \$ on the next line.
3. The user places the disk back into drive zero.
4. When the RK05 load light appears, the system is ready to be booted.
5. The user type in: DK (CR)
This causes the loading of the bootstrap routine into memory and the execution of that routine.
6. The program should identify itself and initiate a dialogue (which won't be discussed here).

CONSOLE EMULATOR

The following discussion will describe the effects of entering information incorrectly to the console emulator routine.

Symbols

Space Bar = (SR)

Carriage Return Key = (CR)

Any Octal Number (0 - 7) Key (X)

Non-Octal Number (8 or 9) keys (9)

(Y) = Represents:

1. All keys (other than numbers which are unknown).

2. Keys which are known but do not constitute a valid code in the context which they are entered.

Refer to previous sections for a discussion of the correct method operating the console emulator routine.

ESCAPE ROUTE

If an entry has not been completed and the user realizes that an incorrect or unwanted character has been entered, depress the rub out or delete key. This action will void the entire entry and allow the user to try again.

ERROR	DEPOSIT	ERROR	USEFUL EXAMPLES	
			OPERATOR	TERMINAL
L was followed by a key other than (23)		Terminal display will immediately return a \$ to signify an unknown code. No address is loaded.	Try again,	L(Y) \$L \$ \$
An illegal (non octal) number (0 or 9) is typed after the correct load entrance within an otherwise valid number.		Upon receipt of the illegal number, the console will ignore the entire address and return a \$.	Try Again,	L(8B)XXX9 \$LXXX \$
An incorrect alpha key is typed after the correct load entrance within an otherwise valid number.		Same as illegal no.	Try again,	L(8B) XXXX \$L XXX \$
The most significant octal number in a six bit address is greater than one.		An address will be loaded, however, the state of the most significant address bit will be determined by bit (5 only): 2 = 0 3 = 1 4 = 2 5 = 1 6 = 0 7 = 1	Try again if required,	S(8B) SXXXXXX \$L XXXX \$
An unwanted byte (octal octal number) is loaded.		Address will be loaded, but unchanged.	Try again,	
An extra (seventh) octal number is typed.		The loaded number will be incorrect. The system will accept any six word but will only remember the last six characters typed in.	Try again,	L(8B) XXXXXX \$L XXXX \$ Actually Load XXXXXXX
A memory location higher than the highest memory location available in the machine is loaded.		No errors will result unless a deposit, examine, or start is attempted.	Try Again,	L(8B) XXXXX (CR) L XXXXX
Load entrance and number were entered correctly, (CR) wasn't entered.		Machine will wait indefinitely for (CR) it will not be returned.	Type (CR)	L(8B) XXXXX (CR) \$L XXXXX XXXX(CR)
E or S is followed by a key other than space.		Terminal display will immediately return a \$ to signify an unknown code.	Try Again,	E(Y) or S(X) \$E \$S or \$ \$

Examine or start is attempted to a memory location which is higher than the highest available memory location in the machine (I/O page can be examined) or an odd memory location.

Examine is performed without loading an address prior to first examine.

Start is performed without loading an address prior to starting.

D was followed by a key other than space.

Deposit is attempted to a memory location which is higher than the highest available memory location in the machine (with the exception of the I/O page).

Deposit is performed without loading an address or knowing what address has been previously loaded.

Deposit is attempted into an odd address.

The system will hang up when (36) is executed.

Examine of an unknown address will be performed. It is possible to access an address which doesn't exist. The system may hangup in a program loop.

Start at an unknown location will occur.

Terminal display will immediately return a \$ to signify an unknown code.

The system will hang up when (33) is executed.

a. Data will be written over and lost.

b. Machine might hang up in a program loop.

The system will hang up when (38) is executed.

Depress the boot switch.

Try again or boot if system hangs up.

Reload program and try again.

Try again.

Activate the boot switch to reboot the system.

a. Immediately following the error, perform an examine to determine the address which was deposited into. Restore original contents if known.

b. Reboot machine.

Depress the boot switch.

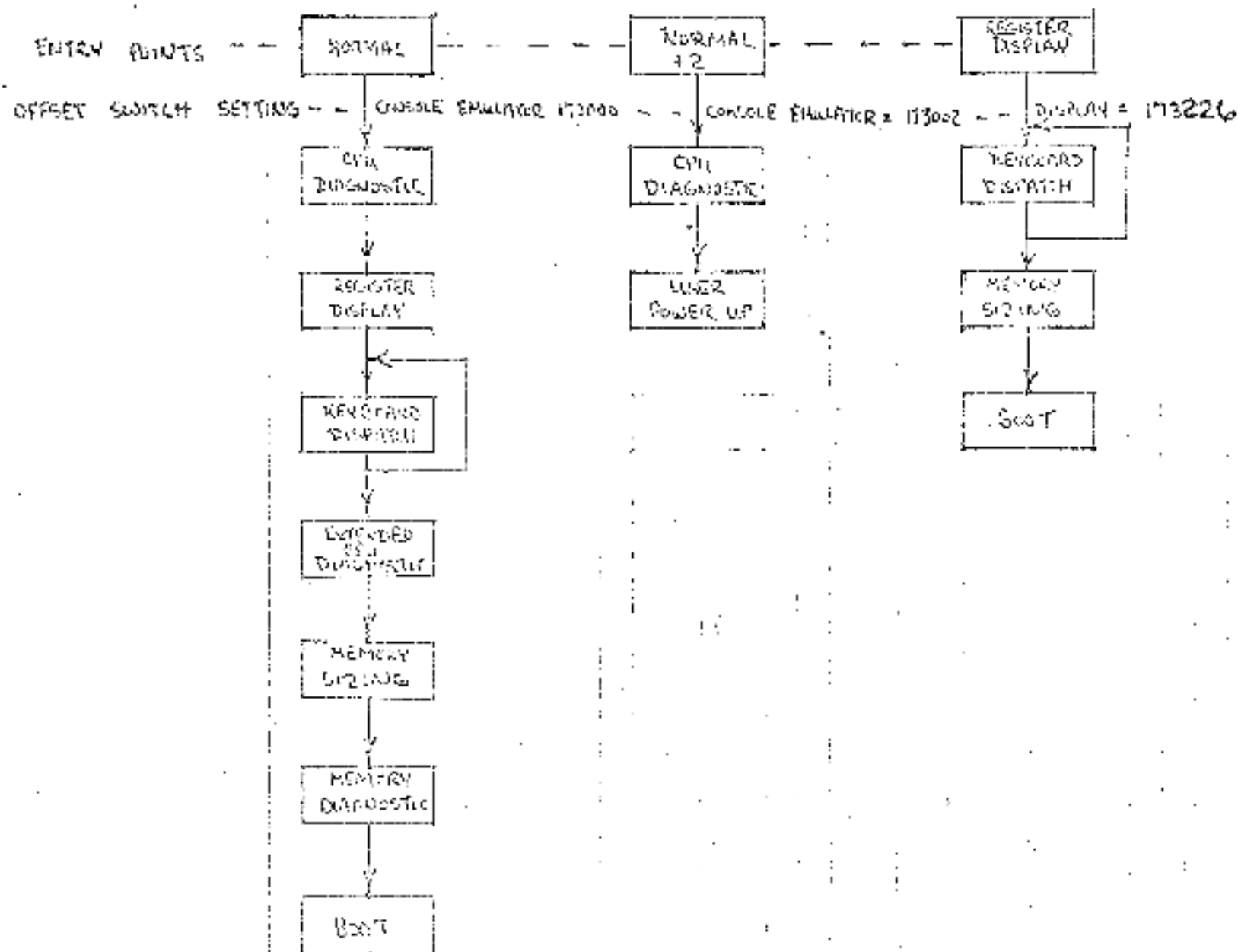
E(39) or S(36)

03Y)

\$E 07
\$S

\$D
\$

FIGURE 13
MAG-1 - VB -- PROGRAM FLOW



4.3.2.5 Program Flow of M9301-YA and M9321-YB - Figure 12 and Figure 13 show the program flows for the M9301-YA and M9321-YB respectively. Note that entry points are dependent on the switch settings S1=1 thru S1=10 on the M9321 module. Addresses which must be generated for the various devices are shown next to each entry.

4.3.3 Installation

As a universal bootstrap/terminator module, the M9321-YA and M9321-YB can be adapted by the user to meet a variety of boot requirements and system configurations. Major factors that must be considered during installation are as follows.

4.3.3.1 Power Up Reboot Enable - Automatic booting or all power ups can be enabled or disabled using the POWER UP REBOOT ENABLE switch (S1=2). If this DIP switch is set to the "OFF" position, the processor will power up normally obtaining a new PC from memory location 24(8) and a new PSN from location 26(9). When the switch is set the "ON" position, the processor will obtain its new PC from location 173024(6) which happens to be the address of the BOOT SELECT switches S1=3 thru S1=12.

The function performed by the REBOOT ENABLE switch (S1=2) can be removed to an external switch using the FAST ON tabs on the M9321 MODULE. THIS EXTERNAL SWITCH CLOSURE SHOULD BE MADE TO GROUND (ENABLING BOOT) USING FAST ON tab TP3 as a ground return. In the PCP 11/00, AND 3M, when MOS memory is present with battery backup, a battery status indication signal is generated by the power supply. This signal should be attached to the POWER UP REBOOT ENABLE Input (TP2) on the M9321. If this status signal goes low, the contents of the MOS memory is no longer valid and must be reloaded, usually from some mass storage device. The M9321, sensing the status of the memory forces a boot on power up, allowing new data to be written into memory.

If the battery status input is high (logic "1"), the M9321 will not automatically boot on power up, and execution will begin at the address specified by location 24.

4.3.3.2 Lock ROM Enable - This DIP switch S1=1 when set to the "OFF" position prevents the M9301 from responding to the I/O address range 76532 thru 76677. On both the M9301-YA and M9321-YB, this address space is occupied by the DISKETTE (RX11) and CASSETTE (TA11) bootstraps.

4.3.3.3 Boot Switch Selection - To select which device boot will be run on power-ups and external boot enables, eight DIP switches (S1=3 thru S1=12) are provided on both the M9301-YA and M9321-YB. Actual

ON=OFF selection of each switch for the various devices are shown in TABLE 3.

4.3.3.4 External Boot Switch - A device can be externally booted using the EXTERNAL BOOT input on FAST ON tab TP1. If this input is brought to ground, BUS AC LO L will be activated causing the processor to perform a POWER FAIL. Upon returning to a logic "1", this input will deactivate BUS AC LO L initiating a POWER UP sequence in the CPU and thus the boot select switches. FAST ON tab TP3 should be used as a ground return for the external boot switch.

4.4 M9301-YC

This version of the M9301 has been created specifically for the 11/72. It contains basic CPU, cache and Memory diagnostics in addition to booting from one of 9 devices. It also includes the capability of booting into other than the lowest bank of physical memory.

Physical Differences from M9301

The M9301-YC variation uses 4, Tri-State 80429 which contains information used by the 11/72. The module also requires 0u1-yo resistor for the Bus Grant lines on the Unibus.

11/72 Basic Diagnostics

4.4.1 Memory Map

See Fig. (14)

CACHE MEMORY
DIAGNOSTICS

BOOTSTRAP

PROGRAM

17773029

CPU AND MEMORY

DIAGNOSTICS

17765000

FIGURE 14
M9321-10 PROGRAM MEMORY MAP

4.4.2 General Description

The diagnostic portion of the program will test the basic CPU, including: the branches, the registers, all addressing modes, and most of the instructions in the PDP-11 repertoire. It will then set the stack pointer to kernel Dspace 0, A, R, 7, check and turn on, if requested, memory management and the unibus map, and check memory from virtual address 100 to 15777b. After main memory has been verified, with the cache off, the cache memory will be tested to verify that "hits" occur properly, then main memory will be scanned again to insure that the cache is working properly throughout the 256K of memory to be used in the "boot" operation.

If one of the cache memory tests fails, the operator can attempt to "boot" the system anyway by pressing "Continue". This will cause the program to force "Misses" in both groups of the cache before going to the bootstrap section of the program.

4.4.3 Diagnostic Test Descriptions

See fig. 15

TEST1 THIS TEST VERIFIES THE UNCONDITIONAL BRANCH

THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN THIS TEST IS ENTERED AND THEY SHOULD REMAIN THAT WAY UPON THE COMPLETION OF THIS TEST.

TEST2 TEST CLR, MODE "2", AND "BMI", "BVS", "BHI", "BLOS"

THE REGISTERS AND CONDITION CODES ARE ALL UNDEFINED WHEN THE THIS TEST IS ENTERED. UPON COMPLETION OF THIS TEST THE "SP" (R6) SHOULD BE ZERO AND ONLY THE "Z" FLOP-FLOP WILL BE SET.

TEST3 TEST "DEC", MODE "0", AND "BPL", "BGE", "BGT", "BLE"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0.

THE REGISTER ARE: R0 = 7, R1 = ? R2 = ?

R3 = ? R4 = ? R5 = ? SP = 000000

UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:

N = 1, Z = 0, V = 0, AND C = 0

THE REGISTERS AFFECTED BY THE TEST ARE:

SP = 177777

```

TEST11 THIS TEST VERIFIES THE UNCONDITIONAL BRANCH
TEST12 TEST "CLR", MODE "2", AND "BMI", "BVS", "BHI", "BLOS"
TEST13 TEST "DEC", MODE "2", AND "BPL", "BEQ", "GE", "SET", "BLE"
TEST14 TEST "ROR", MODE "2", AND "BYC", "BHS", "BHI", "BNE"
TEST15 TEST "BHI", "BLT", AND "BLOS".
TEST16 TEST "BLE" AND "BGT"
TEST17 TEST REGISTER DATA PATH AND MODES "2", "3", "6"
TEST18 TEST "ROL", "ROR", "BLT", AND MODE "6"
TEST19 TEST "ADD", "INC", "COM", AND "BCS", "BLE"
TEST20 TEST "ROR", "BIS", "ADD", AND "RLO", "BGE"
TEST21 TEST "DEC" AND "BLOS", "BLT"
TEST22 TEST "COM", "BIC", AND "BST", "BGE", "BLE"
TEST23 TEST "ADC", "CHP", "BIT", AND "BNE", "BGT", "BES"
TEST24 TEST "MOV3", "SOB", "CLR", "TST" AND "BPL", "BNE"
TEST25 TEST "ASR", "ASL"
TEST26 TEST ASH, AND SHAB
TEST27 TEST 16 KERNEL P.A.R.'S
TEST28 TEST AND LOAD KIPDR'S
TEST29 TEST "JGR", "RTS", "RTI", & "JMR"
TEST30 LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP
TEST31 TEST MAIN MEMORY FROM VIRTUAL 100 TO 28K
BOOTSTRAP ENTRY POINT IS AT 17773200
CODE TO WAIT FOR IUI2 TO COME ON LINE
THIS IS THE CODE TO READ THE SWITCH REGISTER AND DECODE IT
THIS IS THE START OF THE TM11/TU12 BOOT STRAP (MAGNETIC TAPE, T'11)
THIS IS THE START OF THE TC11/TU15 BOOT STRAP (DECTAPE, TC11-G)
THIS IS THE START OF THE RK11/RK05 BOOT STRAP (DECRAK DISK CARTRIDGE)
THIS IS THE START OF THE RP11/RP03 BOOT STRAP (DISK PACK, RP11-C)
THIS IS THE START OF THE COMMON READ CODE
THIS IS THE START OF THE RH70/TU16 BOOT STRAP (MAGNETIC TAPE SYSTEM)
THIS IS THE START OF THE R-70/RP04 BOOT STRAP (DISK PACK, RP04)
THIS IS THE START OF THE RH70/R504 BOOT STRAP (FIXED HEAD DISK, R-800)
THIS IS THE START OF THE COMMON RH-70 CODE
THIS IS THE START OF THE RX11/RX21 BOOT STRAP (FLOPPY DISK)
THIS IS THE START RESERVED FOR A FUTURE DEVICE
FUNCTION CODES FOR THE ALL OF THE DEVICES
COMMAND AND STATUS REGISTER ADDRESS TABLE
FUNCTION POINTER TABLE
STARTING ADDRESS TABLE
CACHE MEMORY DIAGNOSTIC TESTS
TEST26 TEST CACHE DATA MEMORY
TEST27 TEST VIRTUAL 28K WITH CACHE ON

```

Figure (15)

TEST4 TEST "RDR", MOVE "R", AND "BYC", "BHS", "BHI", "BNE",

UPON ENTERING THIS TEST THE CONDITION CODES ARE:

N = 1, Z = 0, V = 0, AND C = 0.

THE REGISTERS ARE: R0 = 1, R1 = 7 R2 = 7

R3 = 7 R4 = 7 R5 = 7 SP = 177777

UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:

N = 0, Z = 0, V = 1, AND C = 1

THE REGISTERS AFFECTED BY THE TEST ARE:

SP = 077777

TEST5 TEST "BHI", "BLT", AND "BLOS"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 2, V = 1, AND C = 1.

THE REGISTERS ARE: R0 = 7, R1 = 7 R2 = 7

R3 = 7 R4 = 7 R5 = 7 SP = 077777

UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:

N = 1, Z = 1, V = 1, AND C = 1

THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

TEST6 TEST "BLE" AND "BGT"

UPON ENTERING THIS TEST THE CONDITION CODES ARE:

N = 1, Z = 1, V = 1, AND C = 1.

THE REGISTERS ARE: R0 = 7, R1 = 7 R2 = 7

R3 = 7 R4 = 7 R5 = 7 SP = 077777

UPON COMPLETION OF THIS TEST THE CONDITION CODES WILL BE:

N = 1, Z = 0, V = 1, AND C = 1

THE REGISTERS ARE ALL UNAFFECTED BY THE TEST.

TEST7 TEST REGISTER DATA PATH AND MODES "2", "4", "6"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 1, Z = 0, V = 1, AND C = 1.

THE REGISTER REGISTER ARE: R0 = 7, R1 = 7, R2 = 7

R3 = 7, R4 = 7, R5 = 7, SP = 277777.

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0.

THE REGISTERS ARE LEFT AS FOLLOWS:

R0 = 125252, R1 = 000700, R2 = 125252, R3 = 125252

R4 = 125252, R5 = 125252, SP = 125252, AND MAPL00 = 125252

TEST10 TEST "ROL", "RCC", "BLT", AND MODE "6"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0.

THE REGISTERS ARE: R0 = 125252, R1 = 000000, R2 = 125252

R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252.

MAPL00 = 125252

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 0, Z = 0, V = 1, AND C = 1.
 THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
 MAP100 WHICH SHOULD NOW EQUAL 052524.

TEST11 TEST "ADD", "INC", "COM", AND "DEC", "BLE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
 N = 2, Z = 0, V = 1, AND C = 1.
 THE REGISTERS ARE: R0 = 125252, R1 = 002000, R2 = 125252
 R3 = 125252, R4 = 125252, R5 = 125252, SP = 125252,
 MAP100 = 052524.
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 2, Z = 1, V = 2, AND C = 0.
 THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
 R3 WHICH NOW EQUALS 000200, AND R1 WHICH IS ALSO 002000

TEST12 TEST "ROR", "BIS", "ADD", AND "BLU", "BGE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
 N = 0, Z = 1, V = 0, AND C = 2.
 THE REGISTERS ARE: R2 = 125252, R1 = 002000, R3 = 125252
 R4 = 002000, R5 = 125252, R6 = 125252, SP = 125252.
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 2, Z = 1, V = 2, AND C = 0.
 THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
 R3 WHICH SHOULD BE MODIFIED BACK TO 002000, AND
 R4 WHICH SHOULD NOW EQUAL 052525

TEST13 TEST "DEC" AND "BLUS", "BLT"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
 N = 0, Z = 1, V = 0, AND C = 2.
 THE REGISTERS ARE: R2 = 125252, R1 = 002000, R3 = 125252
 R4 = 000300, R5 = 052525, R6 = 125252, SP = 125252
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 1, Z = 0, V = 0, AND C = 0.
 THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
 R1 WHICH SHOULD NOW EQUAL 177777

TEST14 TEST "COM", "BIC", AND "SGT", "BLE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
 V = 1, Z = 2, V = 0, AND C = 0.
 THE REGISTERS ARE: R0 = 125252, R1 = 177777, R2 = 125252
 R3 = 000200, R4 = 052525, R5 = 125252, SP = 125252.
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 0, Z = 0, V = 1, AND C = 1.
 THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR
 R0 WHICH SHOULD NOW EQUAL 252525, AND
 R1 WHICH SHOULD NOW EQUAL 252524

TEST15 TEST "ADC", "CMP", "BIT", AND "BNE", "BGT", "BEQ"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 0, V = 1, AND C = 1,

THE REGISTERS ARE: R0 = 252525, R1 = 052520, R2 = 125252

R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252,

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0,

THE REGISTERS ARE: R0 =

R2 = 052525, R1 = 002000, R2 = 125252, R3 = 000000

R4 = 052525, R5 = 052525, SP = 125252,

TEST16 TEST "DOVB", "SOB", "CLR", "YST" AND "BPL", "BNE"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0,

THE REGISTERS ARE: R2 = 052525, R1 = 002000, R2 = 125252

R3 = 002000, R4 = 052525, R5 = 052525, SP = 125252,

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0,

R0 IS DECREMENTED BY A SOB INSTRUCTION TO 002000

R1 IS CLEARED AND THEN INCREMENTED AROUND TO 000020

TEST17 TEST "ASR", "ASL"

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 0,

THE REGISTERS ARE: R2 = 125252, R1 = 002000, R2 = 125252

R3 = 002000, R4 = 052525, R5 = 052525, SP = 125252,

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 0, V = 0, AND C = 0,

THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR

R0 WHICH IS NOW EQUAL TO 002000,

R1 WHICH IS NOW 000021, AND

R2 WHICH IS NOW 002000,

TEST18 TEST ASH, AND SWAH

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 0, V = 0, AND C = 0,

THE REGISTERS ARE: R0 = 000000, R1 = 002001, R2 = 002000

R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,

UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 1,

THE REGISTERS ARE LEFT UNCHANGED EXCEPT FOR

R1 WHICH SHOULD NOW EQUAL 002002

TEST19 TEST 10 KERNEL P, A, R, S

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:

N = 0, Z = 1, V = 0, AND C = 1,

THE REGISTERS ARE: R0 = 000000, R1 = 000000, R2 = 000000
 R3 = 000000, R4 = 052525, R5 = 052525, SP = 125252,
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 0, Z = 1, V = 0, AND C = 0.
 THE REGISTERS NOW EQUAL:
 R0 = 170000, R1 = 000000, R2 = 020000, R3 = 000000
 R4 = 052525, R5 = 125252, SP = 125252,
 ALL KERNEL P, D, R, 'S = 125252.

TEST22 TEST AND LOAD KIPDR'S

WHEN THIS TEST IS ENTERED THE CONDITION CODES ARE:
 N = 0, Z = 1, V = 0, AND C = 0;
 THE REGISTERS ARE: R0 = 170000, R1 = 000000, R2 = 020000
 R3 = 000000, R4 = 052525, R5 = 125252, SP = 125252
 UPON COMPLETION OF THIS TEST THE CONDITION CODES ARE:
 N = 0, Z = 1, V = 0, AND C = 0
 THE REGISTERS THAT ARE MODIFIED ARE:
 R0 = 170000, R1 = 020000, R2 = 070000
 ALL KERNEL IN-SPACE P, D, R, 'S (170000 - 170000) = 070000

TEST23 TEST "JSR", "RTS", "RTN", AND "JMP"

THIS TEST FIRST SETS THE STACK POINTER TO "K0PAR7" (172376),
 AND THEN VERIFIES THAT "JSR", "RTS", "RTN", AND "JMP"
 ALL WORK PROPERLY.

ON ENTRY TO THIS TEST THE STACK POINTER "SP" IS INITIALIZED
 TO 172376 AND IS LEFT THAT WAY ON EXIT.

TEST24 LOAD AND TURN ON MEMORY MANAGEMENT AND THE UNIBUS MAP

THIS TEST IS ONLY EXECUTED IF THE UPPER 4 BITS <15:12> OF
 THE SWITCH REGISTER ARE NON-ZERO. THE TEST WILL LOAD MEMORY
 MANAGEMENT TO RELOCATE TO THE 32K BLOCK NUMBER SPECIFIED,
 IT WILL ALSO SET UP THE UNIBUS MAP REGISTER 2 THRU 6 TO
 RELOCATE THE UNIBUS ADDRESSES CORRECTLY. (IE. IF BITS <15:12>
 SPECIFY BLOCK NUMBER 3, THEN YOU WANT TO BOOT INTO
 MEMORY FROM 96K TO 128K. THE KIPAR'S WILL BE LOADED AS FOLLOWS:
 KIPAR0 = 000000, KIPAR1 = 000000, KIPAR2 = 000000, KIPAR3 = 000000
 KIPAR4 = 000000, KIPAR5 = 000000, KIPAR6 = 000000,
 KIPAR7 WILL ALWAYS EQUAL 177600.
 THE UNIBUS MAP REGISTERS WILL THEN BE SET AS FOLLOWS:
 MAPL0 = 000000, MAPL1 = 03, MAPL2 = 000000, MAPL3 = 03,
 MAPL4 = 000000, MAPL5 = 03, MAPL6 = 000000, MAPL7 = 03,
 MAPL8 = 100000, MAPL9 = 03, MAPL10 = 127000, MAPL11 = 03,
 MAPL12 = 100000, MAPL13 = 03,

TEST25 TEST MAIN MEMORY FROM VIRTUAL 1000 TO 28K

THIS TEST WILL TEST MAIN MEMORY WITH THE CACHE DISABLED, FROM

VIRTUAL ADDRESS 001000 TO 157776. IF THE DATA DOES NOT COMPARE PROPERLY THE TEST WILL HALT AT EITHER 165740 OR 165756. IF A PARITY ERROR OCCURS THE TEST WILL HALT AT ADDRESS 165776, WITH THE PC + 2 ON THE STACK WHICH IS IN THE KERNEL 2-SPACE P,4,R,CS.

IN THIS TEST THE REGISTERS ARE INITIALIZED AS FOLLOWS:
 R0 = 001000, R1 = DATA READ, R2 = 067400, R3 = 001000
 R4 = 067400, R5 = 177746 (CONTROL REG.) SP = 172376

THE FOLLOWING TWO TESTS ARE CACHE MEMORY TESTS. IF EITHER OF THEM FAILS TO RUN SUCCESSFULLY THEY WILL COME TO A HALT IN THE M9321 ROM. IF YOU DESIRE TO TRY TO BOOT YOUR SYSTEM, OR DIAGNOSTIC ANYWAY, YOU CAN PRESS "CONTINUE" AND THE PROGRAM WILL FORCE MISSES IN BOTH GROUPS OF THE CACHE AND GO TO THE BOOT STRAP THAT HAS BEEN SELECTED.

TEST26 TEST CACHE DATA MEMORY

THIS TEST WILL CHECK THE DATA MEMORY IN THE CACHE, FIRST GROUP 0 AND THEN GROUP 1. IT LOADS 052525 INTO AN ADDRESS COMPLEMENT, IT WRITES AND THEN READS THE DATA. THEN IT CHECKS TO INSURE THAT ADDRESS THE DATA WAS A HIT. THEN THE SEQUENCE IS REPEATED ON THE SAME WITH 125252 AS THE DATA. ALL CACHE MEMORY DATA LOCATIONS ARE TESTED IN THIS WAY. IF EITHER GROUP FAILS AND THE OPERATOR PASSES CONTINUE THE PROGRAM WILL TRY TO BOOT WITH THE CACHE DISABLED.

THE REGISTERS ARE INITIALIZED AS FOLLOWS FOR THIS TEST:
 R0 = 1200 (ADDRESS), R1 = 2 (COUNT), R2 = 1000 (COUNT)
 R3 = 1000 (COUNT), R4 = 125252 (PATTERN) R5 = 177746 (CONTROL REG)
 SP = 172376 (FLAG OF ZERO PUSHED ON STACK)

TEST27 TEST VIRTUAL 256 WITH CACHE ON

THIS TEST CHECKS VIRTUAL MEMORY FROM 001000 THRU 157776 TO INSURE THAT YOU CAN GET HITS ALL THE WAY UP THROUGH MAIN MEMORY. IT STARTS WITH GROUP 1 ENABLED, THEN TESTS GROUP 0, AND FINALLY CHECKS MEMORY WITH BOTH GROUPS ENABLED. IF ANY OF THE THREE PASSES FAIL THE TEST WILL HALT AT "COUNT = 2". THEN IF THE OPERATOR PASSES "CONTINUE", THE PROGRAM WILL TRY TO BOOT WITH THE CACHE DISABLED.

UPON ENTRY THE REGISTERS WILL BE SET UP AS FOLLOWS:
 R0 = 001000 (ADDRESS), R1 = 3 (PASS COUNT), R2 = 67400 (MEMORY COUNTER),
 R3 = 1000 (FIRST ADDRESS), R4 = 67400 (MEMORY COUNTER),
 R5 = 177746 (CONTROL REG.), SP = 172376 (POINTING TO CODE FOR CONTROL REG.)

UPON COMPLETION OF THIS TEST MAIN MEMORY FROM VIRTUAL ADDRESS 001000 THRU 157776 WILL CONTAIN ITS OWN VIRTUAL ADDRESS.

11/70 Bootstrap

The bootstrap portion of the program looks at the lower byte of the switch register to determine which one of 9 devices and which drive number to attempt the "BOOT" from, switches <02 : 07> select the drive number (0 = 7), and switches <08 : 03> select the device code (1 = 11), if the lower byte of the switch register is zero, the program will read the set of switches on the M9381-VC to determine the device and drive number. These switches can be set by field service to select a "DEFAULT BOOT" device.

THE DEVICE CODES AND DEVICE NAMES ARE AS FOLLOWS:

1.	TM11/TU10	MAGNETIC TAPE, TM11
2.	TC11/TU56	DECTAPE, TC11=6
3.	RK11/RK25	DECPACK DISK CARTRIDGE, RK11=0
4.	RP11/RP33	DISK PACK, RP11=C
5.	RESERVED	
6.	RH72/TU16	MAGNETIC TAPE SYSTEM, THU16
7.	RH72/RP34	DISK PACK, RHP34
10.	RH72/R504	FIXED HEAD DISK, RAS04 (OR RAS03)
11.	RX11/RX81	DISKETTE

If the bootstrap operation fails as a result of a hardware error in the peripheral device the program will do a "RESET" instruction and jump back to the test that sets up and turns on memory management and tests memory. Then the program will attempt to "BOOT" again.

4.2.3 Installation

The External Back Switch and Boot on Power-Up options are not available on the M9381-VC. Therefore Power up RESCOT ENABLE switch on the module (see schematics) should always be off.

Because it is required that the diagnostic portion of the Bootstrap always be executed the LOW ROM ENABLE switch on the module (see schematics) should always be on. The remaining 8 switches should be set depending on the default device type and unit number desired. (See starting procedure and schematics).

4.4.5 Starting Procedure

Switch Settings

The lower byte of the switch register should be set to have the drive number (0 = 7) in switches <02 : 08>, and the device code (1 = 11) in switches <08 : 03>.

The upper byte of the switch register should be set to have the bank number of the 32k block of memory to be used for the bootstrap

operation (N = 17) to switches 415 : 12*,

THE DEVICE CODES ARE AS FOLLOWS:

1. TM11/TU10 MAGNETIC TAPE, TM11
2. TC11/TU56 DECTAPE, TC11=G
3. RK11/RK05 DECPACK DIS CARTRIDGE, RK11=D
4. RP11/RP03 DISK PACK, RP11=C
5. RESERVED FOR FUTURE DEVICE
6. RHT0/TU16 MAGNETIC TAPE SYSTEM, TAU16
7. R=70/RP04 DISK PACK, RNP04
10. R=70/R504 FIXED HEAD DISK, R=504 (OR R=503)
11. RX11/RX01 DISKETTE

THE MEMORY BLOCKS ARE AS FOLLOWS:

0. PHYSICAL MEMORY 0 = 20K
1. PHYSICAL MEMORY 32K = 60K
2. PHYSICAL MEMORY 60K = 92K
3. PHYSICAL MEMORY 96K = 124K
4. PHYSICAL MEMORY 128K = 156K
- .
- .
10. PHYSICAL MEMORY 256K = 284K
- .
14. PHYSICAL MEMORY 384K = 412K
15. PHYSICAL MEMORY 416K = 444K
16. PHYSICAL MEMORY 448K = 476K
17. PHYSICAL MEMORY 482K = 506K

Stacking Addresses

The normal starting address for this program is 17776580H.

If the diagnostic portion of this program fails and the operator wants to attempt to "BOOT" anyway, he must follow these steps:

1. Set up memory management if "BOOTING" into other than the lower 28K of memory.
- 2A. If device is on mamebus:
Set stack pointer to a valid address and load that address with the memory bank number he would put into switches 415:12*.
- 2B. If device is on unibus:
Set up unibus map registers 3 thru 6 to map to same memory as memory management.

3. Deposit address 173000 into the PC,
4. Set the device code and drive number in the lower byte of the switch register,
5. Press continue,

Examples:

- A. RP04 -- SET STACK POINTER TO 40220
 LOAD 200270 INTO ADDRESS 40320
 LOAD 173020 INTO THE PC (17777727)
 SET 022070 INTO SWITCHES (RP04 DRIVE 0)
 PRESS "CONTINUE"
- B. RK25 -- LOAD 173002 INTO THE PC (177777707)
 SET 002030 INTO SWITCHES (RK25 DRIVE 0)
 PRESS "CONTINUE"

Operator Action

If the diagnostic portion of the ROM fails record the PC of the "HALT" instruction and refer to the listing to find out what portion of the machine failed.

9.4.7 errors

List of error halts indexed by the address displayed

ADDRESS DISPLAYED	TEST NUMBER AND SUBSYSTEM UNDER TEST
17765024	TEST 1 BRANCH TEST
17765028	TEST 2 BRANCH TEST
17765036	TEST 3 BRANCH TEST
17765052	TEST 4 BRANCH TEST
17765066	TEST 5 BRANCH TEST
17765076	TEST 6 BRANCH TEST
17765130	TEST 7 REGISTER DATA PATH TEST
17765146	TEST 10 BRANCH TEST
17765166	TEST 11 CPU INSTRUCTION TEST
17765204	TEST 12 CPU INSTRUCTION TEST
17765214	TEST 13 CPU INSTRUCTION TEST
17765222	TEST 14 "CDM" INSTRUCTION TEST
17765236	TEST 14 CPU INSTRUCTION TEST
17765260	TEST 15 CPU INSTRUCTION TEST
17765278	TEST 16 BRANCH TEST
17765312	TEST 16 CPU INSTRUCTION TEST
17765346	TEST 17 CPU INSTRUCTION TEST
17765360	TEST 22 CPU INSTRUCTION TEST
17765374	TEST 27 CPU INSTRUCTION TEST
17765450	TEST 21 KERNEL P.A.R. TEST
17765474	TEST 22 KERNEL P.D.R. TEST
17765510	TEST 23 "JSR" TEST
17765520	TEST 23 "JSR" TEST
17765530	TEST 23 "RTS" TEST
17765542	TEST 23 "RTI" TEST
17765550	TEST 23 "JMP" TEST
17765762	TEST 25 MAIN MEMORY DATA COMPARE ERROR
17766002	TEST 25 MAIN MEMORY PARITY ERROR NO RECOVERY POSSIBLE FROM THIS ERROR
17773644	TEST 26 CACHE MEMORY DATA COMPARE ERROR
17773654	TEST 26 CACHE MEMORY NO "HIT" PRESSING "CONTINUE" HERE WILL CAUSE "BOOT" ATTEMPT FORCING "MISSES"
17773736	TEST 27 CACHE MEMORY DATA COMPARE ERROR
17773746	TEST 27 CACHE MEMORY NO "HIT" PRESSING "CONTINUE" HERE WILL CAUSE "BOOT" ATTEMPT FORCING "MISSES"
17773764	TEST 25 OR 26 CACHE MEMORY PARITY ERROR PRESSING "CONTINUE" HERE WILL CAUSE "BOOT" ATTEMPT FORCING "MISSES"

Error Recovery

Most of the above error halts are "HARD" failures, which means that there is no recovery from them. Especially the two (2) main memory halts are not recoverable, your best bet is to try to "BOOT" into another 32K bank of memory if it appears to be a main memory failure.

If the processor halts in one of the two cache tests the error can be recovered from. By pressing "CONTINUE" the program will either attempt to finish the test (if at either 17773644 or 17773736) or force "misses" in both groups of the cache and attempt to "BOOT" the system monitor with the cache fully disabled (if at either 17773654, 17773746, or 17773764).

If this program fails in an uncontrolled manner it might be due to an unexpected trap to location 002204. If this is suspected then load a "000206" into address 220004 and a "000020" into location 000226. This will cause all traps to location 000224 to halt with 0000001% in the address lights so that the operator can examine the CPU error register at location 17777766.

THE BITS IN THE CPU ERROR REGISTER ARE DEFINED AS FOLLOWS:

BIT01	= RED ZONE STACK LIMIT
BIT03	= YELLOW ZONE STACK LIMIT
BIT04	= UNIBUS TIME-OUT
BIT05	= NON-EXISTANT MEMORY (CACHE)
BIT06	= ODD ADDRESS ERROR
BIT07	= ILLEGAL HALT

5.2 EXTENDED ADDRESSING

5.1 Extended Addressing (Definition)

The console emulator routine normally allows accesses to only the lower 28K of memory and the I/O page (160000(9) to 177776(8)). However, it is possible by use of memory management to use the console emulator to access beyond 28K for the examine and deposit functions. The reader should be familiar with the concepts of memory management in the K011F processor.

5.2 Definition of Virtual and Physical Addresses

The processor manipulates 16-bit numbers within general registers and memory locations which it often uses as addresses. These addresses are designated virtual addresses as opposed to physical addresses which are asserted on the Unibus to which devices are connected to respond.

5.3 Address Mapping without Memory Management

With memory management disabled (as is the case following depressing the boot switch), a simple hardware mapping scheme converts virtual addresses to physical addresses. Virtual addresses in the 2 to 28K

range are mapped directly into physical addresses in the range from 0 to 28K. Virtual addresses on the I/O page (160000-177776) are mapped into physical addresses in the range from 128K to 134 (1368700(H)=377776(H)).

5.4 Address Mapping with Memory Management

With memory management enabled, a different mapping scheme is used. In this scheme, a relocation constant is added to the virtual address to create a physical or "relocated" address.

Virtual address space consists of eight 4K banks where each bank can be relocated by the relocation constant associated with that bank. The procedure specified in this section allows the user to:

1. Create a virtual address to type into the load address command.
2. Determine the relocation constant to relocate the calculated virtual address into the desired physical address.
3. Enable or disable the memory management hardware.

5.5 Creation of a Virtual Address

The easiest way to create a virtual address is to divide the 18 bit physical address into two separate fields - a virtual address and a physical bank number. The virtual address is represented by the lower 13 bits and the physical bank by the upper five bits. This creates a virtual address in virtual bank 0. The calculated relocation constant is placed in the relocation register associated with virtual bank 0.

For example, assume a user wishes to access location 533720. The normal access capability of the console is 0 to 28K. This address (533720) is between the 28K limit and the I/O page (760000-777776), and consequently must be accessed as a relocated virtual address, with memory management enabled. The virtual address is 13722(8) in physical bank 25(6) and is derived as follows:

All locations in either bank #25 (520000-537776) or bank #37 (I/O page: 760000-777776) may be accessed through virtual addresses 000000-217776 and 162000-177776, respectively. The relocation and

descriptor registers in the K011x6 are still accessible since their addresses are within the I/O page.

The relocation constant for physical bank 25 is 005220. This constant is added in the relocation unit to the virtual address, as shown, yielding 533720.

```

013720 Virtual address
520020 Relocated Constant (Table A-1)
-----
533720 Physical Address

```

When memory management is enabled all CPU accesses are relocated. Instructions and data access to the console emulator routine will be relocated through virtual bank 7 since their virtual addresses exist in this bank (see Table 5.1 for the corresponding addresses of each of the eight virtual banks). Note that accesses to the I/O page (virtual bank 7) are not automatically relocated with memory management while accesses to the I/O page are automatically relocated when memory management is not utilized.

5.6 Memory Management Registers

The relocation constant that is added to the virtual address is stored in a relocation register. One such register exists for each of the eight virtual banks. In addition to the relocation registers, each bank has its own descriptor register which provides information regarding the types of accesses allowed (read only, read or write, or no access).

The memory management logic also provides various forms of protection against unauthorized access. The corresponding descriptor register must be set up along with the relocation register to allow access anywhere within the 4K bank.

5.7 Address Assignments

The Unibus addresses of the relocation registers and the descriptor registers are given in Table 5.1. The relocation constant to be loaded into the relocation register for each 4K bank is provided in Table 5.2. The data to be loaded in the descriptor register to provide read/write access to the full 4K is always 077425.

The Unibus address of the control register to enable memory management is 177572. This register is loaded with the value 002K01 to enable memory management and 0 to disable it.

To complete the example previously described (location 533720), the console routine would be as follows:

```

SL 172340 /Setting relocation register for virtual bank 0
SD 5200 /To access extended memory
SL 172356 /Setting relocation register for virtual bank 7
SD 7620 /To access the I/O page
SL 172380 /Address of descriptor register, virtual
SD 77426 /bank 2
SL 172316 /Address of descriptor register, virtual
SD 77426 /bank 7
SL 177572 /Address of control registers; enable
SD ! /memory management
SL 13728 /Virtual address of location desired
SD (examine) /The data in location 533728
 /will be typed.

```

Table S.1
Unibus Address Assignments

Virtual Address	Virtual Bank	Relocation Register	Descriptor Register
1600000-177776	7	172356	172316
1400000-157776	6	172354	172314
1200000-137776	5	172352	172312
1000000-117776	4	172350	172312
0800000-097776	3	172346	172306
0400000-057776	2	172344	172304
0200000-037776	1	172342	172302
0000000-017776	0	172340	172300

Table 3.2
Relocation Constants

Physical Bank Number	Relocation Constant
37	227602
36	227402
35	227202
34	227002
33	226802
32	226602
31	226402
30	226202
29	226002
28	225802
27	225602
26	225402
25	225202
24	225002
23	224802
22	224602
21	224402
20	224202
19	224002
18	223802
17	223602
16	223402
15	223202
14	223002
13	222802
12	222602
11	222402
10	222202
9	222002
8	221802
7	221602
6	221402
5	221202
4	221002
3	220802
2	220602
1	220402
0	220202

Loading a new relocation constant into the relocation register for virtual bank 2 will cause virtual addresses 022400-177776 to access the new physical bank. A second bank can be made accessible by loading the relocation constant and descriptor data into the relocation and descriptor registers for virtual bank 1 and accessing the location through virtual address 022220-037776. Seven banks are accessible in this manner, by loading the proper constants, setting up the descriptor data, and selecting the proper virtual address. Bank 7 (1/2 page) must remain relocated to physical bank 37 as it is accessed by the CPU to execute the console emulator routine.

Memory management is disabled by clearing (loading with 99) the Control Register 177572. It should always be disabled prior to typing a 'boot' command.

The start command automatically disables memory management and the CPU begins executing at the physical address corresponding to the address specified by the previous Load Address command. Depressing the boot switch automatically disables memory management. The contents of the relocation registers are not modified.

The HALT/CONTINUE switch has no effect on memory management.

6.2 H9301-YD

6.1 Purpose

The H9301-YD is programmed to provide transparent pass-through of data between a terminal or a satellite computer and an asynchronous serial line on the base computer. It also contains all of the necessary instructions for requesting a secondary mode program load and for accepting a down-line load on its serial line from another machine using ODUMP protocol. These features enable a PDP-11 computer to be a satellite in a REMOTE-11 system.

6.2 Functionality

6.2.1 Normal Bootstrap (SA=173000)

Ordinarily, when the RDM code is initiated, the satellite comes up in pass-through mode. First, the memory size of the computer is ascertained. Then, necessary communications registers are set up, and the OSOP message "Enter terminal mode" is sent on the serial line. All further communication is in ASCII with the RDM program polling the ready flags in the four control and status registers to determine the next action. XON ("Q") and XOFF ("S") are supported with the satellite computer, and transmission is assured to be full duplex.

The only way that terminal mode may be discontinued is the receipt of a DDCMP message. The ROM only accepts the messages, "Program load without transfer address", "Program load with transfer address", and "Enter terminal mode."

6.2.2 Secondary mode bootstrap.

An alternate start address (173214) will cause the "Enter terminal mode" message to be replaced by "Request secondary mode program load." All other actions are identical to the normal bootstrap. The host machine should respond to this message with a program load so that terminal mode is only transiently activated. The bus addressed 177550-177566 will be addressed during this time. The secondary mode program load message may be used for loading programs in to satellites without terminals or for loading a scroller into a machine with a graphics terminal.

6.2.3 Sending DDCMP Messages

A callable subroutine within the ROM will send DDCMP "Rdy" mode messages. Location 162 is loaded by the 49307 with the address of this subroutine. To use it, call by

```
MOV     4MSG, R5
JBR PC, 162
```

where MSG has the following format

bytes 0 and 1 contain the number of bytes in the message

byte 2 has an OSCP code

bytes 3 through n have the data (if any)

The message is sent using interrupt driven code, but control is not returned to the user program until the message has been completely sent out.

4.2.4 Receiving DDCMP Messages

The boot will automatically receive DDCMP messages if properly initialized and the interrupt for the serial line receive register is enabled. A program to do this follows:

```

MOV    #150,R0      ; GET ADDRESS OF DESCRIPTOR BLOCK
MOV    R0,R2        ; SETUP DESCRIPTOR POINTER
CMP     (R2)+,(R2)+  ; R2 R2 + 2
MOV    R2,(R0)       ; RESET BUFFER POINTER
MOV    #10,,=(R2)    ; BYTE COUNT OF DDCMP HEADER
CLR     =(R0)        ; INITIALIZE CRC AND FLAGS
CLR     =(R2)
CLR     =(R2)        ; ZERO FOR NO COMPLETION ROUTINE
MOV    #160,=(SP)    ; GET DL ADDRESS INPUT
ADD     #776,(SP)    ; STATUS REGISTER FROM BOOT
BIS     #102,0(57)+  ; ENABLE INTERRUPT
TST     =(R0)        ; WAIT UNTIL MESSAGE COMPLETE
BEQ     ,=4
BMI     ERROR
CMP     (R0)+,(R0)+  ; POINT TO DDCMP CODE

```

To restart the boot:

```
JMP #164
```

The M9301-70 uses locations 150-167 for communications and 172-171 for temporary data during program loads. It also loads location 54 with the high usable memory address. The address in 54 has been adjusted to leave room for buffers and a stack for use by the boot.

6.3 Using the M9321-YD

The M9321-YD ROM will run on any PDP-11 computer. Two PL-11's are required with the following addresses and vectors:

FUNCTION	ADDRESS	VECTOR
Local terminal	177560	60
Interprocessor	1775610	400

The ROM may be activated by placing the address given for the desired function in switch register and pressing LOAD ADDRESS, START or by utilizing the power-up bootstrap feature of the M9321. The DIP switches should all be off for normal boot. Secondary mode requires the switches to be set to -----.

6.4 Program Listing

7.0 APPENDIX

7.1. General description:

This fully decoded 2048 Bit Memory, is organized as 512 words of 4 bits each. It has TTL compatible inputs and TTL compatible tristate outputs. There is also one Chip Enable provided whose outputs are buzzable to allow for memory expansion capability.

Memory Arrays are addressed in straight binary with full tri-state decoding. An overriding chip-select input is provided which when taken high, will inhibit the function causing all outputs to be in a high-impedance state they neither loads nor drives the bus lines. Data as specified by C.E.C. are permanently programmed into the 2048 bit locations.

7.2. APPLICABLE DOCUMENTS (Latest revision or data of order):

Digital:

A-5P-7605212-0-2, "Process Compatibility Test Methods".

A-PS-1900032-06, "General Requirements DEC Quality Assurance Specification for Bipolar Integrated Circuits".

7.3. REQUIREMENTS:

This device shall meet the following requirements under all operating

conditions and over the full operating free Air Temperature Range.

7.3.1 Mechanical:

7.3.1.1 Package Configuration: - 16 Pin dual in line shall meet the requirements of Digital Specification A-P5-1927002-68, Section 1.2.5.

7.3. REQUIREMENTS (Continued)

7.3.1.2 Material (Packaging): - Shall be ceramic or plastic (Epoxy-B) or equivalent. Silicone package shall not be shipped without prior written approval from D.E.C.

7.3.1.3 Pin Configuration: - Shall meet the requirements of Digital, A-P5-1900002-68, be of uniform high quality, delivered free from grease, oil and other contaminants.

7.3.1.4 Pin Connection Diagram: - Shall meet the requirements of Figure 1.

7.3.1.5 Thermal Resistance:

- A. Junction to Ambient:
R_{θJA} = 75 C/W maximum (measured in free-air with the device soldered into a printed circuit board).
- B. Junction to Case:
R_{θJC} = 28 C/W maximum (measured with the device immersed in free bath).

7.3.2 Electrical:

7.3.2.1 Logic Diagram: - Shall meet requirements of Figure 2.

7.3.2.2 Absolute Maximum Ratings: - Reference Table 1.

7.3.2.3 Recommended Operating Conditions = Reference Table 11.

7.3.2.4 Electrical Characteristics = Reference Table 11.

7.3.2.5 Test Load and Timing Diagrams = Shall meet the requirements of Figure 3.

7.3.3 Environmental:

7.3.3.1 Temperature:

- A. Operating: 0 C to +75 C,
- B. Storage: -65 C to +150 C

7.3.3.2 Altitude = The device shall not be mechanically or electrically damaged at altitudes of 50,000 feet (92mm mercury).

7.3.3.3 Humidity:

- A. Operating: 10% to 90% R.H. over the operating temperature range, (non-condensing).
- B. Storage: 5% to 95% R.H. over the storage temperature range, (condensing allowed).

7.3 REQUIREMENTS (Continued)

7.3.4 Markings:

Shall contain vendor name or symbol, vendor part number, Pin 1 location and date code.

7.3.5 Process Compatibility Test Methods:

The device shall stay within the initial electrical/mechanical requirements and shall not show any evidence of degradation in cosmetics when subjected to the following methods,

7.3.5.1 Marking: Digital, A=SP=7005212=0=2, Section 1, Test Method 120.

"Solvent Resistance".

7.3.5.2 Refer to Digital, A=PS=1922002-G8 for other Process Compatibility Requirements.

7.3.6 Shelf Life:

The device shall meet the initial Electrical/Mechanical requirements after 1 year at storage requirements for temperature and relative humidity.

7.3.7 Packaging and Shipping:

Marking on the packaging shall contain as minimum information, vendors name or symbol, vendors part number, Purchase Order Number and quantity. It shall meet I.C.C. requirements for shipment by airplane, rail and truck. Devices shall be packaged to meet the requirements of Digital A=PS=1900222-G5.

7.3.8 Digital A=PS=1900222-G5:

General Requirements DEC Quality Assurance Specification for Bipolar Integrated Circuits shall apply where no other document is specifically referenced.

7.4. CONFLICT OF REQUIREMENTS:

The requirements of this document shall take precedent over all and any documents when a conflict arises.

7.5. Approval:

The devices submitted under this specification shall have been initially approved by Digital Equipment Corporation. Approval shall be given only after samples representative of the vendors normal production run have been examined, tested and found to meet the requirements as specified.

7.6. Construction changes:

Approved vendors who desire at any time to make a change in the design, materials, process, process control which impact any requirement, shall submit a written request describing in detail the changes requested. Also, evidence to justify such changes. The cognizant engineer will then submit this request to the proper Engineering Department(s) Component Engineering Group and all product lines affected. No changes shall be incorporated until written approval has been received from the above mentioned group or groups authorized by the Cognizant Engineer.

Failure to comply shall be sufficient cause for removal as "Qualified Source"; complete requalification may be required before the product is deemed acceptable.

TABLE 1
ABSOLUTE MAXIMUM RATINGS

PARAMETER NAME	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	VCC	+7.0	V
Input Voltage	VIN	-1.5 TO +6.5	V
Output Voltage	VOU1	+0.3 TO +5.5	V
Temperature: Storage Range	Tsto	+65 to +150	°C

TABLE 11
RECOMMENDED OPERATING CONDITIONS

PARAMETER NAME	SYMBOL	VALUE			UNIT
		MIN.	NOM.	MAX.	
Supply Voltage	VCC	4.75	5.0	5.25	V
Temperature: Operating Free-Air	Ta	0		+75	°C

TABLE 111

ELECTRICAL CHARACTERISTICS

V_{CC} CHARACTERISTICS (V_{CC}=5.0V, 45%, 1s, 25°C)

PARAMETER NAME	SYMBOL	TEST CONDITIONS	VALUE MIN, MAX, TYP	UNIT
High Level Input Voltage	V _{IH}		2.7	V
Low Level Input Voltage	V _{IL}		0.8	V
Input Clamp Voltage	V _{IC}	(1) I _{IN} =1mA	-1.5	V
High-Level Output Voltage	V _{OH}	(1) I _{OL} =2.1mA	2.4	V
Low-Level Output Voltage	V _{OL}	V _{CC} =0.0V (1) I _{OL} =1mA	0.45	V
Input Breakdown Voltage	BV _{IN}	(1) I _{IN} =1mA	5.5	V
Output Leakage Current	I _{OL}	V _{CC} =5.5V, V _{OL} =0.4V(1)	100	nA
		10 (High State) V _{CC} =5.5V, V _{OL} =2.4V	40	nA
		17 (High State) V _{CC} =0.0V, V _{OL} =0.4V	40	nA
SUPPLY CURRENT	I _{CC}	Inputs either Open or At Ground(1)	100	nA
Output Short Circuit Current	I _{OS}	V _{OH} =V _{CC}	-15	mA
Address Input Load Current	I _A	V _A =0.0V	-1.5	mA
Chip Enable Input Load Current	(1) I _{EB}	V _{EB} =0.0V	-1.5	mA
Address Input Leakage Current	(1) I _{IA}	V _A =2.4V	50	nA
Chip Enable Leakage Current	(1) I _{EB}	V _{EB} =2.4V	50	nA
Capacitance C _{IN}	C _{IN}	V _{IN} =0.0V, V _{CC} =0V	7	pF
Capacitance C _{OUT}	C _{OUT}	V _O =2.4V, V _{OL} =0V	0	pF

NOTE

The above characteristics are guaranteed to meet the output high level state when the chip is enabled ($CE=0.4V$) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

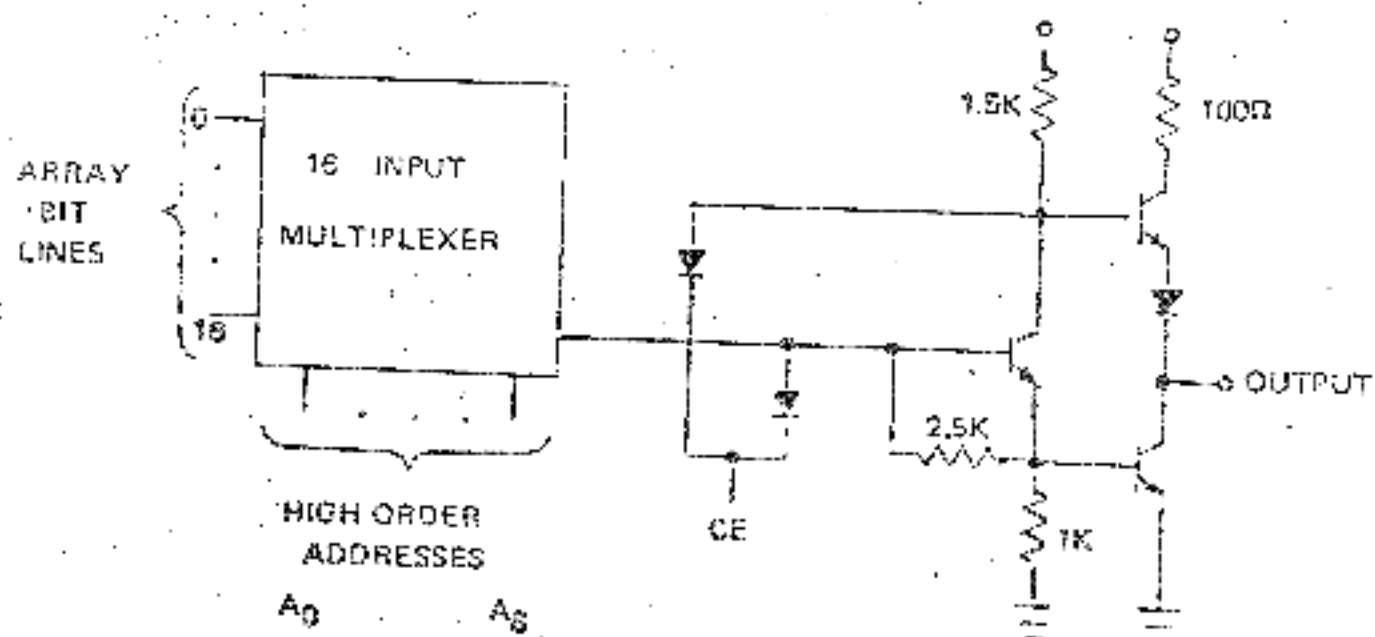
ELECTRICAL CHARACTERISTICS (Continued)

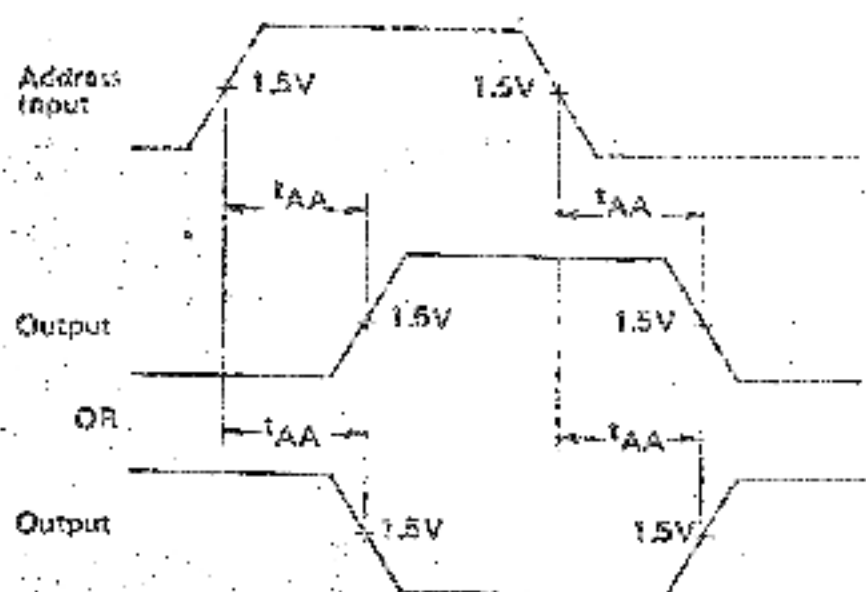
A.C. SWITCHING CHARACTERISTICS ($T_A=25^\circ C$, $V_{CC}=5.2V$)

PARAMETER NAME	SYMBOL	MIN.	VALUE 25°C TO 75°C			UNIT
			MAX.	MIN.	MAX.	
Access Time (Via Address Inputs)	t_{AA}		72	80		ns
Output Disable Inputs	$t_{DIS}(2)$		30		35	ns
Output Enable Time	$t_{EN}(2)$		32	35		ns

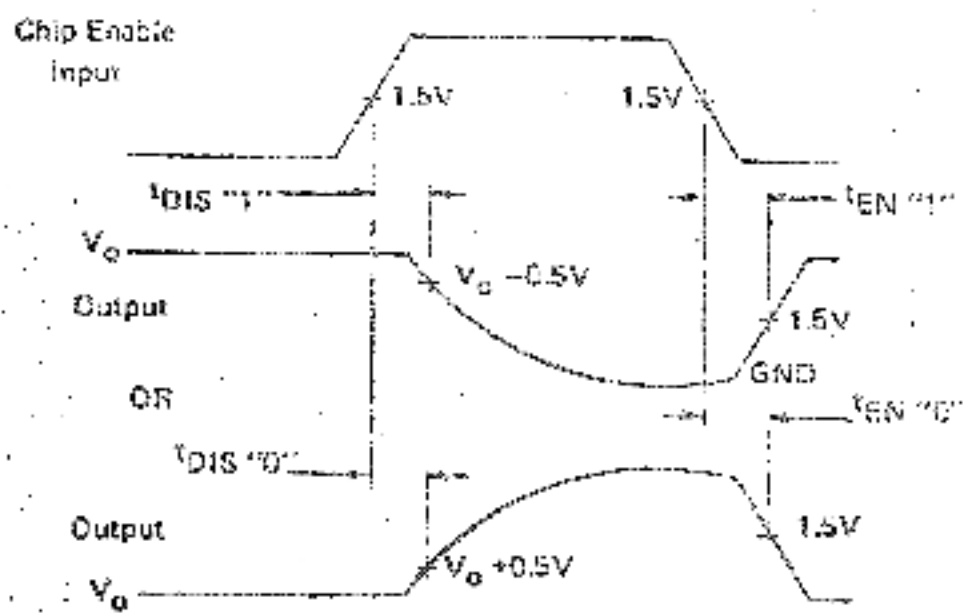
NOTE

Output Disable Time is the time taken for the output to reach a high resistance state when either $CH0$ Enable is taken high. Output Enable time is the time taken for the Output to become active when both $CH0$ Enables are taken low. The high resistance state is defined as a point on the output waveform equal to a V of 2.5V from the active output level.





ACCESS TIME VIA ADDRESS INPUTS



OUTPUT ENABLE AND DISABLE TIMES

SWITCHING WAVEFORMS

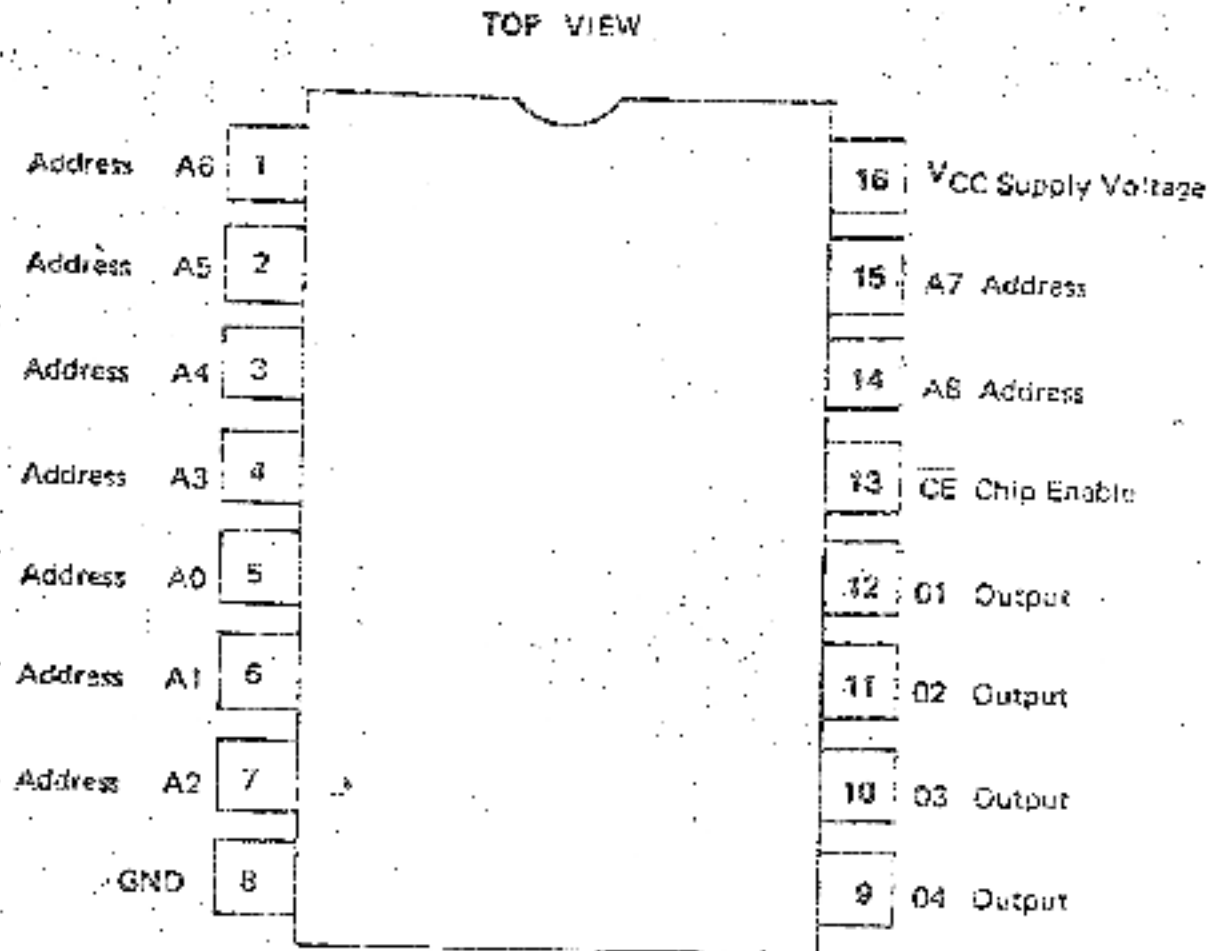


FIGURE 1

PIN CONNECTION DIAGRAM

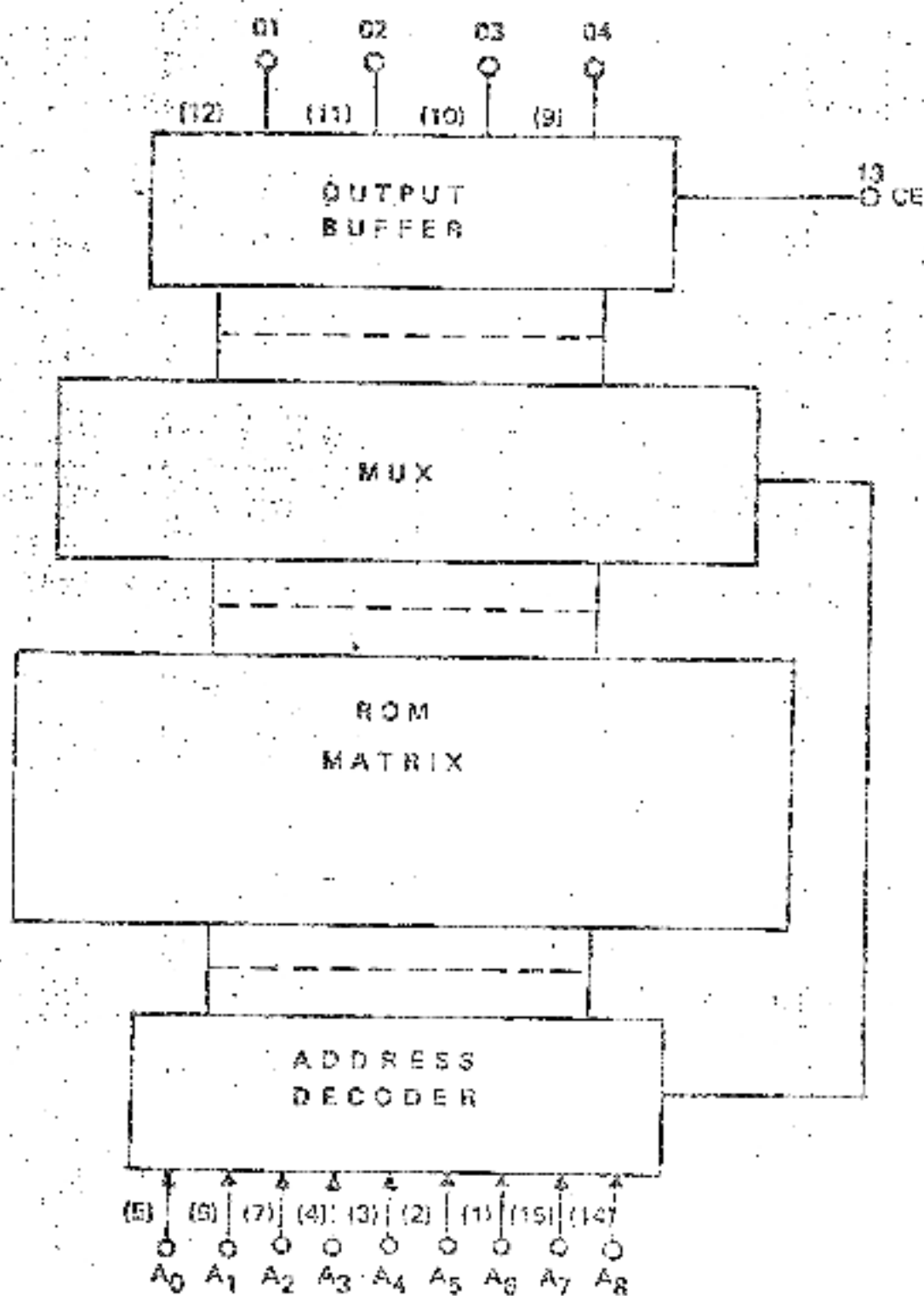


FIGURE
LOGIC BLOCK DIAGRAM

PROGRAMMING PROCEDURE:

Device Description: This memory array is manufactured with logic level sense in all storage locations. In order to program a logic level one at a specified bit, electrically alter a bit at logic level "2" to logic level "1". There are 2348 bits which are organized as 512 words of 4 bits each.

The device is programmed per the Digital Equipment Corporation factory specification.

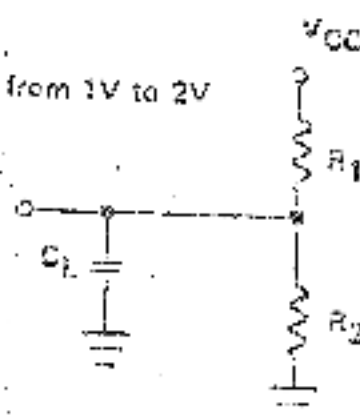
CHARACTERISTICS	LIMIT	UNITS	CONDITION
Programming Pulses			
Amplitude	$20V \pm 5\%$	mA	Constant Current
Voltage (clamp)	$28.0 \pm 3\% \pm 2\%$	V	voltage limit of current source.
Ramp Rate dv/dt Pulse width	7V max, $7.5 \pm 5\%$	V/ μ s μ s	15 V points, 150 load.
Pulse Cycle	70% min.		
Sense Current	20.0 ± 3.5	mA	The sense current must be interrupted after each address change for 12 μ s min. The sense current ramp rate dv/dt must be $< 70V/\mu$ s, and clamped to $28.0V \pm 3\% \pm 2\%$.
Programming Vcc	$5.0 \pm 5\% \pm 0\%$	V	
Maximum Sensed Voltage for a programmed "1".	7.0 ± 2.1	V	A bit programmed when two successive sense readings 13 μ s apart with no intervening programming pulses, pass the limit. When this condition has been met, 16 additional program pulses are applied and the pulse train is then terminated.
Delay from trailing edge of program pulse before sensing output voltage	3.7 min.	μ s	
To Electrically Alter a Bit at Logic "2" to Logic "1".	230	μ s	

Input Conditions:

Amplitude -0V to 3V

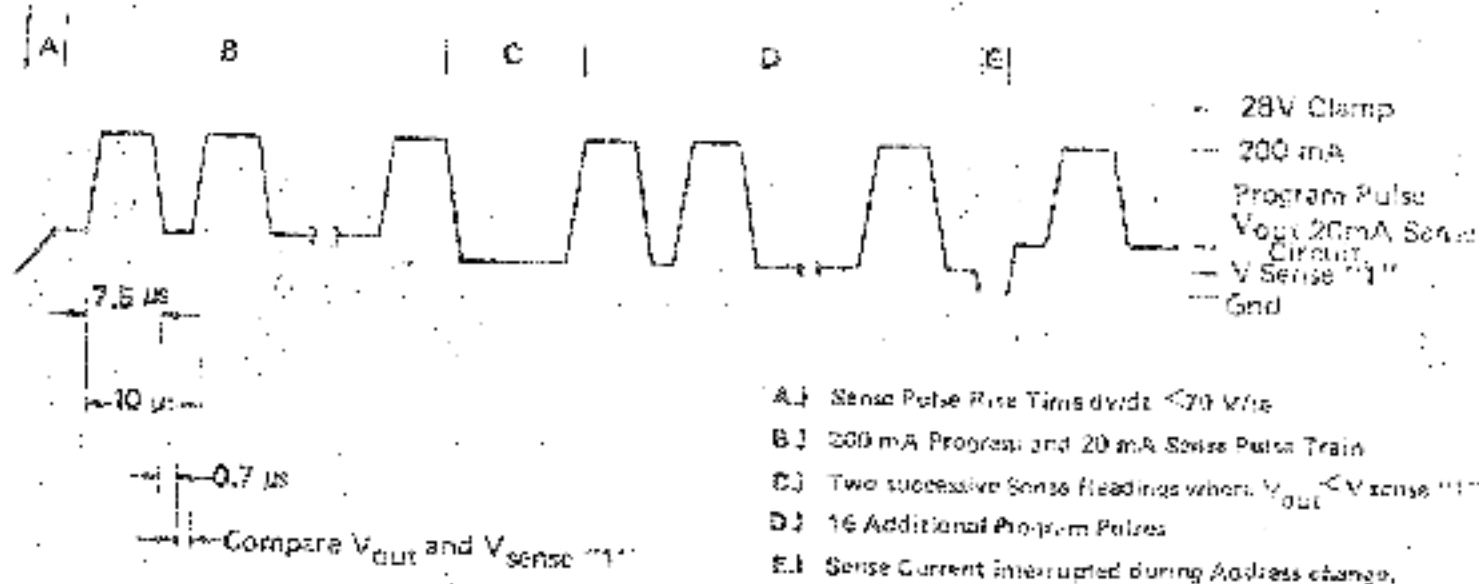
Rise & Fall Time -5ns from 1V to 2V

Frequency - 1Mhz



SWITCHING PARAMETER	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30 pF
t_{DIS} "1"	∞	600 Ω	10 pF
t_{DIS} "0"	300 Ω	600 Ω	10 pF
t_{EN} "1"	∞	600 Ω	30 pF
t_{EN} "0"	300 Ω	600 Ω	30 pF

SWITCHING TIME TEST CONDITION
OUTPUT LOAD CIRCUIT



VOLTAGE WAVEFORM DURING PROGRAMMING

