MS11-L MOS memory technical manual

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MS11-L MOS memory technical manual

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CHAPTER 1
CHARACTERISTICS AND SPECIFICATIONS

1.1 INTRODUCTION

This manual describes the MS11-L which is a metal oxide semiconductor (MOS), random access memory (RAM) designed to be used with the PDP-11 Unibus or special buses with reserve addressing capability. The memory assumes the role of a slave device to the PDP-11 processor or to any peripheral device that is designated bus master. The MS11-L provides storage for 18-bit words (16 data bits and 2 parity bits) and also contains parity control circuitry and a control and status register (CSR). There are four versions of the MS11-L that are differentiated by the total memory capacity available on the module (Table 1-1). Note that the maximum configuration is 128K (131,072 words).

Table 1-1 MS11-L Versions

Option Designation	Module Designation	Storage Capacity
MS11-LA	M7891-AA	32K × 18-bit
MS11-LB	M7891-BA	64K × 18-bit
MS11-LC	M7891-CA	96K × 18-bit
MS11-LD	M7891-DA	128K × 18-bit

1.2 GENERAL DESCRIPTION

The MS11-L consists of a single, hex-height module (M7891) that contains the Unibus/special bus interface, timing and control logic, refresh circuitry and a MOS storage array. The module also contains circuitry to generate and check parity, and a control and status register (CSR).

The memory starting address can be set at any 4K boundary within the 128K Unibus address space or 2048K special bus address space. (Special buses compatible with the MS11-L contain 22 address lines as opposed to 18 Unibus address lines.) The MS11-L allows the top 2K, 4K or 8K of the Unibus or special bus address space to be reserved for the I/O peripheral page. Note that there is no address interleaving with the MS11-L.

The memory storage elements are 16384 × 1-bit, MOS dynamic RAM devices. The MOS storage array contains 18 of these devices for each 16K bank of memory; e.g., a 128K memory contains 144 storage devices, a 64K memory contains 72 storage devices. Unlike core memory, the read operation for MOS storage devices is nondestructive; consequently, the write-after-read operation associated with core memory is eliminated. The MOS storage devices must be periodically refreshed so that the data remains valid.

The MS11-L memory uses +5 V and either ±15 V or +12 V power. Since the MOS storage devices are volatile (data is not retained when power is lost), a battery backup unit is available which supports the MOS power supply regulator(s). Therefore, dc power is available to MOS memory only, for a limited time during an ac power failure. In the battery support mode, power is used only to refresh the MOS storage array so that battery backup time, and therefore, data retention time, are maximized. A green LED on the module stays on as long as +5 V power is supplied to the logic required for memory refresh.

The control and status register (CSR) in the MS11-L contains 11 bits which are used to store information in case of a parity error and control certain parity functions. The CSR has its own address in the top 2K of the Unibus or special bus address space and can be read or written into by any device designated as bus master, even during a memory refresh cycle.

The parity control circuitry in the MS11-L generates parity bits based on data being written into memory during a DATO or DATOB bus cycle. One parity bit is assigned to each data byte and is stored with the data in the MOS storage array. When data is retrieved from memory during a DATI or DATIP bus cycle, the parity of the data is recalculated and compared to the stored bits. If the parity bits correspond, the data is assumed to be correct; if the parity bits do not correspond, the data is assumed to be unreliable and the memory initiates the following action:

1. The parity error bit (bit 15) of the CSR is set to a logical 1.
2. A red LED on the module turns on, providing a visual indication of a parity error.
3. If bit 0 in the CSR is set, the memory asserts BUS PB L which warns the processor that a parity error has occurred.
4. Part of the address of the faulty data is recorded in the CSR (Paragraph 2.3).

1.3 SPECIFICATIONS

1.3.1 Functional Specifications

Capacity		
MS11-LA	32,768 (32K) words	18-bit words (2 data bytes with 2 parity bits)
MS11-LB	65,536 (64K) words	
MS11-LC	98,304 (96K) words	
MS11-LD	131,072 (128K) words	
Refresh Timing		
Cycle time	570 ns (typical), 610 ns (maximum)	
Repetition rate	One cycle every 14.5 μs (typical), 13.5 μs (maximum)	

NOTE

Refresh cycle time is defined as the time interval between the assertion of REF REQ L and the negation of BUSY L. These signals are internal to the memory module.

Access and Cycle Times (Table 1-2)

Table 1-2 Access and Cycle Times

Bus Mode	Access Time (ns)		Cycle Time (ns)	
	Typical	Maximum	Typical	Maximum
DATI/DATIP (Memory)	385	415	510	540
DATO/DATOB (Memory)	125	150	510	540
DATI/DATIP (CSR)	60	80	---	---
DATO/DATOB (CSR)	60	80		

NOTES

1. **Access time – The time interval between memory reception of BUS MSYN L (at the input of the receiver) and the assertion of BUS SSYN L on the Unibus or special bus.**

   Cycle time – The time interval between the assertion of MEM REQ L and the negation of BUSY L. These signals are internal to the memory module.

2. **If the memory is accessed by a bus master during a refresh cycle (causing a refresh conflict), the data transfer is delayed until the refresh cycle is completed. In the worst case, memory access and cycle times are increased by the entire refresh time; 570 ns (typical), 610 ns (maximum). Access to the CSR is not affected by a refresh cycle.**

3. **If the memory is accessed by a bus master momentarily before the start of a refresh cycle, memory cycle and access times are increased by the refresh arbitration time; 60 ns (typical), 90 ns (maximum). Access to the CSR is not affected by refresh arbitration.**

1.3.2 Electrical Specifications

Voltage Requirements

+5 V ±5%, max ripple = 0.2 V p-p
+15 V +10%, -3.3% or +12 V ±5%, max ripple = 1 V p-p
15 V ±10% or 12 V ±10%, max ripple = 1 V p-p

Current and Power Requirements — Tables 1-3 and 1-4

1.3.3 Physical and Environmental Specifications

MS11-LA	M7891-AA	All versions are hex-height multilayer, 21.6 × 38.1 cm (8.5 × 15 inch)
MS11-LB	M7891-BA	
MS11-LC	M7891-CA	
MS11-LD	M7891-DA	
Operating Temperature		5° to 50° C (41° to 122° F)
Humidity		10 to 95 percent (noncondensing)

Table 1-3 Current and Power Requirements

Memory Option	+5 V		+5 VBBU		-12 V/-15 V		+12 V/+15 V			
							Standby		Active	
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
MS11-LA (32K × 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	9 mA (0.108/0.125 W)	11 mA (0.145/0.182 W)	85 mA (1.02/1.28 W)	105 mA (1.32/1.73 W)	485 mA (5.82/7.28 W)	540 mA (6.8/8.91 W)
MS11-LB (64K × 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	12 mA (0.144/0.18 W)	14 mA (0.185/0.23 W)	140 mA (1.68/2.1 W)	160 mA (2.02/2.64 W)	535 mA (6.42/8.03 W)	595 mA (7.59/9.82 W)
MS11-LC (96K × 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	15 mA (0.180/0.225 W)	17 mA (0.224/0.281 W)	190 mA (2.28/2.85 W)	215 mA (2.71/3.55 W)	590 mA (7.08/8.85 W)	650 mA (8.19/10.73 W)
MS11-LD (128K × 18)	1.5 A (7.5 W)	1.8 A (9.5 W)	1.0 A (5.0 W)	1.3 A (6.8 W)	18 mA (0.216/0.27 W)	20 mA (0.264/0.33 W)	240 mA (2.88/3.6 W)	265 mA (3.34/4.73 W)	640 mA (7.68/9.6 W)	700 mA (8.82/11.55 W)

NOTES

1. The module has inputs for two sources of +5 V power designated +5 VBBU (optionally battery supported) and +5 V (not battery supported). The voltage tolerances required for the +5 V and +5 VBBU inputs are the same. The total module consumption of +5 V power during normal operation is equal to the sum of the +5 V and +5 VBBU ratings (Paragraph 2.2.1.4).

2. The standby and active ratings for +5 V, +5 VBBU and -12 V/-15 V are the same.

3. The maximum power ratings have been calculated using the worst case voltage tolerances.

Table 1-4 Total Module Power Requirements

Memory Option	Standby		Active		Battery Backup Mode	
	Typ	Max	Typ	Max	Typ	Max
MS11-LA (32K × 18)	13.6/13.9 W	17.8/18.2 W	18.4/19.9 W	23.3/25.4 W	6.1/6.4 W	8.3/8.7 W
MS11-LB (64K × 18)	14.3/14.8 W	18.5/19.2 W	19.1/20.7 W	24/26.4 W	6.8/7.3 W	9/9.7 W
MS11-LC (96K × 18)	15/15.6 W	19.2/20.1 W	19.8/21.6 W	24.7/27.3 W	7.5/8.1 W	9.7/10.6 W
MS11-LD (128K × 18)	15.6/16.4 W	19.9/21 W	20.4/22.4 W	25.4/28.2 W	8.1/8.9 W	10.4/11.5 W

NOTES

1. **XX/YY = rating when ±12 V/±15 V power is used.**
2. **The maximum power ratings have been calculated using the worst case voltage tolerances.**

1.4 RELATED DOCUMENTS

Additional reference information can be found in the documents listed below.

Title	Document No.	Availability
PDP-11 Family Field Installation and Acceptance Procedures Manual	EK-FS003-IN	Hardcopy and Microfiche
PDP-11 Peripherals Handbook	EB-05961	Hardcopy only
PDP-11/04/34/45/55/60 Processor Handbook	EB-09340	Hardcopy only

These documents can be ordered from:

Digital Equipment Corporation
Supplies and Accessories Group
Cotton Road
Nashua, New Hampshire 03060

For information concerning Microfiche Libraries, contact:

Digital Equipment Corporation
Micropublishing Group

BU/F
Bedford, MA.

CHAPTER 2
INSTALLATION AND PROGRAMMING

2.1 GENERAL

This chapter presents the information necessary for installation and programming of the MS11-L and applies to all versions of the memory. Installation procedures include: switch/jumper settings, backplane placement, power voltage checks and MAINDEC testing. Programming information includes a discussion of bit assignments in the control and status register (CSR). Power voltage regulation on the module is also discussed in this chapter.

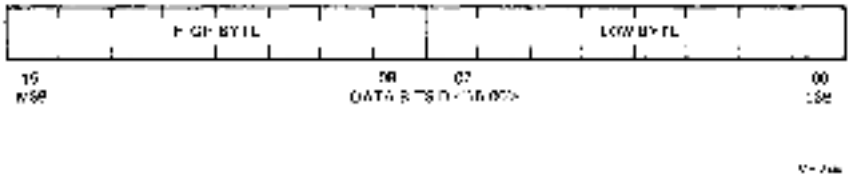
2.2 INSTALLATION

2.2.1 Switch and Jumper Configurations

The MS11-L contains 15 jumpers and two switchpacks; one switchpack contains four switches (S1-1 to S1-4) and the other contains nine switches (S2-1 to S2-9). The location of the jumpers and switches is shown in Figure 2-1. In normal operation, jumpers W10-W16 and W20 should be IN. The other jumpers are used to specify Unibus or special bus operation, I/O peripheral page size, and the dc power inputs available to the module. The memory starting address and CSR address are specified by the switches.

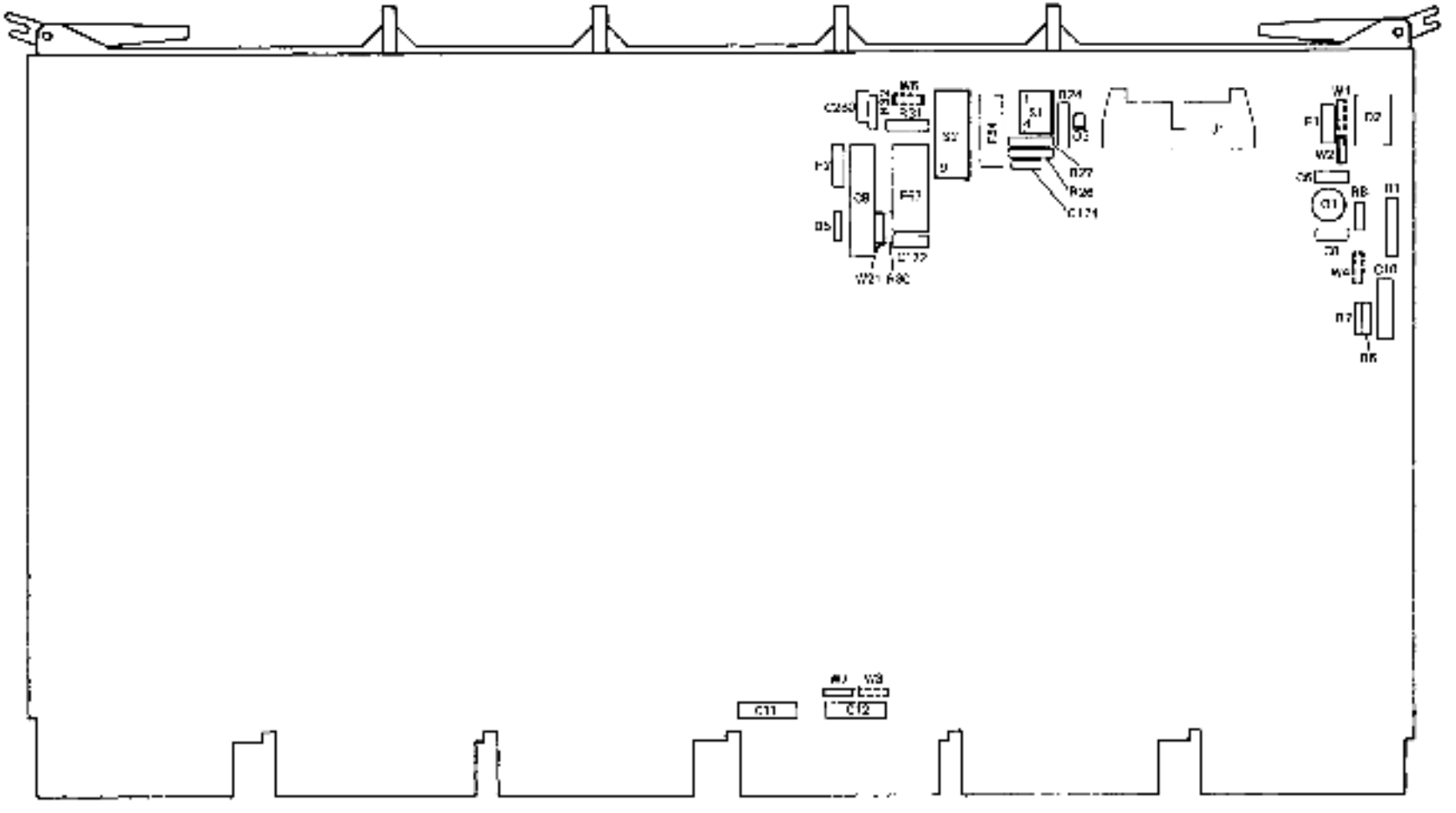
2.2.1.1 Memory Addressing

PDP-11 Memory Conventions – The MS11-L can be used with the PDP-11 Unibus or special buses with reserve addressing capability. Memory in these computer systems is organized into 16-bit data words, each containing two 8-bit bytes. These bytes are identified as low or high, as shown below.



Each byte is addressable and has its own address location; low bytes are even-numbered and high bytes are odd-numbered. Words are addressed by even numbered locations only, and the high (odd) byte for each word is automatically included.

Via the Unibus, 131,072 (128K) words or 262,144 (256K) bytes can be addressed; 2,097,152 (2048K) words or 4,194,034 (4096K) bytes can be addressed via a special bus. Each byte location in Unibus memory is specified by a 6-digit octal number, but with a special bus, 8-digit octal numbers are used. The address range is 000000 through 777777 on the Unibus and 00000000 through 17777777 on a special bus (Figure 2 through 2).



NOTES
1. JUMPERS W10 - W19 AND W20 ARE NOT SHOWN SINCE THEY SHOULD NOT BE TAMPERED WITH IN THE FIELD.

2. THE JUMPERS SHOWN ARE ZERO OHM RESISTORS
   - ▭ JUMPER IN
   - CT JUMPER OUT

   THE JUMPER CONFIGURATION IN THE FIGURE IS THE MOST COMMON

Figure 2-1 Switch and Jumper Locations

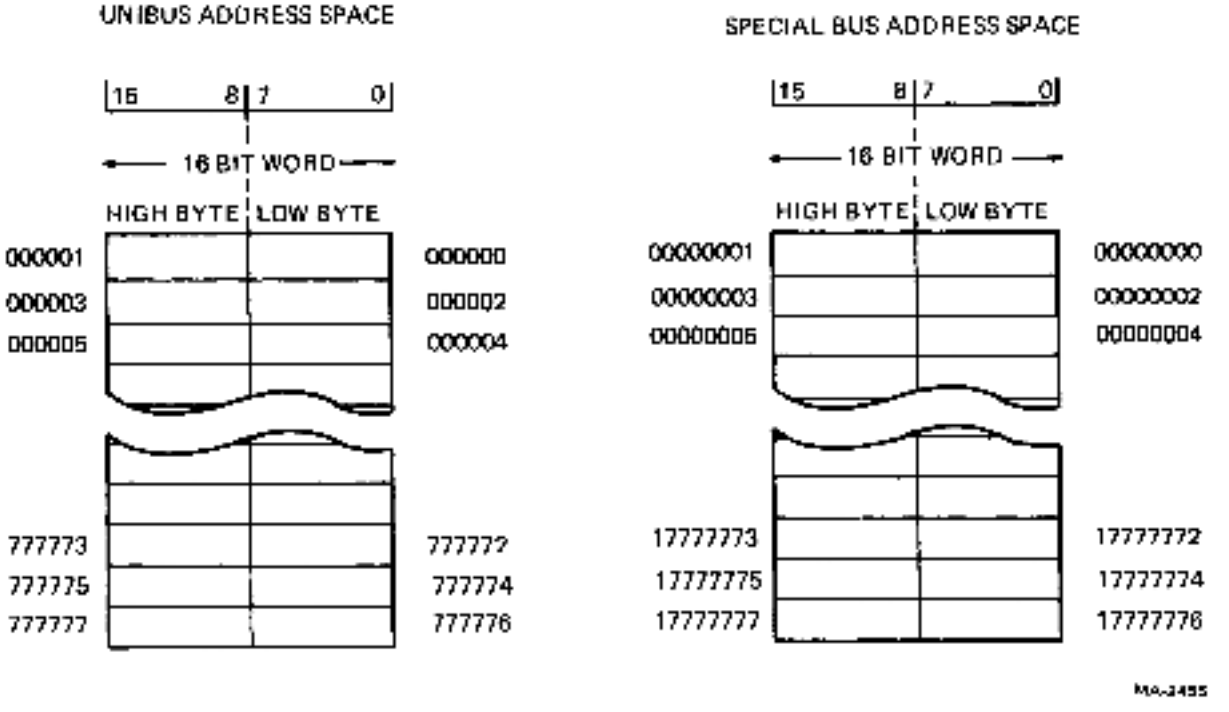


Figure 2-2 Bus Accessible Data Locations

The memory address decoding logic responds to the binary equivalent of the octal address. The binary equivalent of 00017772 is shown below. The MS11-L decodes an 18-bit address (A17–A00) on the Unibus or a 22-bit address (A21–A00) on a special bus.

The address space on a bus occupied by a memory module is determined by the memory starting address and address range. A unique starting address is selected by switches on the MS11-L which correspond to address bits A17–A13 on the Unibus or A21–A13 on a special bus. Table 2-1 lists the octal address ranges of the MS11-L versions and the associated address bits which determine the word location within the module. Address bit A00 is used to select a data byte during a DATOB bus cycle.

Table 2-1 MS11-L Address Ranges

Memory Designation	Storage Capacity	Octal Address Range	Associated Address Bits
MS11-LA	32,768 words (65,536 bytes)	00000000–00177777	A15–A00
MS11-LB	65,536 words (131,072 bytes)	00000000–00377777	A16–A00
MS11-LC	98,304 words (196,608 bytes)	00000000–00577777	A17–A00
MS11-LD	131,072 words (262,144 bytes)	00000000–00777777	A17–A00

Memory Starting Address Selection - The lowest bus address which the MS11-L responds to is the memory starting address. The starting address must be assigned to a 4K boundary within the 128K Unibus address space or 2048K special bus address space. The starting address is assigned by manually setting nine switches, S2-1 through S2-9, to the appropriate positions for the desired location (Tables 2-2 and 2-3).

Table 2-2 Starting Address Configurations (Part 1)

Partial Starting Address		Switch Positions			
Decimal	Octal	S2-1 (A21)	S2-2 (A20)	S2-3 (A19)	S2-4 (A18)
0K	00RR0000	ON	ON	ON	ON
128K	01RR0000	ON	ON	ON	OFF
256K	02RR0000	ON	ON	OFF	ON
384K	03RR0000	ON	ON	OFF	OFF
512K	04RR0000	ON	OFF	ON	ON
640K	05RR0000	ON	OFF	ON	OFF
768K	06RR0000	ON	OFF	OFF	ON
896K	07RR0000	ON	OFF	OFF	OFF
1024K	10RR0000	OFF	ON	ON	ON
1152K	11RR0000	OFF	ON	ON	OFF
1280K	12RR0000	OFF	ON	OFF	ON
1408K	13RR0000	OFF	ON	OFF	OFF
1536K	14RR0000	OFF	OFF	ON	ON
1664K	15RR0000	OFF	OFF	ON	OFF
1792K	16RR0000	OFF	OFF	OFF	ON
1920K	17RR0000	OFF	OFF	OFF	OFF

NOTES

1. **RR = octal digits determined by switches S2-5 to S2-9**
2. **The decimal addresses listed are equivalent to the associated octal addresses if RR = 00**

Table 2-3 Starting Address Configurations (Part 2)

Partial Starting Address		Switch Positions				
Decimal	Octal	S2-5 (A17)	S2-6 (A16)	S2-7 (A15)	S2-8 (A14)	S2-9 (A13)
0K	SS000000	ON	ON	ON	ON	ON
4K	SS020000	ON	ON	ON	ON	OFF
8K	SS040000	ON	ON	ON	OFF	ON
12K	SS060000	ON	ON	ON	OFF	OFF
16K	SS100000	ON	ON	OFF	ON	ON
20K	SS120000	ON	ON	OFF	ON	OFF
24K	SS140000	ON	ON	OFF	OFF	ON
28K	SS160000	ON	ON	OFF	OFF	OFF
32K	SS200000	ON	OFF	ON	ON	ON
36K	SS220000	ON	OFF	ON	ON	OFF
40K	SS240000	ON	OFF	ON	OFF	ON
44K	SS260000	ON	OFF	ON	OFF	OFF
48K	SS300000	ON	OFF	OFF	ON	ON
52K	SS320000	ON	OFF	OFF	ON	OFF
56K	SS340000	ON	OFF	OFF	OFF	ON
60K	SS360000	ON	OFF	OFF	OFF	OFF
64K	SS400000	OFF	ON	ON	ON	ON
68K	SS420000	OFF	ON	ON	ON	OFF
72K	SS440000	OFF	ON	ON	OFF	ON
76K	SS460000	OFF	ON	ON	OFF	OFF
80K	SS500000	OFF	ON	OFF	ON	ON
84K	SS520000	OFF	ON	OFF	ON	OFF
88K	SS540000	OFF	ON	OFF	OFF	ON
92K	SS560000	OFF	ON	OFF	OFF	OFF
96K	SS600000	OFF	OFF	ON	ON	ON
100K	SS620000	OFF	OFF	ON	ON	OFF
104K	SS640000	OFF	OFF	ON	OFF	ON
108K	SS660000	OFF	OFF	ON	OFF	OFF
112K	SS700000	OFF	OFF	OFF	ON	ON
116K	SS720000	OFF	OFF	OFF	ON	OFF
120K	SS740000	OFF	OFF	OFF	OFF	ON
124K	SS760000	OFF	OFF	OFF	OFF	OFF

NOTES

1. **SS = octal digits determined by switches S2-1 to S2-4**

2. **The decimal addresses listed are equivalent to the associated octal addresses if SS = 00**

Switches S2-1 through S2-9 correspond to address bits A21–A13 respectively on a special bus; a switch in the OFF position corresponds to a logical 1. The positions of S2-1 through S2-4 specify the starting address to a 128K range: S2-5 to S2-9 specify the starting address to a 4K boundary within a 128K range.

NOTE

Switches S2-1 to S2-4 should be set to the ON position if the MS11-L is used with the PDP-11 Unibus.

Unibus or special bus operation of the MS11-L is selected by jumper W4:

W4 OUT – Unibus operation
W4 IN – Special bus operation

2.2.1.2 I/O Peripheral Page Size Selection – The I/O peripheral page is the address space reserved for CPU and peripheral registers. The MS11-L allows the top 2K, 4K or 8K of the Unibus or special bus address space to be reserved for the I/O peripheral page. The peripheral page size is specified by jumpers W5 and W21 as shown in Table 2-4.

Table 2-4 Peripheral Page Size Selection

Peripheral Page Size	Unibus Location	Special Bus Location	Jumpers	
			W5	W21
2K	126K–128K	2046K–2048K	IN	IN
4K	124K–128K	2044K–2048K	OUT	IN
8K	120K–128K	2040K–2048K	OUT	OUT

NOTES

1. **The remaining jumper configuration, W5 IN and W21 OUT, should never be used since it results in a peripheral page which is not continuous.**

2. **Memory diagnostics are not compatible with a 2K or 8K peripheral page (Paragraph 2.2.4).**

2.2.1.3 CSR Address Selection The control and status register (CSR) can be read or written into via the Unibus or special bus, even during a memory refresh cycle. Address decoding logic in the MS11-L specifies the CSR address in the range of 772100–772136 for Unibus operation or 17772100–17772136 for special bus operation. Four switches, S1-1 through S1-4, are used to select the exact CSR address (Table 2-5). Switches S1-1 through S1-4 correspond to address bits A04–A01 respectively; a switch in the OFF position corresponds to a logical 1. The CSR is always accessed as an entire data word since bit A00 is not decoded by the CSR address logic. The Unibus or special bus address of the CSR is in the top 2K of the available address space.

NOTE

The CSR address has no relevance to the memory starting address or storage capacity of the MS11-L.

Table 2-5 CSR Address Selection

Unibus Address	Special Bus Address	Switch Positions			
		S1-1 (A04)	S1-2 (A03)	S1-3 (A02)	S1-4 (A01)
772100	17772100	ON	ON	ON	ON
772102	17772102	ON	ON	ON	OFF
772104	17772104	ON	ON	OFF	ON
772106	17772106	ON	ON	OFF	OFF
772110	17772110	ON	OFF	ON	ON
772112	17772112	ON	OFF	ON	OFF
772114	17772114	ON	OFF	OFF	ON
722116	17772116	ON	OFF	OFF	OFF
772120	17772120	OFF	ON	ON	ON
772122	17772122	OFF	ON	ON	OFF
772124	17772124	OFF	ON	OFF	ON
772126	17772126	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF

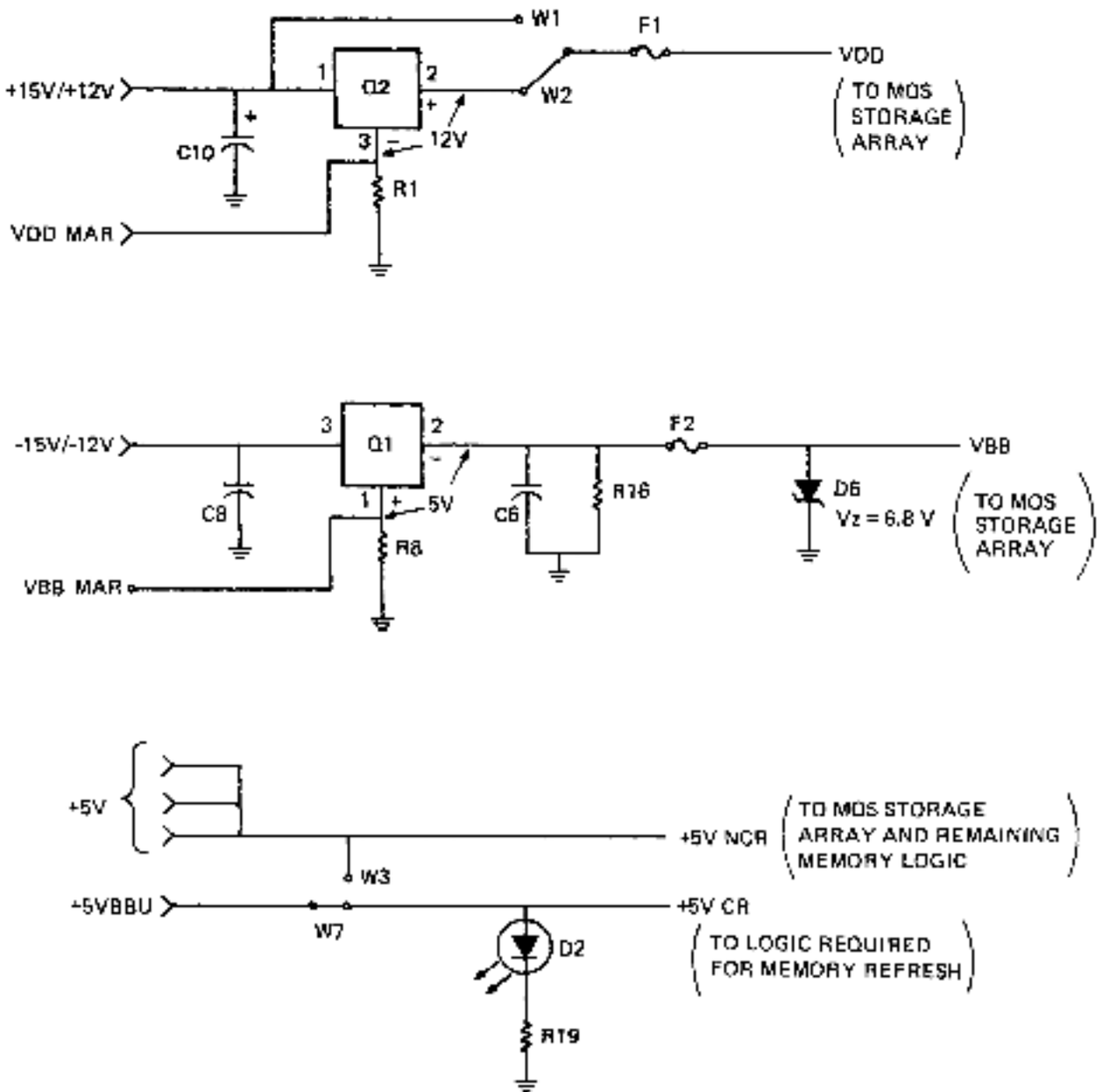
2.2.1.4 Power Voltages - The MS11-L uses +5 V and either ±15 V or ±12 V power. Jumpers W1 and W2 are used as listed below to specify ±15 V or ±12 V operation.

Power Voltage	Jumpers	
	W1	W2
±15 V	OUT	IN
+12 V	IN	OUT

The circuit shown in Figure 2-3 yields +12 V and -5 V which are designated VDD and VBB respectively and are routed to the MOS storage array. The major components of the circuit are Q1 and Q2 which are three-terminal voltage regulators. Regulator Q2 produces +12 V from a +15 V module input and Q1 produces -5 V from a -15 V or -12 V module input. In normal operation, voltage drops across R1 and R8 are negligible. Fuses F1 and F2 provide current overload protection and zener diode D5 provides overvoltage protection. If an overvoltage condition occurs, D5 conducts so that VBB is clamped to -6.8 V. Note that if the module operates with ±12 V inputs, the output of Q2 is not used but current flows from the module input via W1. The ±15 V/±12 V module inputs are battery supported during an ac power failure if a battery backup unit is present.

The module has inputs for two sources of +5 V power, designated +5 VBBU and +5 V. Jumpers W3 and W7 are associated with the +5 VBBU and +5 V inputs and are configured as follows.

Power Voltages	Jumpers		Comments
	W3	W7	
+5 V and +5 VBBU	OUT	IN	Normal configuration
+5 V only	IN	OUT	Used if power is available at the +5 V input only.



NOTES:

1. AS SHOWN, W1 AND W2 INDICATE ±15V OPERATION AND W3 AND W7 INDICATE MODULE USAGE OF +5V AND +5VBBU. JUMPERS W3 AND W7 SHARE A HOLE ON THE MODULE SO THAT BOTH JUMPERS CAN NOT BE IN AT THE SAME TIME.

2. INPUTS VDD MAR AND VBB MAR ARE USED AT THE FACTORY TO MARGIN THE MEMORY (IN ±15V OPERATION ONLY).

MA 2456

Figure 2-3 Power Voltages

With W3 OUT and W7 IN, power is routed from the +5 VBBU input to the logic required for memory refresh; power from the +5 V input is routed to the MOS storage array and the remaining memory logic. The +5 VBBU input is battery supported during an ac power failure if a battery backup unit is present. In the battery support mode, power is used only to refresh the MOS storage array so that battery backup time and therefore data retention time are maximized. (The MOS storage devices do not require +5 V power during a refresh cycle.) Note that in most systems, power is supplied to the +5 V and +5 VBBU inputs even if the battery backup unit is not used. With W3 IN and W7 OUT, the power distribution lines on the module for +5 V and +5 VBBU are jumpered together and the +5 VBBU module input is disconnected.

A green LED (D2) stays on as long as the logic required for refresh receives power from either the +5 V or +5 VBBU input. The MS11-L should not be extracted from the backplane when the green LED is ON, even in battery support mode.

2.2.2 Backplane Placement (Unibus Operation Only)

The MS11-L should be inserted into any slot in a backplane which contains modified Unibus connectors in sections A and B. For example:

DD11-PK	Slots 3–8
DD11-DK	Slots 2–8
DD11-CK	Slots 2 and 3.

The MS11-L is compatible with all modified Unibus parity or non-parity memories. The MS11-L does not require an M7850 Parity Controller; however, an M7850 is required for other parity memories that may be in the same backplane. The presence of the M7850 does not affect the MS11-L. The backplane connections used by the MS11-L are listed in Table 2-6.

2.2.3 Power Voltage Check

Once primary power has been turned on, the dc power voltages listed below should be checked at the backplane.

Voltage and Tolerance	Backplane Pin(s)
+5 V +5%, max ripple = 0.2 V p-p	AA2, BA2, CA2
+5 VBBU +5%, max ripple = 0.2 V p-p (only if jumper W7 is IN and W3 is OUT on the module)	BD1
+15 V +10%, -3.3% or +12 V +5%, max ripple = 1 V p-p	AR1
-15 V ±10% or -12 V +10%, max ripple = 1 V p-p	AS1

2.2.4 MAINDEC Testing

The following diagnostic program should be used with the MS11-L: 0-128K Memory and Memory Parity Exerciser (MAINDEC-11-CZQMC). To verify proper operation of the memory, run two passes of the diagnostic. No errors are permitted. Also, verify that the program printout agrees with the total memory in the system.

Table 2-6 MS11-L Pin Out

	A		B		C		D		E		F	
	1	2	1	2	1	2	1	2	1	2	1	2
A	INIT L	+ 5 V	–	+ 5 V	NPG IN H	+ 5 V	–	–				
B				–	NPG OUT H	–	–	GND	–	GND		GND
C	D00 L	GND	–	GND	–	GND	–	–	–	–	–	–
D	D02 L	D01 L	+ 5 V Battery	–	–	–	–	–	–	–	–	
E	D04 L	D03 L	A19 L	A18 L	–		–	–	–	–		
F	D06 L	D05 L	–	DC LO L	VDD MAR	–		–	–	–		
H	D08 L	D07 L	A01 L	A00 L	–			–	–	–		
J	D10 L	D09 L	A03 L	A02 L	–			BUS G7 SO H	–	–		
K	D12 L	D11 L	A05 L	A04 L	–		–	BUS G7 OUT H	–			
L	D14 L	D13 L	A07 L	A06 L				BUS G5 SO H		–	–	–
M	–	D15 L	A09 L	A08 L		–		BUS G6 OUT H	–	–	–	–
N	A21 L	PB L	A11 L	A10 L		–	–	BUS G5 SO H			–	–
P	A20 L		A13 L	A12 L	–			BUS G5 OUT H	–			
R	– 15 V / 12 V Battery	–	A15 L	A14 L	–	–	–	BUS G4 SO H			–	–
S	– 15 V / 12 V Battery		A17 L	A16 L	–		GND	BUS G4 OUT H	GND	–	GND	–
T	GND		GND	CTL	GND				–	–		
U	–	–	SSYN L	C0 L	–	–			–	–	–	
V	–	–	MSYN L		–	–						

NOTES

1. Pins AN1, AP1, BE1 and BE2 are used for address lines A21 L - A18 L in special bus operation. In Unibus operation, the signals on these pins are ignored by the MS11-L (receivers disabled). In Unibus operation, AN1, AP1, BE1 and BE2 contain the internal bus used by the M7850 Parity Controller.

2. Pins marked by] are tied together on the module to provide grant continuity.

NOTE
MAINDEC-11-CZQMC diagnostic is compatible with a 4K I/O peripheral page only (Paragraph 2.2.1.2).

2.3 CSR BIT ASSIGNMENTS

The control and status register (CSR) in the MS11-L allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The CSR is assigned an address and can be accessed by a bus master via the Unibus or a special bus, even during a memory refresh cycle. Some CSR bits are cleared by the assertion of BUS INIT L. This signal is asserted for a short time by the processor after system power has come up or in response to a reset instruction. The CSR bit assignments are illustrated in Figure 2-4 and are described as follows:

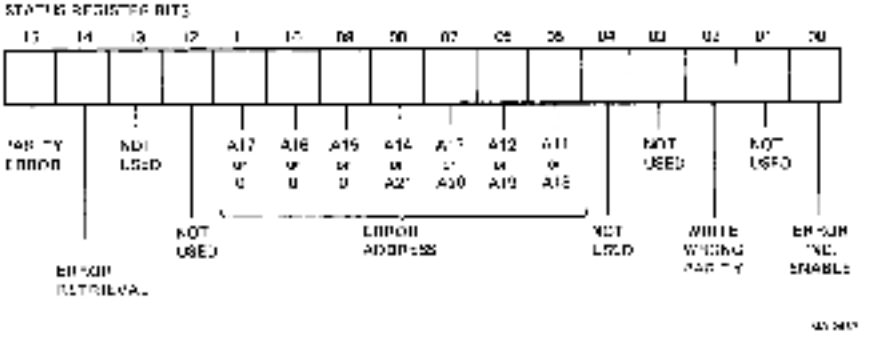


Figure 2-4 CSR Bit Assignments

Bits 1, 3, 4, 12, and 13 — These bits are not used and are always read as logical 0s. Writing into these bits has no effect on the CSR.

Bit 0 — Error Indication Enable - This bit, when set (logical 1), allows the MS11-L to assert BUS PB L when data is retrieved from memory if a parity error has been detected. This bit can be read or loaded by the program (read/write bit) and is cleared by BUS INIT L.

Bit 2 — Write Wrong Parity – This bit, when set, causes the MS11-L to generate the wrong (incorrect) parity when data is written into memory during a DATO or DATOB bus cycle. A parity error should then be detected when this data is read during a DATI or DATIP bus cycle. The bit is usually set for diagnostic purposes and should be cleared (logical 0) for normal operation (correct parity generated). Bit 2 is a read/write bit and is cleared by BUS INIT L.

Bits 05-11 — Error Address – Once a parity error has occurred, these bits contain a partial address of the faulty data which caused the parity error. In Unibus operation, address bits A17–A11 are in CSR bits 11–05 respectively, specifying the faulty data location to a 1K segment of memory. In special bus operation, the address bits placed in bits 05–11 are determined by bit 14. Bits 05–11 are read/write bits and are not cleared by BUS INIT L.

Bit 14

Special Bus Error Retrieval – This bit, when set, causes the MS11-L to place A21–A18 of the faulty data location into CSR bits 08–05; logical 0s are placed in bits 11–09. Address bits A17 A11 are placed in bits 11–05 when bit 14 is cleared. In special bus operation, bit 14 is a read/write bit and is cleared by BUS INIT L. In Unibus operation bit 14 is a read-only bit and is always a logical 0 (clear).

NOTE

In normal special bus operation, bit 14 should be a logical 0. If a parity error has occurred, the partial address (A21-A11) of the faulty data can be retrieved using the following sequence.

1. **Read the CSR with a DATI bus cycle to obtain A17–A11. Bit 14 should be read as a logical 0.**

2. **Write a logical 1 in bit 14 of the CSR with a DATO bus cycle.**

3. **Read the CSR with a DATI bus cycle to obtain A21–A18. But 14 should be read as a logical 1.**

Bit 15

Parity Error Bit - This bit, when set, indicates that a parity error has occurred and also turns on a red LED on the module, providing a visual indication of a parity error. Bit 15 is a flag, but it does not cause a parity error trap in the processor. This bit is a read/write bit and is cleared by BUS INIT L.

CHAPTER 3
THEORY OF OPERATION

3.1 GENERAL

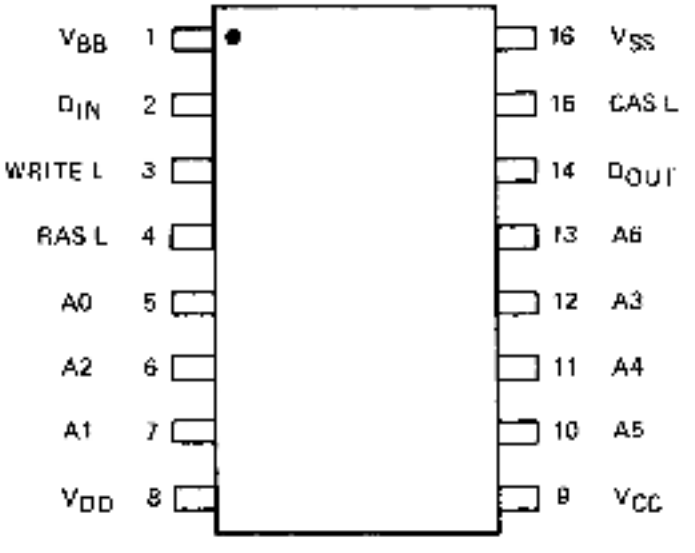
This chapter contains functional and detailed descriptions of the circuitry in the MS11-L. The descriptions in this chapter are supported by the MS11-L Field Maintenance Print Set (MP00672).

3.2 MOS STORAGE ARRAY

3.2.1 16K MOS RAM Chip Description

The MOS storage device used in the MS11-L is a 16384 × 1-bit, dynamic, random-access-memory circuit. The circuit is packaged in a standard 16-pin DIP (Figure 3-1). Timing diagrams for the read cycle and write cycle are shown in Figures 3-2 and 3-3.

To specify a data location within the chip, 14 address bits are required. The 14 address bits are multiplexed, seven at a time, onto the A6 -A0 inputs and are latched into on-chip address registers by two signals. The first seven bits comprise the row address and are latched by asserting the RAS L (Row Address Strobe) signal. The other seven bits make up the column address and are latched by asserting the CAS L (Column Address Strobe) signal. The internal timing chain of the chip is started at the negative transition of RAS L.



CHIP SUPPLY VOLTAGES

VOLTAGE	OPERATION
VDD	+ 12 Vdc
VCC	+ 5 Vdc
VSS	Ground
VBB	5 V

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Figure 3-1 16K MOS RAM Chip

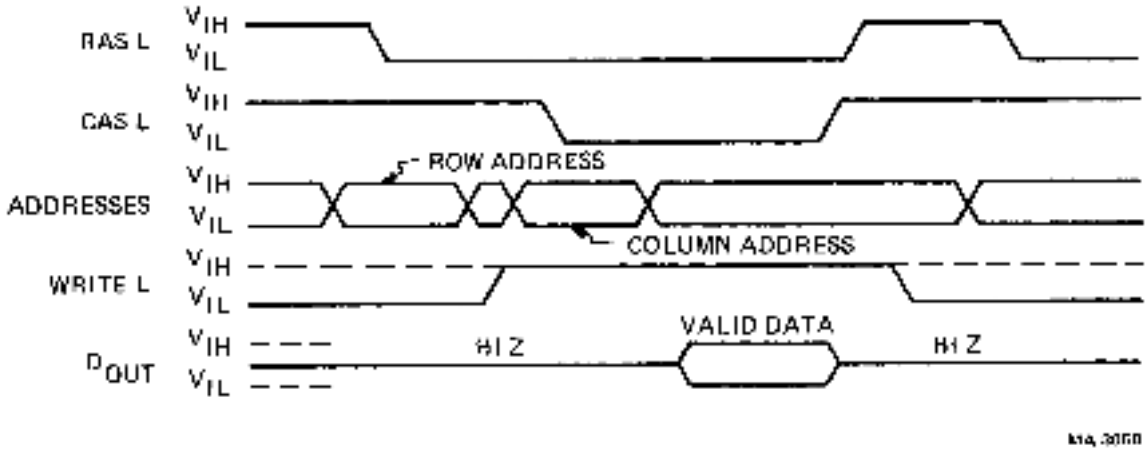


Figure 3-2 Chip Read Timing

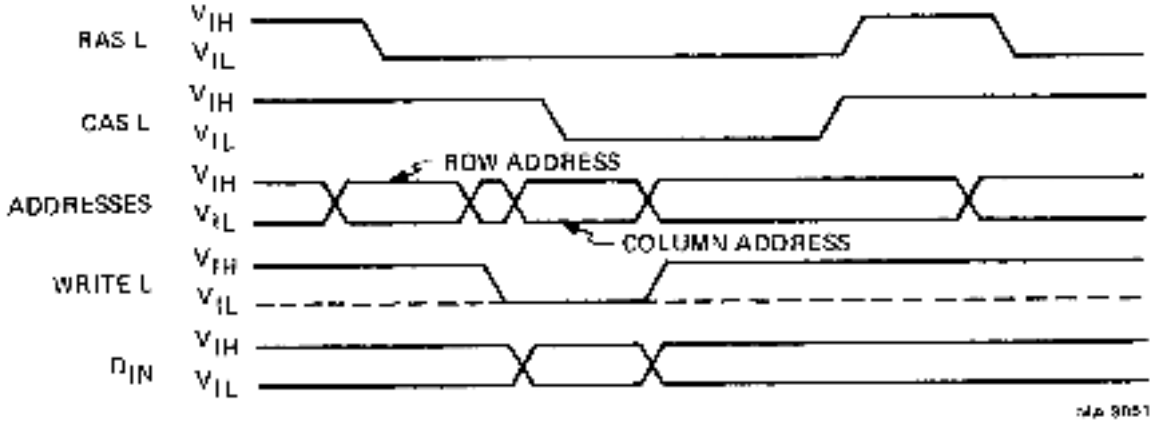


Figure 3-3 Chip Write Timing

For a read cycle, the WRITE L signal must be high during the entire time that CAS L is asserted. The data is available on the D OUT line at access time (135 ns max. after CAS L is asserted) and remains valid until CAS L is negated. The D OUT line is driven by a tristate buffer and is in a high impedance (open circuit) state when a valid data output is not present.

A write cycle is specified if the WRITE L signal goes low before CAS L is asserted. The data on the D IN line is strobed into an input buffer by the negative transition of the CAS L signal. Since the D OUT line remains in the high impedance state during a write cycle, the D IN and D OUT lines can be tied together to form a common input/output bus.

The MOS chips must be periodically refreshed so that data remains valid. The data in locations specified by the row address is refreshed during a read or write cycle. Since a data location may be addressed infrequently, if at all, during normal read/write operations, a RAS only refresh cycle is initiated by the MS11-L approximately every 14.5 μs. A different row address is supplied by the MS11-L during each refresh cycle so that data in all 128 row addresses is refreshed in less than 2 ms. The chip does not require a VCC input (+5 V) during a refresh cycle.

3.2.2 Storage Array Organization

The storage array in the MS11-L contains up to 144 16K MOS RAM chips, providing storage for up to 128K 18-bit words (2 data bytes and 2 parity bits). The number of chips in the array is different for each version of the MS11-L. The storage array for a 128K memory is shown in sheets 11 14 of the print set. Each sheet shows 32K of memory.

A bank of 18 chips is allocated to each 16K bank of memory; e.g., a 128K memory contains 8 chips for each data and parity bit (Tables 3-1 and 3-2). Parity for the high and low data bytes is written into the array via PDI17 H and PDI16 H. The two parity bits are retrieved via PDO17 H and PDO16 H. Data is written into and retrieved from the storage array via the DAT<15:00> H lines. The D OUT and D IN lines are tied together for chips that store data.

Table 3-1 Data Storage in Array

Memory Bank	Data Storage Chips		Associated Chip Input Lines				
	High Byte (Bits 15–08)	Low Byte (Bits 07–00)	A6–A0 Lines	CAS L Lines	RAS L Lines	Write L Lines	
						High Byte	Low Byte
0 16K	E87 E94	E95 E102	AA<7–1>L	CAS 0 L	RAS 0 L	WTBT 2 L	WTBT 0 L
16–32K	E103–E110	E111–E118	AA<7–1> L	CAS 1 L	RAS 1 L	WTBT 2 L	WTBT 0 L
32–48K	E120–E127	E128–E135	BA<7–1> L	CAS 2 L	RAS 2 L	WTBT 2 L	WTBT 0 L
48–64K	E137–E144	E145–E152	BA<7–1> L	CAS 3 L	RAS 3 L	WTBT 2 L	WTBT 0 L
64–80K	E153–E160	E161–E168	CA<7–1> L	CAS 4 L	RAS 4 L	WTBT 3 L	WTBT 1 L
80–96K	E170–E177	E178–E185	CA<7–1> L	CAS 5 L	RAS 5 L	WTBT 3 L	WTBT 1 L
96–112K	E187–E194	E195–E202	DA<7–1> L	CAS 6 L	RAS 6 L	WTBT 3 L	WTBT 1 L
112–128K	E204 E211	E212 E219	DA<7 1> L	CAS 7 L	RAS 7 L	WTBT 3 L	WTBT 1 L

Table 3-2 Parity Storage In Array

Memory Bank	Parity Storage Chips		Associated Chip Input Lines				
	High Byte (bit 17)	Low Byte (bit 16)	A6-A0 Lines	CAS L Lines	RAS L Lines	Write L Lines	
						High Byte	Low Byte
0–16K	E77	E85	PA<7–1>L	PCAS 0 L	PRAS 0 L	WTBT 2 L	WTBT 0 L
16–32K	E76	E84	PA<7–1>L	PCAS 0 L	PRAS 1 L	WTBT 2 L	WTBT 0 L
32–48K	E75	E83	PA<7–1>L	PCAS 0 L	PRAS 2 L	WTBT 2 L	WTBT 0 L
48–64K	E74	E82	PA<7–1>L	PCAS 0 L	PRAS 3 L	WTBT 2 L	WTBT 0 L
64–80K	E73	E81	PA<7–1>L	PCAS 0 L	PRAS 4 L	WTBT 2 L	WTBT 0 L
80–96K	E72	E80	PA<7–1>L	PCAS 0 L	PRAS 5 L	WTBT 2 L	WTBT 0 L
96–112K	E71	E79	PA<7–1>L	PCAS 0 L	PRAS 6 L	WTBT 2 L	WTBT 0 L
112–128K	E70	E78	PA<7–1>L	PCAS 0 L	PRAS 7 L	WTBT 2 L	WTBT 0 L

The remaining input signals required by the chips are generated by the MS11-L logic. These signals are distributed to the array via a number of inverting line drivers, due to fanout considerations. The number of drivers is different for each version of the MS11-L. Sheets 9 and 10 in the print set show the 64 drivers used in a 128K memory. The signal distribution to the 128K array is summarized below.

1. The multiplexed row address and column address signals are routed to all the chips in the array by five groups of seven lines.
2. One Column Address Strobe is routed to all the chips in the array by nine lines.
3. One Row Address Strobe is routed to each 18-chip bank by two lines.
4. One write byte signal is routed by two lines to the 72 chips which correspond to each byte (data and parity).

During a memory data cycle, the 18-chip bank which contains the desired word location is enabled by asserting the appropriate Row Address Strobe. Chips that do not receive an asserted RAS L signal, do not cycle internally, remaining in a low-power (standby) state.

3.3 FUNCTIONAL DESCRIPTION

A block diagram of the MS11-L is shown in Figure 3-4. The memory is compatible with the PDP-11 Unibus or special buses that have 22 address bits. Unibus or special bus operation is specified by a jumper on the module. Data cycles are initiated by the bus master; refresh cycles are initiated within the memory.

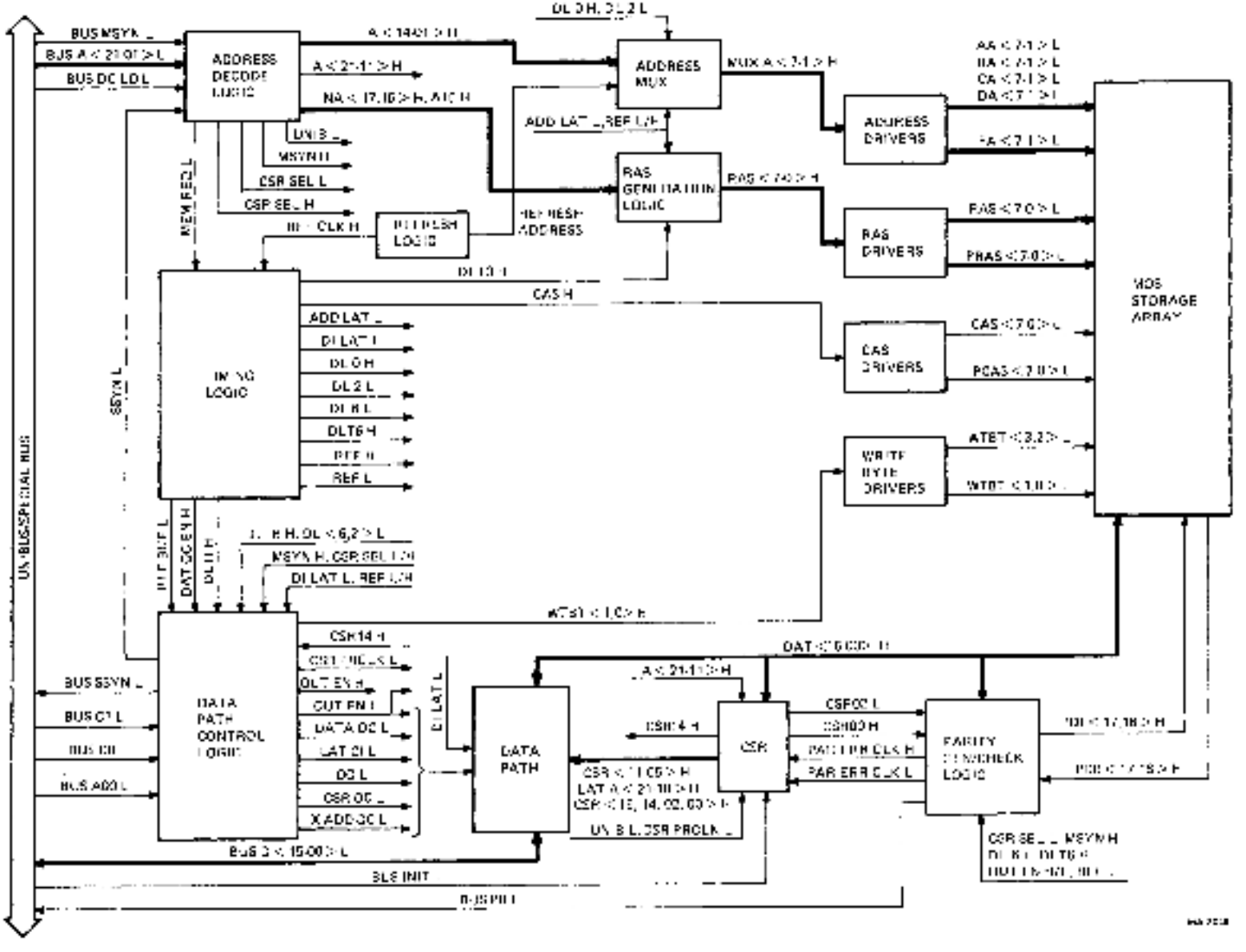


Figure 3-4 MS11-L Block Diagram

The address decode logic determines if an address on the bus is assigned to the CSR or MOS storage array in the MS11-L. The address decode logic also checks BUS DC LO L (generated by the computer power supply) and SSYN L. Access to the MOS storage array is prevented if BUS DC LO L or SSYN L is asserted or if the bus address is within the I/O peripheral page. Access to the CSR is prevented if BUS DC LO L is asserted. If Unibus operation is specified, the logic associated with address bits A21 A18 is disabled. Therefore, the assigned CSR address and address space reserved for the I/O peripheral page are automatically in the Unibus address space.

With BUS MSYN L asserted, the address decode logic enables bus master access to the storage array by asserting MEM REQ L. The timing logic then intitiates a memory data cycle if the memory is not busy. Timing signals and address information are used by the address mux and RAS generation logic to provide the row address, column address and Row Address Strobe to the array. The Column Address Strobe is provided by the timing logic. Address bits A17 and A16 may have been modified by the address decode logic to provide NA17 and NA16. These two lines and A15–A01 are latched in and specify the data location in a 128K MOS storage array as follows:

NA17,NA16,A15		Select 1 of 8 RAS signals to be asserted which in turn enables the 18-chip bank that contains the desired data location
A14–A08	Column address	Collectively select the desired word location within the enabled 18-chip bank.
A07–A01	Row address	

Control signals on the bus (C0 and C1) specify the type of data transfer (DATI, DATIP, DATO or DATOB). If a DATOB cycle is specified, address bit A00 selects the byte to be written. The data path control logic uses bus signals C0, C1 and A00 in conjunction with address decode and timing signals to control the flow of data on the module. Signals BUS SSYN L and SSYN L are also controlled by the data path control logic.

For a memory data cycle, C0, C1 and A00 are latched-in. If a memory write cycle (DATO or DATOB) is specified, data from the bus is channeled to the DAT<15:00>H lines and latched. Two parity bits are generated based on the data (one parity bit for each data byte). The appropriate data byte(s) and parity bit(s) are then written into the desired location of the MOS storage array. If a memory read cycle (DATI or DATIP) is specified, the two data bytes and parity bits are retrieved from the desired location in the storage array. The parity of the data is recalculated and compared to the retrieved parity. The data is then placed on the bus and if a parity error is detected, the parity gen/check logic initiates the following steps:

1. The parity error bit (bit 15) in the CSR is set to a logical 1.
2. A red LED on the module turns on, providing a visual indication of a parity error.
3. If bit 0 in the CSR is set, signal BUS PB L is asserted warning the CPU that a parity error has occurred.
4. A partial address of the faulty data is stored in the CSR.

The write byte signals specify a read or write operation for the MOS chips in the array that are associated with each byte. The specified operation is carried out by the 18-chip bank for which the Row Address Strobe and Column Address Strobe are asserted. A DATIP bus cycle involving memory data is executed in the same manner as a DATI cycle.

The control and status register (CSR) allows program control of certain parity functions and contains diagnostic information if a parity error has occurred. The address decode logic enables bus master access to the CSR by asserting CSR SEL H, CSR SEL L and then MSYN H. The timing logic is not activated for a data transfer involving the CSR. Therefore, the CSR can be accessed during a refresh cycle. If bus signals C0 and C1 specify a write cycle (DATO or DATOB), data from the bus is channeled to the DAT<15-00> H lines and clocked into the CSR. A DATOB bus cycle is executed as a DATO cycle. If a read cycle (DATI or DATIP) is specified, information from the CSR is channeled via the data path circuit to the bus. The information placed on the bus for bits 11-05 is determined by the data path control logic in accordance with CSR bit 14. Error address information (A17-A11) or data previously written into the CSR is retrieved if CSR bit 14 is cleared. Error address bits A21-A18 are retrieved if bit 14 is set. For special bus operation, CSR bit 14 is a read/write bit but for Unibus operation it is a read-only bit which is always cleared. A DATIP bus cycle is executed as a DATI cycle.

All MOS chips in the storage array are periodically refreshed by a specially-timed, RAS-only, refresh cycle. An oscillator in the refresh logic is used to activate the timing logic for a refresh cycle every 14.5 μ s if the memory is not busy. In accordance with the timing signals, the address mux channels the refresh address to the array, and the RAS generation logic asserts all eight Row Address Strobes. For each chip in the array, the refresh address is interpreted as a row address specifying 128 data cells that are refreshed in a cycle. After each refresh cycle, the address is incremented by one. Therefore, a different address is used during each successive refresh cycle so that all 128 row addresses are refreshed in less than 2 ms. Note that the Column Address Strobe and write byte signals are inhibited.

3.4 TIMING LOGIC

The timing logic, shown in Figure 3-5, generates a sequence of signals that causes the execution of a memory data cycle or refresh cycle. To initiate a memory data cycle, the address decode logic must assert MEM REQ L. To initiate a refresh cycle, REF REQ L must be asserted by clocking a logical 1 into E6-B at the leading (rising) edge of REF CLK H. The timing logic is not used to execute a data cycle involving the CSR.

With BUSY L negated, the assertion of MEM REQ L or REF REQ L causes E23 pin 3 to go high. Capacitor C4 discharges, DL 0 H is asserted triggering the timing chain, and BUSY L is asserted. Signal BUSY L remains asserted until the end of the cycle and therefore, the start of another cycle is prevented until the present cycle is completed. Memory data cycles and refresh cycles are executed on a first-come/first-serve basis.

For a refresh cycle, a logical 1 is clocked into E6-A at the leading (rising) edge of E23 pin 3; a logical 0 is clocked into E6-A for a memory data cycle. Therefore, REF H, REF L, REF BUF H and REF BUF L are asserted for a refresh cycle only. Note that E6-A is cleared at a later time in a refresh cycle and therefore, E6-A always contains a logical 0 at the end of a cycle.

The triggering of the timing chain is delayed from the beginning of a cycle but the delay is longer for a refresh cycle than for a memory data cycle. For a refresh cycle, the Q output of E6-B inhibits E7 pin 6 from going low, when E7 pin 8 goes low. Capacitor C4 discharges through a higher resistance (R7 as opposed to R7/R10) so the discharge time is longer. Therefore, the triggering of the timing chain is delayed an extra 50-60 ns for a refresh cycle.

The timing chain is generated by a 200 ns delay line (E18). The timing chain is triggered by the leading (rising) edge of DL 0 H which is applied to the input of E18. The positive-edged signal travels down the delay line, appearing at the taps along the way. Feedback derived from the DL 10 H tap is used to truncate DL 0 H, resulting in a 230 ns pulse width. Therefore, a positive pulse, 230 ns wide, appears at each delay line tap with the taps spaced at 20 ns intervals along the line.

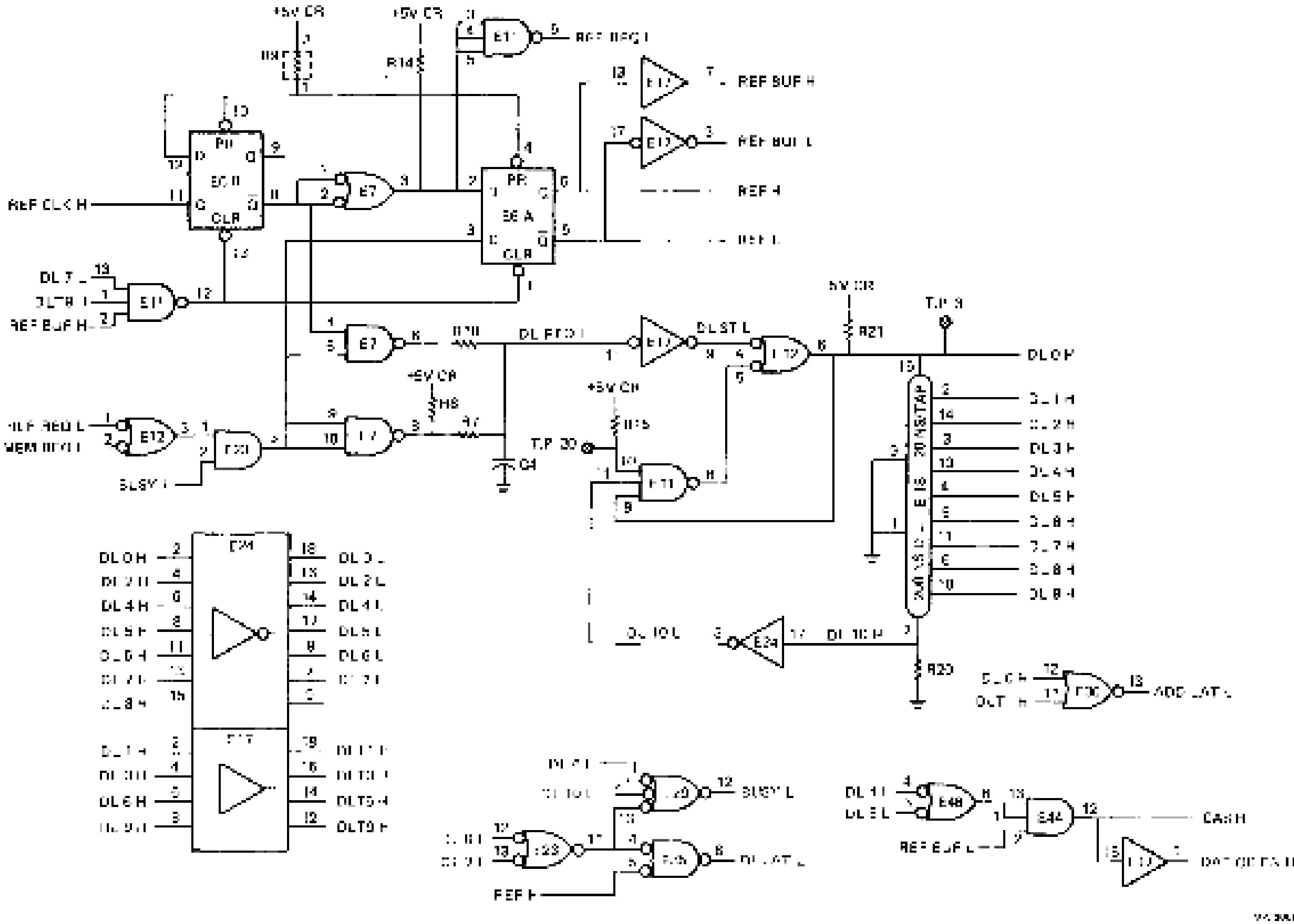


Figure 3-5 Timing Logic

The timing logic produces 13 signals that are used by other sections of the memory logic; 10 of these signals are timing chain outputs. Signal DL 0 H is considered one output of the timing chain. The other nine are derived from various gates that are controlled by the delay line taps and DL 0 H. Signals REF H, REF L and REF BUF L which are controlled by E6-A determine whether the timing chain causes the execution of a refresh cycle or a memory data cycle.

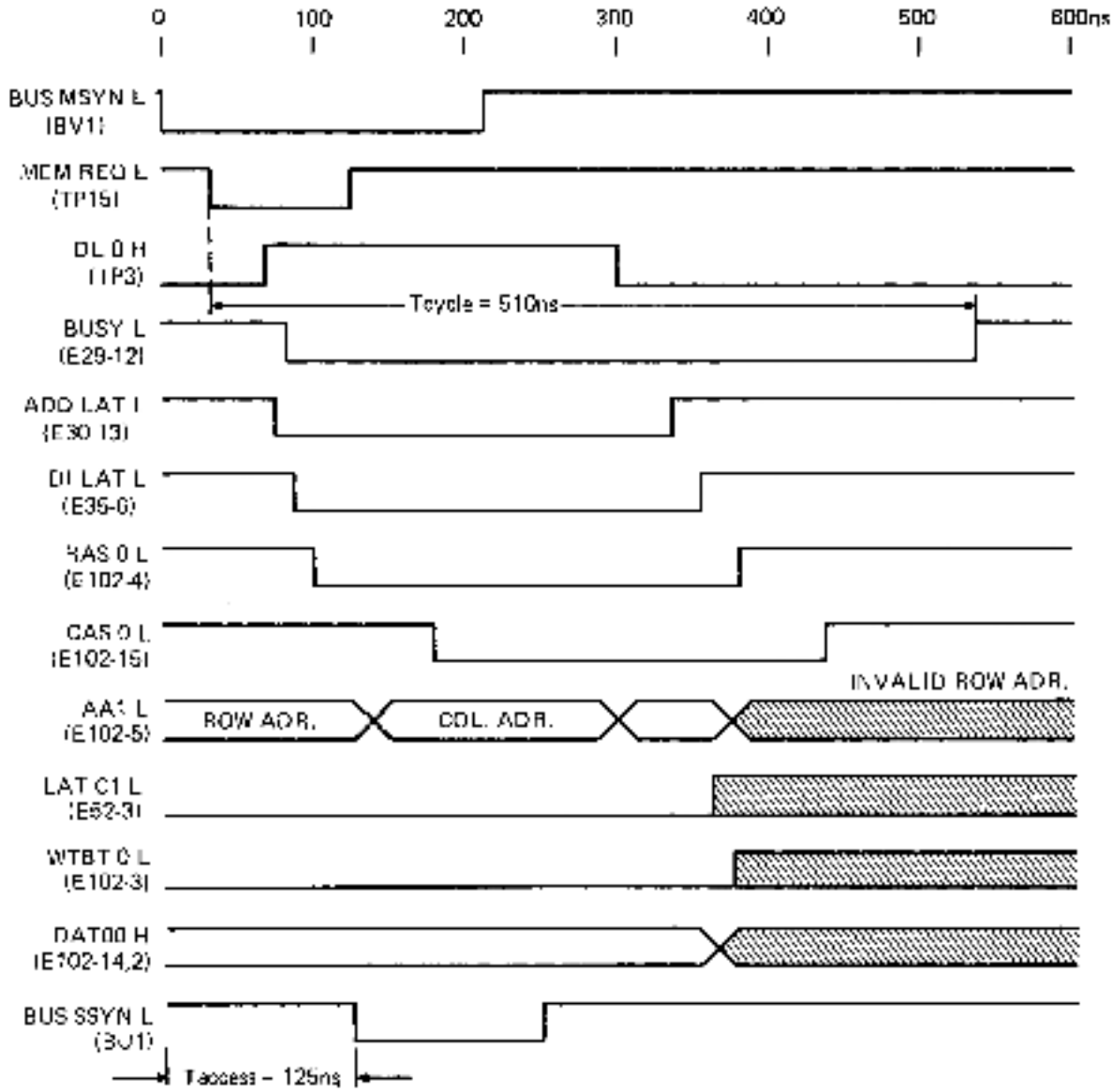
3.4.1 Memory Data Cycle Execution

Signals REF H, REF L and REF BUF L are negated so the timing chain executes a memory data cycle. The data path control logic determines if a DATI, DATO or DATOB data transfer is performed. A DATIP data transfer is interpreted as a DATI. The timing for these cycles is shown in Figures 3-6 and 3-7. The timing chain outputs, except DLT3 H, are listed below with a functional description of their effects during a memory data cycle. Signal DLT3 H is used for a refresh cycle only.

ADD LAT L	This signal, when asserted, causes the address mux to latch in the row address and column address, and also enables the RAS generation logic to assert 1 of 8 Row Address Strobe signals.
DI LAT L	This signal, when asserted, is used by the data path control and RAS generation logic to latch in the following address and control signals: C0, C1, A00, NA17, NA16 and A15. If a DATO or DATOB operation is specified, this timing signal is also used by the data path circuit to latch in data from the bus.
DL 2 L,DL 0 H	These signals are used to control the address mux. The row address is placed on-line until the DL 2 L pulse appears. The column address is then placed on-line from the leading (falling) edge of DL 2 L until the trailing (falling) edge of DL 0 H.
CAS H	This signal is the Column Address Strobe that is routed to all the MOS chips in the array by inverting line drivers. When this timing signal is asserted, the column address is latched into the 18 chips that are enabled by the Row Address Strobe signal.
DAT OC EN H	If a DATI operation is specified, the assertion of this timing signal results in the assertion of DATA OC L by the data path control. The tristate outputs of the data-out latches in the data path are then enabled.
DLT6 H,DL 6 L	If a DATI operation is specified, these signals, when asserted, enable the parity checking circuitry in the parity gen/check logic.
DLT1 H	If a DATO or DATOB operation is specified, the leading (rising) edge of this signal causes the data path control logic to assert BUS SSYN L and SSYN L.
DL 2 L,DLT6 H	If a DATI operation is specified, these signals are used by the data path control logic to gate the following signals: BUS SSYN L, SSYN L, OUT EN L and OUT EN H. These data path control outputs are asserted at the trailing (rising) edge of DL 2 L. Data from the storage array is latched in by the data-out latches, and the line transceivers are enabled placing data on the bus. At this time, the parity gen/check logic initiates certain steps if a parity error has been detected.

3.4.2 Refresh Cycle Execution

Signals REF H, REF L and REF BUF L are asserted so the timing chain executes a refresh cycle (Figure 3-8). These three signals disable the data cycle functions of the timing chain and enable the refresh functions as follows.

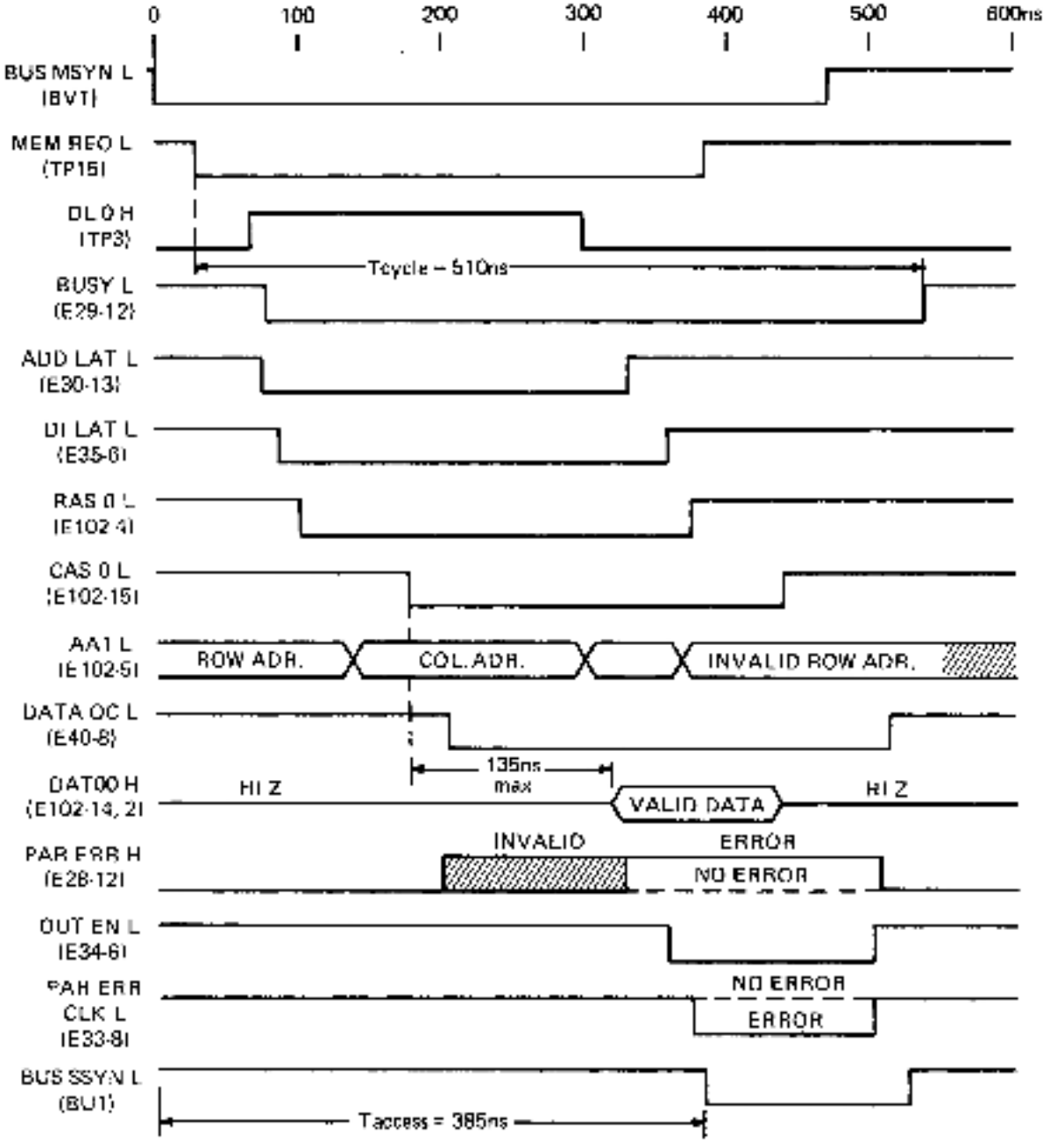


NOTES

1. SIGNALS RAS 0 L, CAS 0 L, AA1 L, WTBT 0 L AND DAT00 H ARE AT THE MOS STORAGE ARRAY (PARAGRAPH 3.2.2).
2. FOR A DATO OPERATION, BUS AND PROCESSOR DELAYS DETERMINE WHEN THE FOLLOWING SIGNALS ARE FIRST ASSERTED: LAT C1 L, WTBT 0 L, DATA (i.e. DAT00 H) AND THE MULTIPLEXED ROW ADDRESS (i.e. AA1 L). TYPICALLY, THESE SIGNALS ARE ASSERTED BY THE TIME BUS MSYN L APPEARS AT THE MEMORY RECEIVER. SIGNALS LAT C1 L AND WTBT 0 L ARE LATCHED WHEN DI LAT L IS ASSERTED.
3. DATA FROM THE BUS IS CHANNELED TO THE DAT < 15:00 > H LINES WHEN LAT C1 L IS ASSERTED.

MA-3946

Figure 3-6 DATO/DATOB Memory Timing (Typical)



NOTES

1. SIGNALS PAR ERR H, PAR ERR CLK L AND PAR ERR CLK H ARE GENERATED BY THE PARITY GEN/CHECK LOGIC.
2. ONCE THE DATA AND PARITY BITS ARE RETRIEVED FROM THE ARRAY, SIGNAL PAR ERR H BECOMES VALID.

MA-3047

Figure 3-7 DATI/DATIP Memory Timing (Typical)

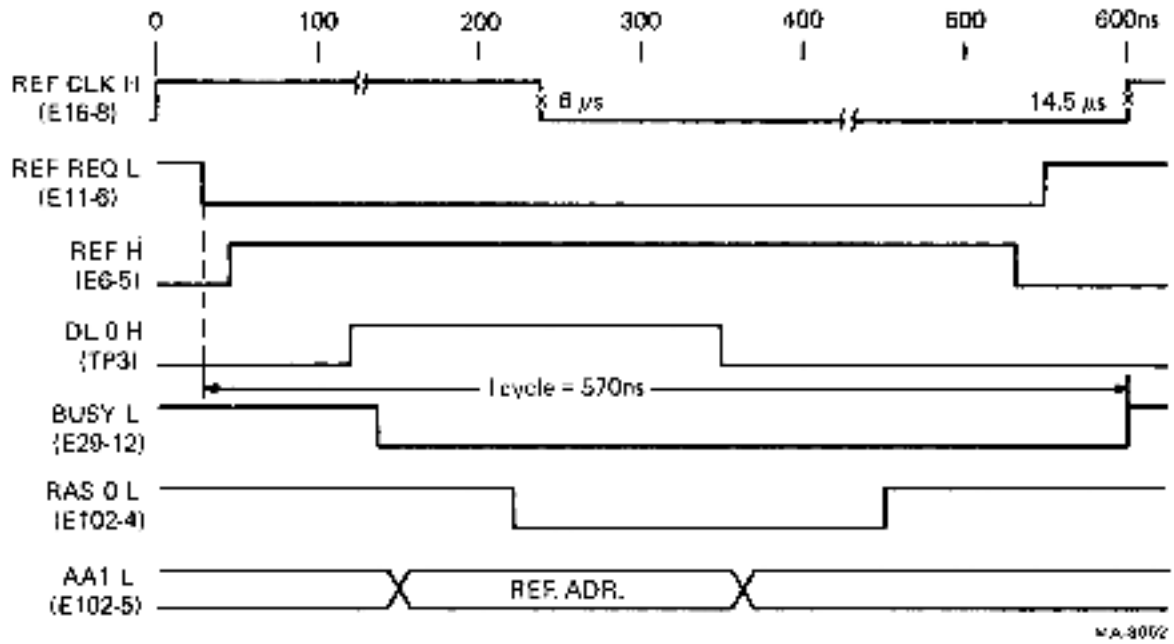


Figure 3-8 Refresh Timing (Typical)

REF L

1. Disables the selection of the row address and column address by the address mux.
2. Disables the decoding of NA17, NA16 and A15 by the RAS generation logic.
3. Disables the effect of the timing signals on the following data path control outputs: OUT EN H, OUT EN L, SSYN L and BUS SSYN L. However, these outputs can still be asserted in reaction to a data transfer involving the CSR.
4. Disables the circuitry which reacts to a parity error.

REF BUF H

1. Inhibits the assertion of the write byte signals by the data path control logic.
2. Inhibits the assertion of CAS H and DAT OC EN H by the timing logic.

REF H

1. Inhibits the assertion of DI LAT L by the timing logic.
2. Enables the address mux to select the refresh address when DL 0 H is asserted.
3. Enables the RAS generation logic to assert all eight Row Address Strobes when DLT 3 H is asserted.

Timing chain signals DL 7 L and DLT9 H are used in conjunction with REF BUF H to produce a clear pulse for E6-A and E6-B (Figure 3-5). Flip-Flop E6-A, in turn controls signals REF H, REF L, REF BUF H and REF BUF L. In preparation for the next memory cycle, these four signals are negated when E6-A and E6-B are cleared at the trailing (rising) edge of DL 7 L. Signal REF REQ L is also negated at this time.

3.5 REFRESH LOGIC

The refresh logic, shown in sheet 6 of the print set, generates REF CLK H and the refresh address. Signal REF CLK H is derived from a 555 timer (E5) which is set up as a free running oscillator, powered by the +15 V/+12 V module input (V-555). The REF CLK H signal oscillates with a period of 14.5 μs and has a positive pulse width of 6 μs during each period. The leading (rising) edge of REF CLK H is used by the timing logic to assert REF REQ L and therefore, REF REQ L is asserted once every 14.5 μs. Signal REF REQ L, when asserted, initiates a refresh cycle if the memory is not busy. If the memory is busy, the refresh cycle is delayed until the present cycle is completed (Paragraph 3.4).

The refresh address is generated by a dual, 4-bit, binary counter (E43) which is wired to function as a single 8-bit counter. The eighth bit at E43 pin 8 is not used. The 7-bit refresh address is in the range of 0–127 and is incremented at the trailing (falling) edge of REF CLK H after each refresh cycle. The incremented address is then used during the next refresh cycle. Each data cell in all the MOS chips is periodically refreshed in less than 2 ms (once for every 128 refresh cycles).

3.6 ADDRESS DECODE LOGIC

The address decode logic, shown in Figure 3-9, determines if an address on the Unibus/special bus is assigned to the CSR or a memory location in the MS11-L. (Addressing conventions for the Unibus and special bus are discussed in Paragraph 2.2.1.1).

Line receivers (8640s) and transceivers (8641) accept A21–A01 from a special bus or A17–A01 from the Unibus. In Unibus operation, jumper W4 is OUT, the receivers for A21–A18 are disabled, and UNIB L is asserted.

To determine if the CSR is selected for a data transfer, the bus address is decoded by the combination of comparator E54 and the following gates: E52, E59, E53, E60 and E45. With UNIB L asserted for Unibus operation, E53 pin 3 is held high and A17–A01 are decoded. In special bus operation, the signal level at E53 pin 3 is determined by A21–A18 and therefore A21–A01 are decoded. The CSR address, assigned by S1–1 to S1–4, is in the range of 772100–772136 for Unibus operation or 17772100–17772136 for special bus operation (Paragraph 2.2.1.3). For each mode of operation, CSR SEL H and CSR SEL L are asserted if an address on the bus matches the assigned CSR address.

On the Unibus/special bus, BUS DC LO L is negated as long as +5 V power is reliable. With BUS DC LO L negated, the address decode logic generates MSYN H whenever BUS MSYN L is asserted. With CSR SEL H, CSR SEL L and MSYN H asserted, the MS11-L responds to a data transfer involving the CSR.

Jumpers W5 and W21 are used to specify the I/O peripheral page to the top 2K, 4K or 8K of the Unibus or special bus address space (Paragraph 2.2.1.2). If the address on the bus is within the peripheral page, the output of E60 is low. The CSR address is always in the top 2K of the available address space.

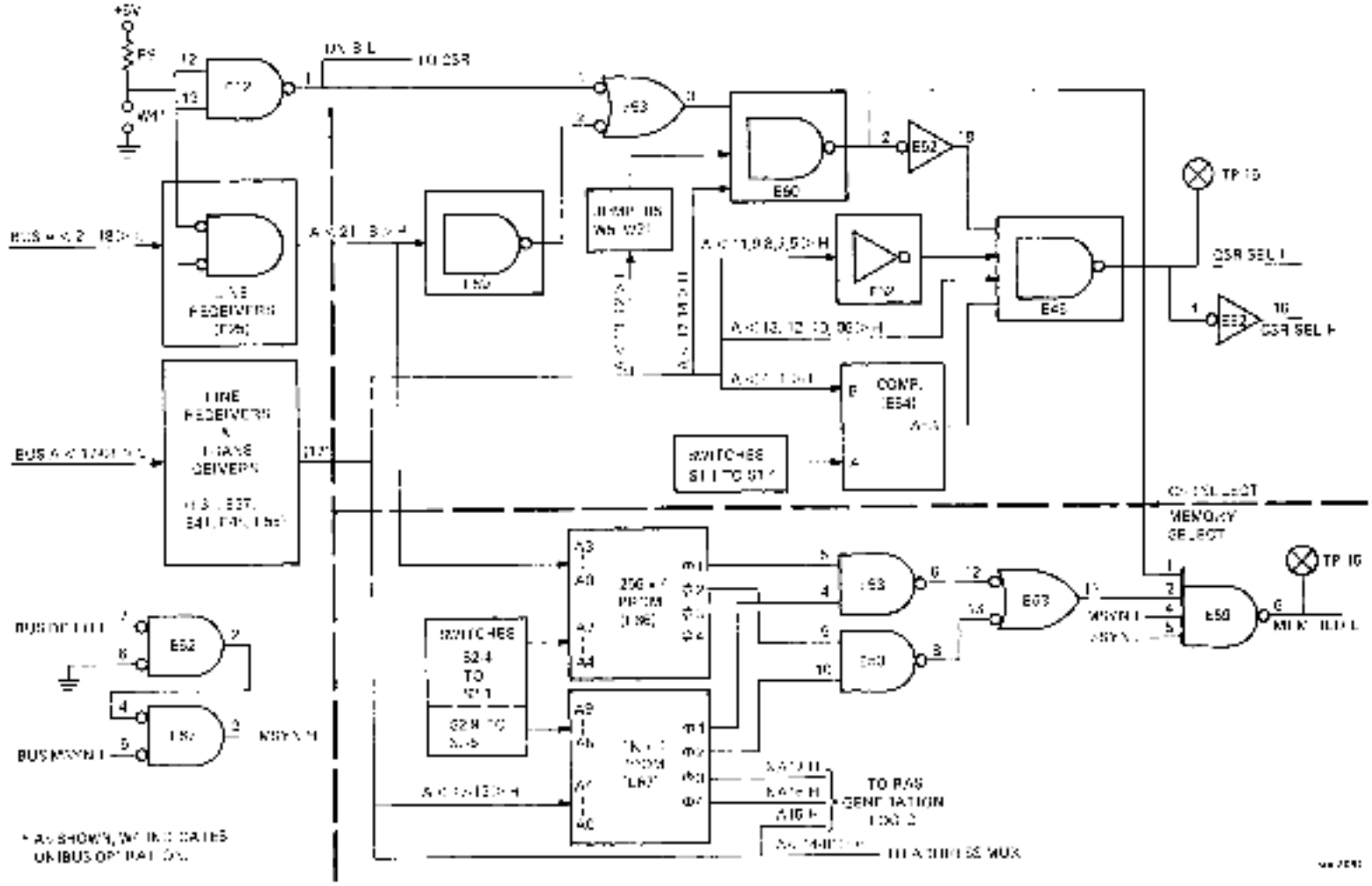


Figure 3-9 Address Decode Logic

In special bus operation, A21–A13 are decoded by E66, E67 and E53 to determine if a memory location assigned to the MS11-L is selected for a data transfer. Device E66 is a 256 × 4-bit, programmable-read-only memory (PROM) and E67 is a 1K × 4-bit PROM. The Φ1 and Φ2 outputs of both PROMs are used to decode A21–A13. The address space on the bus occupied by the memory module is determined by the memory starting address and address range. Switches S2-1 through S2-9 assign the starting address to a 4K boundary in the bus address space (Paragraph 2.2.1.1). The content of E67 is related to the memory address range and is therefore different for each version of the MS11-L. However, the content of E66 is the same for all MS11-L versions. If an address on the bus is within the address space occupied by the module, the Φ1 outputs or Φ2 outputs go high and E53 pin 11 goes high. In Unibus operation, logical 0s are presented to E66 for address bits A21–A18 since the corresponding line receivers have been disabled. To respond correctly to Unibus memory addresses, S2-1 through S2-4 should be ON.

The address decode logic enables bus master access to a memory location on the module by asserting MEM REQ L at E59 pin 6. Signal MEM REQ L is asserted providing the following conditions are met:

1. Gate E53 pin 11 is high, indicating that the address on the bus is assigned to a memory location on the module.

2. The output of E60 is high, indicating that the address on the bus is not in the I/O peripheral page.

3. Signal MSYN H is asserted, indicating that BUS MSYN L is asserted and BUS DC LO L is negated.

4. Signal SSYN L is negated, indicating that BUS SSYN L is not currently asserted by the MS11-L. All prior communication with a bus master is finished.

Signal MEM REQ L, when asserted, initiates a memory data cycle if the memory is not busy. If the memory is busy, the memory data cycle is delayed until the present cycle is completed (Paragraph 3.4).

Address information is channeled to the address mux and RAS generation logic via the address decode line receivers as soon as it is available on the bus. In accordance with the address space occupied by the module, E76 may have modified address bits A17 and A16 to provide NA17 and NA16.

3.7 RAS GENERATION LOGIC

The RAS generation logic, shown in Figure 3-10, produces eight Row Address Strobe signals (RAS <7-0> H). In a 128K memory, all 8 signals are routed to the MOS storage array by 16 inverting line drivers. The logic contains a latch with tristate outputs (E38), a 3:8 decoder (E51), and two 2:1 multiplexers (E58 and E65). Signals ADD LAT L, DI LAT L and DLT3 H are generated by the timing chain. The tristate outputs of E38 are always enabled since E38 pin 1 is grounded.

For a memory data cycle, REF H and REF L are negated. With REF H negated, the B inputs of the multiplexers are selected during the entire cycle. Address information (NA17, NA16 and A15) appears at the decoder inputs before the timing chain is triggered and is latched at a later time when DI LAT L is asserted. When ADD LAT L is asserted, the decoder is enabled and 1 of 8 RAS H signals is asserted, enabling the 16-chip bank that contains the desired memory location for a data transfer (Table 3-3). MOS chips in the array that do not receive the asserted Row Address Strobe, do not cycle internally, remaining in a low-power (standby) state.

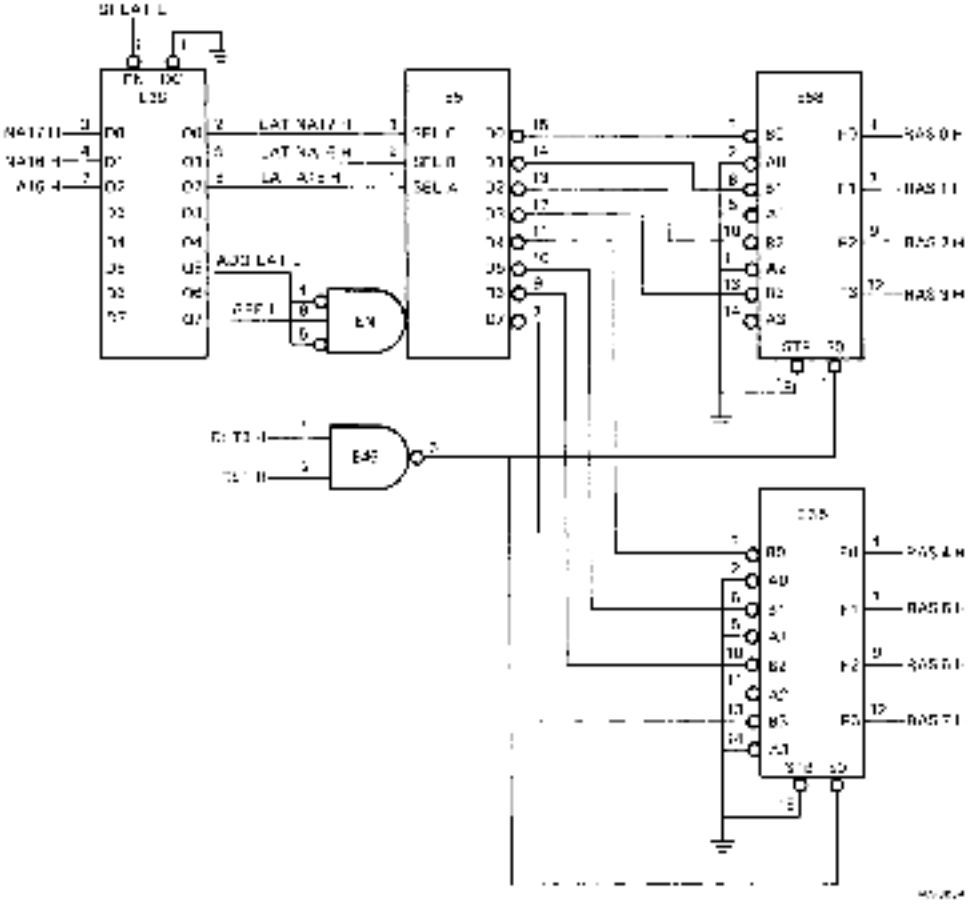


Figure 3-10 RAS Generation Logic

Table 3-3 RAS Generation

Memory Bank	Address Information			Associated Row Address Strobe
	NA17 H	NA16 H	A15 H	
0–16K	LO	LO	LO	RAS 0 H
16–32K	LO	LO	HI	RAS 1 H
32–48K	LO	HI	LO	RAS 2 H
48–64K	LO	HI	HI	RAS 3 H
64–80K	HI	LO	LO	RAS 4 H
80–96K	HI	LO	HI	RAS 5 H
96–112K	HI	HI	LO	RAS 6 H
112–128K	HI	HI	HI	RAS 7 H

For a refresh cycle, REF H and REF L are asserted. With REF L asserted, the decoder is disabled. When DLT3 H is asserted, the A inputs of the multiplexers are selected and all eight RAS H signals are asserted. Therefore, all the MOS chips in the storage array are enabled for a refresh cycle.

3.8 ADDRESS MUX

The address mux, shown in sheet 6 of the print set, contains 3 octal latches with tristate outputs (E50, E57 and E64). The appropriate latch outputs are wire-ORed to produce seven address lines (MUX A<7:1> H); e.g., the three Q0 outputs are wire-ORed to produce MUX A1 H. In a 128K memory, the 7 address mux outputs are routed to the MOS storage array by 35 inverting line drivers. Signals ADD LAT L and DL 2 L are generated by the timing chain which is triggered by DL 0 H.

For a memory data cycle, REF H and REF L are negated. The row address (A<07:01> H) and column address (A<14:08> H) appear at the inputs of E57 and E64 before the timing chain is triggered. With DL 0 H and DL 2 L negated, the tristate outputs of E57 are enabled and therefore, the row address is channeled to the MUX A<7:1> H lines as soon as it is received. The row address and column address are latched in when ADD LAT L is asserted by the timing chain. At the leading (falling) edge of DL 2 L, the outputs of E57 are disabled and E64 places the column address on-line. The column address is then removed from the mux output lines at the trailing (falling) edge of DL 0 H.

For a refresh cycle, REF H and REF L are asserted. With REF L asserted, the outputs of E57 and E64 are disabled. The refresh address appears at the inputs of E50 before the refresh cycle is initiated. When DL 0 H is asserted, E50 channels the refresh address to the mux output lines.

3.9 DATA PATH CONTROL LOGIC

The data path control logic, shown in Figure 3-11, generates nine signals that are used by other sections of the MS11-L to control the flow of data for memory data cycles and CSR data cycles. An input for the parity gen/check logic and signals SSYN L and BUS SSYN L are also provided by the data path control logic. Timing for memory data cycles is shown in Figures 3-6 and 3-7 while Figure 3-12 shows the timing for the CSR data cycles. The data path control outputs are generated in accordance with Unibus/special bus signals, address decode signals and timing signals. Signals REF H, REF L and REF BUF L are asserted by the timing logic for a refresh cycle only.

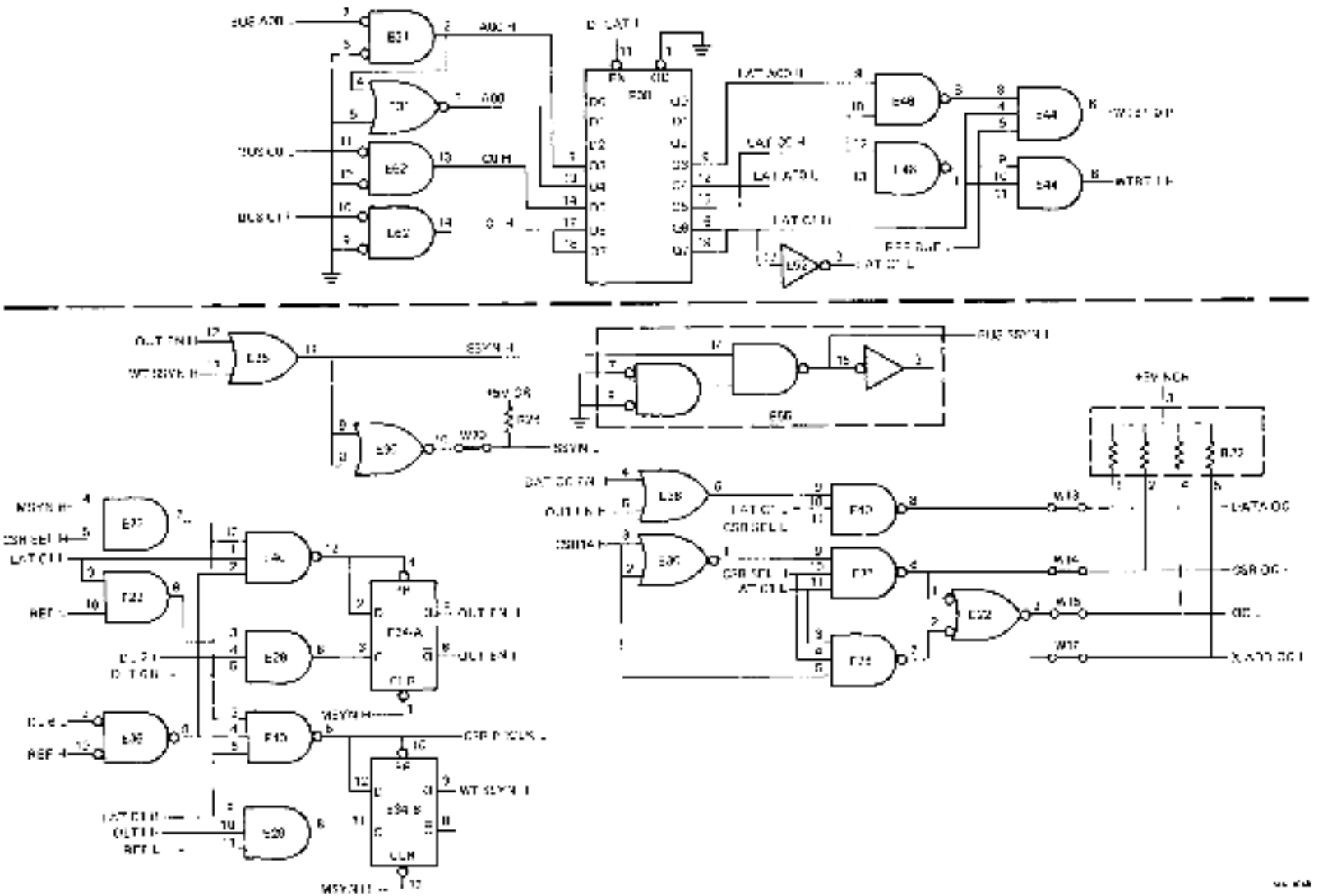
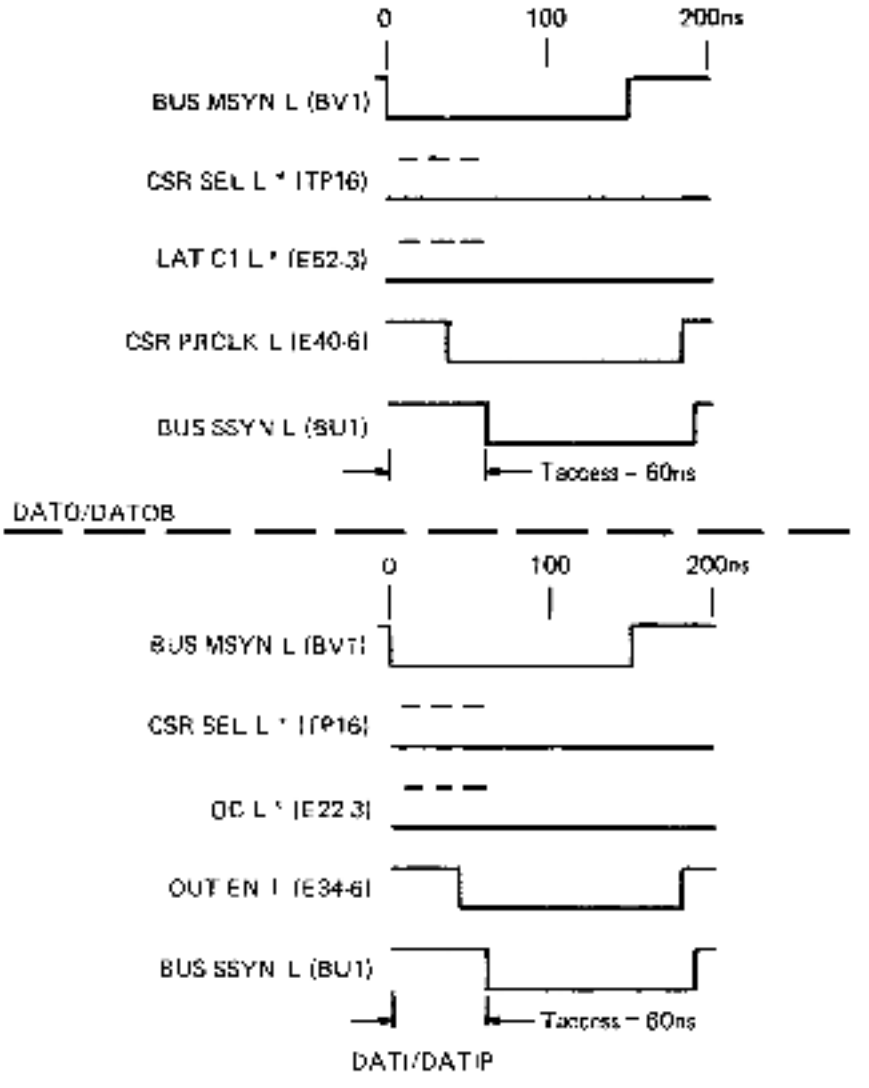


Figure 3-11 Data Path Control Logic



* ACTUAL TIME DEPENDS ON BUS AND PROCESSOR DELAYS. TYPICALLY, THE SIGNAL IS ASSERTED BY THE TIME BUS MSYN L APPEARS AT THE MEMORY RECEIVER

MA-3048

Figure 3-12 CSR Timing (Typical)

Unibus/special bus signals C0, C1 and A00 are decoded to determine the state of the write byte signals (WTBT <1:0> H), except during a refresh cycle (Table 3-4). In a 128K memory, four inverting line drivers route the write byte signals to the MOS storage array. The write byte signals specify a read or write operation for the MOS chips in the array that are associated with each byte. The specified operation is executed by the 18-chip bank for which the Row Address Strobe and Column Address Strobe are asserted. Bus signal C1 is also used to generate LAT C1 H and LAT C1 L which are used elsewhere in the data path control logic. Signal LAT C1 L is also routed to the data path circuit. Note that LAT C1 H, LAT C1 L and the write byte signals are latched when D1 LAT L is asserted by the timing chain.

Table 3-4 Write Byte Selection

Data Transfer Type	Bus Signals			Write Byte Signals		Effect on MOS Storage Array During 0 Memory Data Cycle
	BUS C1 L	BUS C0 L	BUS A00 L	WTBT 1 H	WTBT 0 H	
DATI	HI	HI	X	LO	LO	An entire word (bits 17–00) is read from the array
DATIP	HI	LO	X	LO	LO	Same as DATI
DATO	LO	HI	X	HI	HI	An entire word is written into the array
DATOB	LO	LO	HI	LO	HI	The low byte (bits 07–00 and 16) is written into the array
DATOB	LO	LO	LO	HI	LO	The high byte (bits 15–08 and 17) is written into the array

NOTE

The MOS array stores 18-bit words. Bits 15–00 are data, and bits 17 and 16 are the associated parity bits generated by the MS11-L.

To generate the nine remaining outputs, the data path control logic decodes the following signals:

LAT C1 L, LAT C1 H	Derived from bus signal C1
CSR SEL L, CSR SEL H, MSYN H	Address decode signals
DAT 0C EN H, DLT1 H, DL 2 L, DLT6 H, DL 6 L	Timing chain signals.

Table 3-5 relates four modes of operation to the remaining data path control outputs. A different combination of outputs is asserted for each mode. The timing chain is not activated for CSR data cycles.

Table 3-5 Operating Mode Selection

Mode	LAT C1 H	LAT C1 L	CSR SEL H	CSR SEL L	Sequence Signal	Asserted Data Path Control Outputs
DATI/DATIP (Memory)	LO	HI	LO	HI	DAT OC EN H ↑ DL 2 L ↓	DATA OC L OUT EN L, OUT EN H, SSYN L, BUS SSYN L
DATO/DATOB (Memory)	HI	LO	LO	HI	DLT1 H ↑	SSYN L, BUS SSYN L
DATI/DATIP (CSR)	LO	HI	HI	LO	– MSYN H ↑	OC L, CSR OC L or X ADD OC L OUT EN L, OUT EN H, SSYN L, BUS SSYN L
DATO/DATOB	HI	LO	HI	LO	MSYN H ↑	CSR PRCLK L, SSYN L, BUS SSYN L

NOTES

1. **(Signal) ↑ = leading edge of asserted signal**
   (Signal) ↓ = trailing edge of asserted signal

2. **In accordance with the bus mode, the indicated edge of a sequence signal triggers the assertion of the associated control output(s). A control output triggered by a sequence signal remains asserted until the trailing (falling) edge of MSYN H.**

3. **For a CSR read operation, CSR OC L is asserted if bit 14 in the CSR is a logical 0 or X ADD OC L is asserted if bit 14 is a logical 1. In either case OC L is asserted.**

Signals DATA OC L,OC L, CSR OC L and X ADD OC L are generated by various gates in the data path control logic (Figure 3-11). These signals in conjunction with OUT EN L are used by the data path circuit to channel data to the bus from the MOS storage array or CSR. The data path circuit uses LAT C1 L to channel data from the bus to the MOS storage array and CSR.

Signals OUT EN H and OUT EN L are generated by flip-flop E34-A. For a memory read cycle, a logical 1 is clocked into E34-A in accordance with DL 2 L and DLT6 H. For a CSR read cycle, E34-A is set by a negative pulse at E40 pin 12 when MSYN H is asserted. The OUT EN H signal is used by the parity gen/check logic to initiate certain steps if a parity error is detected during a memory read cycle.

Signal CSR PRCLK L which is asserted by E40 pin 6 during a CSR write cycle generates two clock signals for the CSR, and sets flip-flop E34-B. Note that for a memory write cycle, a logical 1 is clocked into E34-B at the leading (rising) edge of DLT1 H.

Signals BUS SSYN L and SSYN L are asserted when the Q output of either E34-A or -B goes high. Therefore, although the timing is different, BUS SSYN L and SSYN L are asserted in all four modes of operation. Once BUS SSYN L is asserted, the bus master negates BUS MSYN L. Then BUS SSYN L

is negated since E34-A and -B are cleared by MSYN H. The bus is now free for another data cycle. However, if the memory was just accessed, the memory data cycle is still in progress. Bus master access to the CSR is inhibited when DL 6 L is asserted by the timing chain.

For a refresh cycle, signals REF L, REF H and REF BUF L are asserted. The clock signals for E34-A and -B are inhibited by REF L. E36 pin 8 is held high by REF H, and DAT OC EN H is inhibited by the timing logic. Therefore, the timing chain has no effect on the data path control logic. Also, the write byte signals are held low by REF BUF L. The CSR can be accessed at any time during a refresh cycle.

3.10 DATA PATH

The data path circuit shown in Figure 3–13 contains line transceivers (8641s) for Unibus/special bus data and three groups of octal latches: data-in (E2,E4), data-out (E26,E32) and CSR-out (E9,E14,E20). These latches have tristate outputs which are controlled by signals from the data path control logic. Signal DI LAT L is generated by the timing chain during a memory data cycle.

When a CSR or memory write cycle (DATO or DATOB) is performed, LAT C1 L is asserted allowing E2 and E4 to channel the Unibus/special bus data to the DAT<15–00> H lines. The DAT<15–00> H lines form an internal data bus on the module. For a CSR write cycle, data is strobed into the CSR bits that are used. For a memory write cycle, data is latched when DI LAT L is asserted, two parity bits are generated, and the appropriate data byte(s) and parity bit(s) are written into the MOS storage array.

During a memory read cycle (DATI or DATIP), DATA OC L is asserted enabling the outputs of E26 and E32. As soon as data is retrieved from the MOS storage array, it is channeled to the line transceivers. The parity of the data is also recalculated and compared to the parity bits retrieved from the array. Data is then latched by E26 and E32 and placed on the Unibus/special bus when OUT EN L is asserted. At this time, the parity gen/check logic initiates certain steps if a parity error is detected. Note that the MOS storage array latches the data and parity bits that it supplies until the Column Address Strobe is negated by the timing chain.

The CSR-out latches, E14, E20 and E9, are controlled by OC L, CSR OC L and X ADD OC L respectively. When a CSR read cycle is performed, information is channeled to the line transceivers by E14 and either E20 or E9, and is then placed on the bus when OUT EN L is asserted. Error address information (A17–A11) or data previously written into the CSR is transferred to bus data lines 11–05 via E20, if bit 14 in the CSR is a logical 0 (CSR OC L is low and X ADD OC L is high). Via E9, error address bits A21–A18 are transferred to bus data lines 08–05 and logical 0s are transferred to 11–09, if CSR bit 14 is a logical 1 (CSR OC L is high and X ADD OC L is low). In either case, the remaining four bits that are used in the CSR word are transferred to the bus via E14 since OC L always goes low for a CSR read operation. Five logical 0s, which correspond to latch inputs that are grounded, are placed on the bus for the unassigned bits. In Unibus operation, bit 14 in the CSR is forced to logical 0.

3.11 PARITY GEN/CHECK LOGIC AND CSR (Figures 3-14 and 3-15)

3.11.1 Parity Generation

The parity gen/check logic uses two 74S280 chips (E56 and E63) to generate two parity bits for data on the DAT<15–00> H lines. A signal derived from CSR bit 2, and one data byte are applied to each chip. The parity bits are designated bit 17 (assigned to the high byte) and bit 16 (assigned to the low byte). Bits 17 and 16 are routed to the MOS storage array by the PDI17 H and PDI16 H lines. For a memory write cycle, data from the Unibus/special bus is channeled to the DAT<15–00> H lines and latched. The appropriate data byte(s) and assigned parity bit(s) are then written into the MOS storage array.

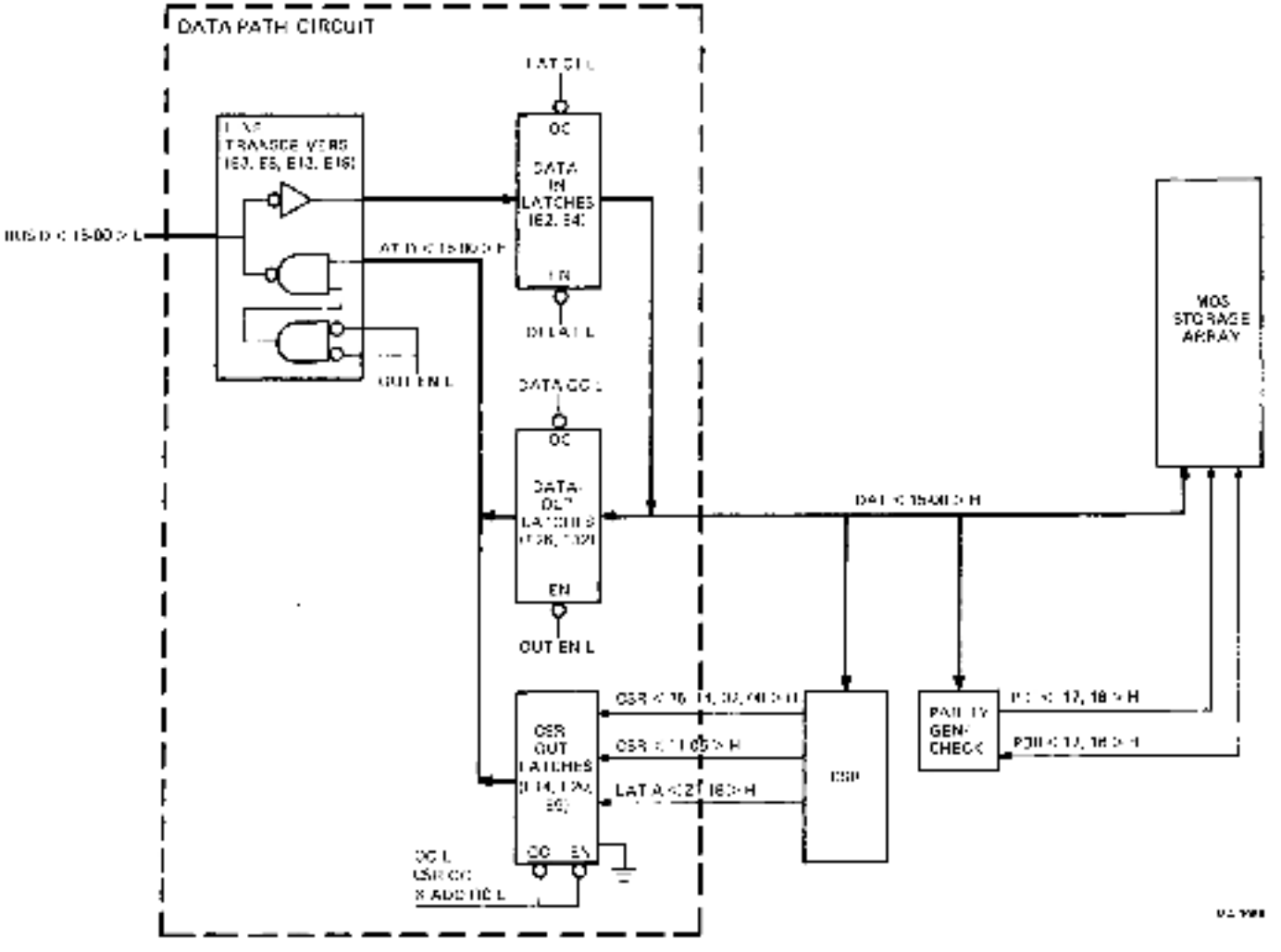


Figure 3-13 Data Path

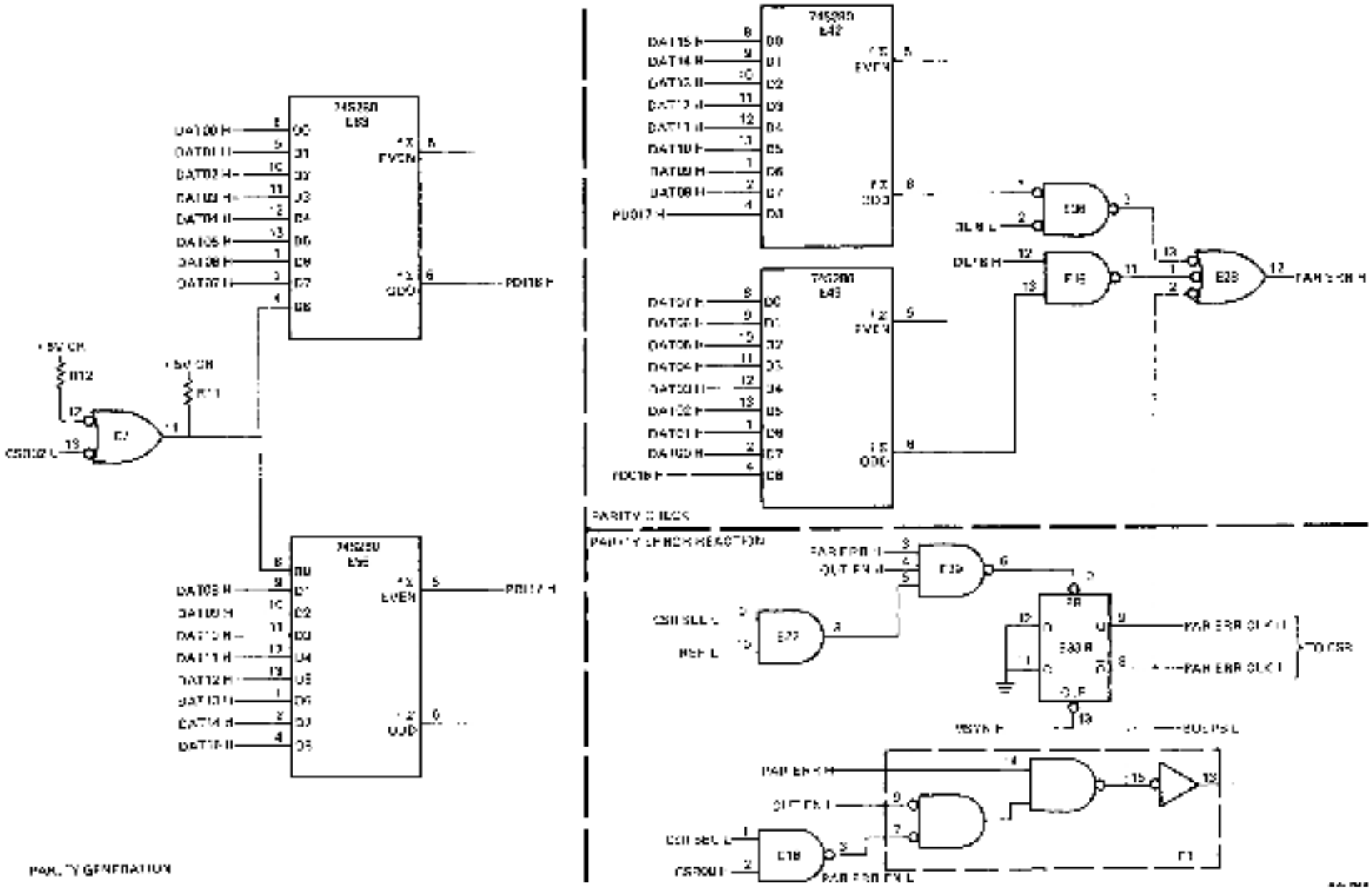


Figure 3-14 Parity Gen/Check Logic

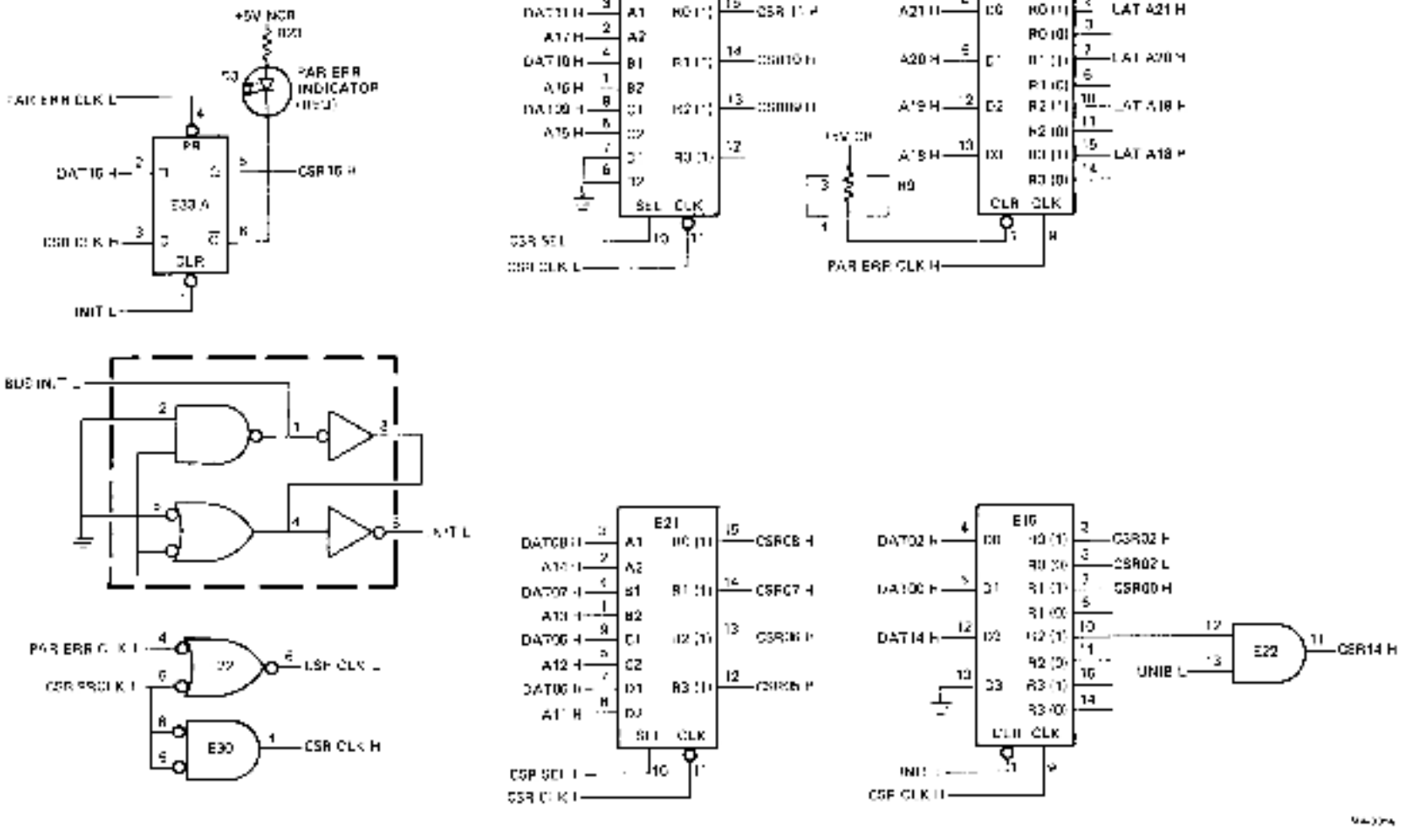


Figure 3-15 CSR

The outputs of E56 and E63 are determined by the number of logical 1s (high signals) in their respective 9-bit inputs. The parity calculation is controlled by bit 2 in the CSR. If CSR bit 2 is a logical 0, CSR02 L is negated and the parity that is calculated is correct (each parity bit reflects the number of logical 1s in the corresponding data byte). Odd parity is calculated to produce bit 17; even parity is calculated to produce bit 16. For an odd (even) parity calculation, the parity bit is set or cleared so that the total number of logical 1s is odd (even) once the parity bit is added to the data byte. If CSR bit 2 is a logical 1, the wrong parity is calculated yielding parity bits that are inverted with respect to their correct values.

3.11.2 Parity Check

The parity gen/check logic uses two 74S280 chips (E42, E49) and three gates to determine if the parity is correct for both bytes retrieved from the MOS storage array. For the high byte, odd parity is correct; for the low byte, even parity is correct.

During a memory read cycle, timing signals DL 6 L and DLT6 H are already asserted when the data and parity bits stored in the array become available. Each data byte with its associated parity bit is applied to one 74S280 chip (E42 or E49). The odd output of E42 or E49 is high (low) if the number of logical 1s in the 9-bit input is odd (even). Signal PAR ERR H is asserted if the parity of one or both bytes is not correct.

3.11.3 Parity Error Reaction

Signals PAR ERR H, PAR ERR CLK H and PAR ERR CLK L are used to initiate certain steps if a parity error is detected during a memory read cycle (Figure 3-14). For a memory read cycle, CSR SEL L and REF L are negated and PAR ERR H is already valid when OUT EN L and OUT EN H are asserted. If PAR ERR H is high (indicating a parity error), E33-B is set once OUT EN H is asserted and therefore, PAR ERR CLK H and PAR ERR CLK L are asserted. The parity error reaction is executed as follows:

1. With PAR ERR H high and OUT EN L low, BUS PB L is asserted on the Unibus/special bus if CSR bit 0 is set (CSR00 H is high). The line transceivers for data as well as BUS PB L are enabled when OUT EN L goes low. Signal PAR ERR H is held high as long as PAR ERR CLK L is asserted.

2. Signal PAR ERR CLK L, when asserted, sets E33-A (bit 15) in the CSR (Figure 3-15). The Q output of E33-A then turns on a red LED (D3) on the module.

3. The assertion of PAR ERR CLK L also causes CSR CLK L to go low which in turn strobes error address bits A17–A11 into the CSR. (Since CSR SEL L is negated, the A2–D2 inputs of E21 and E27 are selected for storage when the clock pulse is received.)

4. Signal PAR ERR CLK H, when asserted, strobes error address bits A21–A18 into E10 of the CSR. For Unibus operation, logical 0s are strobed into E10 for A21–A18, since the corresponding line receivers have been disabled.

3.11.4 CSR Access

The CSR has its own address in the top 2K of the Unibus or special bus address space and can be read or written into by any device designated as bus master, even during a memory refresh cycle. The address decode logic enables bus master access to the CSR by asserting CSR SEL H, CSR SEL L and then MSYN H.

If bus signals C0 and C1 specify a write cycle (DATO or DATOB), data from the bus is channeled to the DAT<15-00> H lines. When MSYN H is asserted, the data path control logic asserts CSR PRCLK L which in turn generates two CSR clock signals that strobe the data into the CSR (Figure 3-15). The leading (rising) edge of CSR CLK H strobes data bits 15, 14, 02 and 00 into the CSR. However, for Unibus operation, CSR14 H (bit 14) is held low (logical 0), since UNIB L is asserted. The leading (falling) edge of CSR CLK L strobes data bits 11-05 into the CSR, since CSR SEL L is asserted. (Data and error address information are present at the inputs of E21 and E27 but the asserted CSR SEL L signal selects the data inputs for storage when the clock signal is received.) A CSR write cycle destroys any error address bits previously stored in E21 and E27; however, E10 is not affected.

If a read cycle (DATI or DATIP) is specified, information from the CSR is channeled via the data path circuit to the bus. The information placed on the bus for bits 11-05 is determined by the data path control logic in accordance with CSR bit 14. The contents of E21 and E27 are retrieved if bit 14 is a logical 0; the contents of E10 are retrieved if bit 14 is a logical 1. In either case, the contents of E15 and E33-A are retrieved and unassigned bits in the CSR word are read as logical 0s.

CSR bits 15, 14, 02 and 00 are cleared by the assertion of BUS INIT L. This signal is asserted for a short time by the processor after system power-up or in response to a reset instruction. The MS11-L is prevented from accidentally asserting BUS PB L (indicating a parity error) before the first memory read cycle. The generation of correct parity for the first memory write cycle is also ensured.

CHAPTER 4
MAINTENANCE

4.1 GENERAL

This chapter discusses preventive and corrective maintenance procedures that apply to all versions of the MS11-L memory. A major point in the maintenance philosophy is that the user understands the normal operation of the MS11-L as described in the previous chapters. This knowledge and the maintenance information in this chapter should enable the user to isolate malfunctions.

Two pieces of equipment are recommended for checking and troubleshooting the memory: the Tektronix 453 Dual Trace Oscilloscope (or equivalent) and the Weston Schlumberger Model 4443 Digital Voltmeter (or equivalent) with 0.5% accuracy.

All tests and adjustments must be performed in an ambient temperature range of 20° to 30° C (68° to 86° F). All power (and the battery backup) must be OFF before installing or removing modules. When the green LED on the MS11-L module is OFF, it is safe to proceed.

4.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks, performed at intervals, to detect conditions that lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance and may be performed along with other scheduled preventive maintenance procedures for the computer system.

1. Visual inspection
2. Voltage measurements
3. MAINDEC testing

4.2.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

4.2.2 Voltage Measurements

Once primary power has been turned on, the dc power voltages listed below should be checked at the backplane.

Voltage and Tolerance	Backplane Pin(s)
+5 V ± 5%, max ripple = 0.2 V p-p	AA2, BA2, CA2
+5 V BBU ± 5% max ripple = 0.2 V p-p (only if jumper W7 is IN and W3 is OUT on the module)	BD1
+15 V ± 10%, 3.3% or +12 V ± 5%, max ripple = 1 V p-p	AR1
−15 V ± 10% or −12 V ± 10%, max ripple = 1 V p-p	AS1

4.2.3 MAINDEC Testing

The following diagnostic program should be used with the MS11-L: 0-128K Memory and Memory Parity Exerciser (MAINDEC-11-CZQMC). To verify proper operation of the memory, run two passes of the diagnostic. No errors are permitted. Also, verify that the program printout agrees with the total memory in the system.

NOTE

The MAINDEC-11-CZQMC diagnostic is compatible with a 4K I/O peripheral page only (Paragraph 2.2.1.2)

4.3 CORRECTIVE MAINTENANCE

This paragraph discusses procedures for specific corrective maintenance of the MS11-L. If a problem has been isolated to the MS11-L, the bad memory should be replaced with a new memory module and then the system should be retested. The MAINDEC-11-CZQMC diagnostic should be used for fault isolation (Paragraph 4.2.3). In most cases, a bad memory module can be detected by utilizing the error printout and program listing. Troubleshooting procedures, presented in the following paragraphs, can be used in addition to MAINDEC testing or if the diagnostic program cannot be loaded. It is assumed that a visual inspection and voltage measurements have already been carried out as specified in Paragraphs 4.2.1 and 4.2.2.

The following paragraphs also assume that the starting address of the MS11-L is assigned at 000000. If any other starting address is used, the operator should modify the following procedures as appropriate.

4.3.1 Initial Check

Load address 000000 via the switch register or input device. If the address can be loaded (i.e., the proper address is displayed), examine the contents of location 0. Then, the contents of the CSR should be examined. If both address 0 and the CSR do not respond (i.e., the MS11-L does not return BUS SSYN L), it is likely that a fault exists in the data path control logic (Figure 3-11), or MSYN H (E62-3) is not reacting properly to BUS MSYN L. The address decode logic is probably faulty if only address 0 can be accessed; the address decode logic or timing logic may be at fault if only the CSR can be accessed.

4.3.2 Address Decode Check

Two test points are provided to check the address decode logic: CSR SEL L (T.P. 16) and MEM REQ L (T.P. 15). Load the CSR address, and check CSR SEL L (T.P. 16) with an oscilloscope. The signal should be low indicating that the address on the bus matches the assigned CSR address; its failure prevents the bus master from accessing the CSR. Examine address 0, and check MEM REQ L (T.P. 15) with an oscilloscope. The signal should go low approximately 30 ns after BUS MSYN L is asserted and should stay low until SSYN L is asserted (about the same time BUS SSYN L is returned). Signal MEM REQ L is used to initiate a memory data cycle and its failure prevents the bus master from accessing the MOS storage array. If MEM REQ L does not go low, load address 0, and check the inputs of E59 which are combined to generate MEM REQ L (Paragraph 3.6). Note that MSYN H should be low since BUS MSYN L is negated for a load address operation.

4.3.3 Timing Logic Check

The timing logic generates a sequence of signals that causes the execution of a memory data cycle or refresh cycle. With the processor halted, check DL 0 H (T.P. 3) with an oscilloscope. The signal should be a 230 ns positive pulse which should appear once every 14.5 μs (once for each refresh cycle). Signal DL 0 H is the input to the delay line which generates the timing chain; its failure prevents the bus master from accessing the MOS storage array, and prevents the execution of a memory refresh cycle. Note that a significant deviation in the pulse width of DL 0 H changes the timing of a memory data cycle or refresh cycle, and may result in malfunction of the MS11-L.

If DL 0 H is right, the following timing pulses should appear during a refresh cycle: ADD LAT L, DLT1 H, DL 2 L, DLT3 H, DLT6 H and DL 6 L (Figure 3-5). However, except for DLT3 H, the effect of these timing pulses on the memory logic is inhibited during a refresh cycle. Memory signals that are applicable to a refresh cycle are shown in Figure 3-8; memory signals that are applicable to the data cycles are shown in Figures 3-6 and 3-7. If DL 0 H has failed, check T.P. 20 and also refer to the refresh logic check (Paragraph 4.3.4). Test point T.P. 20 should be high as long as +5 V or +5 VBBU power is applied to the MS11-L (Paragraph 2.2.1.4). Signal DL 0 H is inhibited if T.P. 20 is low. Note that if T.P. 20 is low and the green LED is ON, the MS11-L should be replaced.

4.3.4 Refresh Logic Check

Check the signal at T.P. 18 with an oscilloscope (sheet 6 of the print set). This signal should oscillate with a period of about 14.5 μs and should have a negative pulse width of about 6 μs during each period. A refresh cycle cannot be initiated if this signal is absent and therefore, its failure can result in the random loss of data in the MOS storage array. Also check the outputs of the refresh address counter (E43) to ensure that it is incrementing.

4.3.5 Data Shorts Check

Using memory location 000000, check for data line shorts by depositing and examining successively the following data words: 000001, 000002, 000004, 000010, 000020, 000040, 000100, 000200, 000400, 001000, 002000, 004000, 010000, 020000, 040000, 100000. If no problems are found, check the address circuitry.

4.3.6 Address Circuits Check (A14–A01)

To check the address circuits, proceed as follows.

1. Deposit data word 000000 in the following locations: 000000, 000002, 000004, 000010, 000020, 000040, 000100, 000200, 000400, 001000, 002000, 004000, 010000, 020000, 040000.
2. Deposit 777777 in location 000000.
3. Examine location 000002. The data should be 000000 as deposited in Step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.
4. Deposit 777777 in location 000002.
5. Examine location 000004. The data should be 000000, as deposited in Step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.
6. Carry on the sequence begun in Step 2 (i.e., location 000004 is next).

4.3.7 Toggle in Memory Test

This test writes 0s, writes 1s, reads 1s, writes 0s, and reads 0s in a given location. It then decrements the address and repeats the above process over a given address range. Load the program starting at address 100000. Set the top address to 100000 and the bottom address to 0. This will check memory over the first 16K. If this test is successful, load the program starting at address 0. Set the top address to 177776. Set the bottom address to 100000. This will check memory over the second 16K, where the absolute loader will reside.

R0 = Highest Address
R1 = Lowest Address

```
 0    012700              MOV # TOP ADDRESS, R0
 2    TOP ADDRESS
 4    012701              MOV # LOW ADDRESS, R1
 6    LOW ADDRESS
10    005040        A:    CLR -(R0)
12    005110              COM (R0)
14    022710              CMP #177777, (R0)
16    177777
20    001005              BNE B
22    005110              COM (R0)
24    001003              BNE B
26    020001              CMP R0, R1
30    001365              BNE A
32    000000              HALT:    ;test complete
34    000000        B:    HALT:    ;error
```

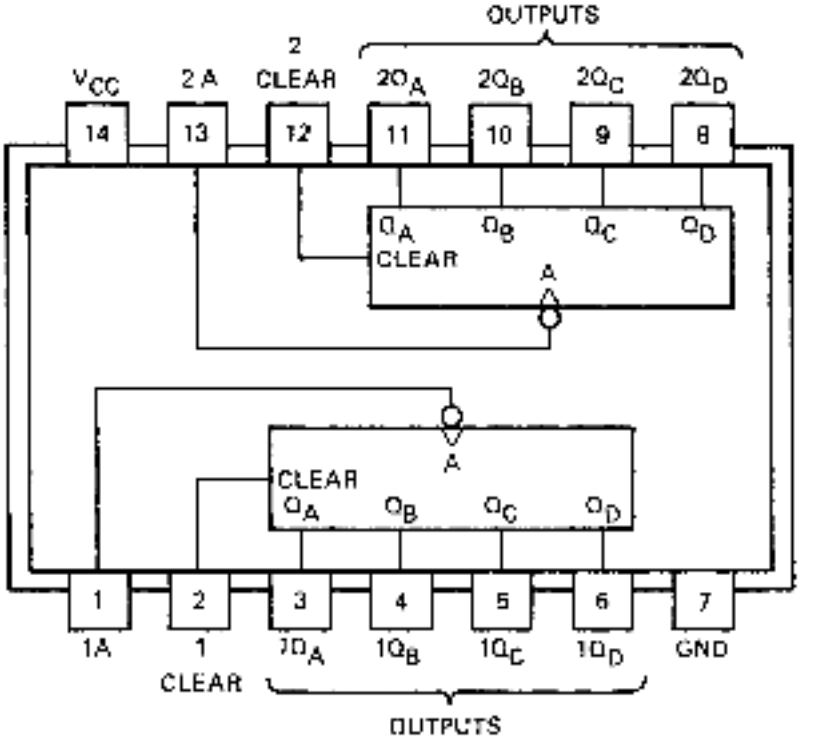
If no error is found, the program stops at location 32. If an error occurs, the program stops at location 34 and the failing address is contained in R0.

APPENDIX A
IC DESCRIPTIONS

This appendix contains descriptions of several integrated circuits (ICs) used in the MS11-L. The ICs described are listed below.

74LS393	Dual 4-Bit Binary Counter
74LS85	4-Bit Magnitude Comparator
74S280	9-Bit Odd/Even Parity Generator/Checker
74LS298	Quad 2:1 Multiplexer with Storage

74LS393 DUAL 4-BIT BINARY COUNTER



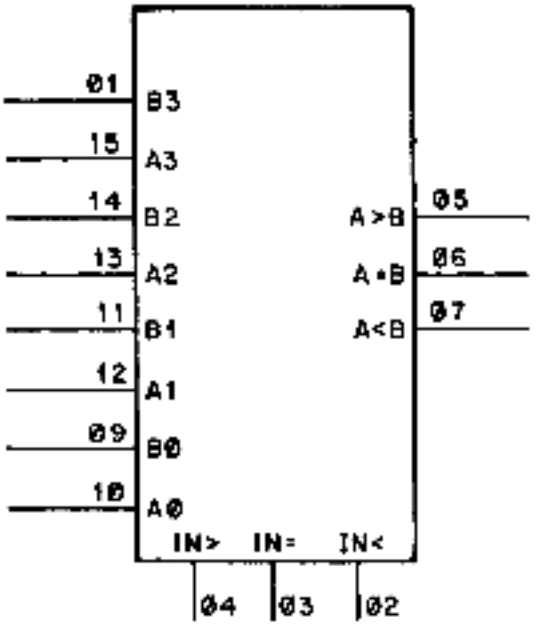
HIGH INPUT TO CLEAR RESETS ALL FOUR OUTPUTS LOW.
NEGATIVE EDGE OF INPUT TO "A" INCREMENTS THE COUNT.

COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

MA-3090

74LS85 4-BIT MAGNITUDE COMPARATOR



VCC = PIN 16
GND = PIN 08

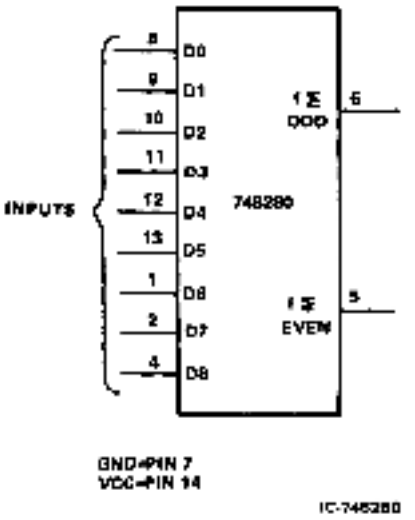
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE. H = high level, L = low level, X = irrelevant

IC-74S85

74S280 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

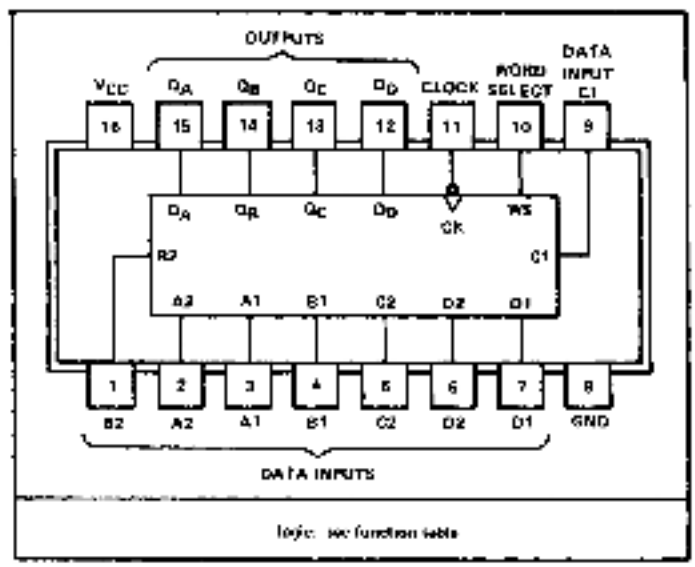


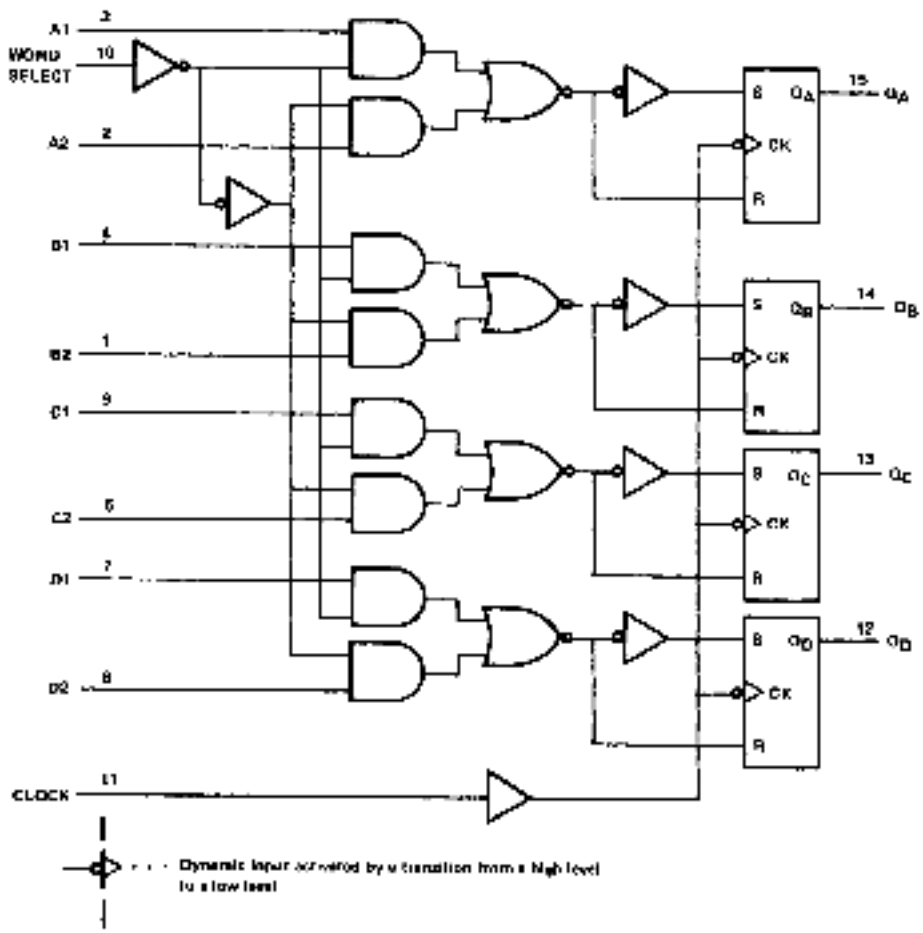
74LS298 QUAD 2:1 MULTIPLEXER WITH STORAGE

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from high to low level
a1, a2, etc. = the level of steady state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., established on the most-recent ↑ transition of the clock input





IC 74298

MS11-L MOS MEMORY TECHNICAL MANUAL
EK-MS11L-TM-001

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