digital

RL01/RL02 DISK SUBSYSTEM USER'S GUIDE

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RL01/RL02 DISK SUBSYSTEM USER'S GUIDE

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CHAPTER 1
INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides information on the capabilities, installation, operation, and programming of the RL01/RL02 Disk Subsystem. The basic subsystem comprises one RL11, RLV11 or RL8A controller and up to four RL01 or RL02 Disk Drives.

This manual is intended primarily for operating and programming personnel. Service should be performed only by qualified Digital field engineering and maintenance personnel. A prerequisite for understanding this manual is a basic knowledge of PDP 8 and PDP 11 processors and peripherals.

1.2 REFERENCE DOCUMENTS

Table 1-1 lists the documents that will be available to provide the information necessary for a complete understanding of the function, theory and maintenance of the RL01/RL02 Disk Drives and the RLV11/RL8-A Controllers. The Unibus and LSI-11 Bus are described in the *PDP11 Bus Handbook* (EB-17525). The Omnibus is described in the *PDP8/A Miniprocessor User's Manual* (EK-8A002-MM).

Table 1-1 Reference Documents

Title	Document No.
RL01/RL02 Disk Drive Technical Manual	EK-RL012-TM
RL01 Disk Drive Illustrated Parts Breakdown	EP-00016-IP
RL02 Disk Drive Illustrated Parts Breakdown	EP-00016-IP
RL01/RL02 Disk Subsystem Preventive Maintenance Manual *	EP-00008-PM
RL01/RL02 Disk Drive Pocket Service Guide	EK-RL012-PG
RL11 Controller Technical Description Manual	EK-0RL11-TD
RLV11 Controller Technical Description Manual	EK-RLV11-TD
RL8A OMNIBUS Controller Technical Manual	EK-0RL8A-TM

* NOTE – This document is only available to Digital Equipment Corporation Service personnel.

1.3 SUBSYSTEM DESCRIPTION

The RL01/RL02 mass storage subsystem is based on the RL01K/RL02K disk cartridges, the RL01/RL02 drive unit(s), and an appropriate controller such as the RL11 (PDP 11), RLV11 (LSI-11), or RL8A (PDP-8). The basic subsystem is illustrated in Figure 1-1.

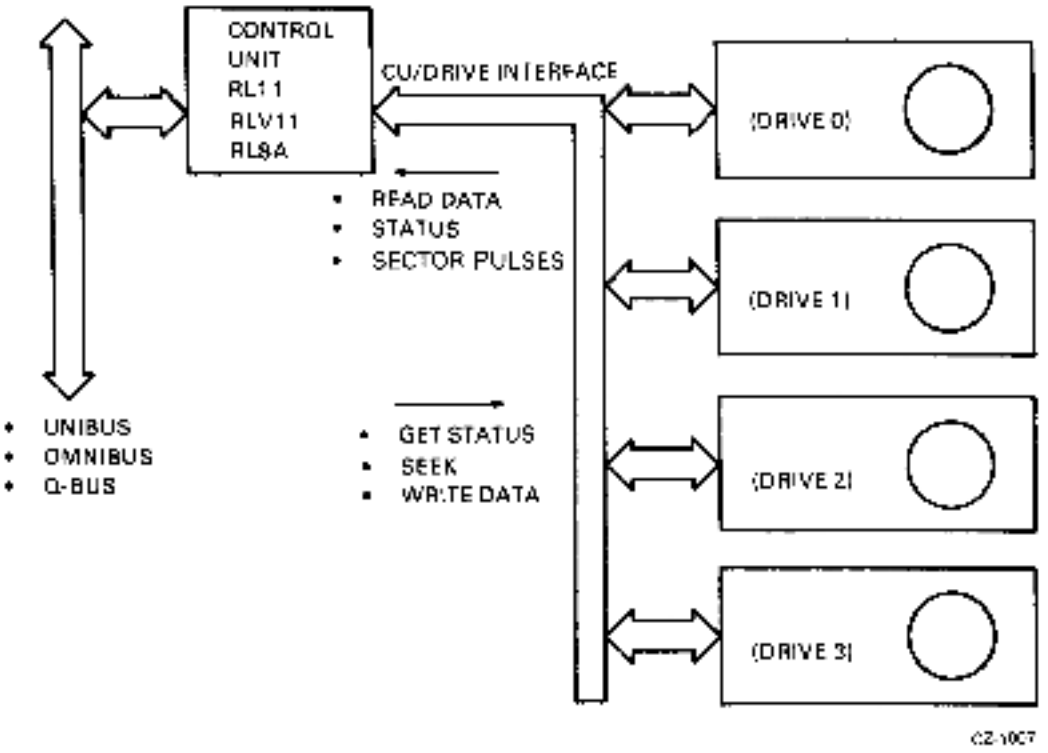


Figure 1-1 Typical RL01/RL02 Mass Storage Subsystem Configuration

1.3.1 RL01/RL02 Disk Drive

The RL01/RL02 drive unit is built into a chassis that slides out of the cabinet to allow the operator access to the top cover for loading and unloading of the disk cartridge. If the stops on the slide are manually released the chassis can be pulled farther out so that the rear top cover can be removed for servicing. The front panel contains operator controls and indicators.

The chassis contains a spindle, two read/write heads mounted on a positioner, logic modules, a power supply with an ac power cord and circuit breaker, a closed-loop clean air system, a cooling air system, appropriate safety interlocks, and connectors for the I/O cable(s).

The drive unit is shown in Figure 1-2.

The RL02 drive unit has a label reading "RL02" on the front panel. The RL01 drive currently does not have a label identifying it as an RL01.

1.3.2 RL Controllers

There are three controllers available for the RL01/RL02 subsystem. All can handle up to four drives and all feature Direct Memory Access (DMA) operation.

1.3.2.1 RL11 Controller Description — The RL11 Controller consists of a single, hex height Small Peripheral Controller (SPC) module designated M7762. It is used to interface the drive with the PDP-11 Unibus. The data is formatted in 16-bit words. This controller can handle any combination of up to four RL01 and/or RL02 Drives.

1.3.2.2 RLV11 Controller Description — The RLV11 Controller consists of two quad height modules designated M8013 and M8014. This controller interfaces the drive with the LSI-11 Bus. The data is formatted in 16-bit words. This controller can handle any combination of up to four RL01 and/or RL02 Drives.

1.3.2.3 RL8A Controller Description — The RL8A Controller consists of a single, hex-height module designated M8433. It is used to interface the drive with the PDP 8 Omnibus. The data can be formatted in either 8 bit bytes or 12 bit words. This controller has a jumper-determined choice of handling RL01 or RL02 Drives. However, in the RL02 jumpered configuration, it can handle any combination of up to four RL01 and/or RL02 Drives.

1.3.3 RL01K/RL02K Disk Cartridge

The RL01K or RL02K is a removable, top-loading 5440-type disk cartridge that is formatted in a manner unique to the RL01/RL02 subsystem. Both cartridges contain a single platter. The RL01K cartridge has a capacity of 5.2 megabytes of user data, and the RL02K cartridge will hold 10.4 megabytes of data. Both sides of the platter are used for data. There are 256 tracks on each RL01K platter surface and 512 tracks on each RL02K platter surface. Each track is divided into 40 sectors. Each sector contains 256 bytes of data. The last track of the last surface is reserved for the cartridge serial number and bad sector information. Head positioning servo information and header information are prerecorded at the factory and cannot be reformatted in the field. This information, along with the data, is read by the read/write heads but the internal logic of the drive unit protects the servo and header information from being overwritten.

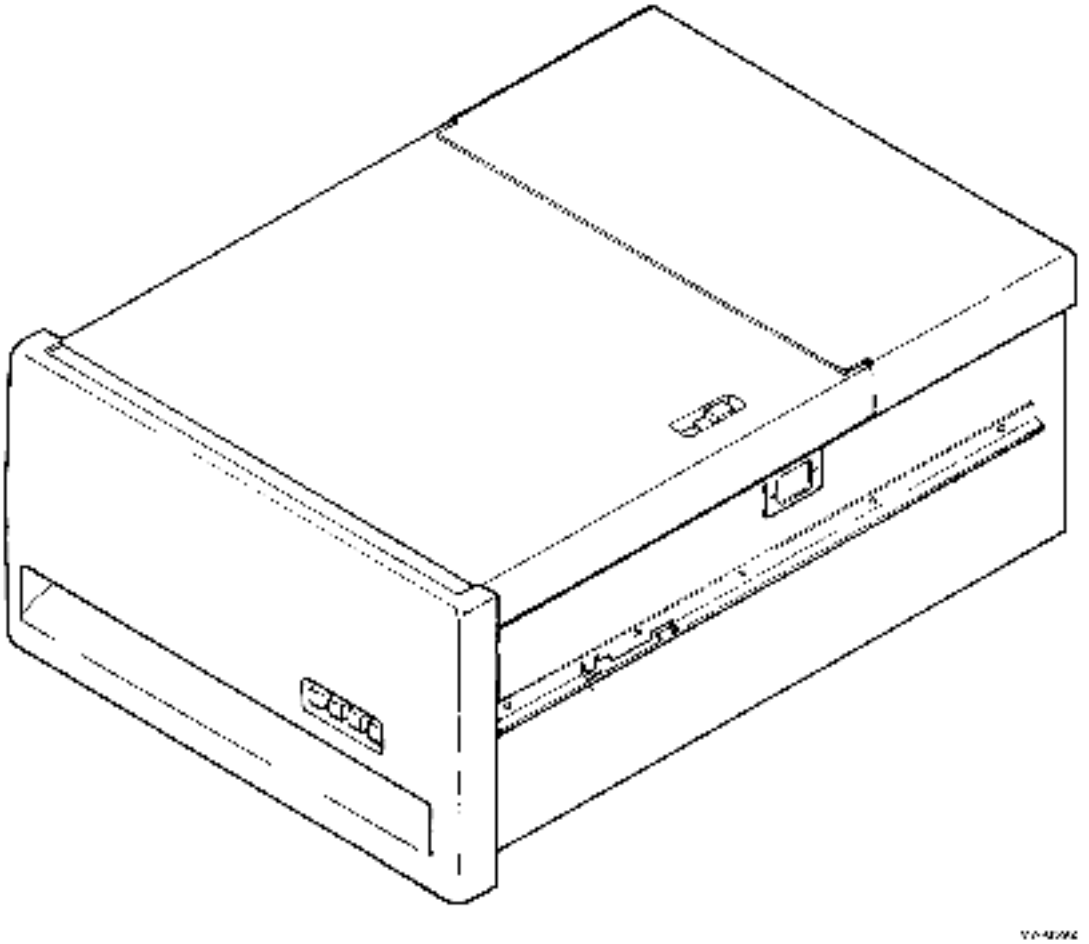


Figure 1-2 RL01/RL02 Disk Drive

1.3.3.1 Interchangeability – The RL01K and RL02K Disk Cartridges are not functionally interchangeable although they are physically interchangeable. It is possible to mount an RL01K cartridge on an RL02 drive, for example, but proper operation will not occur. An RL01K cartridge written on an RL01 unit can be read on any other RL01 unit even if that unit is controlled by a different type of controller. The only limitation to this interchangeability is that if an RL8A controller is used to write data and the cartridge is to be used on a drive controlled by an RL11 or an RLV11 controller, the RL8A must use an 8-bit byte mode of operation.

An RL02K cartridge written on an RL02 unit can be read on any other RL02 unit (assuming the same conditions mentioned above).

1.3.3.2 Sector Format – As shown in Figure 1-3, each sector contains:

- Servo information for head positioning
- Header (address) information
- Data – 128 words of 16 bits each, OR
  256 bytes of 8 bits each, OR
  170 words of 12 bits each

Only the data portion of a sector can be written by the user. The servo and header information is protected by the drive logic and controller to ensure disk integrity and cannot be written in the field.

Each sector starts with a sector pulse that is produced by a sector transducer mounted on the drive unit. It senses the sector notches that are machined into the hub of the disk cartridge.

During the time that sector notch passes by the sector transducer, the heads detect two servo pulse bursts (S1 and S2) that are prerecorded on the platter. These servo bursts are used by the drive logic for head positioning.

Following the servo pulse bursts is the header. It consists of:

- A preamble of three words – 47 "0" bits and one "1" bit
- A word that contains the address – sector, head, and cylinder
- A word of all zeroes
- A word containing information created by the Cyclic Redundancy Check (CRC) logic
- A one-word postamble of all zeroes

Following the header is the user writable data area. It consists of:

- A preamble of three words – 47 "0" bits and one "1" bit
- Data (128 words of 16 bits or 256 bytes of 8 bits or 170 words of 12 bits)
- A word containing CRC-generated information
- A one-word postamble of all zero bits

Following each sector is a period of idle time that is simply a wait for the next sector pulse.

In addition to the data tracks, there are tracks both inside and outside of the data area that contain unique servo signals that define those areas as guard bands. If the read/write heads attempt to enter a guard band, the drive logic causes the positioner to retreat from the guard band and return to the data area.

The disk has a nominal rotational speed of 2400 rev/min. Therefore, the time for one revolution is 25 milliseconds. Since the revolution is divided into 40 sectors, the duration of each sector is 625 microseconds. This 625 microsecond period is divided into non-data (sector pulse, header, idle time) time and data time. The data time period is 500 microseconds. Thus, the data is transferred in 500 microsecond bursts that occur every 625 microseconds.

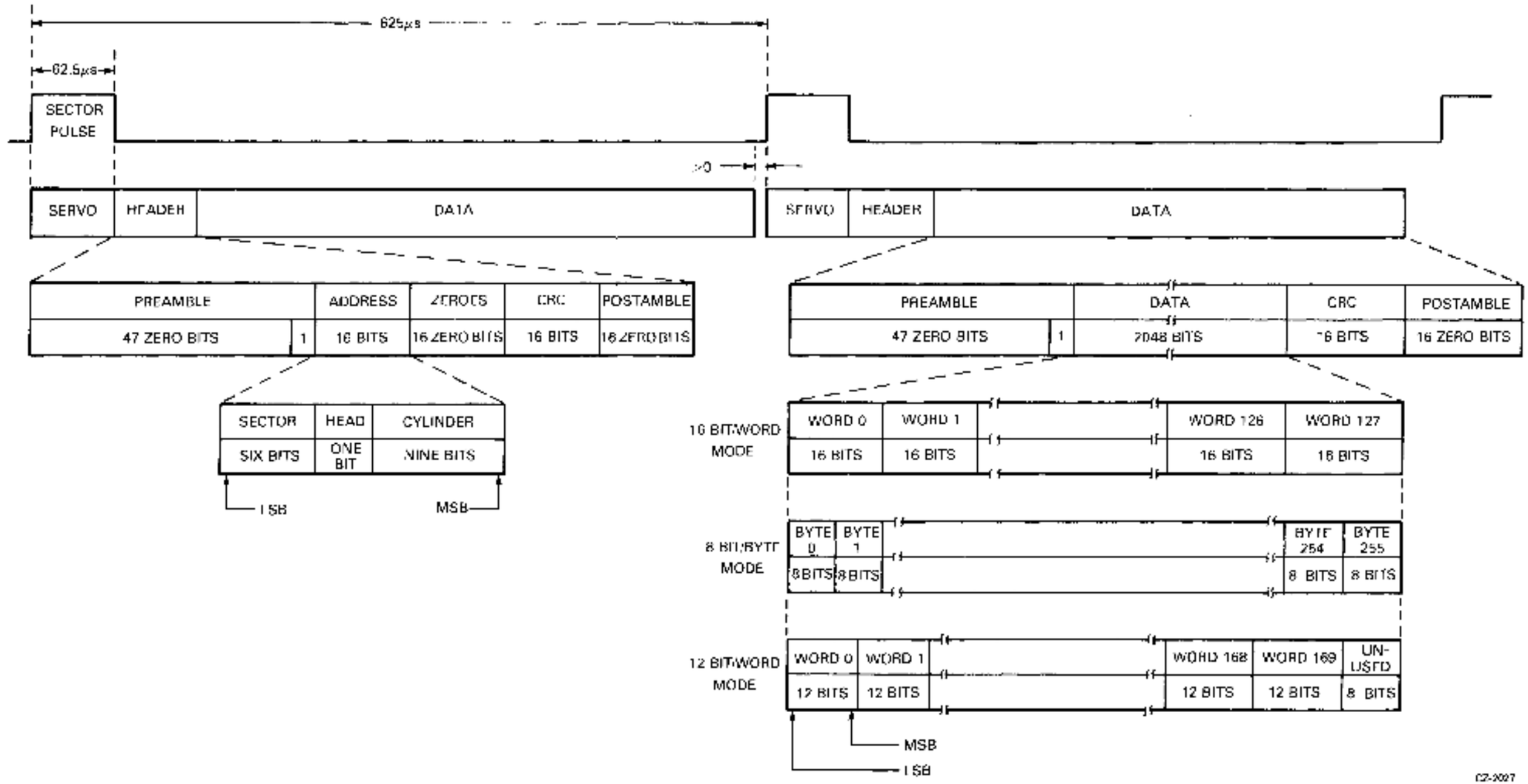


Figure 1-3 RL01/RL02K Disk Cartridge Format

For 16 bit word mode there are 128 words of data in a sector so the peak transfer rate is 3.9 microseconds per word and the average transfer rate is 4.9 microseconds per word.

For 8 bit bytes (256 bytes per sector), the peak transfer rate is 1.9 microseconds per byte and the average transfer rate is 2.4 microseconds per byte.

For 12 bit word mode (170 words per sector), the peak transfer rate is 2.9 microseconds per word and the average transfer rate is 3.7 microseconds per word.

1.4 SECTOR LOCATION

The RL01K/RL02K Disk Cartridges do not have a physical index notch (occuring once per revolution) machined into the hub as some cartridges do. The controller determines the rotational position of the disk cartridge by reading, from the header, the sector address as well as the head (surface) and cylinder (track) addresses. Thus, the cartridge does not need a physical index. The sectors are relocated to optimize the data transfer rate when it becomes necessary to perform a seek during a data transfer.

A head switch to the other surface is considered a seek because the RL01/RL02 subsystem uses servo information that is recorded on each track. The newly selected head will position itself over the center of the track. There is no hardware-controlled implicit seek on the RL01/RL02 subsystem. All seeks, including spiral (mid-transfer) seeks, must be programmed into the software. The correct head must be selected and positioned over the correct track by a seek operation before the software can initiate a data transfer.

When the end of a track is reached, and the data transfer has not been completed, the software must do one of two things. It must switch to the head that is over the corresponding track on the other surface (6.5 milliseconds average, 8 milliseconds maximum) or the software must issue a seek to the next cylinder (15 milliseconds). If the head is to be switched also, the seek and the head switching are normally combined. Once the unit has completed the seek operation, the software can continue the data transfer.

To reduce the rotational latency following a head switch seek, surface one is offset by 17 sectors from surface zero. The eight milliseconds head switch corresponds to 13 sectors of this offset and the additional four sectors allow for software overhead.

To reduce the rotational latency following a one cylinder seek (with head switch), surface zero of a cylinder is offset by 29 sectors from surface one of the previous cylinder. The 15 millisecond seek time takes 24 sectors of this offset and five more sector times are allowed for software overhead.

These two offset patterns are illustrated in Figures 1-4 and 1-5.

1.5 BAD SECTOR FILE

The Bad Sector File is a list of all bad sectors found on an RL01K/RL02K Disk Cartridge. It also contains the cartridge serial number. The operating system uses this information to avoid allocating bad sectors to a user's files.

If there is an error in a header, or if there are 16 consecutive read/write errors within one sector, that sector is defined as a bad sector.

This file is recorded on surface 1, track 255 (decimal) of an RL01K cartridge, and surface 1, track 511 (decimal) of an RL02K cartridge. The file consists of 40 sectors of 128 words each. Figure 1-6 shows the format of the Bad Sector File.

There is room in the file for 128 entries written by the factory and for 128 entries that can be written in the field if bad sectors develop during field use.

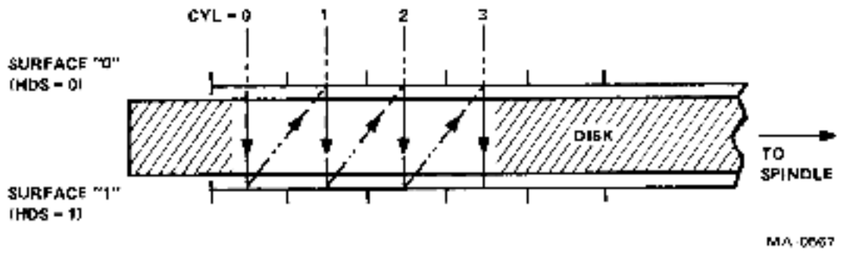
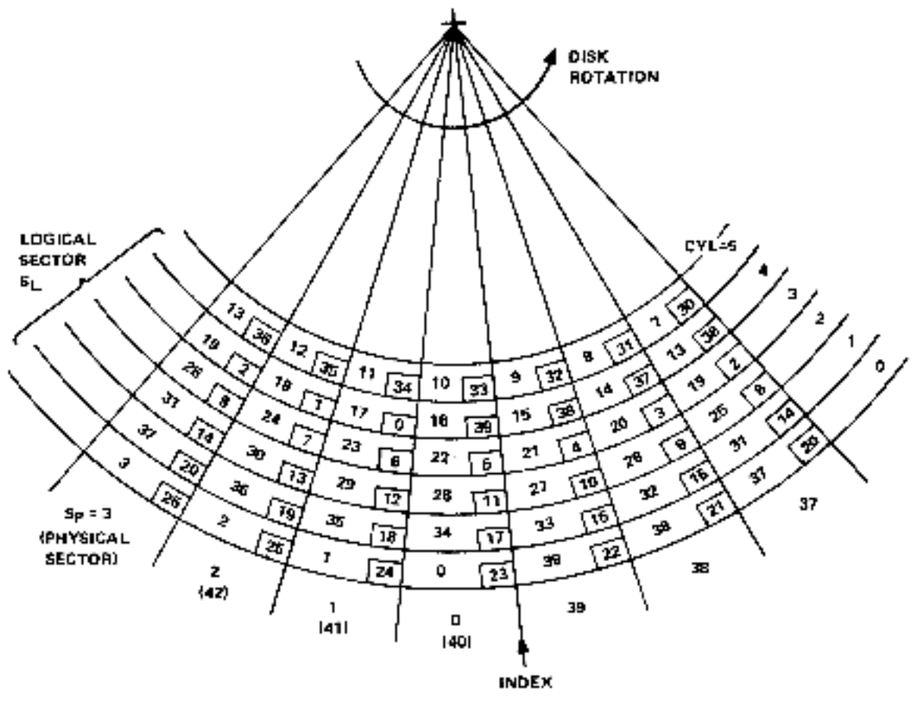


Figure 1-4 Access Method for Sequential Transfers



NOTE:
NUMBERS IN BLOCKS REFER TO HEAD 1.

MA-0578

Figure 1-5 Sector Relocation

BAD SECTOR FILE

SECTOR	CONTENTS
0 1	FACTORY WRITTEN BAD SECTOR INFO
2 3	ALL ONES
4 5	DUPLICATE OF SECTORS 0, 1
7	ALL ONES
8 9	DUPLICATE OF SECTORS 0, 1
10 11	ALL ONES
12 13	DUPLICATE OF SECTORS 0, 1
14 15	ALL ONES
16 17	DUPLICATE OF SECTORS 0, 1
18 19	ALL ONES
20 21	FIELD WRITTEN BAD SECTOR INFO
22 23	ALL ONES
24 25	DUPLICATE OF SECTORS 20, 21
26 27	ALL ONES
28 29	DUPLICATE OF SECTORS 20, 21
30 31	ALL ONES
32 33	DUPLICATE OF SECTORS 20, 21
34 35	ALL ONES
36 37	DUPLICATE OF SECTORS 20, 21
38 39	ALL ONES

LAST CYLINDER LAST SURFACE

TWO SECTORS

256 16 BIT WORDS 125 ENTRIES

WORD	MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB 0
0	ZERO	5 LEAST SIGNIFICANT OCTAL DIGITS OF CARTRIDGE SERIAL NUMBER														
1	ZERO	5 MOST SIGNIFICANT OCTAL DIGITS OF CARTRIDGE SERIAL NUMBER														
2	ZEROES															
3	ZEROES															
FIRST BAD SECTOR ENTRY 4	ZEROES							CYLINDER ADDRESS								
5	ZEROES							HEAD	ZEROES		SECTOR ADDRESS					
SECOND BAD SECTOR ENTRY 6	SAME FORMAT AS FIRST BAD SECTOR ENTRY															
7																
125th BAD SECTOR ENTRY 252	SAME FORMAT AS FIRST BAD SECTOR ENTRY															
253																
254	ALL ONES															
255	ALL ONES															

NOTE: UNUSED BAD SECTOR ENTRIES ARE ALL ONES

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Figure 1-6 Bad Sector File Format

1.6 RL01/RL02 SPECIFICATIONS

The following tables list the specifications of the RL01/RL02 drives and the RL01K/RL02K cartridges.

Table 1-2 RL01/RL02 Disk Drive Physical and Environmental Specifications
Table 1-3 RL01/RL02 Disk Drive Operational Specifications
Table 1-4 RL01K/RL02K Disk Cartridge Specifications

Table 1-2 RL01/RL02 Disk Drive
Physical and Environmental Specifications

Characteristics	Specifications
Width	Compatible with 19 inch RETMA rack
Depth	63.5 cm (25 in) behind bezel
Height	26.52 cm (10.44 in)
Weight	34 kg (75 lb)
Mounting	The drive mounts on chassis slides
Power Source	90-127 Vac (47.5-63 Hz) 180-256 Vac (47.5-63 Hz) (Manually selectable)
Input Power	160 W max at 115 Vac, 60 Hz
Power Factor	Greater than 0.85
Starting Current	3.5A (rms) max @ 90 Vac/47.5-63 Hz 5.0A (rms) max @ 127 Vac/47.5-63 Hz 1.75A (rms) max @ 180 Vac/47.5-63 Hz 2.5A (rms) max @ 254 Vac/47.5-63 Hz
Heat Dissipation	546 Btu/hr max
Power Cord and Connector	A molded line cord compatible with the drive operating voltage and the 8a1 power control for 120 Vac is attached to the drive. The power cord is 2.74 m (9 ft) long and the plug is NEMA 5-15P. The 230 Vac plug to be attached to high voltage drives is NEMA 6-15P.
Safety	The RL01/RL02 Disk Drive is U.L. listed and CSA certified.
Interlocks	Interlocks are used where potential exists for damage to drive, media, operators, or service personnel.

Table 1-2 RL01/RL02 Disk Drive
Physical and Environmental Specifications (Cont)

Characteristics	Specifications
Temperature/Humidity	**Operating:** Temperature: 10° C (50° F) to 40° C (104° F) Derate temperature at 1.8° C/1000 meters (1° F/1000 feet) Relative Humidity: 10 to 90 percent with maximum wet bulb temperature 28° C (82° F) and minimum dew point 2° C (36° F) **Nonoperating:** Temperature: −40° C (−40° F) to 66° C (151° F) Relative Humidity: 10 to 95 percent, noncondensing
Altitude	**Operating:** 2440 m (8,000 ft) max **Nonoperating:** 9144 m (30,000 ft) max
Shock	**Operating:** Half sine shock pulse of 10 gravity peak of 10 ± 3 ms duration applied once in either direction of three orthagonal axes (3 pulses total) **Nonoperating:** Half sine shock pulses of 40 gravity peak of 30 ± 10 ms duration perpendicular to each of six package surfaces.
Vibration	**Operating:** Sinusoidal vibration (sweep rate 1 octave/min) 5-50 Hz, 0.002 in displacement amplitude 50-500 Hz, 0.25 gravity peak 500-50 Hz, 0.25 gravity peak 50-5 Hz, 0.002 in displacement amplitude **Nonoperating:** Vertical Axis Excitation – 1.40 gravity (rms) overall from 10 to 300 Hz; power spectral density of 0.029 g^2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 300 Hz Longitudinal and Lateral Axis Excitation – 0.68 gravity (rms) overall from 10 to 200 Hz; power spectral density of 0.007 g^2/Hz from 10 to 50 Hz, with 8 dB/octave rolloff from 50 to 200 Hz
EMI	Meets DEC Standard 102, Section 7.
Dust	The drive will operate in an ambient atmosphere of less than 5 million particles 0.5 microns or larger per cubic foot of air. The drive is intended to run in a light industry or cleaner environment.
Attitude	Maximum pitch: ± 15 degrees Maximum roll: ± 15 degrees

Table 1-3 RL01/RL02 Disk Drive Operational Specifications

Characteristics	Specifications
General	Linear bit density: 147 bits/mm (3725 bits/in) at innermost track 16 bit words per sector: 128 Number of sectors per track: 40 Track density: 4.9/mm (125/in) for RL01K, 9.8/mm (250/in) for RL02K Number of tracks per surface: 256 for RL01K, 512 for RL02K Number of surfaces: 2 Formatted capacity (megabytes): 5.2 for RL01K, 10.4 for RL02K Encoding method: Modified Frequency Modulation (MFM)
Transfer Rate (Unbuffered Values)	Bit rate: 4.1 megabits/second ± 1 percent Bit cell width: 244 ns ± 1 percent Word transfer rate (16 bit words): 256 kilowords/second ± 1 percent
Latency	Rotational frequency: 2400 rev/min ± 0.25% Average latency: 12.5 ms ± 0.25% Maximum latency: 25.0 ms ± 0.25%
Seek Time	Average seek time: 55 ms max (85 tracks for RL01, 170 tracks for RL02) One cylinder/track seek time: 15 ms max Maximum seek time: 100 ms max (256 tracks for RL01, 512 tracks for RL02)
Start/Stop Time	Start time: 45 seconds Stop time: 30 seconds
Data Format	Refer to Figure 1-3

Table 1-4 RL01K/RL02K Disk Cartridge Specifications

Characteristics	Specifications
Operating Environment	The cartridge will operate over a temperature range of 4° C to 48° C (40° F to 120° F), at a relative humidity of 8 to 80 percent. The wet bulb reading must be less than 25° C (78° F). Before a cartridge is placed in operation, it should be conditioned within its cover for a minimum of 2 hours in the same environment as that in which the disk drive is operating. (The above specified ranges do not necessarily apply to the disk drive)
Storage Environment	The cartridge should be stored at a temperature between −40° C to 65° C (−40° F to 150° F), with a wet bulb reading not exceeding 29° C (85° F). For wet bulb temperatures between 0.56° C and 29° C (33° F and 85° F) the disk cartridge will withstand a relative humidity of 8 to 80 percent. The stray magnetic field intensity shall not exceed 50 Oe.
Dimensions (Cartridge)	The external diameter of the top cover is 38.35 cm (15.1 in).
	The external diameter of the protection cover is 37.03 cm (14.58 in).
	The external height of the cartridge is 6.19 cm (2.44 in).
Maximum Speed	The rotating parts of the disk cartridge are capable of withstanding the effect of stress created while rotating at 2,500 rev/min.
Track Geometry	There are 256 discrete concentric tracks per data surface for the RL01K, 512 tracks per data surface for the RL02K.
Identification of Data Location	Data Track Identification – Data tracks are numbered by consecutive decimal numbers (000-255, RL01K; 000-511, RL02K) starting at the outermost data track of each data surface.
	Data Surface Identification – The upper data surface is numbered 0 and the lower surface is numbered 1, to correspond with the head numbers.
	Cylinder Address – A cylinder is defined as both data tracks (on either surface) with a common data track identification.
	Data Track Address – A 16-bit word defines the data track address. Bits 0-5 define the sector, bit 6 defines the surface, and bits 7-15 define the cylinder address. This information is in word 1 of each sector's header.

CHAPTER 2
INSTALLATION

2.1 SITE PREPARATION AND PLANNING

This chapter describes power, space, environmental, cabling and safety requirements that must be considered before installation of the RL01/RL02 Disk Subsystem.

2.1.1 Environmental Considerations

The RL01/RL02 Disk Subsystem is designed to operate in a business or light industry environment. Although cleanliness is an important consideration in the installation of any computer system, it is particularly crucial for proper operation of a disk drive. The RL02K-RL02K Disk Cartridge is not sealed while being loaded and is therefore vulnerable to dust or smoke particles suspended in the air, as well as fingerprints, hair, lint, etc. These minute obstructions can cause head crashes, resulting in severe damage to the read/write heads and disk surfaces.

2.1.1.1 Cleanliness – The RL01/RL02 Disk Drives can operate in an ambient with less than one million particles per cubic foot of air which are 0.5 micron or larger in diameter. The drive contains a filter system which, under these conditions, maintains the particle count within the cartridge below 100 particles per cubic foot.

2.1.1.2 Space Requirements – Provision should be made for service clearances of 1 m (36 in) at the front and rear of the rack or cabinet in which the drive is mounted and 1 m (36 in) at either side.

Storage space for the RL01K/RL02K cartridges should also be made available. Each cartridge has a diameter of approximately 38 cm (15 in) and a height of approximately 6 cm (2.5 in).

CAUTION

RL01K/RL02K Disk Cartridges must never be stacked on top of each other. A designated shelf area or specially designed disk cartridge storage unit is recommended (see the DIGITAL Supplies and Accessories Catalog).

2.1.1.3 Floor Loading – The weight of the RL01/RL02 Disk Drive alone is 34 kg (75 lb), which will not place undue stress on most floors. However, the added weight of the rack or cabinet as well as the number of drives to be installed should be considered in relation to the weight of existing computer systems. Possible future expansion should also be a consideration.

2.1.1.4 Heat Dissipation – The heat dissipation of each RL01/RL02 Disk Drive is 546 Btu/hour maximum. The approximate cooling requirements for the entire system can be calculated by multiplying this figure by the number of drives, adding the result to the total heat dissipation of the other system components, and then adjusting the total figure to compensate for personnel, cooling system efficiency, etc. It is advisable to allow a safety margin of at least 25 percent above the maximum estimated requirements.

2.1.1.5 Acoustics – Most computer sites require at least some degree of acoustical treatment. However, the RL01/RL02 Disk Subsystem should not contribute unduly to the overall system noise level. Ensure that acoustical materials used do not produce or harbor dust.

2.1.1.6 Temperature – The RL01/RL02 Disk Subsystem will operate over a temperature range of 10° C (50° F) to 40° C (104° F). The maximum temperature gradient is 16.6° C (30° F) per hour. The nonoperating temperature range is from -40° C (-40° F) to 66° C (151° F).

2.1.1.7 Relative Humidity – Humidity control is important for proper operation of any computer system since static electricity may cause memory errors or even permanent damage to logic components. The RL01/RL02 Disk Subsystem is designed to operate within a relative humidity range of 10 to 90 percent, with a maximum wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F). The nonoperating relative humidity range is from 10 to 95 percent, with a maximum wet bulb temperature of 46° C (115° F).

2.1.1.8 Altitude – Computer systems operating at high altitudes may have heat dissipation problems. Altitude also affects the flying height of read/write heads in disk drives. The maximum altitude specified for operating the RL01/RL02 Disk Subsystem is 2440 M (8000 ft). Also, the maximum allowable operating temperature is reduced by a factor of 1.8° C per 1000m (1° F per 1000 ft) above sea level. Thus, the maximum allowable operating temperature at 2440 m (8000 ft) would be reduced to 36°C (96° F).

2.1.1.9 Power and Safety Precautions – The RL01/RL02 Disk Subsystem presents no unusual fire or safety hazards to an existing computer system. AC power wiring should be checked carefully, however, to ensure that its capacity is adequate for the added load as well as for any possible expansion. The RL01/RL02 Disk Drive is UL listed and CSA certified.

2.1.1.10 Radiated Emissions – Any source of electromagnetic interference (EMI) that is near the computer system may affect the operation of the processor and its related peripheral equipment. Common EMI sources that are known causes of failures include:

- Thunderstorms
- Broadcast stations
- Radar
- Mobile communications
- High voltage power lines
- Power tools
- Arc welders
- Vehicle ignition systems
- Static electricity

The effect of radiated EMI emissions on a computer system is unpredictable. Thus, grounding plays an important role in protecting the circuits used in disk drive subsystems.

To help reduce the effects of known high-intensity EMI emissions perform the following actions:

- Ground window screens and other large metal surfaces.
- Ensure that the overall computer system is grounded properly (refer to Paragraph 2.1.5, Grounding Requirements).
- Provide proper storage (metal cabinets with doors) for disk cartridges.

2.1.1.11 Attitude/Mechanical Shock – Performance of the RL01/RL02 Disk Subsystem will not be affected by an attitude where maximum pitch and roll do not exceed 15 degrees.

The subsystem is designed to operate while a half-sine shock pulse of 10 gravity peak and 10 + 5 ms duration is applied once in either direction of three orthagonal axes (three pulses total).

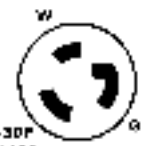
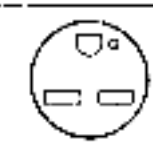
2.1.2 Options

The RL01/RL02 Disk Drive can be shipped with various controllers (for Unibus, Omnibus and LSI 11 Bus computer systems), and can be configured for 115 Vac or 230 Vac operation.

Table 2-1 shows saleable RL01/RL02 subsystem options. Table 2-2 shows RL01/RL02 cabinet options.

Table 2-1 Saleable RL01/RL02 Subsystem Options

Option Number	Description
RL01A	RL01 unit, BC20J I/O cable, chassis slide and mounting hardware
RL02A	RL02 unit, BC20J I/O cable, chassis slide and mounting hardware
RL01-AK	RL01-A (drive), RL01K-DC (cartridge)
RL02-AK	RL02-A (drive), RL02K-DC (cartridge)
RL01K-DC	RL01 Data Cartridge
RL02K-DC	RL02 Data Cartridge
RL11-AK	RL01-AK, RL11 Controller, BC06R, terminator
RL211-AK	RL02-AK, RL11 Controller, BC06R, terminator
RLV11-AK	RL01-AK, RLV11 Controller, BC06R, terminator
RLV21-AK	RL02-AK, RLV11 Controller, BC06R, terminator
RL8A-AK	RL01-AK, RL8-A Controller, BC80J, terminator
RL28A-AK	RL02-AK, RL8-A Controller, BC80J, terminator

SOURCE	PLUG	RECEPTACLE	USED ON	
120V 15A 1-PHASE	 HUBBEL #5269-C NEMA # 5-15P DEC # 90-08838	 #5362 5-15R 12-05361	ALL 120V TABLE-TOP COMPUTERS STANDARD 120V LOW-CURRENT DISTRIBUTION. 120V TU10 UNITS MO81 120V TERMINAL DEVICES	POWER CONTROLLER 861-F
120/208V 30A 3-PHASE Y	 HUBBEL #2611 NEMA # L5-30P DEC # 12-11193	 #2610 L5-30R 12-11194	ALL 120V STANDARD CABINET MOUNTED EQPT	POWER CONTROLLER 861-C
120/208-240V 20A 2-PHASE or 120/208V 20A 3-PHASE Y	 HUBBEL #2411 NEMA # L14-20P DEC # 12-11046	 #2410 L14-20R 12-11046	120V PDP 11/45 PRO CESSOR CABINET ONLY.	POWER CONTROLLER 861-A
120/208V 20A 3-PHASE Y	 HUBBELL #2511 NEMA # L21-20P DEC # 12-11206	 #2510 L21-20R 12-11210	60 Hz RM 10 DRUM 60 Hz RP02/RP03/ RP04. RP05. RP06	
240V 15A 1-PHASE	 NEMA # 6-15P DEC # 90-08863	 6-15R 12-11209	ALL 240V TABLE-TOP COMPUTERS STANDARD LOW-CURRENT 240V DISTRIBUTION MOST 240V TERMINAL DEVICES 240V TU10	
240V 20A 1-PHASE	 HUBBEL #2321 NEMA # L6-20P DEC # 12-11192	 #2320 L6-20R 12-11191	ALL 240V STANDARD CABINET MOUNTED EQUIPMENT.	POWER CONTROLLER 861-B
240/416V 30A 3-PHASE Y	 NEMA # — NOT NEMA DEC # 12-09010	 NOT NEMA 12-11359	60 Hz RM10 DRUM 60 Hz RP02/RP03/ RP04	
120V 30A 1-PHASE	 HUBBEL #2811 NEMA L21-30P DEC 12-12314	 #2810 L21-30R 12-12316	PDP11/70 PROCESSOR PDP 11/70 MEM VAX-11/780 PROCESSOR	POWER CONTROLLER 861-D

CP-1968

Figure 2-2 Approved Electrical Plugs and Receptacles

2.1.4 Installation Constraints

The route from the receiving area to the installation site that the equipment will travel should be studied in advance to ensure problem-free delivery. Among the considerations are:

- Height and location of loading doors
- Size, capacity, and availability of elevators
- Number and size of aisles and doors en route
- Bends or obstructions in hallways.

2.1.5 Grounding Requirements

Each cabinet of a DIGITAL computer system is equipped with ground lug terminals that should be connected to a low-impedance earth ground by No. 4 AWG (5 mm/0.20 in) copper wire or stranded No. 4 AWG welding cable. A Burndy QA4C-B solderless lug (or equivalent) is recommended for terminating the cable. DIGITAL supplies a standard grounding conductor with each I/O and memory cabinet.

When two cabinets are bolted together, DIGITAL bonds them electrically with a No. 4 AWG conductor (5 mm/0.20 in) or by several copper mesh straps connected between the cabinet frames. Use the green/yellow conductor in the power cord for safety ground connection.

The green/yellow grounding wire in the power cable must be returned to ground at the system power distribution panel. Note that the green/yellow wire is a non-current carrying conductor, not a neutral conductor.

For information about system grounding considerations, see the *DIGITAL Site Preparation Guide* (EK-OCORP-SO-003)

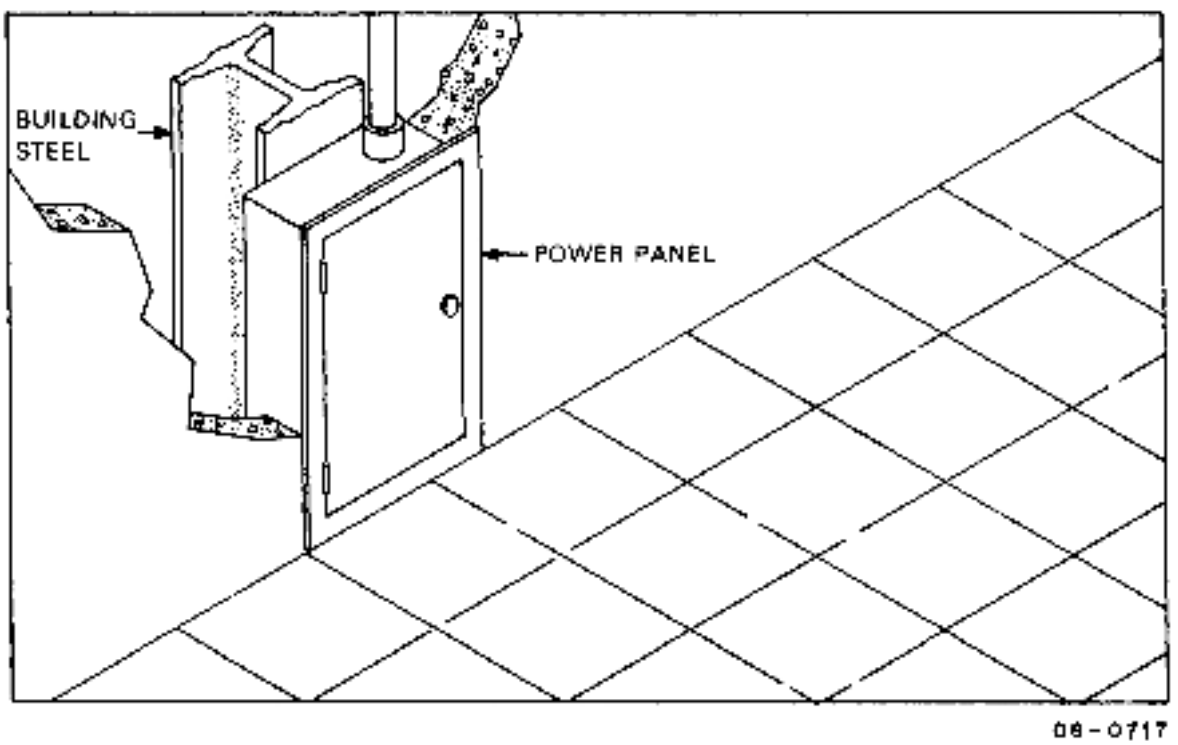


Figure 2-3 Power Panel Grounded To Building Frame

Where neither scheme is possible, a metal area (comprising the power panel, the conduit, and a metal plate) of at least 1 m^2 (10 ft^2) that is in contact with masonry must be connected to the green ground wire (Figure 2-4). The connecting wire must not exceed 1.5 m (5 ft) in length and should be at least a No. 12 AWG (2mm).

When two cabinets are bolted together, DIGITAL bonds them electrically with a No. 4 AWG conductor (5 mm/0.20 in) or by several copper mesh straps connected between the cabinet frames.

After the grounding system is installed, it is advisable to take a voltage reading between the cabinet frame and the nearest grounded object. NBFU No. 70 (published by the National Bureau of Underwriters) provides further details regarding preferred grounding procedures.

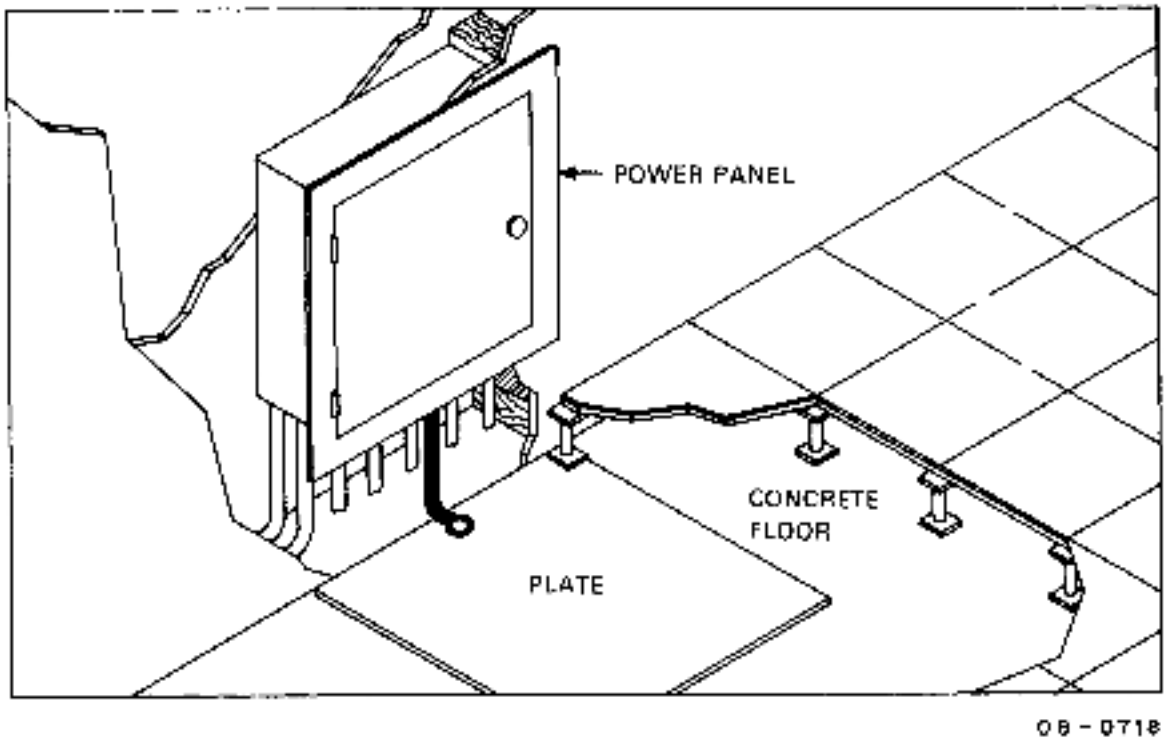


Figure 2-4 Power Panel Grounded To Metal Plate

2.2 AC CABLING

Computer equipment requires a power source with a minimum number of voltage and frequency disturbances. Line voltage disturbances greater than 1/4 cycle (measured at the receptacle during system operation) are undesirable.

DIGITAL power wiring conforms to Underwriters Laboratories, Inc., Handbook UL No. 478, National Electrical Code standards, and the type II requirements of the National Fire Protection Association (NFPA 70). This means that in the United States the wire used as equipment ground is green, or green with a yellow stripe; it carries no load current (except in emergency), but does carry leakage current. No equipment is permitted to leave DIGITAL that does not have a grounding connection to its frame.

The grounded conductor is light grey or white. It must not be used to ground equipment. Its purpose is to conduct current.

Lines 1, 2, and 3 in a typical 60 Hz power system (Figure 2-5) are represented by black, red, and blue wires, respectively, and phase rotation is in that order.

CAUTION

Where no grounded wire can be guaranteed, it must not be assumed. There are some 115 V/60 Hz systems within the United States where neither side of the line is grounded (115 V 3-phase delta).

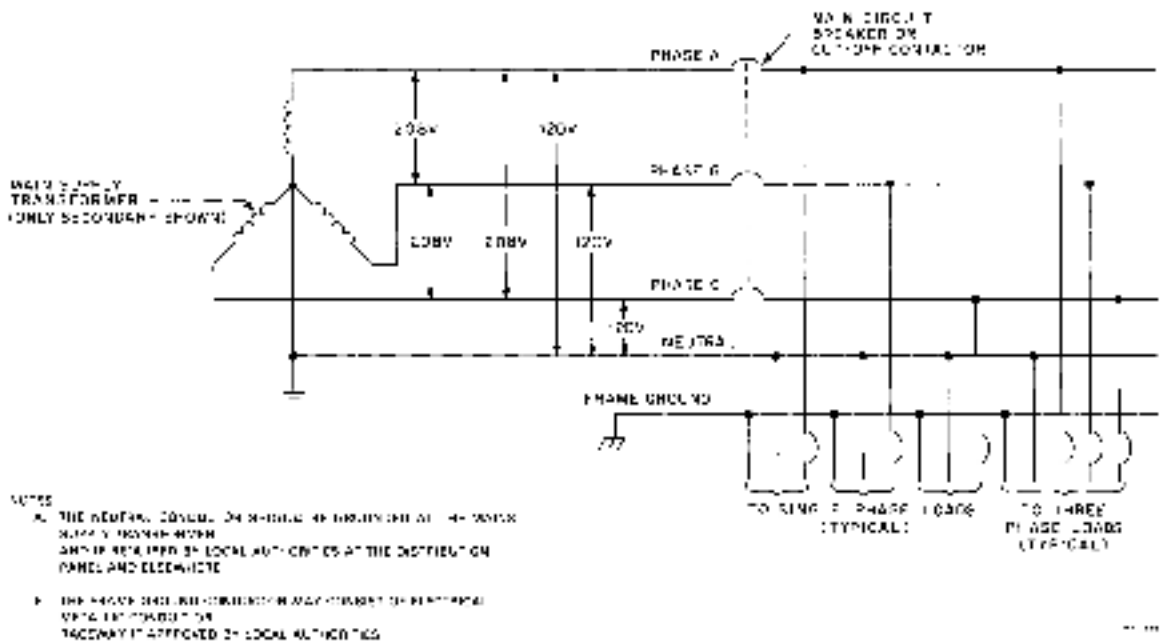


Figure 2-5. Typical 60 Hz Power System

Figure 2-6 shows a typical 50 Hz power system.

Two types of power systems can be used to provide power to the NEMA type L14-20R receptacle. The type shown in Figure 2-7 is referred to as split-phase (or 2 phase 180 displaced) 120/240 Vac. It comprises a center-tapped transformer with 120 Vac between the center tap and either of the two legs. 240 Vac exists between the two outside legs.

The second type (Figure 2-8) is referred to as 3-phase Y (120 displaced) 120/208 Vac. The 120 Vac exists between neutral and any of the three other legs (X, Y, or Z), and 208 Vac exists between any two of the outer legs (i.e., between X and Y, X and Z, or Y and Z). Although Figure 2-8 shows the X and Y connections as the two phases used for the receptacle, any two of the three phases shown can be used.

The ground terminal on the L14-20R receptacle will normally have a green screw, the neutral terminal will be white or silver, and the "hot" terminal will be brass covered.

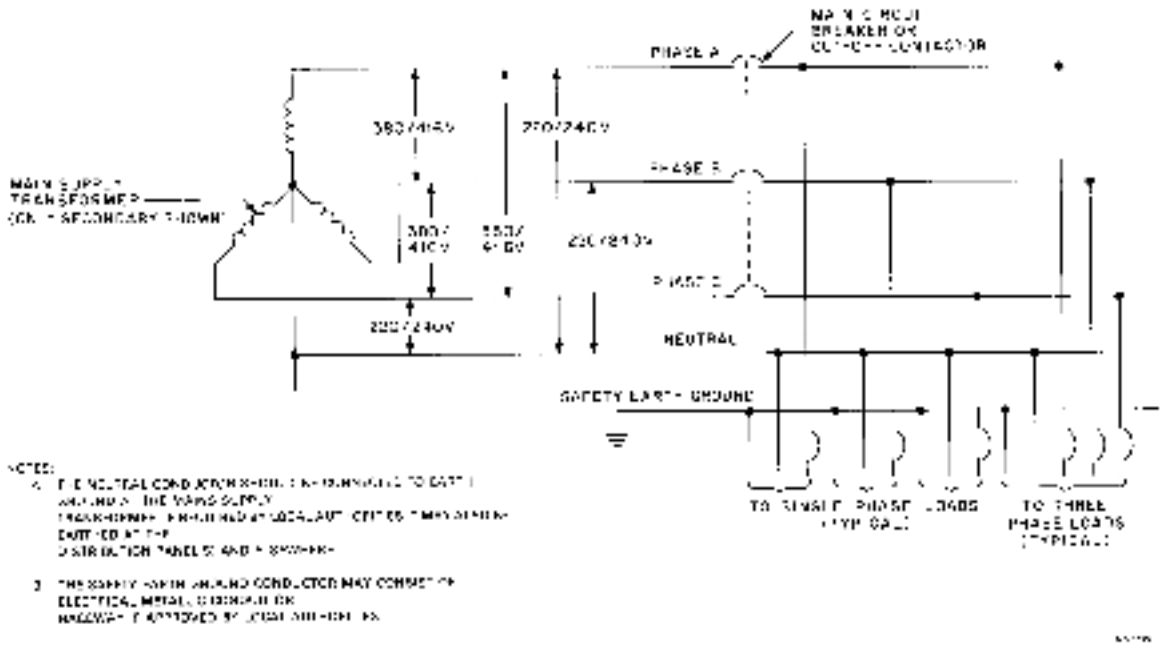


Figure 2-6 Typical 50 Hz Power System

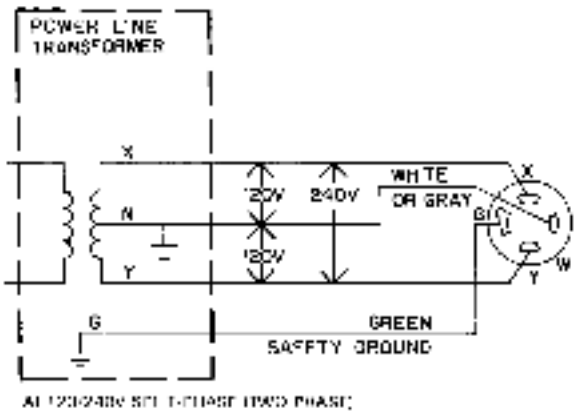


Figure 2-7 Split Phase (2 phase) Power System

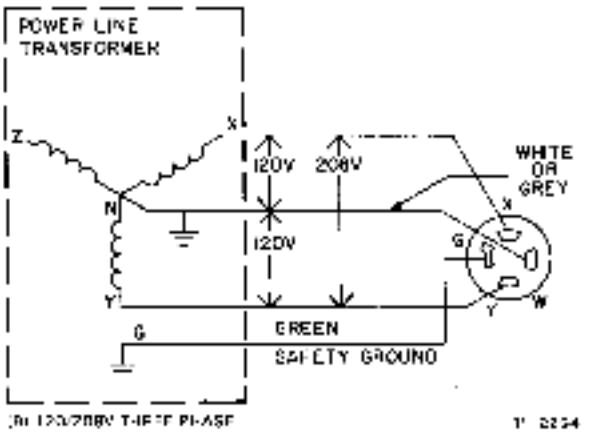


Figure 2-8 Three Phase Y Power System

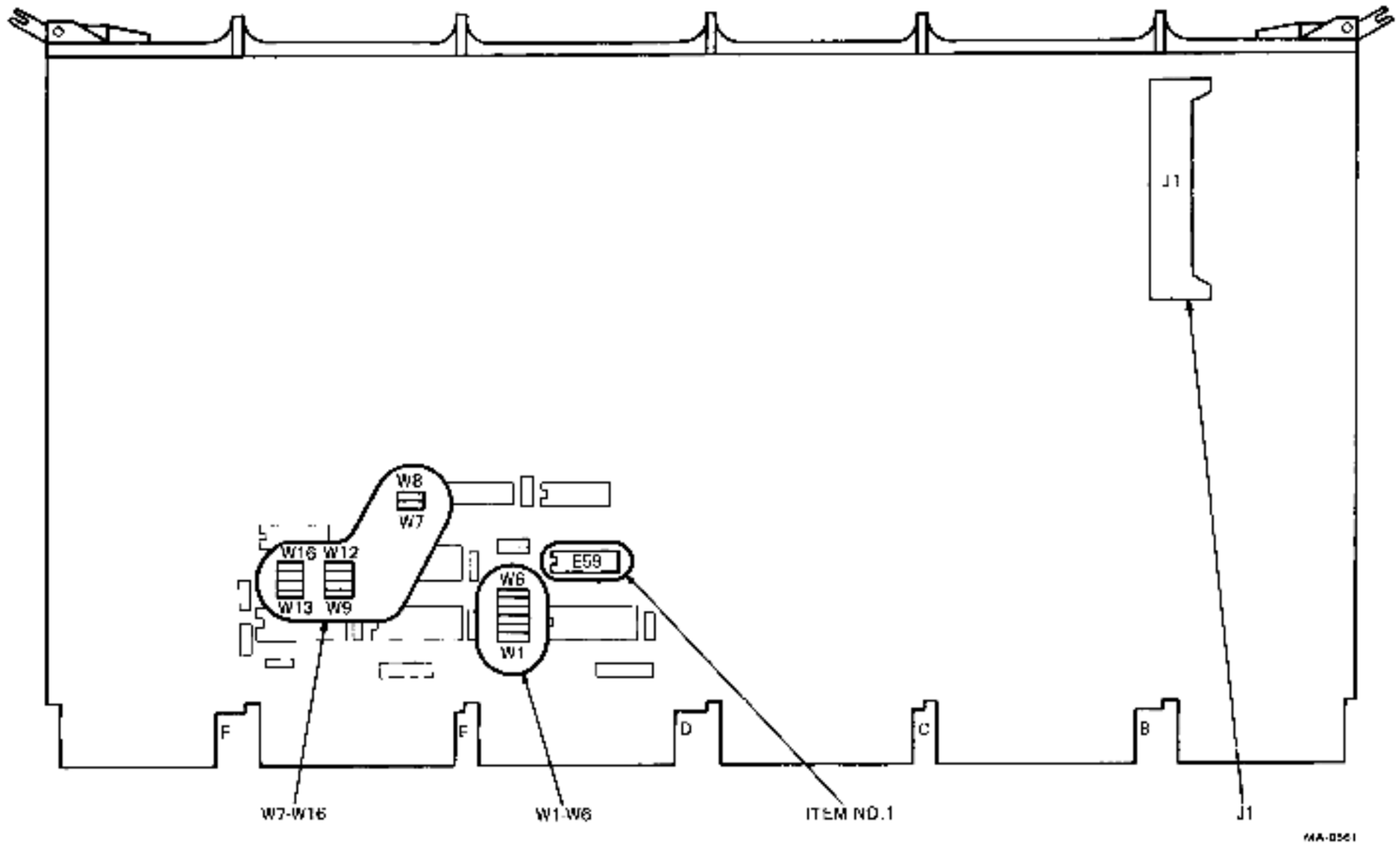
2.3 INSTALLATION – GENERAL

The controller should be installed first, followed by the drive(s). Next, the diagnostics should be run to demonstrate that the subsystem is functioning properly or to diagnose any problems. Paragraph 2.4 explains the installation of the RL11 Controller. Paragraph 2.5 deals with the RLV11 and Paragraph 2.6 describes RL8A installation.

Paragraph 2.7 contains instructions to install the unit and Paragraph 2.8 explains acceptance testing and contains separate paragraphs for each of the three controllers. Paragraph 2.9 describes the use of the M9312 bootstrap module that may be used on RL11-based systems.

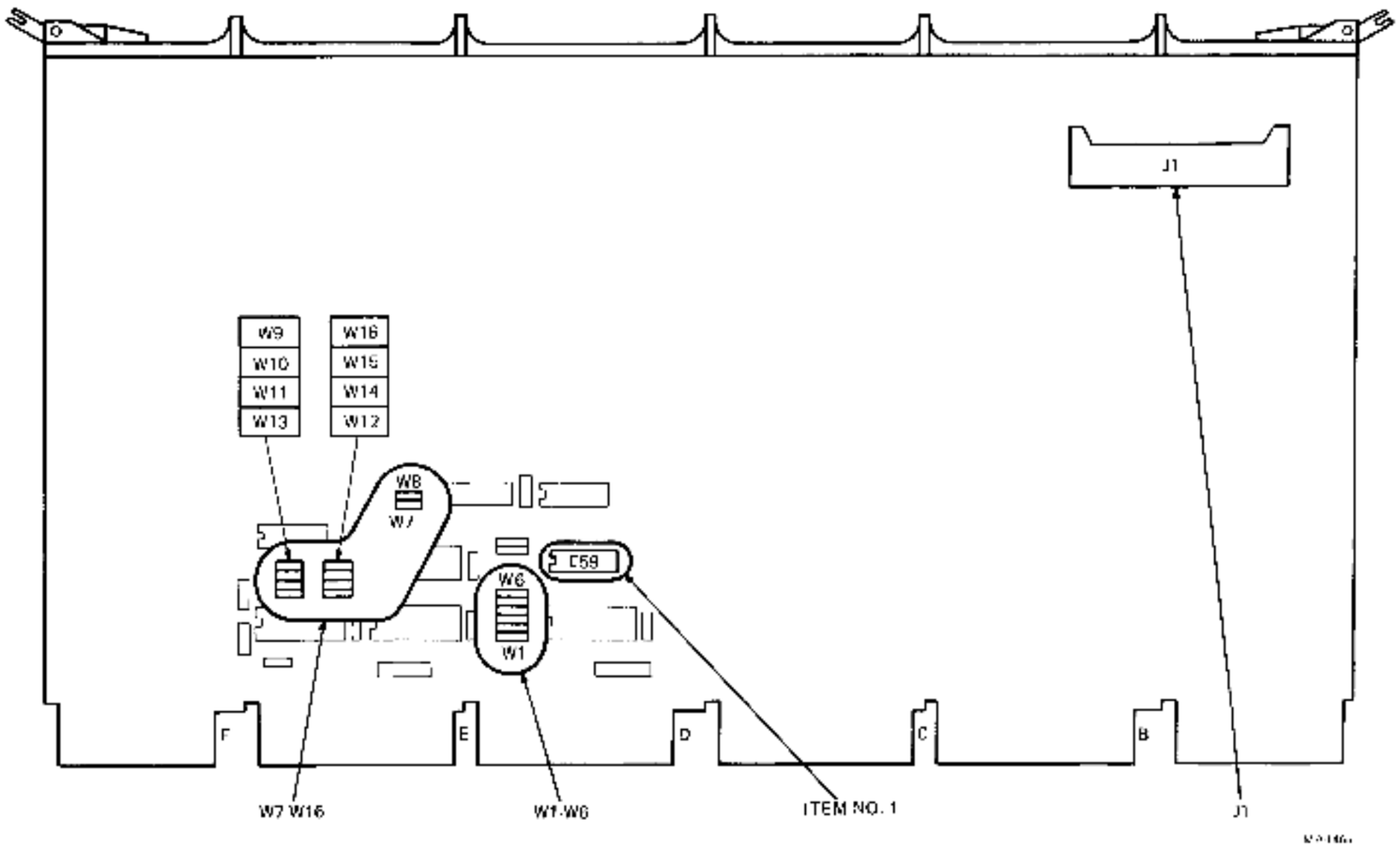
2.4 RL11 CONTROLLER INSTALLATION

The RL11 Controller (M7762) is a single hex-height module that is installed in a hex height SPC slot. Connector J1 connects the controller to the drive bus (Figure 2-9).



OLDER VERSION

Figure 2-9 RL11 Component Layout (Sheet 1 of 2)



NEWER VERSION

Figure 2-9. RL11 Component Layout (Sheet 2 of 2)

Of the 21 jumpers on the RL11 Controller, five are used for factory test purposes. The remaining 16 are for address selection:

W1-W6 VECTOR ADDRESS (160)
W7-W16 BASE ADDRESS (774400)

NOTE
A logical one is represented by the presence of a jumper wire.

The Unibus priority plug sets the priority for bus requests. For the RL11 subsystem, bus requests are at priority level 5 (BR5/BG5). (See Figures 2-10 and 2-11.)

NOTE
Adjustments on the RL11 are preset at the factory and are not to be changed in the field.

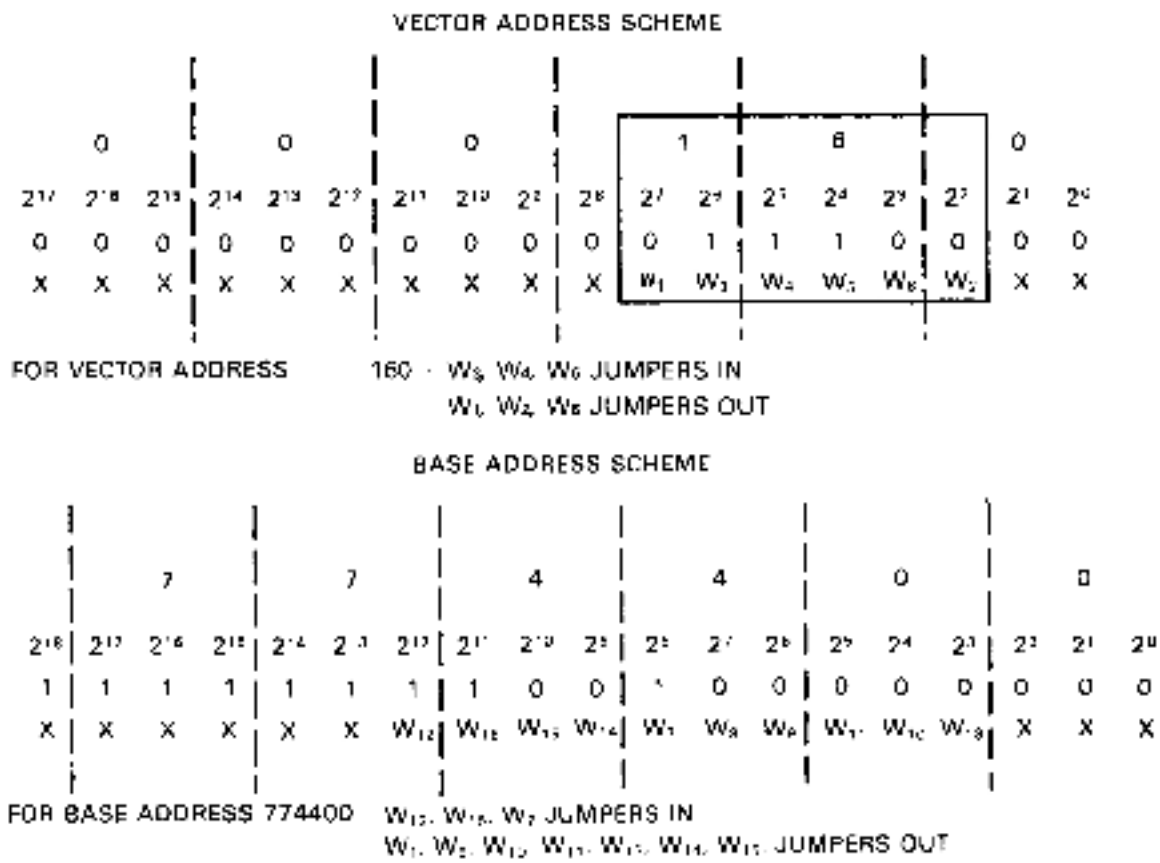
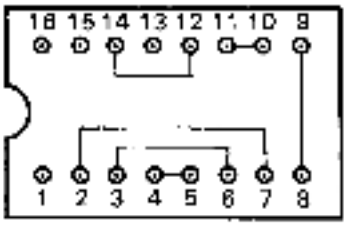


Figure 2-10 RL11 Base And Vector Address Jumper Configuration



PRIORITY JUMPER PLUG FOR
BUS REQUEST LEVEL FIVE (5)

PLUG PIN NUMBER	SIGNAL NAME	UNIBUS PIN
1		
2	BG IN	
3	BG OUT	
4	UB BG 4	DT2
5	UB BG 4 IN	DS2
6	UB BG 5	DR2
7	UB BG 5 IN	DP2
8	UB BG 6	DN2
9	UB BG 6 IN	DM2
10	UB BG 7	DL2
11	UB BG 7 IN	DK2
12	BR	
13	UB BR 4	DD2
14	UB BR 5	DE2
15	UB BR 6	DF2
16	UB BR 7	DH2

MA-0560

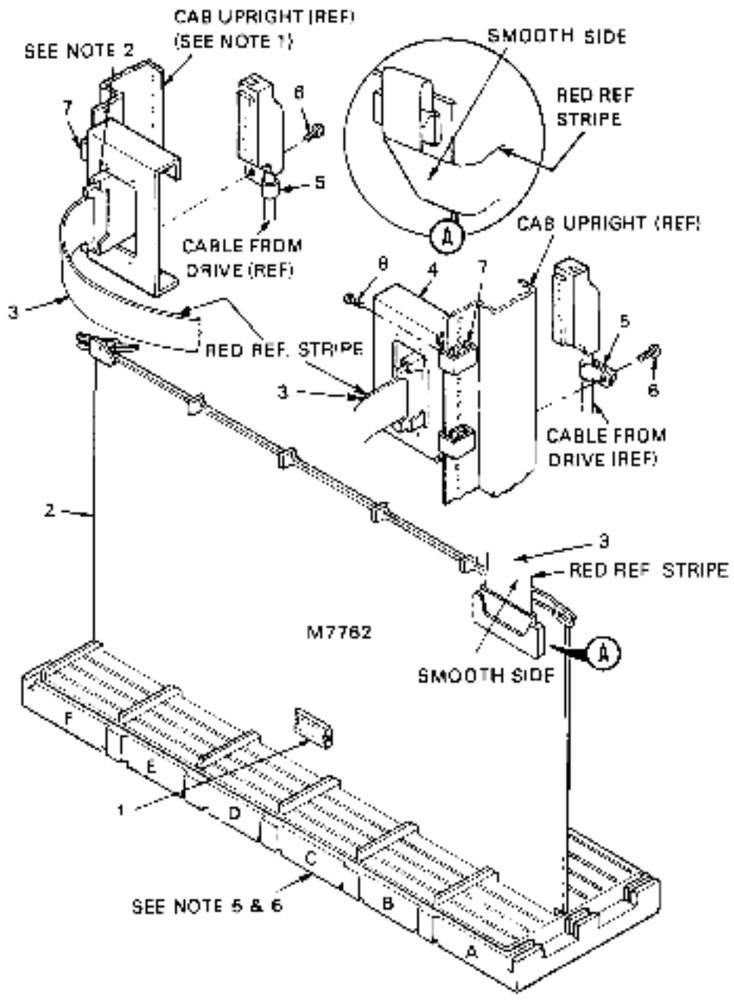
Figure 2-11 RL11 Priority Jumper Assembly Connections

To install the controller:

1. Remove the M7762 module from its shipping container and examine it for any physical damage.

2. If a priority level other than 5 is required, obtain an appropriate priority jumper assembly or set up the priority jumper assembly (item 1, Figure 2-9) using Figure 2-11 as a guide. The vector and base address jumpers W1-W16 are for 160 and 774400, respectively. If the subsystem configuration requires other than standard addresses, set the jumpers up as shown in Figure 2-10. Physical location of these jumpers is shown on Figure 2-9.

3. Install the ribbon cable (BC06R-XX) with the red indicator stripe to the right and the smooth side facing the viewer when viewing the component side of the controller as shown in Figure 2-12. Dress the cable as necessary.



NOTES:

1. WHEN INSTALLED IN BA11K OR BA11L EXPANSION BOX, BC06R CABLE ITEM #3) SHOULD BE FOLDED 90° AND ROUTED UP OUT OF THE BOX AS SHOWN.
2. WHEN ALTERNATE MOUNTING POSITION IS USED CONNECTOR IN TRANSITION BRACKET MUST BE INVERTED SO THAT I/O CABLE FROM DRIVE WILL HANG IN A DOWNWARD POSITION AS SHOWN.
3. ITEM #3 THRU ITEM #8 ARE NOT ASSEMBLED AT THIS POINT BUT ARE SHIPPED WITH UNIT FOR ASSEMBLY AT INSTALLATION TIME.
4. PRIORITY JUMPER ASSY (ITEM #1) TO BE PLUGGED INTO M7762 AT FINAL ASSY
5. THE RL11 MODULE (M7762) WILL OCCUPY ONE HEX SPC SLOT.
6. JUMPER WIRE FROM CA1 TO CB1 ON THE SPC BACKPLANE MUST BE REMOVED AT INSTALLATION

DESCRIPTION	DWG PART NO	ITEM NO.
2 SCREW, PHL TRS HD #10-32 X .50 LG	9006073-03	8
2 NUT, SPRING #10-32	9007786-00	7
1 SCREW, TAP-TLTE, #8 X .38 LG	9008418-01	6
1 CLAMP, CABLE	9007083-00	5
1 TRANSITION BRACKET ASSY	C-AD-7012415-0-0	4
1 CABLE ASSY	D-UA-BC06R-08	3
1 RL11 CONTROLLER	D-UA-M7762-0-0	2
1 PRIORITY JUMPER ASSY	5408778	1

CT-2005

Figure 2-12 RL11 Controller Installation

4. Insert the controller into its appropriate slot in the SPC backplane as shown in Figure 2-12 after ensuring that the slot does not contain a grant continuity module in row D. Do not crimp the ribbon cable. Route the cable up and out to the rear of the cabinet, allowing for cable strain relief.

NOTE
See Appendix A for configuration rules and SPC slot selection considerations.

5. Remove the jumper between CA1 and CB1, (NPR Grant) on the backplane, if the jumper exists.

6. Install the transition bracket at the rear of the cabinet shown in Figure 2-12. Assemble and install transition connector.

7. Connect the other end of the ribbon cable (BC06R-XX) with the red indicator stripe on the top. Use Figure 2-12 as a guide.

8. Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify the voltages are within the ranges specified below.

VOLTAGE	RANGE	TEST POINT	
GROUND		AC2	
−5 VDC	−4.75 TO +5.25 VDC	AA2	BACKPLANE
−15 VDC	−14.25 TO +15.75 VDC	CV1	LOCATION
−15 VDC	−15.75 TO −14.25 VDC	CB2	

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate manual.

2.5 RV11 CONTROLLER INSTALLATION

An RLV11 Controller is comprised of a bus interface module (M8014) and the drive bus module (M8033). Each module has switches, jumpers, dumpots, and connectors that are explained in the following paragraphs.

2.5.1 Bus Interface Module

The bus interface module (M8014) contains the logic circuits that perform the following major functions:

- LSI-11 bus interface functions
- Programmable registers
- Silo data storage and control circuits

An illustration of the component side of M8014 is shown in Figure 2-13. The location of the bus address switches, the vector address switches, and the connector finger assignments are shown in this figure.

The bus address switch is used to set up the device base address. It is normally factory preset to 7440. This means the device CS register has an address of 174400 and the MP register has an address of 174406. The switches have the ON and OFF positions labeled. The ON position is the logical 1 or true state (Figure 2-14).

The vector address switch is used to select the address of the vector for this device when it interrupts. It is factory preset for an address of 160 (Figure 2-15).

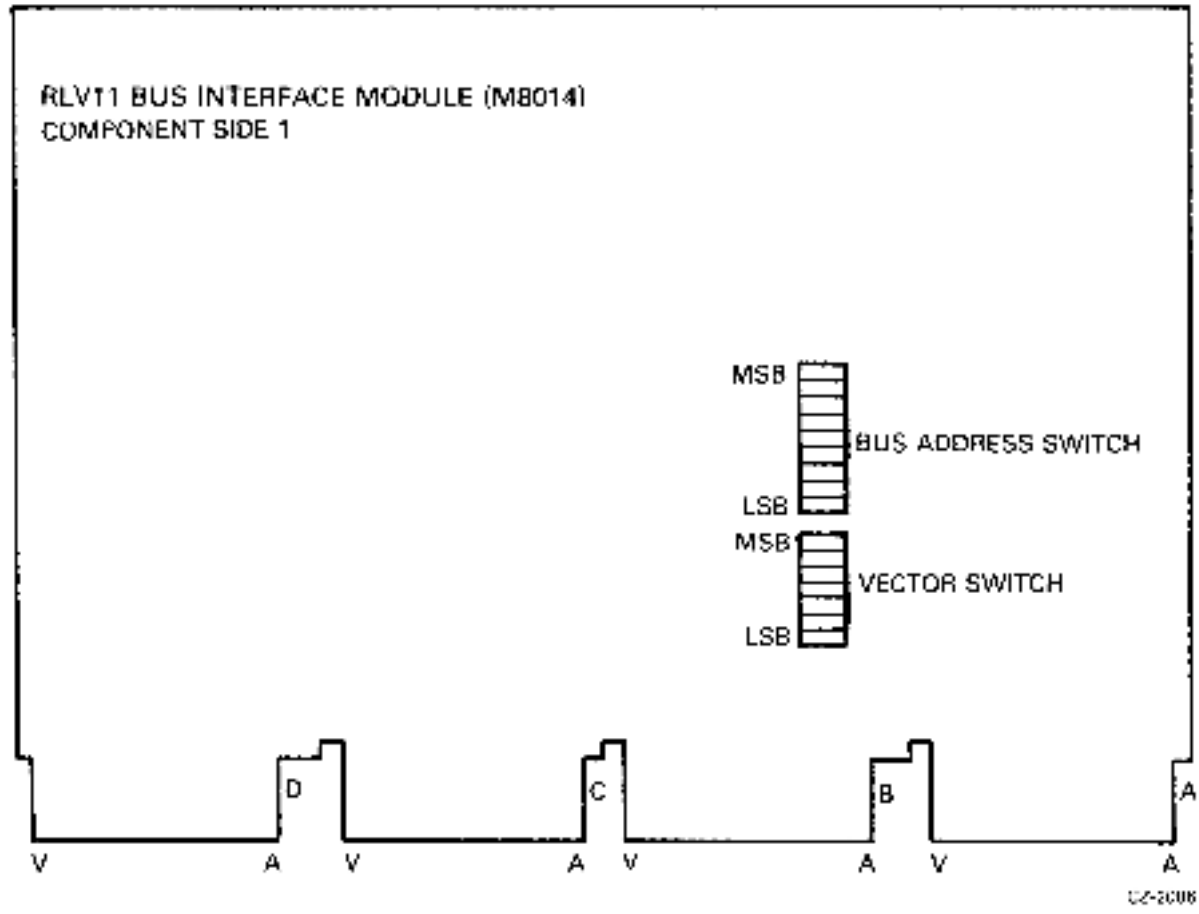
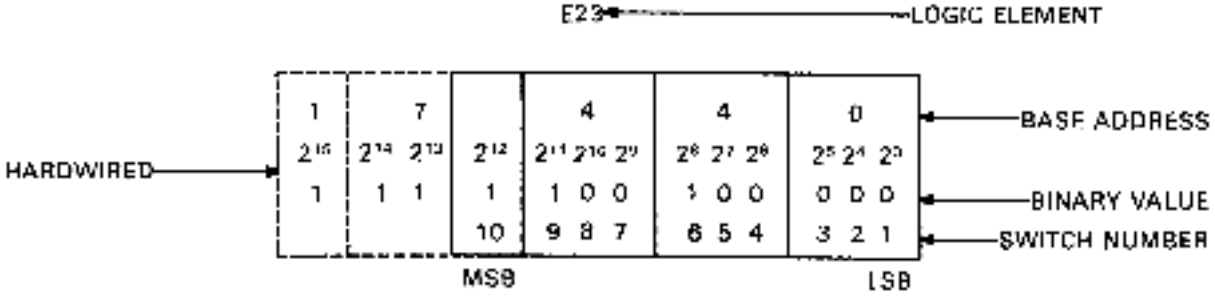


Figure 2-13 RLV11 Bus Interface Module (M8014) (Component Side)



FOR EACH "0" SET THE CORRESPONDING SWITCH "OFF"

FOR EACH "1" SET THE CORRESPONDING SWITCH "ON"

USE THIS SCHEME TO SELECT THE APPROPRIATE BASE ADDRESS IF A DIFFERENT BASE ADDRESS IS REQUIRED

CZ-2034

Figure 2-14 RLV11 Base Address Switch Settings

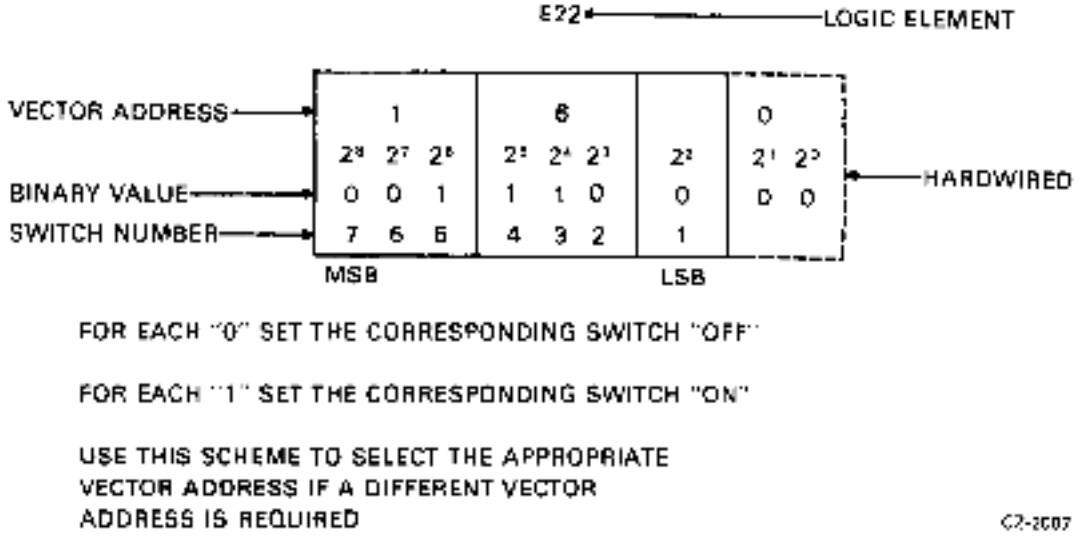


Figure 2-15 RLV11 Vector Address Switch Settings

2.5.2 Drive Module

The drive module (M8013) contains the circuitry that performs the following major functions:

- Data formatting and error detecting circuits
- Control microsequencer and timing circuits
- Drive bus interface

An illustration of the component side of M8013 is shown in Figure 2-16.

NOTE

Adjustments to the RLV11 are preset at the factory and are not to be adjusted in the field.

2.5.3 Module Slot Location

Modules M8013 and M8014 must be inserted into the H9273 backplane (Figure 2-17) such that the M8013 module is in the slot closest to the processor. Outside of this one restriction, the two modules can be inserted in any two unused slots. The controller priority level is based solely on its electrical distance from the microprocessor module in slot 1.

2.5.4 Module Installation

1. Using the normal configuration rules, select two adjacent slots in the backplane for the two controller modules.

2. Insert the ribbon cable (BC06R-XX) into J1 on the M8013 with the red stripe edge toward the top (Row A) of the module.

3. Insert the M8013 module into the selected slot that is closest to the processor.

4. Examine the M8014 to insure that the base address switches and the vector address switches are set correctly. Check jumpers W1 thru W4 for correctness. See Figures 2-14, 2-15 and 2-16.

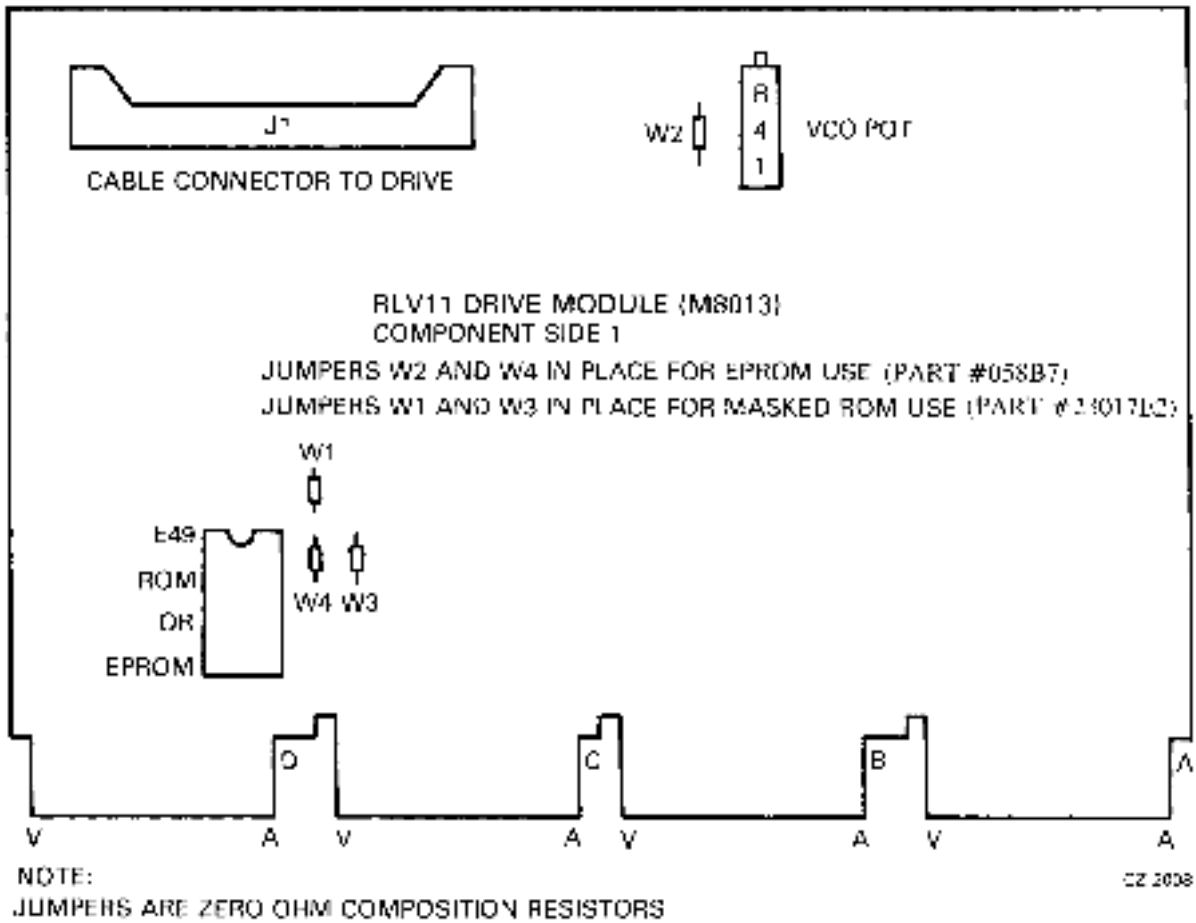


Figure 2-16 RLV11 Drive Module (M8013)

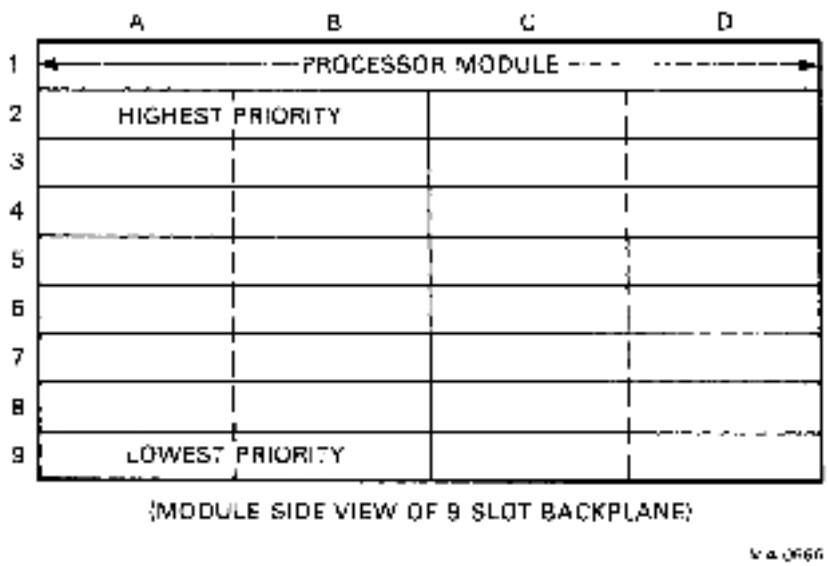


Figure 2-17 H9273 Backplane Grant Priority Structure

5. Insert the M8014 module next to the M8013.

6. Install the transition bracket at the rear of the cabinet as shown in Figure 2-12. Assemble and install the transition connector.

7. Connect the other end of the ribbon cable with the red stripe up.

8. Apply system power and, using a suitable measuring device (i.e., digital voltmeter or equivalent), verify that the voltages are within the ranges specified below.

VOLTAGE	RANGE	TEST POINT
Ground		AC2
+5 Vdc	−4.75 Vdc to +5.25 Vdc	AA2
+12 Vdc	−11.5 Vdc to +12.5 Vdc	AD2
−5 Vdc	−5.25 Vdc to −4.75 Vdc	AL1 (M8013 only)

NOTE

The −5 Vdc is generated on the M8013 module. It is not adjustable but must be within specifications for proper operation. Module replacement is the only corrective procedure.

Measure all voltages between the ground test point and the appropriate voltage test point. If any adjustments to the power supply are necessary, refer to the appropriate manual.

2.6 RL8-A CONTROLLER INSTALLATION

2.6.1 Introduction

The RL8-A Omnibus controller module (M8433) contains the following logic functions:

- Interface logic
- Programmable registers
- Silo data storage and control
- Data formatting and error detection
- Control microsequencer and timing logic
- Drive bus interface logic

NOTE

Adjustments on the RL8-A are preset at the factory and are not to be changed in the field.

2.6.2 Module Slot Location

The module can be inserted into any unused Omnibus hex-height slot between the CPU and the first memory element. The controller is connected to the first drive via a BC80J-20 interface cable. Connections between drives are made using a BC20J-XX (70-12122-10) cable.

2.6.3 Module Installation

1. Remove the M8433 module (see Figure 2-18) and interface cable (BC80J-20) from the shipping container and inspect them for physical damage.

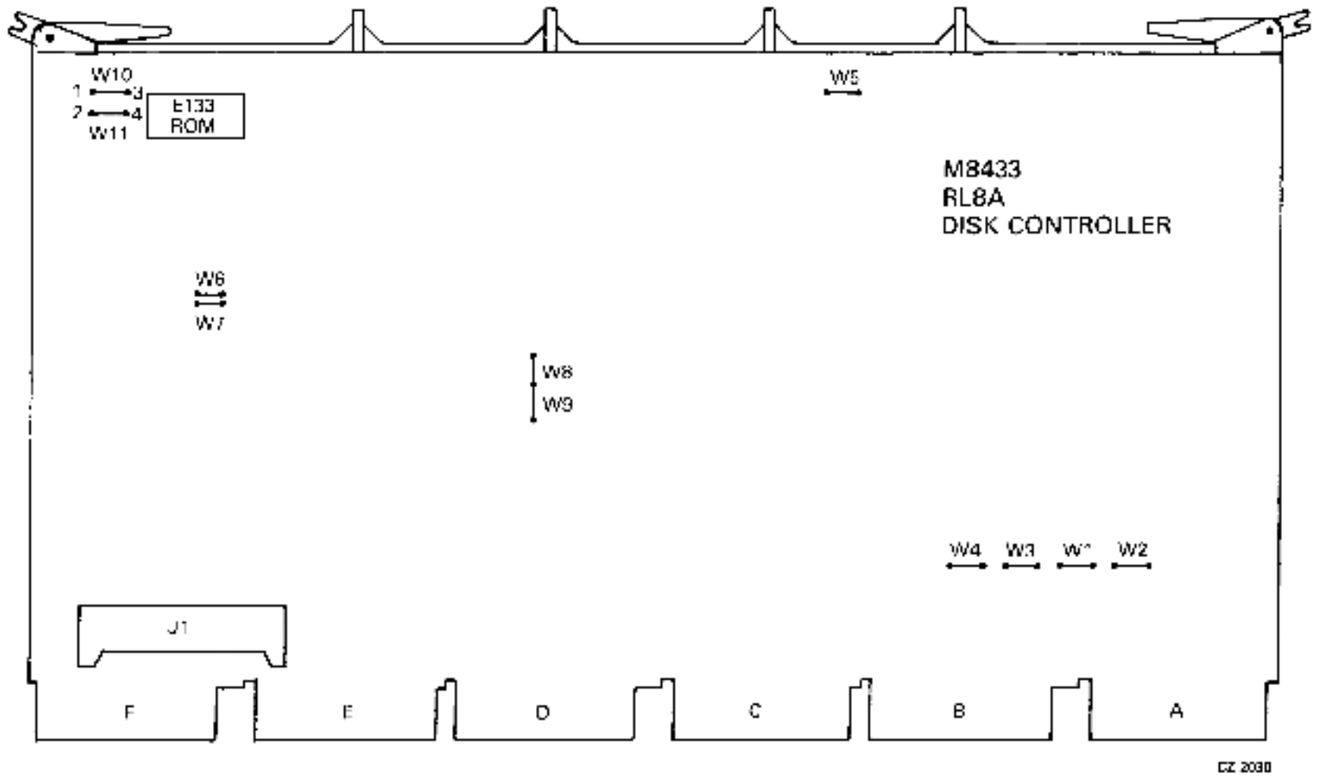


Figure 2-13 RL8-A Jumpers

2. Verify the proper jumper configuration for device codes and priority (Figure 2-18).

Device Code	W1	W2		
60,61	IN	OUT		
62,63	IN	IN		
Break Priority	**W3**	**W4**	**W5**	
0	IN	OUT	IN	
3	OUT	IN	OUT	

NOTE
RL8-A is shipped from the factory with a priority of 0.

Device Type	W8	W9		
RL01	OUT	IN		
RL02	IN	OUT		
ROM Type (E133)	**W10**	**W11**	**W6**	**W7**
012h2	OUT	IN	IN	OUT
8708 or 2708	IN	OUT	OUT	IN

3. Position the BC80J-20 interface-to-drive cable in the PDP-8 chassis and connect the Berg connector to the M8544 module.

4. Install the M8544 module into selected slot on the Omnibus backplane.

5. Route the cable out to where the first drive will be installed.

2.7 RL01/RL02 DISK DRIVE INSTALLATION

2.7.1 Unpacking and Inspection

1. When delivered, each drive and its associated cabinetry are enclosed by a heavy cardboard carton and attached to a shipping skid (Figure 2-19). Remove the plastic straps that secure the shipping carton to the skid.

2. Remove the lid from the top of the carton.

3. Remove the staples that fasten the wooden crating slats and carton flanges to the skid.

4. Remove the shipping carton.

5. Inspect the cabinet and drive for signs of damage. Retain all packing material and receipts in the event that any claims for shipping damage must be filed. All claims should be filed promptly with the transportation company.

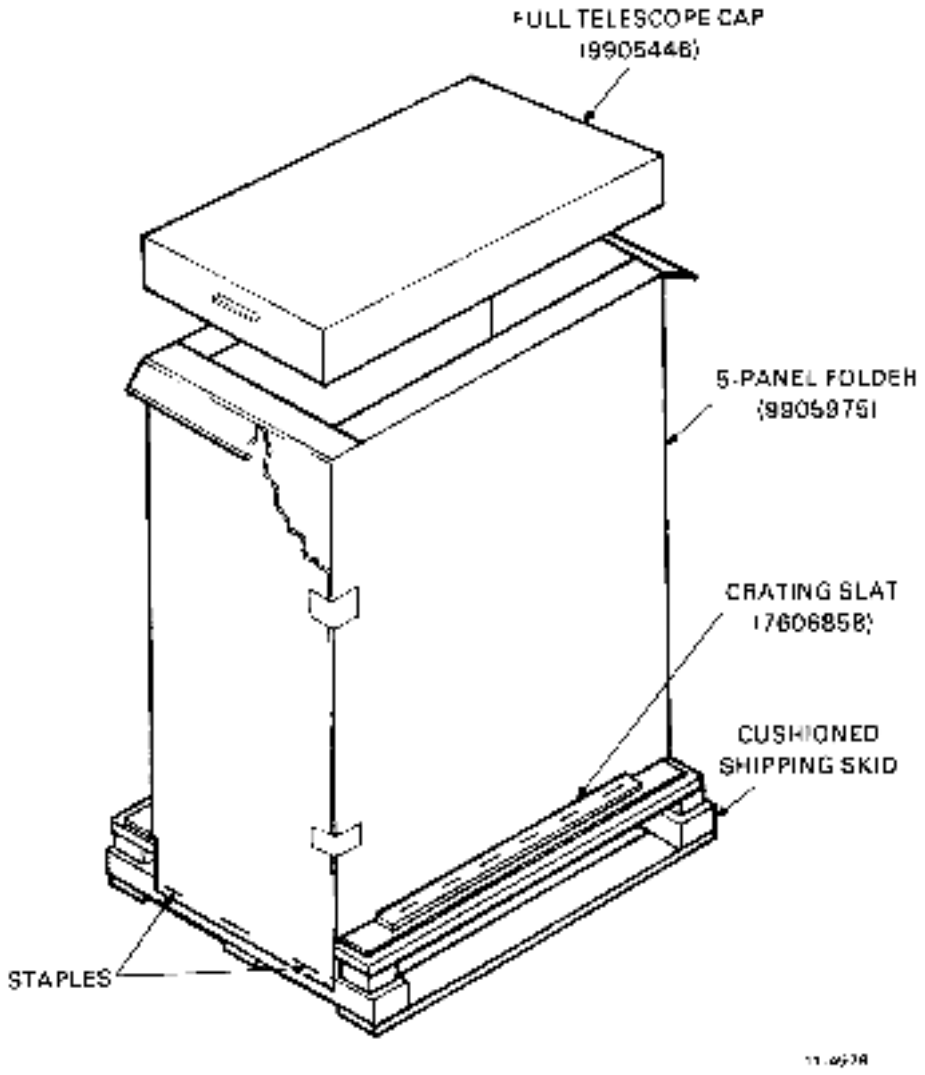


Figure 2–9 H950 Shipping Package

2.7.2 RL01/RL02 Disk Drive Unit Mounting

NOTE

If the RL01/RL02 is to be mounted in an H950 cabinet, the shipping brackets must be retained and refitted after installation. This is the only way to prevent the drive from sliding while repositioning or moving the H950 cabinet.

The drive may be shipped in a rack or cabinet as an integral part of a system or may be shipped in a separate container for addition to an existing system.

If the drive is to be installed in an existing rack or cabinet, install the chassis slides first as described in Steps 1 through 6 below (Figure 2-20). The procedure for installing the drive itself begins with Step 7.

1. Install cabinet stabilizers before mounting the drive.

2. Remove the slides from the disk drive. (Retain the hardware for reassembly.)

3. Install slides into the rack or cabinet using enclosed hardware. Be sure the slides are at the correct height to permit installation of pop panels (dress panels) upon completion of installation. Also verify that the slides do not bind on any hardware used to mount the slide.

4. Extend slides to lock position.

5. Slide drive onto chassis slides and reinstall security mounting hardware.

6. Ensure that the disk drive moves easily on the slides, that there is no binding in the cabinet, and that the proper height has been maintained for dress panels.

7. Open the drive access cover.

NOTE

There is a safety interlock in the RL01 and RL02 Disk Drives that locks the drive access cover when the drive has no power. The manual release to bypass this interlock is located on the right side of the drive under a small access cover (Figure 2-21). Remove the cover to reach the solenoid. Pull down on the solenoid and operate the top release mechanism at the same time to open the drive access cover. After the drive access cover is open, replace the solenoid cover.

8. Loosen the head restraining bracket screw located on the positioner. Turn the bracket 90 degrees and retighten the screw (Figure 2-21).

9. On newer drives there are two shipping screws on the bottom of the unit that secure the spindle/blower motor. Remove the screws.

10. If the drive is being installed in a dual-drive cabinet that has an interlock system to prevent more than one drive being extended at a time, ensure that it is connected.

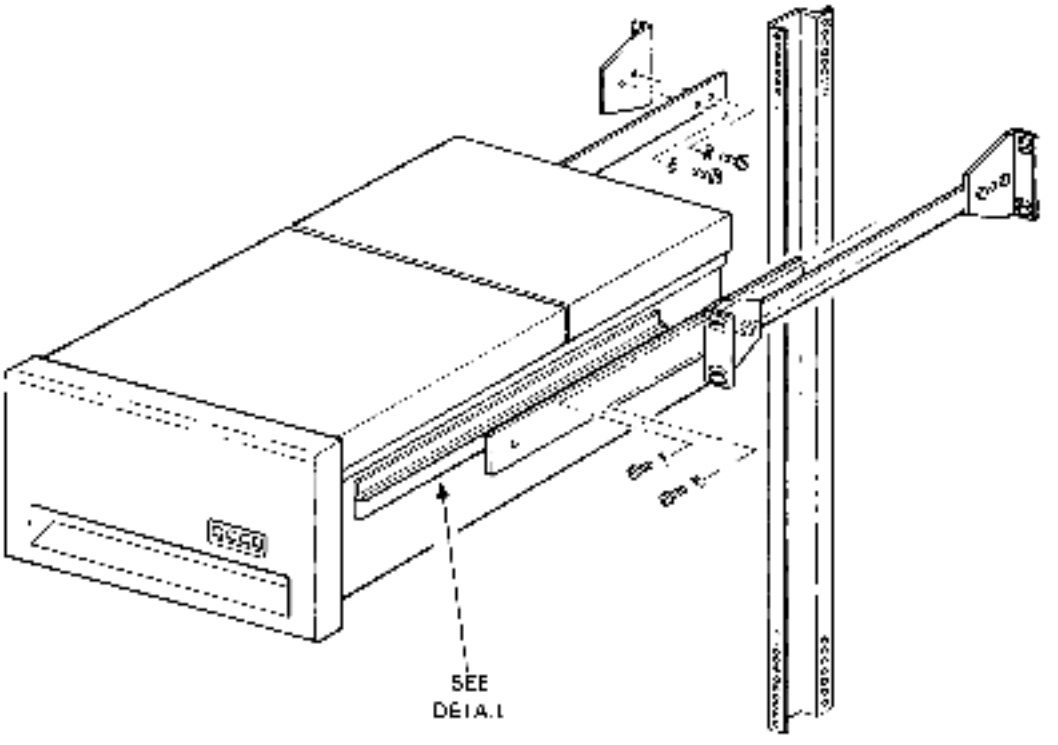
11. Inspect the terminal block covers at the rear of the drive. Ensure that they are configured properly for the input power available (Figure 2-22).

CAUTION

Connection to the wrong power source will result in serious damage to the disk drive.

12. If there is only one disk drive in the system, or if this is the last drive of the daisy chain, install a terminator assembly (DIGITAL part no. 70-12293) in the "cable out" location at the rear of the drive (Figure 2-22).

13. If this is an RL11- or an RLV11 based system, route the I/O cable BC20J-XX (DIGITAL part no. 70-12122-10) between the first drive and the transition connector. If this is an RL8-A-based system, route the BC80J-20 cable from the RL8A to the first drive.



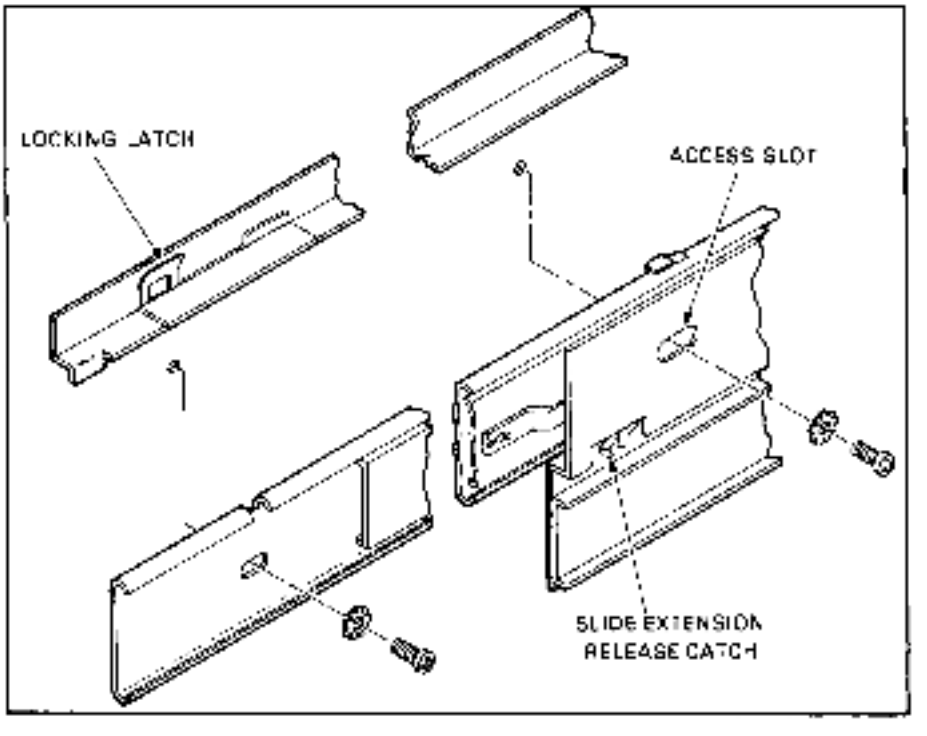


Figure 2-20 RL01/RL02 Cabinet Installation

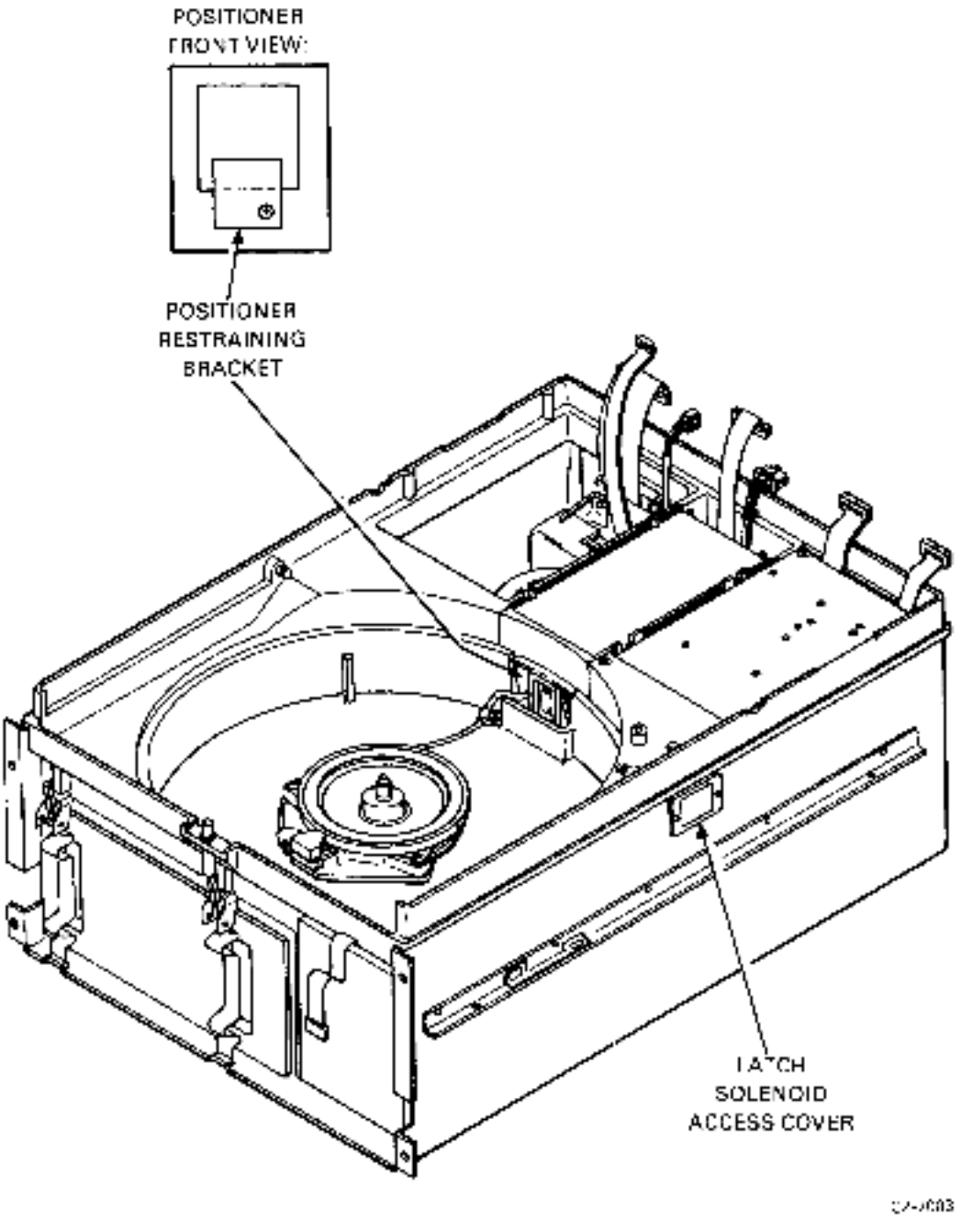


Figure 2-2 RD01/RD02 - Covers Removed

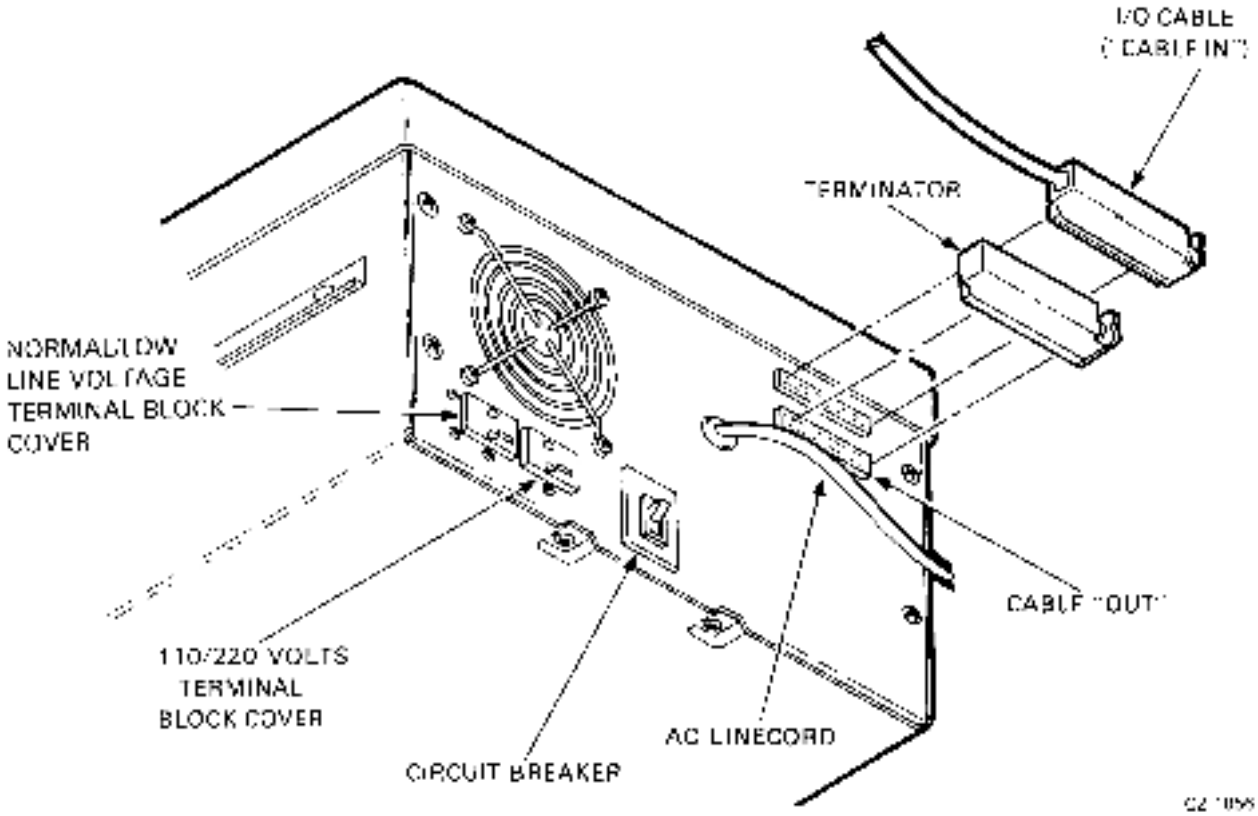


Figure 2-23. RX02/RX01 Disk Drives-Rear View

14. If this is a multidrive installation, connect an I/O cable from "cable in" of this drive to the "cable out" connector of the previous drive. Repeat for each drive.

NOTE

The total length of cable from controller to the last drive must not exceed 30 m (100 ft).

15. Install the proper unit select plug at the front of the drive (Figure 2-23).

2.7.3 Drive Prestartup Inspection

To begin the inspection procedure, remove the top cover by loosening the captive screws and lifting the cover straight up. Rest the cover on the rear of the drive (Figure 2-24). With the drive power off and controller power on, follow these steps.

NOTE

If a problem occurs, consult the *RL01/RL02 Technical Manual.*

1. Ensure that the positioner restraining bracket is not interfering with the positioner (Figure 2-21).

2. Ensure that the positioner is home.

3. Ensure that the read/write head pinlobels are not bent or dirty. (If they are dirty, clean with a solution of 91 percent alcohol and 9 percent water and a lint-free wiper.

4. Ensure that the spindle rotates freely and its top surfaces are not dirty. (Clean as described above).

5. Ensure that the brush assembly is home (not exposed).

6. Ensure that the logic modules and connectors are seated firmly.

7. Turn CB1 ON.

8. Ensure that the spindle rotates slowly counterclockwise for approximately 15 seconds and stops. At this time, the LOAD light will come on.

9. Ensure that the FAULT light is not on.

10. Ensure that the fan at the rear of the drive is operating.

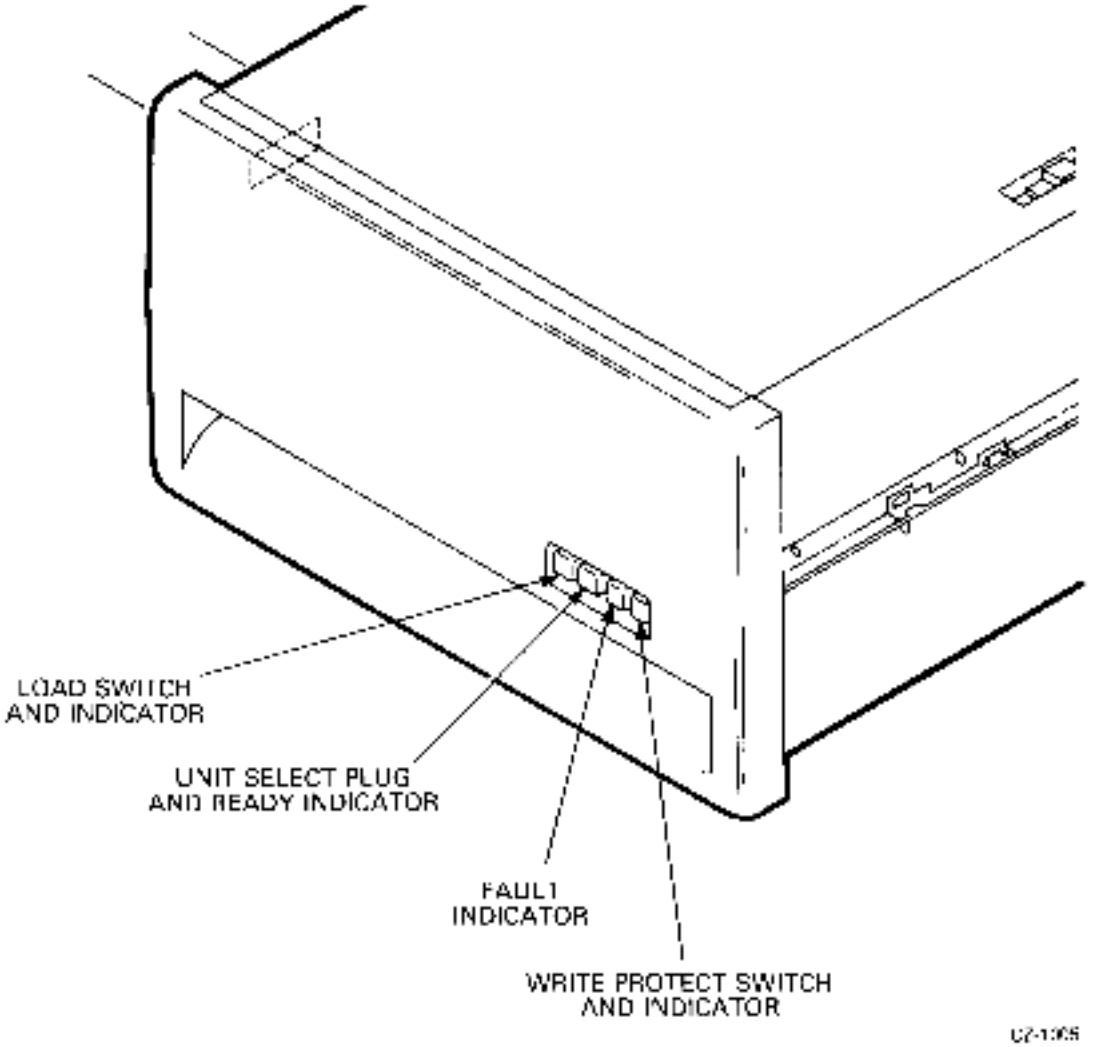


Figure 2-23 RL01/RL02 Disk Drive-Front View

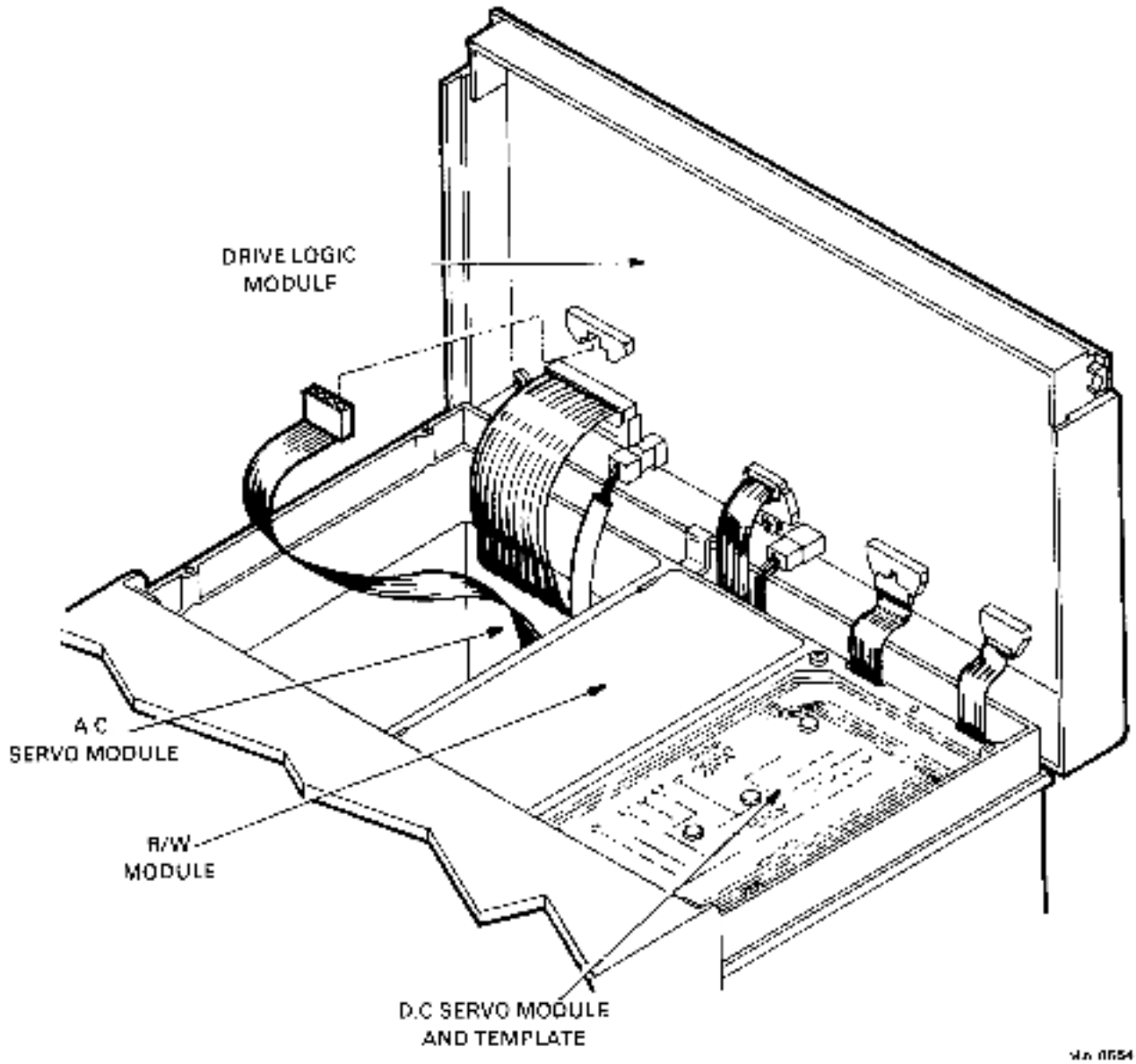


Figure 2-24 RD51/RL02 Disk Drive-Exposed Drive Logic Module

11. Using a suitable measuring device (i.e., digital voltmeter or equivalent), ensure the following drive voltages are within the specified tolerances.

Voltage	Range	Test Point
+15UNREG	(+15.0 to +18.0 Vdc)	−VUNREG
−15UNREG	(−15.0 to −18.0 Vdc)	−VUNREG
+5REG	(+4.85 to +5.35 Vdc)	TP8
+8REG	(+7.7 to +8.3 Vdc)	TP4
−8REG	(−7.7 to −8.3 Vdc)	TP5

See Figure 2-24 for dc servo module location. Test points are located on the mask covering the dc servo module.

12. Verify that the WRITE PROTect switch cycles in and out and the indicator lights up when the switch is pressed.

13. Verify that the LOAD switch cycles in and out when the switch is pressed. Return switch to the "out" position.

14 Turn off CB1.

15. Reinstall the top cover and secure with the captive screws.

16. Ensure that the drive access cover cannot be opened.

17. Turn CB1 on and ensure the drive access cover will open.

2.7.4 Drive Startup Operation Check

1. With the drive power ON, install a scratch cartridge as described in Paragraph 3.3.

2. Close the cover, press the LOAD switch and note that:

   - The LOAD light goes out

   - When the cartridge reaches nominal speed (after approximately 30 seconds), a brush cycle commences. When the brushes have returned home, the read/write heads will load and approach cylinder 0. When the heads have locked onto cylinder 0, the READY light will illuminate. The total time for this process is approximately 45 seconds.

3. Press the LOAD switch again. The READY light should go off and the read/write heads should retract to their home position. The spindle should slow down and then come to a complete stop after about 30 seconds. The LOAD light should illuminate when the spindle has stopped.

4. If the drive startup operation check detailed above is successfully completed (i.e., the READY indicator illuminates), run the subsystem confidence tests described in Paragraph 2.8. If there is a problem, consult the *RL01/RL02 Technical Manual*.

2.8 CONFIDENCE TESTING

Confidence testing consists of running the diagnostic programs. Each diagnostic has a listing that contains operating instructions. Each listing explains system hardware requirements, software environment, which features are tested and how they are tested, program options and how to select them, how to interpret printouts, error handling, device information tables, dialogue with the Diagnostic Supervisor, and complete operating instructions. The listings are available as hard copy printouts or on microfiche.

The binary form of the diagnostic programs are available on various media. It is always advisable to keep a copy of the RL01/RL02 diagnostics on a medium other than the RL01K or RL02K cartridge so that the diagnostics can be loaded through another device if the RL subsystem is down.

When ordering diagnostic media, listings, manuals, or microfiche, check the current catalog or index for the latest revision level. The applicable catalogs and indexes are listed in Table 2-3. Unless otherwise specified when ordering, the latest revision will be shipped.

Table 2-3 Diagnostic Catalogs and Indexes

NAME		PART NUMBER
PDP-11	Diagnostic Software Components Catalogue*	AV-B021E-TC
PDP-8	Software Components Catalogue*	AV-0872B-TA
PDP-11	MAINDEC Index (microfiche)	AII-9026P-MC
PDP-8	MAINDEC Index (microfiche)	AII-6572G-MA

* **Note—Both of these catalogs are available on microfiche (EP-08/11DC-02).**

2.8.1 RL11-Based Diagnostics

The diagnostic package used for an RL11/RL01 subsystem before the release of the RL02 consisted of the six free-standing programs listed in Table 2-4. There were two revisions, Revision A and Revision B. These programs handled only RL01 drives (not RL02 units).

Table 2-4 RL11-Based Diagnostics

PART NUMBER	DESCRIPTION
CZRLAA0	Controller Test Part 1
CZRLBA0	Controller Test Part 2
CZRLCA0	Drive Test Part 1
CZRLDA0	Drive Test Part 2
CZRLEA0	Performance Exerciser
CZRLFA0	Drive Compatibility Test

These diagnostics can be run free-standing, under the Diagnostic Supervisor, manually under XXDP, chainable under XXDP (except CZRLFA0 which requires manual intervention), or under manufacturing checkout environments such as SLIDE or ACT 11.

A new diagnostic package is available to test either an RL01 or an RL02 unit. The kit numbers are listed in Table 2-5 and the contents of the tests are shown in Table 2-6.

There is a new program added to the package named CZRLMA0. It is used to read the Bad Sector File and can be used to write entries into the field writable portion of the Bad Sector File. This program is not a diagnostic and should not be used as one. It assumes that the system is functioning properly.

Table 2-5 RL11 Diagnostic Kit Numbers

PART NUMBER	DESCRIPTION
ZI283-RB	Documentation and Paper Tape
ZI283-RZ	Documentation Only
ZI283-PB	Paper Tape Only
ZI283-FR	Microfiche Only

Table 2-6 RL11 Diagnostic Components

PART NUMBER	NAME	ITEM
AC-F111A-MC	CZRLGA0 CONTROLLER TEST #1	DOCUMENTATION
AH-F110A-MC		FICHE
AK-F108A-MC		PAPER TAPE #1
AK-F109A-MC		PAPER TAPE #2
AF-F111A-M0		DECO
AC-F115A-MC	CZRLHA0 CONTROLLER TEST #2	DOCUMENTATION
AH-F114A-MC		FICHE
AK-F112A-MC		PAPER TAPE #1
AK-F113A-MC		PAPER TAPE #2
AF-F115A M0		DECO
AC F119A MC	CZRLIA0 DRIVE TEST #1	DOCUMENTATION
AH-F118A MC		FICHE
AK F116A MC		PAPER TAPE #1
AK F117A MC		PAPER TAPE #2
AF F119A M0		DECO
AC-F123A-MC	CZRLJA0 DRIVE TEST #2	DOCUMENTATION
AH-F122A-MC		FICHE
AK-F120A-MC		PAPER TAPE #1
AK-F121A-MC		PAPER TAPE #2
AF-F123A-M0		DECO
AC-F127A-MC	CZRLKA0 PERFORMANCE EXERCISER	DOCUMENTATION
AH-F126A-MC		FICHE
AK-F124A-MC		PAPER TAPE #1
AK-F125A-MC		PAPER TAPE #2
AF-F127A-M0		DECO
AC-F131A MC	CZRLLA0 DRIVE COMPATIBILITY TEST	DOCUMENTATION
AH-F130A MC		FICHE
AK-F128A MC		PAPER TAPE #1
AK F129A-MC		PAPER TAPE #2
AF F131A-M0		DECO
AC F135A-MC	CZRLMA0 BAD SECTOR FILE UTILITY	DOCUMENTATION
AH F134A-MC		FICHE
AK F132A-MC		PAPER TAPE#1
AK-F133A-MC		PAPER TAPE #2
AF-F135A-M0		DECO

In addition to the free-standing diagnostics, there is a DECX11 module for use with the DECX11 System Exerciser. The current revision is designated RLAA and is in DECX11 Option Library #5 DXQLO. Revision A (RLAA) will operate an RL01 drive only. Revision B (RLAB) will operate either an RL01 or an RL02.

There is also an RL subsystem driver for the Maintenance Program Generator (MPG).

The binary form of the diagnostics is included as part of XXDP. This makes them available on media for the RK05, RK06, RK07, RL01, RX01, DECtape, magnetic tape, and DECassette.

The use of XXDP, DECX11, and MPG is explained in the manuals listed in Table 2-7.

Table 2-7 User Documents

PART NUMBER HARD COPY	PART NUMBER MICROFICHE	NAME
AC-9093I-MC	FP DZQXA J D	CZQXAA0 XXDP USER GUIDE
AC-8240Z-MC	AH 8242Z MC	CXQBAZ0 DECX11 USER DOCUMENT
AC-816JC-MC	FP-DTUMA-C D	CTUMAC0 M.P.G. USER MANUAL

2.8.2 RLV11-Based Diagnostics

The RLV11 Controller based subsystem is tested with the same set of diagnostics as the RL11 Controller subsystem with the following exception. The RLV11 has an internal maintenance feature that is not tested by the RL11 diagnostics so there is one additional diagnostic program called the CRVLAA0 Diskless Test. It should be run first.

The diagnostic kit includes the same items as the RL11 diagnostic kit plus the CVRLAA0 test. The RLV11 kit designations are shown in Table 2-8.

Table 2-8 RLV11 Diagnostic Kit Designations

DESIGNATION	CONTENTS
ZJ285-RB	Documentation and Paper Tape
ZJ285-RZ	Documentation Only
ZJ285-PB	Paper Tape Only
ZJ285-UR	Microfiche Only

The DECX11 module is the same one used for the RL11.

2.8.3 RL8A-Based Diagnostics

There are six free-standing diagnostic programs for the RL8/RL01 system. There is also a DECX8 module for use with the DECX8 system exerciser. These diagnostics are available in a kit (see Table 2-9) or as individual components (see Table 2-10) and are for use with RL01 only.

Table 2-9 RL8/RL01 Diagnostic Kits

PART NUMBER	CONTENTS
ZB233-RB	Documentation and Paper Tape
ZB233-RZ	Documentation Only
ZB233-PB	Paper Tape Only
ZB233-UR	Microfiche

Table 2-10 RL8/RL01 Diagnostic Components

PART NUMBER	DESIGNATION
AC-C656A-MA	AJRLAA0, RL8A DISKLESS CONTROL TEST (DOC)
AH-C657A-MA	AJRLAA0, RL8A DISKLESS CONTROL TEST (FICHE)
AK-C658A-MA	AJRLAA0, RL8A DISKLESS CONTROL TEST (P. TAPE)
AL-C659A-NA	AJRLAA0, RL8A DISKLESS CONTROL TEST (DECTAPE)
AC-C660A-MA	AJRLBA0, RL8A/RL01 DRIVE TEST 1 (DOCUMENT)
AH-C661A-MA	AJRLBA0, RL8A/RL01 DRIVE TEST 1 (FICHE)
AK-C662A-MA	AJRLBA0, RL8A/RL01 DRIVE TEST 1 (P. TAPE)
AL-C663A-NA	AJRLBA0, RL8A/RL01 DRIVE TEST 1 (DECTAPE)
AC-C664A-MA	AJRLCA0, RL8A/RL01 DRIVE TEST 2 (DOCUMENT)
AH-C665A-MA	AJRLCA0, RL8A/RL01 DRIVE TEST 2 (FICHE)
AK-C666A-MA	AJRLCA0, RL8A/RL01 DRIVE TEST 2 (P. TAPE)
AL-C667A-NA	AJRLCA0, RL8A/RL01 DRIVE TEST 2 (DECTAPE)
AC-C668A-MA	AJRLDA0, RL8A/RL01 COMPAT. VERIFY (DOCUMENT)
AH-C669A-MA	AJRLDA0, RL8A/RL01 COMPAT. VERIFY (FICHE)
AK-C670A-MA	AJRLDA0, RL8A/RL01 COMPAT. VERIFY (P. TAPE)
AL-C671A-NA	AJRLDA0, RL8A/RL01 COMPAT. VERIFY (DECTAPE)
AC-C672A-MA	AJRLEA0, RL8A/RL01 PERF. EXER. (DOCUMENT)
AH-C673A-MA	AJRLEA0, RL8A/RL01 PERF. EXER. (FICHE)
AK-C674A-MA	AJRLEA0, RL8A/RL01 PERF. EXER. (P. TAPE)
AL-C675A-NA	AJRLEA0, RL8A/RL01 PERF. EXER. (DECTAPE)
AC-C676A-MA	AXRLAA0, RL8A DECX8 MODULE (DOCUMENT)
AH-C677A-MA	AXRLAA0, RL8A DECX8 MODULE (FICHE)
AK-C678A-MA	AXRLAA0, RL8A DECX8 MODULE (P. TAPE)
AC-C680A-MA	AJRLGA0, RL8A/RL01 PACK VERIFY (DOCUMENT)
AH-C681A-MA	AJRLGA0, RL8A/RL01 PACK VERIFY (FICHE)
AK-C682A-MA	AJRLGA0, RL8A/RL01 PACK VERIFY (P. TAPE)
AL-C683A-NA	AJRLGA0, RL8A/RL01 PACK VERIFY (DECTAPE)

There are six free-standing diagnostic programs for the RL8/RL02 subsystem, plus a module for use with the DECX8 System Exerciser. They are available in kit form (Table 2-11) or as individual components (Table 2-12). The Diskless Controller Test AJRLAC0 is simply Revision C of the RL01 test and can test a subsystem with either RL01 or RL02 units. The other diagnostics test RL02-based systems only.

Table 2-11 RL8/RL02 Diagnostic Kits

PART NUMBER	CONTENTS
ZF241-RZ	DOCUMENTATION
ZF241-RB	DOCUMENTATION AND PAPER TAPE
ZF241-PB	PAPER TAPE
ZF241-FR	FICHE
ZF241-PH	RL02
ZF241-RH	RL02 AND DOCUMENTATION

Table 2-12 RL8/RL02 Diagnostic Components

PART NUMBER	NAME	ITEM
AC-C656C-MA	AJRLAC0 RL8A DISKLESS CONTROL TEST	DOCUMENTATION
AH-C657C-MA		FICHE
AK-C658C-MA		PAPER TAPE
AL-C659C-NA		DEC TAPE
AC-F362A-MA	AJRLIA0 RL8/RL02 SEEK/FUNCTION	DOCUMENTATION
AK-F363A MA		PAPER TAPE
AH F364A MA		FICHE
AL F365A-MA		DEC TAPE
AF-F362A-M0		DECO/DEPO
AC-F366A-MA	AJRLIA0 RL8/RL02 READ/WRITE	DOCUMENTATION
AK-F367A-MA		PAPER TAPE
AH-F368A-MA		FICHE
AL F369A MA		DEC TAPE
AF F366A M0		DECO/DEPO
AC-F370A-MA	AJRLJA0 RL8/RL02 DRIVE COMPAT	DOCUMENTATION
AK-F371A-MA		PAPER TAPE
AH-F372A-MA		FICHE
AL-F373A-MA		DEC TAPE
AF-F370A-M0		DECO/DEPO
AC-F374A-MA	AJRLKA0 RL8/RL02 PERF. EXER.	DOCUMENTATION
AK-F375A-MA		PAPER TAPE
AH-F376A-MA		FICHE
AL-F377A-MA		DEC TAPE
AF F374A M0		DEPO/DECO
AC F378A MA	AJRLLA0 RL8/RL02 PACK VERIFY	DOCUMENTATION
AK F379A MA		PAPER TAPE
AH-F380A-MA		FICHE
AL-F381A-MA		DEC TAPE
AF F378A M0		DECO/DEPO
AC F382A MA	AXRLBA0 DEC/X8 MOD RL8/RL02	DOCUMENTATION
AK F383A MA		PAPER TAPE
AH-F384A-MA		FICHE
AF-F382A-M0		DECO/DEPO

2.9 USE OF THE M9312 BOOTSTRAP WITH AN RL11 SUBSYSTEM

The M9312 module is used on many PDP-11 Unibus systems to provide bootstrap capability as well as other functions. The module has five IC sockets for ROM chips, four of which are reserved for peripheral bootstrap programs. There are several ROM chips available for the different peripheral devices, and an M9312 is configured by selecting the appropriate chips for the particular system on which it is used.

The RL subsystem bootstrap program is contained in ROM chip number 23-751A9. This chip can be ordered individually and is also available in kit MR11-EA, which consists of an M9312 module plus all the available ROM chips.

An RL system disk can be booted by a command to the console emulator (a program that is a feature of the M9312). The device mnemonic for the RL11 is DL or DLn, where n is the unit number (0 through 3).

More information on the M9312 is available in the *M9312 Technical Manual*. It is available in printed form (EK-M9312-TM) or on microfiche (EP-M9312-TM).

CHAPTER 3
OPERATOR'S GUIDE

3.1 INTRODUCTION

This chapter describes the function of all external controls available to the user of the RL01/RL02 Disk Drive and explains how to operate the subsystem.

3.2 CONTROLS AND INDICATORS

Figures 3-1 and 3-2 show all the drive controls and indicators.

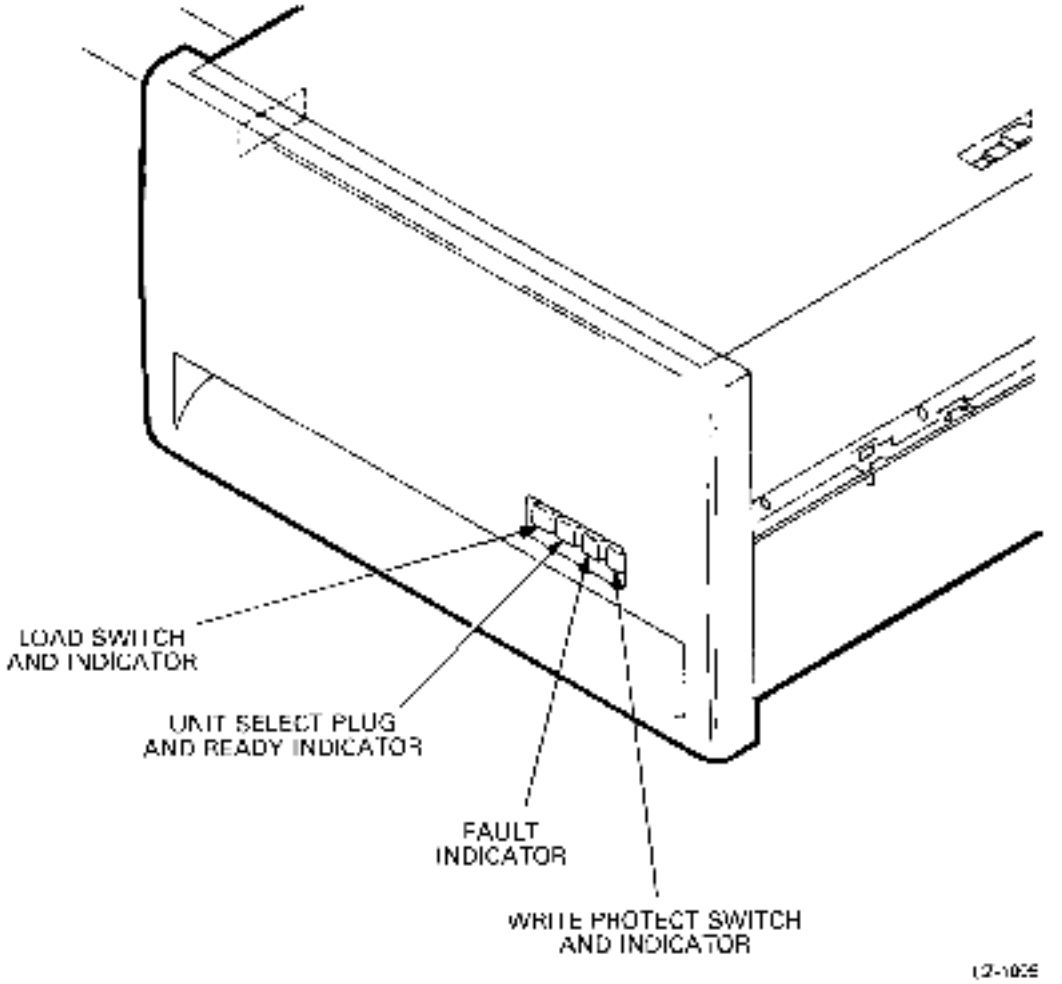


Figure 3-1 RL01/RL02 Disk Drive — Front View

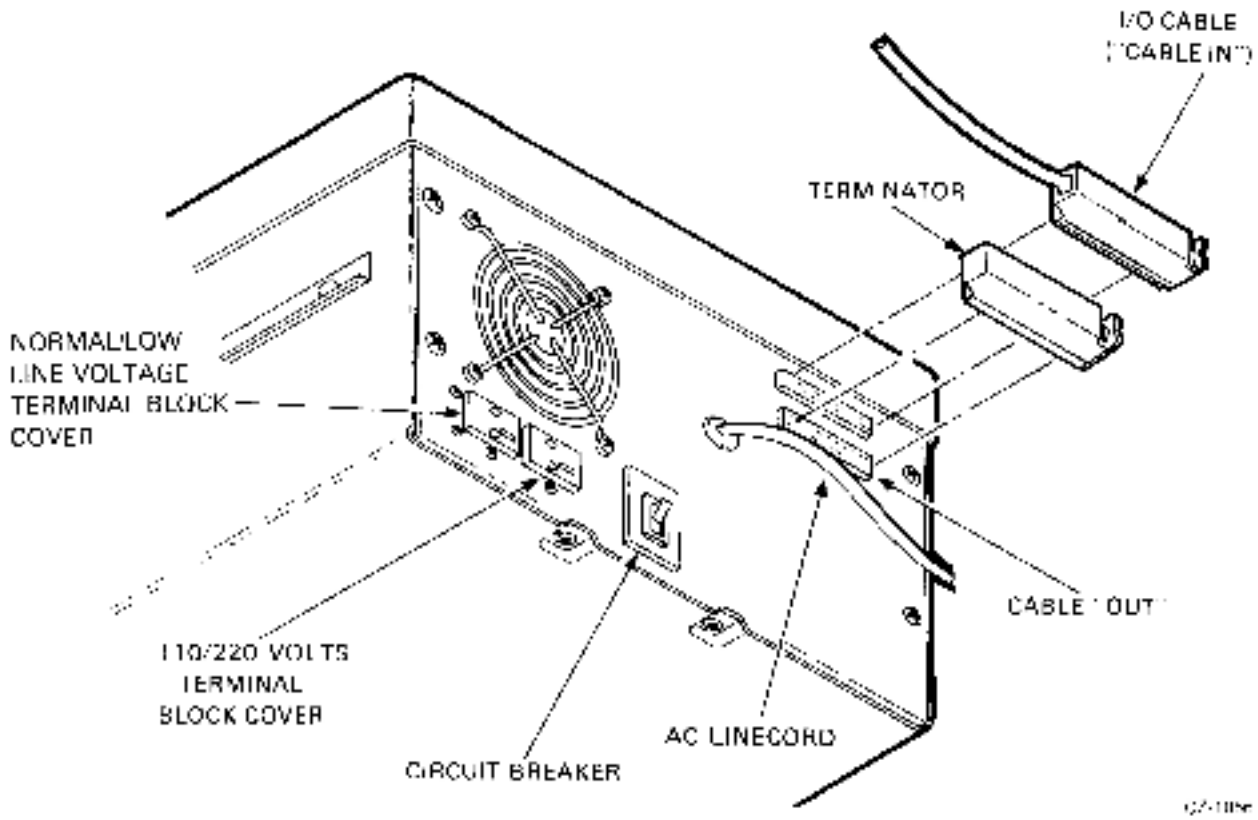


Figure 3-1 RL01/RL02 Disk Drive – Rear View

3.2.1 Power ON/OFF Circuit Breaker

When the power plug is inserted into the proper ac outlet, ac power is applied to the rear panel circuit breaker on the drive. When the circuit breaker is switched ON, ac power is applied to the drive and the fan is energized.

3.2.2 Run/Stop Switch with LOAD Indicator

This push on/push off switch, when pressed in, energizes the spindle motor providing the following conditions have been met.

- The RL01K/RL02K cartridge has been installed.
- The cartridge protective cover is in place and the cartridge access door is closed.
- All ac and dc voltages are within specifications.
- The read/write heads are home (retracted).
- The brushes are home.

When this switch is released, the spindle drive motor is deenergized if the read/write heads are not loaded. If the heads are loaded, they are immediately retracted and the spindle drive motor is then deenergized. In the event of a main power interrupt and subsequent power restoration, the drive will cycle up if the switch is ON since it contains mechanical memory.

The LOAD indicator is illuminated whenever:

- The spindle is stopped
- The read/write heads are home
- The brushes are home
- The spindle drive motor is not energized.

3.2.3 UNIT SELECT Switch with READY Indicator

The UNIT SELECT switch is a cam-operated switch that is actuated by inserting a numbered, cammed button. The switch contacts are binary encoded so the drive interface logic recognizes the UNIT SELECT number (0, 1, 2 or 3).

The UNIT SELECT indicator, when lit, indicates a drive READY condition. This condition exists when:

- The read/write heads are loaded
- The heads are detented on a specific track.

3.2.4 FAULT Indicator

The FAULT indicator is lit whenever the following fault or error conditions develop in the disk drive:

- Drive Select Error
- Seek Time Out Error
- Write Current in Heads During Sector Time Error
- Loss of System Clock (this condition is not latched and not represented in status word)
- Write Protect Error
- Write Data Error
- Spin Error

NOTE
Volume Check does not light the FAULT Indicator but does cause DRIVE ERROR.

3.2.5 WRITE PROTECT Switch and Indicator

This push on/push off switch is used to set the WRITE PROTECT condition if it had been reset or to reset the WRITE PROTECT condition if it was set. The switch unit contains a light that is on when the WRITE PROTECT condition is set.

3.3 OPERATING PROCEDURES

This paragraph explains how to load a cartridge into a disk drive and how to cycle up the drive to put the subsystem on-line. The cycle-up procedure assumes that ac power is available, the drive ac circuit breaker is on (muffin fan is energized), system power is on and the LOAD indicator on the drive control panel is on.

3.3.1 Cartridge Loading and Drive Startup Procedure

1. Raise the drive access cover.

2. Prepare a cartridge (Figure 3-3) for loading as follows:

   a. Lift the cartridge by grasping the top cover handle with the right hand.

   b. Support the cartridge with the left hand holding the protection cover.

   c. Lower the top cover handle and push the handle slide to the left with the thumb of the right hand. Again, raise the handle to its full upright position to release the protection cover.

d. Lift the cartridge from the protection cover and carefully seat the cartridge on the spindle with the top cover handle recess facing the rear of the machine.

e. Carefully rotate the top cover handle back and forth to ensure that the spindle locating arms are seated properly within the cartridge housing detent slots.

CAUTION

Use care when seating the cartridge on the drive spindle. Rough handling of the cartridge may cause damage to the spindle/cartridge interface which, in turn, can cause excessive cartridge runout and positioning errors.

f. Gently lower the top cover handle to a horizontal position to engage the cartridge on the drive spindle.

g. Place the protection cover on top of the cartridge.

h. Close the drive access cover.

3. Start the drive as follows:

a. Press the run/stop switch (LOAD indicator).

b. When the drive has completed the drive startup sequence and the read/write heads are detented on cylinder 0, the READY indicator on the numbered UNIT SELECT switch will be illuminated.

c. If write protection is desired, press the WRITE PROTECT switch.

3.3.2 Cartridge Unloading Procedure

1. Power down the drive as follows.

a. Press the run/stop switch and wait approximately 30 seconds for the LOAD indicator to illuminate.

b. Raise the drive access cover.

2. Remove the cartridge as follows.

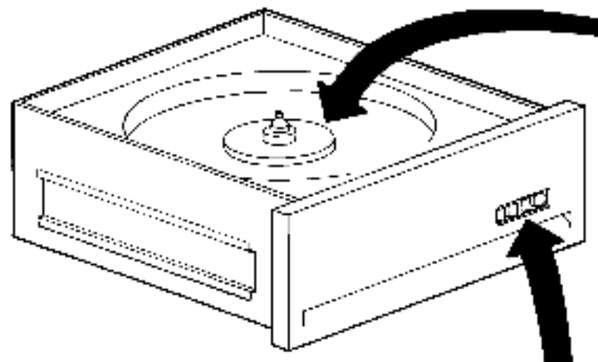
a. Remove the cartridge protection cover and hold the cover in the left hand.

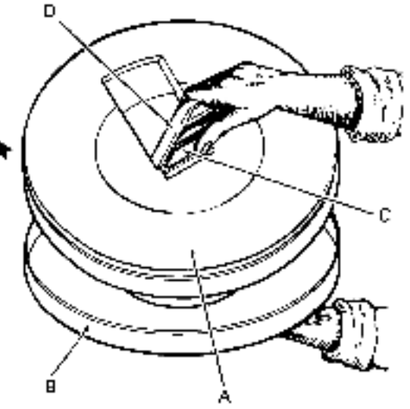
b. Push the top cover handle slide to the left with the thumb before raising the handle.

c. Raise the top cover handle to a full upright position to release the cartridge from the drive spindle.

d. Carefully lift the cartridge up and out of the drive and place it in the protection cover.

e. Lower the top cover handle to the horizontal position to lock the protection cover in place.





TO READY DRIVE

- RAISE CARTRIDGE ACCESS DOOR
- LOAD CARTRIDGE
- CLOSE ACCESS DOOR
- DEPRESS RUN/STOP SWITCH (LOAD INDICATOR)
- AFTER 30 SECONDS, UNIT SELECT INDICATOR SHOULD LIGHT INDICATING DRIVE IS READY TO READ OR WRITE
- IF WRITE PROTECTION IS DESIRED, DEPRESS WRITE PROTECT SWITCH (PROTECT INDICATOR)

DRIVE INDICATORS

LOAD:
LIGHTS TO INDICATE THAT CARTRIDGE MAY BE LOADED OR THAT SPINDLE IS STOPPED.

UNIT SELECT:
INDICATES LOGICAL DRIVE ADDRESS WHEN LIT. INDICATES DRIVE IS READY TO READ, WRITE OR RECEIVE CONTROLLER COMMANDS.

FAULT
WHEN LIT, INDICATES A DRIVE ERROR CONDITION. IF THIS CONDITION PERSISTS, SEEK ASSISTANCE.

WRITE PROTECT:
WHEN LIT, INDICATES THAT CARTRIDGE CURRENTLY MOUNTED IS WRITE PROTECTED

TO LOAD CARTRIDGE:

- SUPPORT CARTRIDGE "A" WITH LEFT HAND HOLDING PROTECTION COVER "B"
- PUSH HANDLE SLIDE "C" TO LEFT WITH THUMB OF RIGHT HAND.
- RAISE COVER HANDLE "D" TO FULL UPRIGHT POSITION, RELEASING PROTECTION COVER "B"
- LIFT CARTRIDGE "A" FROM PROTECTION COVER "B" AND CAREFULLY SEAT IT ON DRIVE SPINDLE WITH HANDLE RECESS FACING REAR OF DRIVE
- CAREFULLY ROTATE TOP COVER HANDLE "D" A FEW DEGREES CLOCKWISE AND COUNTER-CLOCKWISE TO ENSURE FIRM SEATING.
- GENTLY LOWER TOP COVER HANDLE "D" TO HORIZONTAL POSITION TO ENGAGE CARTRIDGE ON DRIVE SPINDLE.
- PLACE PROTECTION COVER "B" ON TOP OF CARTRIDGE

C7-2052

Figure 3-3 Cartridge Loading Procedure

3.4 OPERATOR MAINTENANCE

3.4.1 Introduction

User maintenance procedures are limited to the care and cleaning (external) of the disk cartridge, and the cleaning of the drive spindle assemblies.

3.4.2 Professional Cartridge Cleaning

Cartridges should be professionally cleaned every six months, or whenever practical. Complete cartridge cleaning procedures must be performed by either qualified DIGITAL Field Service personnel or by a professional cleaning service. Application of cleaning procedures to the recording surfaces by unqualified personnel may void not only the warranty on the serviced cartridge, but the warranty for any drive on which the cartridge is operated.

3.4.3 User Cartridge Cleaning

The user should clean the outer sides of a completely assembled cartridge by using a lint-free wiper, dampened with a solution of 9 percent water and 91 percent isopropyl alcohol. However, the cartridge must not be saturated and all excess solvent must be removed with a dry wiper. This procedure is necessary to prevent solvent from entering the seams of the assembly and contaminating the platter.

CAUTION

For cleaning purposes, use only a solution of 9 percent water with 91 percent isopropyl alcohol. Water, trichloroethylene, or other solvents are not permitted.

3.4.4 Spindle Asssembly Cleaning

Using a lint-free wiper, dampened with the isopropyl alcohol solution, clean the spindle cone prior to loading the cartridge. However, do not saturate the assembly; remove all excess solvent with a dry wiper. This procedure is necessary to prevent solvent from entering a loaded cartridge and contaminating the platter. In addition, ensure that the shroud is as free of lint and dust as possible before loading a cartridge. Dry lint and dust may be blown from the spindle area using filtered, dry air. However, do not use plant air that may contain water or oil; canned air is an acceptable substitute.

3.5 CARTRIDGE CARE SUMMARY

The following listing summarizes care and cleaning considerations for the RL01K/RL02K Disk Cartridge.

- Keep cartridges clean.
- Use cartridges at computer room temperature only.
- Manipulate cartridges by the top cover handle only.
- When the protection cover is removed (for loading), do not touch disk surfaces, hub center cone, or surfaces.
- When the protection cover is removed (for loading), interior metal hub surfaces must be clean.

- When the protection cover is removed (for loading), ensure that the disks are not moved or rotated, since improper disk motion may generate plastic particles which can result in disk damage.

- When loading or unloading a drive, insert and remove cartridges gently. In addition, do not use excessive force when manipulating the top cover handle.

- If, during operation, a cartridge makes rumbling or continuous tinging sounds, discontinue use of the cartridge. Use of a damaged cartridge on other drives may damage the drives, resulting in additional damage to all other cartridges used in those drives.

- Each cartridge should be cleaned professionally every six months and/or whenever a specific cartridge is not operating properly.

- Cartridges are factory repairable only. Disassembly in the field is not permitted, and such action may void the warranty on a cartridge, as well as any drive on which the cartridge may be operated.

CHAPTER 4
RL11/RLV11 PROGRAMMING INFORMATION

4.1 GENERAL DESCRIPTION

This chapter describes the RL11 and RLV11 Controllers and points out any differences.

4.1.1 RL11 Controller Description

The RL11 Controller consists of a single hex-height M7762 module. It can be installed in any hex-height small peripheral controller (SPC) slot. This controller provides a programmable interface between the PDP-11 UNIBUS and the RL01/RL02 Disk Drive(s). The controller has four addressable registers that are detailed in Paragraph 4.2. The controller can give any one of seven commands to the drive. These controller commands are explained in detail in Paragraph 4.3.
page 4-2

In addition to the registers and control logic, the RL11 Controller contains a sixteen word silo I/O buffer. Although the buffer is invisible to the programmer, its capacity is one of the differences between the RL11 and RLV11. The RLV11 has a 256 RAM I/O buffer.

4.1.2 RLV11 Controller Description

The RLV11 Controller consists of 2 quad-height modules designated M8013 and M8014. This controller provides a programmable interface between the LSI-11 Q-Bus and the drive(s). Like the RL11, the RLV11 has four addressable registers that are explained in detail in Paragraph 4.2. The RLV11 can give any one of eight commands to the drive. The RLV11 has one command (maintenance command) that the RL11 does not have. These commands are explained in Paragraph 4.3. The RLV11 has a 256 word RAM first in, first out (FIFO) I/O buffer while the RL11 has a 16 word silo.

4.2 ADDRESSABLE REGISTERS

There are four addressable registers in the controller that are used to control and monitor the operation within the controller itself and within the disk drive unit(s). These are described briefly in Table 4-1 and described in detail in the following text.

4.2.1 Control Status Register

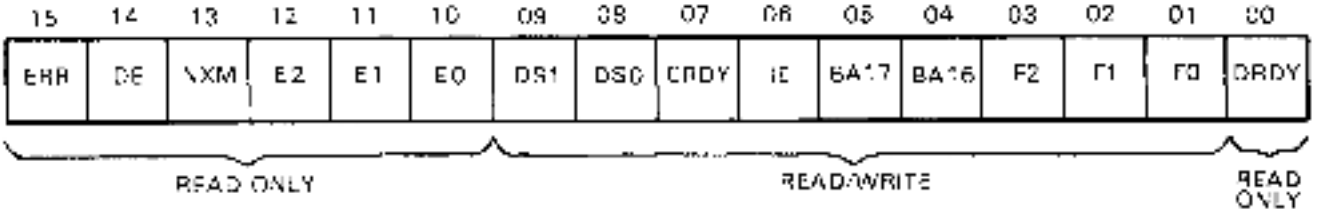
The Control Status (CS) register (Figure 4-1) is a 16-bit register with an address of 774400. Bits 1 through 9 can be read or written; the other bits can only be read.

When the controller is initialized, bits 1-6 and 8-13 are cleared and bit 7 is set. Bit 0 is set whenever the selected drive is in the ready condition; otherwise, the bit is cleared. Bit 14 is set whenever there is a drive error; it is cleared when the drive error is corrected or the drive error is cleared by a Get Status command. Bit 15 is set when there is a drive or controller error (indicated in bits 10-14).

Table 4-1 Controller Addressable Registers

Address (octal)	Type (read/write)	Register Name/Mnemonic	Basic Function
777400	R/W	Control Status (CS)	Indicates drive ready condition; decodes drive commands and provides overall control functions and error indications.
777402	R/W	Bus Address (BA)	Indicates memory location involved in data transfer during a normal read or write operation.
777404	R/W	Disk Address (DA)	Stores information for: (1) seeking to desired track; or (2) selecting sectors to be transferred during read/write operations, or (3) used when requesting a drive status message.
777406	R/W	Multipurpose (MP)	(1) Functions as word counter when transferring read/write data between UNIBUS and drives; or (2) acts as storage buffer when reading drive status; or (3) stores header information from controller silo when executing a read header command.

CONTROL STATUS REGISTER (CSR)



CS-2009

Figure 4-1 CS Register

Bit(s)	Name	Function
0	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a seek operation is initiated and set when the seek operation is completed.
1-3	Function Code	These bits are set by software to indicate the command to be executed. Command execution requires that bit 7 (controller ready) be cleared by software. A zero bit being transferred into bit 7 of the CSR can be considered as a Go bit.

Bit(s)	Name	Function				
1-3	Function Code (Cont)	F2	F1	F0	Command	Octal Code
		0	0	0	No Op (RL11) or Maint. (RLV11)	0
		0	0	1	Write Check	1
		0	1	0	Get Status	2
		0	1	1	Seek	3
		1	0	0	Read Header	4
		1	0	1	Write Data	5
		1	1	0	Read Data	6
		1	1	1	Read Data Without Header Check	7
4-5	Bus Address Extension Bits (BA16, BA17)	The two most significant bus address bits. Read and written as data bits 4 and 5 of the CS register but considered as address bits 16 and 17 of the bus address register (see Paragraph 4.3.2)				
6	Interrupt Enable (IE)	When this bit is set by software, the controller is allowed to interrupt the processor at the normal command or error termination.				
7	Controller Ready (CRDY)	When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. When set, this bit indicates the controller is ready to accept another command.				
8-9	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.				
10	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed within 200 ms.				
11	Data CRC (DCRC) or Header CRC (HCRC) or Write Check (WCE)	If OPI (bit 10) is cleared and this bit is set, a CRC error has occurred when reading the data (DCRC). If OPI (bit 10) is set and bit 11 is also set, the CRC error has occurred on the header (HCRC). If OPI (bit 10) is cleared and bit 11 is set and the function command was a write check, a write check error (WCE) has occurred. **NOTE** **Cyclic redundancy checking is performed on the first and second header words, even though the second header word always contains zeros.**				
12	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write when the silo is empty but the word count has not yet reached zero (meaning that the bus request was ignored for too long). The OPI bit will not be set. This bit will be set during a read when the silo is full (meaning that the word being read could not enter the silo and the bus request has been ignored for too long). The OPI bit will not be set.				

Bit(s)	Name	Function
12	Data Late (DLT) or Header Not Found (HNF) (Cont)	When this bit and OPI are both set, a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare = HNF).

ERROR SUMMARY

	Bits		
Error Name	**12**	**11**	**10**
OPI	0	0	1
Read Data CRC	0	1	0
Write Check	0	1	0
Header CRC	0	1	1
Data Late	1	0	0
Header Not Found	1	0	1

13	Non Existent Memory (NXM)	This bit is set when the addressed memory does not respond within 10 to 20 microseconds of the beginning of a direct memory access (DMA) data transfer.
14	Drive Error (DE)	This bit is tied directly to the DE interface line. When set, it indicates that the selected drive has flagged an error. (The source of the error can be determined by executing a Get Status command.) DE can be cleared by executing a Get Status command with bit 3 of the DA register set.
15	Composite Error (ERR)	When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CS) is set and an error occurs (which sets bit 7), an interrupt will be initiated.

4.2.2 Bus Address Register

The Bus Address (BA) register (Figure 4-2) is a 16-bit register with an address of 774402. Bits 1 through 15 can be read or written; bit 0 is always zero. Bus address bits 16 and 17 are contained in bits 4 and 5 of the CS register (see Paragraph 4.2.1).

The BA register indicates the memory location involved in the data transfer during a normal read or write operation. The contents of the BA register are automatically incremented by two as each word is transferred between the bus and the I/O buffer. This register overflows into CS register bits 4 and 5.

The BA register is cleared by initializing the drive or by loading the register with zeros.

BUS ADDRESS REGISTER (BAR)

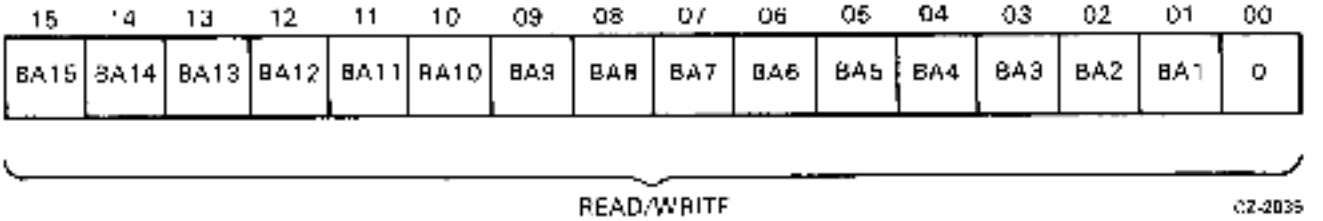


Figure 4-2 BA Register

Bit(s)	Name	Function
0-15	BA0 thru BA15	These bits point to the UNIBUS address that data is to be transferred to/from (normally a memory address). BA16 and BA17 are in CSR bits 4 and 5.

4.2.3 Disk Address Register

The Disk Address (DA) register is a 16-bit register with an address of 7744414. Its contents can have one of three meanings, depending on the function being performed. This register is cleared by initializing the device or loading the register with zeros. All 16 bits can be read or written by the processor.

4.2.3.1 DA Register During a Seek Command – To perform a Seek function, it is necessary to provide cylinder address difference, head select, and head directional information to the selected drive as indicated (Figure 4-3).

DAR DURING SEEK COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DF8	DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0	0	0	HS	0	DIR	0	1

CT-2006

Figure 4-3 DAR – Seek Command

Bit(s)	Name	Function
0	-	Must be a 1.
1	-	Must be a 0.
2	Direction (DIR)	This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).
3		Must be a 0
4	Head Select (HS)	Indicates which head (disk surface) is selected. A one indicates the lower head; a zero, the upper head.
5-6	-	Reserved.
7-15	Cylinder Address Difference DF 08:00	Indicates the number of cylinders the heads are to move on a seek.

4.2.3.2 DA Register During Read or Write Data Command – For a read or write operation, the DA register is loaded with the address of the first sector to be transferred. As each successive sector is transferred, the DA register is automatically incremented (Figure 4-4).

DAR DURING READING OR WRITING DATA COMMANDS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

CZ-0011

Figure 4-4 Read/Write Data Command

Bit(s)	Name	Function
0-5	Sector Address SA (05:00)	Address of one of the 40 sectors on a track.
6	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.
7-15	Cylinder Address CA (08:00)	Address of the cylinders being accessed. (Range is 0 through 777, octal)

4.2.3.3 DA Register During a Get Status Command – For a Get Status command, the DA register bits must be programmed as follows (Figure 4-5):

DAR DURING GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

CZ-0007

Figure 4-5 DAR – Get Status Command

Bit(s)	Name	Function
0	-	Must be a 1.
1	Get Status (GS)	Must be a 1, indicating to the drive that the status word is being requested. At the completion of the Get Status command, the drive status word is read into the controller Multipurpose (MP) register (see Paragraph 4.2.4). With this bit set, the drive ignores bits 8-15.
2	-	Must be a 0.
3	Reset (RST)	When this bit is set, the drive clears its error register before sending a status word to the controller.
4-7	-	Must be a 0.
8-15	-	Not used during a Get Status.

4.2.4 Multipurpose Register

The multipurpose (MP) register is a 16 bit register with an address of 744406. This register has several different bit meanings, as explained below.

4.2.4.1 MP Register After a Get Status Command – When a Get Status command (Figure 4-6) is executed the status word is returned to the controller and transferred to the MP register. The contents of the MP register are defined as follows.

MPR AFTER GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WDE	CHE	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	CO	HO	BH	STC	STB	STA

CZ-2012

Figure 4-6 MPR – Status Word

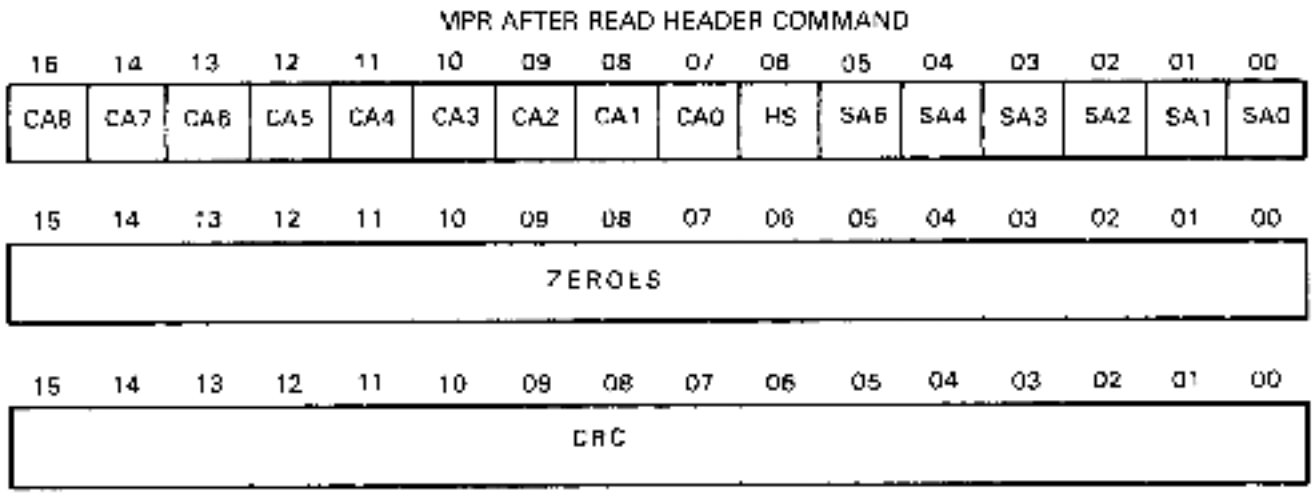
Bit(s)	Name	Function
0-2	State C:A ST C:A	These bits define the state of the drive.

C	B	A	
0	0	0	Load Cartridge
0	0	1	Spin Up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek
1	0	1	Lock On
1	1	0	Unload Heads
1	1	1	Spin Down

3	Brush Home (BH)	Set when the brushes are home.
4	Heads Out (HO)	Set when the heads are over the disk.
5	Cover Open (CO)	Set when the drive access cover is open or the dust cover is not in place.
6	Head Select (HS)	Indicates the currently selected head. A zero indicates the upper head; a one, the lower head.
7	Drive Type (DT)	A zero indicates an RL01; a one, an RL02.
8	Drive Select Error (DSE)	Set when a multiple drive selection is detected
9	Volume Check (VC)	Set when a cartridge is mounted and spun up. Cleared by execution of a Get Status command with Bit 3 asserted.

Bit(s)	Name	Function
10	Write Gate Error (WGE)	Set during Write Gate if one or more of the following conditions occur. • Drive is not "ready to read/write" • Drive is write protected • Sector pulse is occurring • Drive has another error
11	Spin Error (SPE)	Set when spindle has not reached speed in the required time during spin-up or when spindle speed is too high.
12	Seek Time Out (SKTO)	Set when the heads do not come on track in the required time during a Seek command or when "ready to read/write" is lost while the drive is in position (lock on) mode.
13	Write Lock (WLK)	Set when the drive is write protected.
14	Current Head Error (CHE)	Set if write current is detected in the heads when Write Gate is not asserted.
15	Write Data Error (WDE)	Set if Write Gate is asserted but no transitions are being detected on the Write Data line.

4.2.4.2 MP Register After a Read Header Command — When a Read Header command is executed, the next header will be read and its three words will be stored in the data buffer and transferred to the MP register. The first word will contain sector address, head select, and cylinder address information. The second word will contain all zeros. The third word will contain the header CRC information. All three words can be read sequentially by the program (Figure 4-7).



CZ-2013

Figure 4-7 MPR – Three Header Words

Bit(s)	Name	Function
0-5	SA	Sector Address
6	HS	Head Select
7-15	CA	Cylinder Address

4.2.4.3 MP Register During Read/Write Data Commands – Before the reading or writing data, the program should load the word count into the MP register in two's complement form. The counter is incremented as each word is transferred. Usually, the reading or writing operation is terminated when the word counter reaches zero (overflows). The word counter can keep track of any number of data words, from one to the full 40-sector count of 5120 data words (decimal) (Figure 4-8).

MPR DURING READ/WRITE COMMANDS FOR WORD COUNT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	WC12	WC11	WC10	WC9	WC8	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

CZ 2096

Figure 4-8 MPR – Used as a Word Counter

Bit(s)	Name	Function
0-12	Word Count WC 12:00	Contains the two's complement of total number of words to be transferred.
13-15		Must be ones.

MP Register Programming Note – The RL01/RL02 Disk Drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. Program the data transfer to terminate at the end of the last sector of the track.

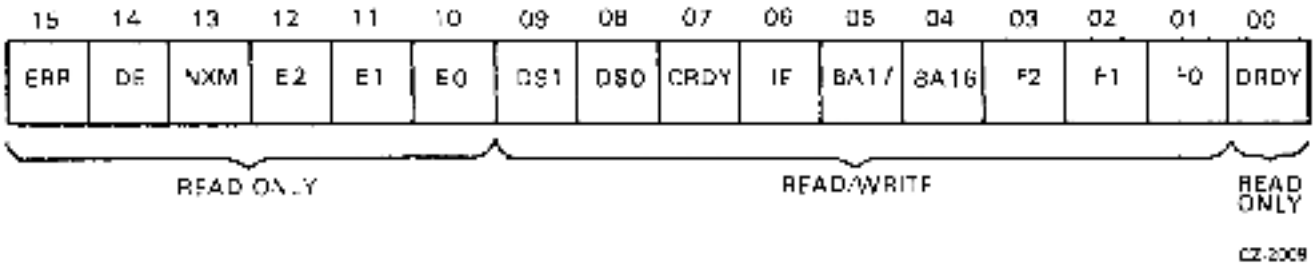
2. Program a seek to the next track. This can be either a head switch to the other surface but same cylinder or a head switch and move to the next cylinder.

3. Program the data transfer to continue at the start of the first sector at the next track.

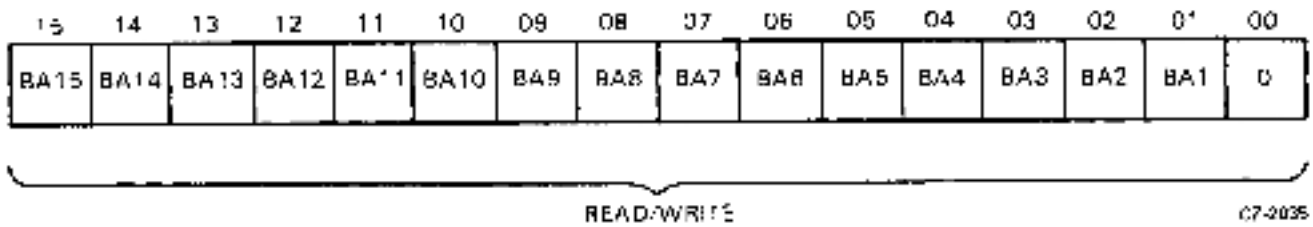
4.2.5 Register Summary

Figure 4-9 is a bit and function summary of the CS, BA, DA, and MP registers.

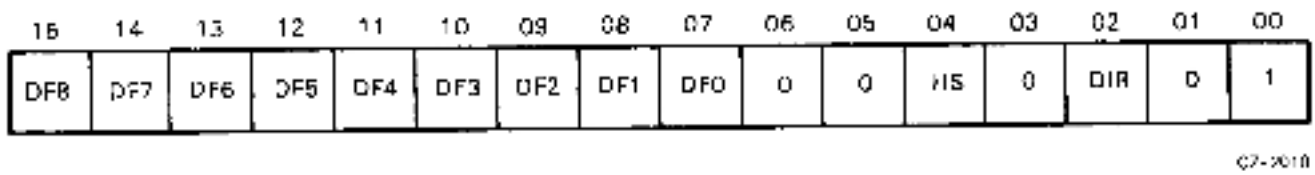
CONTROL STATUS REGISTER (CSR)



BUS ADDRESS REGISTER (BAR)



DAR DURING SEEK COMMAND



DAR DURING READING OR WRITING DATA COMMANDS

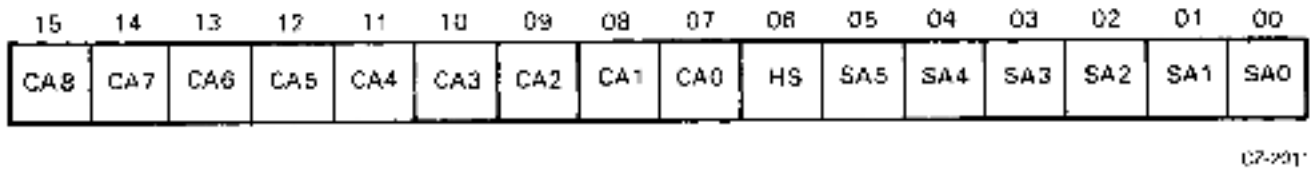


Figure 4-9 Register Summary (Sheet 1 of 2)

DAR DURING GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

CZ-2037

MPR AFTER GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WDE	CHE	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	CO	HO	BH	STC	STB	STA

CZ-2012

MPR AFTER READ HEADER COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ZEROES															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC															

CZ-2013

MPR DURING READ/WRITE COMMANDS FOR WORD COUNT

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	WC12	WC11	WC10	WC9	WC8	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

CZ-2036

Figure 4-9 Register Summary Sheet 2 of 2

4.3 CONTROLLER COMMANDS

The RL11 Controller can give one of seven commands to the drive, while the RLV11 can issue one of eight commands. Table 4-2 lists the commands. Each command is explained in the following paragraphs.

Table 4-2 RL11/RLV11 Controller Commands

Function Code	Command
0	No Op (RL11) or Maint. (RLV11)
1	Write Check
2	Get Status
3	Seek
4	Read Header
5	Write Data
6	Read Data
7	Read Data Without Header Check

4.3.1 No-Op (RL11) or Maintenance (RLV11) – Function Code 0

The RL11 performs no operation aside from clearing errors (except DE), setting CRDY and interrupting if IE is set.

The RLV11 maintenance command is used during a diskless diagnostic routine to detect controller malfunctions or to establish a level of confidence in controller operation. Prior to issuing the maintenance command, a buffer area in memory must be set aside for writing and reading of test patterns. The controller registers must be loaded by program with the following information.

- BAR with address of first memory buffer location
- WC register with a count of 511 (177001 octal)
- DAR with test word
- CSR with a function code 0, reset bit 7

When the RLV11 issues the maintenance command and clears the CRDY bit, the OPI timer is started. The microsequencer decodes the command and starts a maintenance routine. Two internal tests are performed and the DAR is incremented after each. Then, by enabling a DMA transfer to take place between memory and the controller FIFO, 256 words are transferred from the memory write test buffer into the FIFO. Once the FIFO is full, 255 words are transferred into the memory read test buffer previously prepared. The DAR is now incremented a third time. Throughout MAINT, checks are made and if an error occurs, the function stops with ERR set. The DAR is incremented as the test proceeds. This incrementing serves as a trace to determine the failing internal test.

Next, the test word +3 that was initially loaded into the DAR is channeled through the data source selector and into the CRC circuit. A CRC word is generated from this test word and sent through the data source selector again. This CRC of the test word then passes through the write precompensation circuit and the data separator circuit to eventually end up in the FIFO.

The contents of the DAR is then incremented and becomes test word +4. This new test word follows the same path as the preceeding test word and ends up as the second word in the FIFO. At this point, the FIFO holds:

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of test word +4

The contents of the DAR is now incremented once again and becomes test word +5.

Next, the second word in the FIFO (CRC of test word +4) is removed from the FIFO and serialized. It is sent through the data source selector, the CRC, and data source selector again, and so on. It follows the same data path as the two previous words and ends up back in the FIFO as the new second FIFO word. At this point, the FIFO holds:

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of CRC of test word −4

The contents of the DAR is then incremented for the sixth time to become test word +6. The controller ready bit is then set and the CPU receives an interrupt request. This completes the maintenance command operation.

As a result of this maintenance test, the following circuits are tested: the FIFO, the registers, the data source selector, the CRC circuit, the match circuit, the write precompensation circuit, the data separator circuit and the FIFO input and output serializer. Also, many of the microsequencer functions are exercised.

4.3.2 Write Check – Function Code 1

The write check command is used to verify that data was written on the disk correctly. It is used after writing a block of data onto the disk by the write command function. The write check command reads this same block of data from the disk and compares it with the contents of its source data buffer area in main memory. Because this comparison is performed in the controller, this source data must be transferred out of memory and into the controller silo.

Prior to issuing this command, the BA register must be loaded with the address of the first location of the data block in the main memory. The word counter register must be loaded with the data block length. The DA register is then loaded with the starting disk address location. At this point, the write check command can be loaded into the CS register.

Once a header match is found, and the header CRC validates the match, the 128 words of data are read from the disk. The disk data is then compared serially with the serial data coming out of the silo (SER DATA OUT). Either a compare error or a data CRC error will set bit 11 in the CS register.

4.3.3 Get Status – Function Code 2

The Get Status command causes the status word from a drive to be transferred to the controller where the software can access it through the MPR. The software should first verify that the controller is ready to perform an operation (the drive does not have to be ready). Then, the software should load the DAR with ones in bits 01 and 00, a reset bit at 03 and zeroes in the other locations. Next, the software should load the CSR with drive select bits, a negative GO bit, IE bit (if desired) and a code of 2 in the function bits. The controller will now command the selected drive to transfer its status word to the MPR in the controller. If the "reset" bit was set, the drive would reset its status register first.

4.3.4 Seek – Function Code 3

The Seek operation causes the positioner to move (either forward or reverse) some number of cylinders. The software should first verify that the drive is ready to accept a command, then load the DAR with the difference word (difference between the present position and desired position). This word contains the number of cylinders to move (bits 15 through 07), the head select bit (04) and the direction bit (bit 02, 1 = forward, 0 = reverse). Bits 06, 05 and 01 must be reset and bit 00 must be set. After the DAR is loaded, the software should load the CSR with the command word. This word should contain the drive select bits, the negative GO bit, IE bit if desired and a code of 3 in the function bits. The controller sends the Seek command to the selected drive, causing the drive to start its Seek operation. At this time, the controller goes ready and interrupts if IE is set. The controller is now ready to accept another command to perform another operation on another drive while the Seek is occurring.

If the difference word is large enough that the heads attempt to move past the innermost or outermost limits, the head will stop at the guard band and retract to the first even-numbered data track.

4.3.5 Read Header – Function Code 4

When a Read Header function is decoded, the controller will read the first header encountered on the selected drive and place the three header words in the silo. They pass through the silo and stop with the first word in the MP register. The software can then access the first word to determine the current sector, head, and cylinder address. When the software extracts the first word from the MP register, the second word automatically moves in to the MP register. If the software extracts the second word, the third word automatically moves in the MP. This is the CRC word. The software can now access it for checking purposes.

4.3.6 Write Data – Function Code 5

When this function is decoded with CRDY cleared, the controller starts reading successive header words and comparing them to the DA register. When a match is found, the header CRC is checked and, if correct, that sector is written with the words from memory designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. For partial sector writes, the remaining sector area is filled with zeros. At the end of the sector, the sector portion of the DA register is incremented. The next sector is written if all the words have not been written. At the end of the transfer, CRDY is set and an interrupt made if IE is set.

4.3.7 Read Data – Function Code 6

When this function is decoded, the controller begins reading successive header words and comparing them to the contents of the DA register. When a match is found, the header CRC is checked and, if correct, that sector is read and the words are placed in the memory location designated by the BA register. Both the BA and MP registers (word count in two's complement form) are incremented for each word transferred. This operation continues until the contents of the MP register is all zeros. Data CRC is checked and the DA register is incremented at the end of each sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

4.3.8 Read Data Without Header Check – Function Code 7

When this function is decoded, the data portion of the sector following the next sector pulse is read and the words requested are placed in the memory locations designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. The header is neither compared nor checked for CRC errors. Data CRC is checked at the end of a sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

NOTE

The DA register is not incremented during multisector transfer.

4.4 OPERATIONAL CONSIDERATIONS

4.4.1 Interrupt

The controller will request an interrupt if the IE bit and the CRDY bit are both set in the CS register. The IE bit is set or reset by the software and reset with the initialize condition. The CRDY bit is set by the hardware upon completion of a function or upon the setting of an error flag. It is also set by the initialize condition. It is reset by the software to cause the controller to start a function (negative GO bit). The interrupt vector address is 160. The normal priority level for the RL11 is BUS REQUEST 5. The RLV11 Controller uses the one priority level provided by the LSI-11 processor.

4.4.2 Seek Operation

The following sequence is an example of performing a seek function.

1. Issue read header function to drive and wait for interrupt or wait for CRDY.
2. Check error flag.
3. Read the header word from the MP register.
4. Calculate difference and direction for the seek.
5. Move difference word to the DA register.
6. Issue seek function to drive and wait for seek to be completed as indicated by drive ready bit.
7. Check error flag.

A software system that optimizes positional latency (see Paragraph 1.4) would keep current cylinder and head select information in core so that Steps 1, 2 and 3 would be unnecessary. Also, note that reading the header gives rotational position as well, so that some rotational optimization is possible.

4.4.3 Overlapped Seeks

Since the controller comes ready and interrupts as soon as a seek is issued, it is possible to issue seeks to additional drives while the first is seeking. However, no interrupt occurs when the seeks are completed, so the transfer command should be issued to the drive requiring the shortest seek as soon as all seeks are issued. In this way, the drive completing its seek first will immediately perform its transfer and interrupt when done.

4.4.4 Data Transfer

Data transfer is via DMA facility. Sixteen words of FIFO (silo) buffering are provided for data by the RL11. The RLV11 provides 256 words of FIFO (RAM) buffering and will not start transferring a sector unless the FIFO has enough space to hold the entire sector.

To do a data transfer, the software should perform the following steps:

- Load BA register with address of first memory location to be transferred
- Load DA register with address of first disk location to be transferred
- Load WC register with two's complement of number of words to be transferred
- Issue read data or write data and wait for interrupt or test for ready
- Check error flag.

Other drives could do seeks or data transfers between the issuing of seek and the issuing of the data transfers.

4.4.5 Recovery of Data with Bad Headers

Function 7, read data without header check, is provided to allow the recovery of data should headers become unreadable. If constant HNF or HCRC errors are encountered on a particular sector so that the data is not recoverable by the standard read command, proceed as follows. Perform successive read header commands until the sector preceding the bad sector is found. Then, within 340 microseconds issue a read data without header check. The data portion of the next sector will be read without either header compare or header CRC check. Data CRC errors will be reported.

4.4.6 Non-interchangeability of RL01K/RL02K Disk Cartridges

These two types of cartridges are not functionally interchangeable but a cartridge will physically fit into the "wrong" type of drive. If a cartridge is loaded into the wrong drive, no damage will occur to the drive, media, or data but the software will not run normally. If such symptoms are exhibited, the operator should check for the proper cartridge type.

4.5 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them can be considered recoverable in the sense that if the operation is retried it is possible that the error will not occur and successful use of the subsystem can continue. Some of the errors are considered fatal because retries could damage the data, media, or equipment. The errors are listed with the recommended reaction in Table 4-3.

The nature of these errors should be considered when determining how many times to retry the operation before declaring that retrying has reached a practical limit. For instance, a DLT error could be caused by a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability for a short duration. In this latter case, it is likely that the operation would be successful on the first retry. The rate of occurrences is a good indicator of overall system performance and an error logging routine should count that. A general increase in the rate of DLT errors could indicate hardware system failures or it could indicate that the usage of the system is approaching its throughput capacity in its present configuration.

Another example of applying practical reaction to an error is the handling of a HNF error. It should be retried once and if it occurs then possibly the head is not positioned over the correct track. If a read header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If not, then possibly there is a bad spot on the media and another area should be tried. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the original sector.

As an additional example, consider an NXM error. It indicates that a memory unit is not responding to a DMA request for data transfer to/from that memory unit. It is unlikely that the media or disk unit is failing and only slightly more likely that the controller is failing (hardware problem). It is possible that the program is trying to access a non-existant memory unit (software problem). A retry may be worthwhile for one time but more than likely it will occur. The most important piece of information needed for diagnosis is the contents of the BA register.

Each of the errors should be given the same type of practical thought when programming error recovery routines. Whenever an error occurs, the program should log it along with the symptoms such as the contents of the registers, the status of the unit, and whether or not a retry was successful. The more complete the error log, the more quickly and accurately the cause can be diagnosed.

Table 4-3 Errors

CONTROLLER ERROR	BIT IN C.S.	RECOMMENDED REACTION
OPI	10	Retry some practical number of times.
DCRC/HCRC/WCE	11	Retry some practical number of times. Be sure to record contents of the DA register.
DLT/HNF	12	Retry. If HNF, perform a read header, and verify cylinder.
NXM	13	Retry once. Be sure to record the contents of the BA register.
DRIVE ERROR	14	Perform a Get Status and check bits listed below.

Table 4-3 Errors (Cont)

DRIVE ERROR	BIT IN STATUS WORD	RECOMMENDED REACTION
DSE	8	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	10	Retry.
SPE	11	Retry.
SKTO	12	Retry. Wait for 1.5 sec after Reset.
CHE	14	Fatal. Do not retry.
WDE	15	Fatal. Do not retry.

4.6 DIFFERENCE SUMMARY (RK05 and RL01/RL02)

This section may be helpful to users who have formerly used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming an RK05 subsystem and programming an RL01/RL02 subsystem.

In general, the RK05 subsystem had a lot of its functionality built into the hardware while the RL01/RL02 subsystem requires that the software provide some of the functionality. The major differences are explained below.

4.6.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end of track condition and the hardware will cause a mid transfer seek to the next track and then restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface of the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DAR advances to 50 (octal) which is illegal and the OPI error flag is set. It is necessary for the software to 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation or 2) to detect that it has occurred. The software must initiate a separate seek function and as well as a continuance of the read/write function. Note that a head switch from upper to lower surface without a positioner movement to the next cylinder is considered a seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

4.6.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit seek is a software-directed seek operation. An implicit seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired cylinder address or head address does not coincide with the present position. The RL01/RL02 subsystem hardware does not have this capability. The software must ensure that the positioner is over the desired cylinder and the desired head is selected before starting a read/write operation.

4.6.3 Recalibrate

The RK05 subsystem has a return to zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder zero must be performed. If the current cylinder address is not known and the drive is commanded to seek beyond the outer guard band, this guard band will be detected and the head will retreat to cylinder zero.

4.6.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 Disk Cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

4.6.5 Reformatting

The RK05 cartridge can be reformatted in the field while the RL01/RL02K cartridges cannot. The imbedded servo information and Bad Sector File greatly reduce the need to reformat the cartridge in the field.

4.6.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.

CHAPTER 5
RL8-A PROGRAMMING INFORMATION

5.1 GENERAL DESCRIPTION

The RL8-A Controller consists of a single hex-height M8433 module. It interfaces the PDP-8 OMNIBUS with the RL01/RL02 Disk Drive bus and contains the control, monitor, and data handling logic for disk operation. The RL8-A can handle up to four drives via a daisy-chained I/O cable. A PDP-8 can handle two RL8-A Controllers, providing control for up to eight drives.

The RL8-A has six addressable registers that are detailed in Section 5.2. The PDP-8 computer communicates with the controller by accessing these registers using Input Output Transfer (IOT) instructions which have a format of 6XXX. The device codes X60X and X61X are assigned to the first controller. If there is a second controller it uses device codes X62X and X63X. The specific instructions that cause a response in a controller are shown in Table 5-1. The instructions are used to monitor and control the controller and are not used to transfer data. Data is transferred using Direct Memory Access (DMA) operation via data break cycles on the OMNIBUS. The result is an exchange of data between the controller and memory directly, one 12 bit word at a time. The controller has a silo which can buffer up to 16 words. The controller can transfer 12-bit words to the disk as 12 bit words or can transform them into 8-bit bytes by dropping the high order four bits in each word. The controller can transfer data coming from the disk onto the OMNIBUS as 12 bit words or it can group the data as 8 bit bytes and fill in the remaining four bits as zeros. The advantages and disadvantages of both the 8 bit and 12-bit mode are covered in Paragraph 5.4.

Table 5-1 RL8-A Instruction Set

OCTAL CODE *	MNEMONIC	FUNCTION
6600	RLDC	Clear controller, all registers, AC and flags. (Do not use to terminate a disk function.)
6601	RLSD	Skip on function done. Then clear if set to a one.
6602	RLMA	Load break MA register from AC 0:11
6603	RLCA	Load command register A from AC 0:11
6604	RLCB	Load command register B from AC 0:11, execute command
6605	RLSA	Load sector address register from AC 0:5
6607	RLWC	Load word count register from AC 0:11
6610	RRER	Read error register into AC 0, 1, 2, 10, 11

5.2.2 Command Register B

Command Register B is a 12 bit register that contains the mode, drive number, extended memory address bits, interrupt enable, and the function code. The RLCB command (6614) is used to load the register and the RRCB command (6613) reads the register. The RLCB command also executes the function (Figure 5-3).

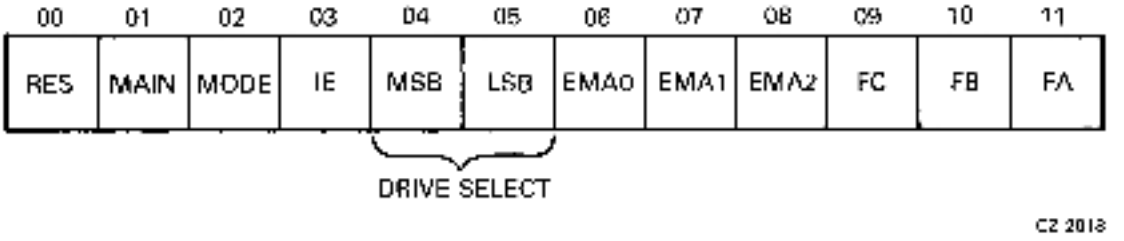


Figure 5-3 Command Register B

Bit	Name	Function
AC0	-	Reserved
AC1	Maintenance	The contents of the Disk Address (DA) register are looped back to the silo for maintenance purposes. Bit 2 of command register B must also be set for this function to work correctly. See Paragraph 5.3.9.
AC2	Mode	When set, this bit indicates that the data field will be 256 8-bit words per sector. When zero, the data field will be truncated to 170 12 bit words per sector. This bit must be set when a Maintenance, a Get Status or a Read Header command is to be executed.
AC3	Interrupt Enable (IE)	When this bit is set, the controller is allowed to interrupt the processor at the conclusion of a normal command or error termination.
AC4:5	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.
AC6:8	Extended Memory Addressed (EMA)	These three bits define the memory field location. This allows up to 32K memory locations to be addressed on processors having more than 4K of memory.
AC9:11	Function Code	These bits indicate the command to be executed by the controller/disk subsystem.

Bit 9	Bit 10	Bit 11	Command
0	0	0	Maintenance
0	0	1	Reset
0	1	0	Get Status
0	1	1	Seek
1	0	0	Read Header
1	0	1	Write Data
1	1	0	Read Data
1	1	1	Read Data Without Header Check

5.2.3 Break Memory Address Register

The Break Memory Address (BRK MA) register is a 12-bit register that points to a memory location. It is loaded by the RLMA command (6602). The contents of the BRK MA register are automatically incremented as each word is transferred between memory and controller.

The register is cleared by initializing the controller or by loading the register with zeros (Figure 5-4).

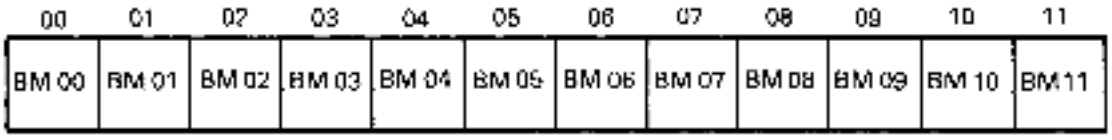


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Figure 5 – Break Memory Address Register

5.2.4 Word Count Register

The Word Count (WC) register is a 12-bit register loaded by the RLWC command (6607) and read by the RRWC command (6611). Before reading or writing data, the word counter is loaded with the two's complement of the number of words to be transferred. As each Direct Memory Address (DMA) transfer takes place, the word counter is incremented and terminates the command on overflow. It can count from 1 to 4096 data words. This corresponds to 24 sectors while in 12 bit word mode. In the 8-bit byte mode the transfer is limited to one sector (170 bytes) (Figure 5-5).

WC Register Programming Note – this disk drive will not do spiral Read/Writes. The program must break up a data transfer if track-to-track Read/Writes are to be done. Between two such data transfers, a seek to the next track or surface must be made.

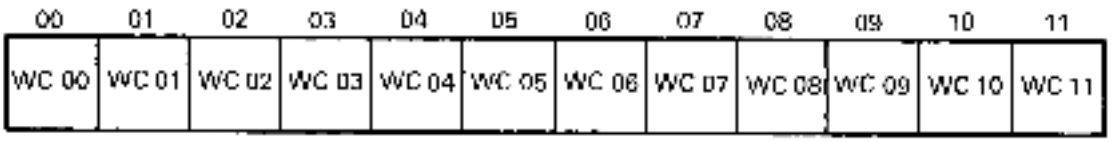

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Figure 5-5 Word Count Register

5.2.5 Sector Address Register

The Sector Address (SA) register is a 6-bit register loaded by an RLSA command (6605) and read by an RRSA command (6614). Before executing a Read or Write operation, the sector address is loaded into the SA register (Figure 5-6).

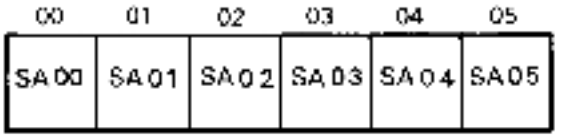

Figure 5-6 Sector Address Register

5.2.6 Error Register

The Error register is a 5-bit register that is read by the RRER command (6610). Bits 0:2 are cleared by initialize or when Command Register B is loaded (Figure 5-7).

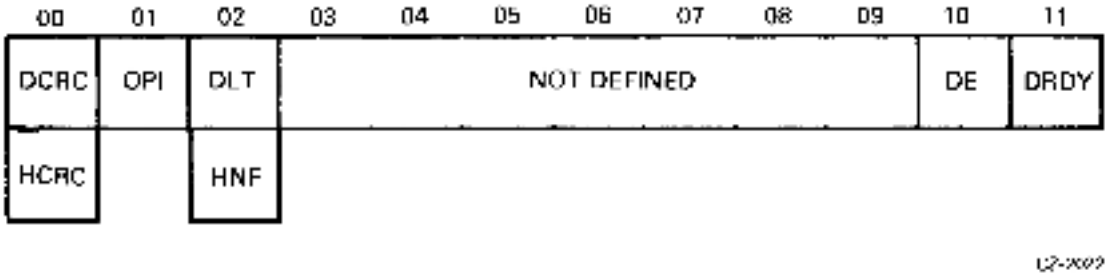

Figure 5-7 Error Register

Bit	Name	Function
AC0	Data CRC (DRCR) or Header CRC (HCRC)	If OPI is cleared and this bit is set, the CRC error occurred in the data (DCRC). If OPI is set and this bit is also set, the CRC error occurred on the header (HCRC).
AC1	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed within 200 ms. It is also used in conjunction with bits 0 and 2 of this register.
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set. This bit is set during a read if the silo is full and the word count is not yet zero (meaning that the word being read could not enter the silo). OPI will not be set. When this bit and OPI are both set, then a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare – HNF).

Bit	Name	Function
AC0:2	Error Code	Summary

Error	Bits 00	01	02
DLT	0	0	1
OPI	0	1	0
HNF	0	1	1
DCRC	1	0	0
HCRC	1	1	0

AC10	Drive Error (DE)	This bit is tied directly to the Drive Error interface line. When set, it indicates that the selected drive has flagged an error. The source of the error can be determined by a Get Status. The DE bit is cleared with a Reset command to the drive.
AC11	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a Seek operation is initiated and set again when the Seek operation is completed.

5.2.7 Silo Data Buffer

The RRSI command (6615) is used to transfer the contents of the silo data buffer to the AC. The silo does the following:

- Stores the result of the Get Status command from the drive (drive errors and status bits)
- Stores the header words when a Read Header command is executed
- Stores the result of a Maintenance command
- Stores the contents of the DA register if the maintenance bit was set in Command Register B

5.2.7.1 Silo Register After a Get Status Command – When a Get Status command is executed and a status word is returned to the controller, the contents of the silo register appear as shown in Figures 5-8 and 5-9.

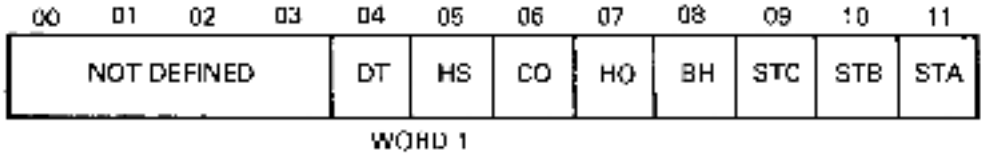

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Figure 5-8 Silo Buffer for Status Word 1

WORD 1

Bit	Name	Function
AC0:3	-	Undefined
AC4	Drive Type	A zero indicates an RL01; a one, an RL02.
AC5	Head Select (HS)	Indicates currently selected head. A zero indicates the upper head; a one, the lower head.
AC6	Cover Open (CO)	Set when the drive access cover is open or the dust cover is not in place.
AC7	Heads Out (HO)	A one indicates that the heads are over the disk; a zero indicates that the heads are home.
AC8	Brush Home (BH)	Set when the brushes are home.
AC9:11	State Bits	These bits define the state of the disk drive.

State Bit Definitions

Bit C	Bit B	Bit A	Definition
0	0	0	Load State
0	0	1	Spin-up
0	1	0	Brush Cycle
0	1	1	Load Heads
1	0	0	Seek (Track Counting)
1	0	1	Lock on (keeping on track)
1	1	0	Unload Heads
1	1	1	Spin-down

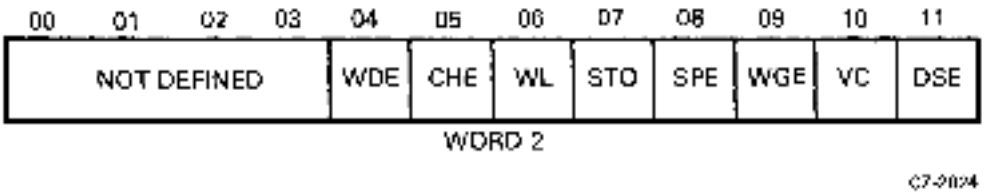


Figure 5-9 SDI Buffer for Status Word 2

WORD 2

Bit(s)	Name	Function
AC0:3	-	Undefined
AC4	Write Data Error (WDE)	This bit is set when the write gate is on but no transitions were detected on the write data line.

Bit(s)	Name	Function
AC5	Current Head Error (CHE)	This bit is set when write current is detected in the heads but the write gate was not asserted.
AC6	Write Lock (WL)	Set when the drive is write protected.
AC7	Seek Time Out Error (SKTO)	Set when the heads did not come on track in the required time during a seek operation, or when the heads drifted off track and did not return within 1.5 seconds.
AC8	Spin Error (SPE)	Set when the spindle does not come up to speed within 40 seconds or when the spindle speed is too high.
AC9	Write Gate Error (WGE)	Set if write gate is asserted and one or more of the following conditions is true. 1. Drive is not "Ready to Read/Write" 2. Drive is write protected 3. Drive is in the midst of sector time 4. Drive has another error asserted
AC10	Volume Check (VC)	Set when a new cartridge has been loaded or when the power has been cycled down, then up. This bit is reset by a Reset command
AC11	Drive Select Error (DSE)	Set when one or more drives have the same number (unit select plug) or have responded to the same number.

5.2.7.2 Silo Data Buffer During a Read Header Command – When a Read Header command is executed, six 8-bit bytes are stored in the silo as six 12-bit words. The first two header words contain sector address, head select, and cylinder address information. The second two words contain all zeros. The last two words contain the header CRC information. All six words are readable by the RRSI command (0615) (Figure 5-10).

5.2.8 Register Summary

Figure 5-11 is a bit and function summary of the addressable registers.

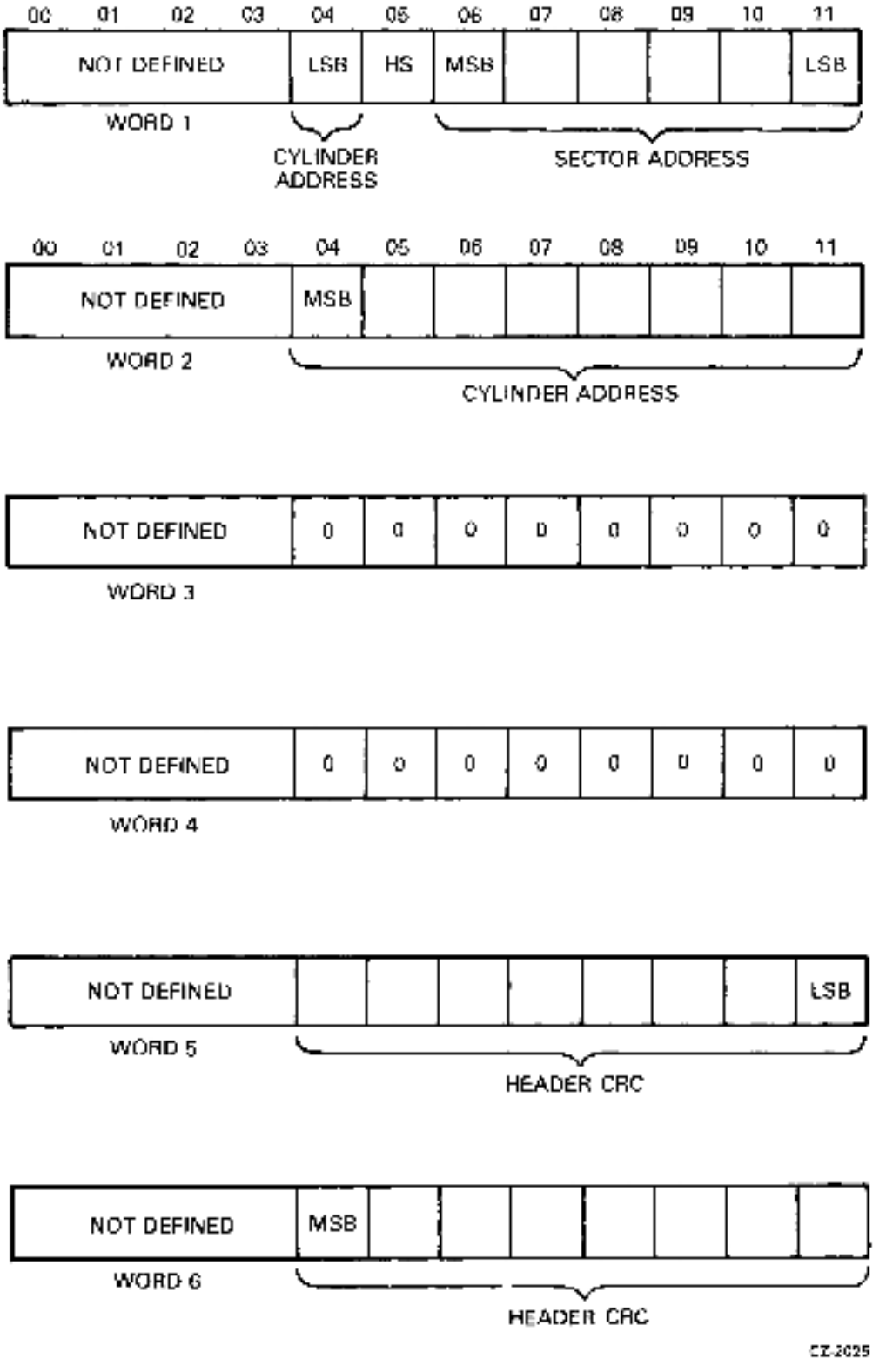
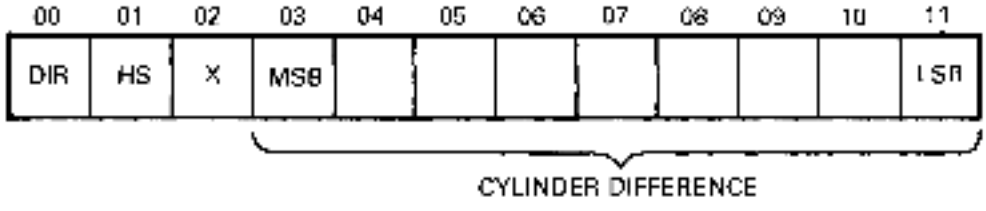


Figure 5-10 Silo Buffer for Header Words



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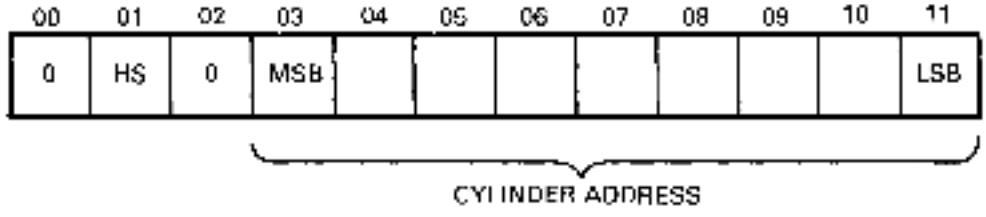
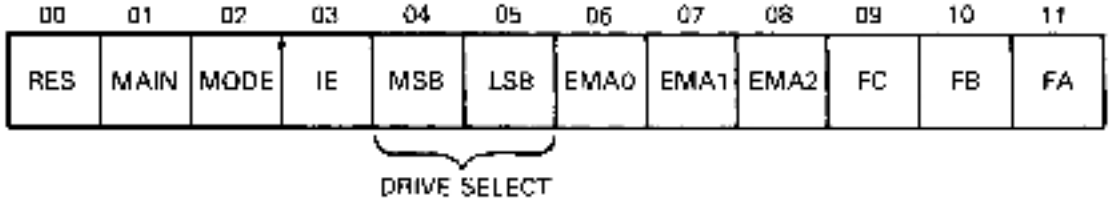
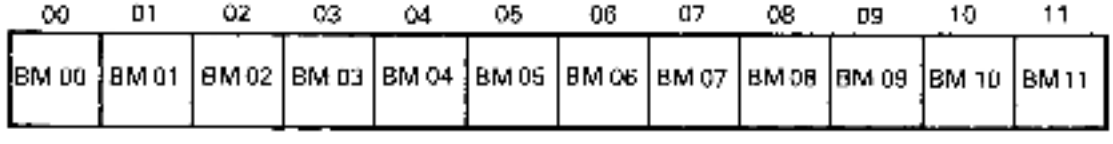


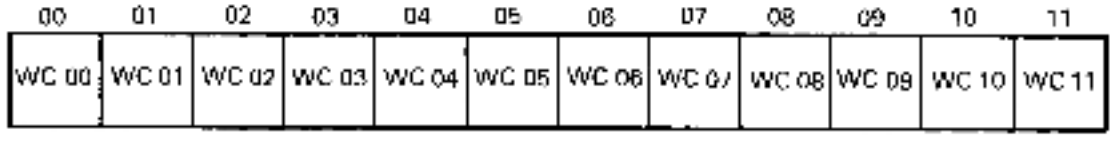
CZ-2017



CZ-2018

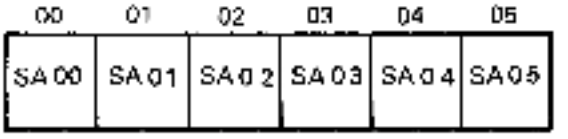


CZ-2019

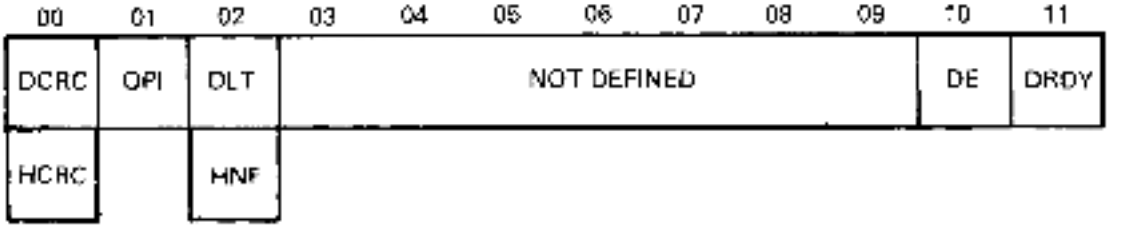


CZ-2020

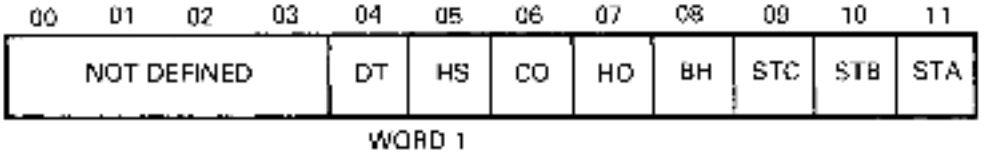
Figure 5-11 Register Summary
(Sheet 1 of 3)



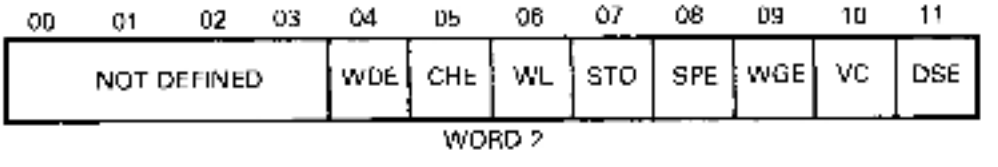
CZ-2021



CZ-2022



CZ-2023



CZ-2024

Figure 5-11 Register Summary (Cont)
(Sheet 2 of 3)

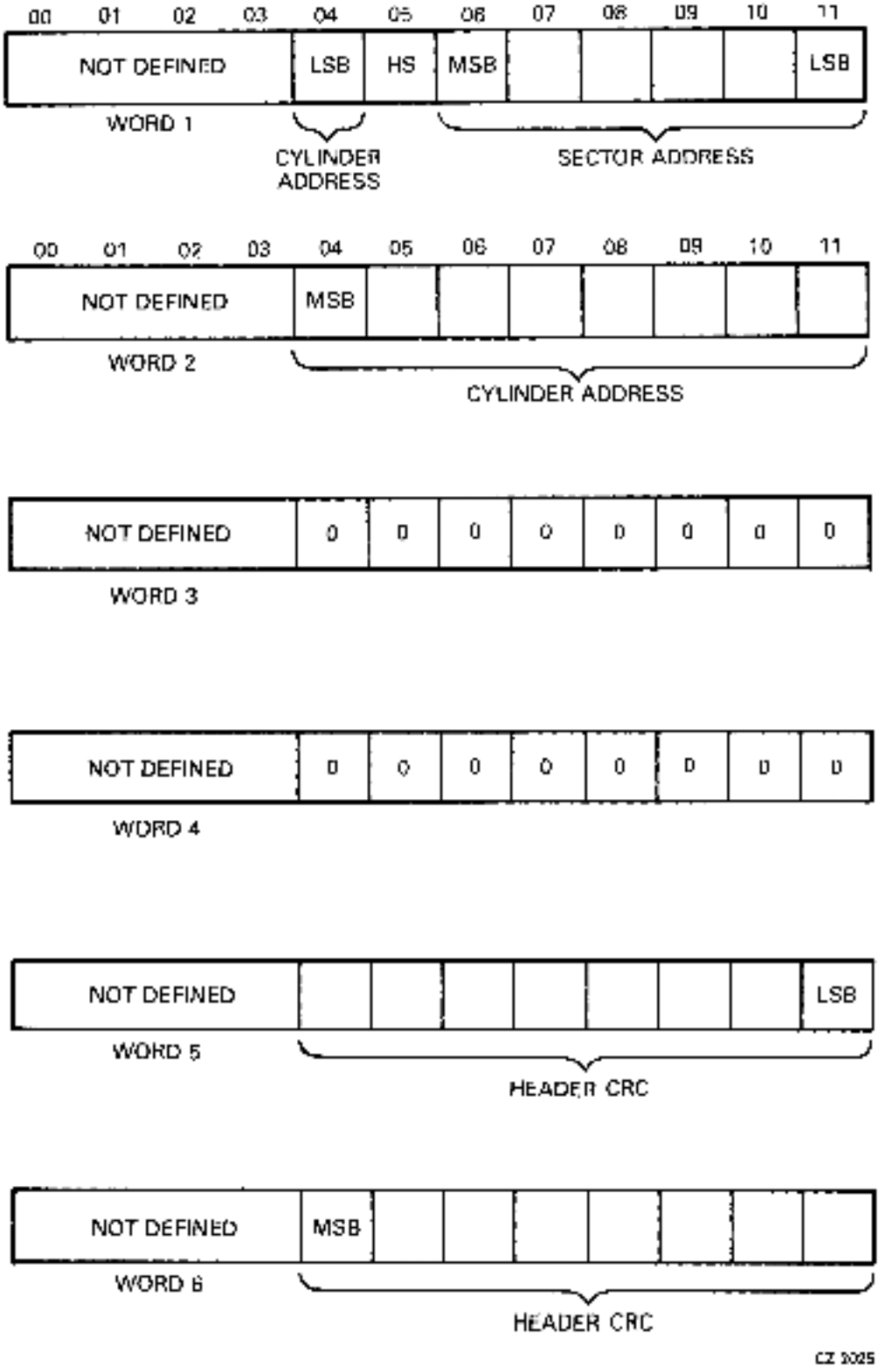


Figure 5-1 Register Summary (Cont)
(Sheet 2 of 3)

5.3 CONTROLLER COMMANDS

The RL8 A Controller is capable of performing eight operations by responding to the function code in the low order three bits of Command Register B. In many cases it is necessary to load other registers prior to loading the function code into Command Register B. No registers should be loaded unless the controller is ready. This condition can be checked by using an appropriate IOT instruction that checks the function done status or by using the interrupt mode.

5.3.1 Maintenance Command

This command tests the controller by causing it to perform the following tasks.

- The controller requests a data word from memory via the OMNIBUS using the Break Memory Address (BRK MA) register as an address. When the controller receives this word, the BRK MA and the Word Count (WC) register are both incremented.

- The data word is bubbled through the silo, serialized and transferred (in 8-bit mode) through the CRC-generating logic where two more 8-bit bytes are appended. This 24-bit data stream goes through the write data precompensation logic and then is looped back and brought in as if it were read data from the drive. The data passes through the phase-locked loop and data separator logic and into the silo where it is converted back to parallel, eight bits per word, and bubbles up through the silo to be available to the OMNIBUS.

- The controller requests three memory accesses and transfers the three words back to memory using the BRK MA register as a pointer. The BRK MA register and WC register are incremented for each transfer. The words are now available for the program to check for diagnostic purposes.

- The above processes repeat and the cycle continues until the WC register equals zero.

Prior to starting this command it is necessary to set up some registers as shown below.

- The BRK MA register should be loaded with the address of the first word of data to be transferred to the controller. The next three words of memory will receive three words of data from the controller.

- The WC register should be loaded with the desired count (in two's complement form). A complete cycle takes four counts.

- The Command Register B should be loaded with 10X0 or 14X0. This sets the mode bit to indicate 8-bit mode. The maintenance bit is a zero. The function code is 000. The remaining bits are irrelevant.

5.3.2 Reset Command

This command is used to reset all of the error bits in the selected drive unit. It does not reset any conditions in the controller nor does it cause any head movement in the drive. Prior to executing this command, the Sector Address Register and Command Register A must be cleared by using appropriate IOT instructions.

5.3.3 Get Status Command

The Get Status command reads the 16-bit status word from the selected drive and transfers it into two 8 bit bytes in two consecutive words in the silo. The computer can then extract them with two IOT RRSI instructions. The format of the bits are shown in Paragraph 5.2.7.1 Prior to performing a Get Status command it is necessary to clear out the Sector Address Register and Command Register A. When Command Register B is loaded with the function code the appropriate drive select bits should be set, the interrupt enable bit should be set if desired, and the mode bit must be set for 8-bit mode. The controller should be ready before performing any of these load register operations but the drive does not have to be ready.

5.3.4 Seek Command

The Seek command is used to move the heads (on the selected drive) or to select the other head. Prior to executing the seek command the Sector Address Register should be cleared and Command Register A should be loaded with a direction bit, a head select bit, and cylinder difference word. Command Register B is then loaded with the drive select bits and the seek function code. The controller will send a command to the selected drive to cause it to start a seek operation. The controller will become ready and can then perform another command even though the drive is still seeking.

If the drive attempts to move the head past the innermost or outermost tracks, the head will retract from the guard band and stop at the first even numbered track it encounters.

5.3.5 Read Header Command

The Read Header command will read the first header encountered on the selected drive and load the header into six consecutive word locations in the silo, one 8-bit byte per word. The computer can then extract this information with IOTRRSI instructions. The format of the information is shown in Paragraph 5.2.7.2. A check is performed on the header that is read.

5.3.6 Write Data Command

The Write Data command requests data from memory, one word at a time, via the Omnibus using the DMA mode. It then transfers the data through the controller silo buffer to the selected drive. The data is written at the specified sector data area. This operation continues, incrementing both the Break Memory Address register and the Word Count register once for each Omnibus transfer, until the Word Count register reaches zero.

Prior to starting this command it is necessary to position the head over the desired track using a Seek command. Then the registers should be loaded as follows.

- Load the Break Memory Address register with the address of the first memory word to be transferred.
- Load the Sector Address register with the address of the first sector to be written.
- Load the Word Counter register with the two's complement of the number of words to be transferred.
- Load the Command Register A with the head select bit and the cylinder address word.
- Load the Command Register B with a mode bit (8-bit or 12-bit mode), interrupt enable bit (optional), drive select bits, extended memory address bits, and the Write Data function code.

The Write Data command will then read headers and perform header checks until the desired header is located. After the header is checked, the data is transferred. The header check includes a header CRC check. There is no implicit seek performed so if the selected head is not positioned over the desired track, the desired header will not be found and an OPI error will occur. If only a partial sector is written, the remainder of the sector is written with all zeros. A CRC word (16 bits) is generated and written for each sector automatically. Since the word count is limited to 4096 this means that the maximum amount of data that can be written with one Write Data command is 10 sectors in 8-bit mode. If 12 bit mode is used, a maximum of 170 words (one sector) can be transferred. The hardware will not perform a spiral (mid-transfer) seek. Therefore, if data must be written that would overflow to the next track, it is necessary to write the data to the end of the track, seek to the next track and then continue to write the remainder of the data.

5.3.7 Read Data Command

The Read Data Command will cause the controller to read data from the selected drive. It will read from the track that is currently under the selected head, starting at the specified sector. The data is transferred through the controller silo buffer. The controller requests DMA transfers to memory via the Omnibus. The Break Memory Address register is incremented once for each 12-bit word transferred over the Omnibus and the Word Count register is counted up. When the Word Count register reaches zero the Read Data command is terminated. Prior to starting the Read Data command, the head should be positioned over the desired track with a Seek command. Load the registers as follows.

- Load the Break Memory Address register with the address of the first location in memory to which the data is to be transferred.
- Load the Sector Address register with the address of the first sector from which the data is to be read.
- Load the Word Counter register with the two's complement of the number of words of data to be read.
- Load the Command Register A with a head select bit and a cylinder address word.
- Load the Command Register B with a mode bit and interrupt enable bit (optional) drive select bits, extended memory address bits, and the function code for Read Data.

The Read Data command then reads headers, comparing them to the desired disk address. The data transfer begins when the desired header is found. The header checks include header CRC checks. There is no implicit seek so if the selected head is not over the desired track, the desired header will not be found and an OPI error will occur.

The RL8-A cannot perform a spiral (mid-transfer) seek. If a block of data to be read passes the end of a track and continues on the other surface or on the next cylinder, it is necessary to program a Read Data just to the end of the track. The drive must then Seek to the next track and then continue reading data.

A CRC check is performed on each sector during a Read Data operation.

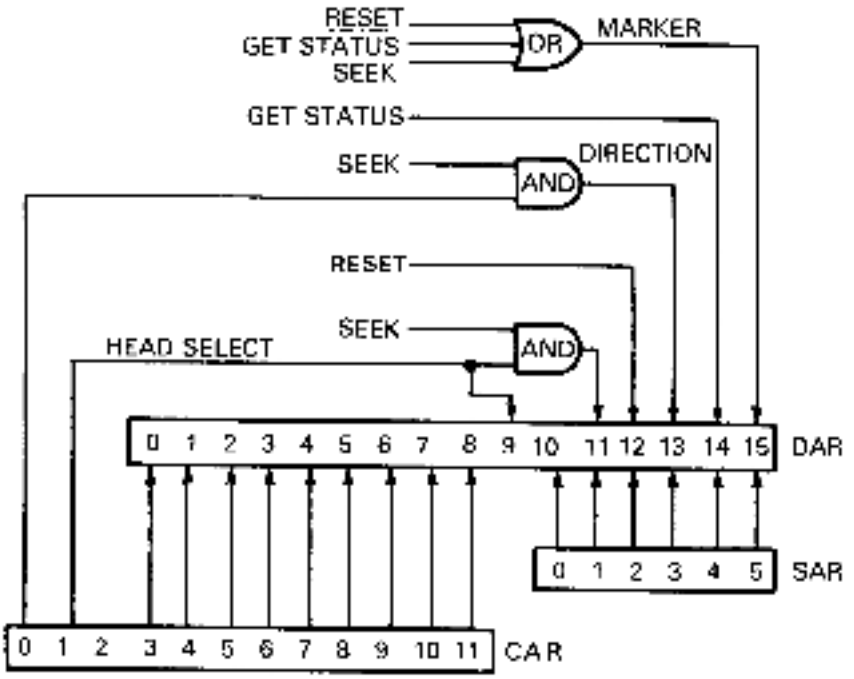
5.3.8 Read Data Without Header Check Command

This command is the same as a Read Data command except that no header check is performed. The next header read is considered a match so that sector is the first sector read. Since no header check takes place, the header CRC is not performed.

5.3.9 Maintenance Bit

The maintenance bit in Command Register B enables a path for the serial information leaving the DA register. When this bit is set, the data that is going out to the drive is looped back and shifted into the silo. The data bubbles through the silo and becomes accessible (as two 8-bit bytes) to IOT RRSI instructions. The program can then monitor the operation of the DA register, which is not a directly addressable register. This feature must be used only with Reset, Get Status, and Seek commands. Because the DA register is a 16-bit register, the 8-bit mode bit should be set. This insures that the contents of the DA register fit into two 8-bit bytes. The contents of the DA register and the two silo words are illustrated in Figure 5-12. During the loading of DA register (which occurs on every command) there is more than one input to some of the bit positions. These inputs are ORed together. Normally, the Sector Address Register is cleared before any Reset, Get Status, or Seek command and Control Register A is cleared before any Reset or Get Status command. It is possible to test all the bits in the DA register by using selected patterns in Control Register A and the Sector Address Register.

LOADING OF DAR



TRANSFER OF DAR TO SILO

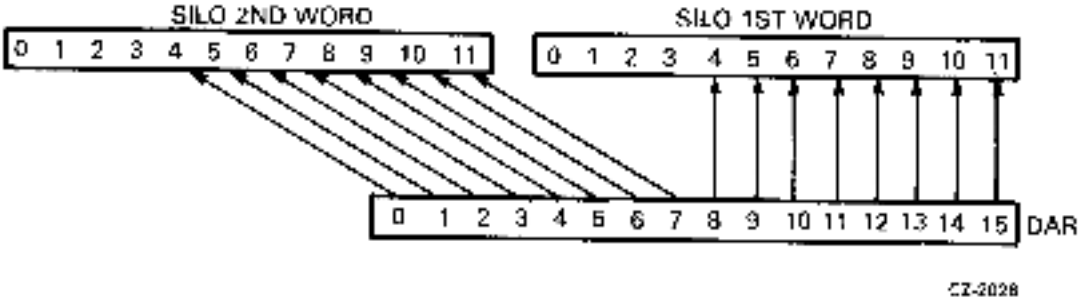


Figure 5-12 Maintenance Mode Bit

5.4 OPERATIONAL CONSIDERATIONS

5.4.1 8-Bit Mode Versus 12-Bit Mode

The disk cartridge is formatted in 8 bit bytes. For instance, the header contains a 16-bit word address, another 16 bit word, then a 16-bit header. The data area is 256 8 bit bytes and the data area CRC is 16 bits. None of these areas are evenly divisible by 12, which is the PDP 8 word length. Therefore, the RL8-A Controller has the capability of operating in either 8-bit mode or 12-bit mode.

When reading in 8-bit mode, the serial data from the disk is broken into 8-bit bytes and put into the silo with eight bits per word. Since the silo is 12 bits wide, the data goes into the eight low order bit positions and zeros are put into the remaining four high order bit positions. That is the format used when the computer transfers a 12-bit word from the silo to the CPU accumulator or to memory. The 8-bit mode is necessary when performing a Read Header, Get Status, or Maintenance command where 16 bits of data are read. Otherwise, information would be lost.

The 8 bit mode can be used for data on the disk, In such a case, 256 8 bit bytes are read from each sector and transferred to memory as 8-bit words. In some cases, this may be an advantage. For example, if 8-bit ASCII data is being handled the 8 bit mode is preferable to 12 bit mode. In most cases, however, the 8 bit mode wastes 33% of the memory space. Because the 12 bit mode uses 12 bit words it uses less memory. In the 12-bit mode each sector contains 170 words with only 8 wasted bits at the end of each sector.

In the 12-bit mode, the RL8-A Controller hardware blocks data into 170 words per sector. The operating system for the PDP-8 uses only 128 words per sector, so that while memory is used more efficiently, some disk space is wasted.

5.4.2 Interrupt

The RL8-A will interrupt the processor if the Interrupt Enable bit is set and the controller is done. If an error occurs during an operation the done condition is set.

5.4.3 Seek Operation

If the program does not keep track of the current position of the head (cylinder and surface), and it is desired to read or write from a particular area from the disk, it is necessary to:

- Read Header to obtain the current position of the head
- Calculate the difference (if any) from the desired position
- Issue a Seek with the proper difference, direction and head select information.

5.4.4 Overlapped Seeks

Since a Seek operation does not involve data transfer, it is possible to have one drive seeking while another is transferring data. Only one drive at a time can transfer data but up to four drives can be seeking simultaneously.

5.4.5 Recovery of Data with Bad Headers

Function 7, Read Data Without Header Check, allows the recovery of data with unreadable headers. If HNF or HCRC errors are repeatedly encountered on a particular sector, and the data is not recoverable by the standard read command, proceed as follows. Read successive headers until the sector preceding the bad sector is found. Then, within 300 microseconds, issue a Read Data Without Header Check. The data portion of the next sector will be read without either header compare or header CRC check. Data CRC errors will be reported.

5.4.6 Non-interchangeability of Disk Cartridges

5.4.6.1 RL01K/RL02K – These two types of cartridges are physically interchangeable but not functionally interchangeable. If a cartridge is installed on the incorrect type of drive, no physical damage will take place and data will not be destroyed. However, the unit will not operate in a normal manner. The symptoms exhibited depend upon the program running at the time. If the system is exhibiting abnormal characteristics the operator should ensure each drive contains the correct type of cartridge.

5.4.6.2 RL8-A/RL11/RLV11 – RL01K cartridges are interchangeable with other RL01K cartridges assuming that the RL8-A has written the cartridges in 8-bit mode. RL02K cartridges are interchangeable with other RL02K cartridges under the same condition.

5.4.7 Use of Two RL8-A Controllers

A PDP 8 system can be configured with two RL8-A Controllers to increase the capacity of the system up to eight drives. However, if both controllers are trying to perform data transfers at the same time, the throughput capacity of the Omnibus may be exceeded. In this case, conflicts (DLT's) will occur.

5.5 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them are considered recoverable. In this case, if the operation is retried it is possible that the error will not recur and use of the subsystem can continue. Some of the errors are considered fatal, however, because retries may cause damage to the data, media, or equipment. The errors are listed with the recommend reaction in Table 5-3.

Table 5-3 Errors

Controller Errors	Recommended Reaction
OPI	Retry some practical number of times.
DCRC/HCRC	Retry. Be sure to record the contents of the DA register.
DLT/HNF	Retry. If an NHF error, perform a Read Header and verify cylinder.
Drive Error	Perform a Get Status and check the bits listed below.
Drive Errors	**Recommended Reaction**
DSE	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	Retry.
SPE	Retry.
SKTO	Retry. Wait for 1.5 sec after Reset.
CHE	Fatal. Do not retry.
WDE	Fatal. Do not retry.

The nature of these errors should be considered when determining how many times to retry the operation. For instance, a DLT error could be a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability. In the latter case, it is likely that the operation would be successful on the first retry. The rate of occurrences is a good indicator of overall system performance and an error logging routine should count the rate at which errors occur. A general increase in the rate of DLT errors could indicate that system usage is approaching its throughput capacity in its present configuration.

Another example of applying practical reaction to an error is the handling of an HNF error. It should be retried once. If it recurs, then the head may not be positioned over the correct track. If a Read Header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If not, then possibly there is a bad spot on the media. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the original sector.

Whenever an error occurs, the program should log it along with the contents of the registers, the status of the unit, and whether or not a retry was successful. The more complete the error log, the easier it is to diagnose the cause of errors.

5.6 DIFFERENCE SUMMARY (RK05 AND RL01/RL02)

This section may be helpful to users who have used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming the RK05 subsystem and programming the RL01/RL02 subsystem.

In general, the RK05 subsystem provides more hardware support of functions while the RL01/RL02 subsystem requires that the software provide some of the functionality. The major differences are explained below.

5.6.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end of track condition. The hardware will cause a mid-transfer seek to the next track and then restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface on the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DA register advances to 50 (octal) which is illegal and therefore sets the OPI error flag. It is necessary for the software to 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation or 2) to detect that it has occurred. The software must initiate a separate seek function and initiate a continuance of the read/write function. A head switch from the upper to the lower surface without a positioner movement is considered a seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

5.6.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit seek is a software directed seek operation. An implicit seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired position is different from the present position. The RL01/RL02 subsystem cannot do an implicit seek. The software must ensure that the positioner is over the desired cylinder and that the desired head is selected before starting a read/write operation.

5.6.3 Recalibrate

The RK05 subsystem has a return to zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder zero must be performed. If the current cylinder address is not known and the drive is commanded to seek beyond the outer guard band, this guard band will be detected and the head will retreat to cylinder zero.

5.6.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 disk cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

5.6.5 Reformatting

The RK05 cartridge can be reformatted in the field while the RL01K/RL02K cartridges cannot. The imbedded servo information and Bad Sector File features greatly reduce the need to reformat in the field.

5.6.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.

APPENDIX A
RL11 CONFIGURATION AND INSTALLATION CONSIDERATIONS

A.1 SPC CONSIDERATIONS

The RL11 is a small peripheral controller (SPC) but does not unconditionally fit into any SPC slot. Early SPCs were always quad height modules or combinations of smaller (single or dual) modules that involved only four rows. Thus, the standard pin assignments applied only to rows C, D, E and F on a hex-height backplane. Many new options, such as the RL11, are hex-height modules and therefore require that rows A and B be vacant since some SPC slots use rows A and B for UNIBUS cables or power connectors. Some hex-height options require standard UNIBUS pinning on rows A and B and some require modified UNIBUS device (MUD) pinning. In the case of the RL11, the only connections used on rows A and B are for +5v and ground. Thus, these rows can be either standard UNIBUS or MUD pinning.

The early SPCs did not utilize Direct Memory Access (DMA) data transfers to/from memory and therefore those signals were not part of the original SPC pin assignments. Some of the newer options, such as the RL11, do utilize DMA transfers. There is a new pin assignment called SPC PRIME that includes these signals. If the RL11 is to be used in an older (non SPC-PRIME) slot then it is necessary to ensure that the following signals are wired on the backplane.

- Pin CA1 NPG In
- Pin CB1 NPG Out
- Pin EJ1 - NPR
- Pin CV1 – AC LO
- Pin CU1 – +15v

If the slot has SPC PRIME pinning then another precaution must be taken. NPG continuity is maintained across an empty SPC PRIME slot by a backplane jumper from pin CA1 to pin CB1. This jumper must be removed whenever a DMA-type option is installed, such as an RL11, and the jumper must be added if the module is removed. This consideration is in addition to the normal Bus Grant Continuity card used in row D of all empty SPC slots.

A.2 SPC CONSIDERATIONS

When configuring a UNIBUS system for the best priority assignments, two characteristics of a peripheral option must be taken into consideration. These are the peak word transfer rate and the TI time (TI time is a function of the peak transfer rate and the silo size). The RL11 has a peak transfer rate of 256 kHz (3.9 microseconds/word) and a TI time of 62.4 microseconds. This dictates its position in the priority scheme. The recommended priority scheme is listed below.

CPU
  Memory
  RK11/RK05
  TM11/TU10
  TC11/TU56
  RL11/RL01, RL02
  RJS04
  RM02
  RJP04
  RK611/RK06-RK07
  RP11C/RP03
  RJS03
  TJU16
  RF11/RS11
DB11

Other general configuration rules are:

- On a PDP-11 UNIBUS, a combination of two disk subsystems and a tape or floppy disk subsystem is considered maximum.
- On a PDP-11/70 system, one UNIBUS disk subsystem is considered maximum if there are MASSBUS disks.
- A disk subsystem should not be installed beyond a bus expander.

RL01/RL02 DISK SUBSYSTEM
USER'S GUIDE
EK-RL012-UG-004

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