

DAVE BAILEY

RM02/03 Disk Subsystem User's Guide



digital

RM02/03 Disk Subsystem User's Guide

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CHAPTER 1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This manual provides information related to the capabilities, installation, operation, and programming of the RM02/03 Disk Subsystem. With the appropriate Massbus controller, this subsystem can be used in the PDP-10, PDP-11, PDP-20, or VAX-11/780 computer-based systems.

This manual is intended primarily for operating and programming personnel. Installation and service should be performed only by qualified DEC field engineering and maintenance personnel.

1.2 GENERAL INFORMATION

The RM02/03 Disk Subsystem has a formatted capacity of 67 megabytes. The drive is housed in a free-standing cabinet and is compatible with the following Massbus drive controllers: RH10, RH20, RH70, and in specific instances, the RH11. Either a 16-bit data word or 18-bit data word format can be utilized, allowing the drive to be configured in DECsystem-10, PDP-11, or DECSYSTEM-20 computer-based systems. In the 16-bit format, the maximum storage capacity is 33,710,080 data words per disk pack and 31,603,200 data words per pack in the 18-bit format. The transfer rate is 1.65 μ s (RM03) or 2.48 μ s (RM02) per word for a 16-bit word or 1.86 μ s (RM03) or 2.79 μ s (RM02) for an 18-bit word. The average seek time for either drive is 30 ms.

1.2.1 Media

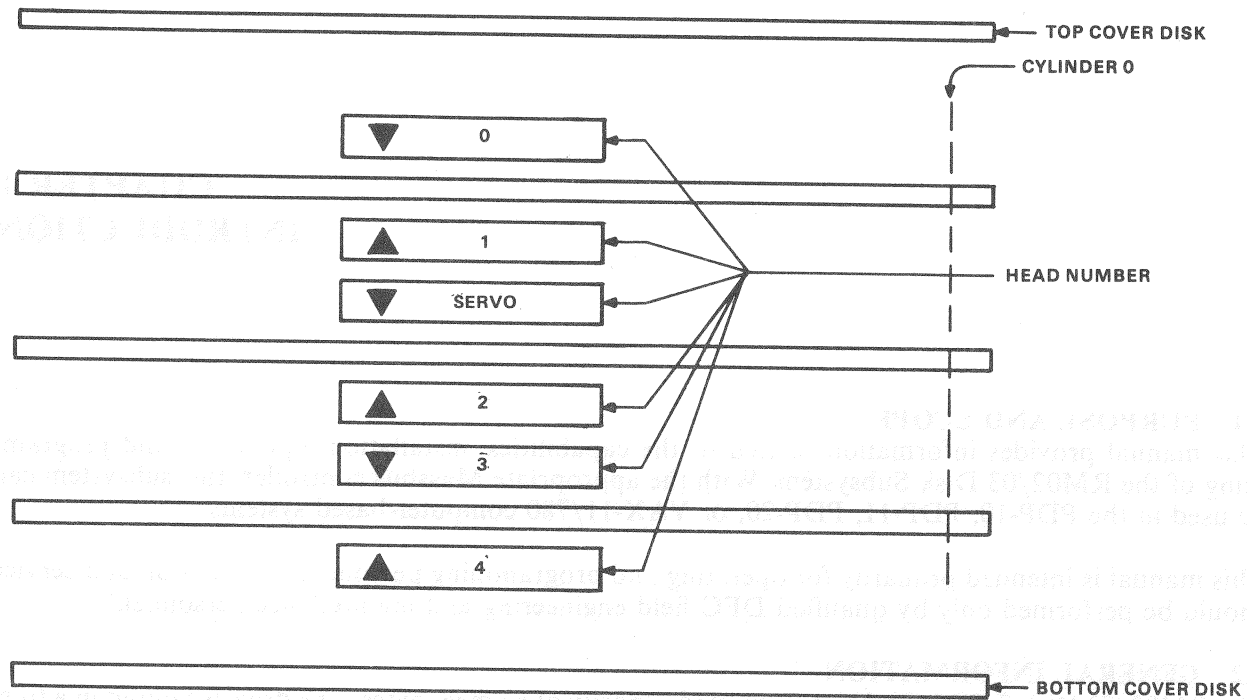
A type 9877 removable disk pack is used with the RM02 or RM03 drive. This 14-inch-diameter pack has five platters; the top and bottom platters are non-functional and only provide protection for the three inner disks. These three disks have six surfaces that are divided into five data storage surfaces and one servo track surface.

1.2.1.1 Pack Format - Each disk pack is divided into individually addressable locations as shown in Figure 1-1. The five read/write data surfaces (designated 0 through 4) are sectioned into 823 (0 through 822) concentric rings called cylinders. These cylinders consist of fixed-length sectors (consecutively numbered 0 to 29 for formats using 18 bits per word or numbered 0 to 31 for formats using 16 bits per word).

Each sector is divided into two information fields with gaps or spaces between these fields. The header field contains address information and the data field stores the 256 data words. The gaps between these fields permit the following actions.

1. Compensation for drive mechanical tolerances
2. Compensation for a decision or command change
3. Compensation for head switching from write to read or vice versa
4. Synchronization of the VFO (variable frequency oscillator)

The drive generates the sector gaps and the controller supplies the header and data information during a pack-formatting operation.



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Figure 1-1 RM03P Disk Pack with Head Location

The disk surface is prerecorded at the manufacturer with positioning signals used by the servo tracking circuits. This track is a read-only surface.

Each disk pack has a maximum formatted capacity of 663,667,200 bits. Table 1-1 shows how these bits are utilized.

1.2.1.2 Sector Format – The five major divisions of a sector are shown in Figure 1-2. Table 1-2 contains the overall bit/byte assignments for sectors of each data format.

1. **Sector Gap** – This gap, which is generated by the RM02 or RM03, contains 28 bytes of 0s and 1 sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 1-3.
2. **Header Field** – The header field is divided into three words as follows:
 - a. **Cylinder Address Word 0** – The 16 bits of this controller-generated word are shown in Figure 1-3 and described in Table 1-3.
 - b. **Sector/Track Address Word** – The 16 bits of this controller-generated word are shown in Figure 1-3 and described in Table 1-4.
 - c. **CRC Word** – This 16-bit word is generated by the cycle redundancy check (CRC) circuits of the drive. These circuits utilize the data in the first two header words to establish this CRC word. This provides a method for error detection in the reading or writing of the Header data.

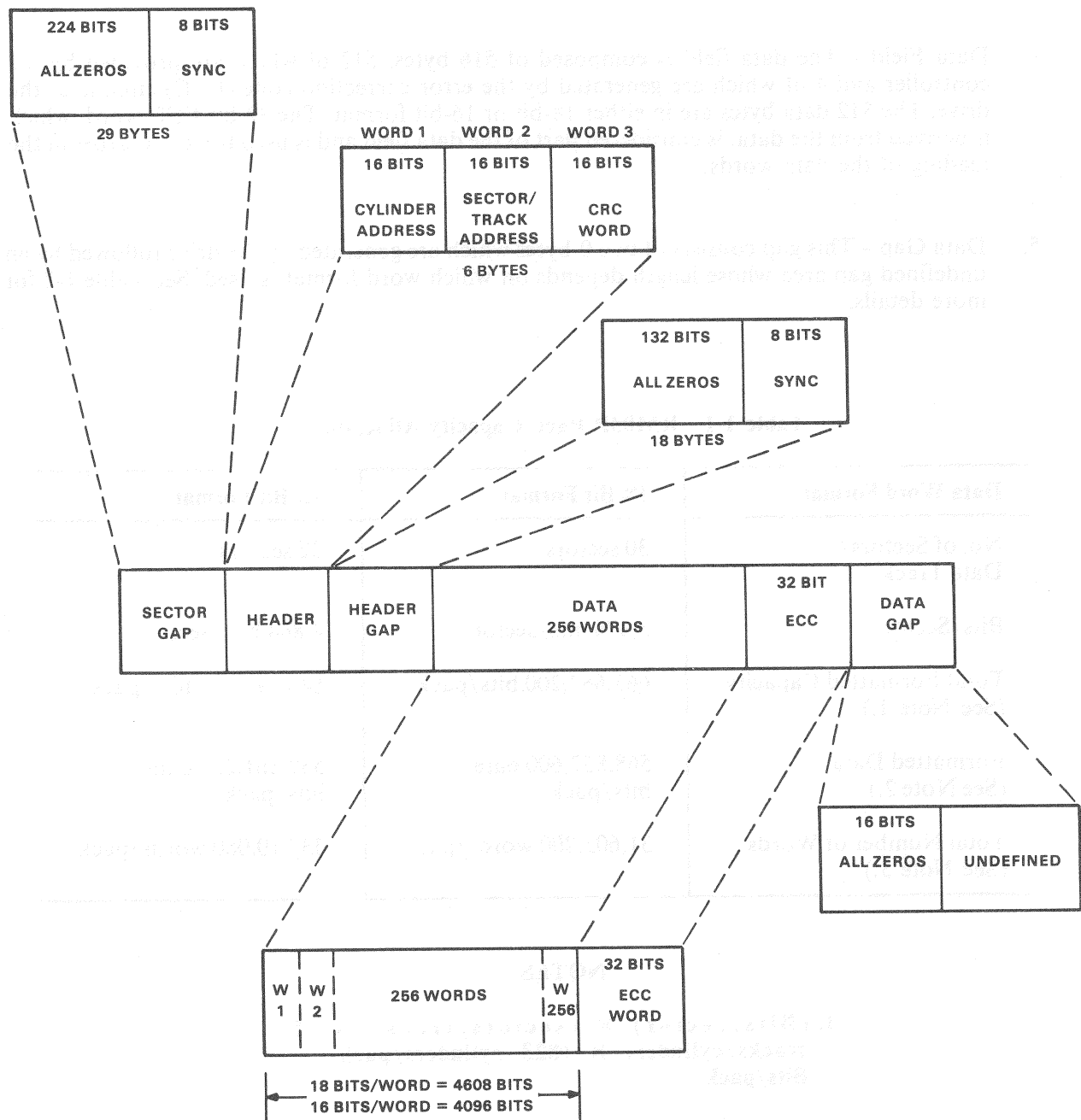
3. **Header Gap** – This gap, which is generated by the drive, contains 17 bytes of 0s and 1 sync byte. The sync byte, which marks the beginning of valid information, is shown in Figure 1-3. Headers are written in 16-bit mode only.
4. **Data Field** – The data field is composed of 516 bytes, 512 of which are provided by the controller and 4 of which are generated by the error correction code (ECC) circuits of the drive. The 512 data bytes are in either 18-bit or 16-bit format. The 32-bit ECC word, which is derived from the data, is considered part of the data field and is used to detect errors in the reading of the data words.
5. **Data Gap** – This gap consists of two 0-bytes which are generated by the drive followed by an undefined gap area whose length depends on which word format is used. See Table 1-2 for more details.

Table 1-1 RM03P Pack Capacity Allocation

Data Word Format	18-Bit Format	16-Bit Format
No. of Sectors/ Data Track	30 sectors	32 sectors
Bits/Sector	5,376 bits/sector	4,864 bits/sector
Total Formatted Capacity (See Note 1.)	663,667,200 bits/pack	640,491,520 bits/pack
Formatted Data (See Note 2.)	568,857,600 data bits/pack	539,361,280 data bits/pack
Total Number of Words (See Note 3.)	31,603,200 words/pack	33,710,080 words/pack

NOTES

1. $(\text{Bits/sector}) \times (\text{sectors/track}) \times (5 \text{ tracks/cylinder}) \times (823 \text{ cylinders/pack}) = \text{Bits/pack}$
2. $(\text{Bits/data word}) \times (256 \text{ words/sector}) \times (\text{sectors/track}) \times (5 \text{ tracks/cylinder}) \times (823 \text{ cylinders/pack}) = \text{Formatted data word bits/pack}$
3. $(\text{Formatted data word bits}) \div (\text{bits/word}) = \text{Words/pack}$



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Figure 1-2 Sector Format

Table 1-2 Assignment of Bits/Bytes in Sectors

Sector Location	18-Bit/Word Format		16-Bit/Word Format	
	Bytes	Bits	Bytes	Bits
Sector Gap	29	232	29	232
Header Field	6	48	6	48
Header Gap	18	144	18	144
Data Field	580	4640	516	4128
Data Gap (fixed)	2	16	2	16
Undefined	37	296	59	472
Total per Sector	672	5376	630	5040

NOTE

All byte descriptions in Table 1-2 are in terms of 8-bit bytes.

Table 1-3 Cylinder Address Bit Assignments

Bit	Name	Description
0-9	CYL	Ten bit locations for the address of the cylinder. Any decimal number from 0 to 822 is valid. Bit 0 is the least-significant bit.
10, 11	Unused	Always 0s.
12	FMT	The format bit that establishes whether the sector is formatted using 18-bit words or 16-bit words. When a 0, 18-bit; when 1, 16-bit.
13	Unused	Always 0.
14	UF	The location where the user can identify this sector as being bad so that data is not recorded here. A 0 indicates a bad sector; 1 a good sector.
15	MF	The location used by the disk pack manufacturer to indicate a bad sector. A 1 indicates bad; a 0 good.

Table 1-4 Sector/Track Address Bit Assignments

Bit	Name	Description
0-4	SA	These five bits contain the address of the sector. Valid decimal numbers are 0-29 for 18-bit formats and 0-31 for 16-bit formats.
5-7	Unused	Always 0s.
8-10	TA	These three bits contain the track address. Valid numbers are 0-4.
11-12	Unused	Reserved for future use.
13-15	Unused	Always 0s.

SYNC BYTE FORMAT

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1

CYLINDER ADDRESS FORMAT (First Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MF	UF	0	FMT	0	0	CYL 512	CYL 256	CYL 128	CYL 64	CYL 32	CYL 16	CYL 8	CYL 4	CYL 2	CYL 1

SECTOR/TRACK ADDRESS FORMAT (Second Header Word)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	*TA 16	*TA 8	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1

*RESERVED FOR FUTURE USE (ARE NORMALLY ZERO).

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Figure 1-3 Header Bits and Sync Byte Format

1.2.2 Subsystem Features and Capabilities

All RM02s and RM03s have error detection and error isolation operations performed on all information (data and header) read from the disk. This feature permits the software to correct detected errors and recover the data that would normally be incorrect.

These drives also have the ability to accept offset commands that cause the heads to move off the track centerline in a program-controlled attempt to recover data that is not normally recoverable. The offset distance is a fixed 200 μ m on either side of the track centerline.

Data is recorded on the disk in fixed-number sector blocks depending on the word length used. There are always 30 sectors per cylinder for 18-bit formats and 32 sectors for 16-bit formats. Each sector contains unique cylinder, sector, and track information encoded in a header block. This block also has provisions for accepting manufacturer- or user-specified codes to indicate that the sector is unacceptable for data storage.

The RM02 and RM03 incorporate a unique integrated backplane that permits dual-port, matched-impedance, Massbus connections to be made directly on to the backplane. This eliminates the requirement for multiple internal cables for the interface. This integrated backplane also simplifies the interconnections of Massbus cables, as up to eight RM02s or RM03s can be daisy-chained from a controller.

Extensive diagnostic programs are available for maintenance procedures. An off-line tester is also available that is used to isolate drive associated faults.

Recording on the disk is by the Modified Frequency Modulation method, commonly referred to as the Miller-Encoded Recording Technique.

The RM02 or RM03 Disk Subsystem also offers a dual-port capability, enabling it to be accessed through two different RH controllers.

1.2.3 Reference Documentation

A list of the related hardware documentation is presented in Table 1-5.

When ordering documentation, the first two letters are unique and identify the type of media. The prefix EK or ER is used for all hard-copy hardware manuals, and EP is used to designate microfiche documentation.

Manual Title	Control Number
RM03 Disk Drive Technical Manual	ER-ORM03-TM
RM03 Disk Drive Maintenance Print Set	ER-ORM03-MP
RM02 Disk Drive Technical Manual	ER-ORM02-TM
RM02 Disk Drive Maintenance Print Set	ER-ORM02-MP
RM02/03 Adapter Technical Description	EK-RM023-TD
RM02/03 Disk Drive Service Manual	EK-RM023-SV
RM02 Disk Subsystem Illustrated Parts Breakdown	EK-ORM02-IP
RM03 Disk Subsystem Illustrated Parts Breakdown	EK-ORM03-IP
RM02 Field Maintenance Print Set	MP-00456
RM03 Field Maintenance Print Set	MP-00350

1.3 SUBSYSTEM CONFIGURATION

Each RM02 or RM03 Disk Subsystem is composed of two hardware elements: the RM02/03 adapter and a storage module drive (SMD). Both of these subsystem elements are located within a single cabinet.

To operate this disk subsystem, a high-speed Massbus controller is needed to interface the Massbus to the computer memory bus. This provides a high-speed path for direct memory transfers to take place. Each Massbus controller can handle anywhere from one to eight RM02 or RM03 Disk Subsystems as shown in Figure 1-4.

Since the RM02/03 Disk Subsystem can be used in any one of four different DIGITAL computer systems, five different Massbus controllers are available. Table 1-6 shows which Massbus controller is used for which computer system.

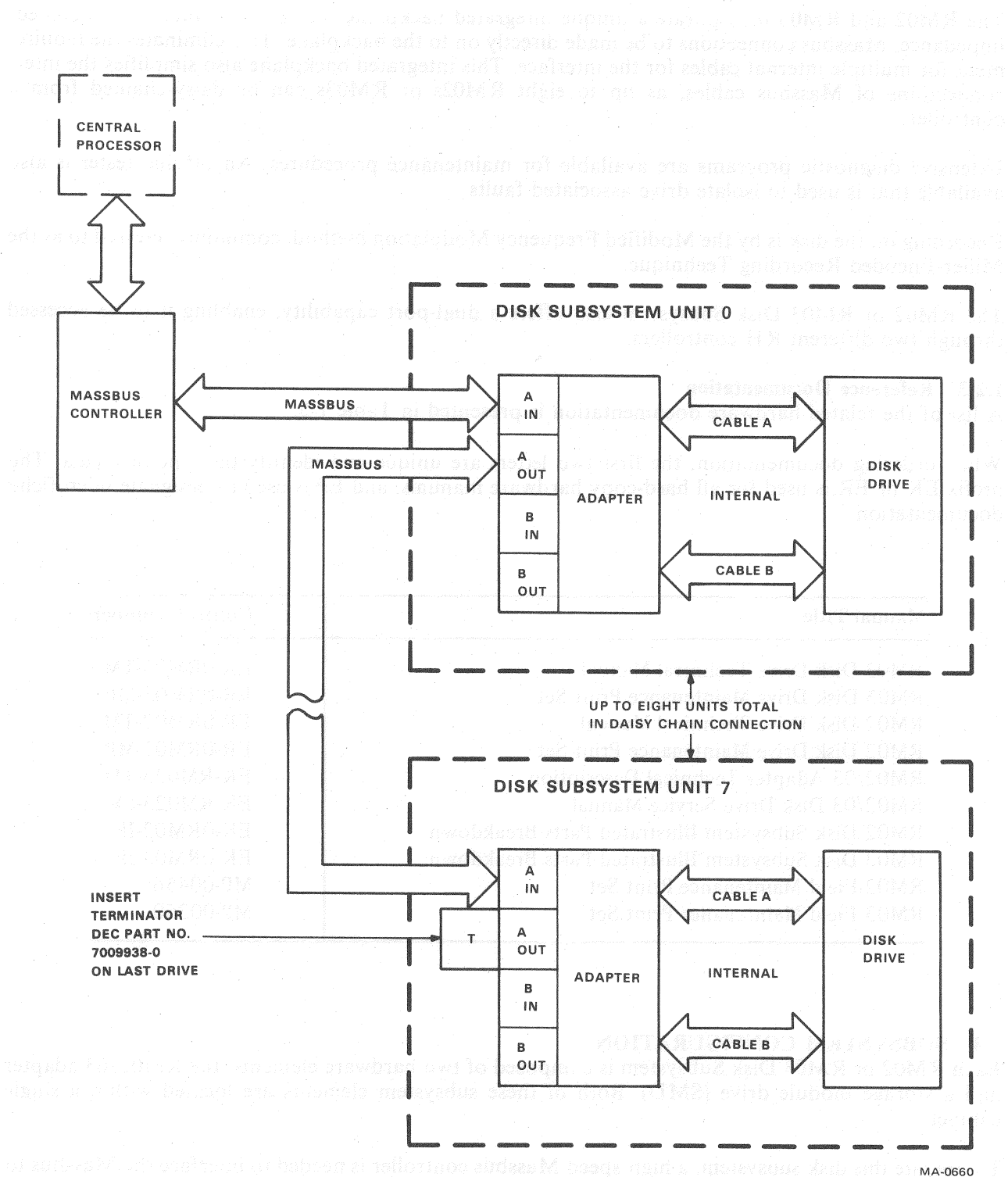


Figure 1-4 Single-Port Subsystem Configuration

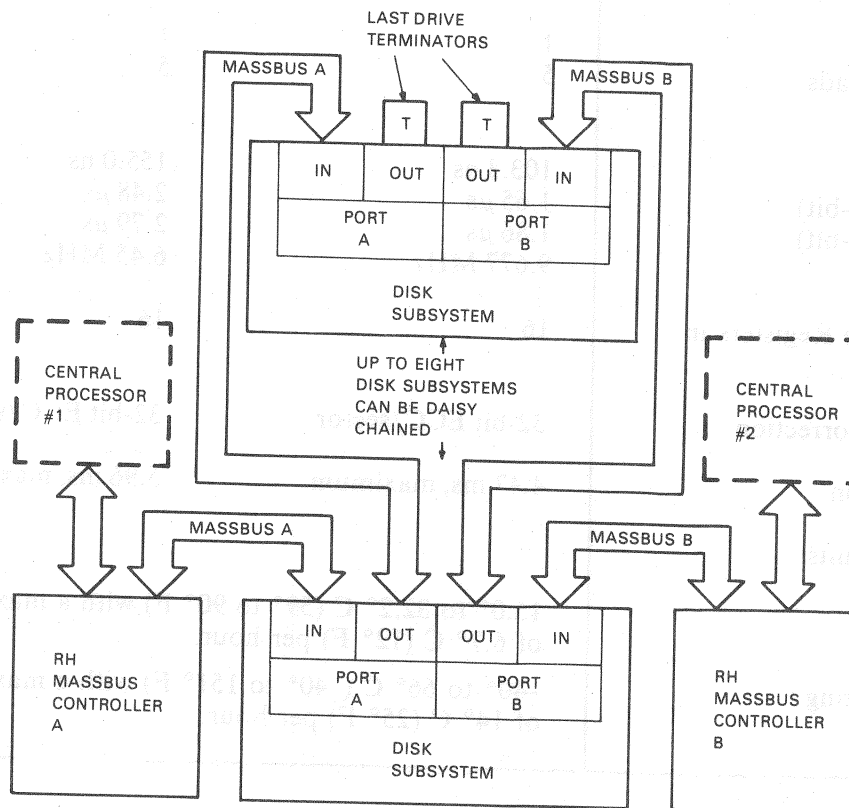
The RM02/03 Disk Subsystem also has a dual-port capability that allows it to be controlled in a time-shared fashion from two separate Massbus controllers. Figure 1-5 shows how this dual-port option is configured up to the controllers.

1.4 SUBSYSTEM SPECIFICATIONS

Performance, power, environmental, and physical specifications for the RM02/03 Disk Subsystem are listed in Table 1-7. The specifications for the disk pack are provided in Table 1-8.

Table 1-6 RH Massbus Controller Types

Computer System	Massbus Controller
Small PDP-11s PDP-11/70 LCG Products VAX-11/780	RH11 Controller RH70 Controller RH11C Controller VAX MBA



MA-0647

Figure 1-5 Dual-Port Subsystem Configuration

Table 1-7 RM02/03 Specifications

Specification	Limit	
Seek Time	RM03	RM02
Maximum seek (822 cylinders)	55 ms	55 ms
One cylinder seek (maximum)	6 ms	6 ms
Average seek	30 ms	30 ms
Seek to the same cylinder	37.5 μ s	37.5 μ s
Latency		
Speed	3600 rev/min	2400 rev/min
Maximum latency	17.3 ms	25.9 ms
Average latency	8.33 ms	12.5 ms
Start/Stop time		
Start (maximum)	35 s	25 s
Start (typical)	25 s	15 s
Stop (with power) (maximum)	35 s	20 s
Stop (with power) (typical)	25 s	10 s
Stop (without power)	120 s	60 s
Heads		
Servo head	1	1
Read/write heads	5	5
Data Rates		
Bit cell time	103.3 ns	155.0 ns
Word rate (16-bit)	1.65 μ s	2.48 μ s
Word rate (18-bit)	1.86 μ s	2.79 μ s
Bit rate	9.677 MHz	6.45 MHz
No. of Addressable Registers in RM02/03 Adapter	16	16
Error Detection/Correction	32-bit ECC/sector	32-bit ECC/sector
Time for Correction	4.47 ms, maximum	5.96 ms, maximum
Environmental Limits		
Temperature		
Operating	15.0° to 32.2° C (59° to 90° F) with a maximum gradient of 6.7° C (12° F) per hour.	
Non-operating	-40° to 66° C (-40° to 151° F) with a maximum gradient of 14° C (25° F) per hour.	

Table 1-7 RM02/03 Specifications (Cont)

Specification	Limit	
Relative humidity		
Operating	20 to 80 percent (providing there is no condensation)	
Non-operating	5 to 95 percent (providing there is no condensation)	
Altitude		
Operating	305 m (1000 ft) below sea level to 2000 m (6500 ft) above sea level.	
Non-operating	305 m (1000 ft) below sea level to 4572 m (15,000 ft) above sea level.	
Electrical		
Voltages available (single-phase)	RM03 100 Vac +10, -10; 60 Hz 120 Vac +8, -18; 60 Hz 240 Vac +17, -27; 50 Hz	RM02 100Vac +10, -10; 60 Hz 120 Vac +8, -18; 60 Hz 240 Vac +17, -27; 50 Hz
Start current for:		
100 Vac, 60 Hz	33 A rms, maximum	TBS
120 Vac, 60 Hz	30 A rms, maximum	TBS
240 Vac, 50 Hz	22 A rms, maximum	TBS
100 Vac, 50 Hz	33 A rms, maximum	TBS
Line current		
Disk and carriage in motion		
100 Vac, 60 Hz	Total	Total
120 Vac, 60 Hz	11 A rms	TBS
240 Vac, 50 Hz	11 A rms	TBS
100 Vac, 50 Hz	7 A rms	TBS
	14 A rms	TBS
In standby mode		
100 Vac, 60 Hz	4.5 A rms	TBS
120 Vac, 60 Hz	4.5 A rms	TBS
240 Vac, 50 Hz	3.5 A rms	TBS
100 Vac, 50 Hz	7 A rms	TBS
Line Cord Length	213.4 cm (7 ft)	213.4 cm (7 ft)
Plug Type		
100 V/60 Hz	NEMA 5-15 P	NEMA 5-15 P
120 V/60 Hz	NEMA 5-15 P	NEMA 5-15 P
240 V/50 Hz	NEMA 6-15 P	NEMA 6-15 P
100 V/50 Hz	NEMA 5-15 P	NEMA 5-15 P
Disk Cartridge Type	RM03P	RM03P

Table 1-8 RM03P Disk Pack Specifications

Specification	Limits
Type	9877 disk pack
Disk Diameter	35.56 cm (14 in)
Number of Disks	5 (the upper and lower disks are not used for recording)
Number of Recording Surfaces	5 read/write and 1 read-only servo surface
Cylinders per Disk Pack	823
Total Number of Tracks	4115 per disk pack
Tracks per Cylinder	5
Bad Sector File	Cylinder 822, track 4
Environmental Requirements	
Temperature range (operating)	10° to 57° C (50° to 135° F); temperature change rate not to exceed 0.1° C (0.2° F) per minute.
Temperature range (non-operating)	-40° to 65° C (-40° to 150° F); temperature change rate not to exceed 14° C (25° F) per hour.
Relative Humidity	
Operating and non-operating	8 to 80 percent
Wet Bulb Reading	
Operating	25° C (78° F), maximum
Non-operating	30° C (85° F), maximum
Altitude	
Operating	Mean sea level to 3050 m (10,000 ft)
Non-operating	Mean sea level to 12,190 m (40,000 ft)
Stray magnetic fields	
Operating and non-operating	Not to exceed 50 oersteds

1.5 RM02/RM03 OPTIONS

The RM02/03 options are specified, according to their power requirements and their number of access ports. Table 1-9 shows what options are currently available.

Table 1-9 RM02/03 Options

RM02/03 Single-Port Options	
RM02-AA or RM03-AA	120 V/60 Hz
RM02-AD or RM03-AD	240 V/50 Hz
RM02-AE or RM03-AE	100 V/60 Hz
RM02-AF or RM03-AF	100 V/50 Hz
RM02/03 Dual-Port Options	
RM02-BA or RM03-BA	120 V/60 Hz
RM02-BD or RM03-BD	240 V/50 Hz
RM02-BE or RM03-BE	100 V/60 Hz
RM02-BF or RM03-BF	100 V/50 Hz

NOTE

A single-port drive is field-upgradable to dual-port capabilities.

Table 1-9 shows dual options are currently available. The RM03/03 options are specified according to their power rating. The RM03/03 options are specified according to their power rating.

Table 1-9 RM03/03 Options

RM03/03 Single-Port Options	
120 V/50 Hz	RM03-AA or RM03-AA
240 V/50 Hz	RM03-AD or RM03-AD
100 V/60 Hz	RM03-AE or RM03-AE
100 V/50 Hz	RM03-AF or RM03-AF
RM03/03 Dual-Port Options	
120 V/50 Hz	RM03-BA or RM03-BA
240 V/50 Hz	RM03-BD or RM03-BD
100 V/60 Hz	RM03-BE or RM03-BE
100 V/50 Hz	RM03-BF or RM03-BF

NOTE
A single-port device is field-upgradeable to dual-port capabilities.

CHAPTER 2 INSTALLATION

2.1 INTRODUCTION

This chapter details the information required to install an RM02 or an RM03 Disk Subsystem. There is a variety of possible combinations of drives, controllers, and processors, and Table 2-1 lists the currently acceptable configurations.

Table 2-1 Subsystem Configurations

Drive	Controller	Processor
RM02	RH11	PDP-11 (excluding PDP-11/70)
RM02/RPxx mix	RH11	PDP-11 (excluding PDP-11/70)
RM03	RH70	PDP-11/70
RM03/RPxx mix	RH70	PDP-11/70

Any special information regarding the drive or drive mix will be detailed in the paragraphs describing the specific controller's installation.

2.2 SITE PREPARATION AND PLANNING

This paragraph describes power, space, environmental, cable length, and safety requirements that must be considered before installation of the RM02 or RM03 Disk Subsystem.

2.2.1 Environmental Considerations

The RM02 and RM03 Disk Subsystems are designed to operate in a business or light industry environment. Although cleanliness is an important consideration in the installation of any computer system, it is particularly crucial for proper operation of a disk drive. The RM03P disk cartridge is not sealed while being loaded and is therefore vulnerable to dust or smoke particles, fingerprint smudges, hair, lint, etc. These minute obstructions can cause head crashes, resulting in catastrophic damage to the read/write heads and disk surfaces.

2.2.1.1 Cleanliness – The drive can operate in an ambient of less than one million particles (0.5 micron or larger in diameter) per cubic foot of air. The drive contains a filter system which, under these conditions, maintains the particle count within the cartridge below 100 particles per cubic foot.

2.2.1.2 Space Requirements – The space requirements for each drive is shown in Figure 2-1. The drives may be arranged so that they are either immediately adjacent to each other, or separated by a distance of up to 61 cm (2 ft) maximum. *If the drives are arranged so that they are immediately adjacent to each other, they will have to be pulled out of line to perform some types of service.*

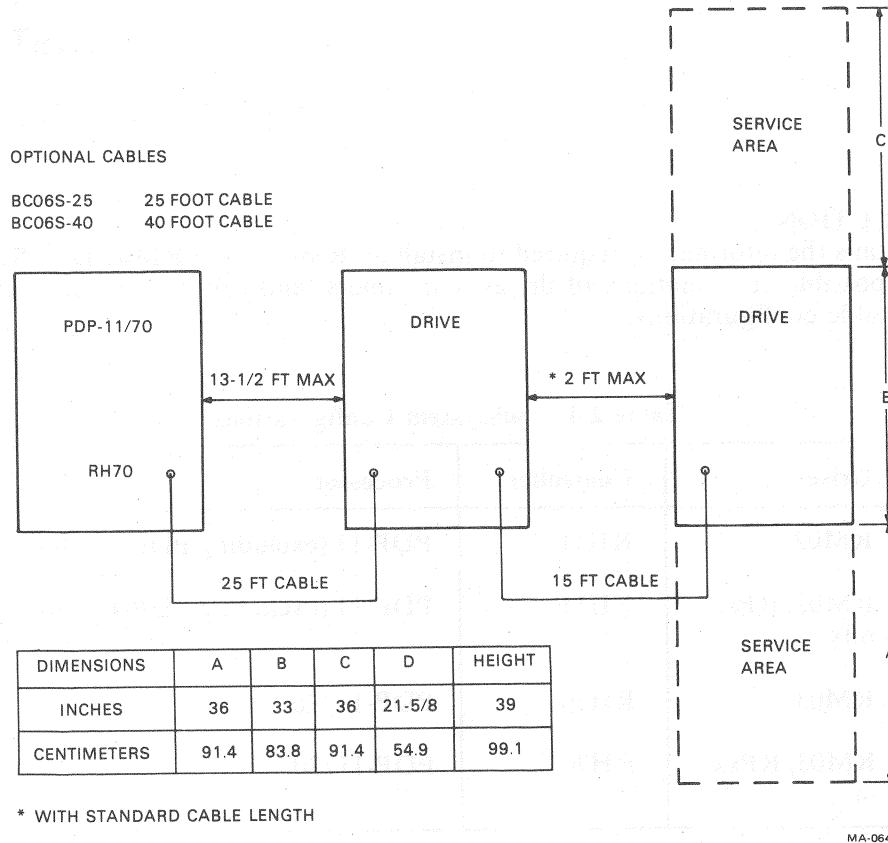


Figure 2-1 Disk Subsystem Space Requirements

The maximum subsystem Massbus cable length is 21.4 m (160 ft). To calculate drive location, assume each drive uses 4 m (13 ft) of Massbus cable within the drive [2 m (6-1/2 ft) in and 2 m (6-1/2 ft) out]. Allow 1.5 m (5 ft) of cable for the connection to the RH controller inside its cabinet. Hence, the first drive may be located up to 4.1 m (13-1/2 ft) from the controller as shown in Figure 2-1.

When calculating the total cable length, add an extra 0.5 m (1-1/2 ft) for each MBA backplane.

2.2.1.3 Floor Loading – The weight of the disk drive alone (196 kg/430 lb) will not place undue stress on most office-building, industrial-plant, or raised-computer-room floors. However, the added weight of the number of cabinets and drives should be considered in relation to the weight of existing computer systems plus needs for possible future expansion.

2.2.1.4 Heat Dissipation – The heat dissipation of some RM02 or RM03 Disk Subsystems may reach 2500 Btu/hour, maximum. The approximate cooling requirements for the entire system can be calculated by multiplying this figure by the number of drives, adding the result to the total heat dissipation of the other system components, and then adjusting the total figure to compensate for personnel, cooling system efficiency, etc. It is advisable to allow a safety margin of at least 25 percent above the maximum estimated requirements.

2.2.1.5 Acoustics – Most computer sites require at least some degree of acoustical treatment. However, the disk subsystem should not contribute unduly to the overall system noise level. Ensure that the acoustical materials used do not produce or harbor dust.

2.2.1.6 Temperature – The operating temperature range of the RM02 or RM03 Disk Subsystem is from 15° C (59° F) to 32° C (90° F). The maximum temperature gradient is 7° C (12° F) per hour. The non-operating temperature range is from -40° C (-40° F) to 66° C (151° F) with a maximum gradient of 20° C (36° F) per hour.

2.2.1.7 Relative Humidity – Humidity control is important for proper operation of any computer system since static electricity can cause memory errors as well as permanent damage to logic components. The RM02 and RM03 Disk Subsystems are designed to operate within a relative humidity range of 20 to 80 percent with a maximum wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F). The non-operating relative humidity range is from 5 to 95 percent, with a maximum wet bulb temperature of 46° C (115° F).

2.2.1.8 Altitude – Computer system operation at high altitudes can result in heat dissipation problems. Altitude also affects the flying height of heads in disk drives. The maximum altitude specified for operating the RM02 or RM03 Disk Subsystem is 2000 m (6500 ft). However, the maximum allowable operating temperature is reduced by a factor of 1.8° C/1000 m (1° F/1000 ft) for high-altitude sites. Thus, the maximum allowable operating temperature at 2000 m (6500 ft) would be reduced to 28° C (83.5° F).

2.2.1.9 Attitude/Mechanical Shock – Performance of the RM02 or RM03 Disk Subsystem will not be affected by an attitude where maximum pitch and roll do not exceed ± 5 degrees.

The subsystem is designed to operate while a half-sine shock pulse of 2 G peak and 10 ms maximum duration is applied once in either direction of three orthogonal axes (3 pulses total).

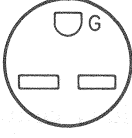
2.2.1.10 Power and Safety Precautions – The RM02 or RM03 Disk Subsystem presents no unusual additional fire or safety hazards to an existing computer system. AC power wiring should be carefully checked, however, to ensure that its capacity is adequate for the added load and for any contemplated expansion. The disk subsystem is UL-listed and CSA-certified.

2.2.2 AC Power Wiring

DEC power wiring conforms to UL, CSA, and VDE standards. This means that the wire used as equipment ground is green and yellow. It carries no load current (except in emergency), but does carry leakage current. No equipment is permitted to leave DEC that does not have a grounding connection to its frame.

The ac return line (also called the "identified" conductor, neutral, common, cold lead, etc.) is blue. It must not be used to ground equipment. Its purpose is to conduct current.

The ac input line (hot wire) is brown. Its purpose is to supply current to the system. The ac plugs and receptacles used on this subsystem are shown in Figure 2-2.

SOURCE	PLUG	RECEPTACLE	USED ON
120V 15A 1-PHASE	HUBBEL #5266-C NEMA # 5-15P DEC # 90-08938 	#5262 5-15R 12-05351 	ALL 120V TABLE-TOP COMPUTERS. STANDARD 120V LOW-CURRENT DISTRIBUTION. 120V TU10 UNITS. MOST 120V TERMINAL DEVICES.
240V 15A 1-PHASE	NEMA # 6-15P DEC # 90-08853 	6-15R 12-11204 	ALL 240V TABLE-TOP COMPUTERS. STANDARD LOW-CURRENT 240V DISTRIBUTION. MOST 240V TERMINAL DEVICES. 240V TU10.

MA-0913

Figure 2-2 Approved Electrical Plugs and Receptacles

2.3 DRIVE UNPACKING AND INSPECTION PROCEDURE

When delivered, the drive and its associated cabinetry are enclosed by a heavy cardboard carton and are attached to a shipping skid (Figure 2-3).

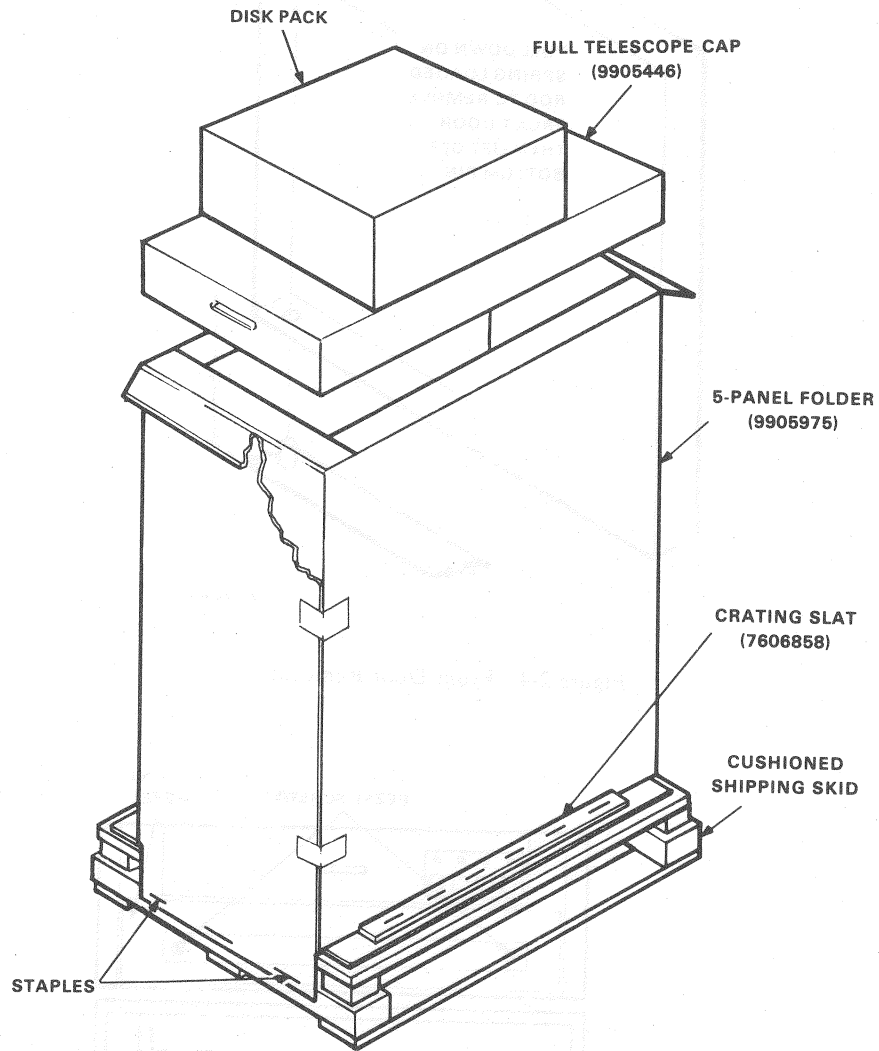
1. Inspect the outside of the container for damage. Then remove the plastic straps that secure the shipping carton to the skid.
2. Remove the disk pack box.
3. Remove the lid from the top of the disk drive carton.
4. Remove the staples that fasten the wooden crating slats and carton flanges to the skid.
5. Remove the shipping carton.
6. Inspect the cabinet and drive for physical signs of shipping damage. Retain all packing material and receipts in the event that any claims are filed for shipping damage. All damage claims should be filed promptly with the transportation company.

Digital Equipment Corporation should be notified immediately if a damage claim is made.

7. Inventory all hardware, cables, manuals, etc. in the shipping carton against the packing slip. Notify Digital Equipment Corporation immediately if any discrepancies exist.
8. Remove front door assembly (Figure 2-4).
9. Remove orange angle brackets (Figure 2-5) which attach MBA drawer assembly to cabinet frame.

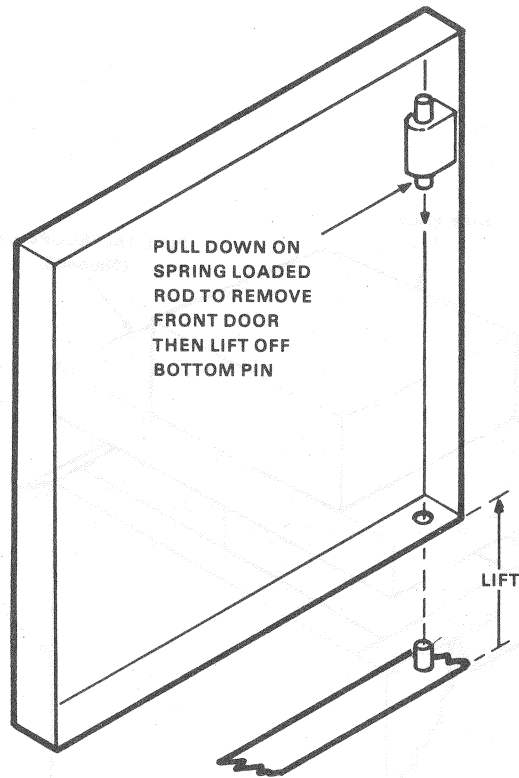
CAUTION

Do not misplace these brackets. They must be replaced before the installation is completed.



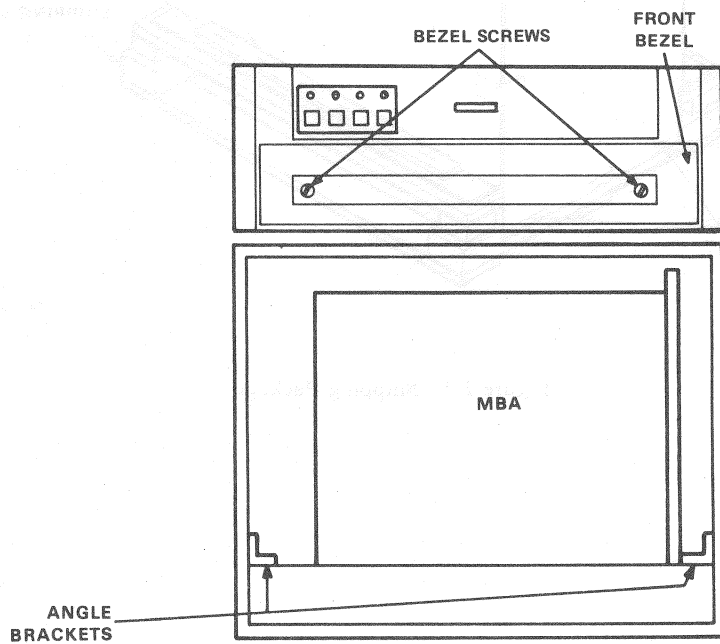
MA-0914

Figure 2-3 Shipping Package



MA-0649

Figure 2-4 Front Door Removal

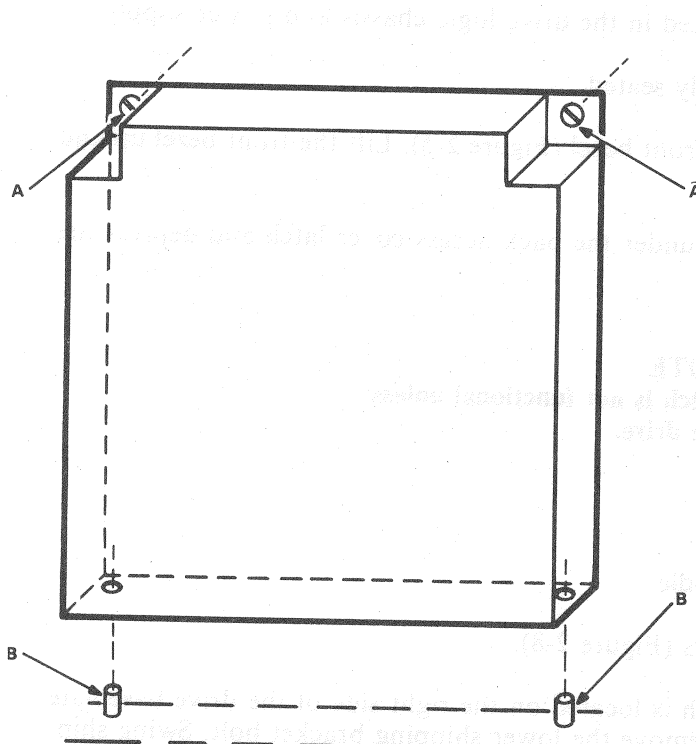


MA-0650

Figure 2-5 Front Bezel Location

10. Remove the rear cover assembly (Figure 2-6).

11. Slide the MBA drawer forward and remove the sheet-metal screws that attach the side panels (Figure 2-7) to the cabinet frame.

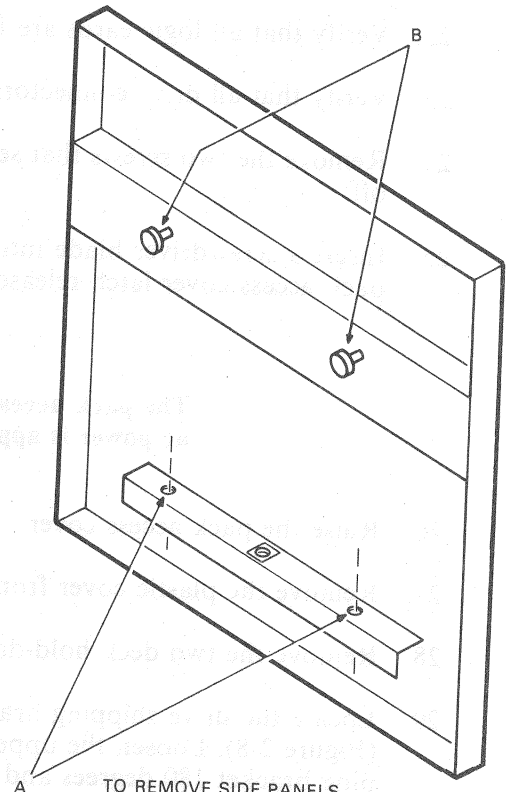


TO REMOVE REAR COVER:

1. LOOSEN LOCKING SCREWS (A).
2. LIFT REAR COVER OFF PINS (B).

MA-0651

Figure 2-6 Rear Cover Removal



TO REMOVE SIDE PANELS
REMOVE SCREWS AT LOCATIONS (A)
AND LIFT PANEL UP. FREE PINS (B),
THEN PULL OUTWARDS.

MA-0646

Figure 2-7 Side Panel Mounting Screws

12. Slide the MBA drawer back into position.
13. Lift off the side panels.
14. Remove the two bolts securing the cabinet to the shipping skid.
15. Remove all skid blocks and position the cabinet leveling feet so that the cabinet rolls freely on its casters.
16. Carefully lower the cabinet off the skid without jarring the cabinet.
17. Roll the cabinet to the area designated by the site preparation plan.
18. Extend the MBA slide forward. Loosen the screws on the MBA logic cage assembly and remove the cover.
19. Ensure that all MBA boards and cable connections are firmly seated.

20. Replace cage cover.
21. Loosen the two quarter-turn fasteners at the rear of the drive and then slide the rear cover back and lift it off.
22. Verify that all logic cards are firmly seated in the drive logic chassis and power supply.
23. Verify that all drive connectors are firmly seated.
24. Remove the two screws that secure the front bezel (Figure 2-5). Lift the front bezel up and off.
25. Insert a screwdriver blade into the slot under the pack access cover latch and depress the pack access cover latch release.

NOTE

The pack access cover latch is not functional unless ac power is applied to the drive.

26. Raise the pack access cover.
27. Remove the plastic cover from the spindle.
28. Remove the two deck hold-down screws (Figure 2-8).
29. Locate the drive shipping bracket which is located on the right side of the drive baseplate (Figure 2-8). Loosen the upper bolt. Remove the lower shipping bracket bolt. Swing shipping bracket 180 degrees and tighten upper bolt. Replace lower shipping bracket bolt.

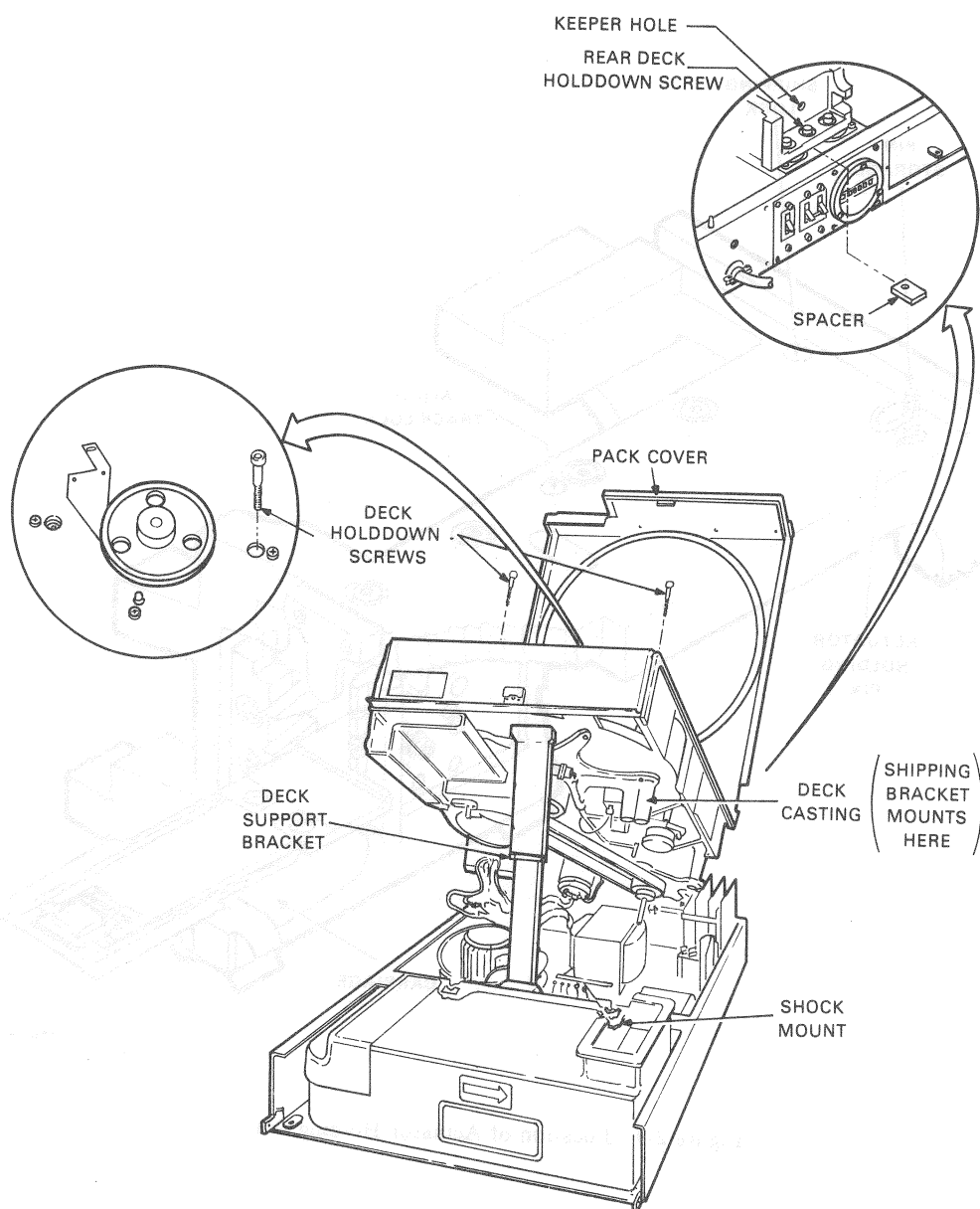
CAUTION

Do not remove or misplace the shipping bracket. It must be used any time the drive is moved.

30. Raise the drive deck and verify that all cabling is intact and that there are no broken or damaged wires.
31. Lower the drive deck and replace the two hold-down screws.
32. Remove the actuator holding pin from the hole labeled "Shipping Lock" and place it into the hole labeled "Pin Storage." The actuator holding pin is located on the rail bracket above the carriage coil assembly (Figure 2-9).
33. Remove the rear deck hold-down screw and spacer (Figure 2-10). Using the hold-down screw, fasten the spacer onto the actuator magnet housing via the keeper hole.

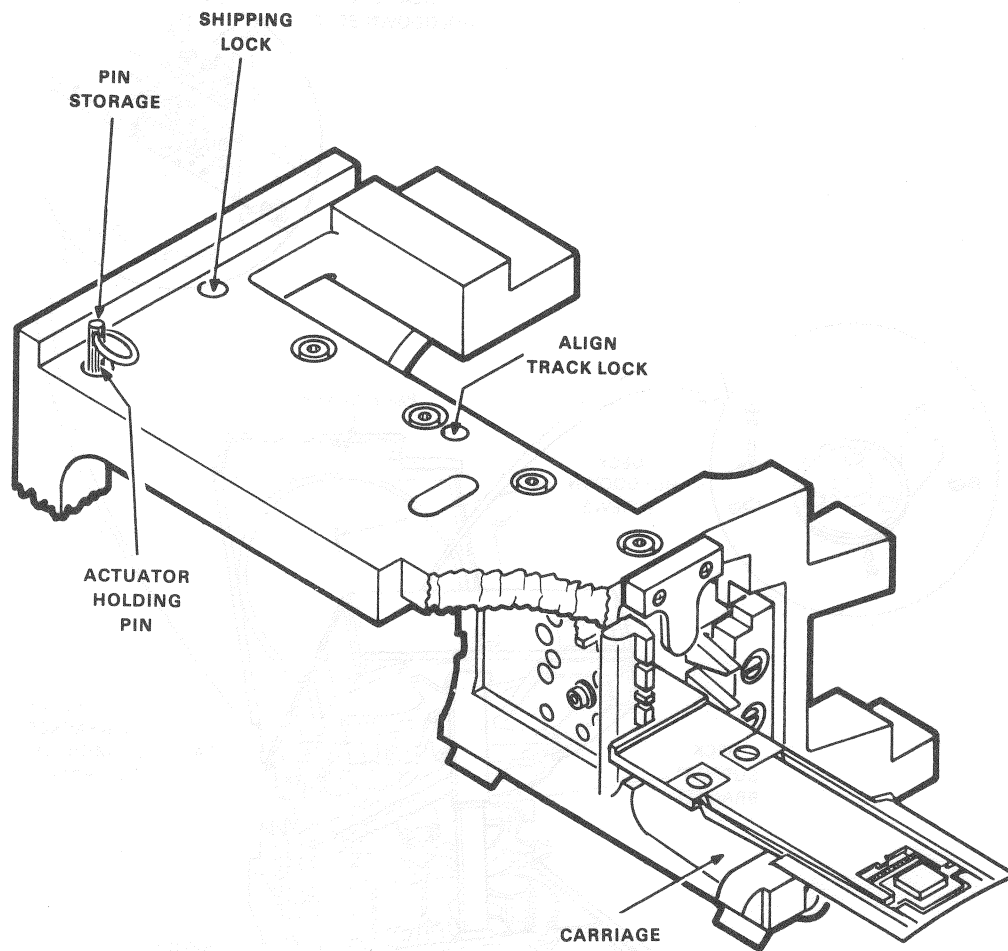
CAUTION

The spacer must be placed between the magnet housing and the baseplate any time the drive deck is raised in order to prevent damage to the rubber shock mounts.



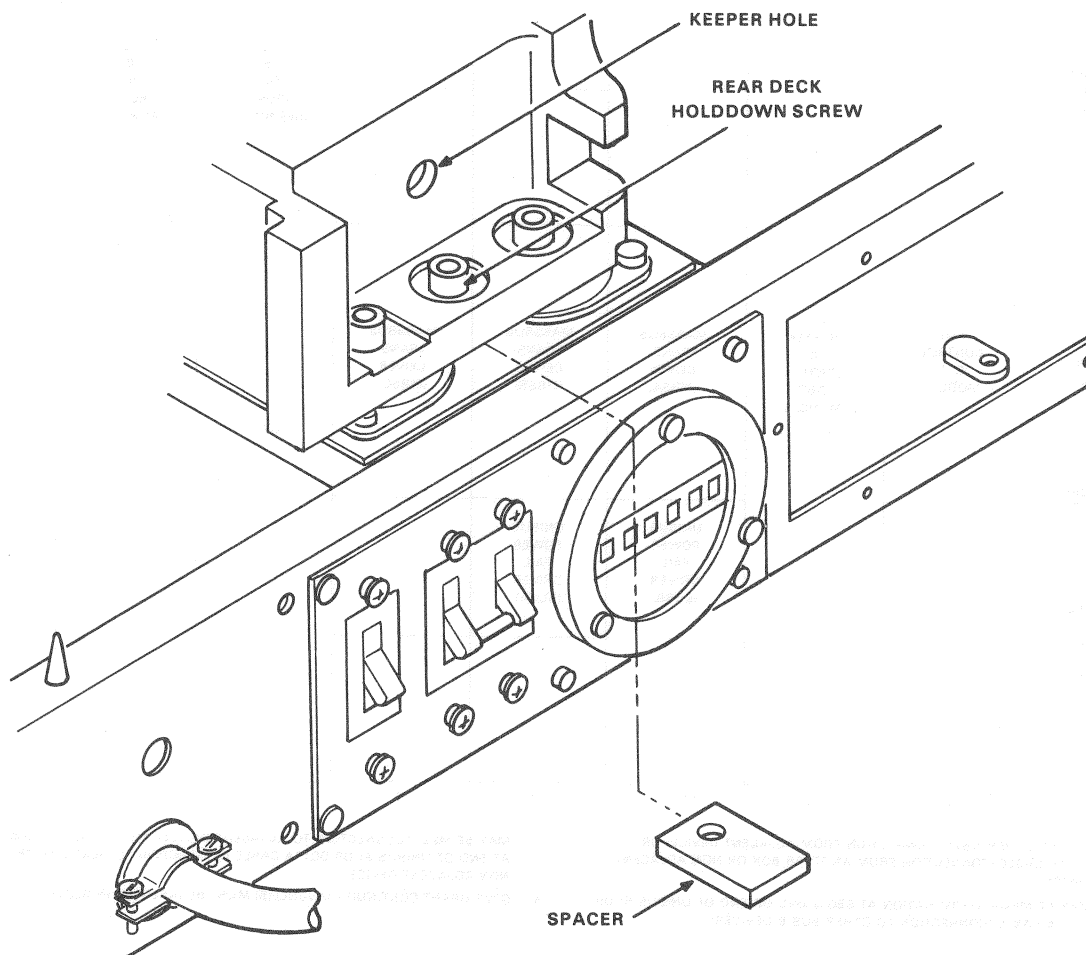
MA-0611

Figure 2-8 Deck Maintenance Position



MA-0607

Figure 2-9 Location of Actuator Holding Pin



MA-0609

Figure 2-10 Location of Rear Deck Holding Screw

2.4 RH11 CONTROLLER INFORMATION

The following paragraphs describe the mechanical and electrical installation, power checks, jumper configurations, and visual inspections necessary for installation of the RH11 controller. The RH11 controller will handle an RM02/RPxx drive mix. The particular details required to accommodate the mix are described in the individual paragraphs on jumper configurations.

2.4.1 Mechanical

The RH11 uses two hex-height modules and must be installed in a mounting box that accommodates hex-height modules. The modules are inserted in a double-system unit backplane which is installed in the mounting box with four thumbscrews. The double-system unit is oriented with the bus cable slots in line with the other options. Figure 2-11 shows a module utilization chart.

2.4.2 Electrical

The power cable connections, Unibus cable connections, and Massbus cable connections are described in the following paragraphs.

A	UNIBUS A IN (BUS A) (SEE NOTE 1)						UNIBUS B OUT (BUS B) (SEE NOTE 2)	UNIBUS B IN (BUS B) (SEE NOTE 2)	UNIBUS A OUT (BUS A) (SEE NOTE 3)
B	M7297								
C	PARITY CONTROL (PAC)	BUS CONTROL (BCT) MODULE	DATA BUFFER & CONTROL (DBC) MODULE	MASSBUS TRANS- CEIVER (MBSA)	MASSBUS TRANS- CEIVER (MBSB)	MASSBUS TRANS- CEIVER (MBS C)			
D	M7296						G727	G727	G727
E	CONTROL & STATUS REGISTERS (CSR)			UNIBUS POWER FAIL DRIVER (BUS B)	UNIBUS POWER FAIL DRIVER (BUS A)				
F									
	1	2	3	4	5	6	7	8	9

NOTES:

1. MAY BE EITHER M920 (CONNECTION FROM ADJACENT DEVICE) OR BC11A CABLE (CONNECTION FROM ANOTHER BOX OR NON ADJACENT DEVICE).
2. MAY BE M9300 (TERMINATION AT BEGINNING OR END OF UNIBUS B) OR BC11A CABLE (CONNECTION TO OTHER BUS B DEVICES).
3. MAY BE M920 (CONNECTION TO ADJACENT DEVICE), M930 (TERMINATION AT END OF UNIBUS A) OR BC11A CABLE (CONNECTION TO NEXT BOX OR NON ADJACENT DEVICE).
4. G727 GRANT CONTINUITY MODULE(S) MUST BE INSERTED IN SLOTS D

11-2384

Figure 2-11 RH11 Module Utilization

2.4.2.1 Power Cable Connections – Power is distributed to the RH11 modules via two power cables that attach to the printed circuit backplane assembly by quick-disconnect tabs. (Refer to RH11 wired assembly drawing, D-AD-7009397-0-0.) The power cables have Mate-N-Lok connectors on one end, which connect to the power distribution panel located above the backplane, and quick-disconnect tabs on the other end, which connect to the printed circuit backplane. The following chart shows the color codes associated with the power harness connections.

Red	+5 Vdc
Black	Gnd
Blue	-15 Vdc
Gray	+15 Vdc
Violet	DC LO (+3 V to +5 V)
Yellow	AC LO (+3 V to +5 V)
Brown	LTC 8 V peak-to-peak ac

CAUTION

When connecting the power cables to the backplane, ensure that backplane wires are not damaged. Also, do not cut AC LO and DC LO wires out of the power harness as they are used for power fail conditions on the Massbus and on both Unibus A and Unibus B ports.

After power connections have been made, check for power shorts with an ohmmeter. Ensure that all modules are firmly seated in the proper slots (Figure 2-11). Power-up the cabinet and measure voltages in accordance with values listed in the color code chart for power connections. After this is done, turn power off.

2.4.2.2 Unibus Cable Connections – The RH11 is a 2-port Unibus device capable of accepting two Unibus cable systems, designated Unibus A and Unibus B.

Unibus A Connections – The Unibus A cable slots connect the RH11 to the processor controlling it. The Unibus A cable enters the RH11 via slot A1, B1 and connects to the next device via slot A9, B9. (Refer to module utilization drawing, D-MU-RH11-0-01.)

Connections to slot A1, B1 are made via the BC11A Unibus cable if the RH11 is the first Unibus A device in the mounting box. Otherwise, connection to A1, B1 from the preceding device is made by an M920 Unibus jumper module. Connection to the next adjacent device on the Unibus is made via the M920 Unibus jumper module; it is made by a BC11A cable if the device is not adjacent.

NOTE

If the RH11 is the last device on Unibus A, an M930 terminator module is installed in slot A9, B9.

Unibus B Connections – Unibus B connections are generally made in systems with multiport memories. When the Unibus B port of the RH11 is not used, an M9300 terminator module (with jumper W1 cut) should be installed in slot A8, B8 to terminate Unibus B signals into the RH11. The second M9300 terminator module should *not* be used in order to conserve power. If the Unibus B port of the RH11 is used, connections are determined on the basis of whether a processor is connected to Unibus B. These connections are described below.

1. **Processor on Unibus B** – If a processor is connected to Unibus B, it is electrically connected at the beginning of the bus. In this case, the M930 terminator modules supplied with the processor are used for bus termination, and the two M9300 Unibus B terminator modules supplied with the RH11 are not used.

NOTE

The M9300 terminator may be used as a substitute for the M930 terminator if the jumpers are selected correctly.

The Unibus B cable connection to the RH11 is made via slot A8, B8 with a BC11A cable. Connection from the RH11 to the next device is made via a BC11A cable connected to slot A7, B7. If the RH11 is the last device on the bus, the M930 or M9300 terminator is installed in slot A7, B7 instead of the BC11A cable.

2. **No Processor on Unibus B** – If no processor is connected to Unibus B, a M9300 Unibus B terminator module must be selected as an NPR arbitrator. If one RH11 is connected to Unibus B, the RH11 is electrically connected at the beginning of the bus with the M9300 selected to act as an NPR arbitrator. One M9300 Unibus B terminator module is placed in slot A8, B8 of the RH11. Jumper W1 on this module must be cut to enable the arbitration logic. Connection to other devices on Unibus B, such as memory, is made via a BC11A cable

connected to slot A7, B7. The second M9300 Unibus B terminator module is installed in the last device on Unibus B. Jumper W2 is removed for terminating the Unibus with no processor connected.

NOTE

In this case, an M930 terminator module can be substituted for the M9300 Unibus B terminator in the last device slot. If more than one RH11 is installed, the user may have extra M9300 modules as a result of a particular configuration. Figures 2-12, 2-13, and 2-14 show typical Unibus configurations.

2.4.2.3 Massbus Cables – Massbus connections to the RH11 are made via three 40-conductor ribbon cables. These cables plug into three M5904 transceivers in the RH11 and are designated Massbus Cable A, Massbus Cable B, and Massbus Cable C. The connections are made as shown below.

Massbus Cable A	Install in M5904 module in slot C4, D4.
Massbus Cable B	Install in M5904 module in slot C5, D5.
Massbus Cable C	Install in M5904 module in slot C6, D6.

The Massbus cables are marked and should be inserted per the individual cable markings. To terminate the Massbus, a 7009938 terminator pack assembly should be plugged into the output connector(s) of the last drive (Figure 2-15).

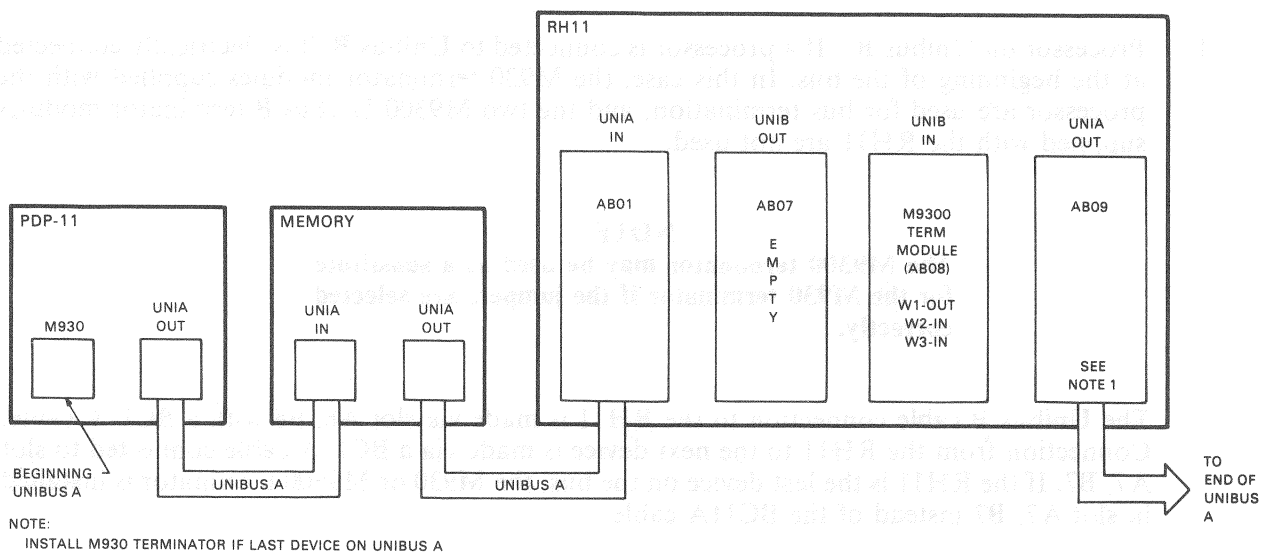


Figure 2-12 Single-Port Unibus Configuration

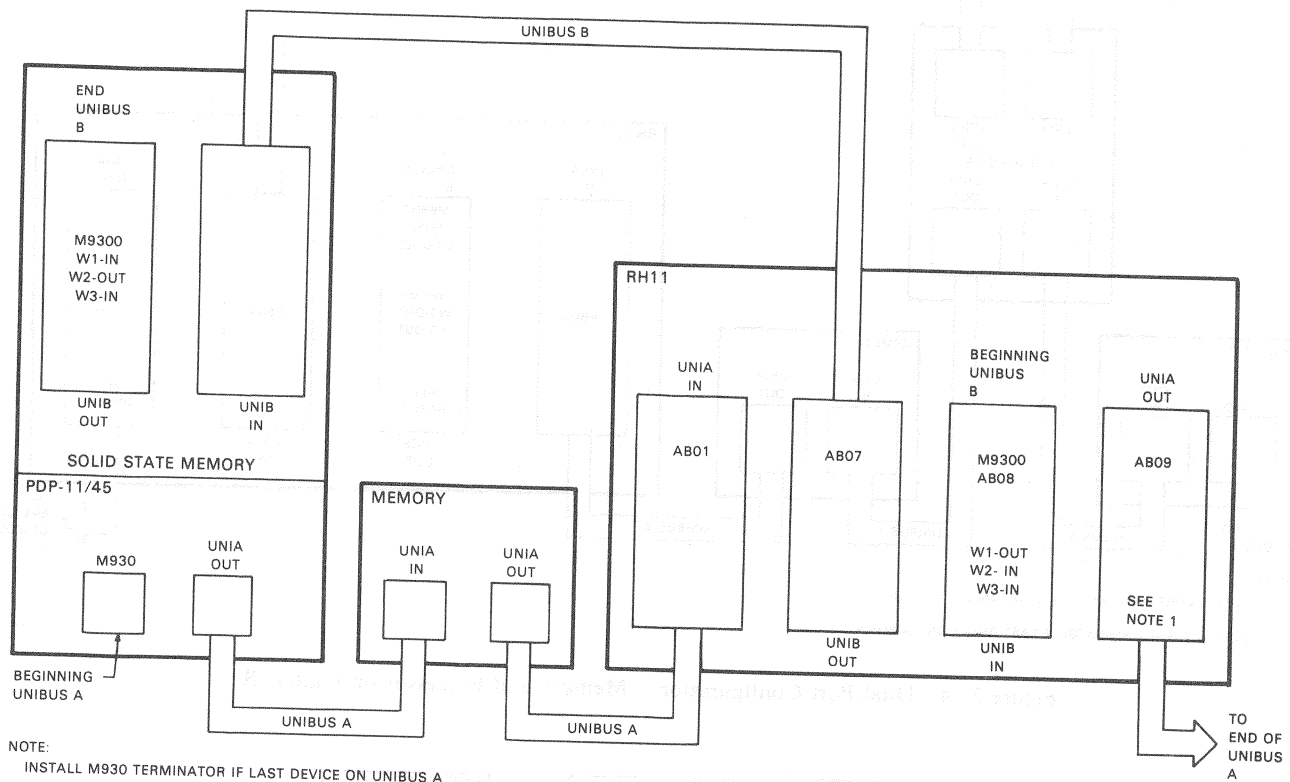
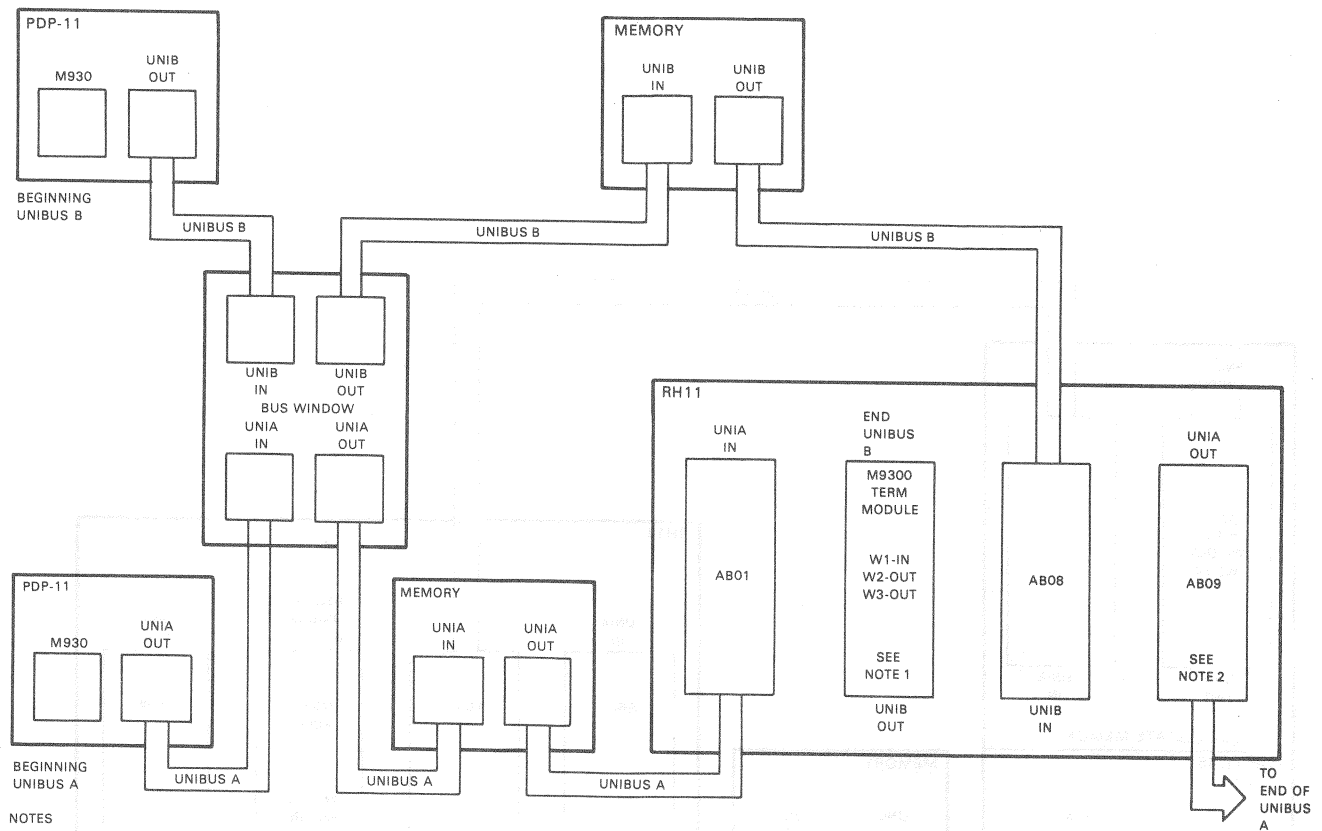
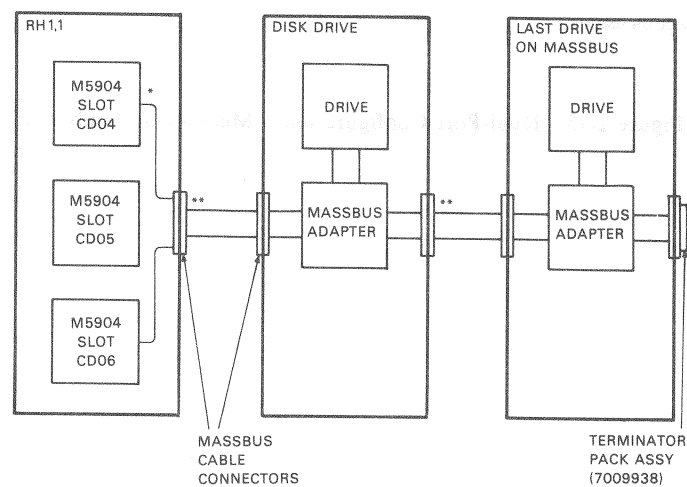


Figure 2-13 Dual-Port Configuration - Memory on Unibus B



11-2222

Figure 2-14 Dual-Port Configuration - Memory and Processor on Unibus B



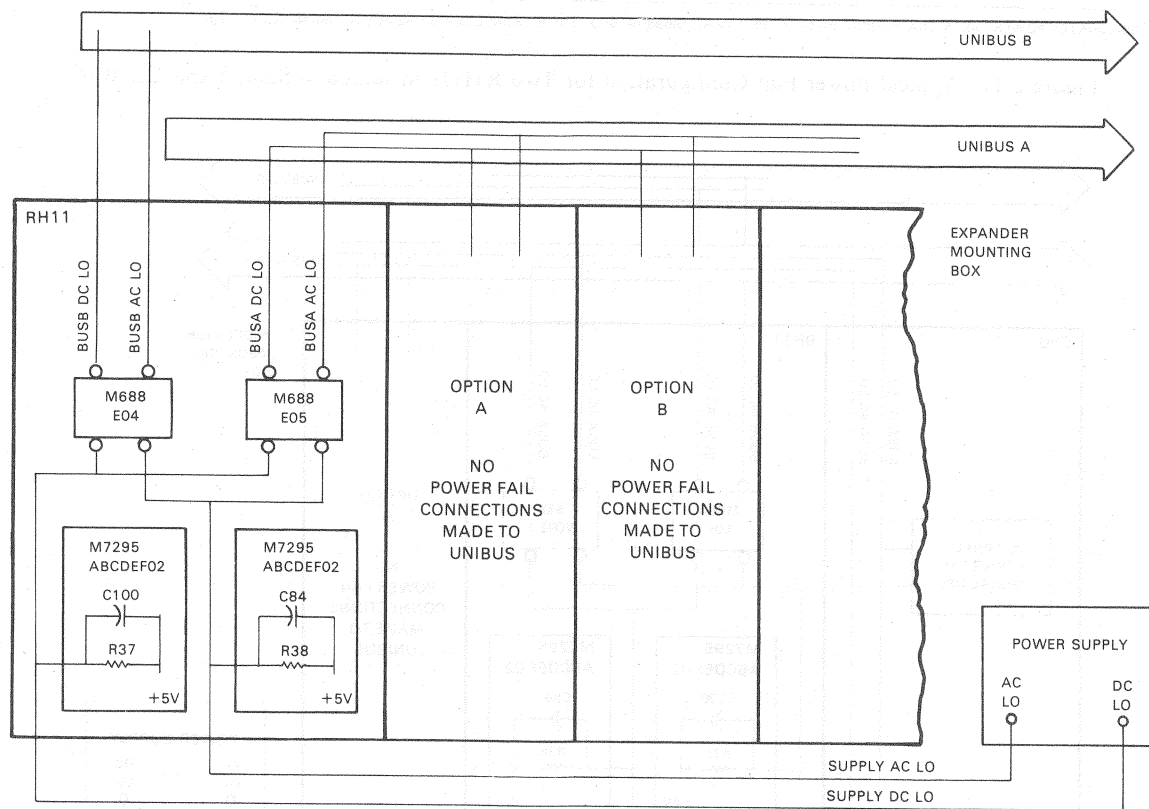
11-2561

Figure 2-15 Massbus Cable System Configuration

2.4.2.4 AC LO, DC LO – AC LO and DC LO signals from the RH11's power supply must be connected to the RH11. The wires supplying these signals *will not be cut* from the power harness. *There will be only one AC LO and one DC LO power fail connection to each Unibus for devices mounted in the same mounting box and sharing the same power supply.* Otherwise, power fail conditions would latch up due to positive feedback to the power fail logic. If a power fail connection for AC LO and DC LO is already made to a Unibus from a device in the same mounting box, the M688 power fail module in the RH11 for that Unibus is removed. The M688 module for Unibus A is located in slot E5 and the M688 module for Unibus B is located in slot E4. The following is a summary of power fail configuration rules.

1. For each mounting box, there is only one AC LO and DC LO power fail connection to a Unibus from the power supply.
2. Power supply AC LO and DC LO must always be wired to each RH11 via the power harness.
3. Power fail signals may only be disconnected from a Unibus in an RH11 by removing the appropriate M688 power fail driver module.
4. Power supply AC LO and DC LO should be disconnected from all other options mounted in the same box as the RH11 if they do not need those signals for internal operation.

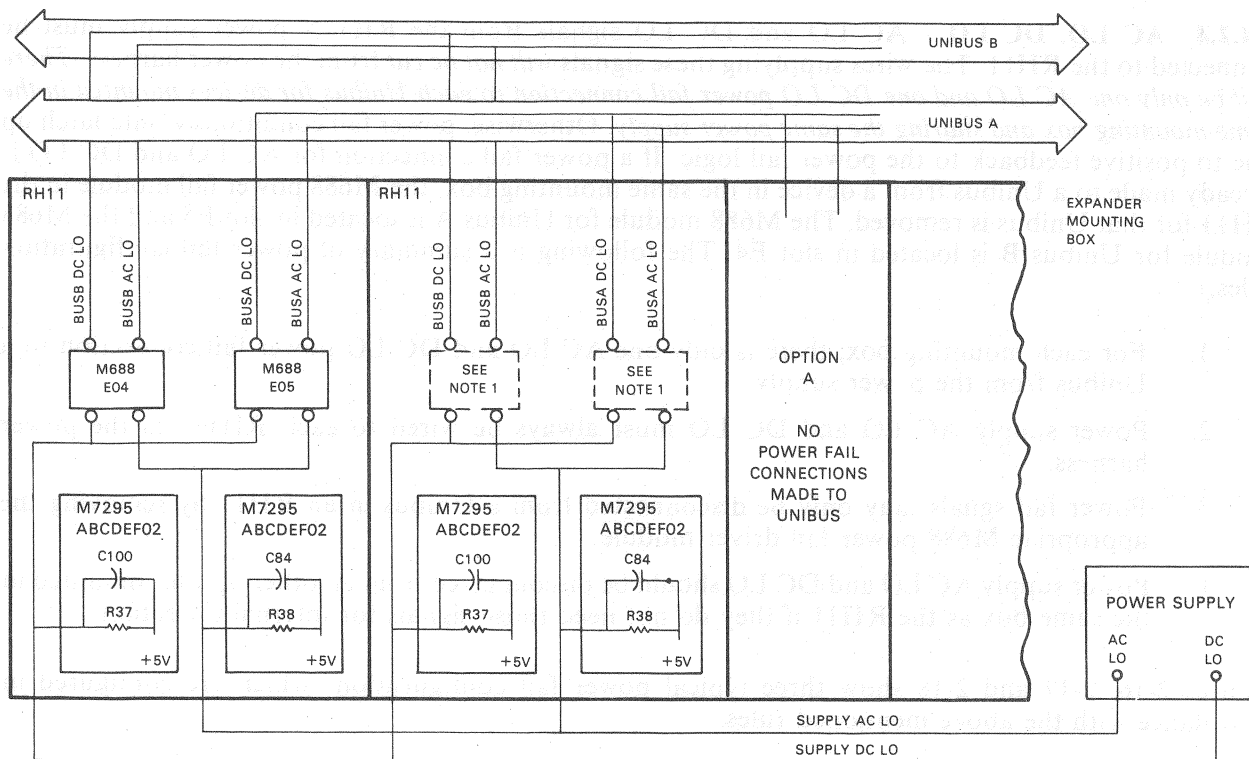
Figures 2-16, 2-17 and 2-18 show three typical power fail configurations which are configured in accordance with the above mentioned rules.



NOTE
ONE RH11 MOUNTED WITH OTHER OPTIONS IN
AN EXPANDER MOUNTING BOX.

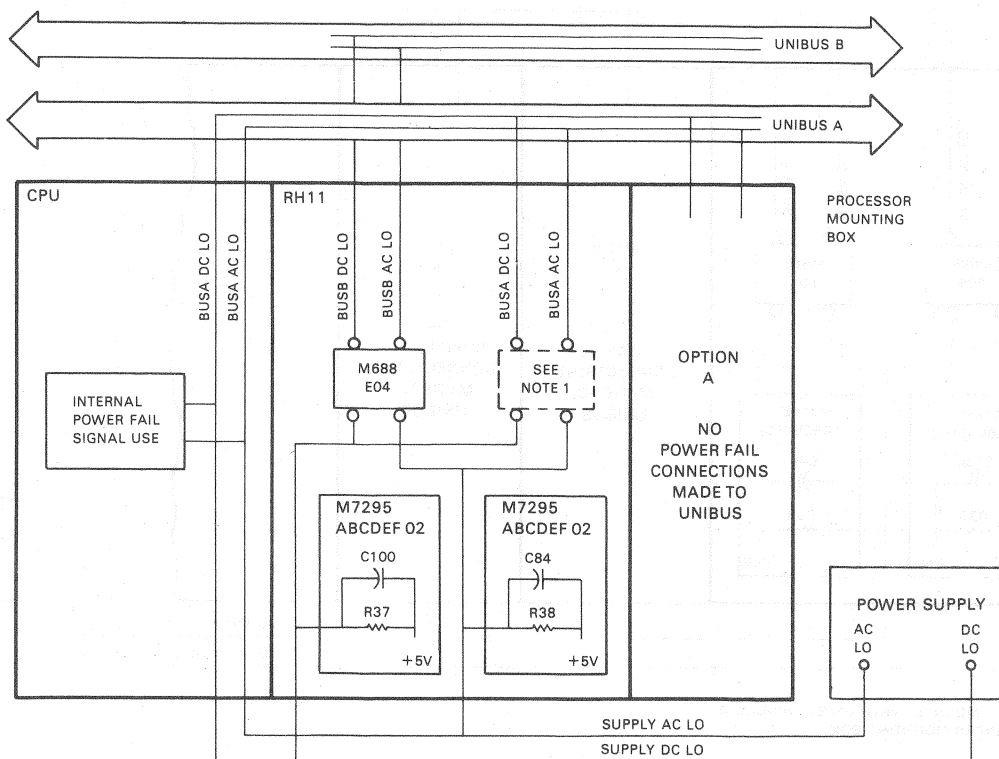
11-2218

Figure 2-16 Typical Power Fail Configuration for RH11 and Options Mounted in Same Expander Box



11 2216

Figure 2-17 Typical Power Fail Configuration for Two RH11s Mounted in Same Expander Box



11-2217

Figure 2-18 Typical Power Fail Configuration for RH11 and CPU Mounted in Processor Box

2.4.3 Jumper Configurations

The following paragraphs describe the various jumper configurations on the BCT (M7295), DBC (M7294), and CSR (M7296) modules. The different configurations for RM02 only and for an RM02/RPxx mix are listed separately within each module subsection.

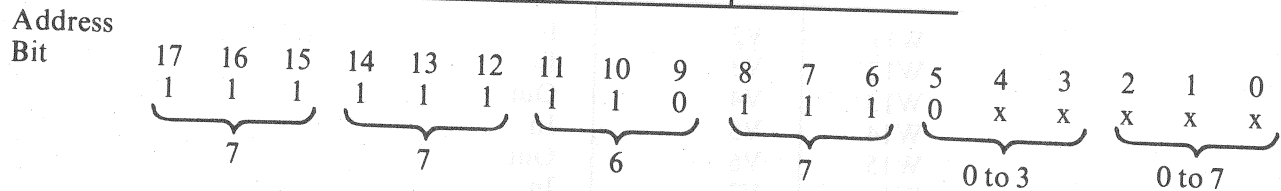
2.4.3.1 BCT Module (M7295) – The BCT module contains jumpers for register selection, BR level interrupt, NPR latency, vector address, and missed transfer error.

Register Selection – The RH11 is capable of responding to 30 possible Unibus addresses. The number of address, however, is dependent on the Massbus device. Jumpers W1–W8 select the block of Unibus addresses to which the RH11/RM02 subsystem responds. The standard block is assigned addresses 77670 through 776746. Table 2-2 shows the addressing scheme.

Table 2-2 RH11/RM02 Register Address Jumper Configurations

Jumper In = Binary 0

Address Bit	Jumper	Jumper In/ Jumper Out
12	W14	Out
11	W10	Out
10	W9	Out
9	W8	In
8	W11	Out
7	W13	Out
6	W15	Out
5	W12	In



The jumpers in E3 (D-CS-M7295-0-1, sheet 2) are used to select the appropriate number of registers for the device. The scheme is to select two less than the appropriate number for the drive. Only the RM02 subsystems have 22 registers; therefore, select a jumper configuration of 20 (shown in Table 2-3). The RM02/RPxx mix of drives have 32 registers and require a jumper configuration of 30 (as in Table 2-4).

BR Level Interrupt – The priority jumper plug for the RH11 is normally set for the BR5 level. This plug is located in E57 (D-CS-M7295-0-1, sheet 7).

NRP Latency – Special circuitry is incorporated on the BCT module to improve NPR latency time for devices connected to the Unibus. This circuitry is enabled via jumper W18 (D-CS-M7295-0-1, sheet 7). When the jumper is left in, the NPR latency feature is enabled. Not all PDP-11 processors work with this special feature.

Table 2-3 RH11/RM02 Jumper Configurations

Slot	Jumper	Jumper In/ Jumper Out
E3	1-16	Out
	2-15	Out
	3-14	In
	4-13	In
	5-12 (2)	Out
	6-11 (4)	Out
	7-10 (8)	In
	8-9 (16)	Out

Table 2-4 RH11/RM02/RPxx Mix Jumper Configurations

Slot	Jumper	Jumper In/ Jumper Out
E3	1-16	Out
	2-15	Out
	3-14	In
	4-13	In
	5-12 (2)	Out
	6-11 (4)	Out
	7-10 (8)	Out
	8-9 (16)	Out

Bus Grant – If there are no small peripheral controllers installed in slots C7–F7, C8–F8, and C9–F9, then G727 grant continuity modules must be installed in slot D7, D8, or D9. These modules merely continue the Bus Grant signals to the next device on the Unibus.

Vector Address Jumpers – The interrupt vector transferred to the processor is jumper-selectable via jumpers W11–W17, representing vector bits 2-8, respectively. The RM02 subsystems are assigned a vector address of 000254, with the jumper configuration shown in Table 2-5.

Table 2-5 Interrupt Vector Jumper Configurations

Jumper	Vector Bits	Jumper In/ Jumper Out*
W11	V2	In
W12	V3	In
W13	V4	Out
W14	V5	In
W15	V6	Out
W16	V7	In
W17	V8	Out

*Jumper In = Binary 1.

MXF Jumper – Jumper W19 (D-CD-M7295-0-1, sheet 9) is used to disable detection of MXF errors and is used during special maintenance procedures. W19 is normally left in.

2.4.3.2 DBC Module (M7294) – The DBC module contains jumpers for NPR cycle selection, Unibus parity, and start counter capacities.

NPR Cycle Selection Jumpers – Two jumpers select the type of cycle to be implemented when performing NPRs. Jumper E66 (3–4) (D-CS-M7294-0-1, sheet 2) selects the RH11 to perform one memory reference for each NPR request; this jumper is removed in the RM02 subsystem to allow back-to-back memory cycles to occur. Jumper E66 (2–15) takes advantage of dedicated Unibus B systems (those in which the RH11 is used exclusively as a Unibus B master) by allowing the RH11 to transfer complete consecutive blocks of data without giving up the Unibus; to implement this feature, both this jumper and E66 (3–14) must be cut (BUS HOG mode).

Unibus Parity Jumpers – The RH11 option can be selected for 16-data-bit transfers (plus 2 parity bits) or 18-data-bit transfers. Unibus A and Unibus B can each be selected individually via jumpers W1 and W2 (D-CS-M7294-0-1, sheet 8). If left in, jumper W1 allows parity error code detection on Unibus A when the RH11 is performing DATI operations; if W1 is removed, the PA and PB parity lines of Unibus B are used as data bits 16 and 17, respectively. Jumper W2 serves Unibus B in the same manner as W1 serves Unibus A. Both jumpers are normally left in.

Start Counter Jumpers – Various Silo capacities are jumper-selectable before a write operation onto the disk drive is started. The jumper selections are listed below (D-CS-M7294-0-1, sheet 9).

Jumper E66, Pins 1-16	Selects full capacity of 64 words
Jumper E66, Pins 5-12	Selects 32 words
Jumper E66, Pins 7-10	Selects 16 words
No Jumper	Selects 1 word

NOTE

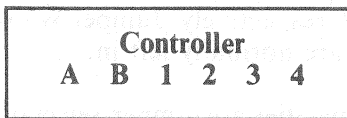
Only the jumper representing the desired Silo capacity should be connected. The other jumpers should be removed. For RM02 subsystems, the 64-word jumper E66, pins 1-16) should be connected.

2.4.3.3 CSR Module (M7296) –The CSR module contains a jumper (W1 on D-CS-M7296-0-1, sheet 2) to allow for Unibus A selection only. This jumper overrides the ability of the program to select Unibus B data transfers. The jumper is normally removed.

2.4.3.4 RH11 Installation Checklist

1. Visually check the RH11 backplane assembly for bent pins by sighting along the rows of pins from two directions. Also check for pinched or broken wires.
2. Check the backplane for the current wire-wrap revision and remove and check all RH11 modules for current ECO revisions.
3. Mount for RH11 backplane assembly in the appropriate mounting box using four 8/32-inch × 1-inch Allen-head screws.
4. Connect the two power harnesses to the RH11. Ensure that Mate-N-Lok connectors are seated firmly in the power distribution panel located on the chassis above the backplane.
5. Check the RH11 backplane again for bent pins and shorted wires.
6. Power-up the CPU or expander box and check all voltages, then power-down.
7. Check that the wires supplying AC LO and DC LO signals from the power supply are connected to the RH11.
8. Verify and/or select the jumper configurations in the RH11.
9. Verify that all modules are placed according to the RH11 module utilization list (D-MU-RH11-0-1).
10. Verify that Unibus cable connections are made.
11. Mount an input/output connector block assembly (7009861) to a connector panel (7412379) with four 4/40-inch × 5-inch screws (9008042-8).

12. Verify that two pressure-sensitive labels are applied to the connector panel for each input/output connector block assembly (E-UA-RM02-A-0). Label 1 is applied above the input/output connector block assembly, and Label 2 is applied below it.



Label 1

The second line of Label 1 must be marked so that only one letter and one number are visible. The single controller (RH11) used in an RM02-AA or -AB subsystem, as well as the first controller used in an RM02-BA or -BB subsystem, is referred to as controller A. If it is the first subsystem using the connector panel, it is designated controller A1 (etc., up to controller A4). The second controller in an RM02-BA or -BB subsystem is designated as controller BX, where X is the same subsystem number as the associated controller A.

Example: Two RH11 controllers are mounted in the same cabinet, one for each of two RM02-AA subsystems. Each RH11 uses one input/output connector block on the connector panel; the first is called controller A1, the second is A2. Later, an RM02-BA subsystem is installed with its two RH11 controllers mounted in the same cabinet. The remaining two slots on the connector panel are used, with one being labeled A3 and the other B3.



Label 2

This label simply shows the relative positions of the flat Massbus cables A, B, and C.

13. Mount the connector panel at the bottom rear of the cabinet containing the RH11, using four 10/32-inch Tinnerman nuts (Part No. 9006586) and four 10/32-inch $\times$ 0.38-inch Truss-head screws (Part No. 9006071-3). (Refer to D-UA-RM02-A-0).
14. Clean the air filters at the top of the mounting cabinet, if necessary.
15. Check mounting cabinet fans for proper operation.

2.5 RH70 CONTROLLER INSTALLATION PROCEDURE (RWM03)

The following paragraphs describe the mechanical and electrical installation, power checks, jumper configurations, and visual inspection for the RH70 controller for RM03 and RM03/RPxx applications.

2.5.1 Mechanical

The RH70 uses one hex-height module, three quad-height modules, and three double-height modules (Massbus connectors). There is no mechanical unit to mount. The modules are merely inserted into the appropriate slots in the PDP-11/70 CPU box, as shown in the module utilization chart in Figure 2-19. The Massbus cables are plugged into the double-height slots and jumpers are configured for the proper address and interrupt vector.

2.5.2 Electrical

The PDP-11/70 CPU mounting box contains a wired backplane that runs the full depth of the box. The Unibus signals are prewired on the backplane. Power to the RH70 is provided by the cabinet power supply as follows.

+5 V @ 18.5 A max

-15 V @ 0.5 A max

2.5.3 Module Locations

The PDP-11/70 CPU mounting box houses the floating-point unit, central processor, memory management, Unibus map, cache, five small peripheral controller (SPC) slots, the KW11-L clock, and up to four RH70 controllers. The location of the respective modules is shown in Figure 2-19.

2.5.4 Massbus Cables

Massbus connections to the RH70 are made via three 40-conductor ribbon cables. These cables plug into three M5904 transceivers in the RH70 and are designated Massbus cable A, Massbus cable B, and Massbus cable C. The connections are made to the RH70 as shown in Figure 2-20 and Table 2-6.

Table 2-6 Massbus Cable System Configurations

	Controller A	Controller B	Controller C	Controller D
Massbus Cable A	AB 25	AB 29	AB 33	AB 37
Massbus Cable B	AB 26	AB 30	AB 34	AB 38
Massbus Cable C	AB 27	AB 31	AB 35	AB 39

The Massbus cables are marked and should be inserted with the edge-marking facing the module handles. A Massbus terminator pack assembly (7009938) should be plugged into the last drive attached to the Massbus.

2.5.5 BCT and MDP Jumper Configurations

The following paragraphs describe the various jumper configurations on the BCT (M8153) module and on the MDP (M8150) modules for both RM03 and RM03/RPxx applications.

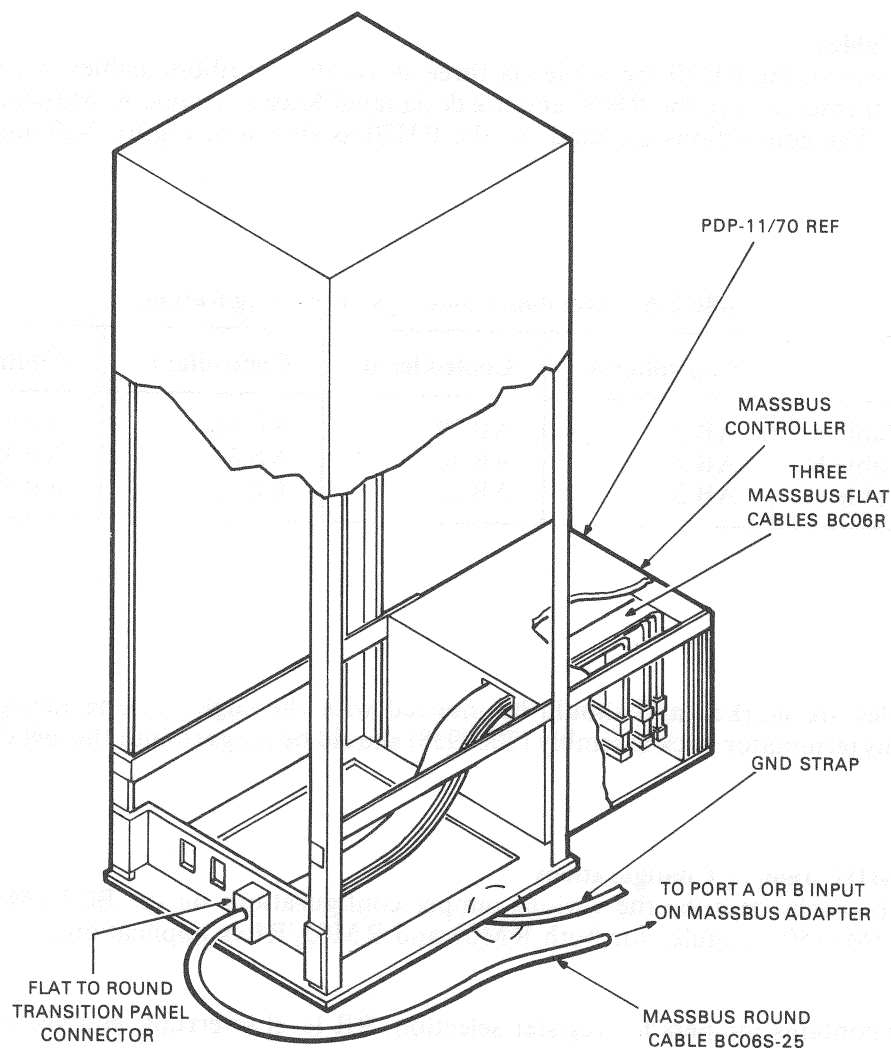
The BCT module contains jumpers for register selection, BR level interrupt, and vector address.

2.5.5.1 Register Selection – The RH70 is capable of responding to 32 possible Unibus addresses. The number of addresses, however, is dependent on the Massbus device. Jumpers W8–W15 select the block of Unibus addresses that both subsystems respond to. The standard addressing block assigned is 776700–776752. For both subsystems, the jumper configuration shown in Table 2-7 should be used.

The jumpers in E41 (D-CS-M8153-0-1, sheet 2 of 6) are selected for the appropriate number of registers in the subsystem, minus 2. For example, there are 22 registers in the RM03 and RM03/RPxx subsystems, so the jumpers are selected for a weighted value of 22-2 or 20, as shown in Table 2-8.

2.5.5.2 BR Level Interrupt – The priority jumper plug for the RH70 is normally set for the BR5 level. This plug is located in E022 (D-CS-M8153-0-1, sheet 4 of 6).

2.5.5.3 Vector Address Jumpers – The interrupt vector transferred to the processor is jumper-selectable via jumpers W1-W7, representing vector bits 2-8.



MA-0599

Figure 2-20 RH70 Massbus Cable Connections

Table 2-7 RH70 Register Address Jumper Configurations

Jumper In = Binary 0

Address Bit	Jumper	Jumper In/ Jumper Out
12	W14	Out
11	W10	Out
10	W9	Out
9	W8	In
8	W11	Out
7	W13	Out
6	W15	Out
5	W12	In

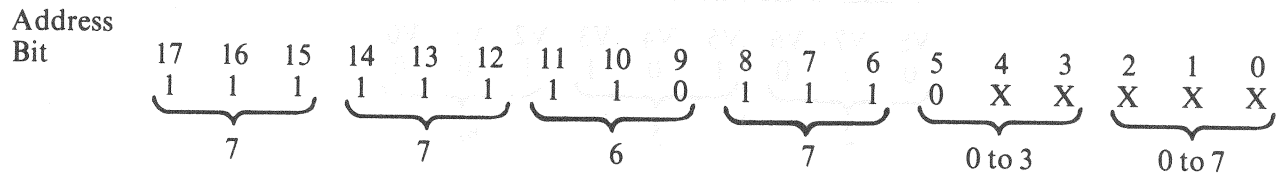


Table 2-8 RH70 Register Select Jumper Configurations

Jumper In = Binary 0

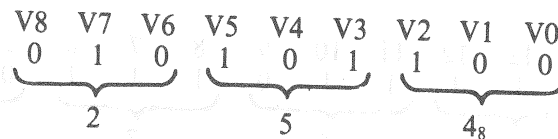
Slot	Jumper Location Pins	Jumper In/ Jumper Out
E41	1-16	Out
	2-15	Out
	3-14	In
	4-13	In
	5-12 (2)	In
	6-11 (4)	Out
	7-10 (8)	In
	8-9 (16)	Out

The RM03 subsystem has been assigned a vector address of 000254. The jumper configuration for this vector address is shown in Table 2-9.

Table 2-9 RH70 Vector Address Jumper Configuration

Jumper In = Binary 1

Vector Bit	Jumper	Jumper In/ Jumper Out
V2	W7	In
V3	W3	In
V4	W6	Out
V5	W2	In
V6	W5	Out
V7	W1	In
V8	W4	Out



2.5.5.4 Maintenance Jumpers MDP Module (M8150) – The MDP module contains jumpers that allow maintenance personnel to disconnect wired-OR connections from the Exclusive-OR network used to detect write-check errors. These jumpers are designated W1–W4 and are shown on D-CS-M8150-0-1, sheet 6 of 9. The jumpers provide maintenance personnel with a method of isolating a faulty output (stuck low) of the wired-AR bus to one of four integrated circuit (IC) chips that perform the Exclusive-OR function during write-check operations. For example, if the output of the E21 and E23 open-collector line is stuck low, when scoping of the inputs indicate that it should be high, the faulty IC (E21 or E23) can be ascertained by removing jumpers W2 and W1. If, after removing the jumpers, the outputs of the Exclusive-OR gates in E23 are still low, it indicates that the E23 chip is defective. If E23 outputs are high, the E21 chip is defective (outputs stuck low).

2.5.5.5 Light-Emitting Diodes (LEDs) – The following light-emitting diodes are incorporated into the RH70 Massbus controller logic BCT module (Figure 2-21) on the M8153.

- SSYN (Slave Sync) D-CS-M8153-0-1, sheet 3 of 6
- TRA (Transfer) D-CS-M8153-0-1, sheet 3 of 6
- BG IN (Bus Grant In) D-CS-M8153-0-1, sheet 4 of 6
- SACK (Selection Acknowledged) D-CS-M8153-0-1, sheet 4 of 6
- BBSY (Bus Busy) D-CS-M8153-0-1, sheet 4 of 6

These LEDs aid maintenance personnel in isolating certain system faults, as described in the following paragraphs.

System Fault No. 1 – The Unibus on the PDP-11/70 is in the “hung” condition (no operations can be performed on Unibus).

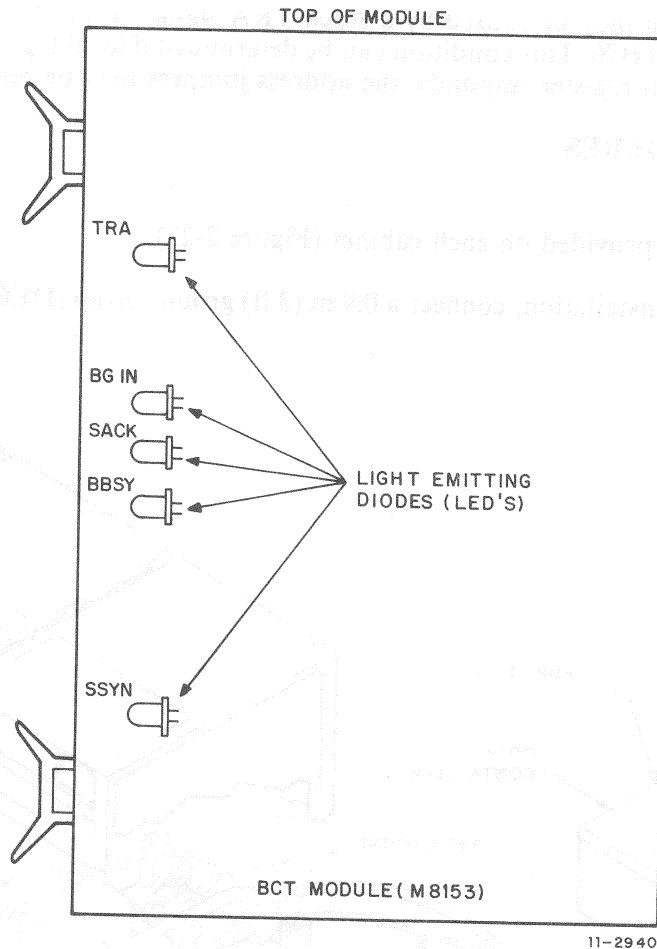


Figure 2-21 LED Physical Locations

Diagnosis – This condition may be caused by:

1. Stuck SACK
2. Stuck BBSY
3. Stuck SSYN.

The LED associated with the fault condition will be illuminated continuously. (LEDs may flicker intermittently during normal operation.)

System Fault No. 2 – The Unibus device interrupt sequence is not functioning properly. (The processor continuously loops in service routine and fails to execute instructions.)

Diagnosis – This condition is caused by discontinuity of the Bus Grant signal on the Unibus from the processor to the device interrupting, and may be caused by missing grant continuity cards or defective circuitry, which normally passes Grant signals from device to device. These will cause the BG IN LED to become illuminated, indicating that the Unibus BG IN signal coming to the device is stuck high.

System Fault No. 3 – The processor attempts to read or write a remote register in the RM03 subsystem and receives an address error indication on the console (CPU traps to location 4).

Diagnosis – This condition may be caused by a stuck TRA signal on the Massbus that prevents the SSYN response from the RH70. This condition can be determined if local registers in the RH70 can be successfully accessed. If no register responds, the address jumpers may be selected improperly.

2.6 CABLING PROCEDURES

2.6.1 Ground Cabling

Two grounding studs are provided on each cabinet (Figure 2-22).

If this is a multiple-drive installation, connect a 0.9 m (3 ft) ground strap (DEC part number 7412827) between each drive.

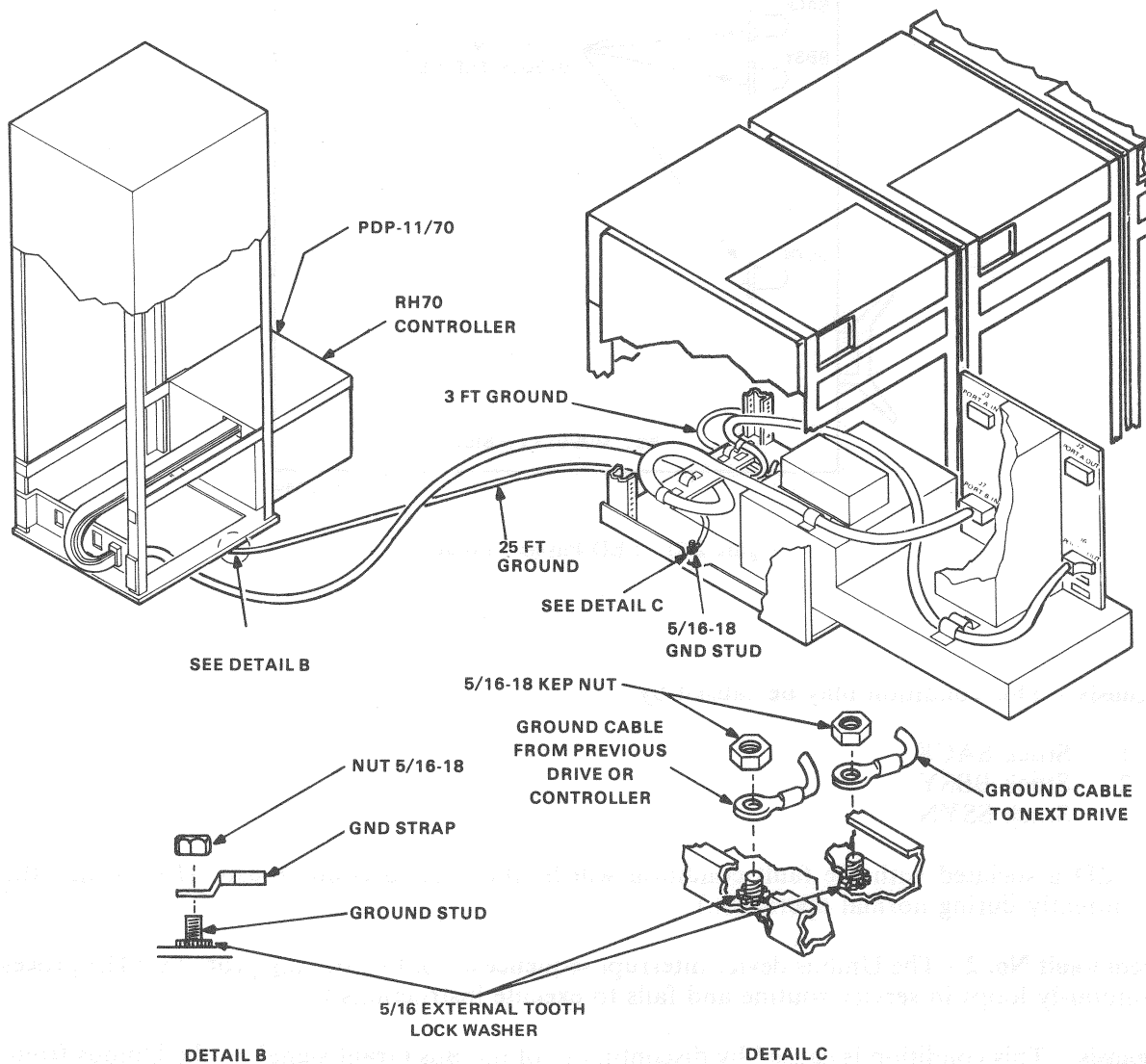


Figure 2-22 Grounding Studs and Cables

2.6.2 BC06S Cable Preparation

When the BC06S Massbus cable is shipped with the disk subsystem, all necessary changes to the cable will be made at the factory. The following information is provided for those instances where a BC06S cable is used that was not shipped with a system. In such instances, some preliminary cable changes may be needed.

The RM02/03 Massbus adapter requires that the BC06S cable exit from its connector at a 90 degree angle. This implies that whenever this cable is used from drive to drive, both connectors need to be at the 90 degree angle position. For the BC06S cable that goes to the RH controller, the connector at the controller end will be at a 45 degree angle and the one at the disk drive end at a 90 degree angle.

If it becomes necessary to change the BC06S cable angle from 45 degrees to 90 degrees in the field, use the following steps.

1. Remove the four screws from the connector as shown in Figure 2-23a.
2. Examine the cable gate as shown in Figure 2-23b. Be careful not to put undue stress on the wired connections. If the cable gate is at 0.38 inch, it should be moved forward so that only 0.25 inch of the cable sleeve remains exposed.
3. With the exposed cable sleeve now at the proper 0.25 inch length, adjust the cable angle to the 90 degree position as shown in Figure 2-23c.
4. Replace the four screws that hold the connector together.

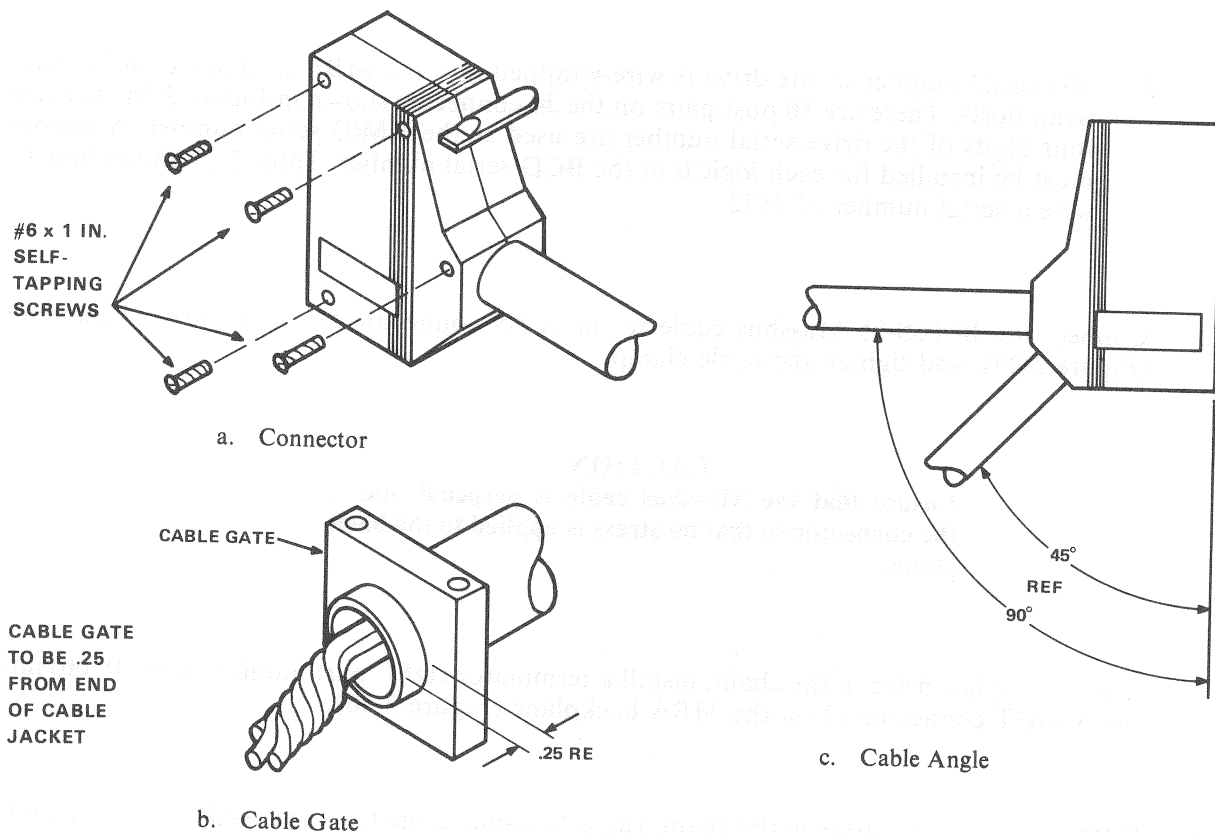


Figure 2-23 BC06S Cable Preparation

MA-1295

2.6.3 Single-Port Cabling Procedure

1. Prior to installing the cables for single-port operation, the following steps should be taken (Figure 2-24).
 - a. Either port A or port B may be used. The correct port transceiver modules must be in place for each mode of operation. Two M5922 modules are needed in the position shown in Figure 2-24 for port A operation. Port B operation requires that the two M5923 modules be in their correct position. The status of both types of port transceiver modules is given in Table 2-10 for each mode of operation. Each port transceiver module may be disabled independently by a switch on each board shown in Figure 2-24.
 - b. Verify that the desired jumpers are installed on the J1 connector on the MBA backplane. Table 2-11 shows how to select the correct jumper configuration.
 - c. Verify that the adapter PORT SELECT switches are in the correct position for the port used. The relationship between the PORT SELECT switch position and the SPRT JUMPER on the MBA J1 connector is shown in Table 2-12.
 - d. The serial number of the drive is wire-wrapped into the MBA backplane on 32 wire-wrap posts. There are 16 post pairs on the J4 connector shown in Figure 2-24. The last four digits of the drive serial number are used as the RM03 serial number. A jumper must be installed for each logic 0 in the BCD serial number. Table 2-13 shows how to wire a serial number of 3172.
2. Connect the BC06S-25 Massbus cable to the A-IN connector J3 on the MBA backplane (Figure 2-25), and tighten the cable clamp.

CAUTION

Ensure that the Massbus cable is perpendicular to the connector so that no stress is applied to the backplane.

3. If this is the last drive in the chain, install a terminator (DEC part number 7009938-00) into the A-OUT connector J2 on the MBA backplane (Figure 2-26).
4. If this is not the last drive in the chain, run a Massbus cable from the A-OUT connector J2 on the MBA backplane to the A-IN connector J3 of the next drive and tighten the appropriate cable clamp.

Table 2-10 Port Transceiver Module Status

Mode of Operation	Port Transceiver Module Status	
	M5922s	M5923s
Single port A	In place and enabled	Removed or in place and disabled
Single port B	Removed or in place and disabled	In place and enabled
Dual port	In place and enabled	In place and enabled

NOTE

Each module has its own disable switch located on its board.

Table 2-11 MBA Backplane J1 Connector

Jumper (J1)	In	Out
1-2	3600 rev/min	Other
3-4	80 MB	Other
5-6*	Single port A	Either port or dual port

*If jumper is in place, only port A can be used.

Table 2-12 Port Select Switch Positions

Front Cabinet Push Buttons (Newer Versions) A B		Adapter Backplane PORT SELECT (Old Versions)	Adapter Backplane J1 Connection SPRT Jumper	
			In	Out
IN	OUT	Port A	Single port A	Single port A
IN	IN	PROG (A/B)	Single port A	Dual port
OUT	OUT			
OUT	IN	Port B	Single port A	Single port B

Table 2-13 MBA Backplane Serial Numbers

Number Bit	Serial Jumper	Resulting BCD Serial Number
1	In	
2	Out	
4	In	2
8	In	
10	Out	+
20	Out	
40	Out	70
80	In	
100	Out	+
200	In	
400	In	100
800	In	
1000	Out	+
2000	Out	
4000	In	3000
8000	In	
		3172

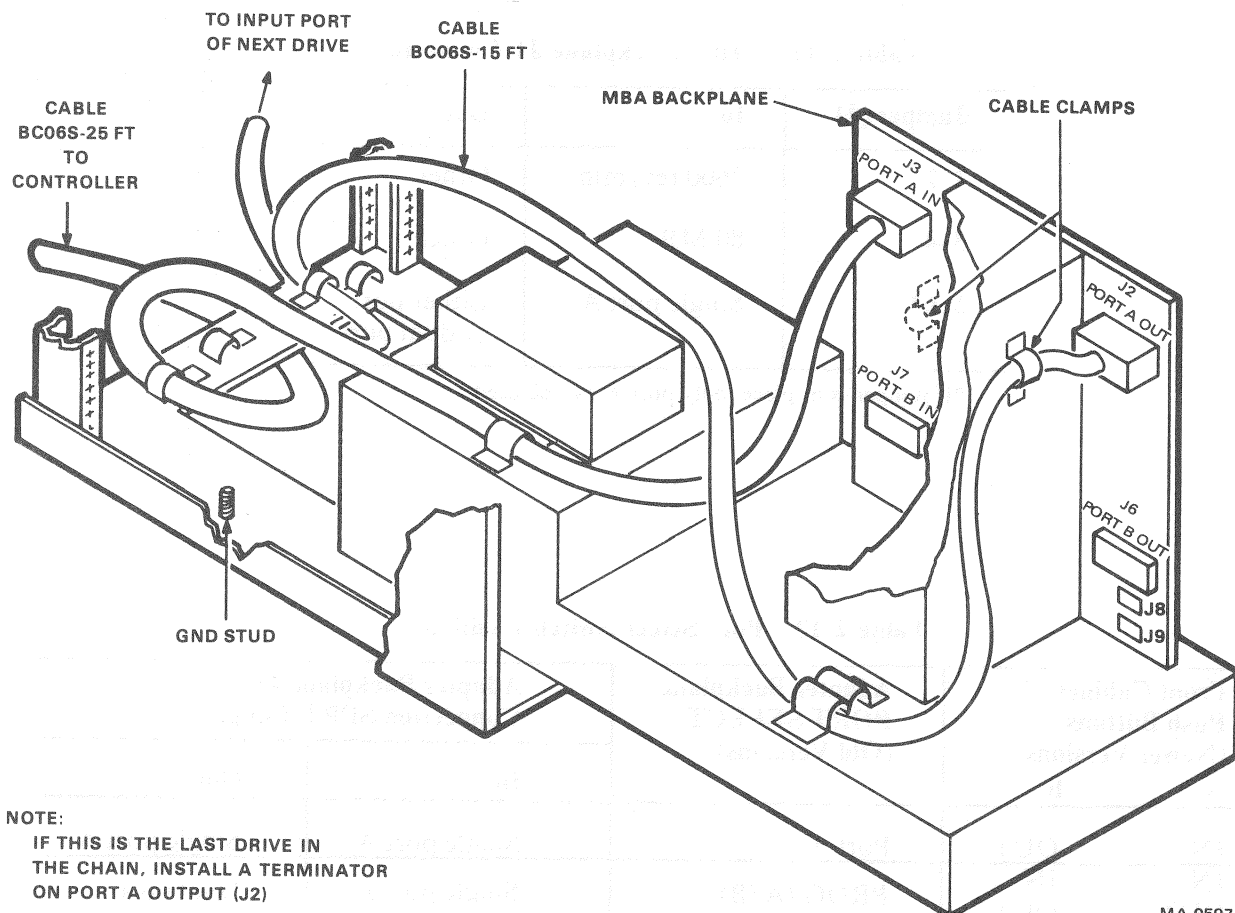
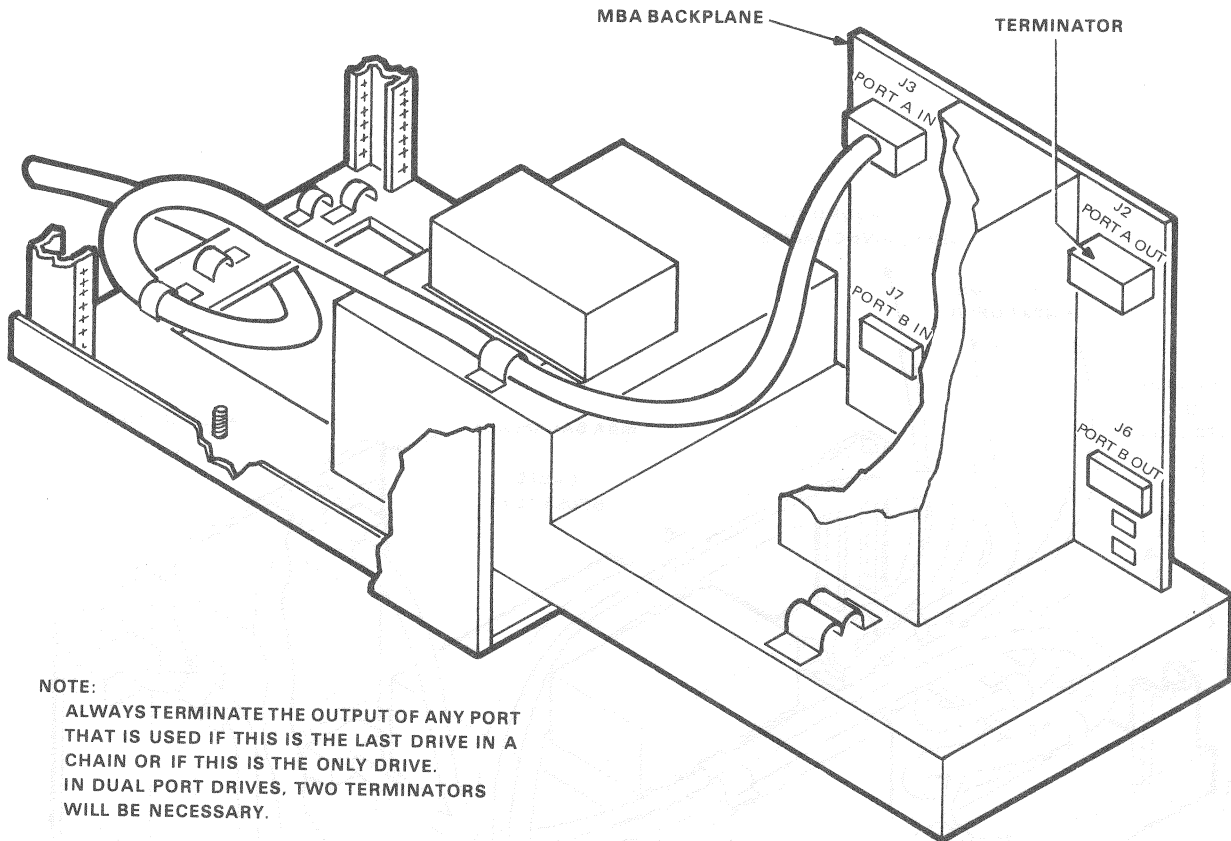


Figure 2-25 BC06S Massbus Cable Connection

MA-0597

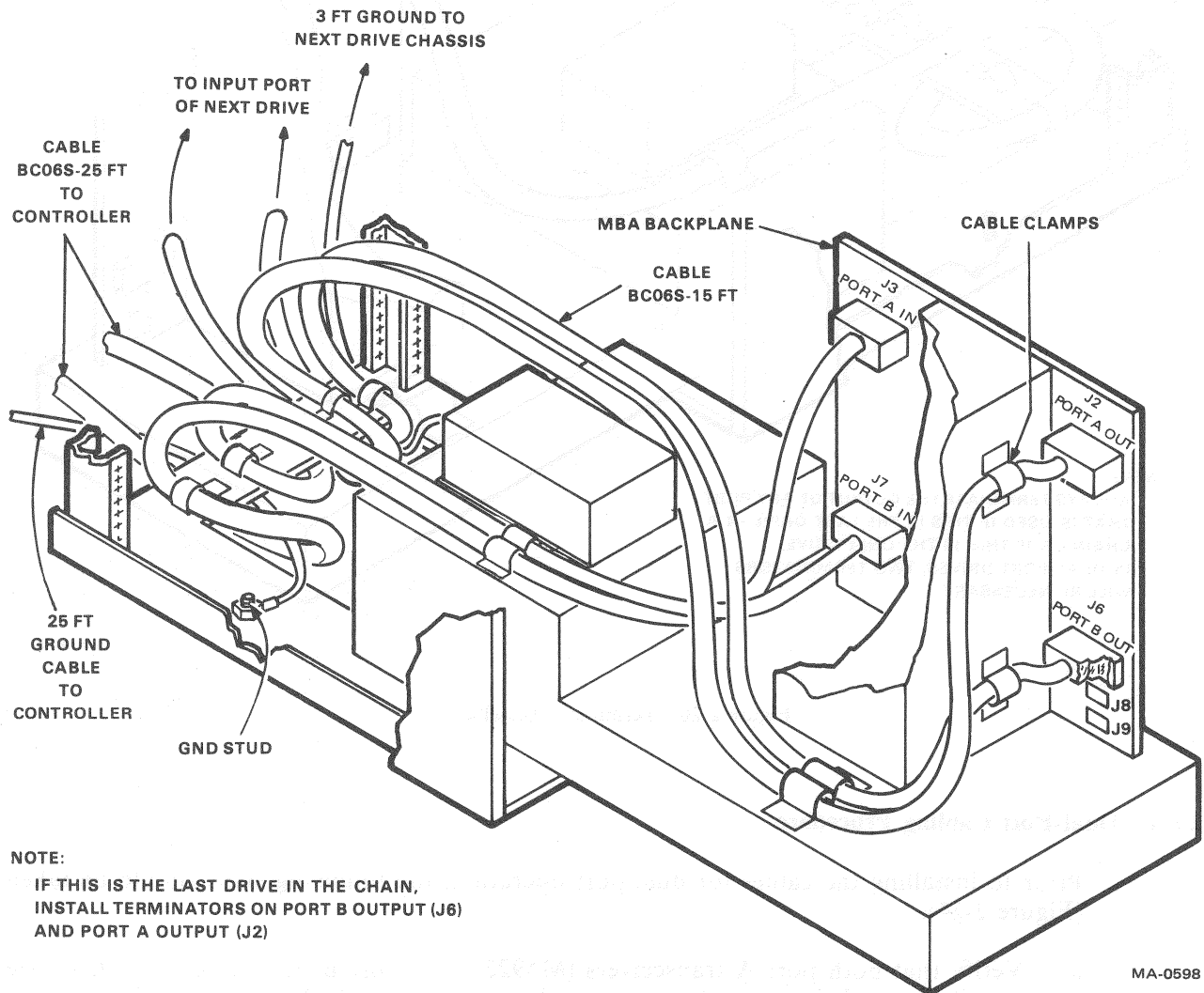


MA-0605

Figure 2-26 Terminator Installation

2.6.4 Dual-Port Cabling Procedure

1. Prior to installing the cables for dual-port operation, the following steps should be taken (Figure 2-24).
 - a. Verify that both port A transceivers (M5922s) and port B transceivers (M5923s) are installed into their proper locations as shown in Figure 2-24.
 - b. Verify that jumper S-6 on the J1 connector of the MBA backplane is left out and that the other two jumpers are in place.
 - c. The PORT SELECT switches should be set to dual-port mode. (Refer to Table 2-12.)
 - d. Verify that the transceiver switches are in the enabled position.
2. Install the Massbus cables for dual-port operation as shown in Figure 2-27.
3. The Massbus terminators must be installed on the output connectors (J2 and J6), of ports A and B whenever it is the only drive or the last drive in a string.

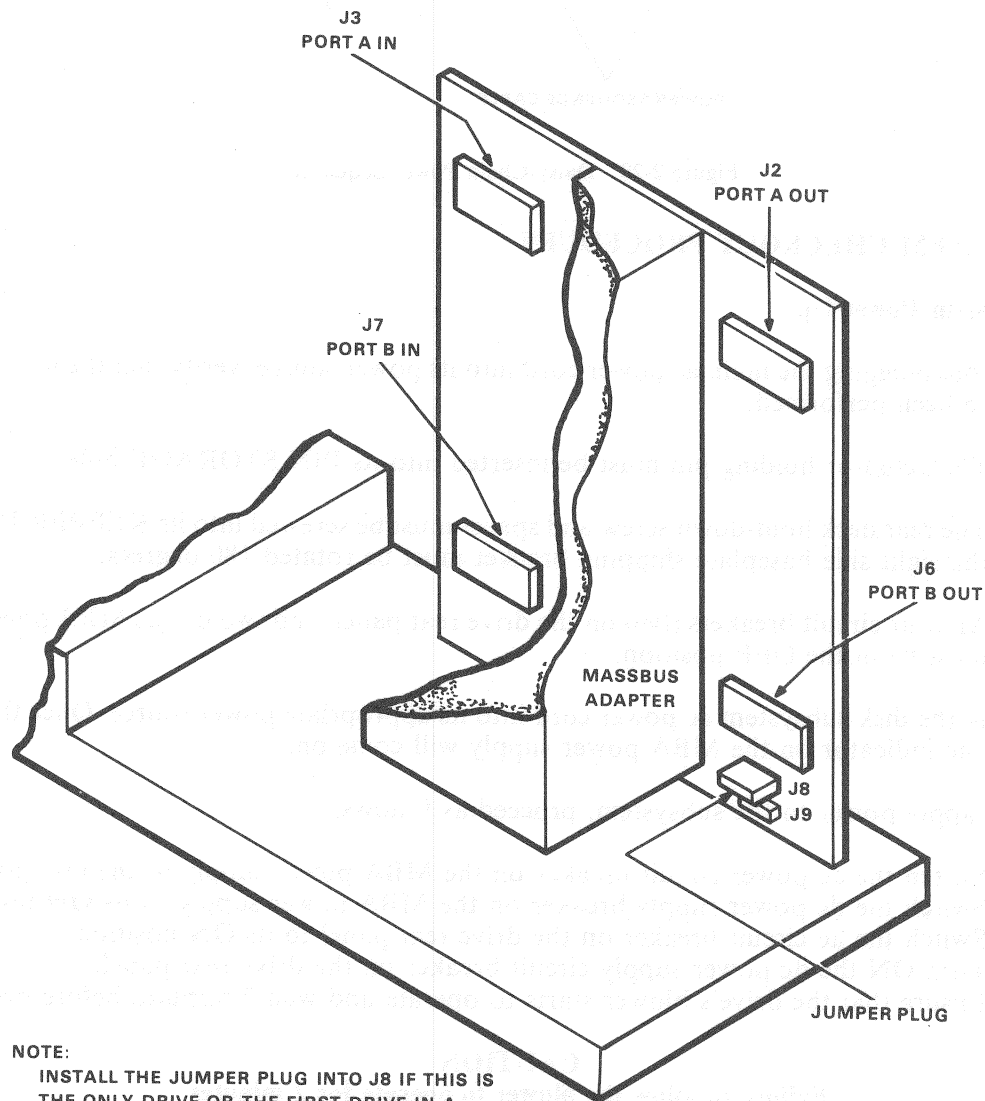


MA-0598

Figure 2-27 Dual Port Cabling

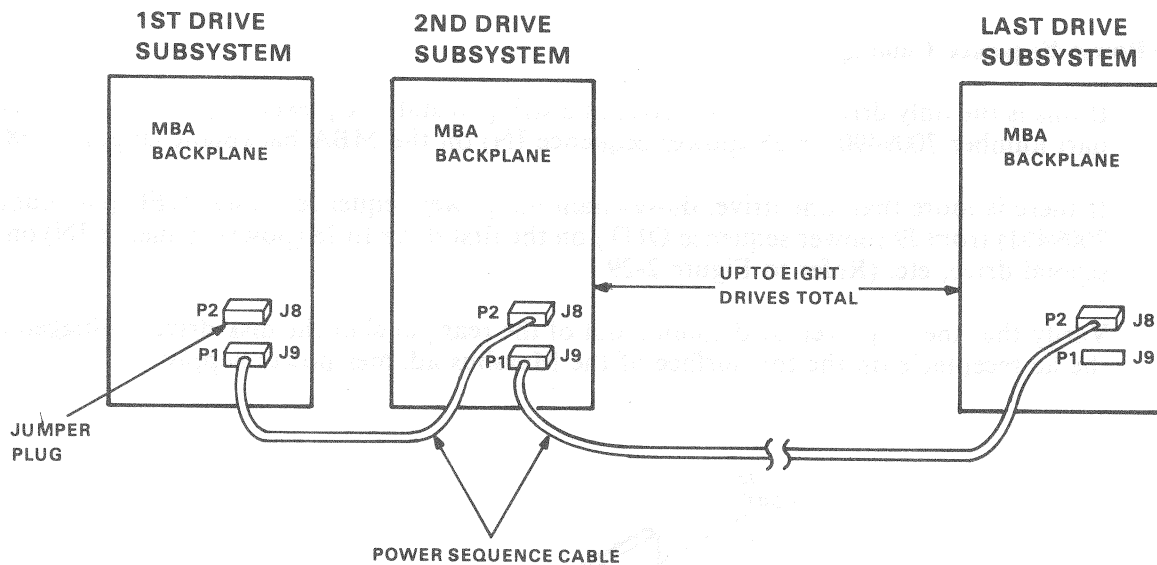
2.6.5 Power Sequence Cabling

1. If this is the only drive or the first drive in a string, install the power sequence jumper (DEC part number 7009490) in J8 (power sequence IN) on the MBA backplane (Figure 2-28).
2. If there is more than one drive, daisy-chain the power sequence cables (DEC part number 7009491) from J9 (power sequence OUT) on the first drive to J8 (power sequence IN) on the second drive, etc. (Refer to Figure 2-29.)
3. Verify that the ac power cord coming out of the rear panel of the disk drive is plugged into the ac receptacle on the top surface of the Massbus adapter power supply.



MA-0664

Figure 2-28 Power Sequence Jumper



MA-0608

Figure 2-29 Daisy-Chain Power Sequence

2.7 SUBSYSTEM CHECKOUT PROCEDURE

2.7.1 Subsystem Power Up

1. Before plugging the main ac power cord into its power source, verify that the following steps have been performed.
 - The actuator holding pin must be inserted into its PIN STORAGE hole.
 - The rear deck hold-down screw and spacer must be screwed into its KEEPER HOLE, and the right side baseplate shipping bracket must be rotated 180 degrees.
 - All four circuit breakers (two on the drive rear panel, and two on the MBA power supply) must be in the OFF position.
2. Plug the disk subsystem ac power cord into its appropriate power source. Once this is done, the ac indicator on the MBA power supply will come on.
3. To apply power to the subsystem, proceed as follows.
 - Switch the ac power circuit breaker on the MBA power supply to the ON position.
 - Switch the dc power supply breaker on the MBA power supply to its ON position.
 - Switch the ac circuit breaker on the drive rear panel to its ON position.
 - Turn ON the dc power supply circuit breaker on the drive rear panel.
 - Ensure that the drive's blower starts to operate and wait 2 minutes before proceeding.

CAUTION

Failure to allow the blower to operate for 2 minutes before installing the disk pack will not allow sufficient purge time and may cause damage to the disk pack or heads.

4. To install a disk pack and initiate a start-up sequence, follow the disk pack installation procedures described in Paragraph 3.2.2 of the Operating Instructions.

2.7.2 Installation of the Field Test Unit

2.7.2.1 General Description – The TB3A2 Field Test Unit (FTU) is a portable, self-contained tester for exercising and/or simulating on-line operations in the DEC I/O storage module drives (SMDs), series BK5.

The FTU is housed in a suitcase-type carrying case that provides a control panel, a logic board, and an integral power supply. The case contains space for storing the power cable, all necessary I/O cables, and a head alignment card. The head alignment card plugs into the logic chassis of the SMD and permits individual head alignment, using a null meter mounted in the FTU control panel.

Modes of Operation

The TB3A2 FTU provides five access (seek) modes, four read/write modes, and two modes for determining head selection.

NOTE

Performing any write operations will destroy formatting on the pack.

Access Modes

Direct Seek – The drive under test will perform a single seek to the track number set in the CYLINDER ADDRESS switches on the FTU control panel.

Continuous Seek – The drive under test will perform repetitive seeks between any two tracks selected by the operator. Operation will continue until the START/STOP switch on the FTU control panel is moved to STOP (STOP switch actuated).

Sequential Forward Seek – The drive under test will perform single-track incremental seeks until the last track is reached, then seek to track 00, and continue incremental seeks in the same manner until the STOP switch is actuated.

Sequential Reverse Seek – The drive under test will perform single-track decremental seeks, starting with the track nominated by the CYLINDER ADDRESS switches, until track 00 is reached. The drive will then return to the nominated track and repeat the operation until the STOP switch is actuated.

Random Seek – The drive under test will perform seeks to random tracks as selected by a free-running counter within the FTU. Operation will continue until the STOP switch is actuated.

Read/Write Modes

The TB3A2 FTU generates serial NRZ write data at a rate determined by the servo clock signals transmitted from the unit under test. When a repeatable access mode is selected (that is, any mode except direct mode), a read/write operation will be completed at the selected cylinder, after which a seek will be initiated to the next cylinder address (as determined by the access mode) and the read/write operation repeated. This seek-read/write sequencing will continue until the STOP switch is actuated or an error occurs. For direct seeks, the read/write R/W operation will continue at the selected track or cylinder (depending upon the head select mode) until the STOP switch is actuated.

The number of tracks read or written during each read/write operation is controlled by the mode of head selection chosen. For manual head selection, only the track under the head selected by the HEAD ADDRESS switches will be read or written. For sequential head selection, the heads will be sequenced so as to read or write each track in the cylinder. When the highest-numbered head (or cylinder track) has been exercised, the drive will seek to another cylinder (except in direct seek) and the read/write operation will be repeated at that new cylinder, starting with head 00.

Write Format – When the FTU WRT-RD SELECT switch is set to WRT FORMAT, the FTU will write each selected track with the appropriate track address and a repetitive 8-bit data pattern that has been set in the DATA PATTERN switches on the FTU control panel. The FTU also provides a means for indicating a defective track when using the write format mode.

Write – When the FTU WRT-RD SELECT switch is set to WRT, the FTU will write the repetitive 8-bit data pattern on the selected track, after having first read and verified the track address.

Read – When the FTU WRT-RD SELECT switch is set to RD, the FTU will read the data from the selected track, after having first read and verified the track address.

Write Then Read – When the FTU WRT-RD SELECT switch is set to WRT.RD, the FTU will verify the track address and write the 8-bit data pattern on the selected track during one revolution of the drive, then verify the track address, and read back the data during the second revolution.

A fifth position (OFF) of the WRT-RD SELECT switch is available for access only operations. This position is also used during the head alignment procedure.

2.7.2.2 Tester Installation

Operating Voltage

The FTU is connected at the factory for use with a 120 Vac 50/60 Hz power source. To reconnect for 240 Vac operation, proceed as follows.

1. Open the FTU cover. Unhinge the cover and set it aside if necessary.
2. Raise the control panel.
3. Remove head alignment card from its compartment on top of the power supply box.
4. Remove four screws securing the cover plate of the power supply; remove the cover plate.
5. Remove the jumper straps connecting terminals 1 and 2, and terminals 3 and 4 of A1TB1 (Figures 2-30 and 2-31).

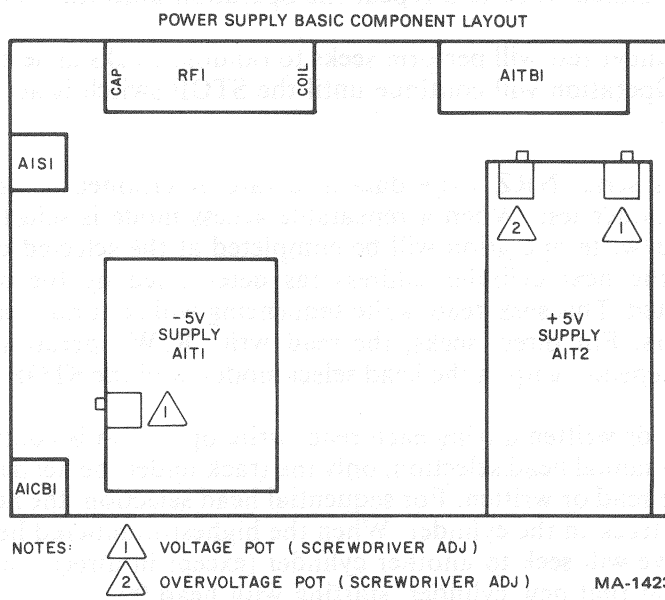
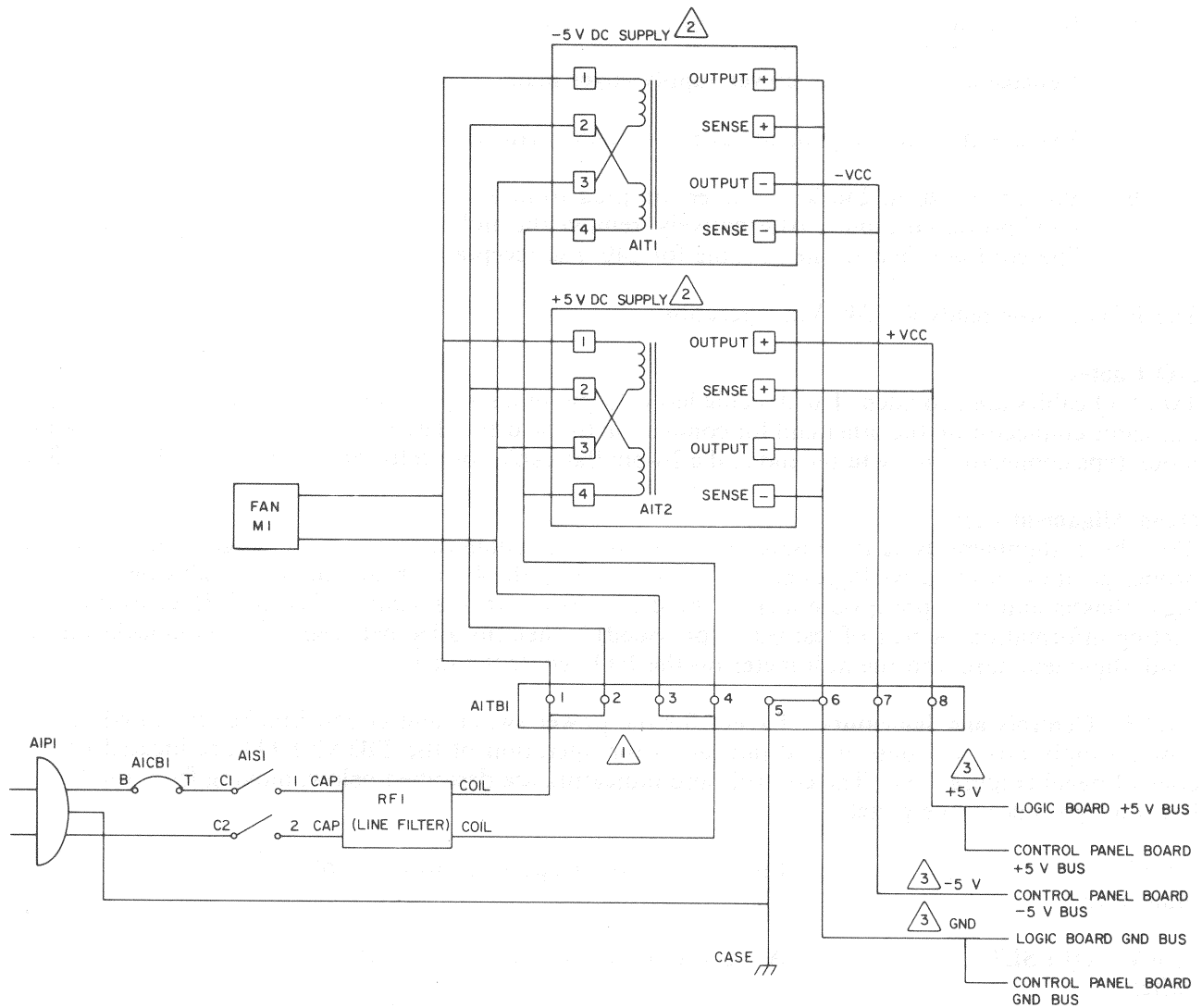


Figure 2-30 FTU Power Supply Layout

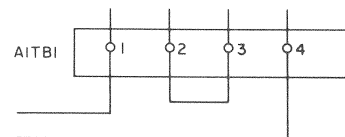


NOTES:



WIRING SHOWN FOR 110V OPERATION

FOR 220V OPERATION, JUMPER 1-2 AND 3-4 ARE REMOVED AND JUMPER 2-3 IS ADDED. THE RESULTANT IS SHOWN BELOW



THESE ARE REPLACED AS A UNIT AND THEREFORE INDIVIDUAL COMPONENTS (OTHER THAN TRANSFORMERS) ARE NOT SHOWN



REFER TO KEY TO LOGIC FOR +5 V, -5 V AND GND BUS CONNECTIONS

MA-1422

Figure 2-31 FTU Power Supply Wiring Diagram

6. Install both jumpers so as to connect terminals 2 and 3.
7. Replace and secure the power supply cover plate.
8. Replace the head alignment card in its compartment.
9. Procure a 120 to 240 Vac conversion plug from a local supply house and attach it to the FTU power cord plug. Alternatively, remove the molded 3-prong plug attached to the FTU line cord and install one suitable for 240 Vac receptacles.

The FTU is now ready for 240 Vac operation.

I/O Cables

Two I/O cables are provided. The A-cable has a 75-pin block-type connector on one end and a 60-pin flat-cable connector on the other end for connection to the drive. The B-cable is equipped with a 34-pin block-type connector on the tester end and a 26-pin flat-cable connector on the drive end (Figure 2-32).

Head Alignment Cable

SMD head alignment using the TB3A2 FTU requires installing the special head alignment card in the proper position of the drive logic chassis, and connecting the 4-wire head alignment cable between the logic chassis and the appropriate jack in the drive's read/write assembly. Figure 2-33 gives the connecting information. A pair of test leads (provided) is then installed between the banana jacks on the head alignment card and the null meter on the FTU control panel.

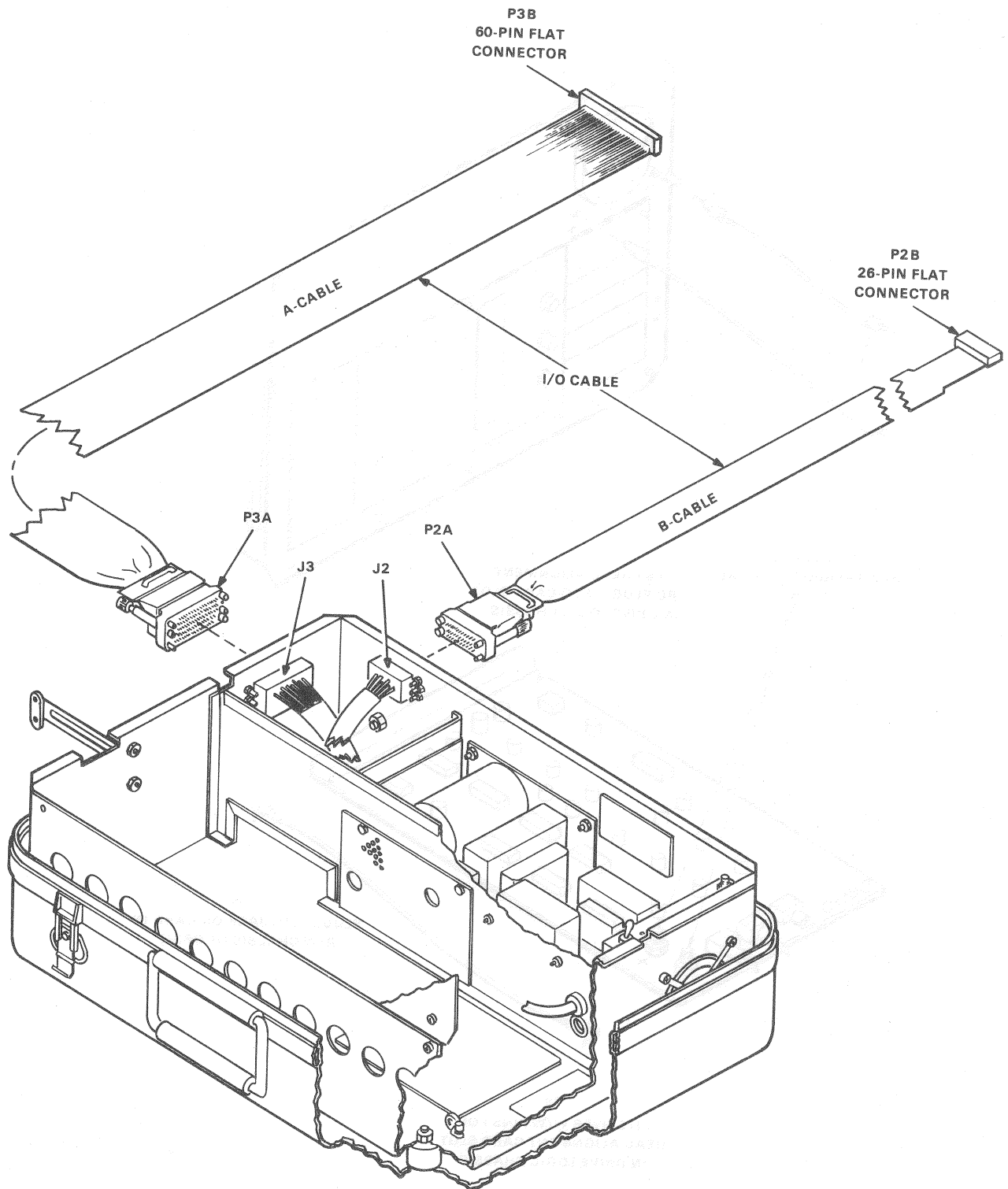
2.7.2.3 Controls and Indicators – Except for the power switch and circuit breaker mounted on the power supply box, all controls and indicators for operation of the TB3A2 FTU are located on the control panel (Figure 2-34). The controls and indicators are described below, moving from top left to bottom right across the panel.

+5 V, -5 V indicators	Indicate that the respective power supply voltages are present.	
SERVO OFFSET switch		A 3-position switch with center "off."
	+	Commands the drive to offset the carriage in the positive direction (toward the spindle).
	Center	Nominal positioning (no offset).
	-	Commands the drive to offset the carriage in the negative direction (away from the spindle).

NOTE

The START/STOP switch must be actuated to effect any change in offset by the drive when in direct mode.

DATA STROBE switch	A 3-position switch with center "off."	
	EARLY	Moves the drive's read strobes from nominal to an earlier time with respect to data.
	Center	Drive strobes at nominal timing.



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Figure 2-32 Tester I/O Cables

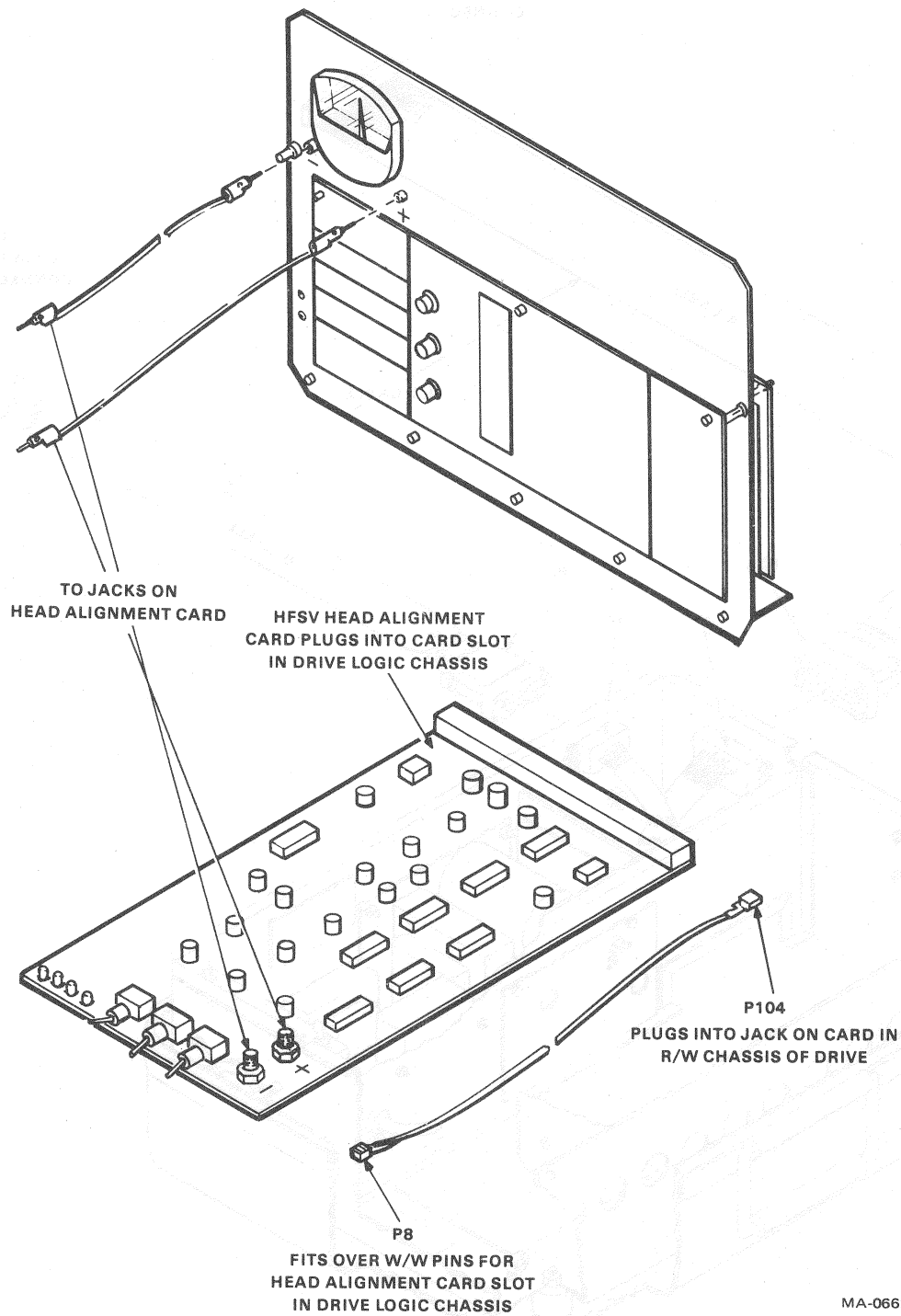
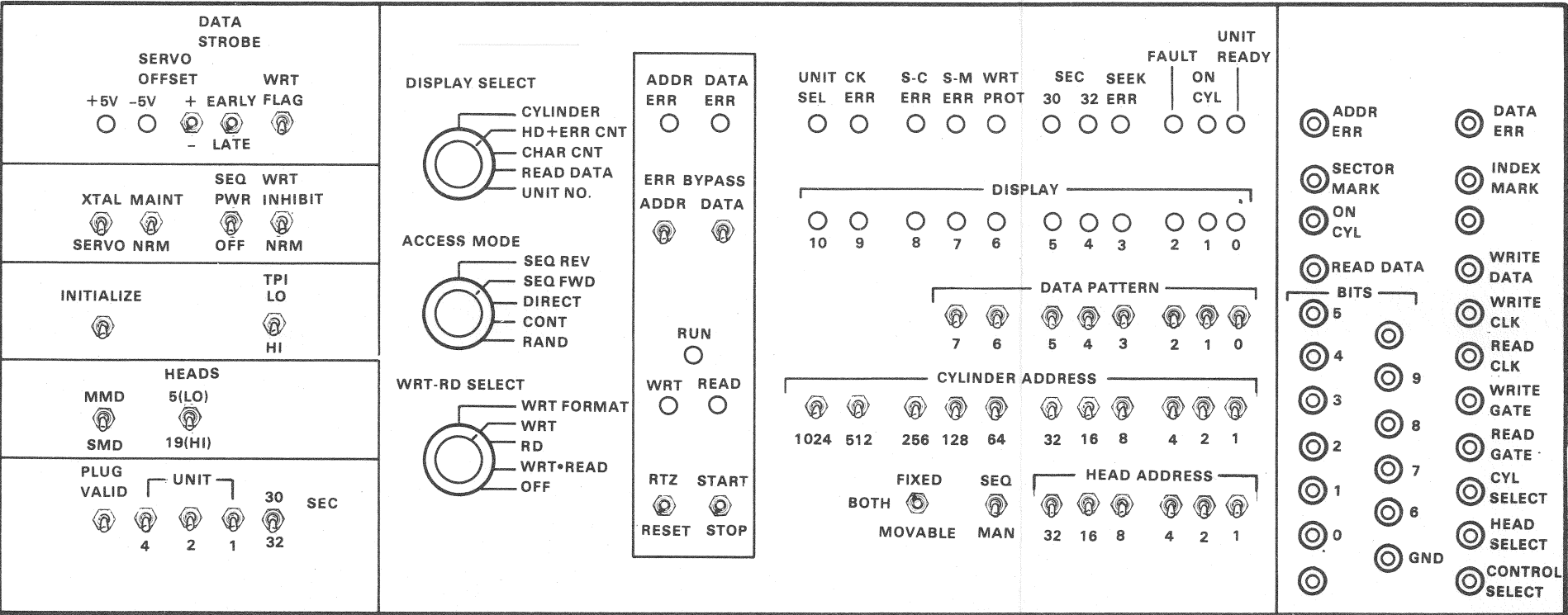


Figure 2-33 Head Alignment Connections



MA-0638

Figure 2-34 TB3A2 Control Panel

DATA STROBE switch (cont)	LATE	Moves the drive's read strobes from nominal to a later time with respect to data.
WRT FLAG switch		When moved up, this switch causes a Defective Track flag bit to be inserted in Bit 6 of Address Word 1, provided that: • WRT-RD SELECT switch is set to WRT FORMAT. • ACCESS MODE switch is set to DIRECT. • Head-select switch (SEQ-MAN) is set to MAN.
XTAL/SERVO switch	XTAL	A crystal oscillator within the FTU provides a nominal 9.667 MHz clock signal. Used for tester maintenance.
	SERVO	Servo Clock signals from the drive provide the basic timing for the FTU.
MAINT/NRM switch	MAINT	Used to perform maintenance on the FTU without a drive connected. Provides pseudo Ready and On Cylinder signals to simulate a drive response. It is also used during head alignments.
	NRM	Normal testing of a drive is done in this position.
SEQ PWR/OFF switch	SEQ PWR	In this position, the FTU commands the drive to power-up, provided that: • The drive is in the remote mode. • Primary power is available at the drive. • The drive's START switch is ON (indicator lighted).
	OFF	In this position, the FTU cannot power-up the drive.
WRT INHIBIT/NRM switch	WRT	Prevents writing by the drive.
	INHIBIT	Writing is inhibited even though all other FTU switches are set to perform a write operation.
	NRM	Allows a normal write operation in the drive, provided that other FTU switches are set to perform a write operation.
INITIALIZE		When moved to the "up" position, this momentary-contact switch provides an Initialized signal to the drive under test.
TPI switch		Not used; position irrelevant.
MMD/SMD switch		Not used; position irrelevant.

HEADS switch

Not used; position irrelevant.

PLUG VALID switch

With FTU's DISPLAY SELECT switch set to UNIT NO. so as to display the PLUG VALID indication, proceed as in Table 2-14.

Table 2-14 Plug Valid Indication

"0" Display Light (Plug Valid Indicator)	Meaning	To Select Drive
ON	Logical address plug is installed in drive.	1. Set PLUG VALID switch "up." 2. Set the three UNIT switches to desired drive number (0-7).
OFF	Logical address plug is not installed in drive.	1. Set PLUG VALID switch "down." 2. Set all three UNIT switches "down" to pseudo-select unit 0.

UNIT switches

421

Used to indicate the binary value of the three Select Address lines to the drive. This code must match that of the logical address plug in the drive under test.

SEC 30/32 switch

Selects the drive under test for either 30- or 32-sector operation.

ACCESS MODE switch

A 5-position rotary switch that controls the seek (access) mode of the drive under test.

SEQ REV

Sequential Reverse – The drive seeks to the address in the FTU CYLINDER ADDRESS switches, sequences down to 0, and then repeats.

SEQ FWD

Sequential Forward – The drive performs a series of incremental seeks, starting with the address that is in the cylinder address register (CAR) at the start of the operation. When maximum cylinder address is reached, the cycle begins again at address 0.

DIRECT

The drive seeks to the address in the CYLINDER ADDRESS switches. Seeking to another address requires changing the address in the switches and manually initiating another seek operation by actuating the START switch.

ACCESS MODE
switch (cont)

CONT

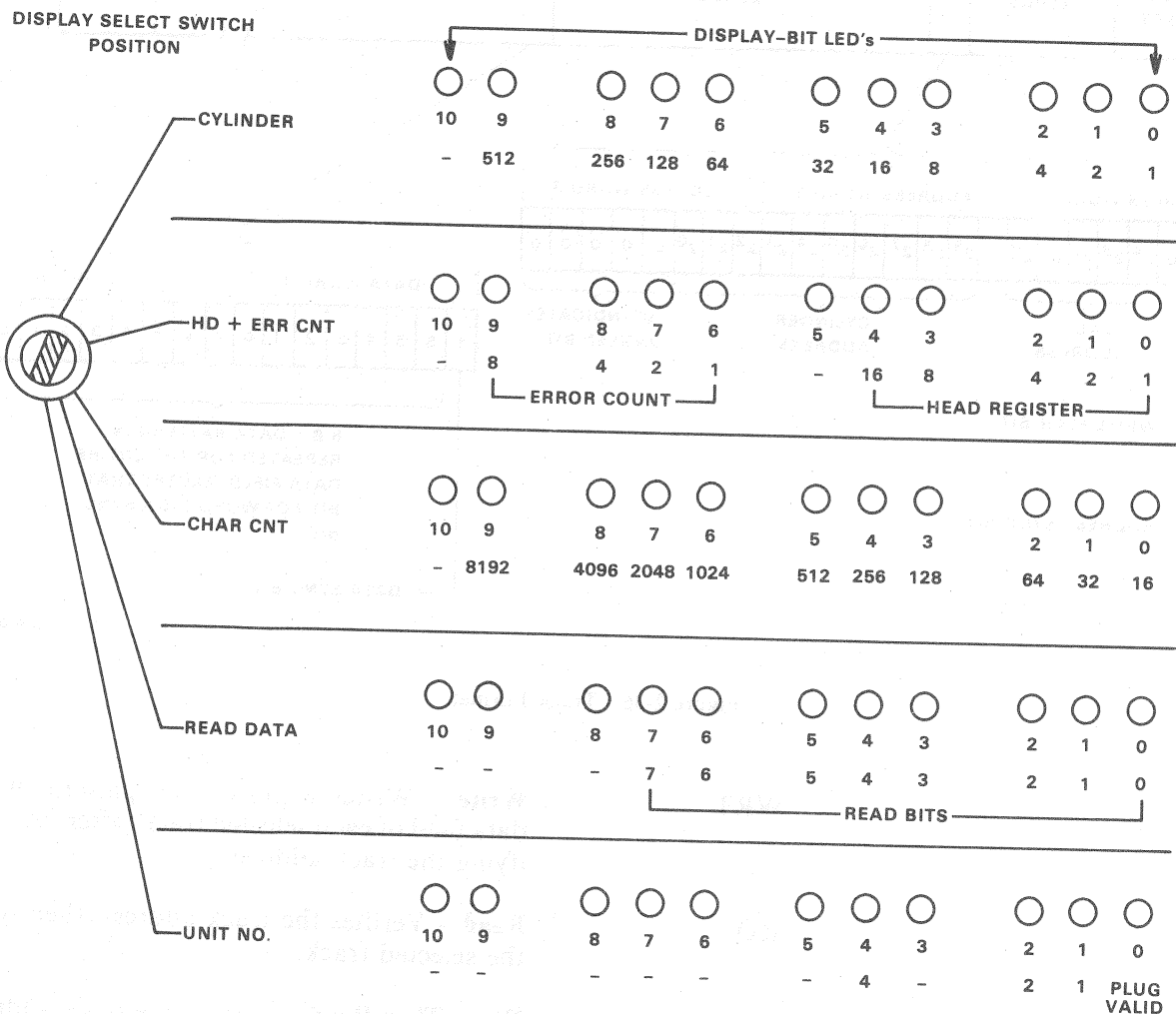
Continuous - The drive seeks alternately between the address in the CYLINDER ADDRESS switches and that in the cylinder address register. The contents of CAR does not change during this operation.

RAND

Random - The drive seeks to random addresses generated by increasing the count in the CAR during the time that the drive is not "on cylinder."

DISPLAY SELECT
switch

A 5-position rotary switch that controls the eleven DISPLAY lamps on the FTU control panel. The interpretation of the display is shown in Figure 2-35. When the switch is set on READ DATA, the cylinder address will be displayed as long as the FTU is running. The data pattern read will be displayed if the FTU has stopped because of a data error; otherwise the display will be 0s.



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Figure 2-35 Display Select Switch

WRT-RD SELECT switch

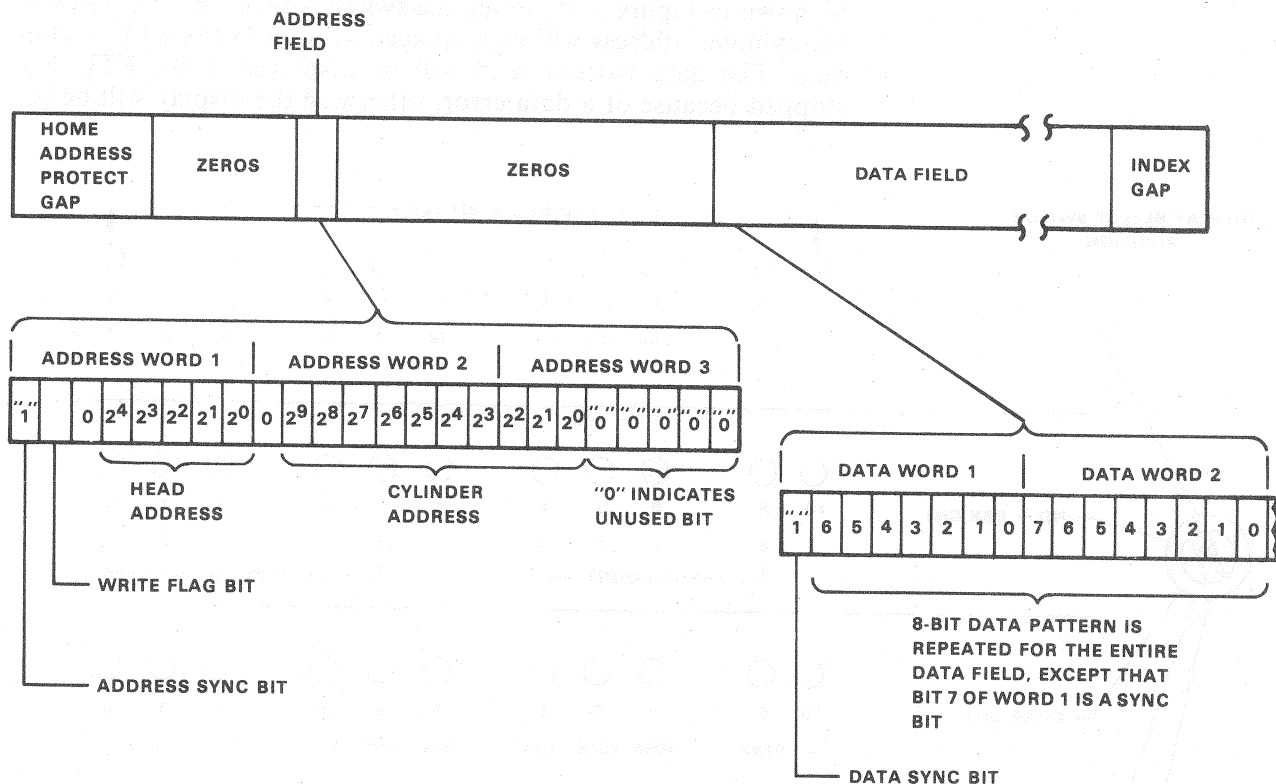
A 5-position rotary switch that determines the manner in which data will be exchanged between the FTU and the drive under test.

WRT FORMAT

Write Format – Writes the correct track address (HA and CA) and a preselected 8-bit data pattern field on each selected track. The format is as shown in Figure 2-36.

NOTE

This format is not the same as the standard **DIGITAL** format.



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Figure 2-36 Track Format

WRT

Write – Writes a preselected pattern in the data field of each selected track, after first verifying the track address.

RD

Read – Verifies the track address, then reads the selected track.

WRT.READ

Write Then Read – Verifies the track address, writes the data field on the selected track, then reads the track. (Operation requires two revolutions.)

WRT-RD SELECT switch (cont)	OFF	Disables all read/write functions; restricts the drive under test to seek operations only.
ADDR ERROR indicator		Indicates that the address information received from the drive differs from the address requested, or that the address sync bit was not received from the drive.
DATA ERROR indicator		Indicated that the 8-bit data pattern received from the drive differs from the pattern set in the DATA PATTERN switches.
ERROR BYPASS switches	ADDR	Address – If this switch is in the “up” position, it allows the FTU to continue operating when an address, S-C, or S-M error occurs. In the “down” position, an address error will stop the FTU.
	DATA	If this switch is in the “up” position, it allows the FTU to continue operating when a data error occurs. In the “down” position, a data error will stop the FTU.
RUN indicator		Indicates that the FTU is running or that the RTZ switch (Return-to-Zero) is being actuated. Five conditions will turn off the indicator. • Returning the RTZ switch to neutral (but provided that RUN was not lit before the RTZ operation) • A valid (unbypassed) error • Actuating the STOP switch • Actuating the RESET switch • If the Ready signal from the drive goes low
WRT indicator		Indicates that the FTU is writing.
RD indicator		Indicates that the FTU is reading.
RTZ/RESET switch		A 3-position momentary switch with center “off.”
	RTZ	Clears HAR and CAR; clears the drive’s fault register and causes the drive to perform a return-to-zero seek. The RUN light on the FTU control panel will be lit as long as this switch is actuated to the RTZ position.
	Center	Neutral position.
	RESET	Clears the error flip-flops in the FTU and the drive. This switch must be actuated after a valid error has occurred in order to be able to restart the FTU.

START/STOP switch	A 3-position momentary switch with center "off."
START	Generates a pulse that starts the FTU; turns on the RUN indicator. An existing error condition must be cleared by actuating the RESET switch before START will have any effect.
Center	Neutral position.
STOP	Stops the FTU; extinguishes the RUN indicator.
UNIT SEL indicator	Indicates that the unit number of the drive under test agrees with that set in the UNIT NO. switches on the FTU, and that the tester is receiving a Plug Valid signal from the drive.
CLK ERROR indicator	Indicates that a period of 200 ns has expired without a servo clock pulse from the drive under test.
S-C ERROR indicator	Indicates that the sector counter in the drive under test does not agree with the sector counter in the FTU.
S-M ERROR	Indicates that an incorrect number of sector marks was received from the drive under test between successive index marks.
WRT PROTECT indicator	Indicates the presence of a Write Protect signal from the drive under test.
SEC 30/32 indicator	Indicates whether the drive is in 30 or 32 sector mode.
SEEK ERROR indicator	Indicates the presence of a Seek Error signal from the drive under test.
FAULT indicator	Indicates the presence of a Fault signal from the drive under test.
ON CL indicator	Indicates the presence of an On Cylinder signal from the drive under test, or a pseudo On Cylinder signal generated by the FTU if in maintenance mode.
UNIT READY indicator	Indicates the presence of a Ready signal. This signal comes from the drive if the A and B I/O cables are connected between the drive and the FTU.
DISPLAY indicators	Refer to diagram shown for the DISPLAY SELECT switch (Figure 2-35).
DATA PATTERNS switches	These switches permit setting the repetitive 8-bit data pattern that is written in the data field of the selected track during a write operation. For read operations, the data read from the track is compared with these switches to check for the presence of a read error. A 1 is indicated when a switch is in the "up" position, a 0 when the switch is "down."

**CYLINDER ADDRESS
switches**

These switches enter the binary value of the cylinder address to which a seek is desired. Used in conjunction with the ACCESS MODE switch. A 1 is indicated when a switch is in the "up" position, a 0 when the switch is "down."

**FIXED/BOTH
MOVABLE switch**

Not used. Reserved for future use with MMDs.

SEQ/MAN

This switch determines the manner in which the head address is selected.

SEQ

Sequential – After performing a write or read operation, the FTU increases the count in the head address register by 1 for each index mark or, when in random, for each access. When the count is maximum (5 or 19), head zero is the next head selected, and the incrementing continues.

MAN

Manual – The FTU will select the head address set in the HEAD ADDRESS switches.

**ADDR ERROR
test point**

This test point goes to a logical 0 when an address error occurs.

**DATA ERROR
test point**

This test point goes to a logical 0 when a data error occurs.

**SECTOR MARK
test point**

This test point goes to a logical 1 when the FTU receives a Sector Mark signal from the drive under test.

**INDEX MARK
test point**

This test point goes to a logical 1 when the FTU receives an Index Mark signal from the drive under test.

**ON CYL
test point**

This test point will be a logical 0 when the drive under test is On Cylinder.

**READ DATA
test point**

This test point reflects the binary value of the serial data bits being received from the drive under test during a read operation. The test point is inoperative during maintenance mode.

**WRITE DATA
test point**

This test point reflects the binary value of the serial data bits being processed by the FTU during a write operation ("0" = 0, "1" = 1). The indication is valid for any write operation, even though the FTU is in the maintenance mode. The test point remains a logical 0 during read operations.

**BITS 0-9
test points**

These ten test points reflect the logical value of the bus-out bits (BOB) delivered to the drive under test via the A-cable. Logically, these bits are present in the FTU's bus-out multiplexer, and are available at the test point panel regardless of the operating mode (including maintenance mode) of the TB3A2. For an interpretation of the specific bus-out bits, see Table 2-15.

Table 2-15 FTU Test Points

Signal Name	Function – A-Cable (To Drive)		
Tag Bus Lines	Three lines that define the operation to be performed by the drive. Tag 1 gates the cylinder address and initiates the seek. Tag 2 gates the head address. Tag 3 is the control select that gates the function to be performed.		
Bus-Out Lines	Tag 1	Tag 2	Tag 3
Bit 0	1	1	Write Gate – Enables write circuits in drive unless drive is write protected.
Bit 1	2	2	Read Gate – Enables read circuits in drive.
Bit 2	4	4	Servo Offset Plus – Offsets the actuator from the nominal On Cylinder position toward the spindle.
Bit 3	8	8	Servo Offset Minus – Offsets the actuator from the nominal On Cylinder position away from the spindle.
Bit 4	16	16	Fault Clear – Pulse to clear the fault summary flip-flop in the drive.
Bit 6	64	–	RTZ – Pulse that causes the drive actuator to seek to track 0.
Bit 7	128	–	Data Strobe Early – Enables the drive's PLO data separator to strobe the data at a time earlier than optimum.
Bit 8	256	–	Data Strobe Late – Enables the drive's PLO data separator to strobe the data at a time later than optimum.
Bit 9	–	–	

GND test point	This test point is a common ground point between the FTU logic board and the control panel.
WRITE CLK test point	This test point reflects the logic level of the 9.667 MHz Write Clock signal that the FTU sends to the drive under test during any write operation.
READ CLK test point	This test point reflects the logic level of the 9.667 MHz Read Clock signal received from the drive under test during any read operation. A read error forces the test point to logical 0.
WRITE GATE test point	A logical 1 at this point indicates the presence of a Write Gate signal generated by the FTU during any write operation.
READ GATE test point	A logical 1 at this test point indicates the presence of a Read Gate signal generated by the FTU during any read operation.

CYL SELECT
test point

This test point goes to a logical 1 when the FTU sends a Cylinder Select signal (Tag 1) to the drive.

HEAD SELECT
test point

This test point goes to a logical 1 when the FTU sends a Head Select signal (Tag 2) to the drive.

CONTROL SELECT
test point

This test point goes to a logical 1 when the FTU sends a Control Select signal (Tag 3) to the drive.

2.7.3 Operation of the Field Test Unit (FTU)

2.7.3.1 General Description – The TB3A2 FTU is used to pin-point a problem in the drive, once the nature of that problem has been defined. Suppose, for example, that a drive is suspected of intermittent read errors. The TB3A2 can be set up to repeatedly write and read back any chosen data pattern on a given track, on the entire pack, on any portion of the pack between two selected cylinders, stopping when an error occurs.

By making several such error-stop passes, and by using the DISPLAY SELECT switch to identify the cylinder, head, character count, and the data pattern read for each error stop, the FE can create a record of error parameters that will provide a failure pattern for pin-pointing the problem.

The character-count display provides an indication of how far from index the error occurred. If you suspect a bad spot on the disk because errors consistently occur for the same head (track) and cylinder, the character count can confirm it. If the character count is random for that situation, suspect intermittent data failures on the selected head rather than a bad spot on the disk.

That is to say, the degree of flexing to which the head lead is subject at a particular head/arm location, plus machine vibration, might cause read/write errors; but they would most logically be random errors, not occurring at the same spot for every revolution of the disk. Discriminations between random errors and bad spots are important when writing the track format on a new scratch pack, as described in the operating procedures (Paragraph 2.7.3.3).

Data and address errors are the most prevalent causes for failure. The TB3A2 FTU provides bypass switches for each of these errors. This allows the FTU to alternately write and read a suspected track (or cylinder or pack area) for an extended period without stopping when an error of this type appears. After the test, the error count display will show the number of errors that occurred during the test period, up to a maximum of 15.

2.7.3.2 Preliminary Setup

1. At the drive, disconnect the A and B I/O cables running to the drive controller; connect the A and B adapter cables, provided with the FTU, between the drive and the tester.
2. Take steps to ensure that the system will not attempt to select the drive while that drive is being exercised by the FTU.
3. Remove ac power from the drive and make the I/O cable connections as determined in step 1. Do not reapply ac power to the drive.
4. Set the SEC (sector) switch on the FTU panel to 30 or 32, as desired for the drive under test.

- Set the following switches as shown for normal testing.

Switch	Position
SEQ PWR	Up
SERVO OFFSET	Center (off)
DATA STROBE	Center (normal)
WRT FLAG	Down (off)
XTAL/SERVO	SERVO
MAINT/NRM	NRM
WRT INHIBIT/NRM	NRM
PLUG VALID	Up
UNIT (3 switches)	To logical address of the drive
ADDR ERROR/BYPASS	Both down (off)
DATA ERROR/BYPASS (2 switches)	

- Turn on the FTU.
- Apply ac power to the drive. The UNIT SEL indicator should light up, as will the WRT PROT indicator if the drive under test is in the write protect mode.
- Install a scratch pack on the drive to be tested.
- Power up the drive. The WRT PROT lamp, if on, will go out when the drive is up to speed. The UNIT READY lamp will light up when the heads are loaded.
- Actuate the INITIALIZE switch.
- Actuate the RTZ switch, then the RESET switch on the FTU panel.

The drive is now ready for exercising. It has performed a seek to cylinder 0 and has selected head 0. The remaining switches on the FTU panel may now be set for the desired function and operating modes, as illustrated in the operating procedures (Paragraph 2.7.3.3).

2.7.3.3 Operating Procedures – The first five of the procedures described below embody every access, read/write, and head-select mode provided by the TB3A2. Paragraph 2.7.3.3.6 checks the data error logic and Paragraph 2.7.4.1 describes the use of the head alignment card.

Continuous Seek, No Read/Write – This procedure performs alternate seeks between the cylinder address in the CAR and the address set in the CYLINDER ADDRESS switches.

- Ensure that the FTU switches are positioned as described in the preliminary setup procedure (Paragraph 2.7.3.2). In addition, position the following switches as shown.

Switch	Position
DISPLAY SELECT	CYLINDER
WRT-RD SELECT	OFF

2. Set the CYLINDER ADDRESS switches to the value of one of the cylinder address to which the drive will seek. (For illustration, choose CA8.)
3. Set the ACCESS MODE switch to DIRECT.
4. Momentarily actuate the START switch. When the ON CYL indicator is lit, move the switch momentarily to STOP. Address 8 is now in the CAR, and will be displayed on the panel.
5. Set the CYLINDER ADDRESS switches to the value of the second cylinder address. (For illustration, choose CA16.)
6. Set the ACCESS MODE switch to CONT.
7. Actuate START. The drive will perform alternate seeks between addresses 8 and 16. The ON CYL indicator will blink rapidly as the heads move on and off cylinder. The cylinder address display lights will alternate between 8 and 16.
8. Stop the FTU.
9. Actuate RTZ.
10. Start the FTU. The tone of the drive will change as it now seeks between cylinders 0 and 16. Observe the display.
11. To stop the operation, actuate either STOP or RESET.

Random Seek, No Read/Write

1. Maintain the preliminary setup switch positions (Paragraph 2.7.3.2, step 5). In addition, set the following switches as shown.

Switch	Position
DISPLAY SELECT	CYLINDER
WRT-RD SELECT	OFF
ACCESS MODE	RAND

2. Actuate START.
3. Ensure that cylinders are being selected randomly by observing the changing pattern on the display lamps.
4. Stop the FTU by actuating STOP or RESET.

Write Format – This procedure is used to write a prescribed format on every track of the disk pack. The next procedure, read, determines whether any of the tracks so written contain errors. The final procedure, write flag, shows how to select a single track, write a “defective track” flag bit on that track, and check to ensure that the flag bit was indeed written. The track format is shown in Figure 2-36.

1. Maintain the switch positions as given in the preliminary setup procedure (Paragraph 2.7.3.2, step 5). In addition, set the following switches as shown.

Switch	Position
DISPLAY SELECT	READ DATA
ACCESS MODE	SEQ FWD
WRT-RD SELECT	WRT FORMAT
CYLINDER ADDRESS	All down (off)
SEQ/MAN	SEQ
HEAD ADDRESS	All down (off)
DATA PATTERN	70 octal

2. Move RTZ/RESET switch to RESET, then to RTZ.
3. Actuate START. Observe the progression of the display lights as the drive moves away from cylinder 0. (With the DISPLAY SELECT switch set to READ DATA, the cylinder address is displayed while the FTU is running.)
4. If an error stop occurs, remove the cause of the error by proceeding as indicated in the trouble analysis chart in Table 2-16. (Data errors will not occur during WRT FORMAT.) Then proceed as follows.
 - a. Actuate RESET to clear the error indication in the FTU.
 - b. Actuate START. This rewrites the track that was selected when the error occurred, then continues the write format operation.
 - c. Do not actuate RTZ. To do so would cause the operation to begin anew at cylinder 0, head 0.
5. After all tracks have been written, stop the FTU. (Writing will begin again at cylinder 0, so the actual stopping point is immaterial.)

Read – This operation tests the entire data pack for errors, using the sequential reverse access mode.

1. Set the following switches as shown. All others should remain as given for the write format procedure.

Switch	Position
DISPLAY SELECT	CYLINDER
ACCESS MODE	SEQ REV
WRT-RD SELECT	RD

2. Set the CYLINDER ADDRESS switches to the maximum cylinder address (822 decimal). The switch settings are as follows.

ON	OFF
512	1024
256	128
32	64
16	8
4	1
2	

Table 2-16 Trouble Analysis (Sheet 1 of 3)

Assume:

1. A & B I/O cables connected between drive and FTU.
2. Power applied to FTU and drive.
3. +5 V indicators on FTU panel are lit.
4. DATA/ADDRESS BYPASS switches OFF.
5. FTU set to READ track format.
6. READ indicator comes on when START switch (on FTU panel) is actuated.

Conditions	1	2	3	4	5	6	7	8
Seek error	N	Y	-	-	-	-	-	-
Clock error in SERVO position	N	-	Y	-	-	-	-	-
Clock error in XTAL position	-	-	-	N	Y	-	-	-
Sector Mark Error	N	-	-	-	-	Y	-	-
Sector Count Error	N	-	-	-	-	-	Y	-
Drive Fault	N	-	-	-	-	-	-	Y
Actions								
Go to sheet 2, "Conditions."	1	-	-	-	-	-	-	-
Actuate RESET, RTZ, START.	-	1	-	-	-	-	-	-
Refer to drive service manual.	-	2	-	-	-	4	4	1
Set XTAL-SERVO switch to XTAL; Actuate RESET, START.	-	-	1	-	-	-	-	-
Check TP5 (WRITE CLK) on FTU panel.	-	-	-	-	1	-	-	-
Refer to FTU diagrams.	-	-	-	-	2	5	5	-
Check B-cable for SERVO CLK signal. Troubleshoot discontinuity in drive, cable, FTU.	-	-	-	1	-	-	-	-
Check that sector switch (SEC) in FTU is set correctly.	-	-	-	-	-	1	1	-
Check TP1 (SECTOR MK) on FTU panel.	-	-	-	-	-	2	2	-
Check TP0 (INDEX MK) on FTU panel.	-	-	-	-	-	3	3	-

Upper-Left Quadrant: Assumptions needed for tests, as well as the test conditions.

Upper-Right Quadrant: Results of the test: N = No; Y = Yes; - = Don't care.

Lower-Left Quadrant: Actions to be taken for each test result.

Lower-Right Quadrant: Numbers show sequence of actions for the test results in a given column. After each action, the test is repeated and, if X = a "no error" or "problem solved" situation.

Table 2-16 Trouble Analysis (Sheet 2 of 3)

Conditions	1	9	10
Address error	N	Y	-
Data error, OFFSET and DATA STROBE switches in center (off) position	N	-	Y
Actions			
Track was read without error.	X	-	-
Perform WRT FORMAT for track in error; READ rewritten track.	-	1	-
Perform WRT.RD retry as follows.	-	-	1
Set FTU switches as indicated below.			
Switch WRT-RD SELECT ACCESS MODE SEQ/MAN HD ADRS CYL ADRS Position WRT.RD DIRECT MAN Select Failing track			
Actuate START; check for conditions 11 or 12 on following page of table.			
Unrecoverable error. Perform WRT FLAG procedure for track in error.	-	2	-

Table 2-16 Trouble Analysis (Sheet 3 of 3)

Conditions	11	12	13	14	15	16	17	18	19	20
Data error on WRT.RD retry	N	Y	-	-	-	-	-	-	-	-
Data error, OFFSET switch in + (FWD) position	-	-	N	Y	-	-	-	-	-	-
Data error, OFFSET switch in - (REV) position	-	-	-	-	N	Y	-	-	-	-
Data error, DATA STROBE switch set EARLY	-	-	-	-	-	-	N	Y	-	-
Data error, DATA STROBE switch set LATE	-	-	-	-	-	-	-	-	N	Y
Actions										
Set OFFSET switch to + (FWD) position; READ track in error.	-	1	-	-	-	-	-	-	-	-
Check Bit 2 TP on FTU panel; if missing, refer to FTU diagrams.*	-	-	-	1	-	-	-	-	-	-
Check BOB2 in drive; if missing, check I/O cable and FWD offset logic in drive.*	-	-	-	2	-	-	-	-	-	-
Set OFFSET switch to - (REV) position; READ track in error.	-	-	-	3	-	-	-	-	-	-
Check Bit 3 TP on FTU panel; if missing, refer to FTU diagrams.*	-	-	-	-	-	1	-	-	-	-
Check BOB3 in drive; if missing, check I/O cable and REV offset logic in drive.*	-	-	-	-	-	2	-	-	-	-
Return OFFSET switch to center (off); set DATA STROBE switch to EARLY. Read track in error.	-	-	-	-	-	3	-	-	-	-
Check Bit 7 TP on FTU panel; if missing, refer to FTU diagrams.*	-	-	-	-	-	-	-	1	-	-
Check BOB7 in drive; if missing, check I/O cable and Early Strobe logic in drive.*	-	-	-	-	-	-	-	2	-	-
Set DATA STROBE switch to LATE; Read track in error.	-	-	-	-	-	-	-	3	-	-
Check Bit 8 TP on FTU panel; if missing, refer to FTU diagrams.*	-	-	-	-	-	-	-	-	-	1
Check BOB8 in drive; if missing, check I/O cable and Late Strobe logic in drive.*	-	-	-	-	-	-	-	-	-	2
Drive has demonstrated its ability to recover data.	X	-	X	-	X	-	X	-	X	-
Unrecoverable error. Perform WRT FLAG procedure for track in error.	-	-	-	-	-	-	-	-	-	3

*When checking for the presence of these bits, the DATA ERROR BYPASS switch must be on ("up" position). This allows reading to continue in the event of an error. The switch should be off ("down" position) when checking for the conditions.

3. Actuate START. Reading will begin at maximum cylinder, head 0. Should an error occur, the RUN light will go out and the panel lamps will display the type of error, as well as the cylinder that was being read when the error occurred. Follow steps 4 and 5 for each separate error stop. If no errors, skip to step 6.
4. Record the error parameters, moving the DISPLAY SELECT switch as needed.

NOTE

It is not necessary to record the ERROR COUNT.
This will remain at count 1 for any stop-on-error operation.

5. After the error parameters have been recorded, actuate RESET to clear the error indication in the FTU, then actuate START to continue reading.
6. When the FTU begins reading again at the maximum cylinder address, actuate STOP to halt the FTU.

Write Flag – A single read may produce random errors that in an on-line environment would be eliminated by the system's error-recovery program.

Before flagging a track as bad – that is, as one that continually produces errors that are not recoverable – it is best to WRT.RD the track several times. If the error persists, the trouble analysis procedure (below) should be executed in an effort to recover the error. Only after both of these attempts have failed, should the track be flagged.

This procedure writes a “defective track” flag bit in Bit 6 of Address Word 1 (Figure 2-36).

1. Set the following FTU switches as indicated. Other switches should remain as shown for the preliminary setup procedure (Paragraph 2.7.3.2, step 5).

Switch	Position
WRT FLAG	Up (on)
DISPLAY SELECT	READ DATA
ACCESS MODE	DIRECT
WRT-RD SELECT	WRT FORMAT
DATA PATTERN (8)	As set when the track was most recently written
CYLINDER ADDRESS (11)	To select the track
HEAD ADDRESS (6)	To be flagged
SEQ-MAN	MAN

2. Actuate RESET, then START. Drive will seek to the selected track.
3. When ON CYL light comes on, wait about 1/2 second and then actuate STOP.
4. Set WRT-RD SELECT switch to RD.
5. Actuate START. The “defective track” flag bit will prohibit reading the track. The ADDRESS ERROR and DATA ERROR lights should not light up.
6. Actuate STOP.

Repeat steps 1 through 6 for each track to be flagged as defective.

NOTE

The WRT FLAG switch must be turned off before reading a track that has not been written as defective; otherwise an address error will occur.

Check Data-Error Logic – This procedure assures the operator that data errors will be recognized by the FTU. It is used when the FTU is exercising a drive in any situation where data errors are expected but none occur – an intermittent read failure, for example. It assumes that the procedure in question is still running and that the scratch pack therefore has a data field written on the tracks being tested.

1. Stop the FTU.
2. Set the following FTU switches as indicated.

Switch	Position
WRT-RD SELECT	RD
DATA ERROR BYPASS	Down (off)
DATA PATTERN	Choose any one switch and move it to the opposition position. (Move just one!)

All other switches must remain as they were at the start of the procedure being questioned.

3. Start the FTU. The FTU should stop with the DATA ERROR indicator lit.
4. Actuate RESET to clear the error indication.
5. Set the DATA ERROR BYPASS switch up (on).
6. Actuate START. The FTU should run without stopping on an error, but the RD/WRT ERROR counter will count the errors (up to 15).
7. Stop the FTU. Return all switches used during this procedure to the state they were in at the start of the procedure being questioned.

Trouble Analysis – Table 2-16 is a decision logic table (DLT). It shows the procedures the operator should take to eliminate any error that might occur when using the FTU to exercise a drive. Address and data errors will, of course, occur only during one of the read or write modes. Other errors may occur for either read/write or access only (no read/write) modes. It should be noted that sector mark and sector count errors are not indicated if the ADDRESS ERROR BYPASS switch is active.

Basically, the DLT deals with attempts to either eliminate or recover data and address errors before writing a “defective track” flag on the track in error. This involves trying various OFFSET and DATA STROBE switch combinations.

The DLT is divided into four quadrants. Each test condition (shown in the upper-left quadrant) is reduced to a yes (Y) or no (N) result, as indicated in numbered columns of the upper-right quadrant, two columns being allotted for each test condition. The two lower quadrants deal with recommended actions.

To determine what actions (if any) should be executed for a given test result, follow the selected column down to the number "1" (first recommended action) in the lower-right quadrant. The specific action to be taken is then located by following across to the lower-left (actions) quadrant. After action 1 has been taken, repeat the test that gave rise to the error condition. If the error persists, perform action 2, test again, and so on. An "X" in the lower-right quadrant indicates a "no error" or a "problem solved" situation, and requires no further remedial action.

Columns 12 through 20 (Table 2-16) define the sequential test that were alluded to in the second paragraph of this procedure, and which should be made in an attempt to recover any data error. Note that the last action item in any of these "yes" (even-numbered) columns instructs the operator to set up the next condition, or test, for rereading the track in error. When the last of these sequential tests has failed to recover the data, then and only then should the write flag procedure be carried out as indicated by action 3 of column 20.

2.7.4 Head Alignment Procedure

2.7.4.1 Installation of Head Alignment Card - This procedure describes the use of the type HFSV head alignment card and the null meter on the FTU control panel to perform read/write and/or servo-head alignment on the SMD under test. The cabling involved is seen in Figures 2-37 and 2-38 gives specific connection information. The switches and indicators on the HFSV card are shown in Figure 2-37.

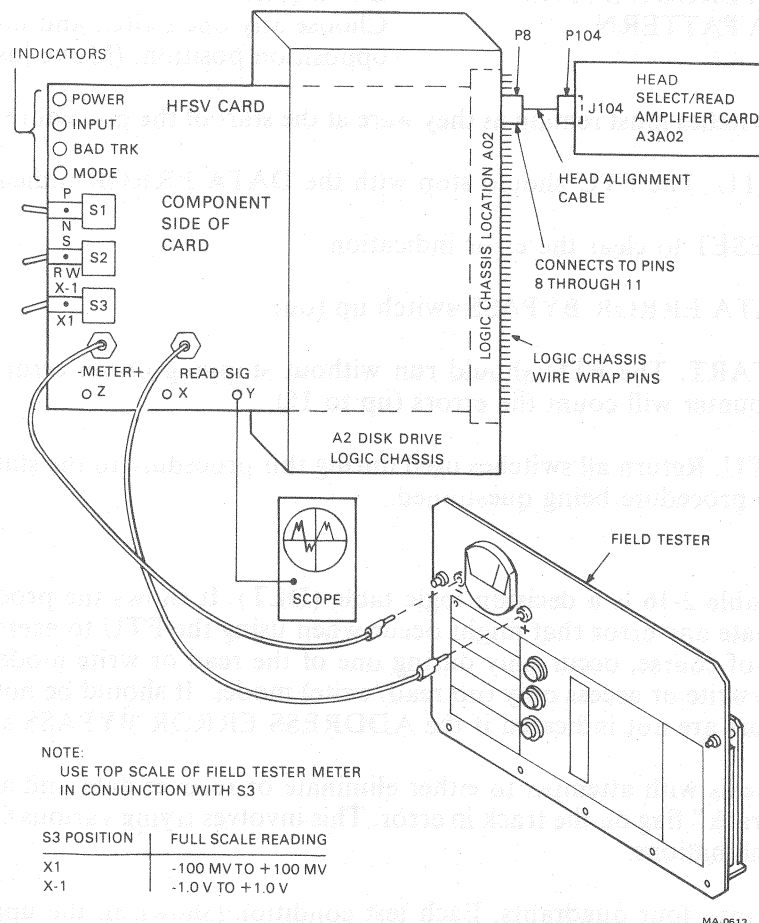
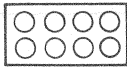


Figure 2-37 Head Alignment Connections

SMD SERIES	HEAD ALIGNMENT CARD LOCATION	HEAD ALIGNMENT CABLE	
		P104 	P8 
CDC BK5xx DEC RM02 RM03	A02	PLUGS INTO J104 ON HEAD SELECT/READ AMPLIFIER CARD IN R/W CHASSIS.	SLIPS OVER W/W PINS 8A,B THROUGH 11A,B AT LOCATION RESERVED FOR HEAD ALIGNMENT CARD

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Figure 2-38 Head Alignment Card

This procedure assumes that the I/O connections between the drive and the FTU have already been made as described in the installation portion of this manual. The installation and cabling of the head alignment card, must be made with ac power removed from the drive and the FTU.

1. Install the proper CE pack on the drive to be tested.
2. Install the HFSV card in the drive's logic chassis at location A02.
3. Install the head alignment cable between the drive's logic chassis and the jack on the card in the read/write (R/W) chassis, as specified in Figure 2-38. Note that P104 is keyed so that it will fit on the R/W card only one way.
4. Connect the test leads, provided with the FTU, between the HFSV card and the null meter on the FTU panel. Observe polarity.
5. Set the WRT INHIBIT/NRM switch on the FTU to WRT INHIBIT.
6. Apply ac power to the drive. The POWER lamp on the HFSV card should light up.
7. Power-up the drive.
8. Turn on the FTU. If the drive under test is in the write protect mode, the WRT PROT light on the FTU panel will be lit.
9. When the drive is up to speed and the READY light on the FTU panel is lit, actuate RESET, then RTZ.
10. Set the MAINT/NRM switch to MAINT. This provides a pseudo-index mark that enables the FTU to generate a head select. (The CE pack does not have an index mark.)

NOTE

Installing the head alignment card (Table 2-17) automatically "write protects" the drive (even though it will not of itself cause the WRT PROT light to come on). Therefore, if write, write-then-read, or write-format operations are to be conducted, the HFSV card must first be removed from the drive.

Table 2-17 Head Alignment Card Switches and Indicators

	Switches
S1	Changes the polarity of the alignment signal to the null meter; P = positive; N = negative. Algebraically subtract P from N to determine alignment error: P = +30 mV; N = -40 mV; Error = 70 mV.
S2	S position selects servo head as input to HFSV. RW position selects a data head as input to HFSV.
S3	Changes sensitivity of HFSV. The X.1 position attenuates card output by a factor of 10, and alignment error cannot be accurately measured. The X1 position does not attenuate HFSV output; alignment error can be accurately measured.
	Indicators
POWER	Lit when power is applied to the card.
INPUT	When lit, indicates that input signals are too low for HFSV to operate.
BAD TRK	When lit, indicates a short duration loss of input. <i>A one-shot keeps the LED lit for at least 4 seconds.</i> The lamp will light when S1 is toggled.
MODE	Lit when S2 is in the S (servo) position or when S3 is set to X.1. When either of these conditions exists, read/write head alignment error cannot be measured.

2.7.4.2 Preliminaries for Head Check or Alignment – Before performing the head arm alignment procedure, read and understand the concepts that follow. These are important for accurate head alignment, and they are only referenced in the procedure.

Thermal Stabilization – In order to ensure accuracy during head alignment, it is important that the drive, CE pack, and FTU be at their normal operating temperature. This requires that all three be connected and allowed to operate (pack turning and heads loaded to cylinder 0) for a minimum of 60 minutes. If head alignment is being performed on more than one drive, provided that the pack was taken immediately from a previous drive and the drive under test has been operating with heads loaded for a minimum of 60 minutes preceding test, the CE pack only requires 15-minute stabilization.

Write Protect – Although the presence of the head alignment card in the appropriate slot will write protect the drive, the WRITE PROTECT switch on the front of the drive should be pushed in, as an extra precaution.

Alignment Tool – Use only the head alignment tool specified in the maintenance tools and materials table. Use of a different tool may cause damage to head-arm or carriage. Always inspect the adjustment end of tool prior to use. The tool must be free of nicks and scratches, and must have a polished surface. If any aluminum deposits are present, polish the tool surface with crocus cloth. Any other polishing medium will damage the tool. Do not use a defective tool; repair or replace the tool if damage exists. When using the tool, position alignment tool so that pin in the end of the tool engages the adjustment slot in the head arm. Ensure that the alignment tool is kept perpendicular to the hole in the carriage at all times. The tool should turn freely in hole. If it doesn't, recheck the end of the tool for damage or aluminum buildup.

Calculating Offset – The formula for calculating head offset is $(P) - (N) = \text{Offset}$, where P is equal to the meter reading with the head alignment card P/N switch in the P position, and N is equal to the reading with the switch in the N position. All meter readings to the left of 0 are negative. The following are examples of offset calculation.

1. $P = +20 \text{ mV}$, $N = +15 \text{ mV}$:
 $(P) - (N) = (+20) - (+15) = +5 \text{ mV}$
2. $P = +20 \text{ mV}$, $N = -15 \text{ mV}$:
 $(P) - (N) = (+20) - (-15) = +35 \text{ mV}$
3. $P = -20 \text{ mV}$, $N = +15 \text{ mV}$:
 $(P) - (N) = (-20) - (+15) = -35 \text{ mV}$

Seek Error Preventing – When the alignment tool is used to position the heads, a small amount of sideways pressure on the tool can cause the carriage to move. This relatively minor amount of movement generates an error voltage which is sensed by the logic as a seek error. The end result is that the logic clears the slope flip-flop and causes the drive to seek to the next even cylinder.

Excessive Misalignment – Occasionally, during the alignment check, a badly misaligned head(s) (in excess of 200 mV offset) may be discovered. If this is so, the head(s) should not be realigned until all packs written by that drive have been dumped (data transferred from pack to other storage). Failure to dump the packs before realignment of the heads will mean that the data is not recoverable.

Carriage Locking – During the alignment procedure (when the heads are over the alignment track), the carriage locking pin and ring assembly is installed in the ALIGN TRACK LOCK hole in the rail bracket assembly. This locks the carriage in place. Failure to install the pin and ring assembly would allow the carriage to retract if any emergency retract signal were generated. If the FE's hands are in the actuator during the head alignment procedure, the retract could be dangerous. It should also be noted that should a retract condition be generated, the carriage locking pin and ring assembly must be immediately removed to allow the heads to retract before a head crash occurs. Carefully observe the instructions regarding the installation and removal of the carriage locking pin and ring assembly.

NOTE

Do not do an RTZ on the FTU with the carriage locking pin in the ALIGN TRACK LOCK hole.

CE Pack – The CE pack has odd-even dibits written on tracks 000 through 330 only, on the servo surface. Do not attempt to access beyond track 330.

2.7.4.3 Head Alignment Check – The following procedure first checks the alignment of the servo head and then checks the alignment of the read-write heads (which are aligned in relation to the servo head).

NOTE

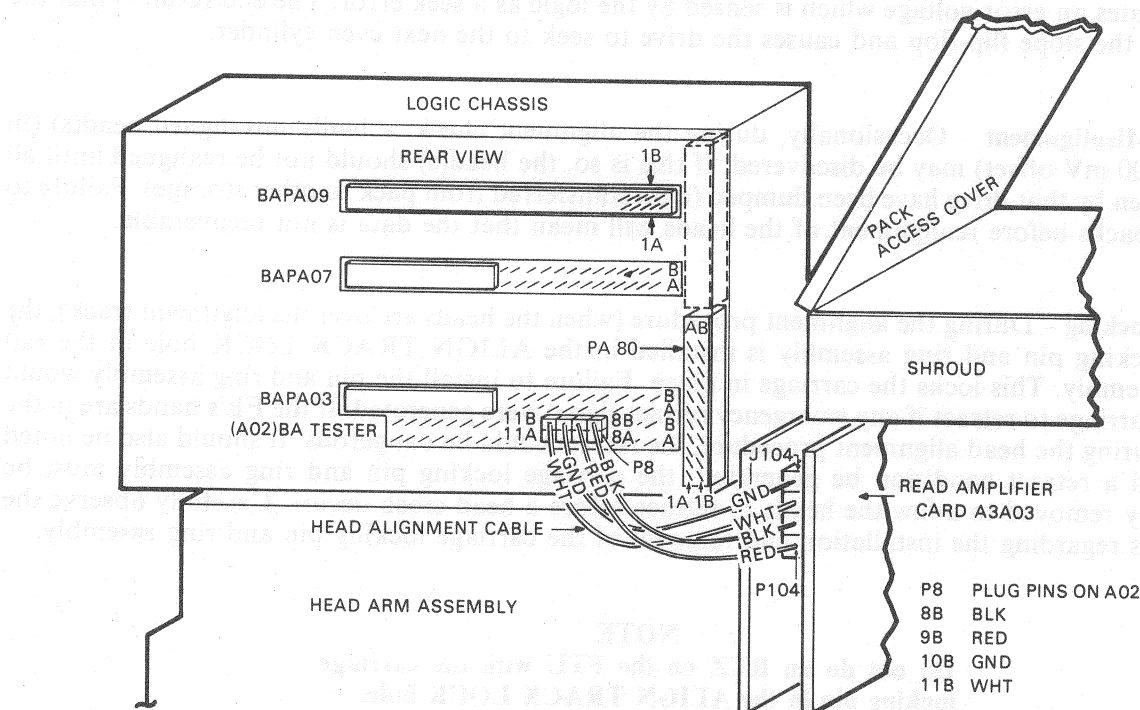
Check that the rear shipping bracket is removed before attempting alignment and place the LOCAL/REMOTE switch in the LOCAL position.

Alignment instructions are provided if any head exceeds the allowable offset. The numbers specified are decimal values for the cylinder address.

1. With heads fully retracted, raise logic chassis to maintenance position and note position of servo head adjustment slot in relation to hole in carriage. The adjustment slot should be approximately centered in carriage alignment hole (Figure 2-39).

NOTE

If drive has been used to write data packs, servo head should not be realigned until all read-write heads have been checked and it is known that excessive misalignment does not exist on any of them. Refer to step 1.



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Figure 2-39 Head Alignment Cable

2. If servo head is misaligned, loosen mounting screw and (using alignment tool) position adjustment slot as shown in Figure 2-40. When servo head is properly positioned, tighten head-mounting screw to a torque of $12 \pm 1/2$ inch-pounds. Lower logic chassis to normal operating position.

NOTE

If servo head is adjusted, all read-write heads must be adjusted.

3. With CE pack installed and oscilloscope connected to head alignment card test point Y, load heads to cylinder 000 and perform thermal stabilization.

CAUTION

Do not attempt to access beyond cylinder 330.

4. When thermal stabilization is completed, command continuous seeks between cylinders 240 and 245 for 30 seconds, minimum. This allows head-gimbal springs to settle to a normal operating position, and also settles any binding between head arm and head-mounting screw. Track 4 is a spare alignment servo track. The switch settings for cylinder 240 are 16, 32, and 128. For cylinder 245, they are 1, 4, 16, 32, 64, and 128.
5. Stop continuous seeks and command a direct seek to cylinder 245.
6. On head alignment card, set S/RW (servo/read write) switch to S position; set X.1/X1 switch to X.1 position.
7. Balanced dibit pattern, similar to Figure 2-41, should be observable on oscilloscope. If pattern is not balanced, terminate head arm alignment and perform trouble analysis.

NOTE

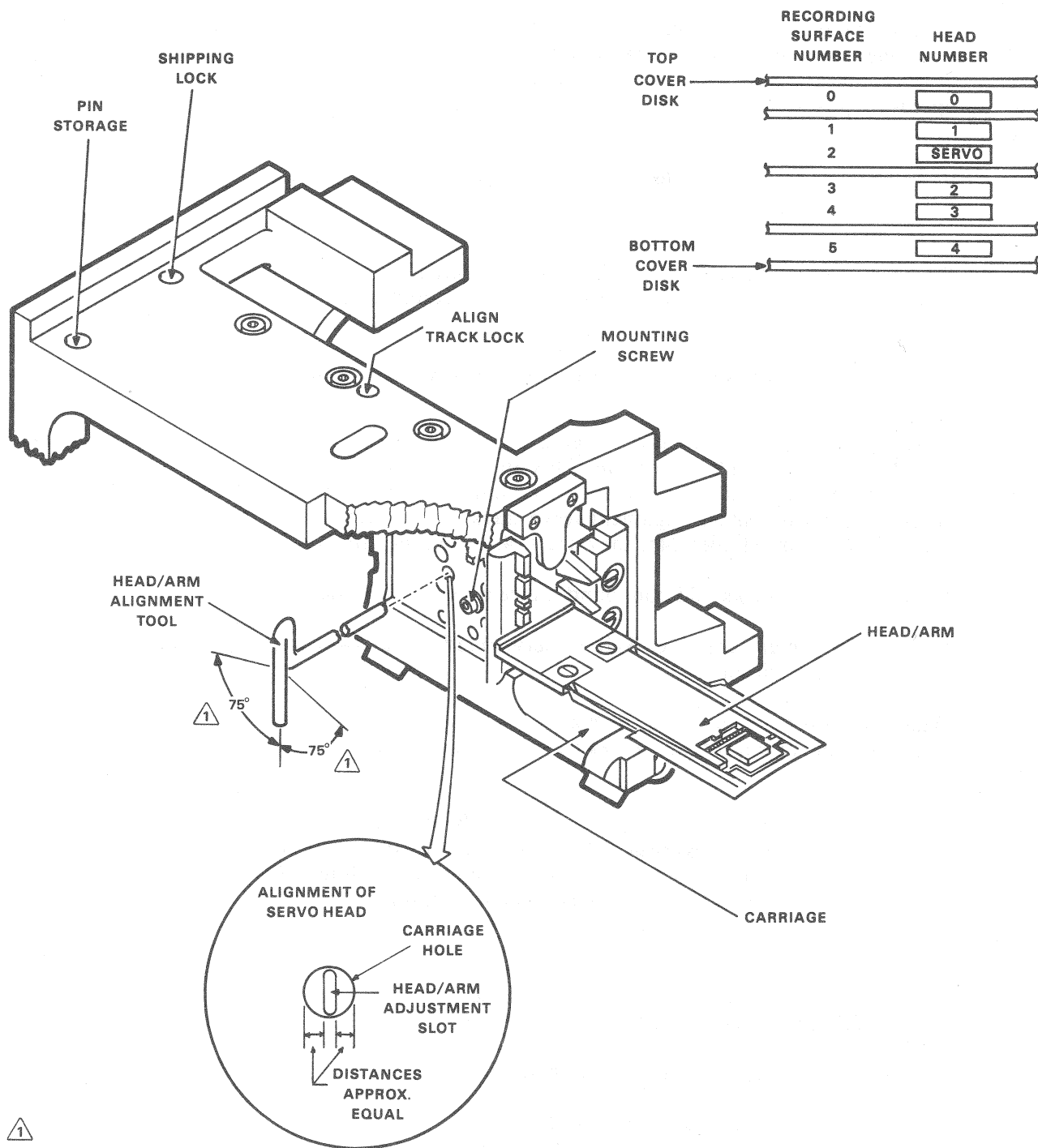
When calculating head offset, if both P and N readings are less than 100 mV, set X.1/X1 switch on head alignment card to X1 position. Return switch to X.1 position before proceeding to next head.

8. If balanced dibit pattern was observed in previous step, calculate head offset for servo head. Servo head offset must be 0 ± 30 mV. If offset is greater than 30 mV, terminate procedure and troubleshoot servo system.
9. On head alignment card, set S/RW switch to RW position. Select head 0.
10. Calculate and record offset for head 0.
11. Repeat previous step for all remaining heads.

CAUTION

If any read-write head exceeded 200 mV offset, excessive misalignment exists. Refer to Step 1 and realign.

12. If calculated offset for any read-write head exceeded 100 mV, proceed to align heads. If all heads were within the offset requirements, restore drive to normal operation.



CAUTION:

ALIGNMENT TOOLS ON SOME DRIVES CANNOT BE ROTATED MORE THAN 150°. ROTATING TOOL BEYOND 150° MAY DAMAGE HEAD SLOT OR ALIGNMENT TOOL.

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Figure 2-40 Head Arm Alignment

OSCILLOSCOPE SETTINGS

LOGIC GND TO SCOPE GND

VOLTS/DIV

CH 1 - 2V

CH 2 - NOT USED

TIME/DIV

A - 2 μ SEC

B - NOT USED

TRIGGERING

A - INTERNAL POSITIVE

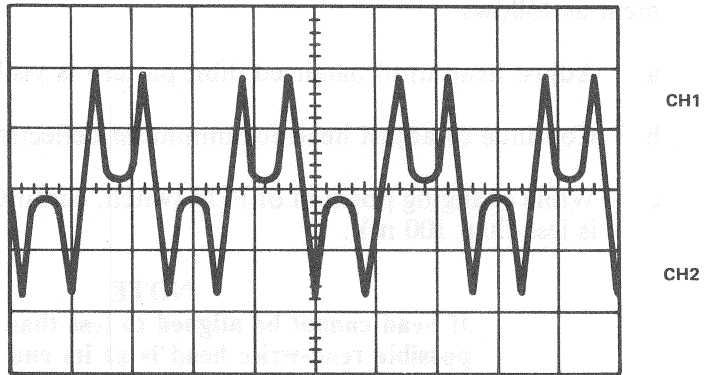
B - NOT USED

PROBE CONNECTIONS (USE X10 PROBE)

CH 1 TO ON HFSV CARD

READ SIGNAL Y

CH 2 - NOT USED



MA-0606

Figure 2-41 Balanced Dibit Pattern

2.7.4.4 Performing Head Alignment

1. Ensure that the locking pin has been removed.
2. Command a return-to-zero seek. Press START switch to stop drive motor and unload heads.
3. Raise logic chassis to maintenance position and loosen head-mounting screw for any head that exceeded the offset specification. Then retighten each loosened screw to a torque of 6 inch-pounds. *Remove the connector support bracket from the head-arm connectors.* This prevents possible electrical contact between the alignment tool and bracket. Contact could cause a short circuit that would damage power amplifier.
4. Press START switch to start drive motor and load heads. Command continuous seeks between cylinders 240 and 245 for 30 seconds, minimum. Note that the MAINT/NRM switch must be in the NRM position to do oscillating seeks.
5. Stop continuous seeks and command a direct seek to cylinder 245.

WARNING

Use care not to cause any short circuits when moving logic chassis to install locking pin. Failure to install locking pin could cause personal injury.

6. Swing down logic chassis and install carriage locking pin and ring assembly in ALIGN TRACK LOCK hole. Return logic chassis to maintenance position.
7. Ground back panel pin A2B09, 03B (Not On Cylinder) to prevent nuisance errors. Ensure that head alignment card X.1/X1 switch is set to X.1 position and select head to be aligned.

NOTE

The MAINT/NRM switch must be in the MAINT position to select a different head. Place the RD/WRT select switch to RD.

8. Using recommended head alignment tool, (with the sleeving on it) perform coarse adjustment as follows.
 - a. Adjust head until balanced dibit pattern is visible on oscilloscope.
 - b. Continue to adjust head for minimum deflection of null meter with respect to 0.
 - c. While changing position of P/N switch, continue to adjust head until calculated offset is less than 100 mV.

NOTE

If head cannot be aligned to less than 100 mV, it is possible read-write head is at its end of travel. Re-check servo head alignment.

9. Repeat previous step for all heads to be aligned.
10. On head alignment card, set X.1/X1 switch to X1 position.
11. Perform fine adjustment same as coarse adjustment except adjust until calculated offset is less than 50 mV. Perform fine head adjustment for all heads to be aligned.
12. Remove ground from backpanel pin A2B09 03B.
13. Move carriage locking pin and ring assembly to PIN STORAGE hole.
14. Perform a return-to-zero seek.
15. For each head adjusted, tighten head-mounting screw to a torque of $12 \pm 1/2$ inch-pounds.
16. Command continuous seeks between cylinders 240 and 245 for 30 seconds, minimum.
17. Stop continuous seeks and command a direct seek to cylinder 245.

WARNING

Use care not to cause any short circuits when moving logic chassis to install locking pin. Failure to install locking pin could cause personal injury.

18. Swing down logic chassis and install carriage locking pin and ring assembly in ALIGN TRACK LOCK hole. Return logic chassis to maintenance position.
19. Ensure that head alignment card X.1/X1 switch is in X1 position.
20. Check alignment of each head that was adjusted to ensure that tightening screws did not change alignment.

CAUTION

Use care when using alignment tool on heads that have been tightened to torque of $12 \pm 1/2$ inch-pounds. Misuse of tool will damage head arm or carriage.

21. If calculated offset for any head exceeds 75 mV, repeat fine adjustment procedure until offset is less than 50 mV.

22. Move carriage locking pin and ring assembly to PIN STORAGE hole.
23. Restore drive to normal operation.

2.8 FIELD ACCEPTANCE PROCEDURE

2.8.1 Introduction

Field acceptance testing is intended to demonstrate the performance of the RM02 or RM03 disk drive subsystem to the customer prior to his acceptance.

2.8.2 Error Definitions/Rates

The drive contains two registers to display the various error conditions possible. Error registers 1 and 2 (RMER1, RMER2) indicate drive error conditions. One bit of RMER2 (SKI) indicates seek errors and is used to calculate the seek error rate (Paragraph 2.8.2.4). Four bits of RMER1 (HCRC, HCE, ECH, and DCK, which may include DTE and FER) indicate data errors; the remaining bits of RMER1 indicate command and control errors. Table 2-18 lists indications of the various error types and their explanations.

2.8.2.1 Hard Errors – Any failure to read data correctly after a complete recovery sequence with ECC enabled constitutes an irrecoverable, or hard, error. (A complete recovery sequence consists of 20 retries, 16 at the nominal head position and 2 at each offset.)

Errors that are not ECC-correctable include bursts greater than 11 bits in length and isolated dropped bits (separated by more than 11 bits) within a sector. The allowable error rate for hard errors is one error per 10^{12} bits read.

2.8.2.2 Soft Errors – Any failure to read data correctly on the first try that is then read successfully during a recovery sequence constitutes a recoverable, or soft, error. (Refer to the Paragraph 2.8.2.1 definition of a complete recovery sequence.) The allowable error rate for soft errors is one error per 10^{10} bits read.

2.8.2.3 Pack-Attributable Errors – An error caused by imperfections in the recording surface is regarded as pack-attributable, or media-dependent. If the imperfection is less than 11 bits long, it is ECC-correctable and will appear as a soft error; if more than 11 bits long, it will appear as a hard error. On a given pack, pack-attributable errors will always appear at the same cylinder, sector, and track addresses, with an ECC POS REG value within 11 bits. The definitions of hard and soft errors in Paragraphs 2.8.2.1 and 2.8.2.2 apply only to randomly distributed errors, and do not take into account errors that are pack-attributable. Imperfections in the pack surface may be found by mapping the pack using the formatter program but there is no guarantee that they will all be found.

2.8.2.4 Seek Errors – A seek error is any positioning operation that is not completed within 500 ms for seek commands, 500 ms for recalibrate commands, and 10 ms for offset and return-to-centerline commands, or that terminates with the positioner in an incorrect location. The allowable error rate for seek errors is one error per 10^6 seek operations.

2.8.3 Field Acceptance Test

The tests described in Paragraph 2.8.4 may be used, individually or in combination, to demonstrate the performance of the disk drive when used with an RH70 controller.

2.8.4 Diagnostic Programs

The diagnostic programs described herein are employed with the RM02 and RM03 subsystems. Refer to the applicable diagnostic operation procedures for more detailed information.

Table 2-18 Error Conditions

Bit	Bit Set Register	Error Type	Explanation
HCE HCRC	RMER1 RMER1	Soft	Sector count field/desired. Sector compare fails due to CRC failure.
HCRC	RMER1	Soft	Sector count field matches desired sector field but there is CRC error.
HCRC FER	RMER1 RMER1	Soft	Format bit in first header word incorrect.
NOTE FER without HCRC during an operation that reads the header indicates wrong format pack mounted.			
DCK	RMER1	Soft	Error detected during read operation by examination of ECC bytes; correctable by retry sequence.
DCK ECH	RMER1 RMER1	Hard	Error detected which is ECC uncorrectable through 28 retry sequence (16 retries at nominal head position and 12 with head offset).
SKI	RMER2	Seek	1. Seek operation fails to complete within 500 ms of initiation. 2. Recalibration operation fails to complete within 500 ms of initiation. 3. Offset or return-to-centerline operation fail.
SKI	RMER2	Seek	Positioner has drifted off cylinder subsequent to completion of positioning operation.
HCE	RMER1	Seek	Sector count field (RHLA) does not match desired sector field (RHDST) and there is not a CRC error. This error is not caused by a positioner failure: It is due to a DCL failure. Therefore, HCE alone indicates a drive seek error.

Test Programs

MAINDEC-ZZ-CZRMF	Extended Drive Test
MAINDEC-ZZ-CZRMG	Dual-Port Logic Test, Part 1
MAINDEC-ZZ-CZRMH	Dual-Port Logic Test, Part 2
MAINDEC-ZZ-CZRMJ	RM02/03 Diskless Controller Test (only MBA test)
MAINDEC-ZZ-CZRMC	RM02/03 Functional Controller Test, Part I
MAINDEC-ZZ-CZRMD	RM02/03 Functional Controller Test, Part II
MAINDEC-ZZ-CZRME	RM02/03 Functional Controller Test, Part III (format the pack before doing Part III)

System Exerciser Program

MAINDEC-ZZ-CZRMB	Performance Exerciser (need formatted pack)
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Utility Programs

MAINDEC-ZZ-CZRMA	Formatter Program (need good pack)
MAINDEC-ZZ-CZRMI	Drive Compatibility Test

MAINTENANCE - 1000

MAINTENANCE - 1000

MAINTENANCE - 1000

MAINTENANCE - 1000

MAINTENANCE - 1000

MAINTENANCE - 1000

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CHAPTER 3 OPERATING INSTRUCTIONS

This chapter contains general information related to subsystem operation and operator maintenance.

3.1 OPERATOR'S CONTROLS AND INDICATORS

The RM02 or RM03 Disk Subsystem has operator's controls and indicators located on the drive's front panel, rear panel, and on the Massbus adapter power supply. See Figure 3-1 for their locations.

3.1.1 Front Panel Controls and Indicators

The front control panel contains eight controls and indicators. They are illustrated in Figure 3-2.

3.1.1.1 START Switch – The START switch is a 2-position pushbutton. Pressing the START switch when the drive is in the power-off condition (disk pack not spinning), lights the START indicator and initiates the power-up sequence provided the following conditions are met.

- Disk pack is installed.
- Pack access cover is closed.
- All power supply circuits are on.

3.1.1.2 START Indicator – This indicator will light when the START switch is depressed from the off position provided the three preconditions just mentioned are met. The light indicates that power is on.

3.1.1.3 READY Indicator – Once the start sequence has been initiated by pressing the START switch, the READY indicator will blink once a second until the disk pack is up to speed.

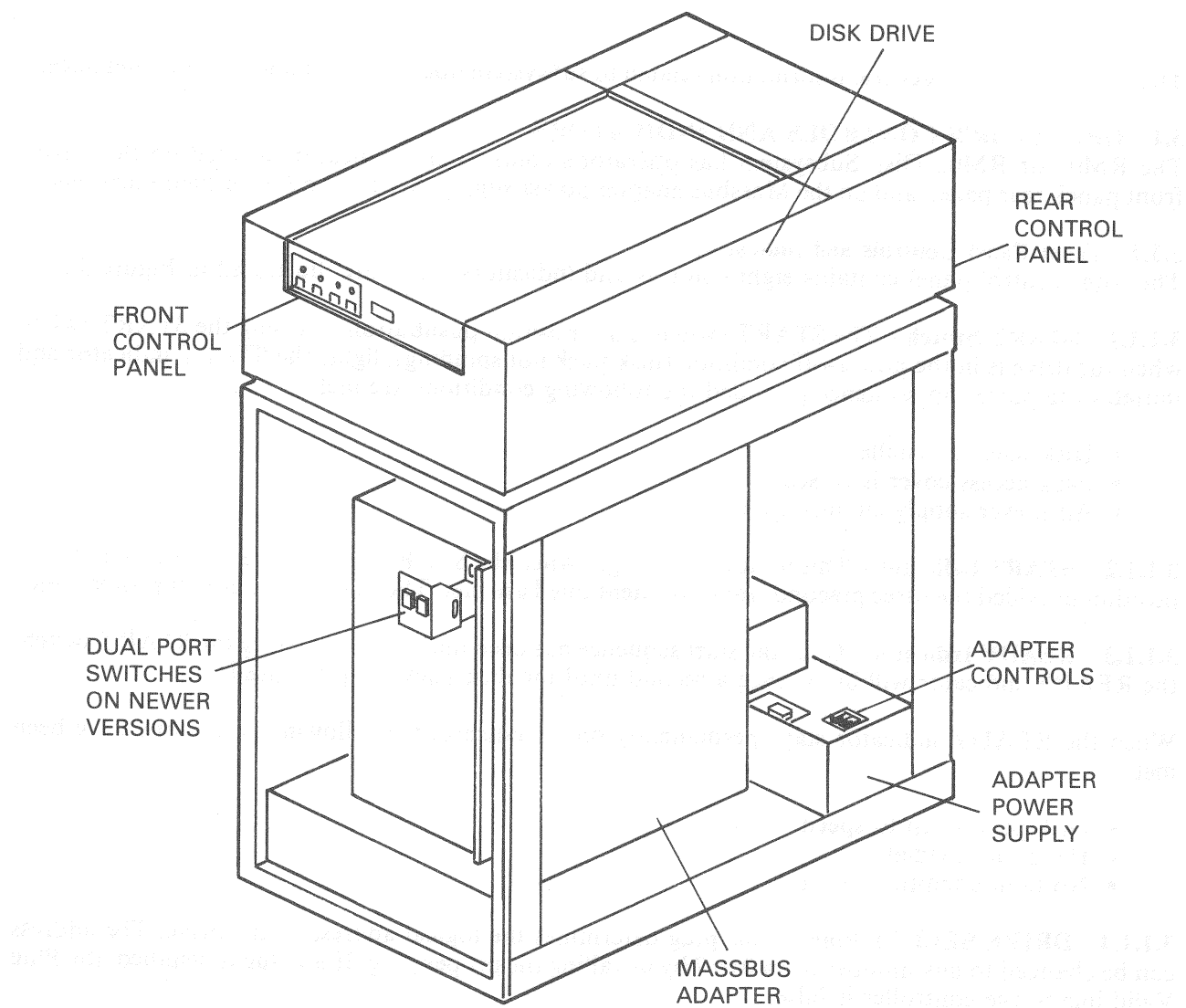
When the READY indicator stays permanently on, it indicates the following conditions have been met.

- Disk pack is up to speed.
- Heads are loaded.
- No fault conditions exists.

3.1.1.4 DRIVE SELECT Plug – This plug determines the logical address of the drive. The address can be changed to any number from 0 to 7 by installing the proper plug. If no plug is installed, the Plug Valid line to the controller is false.

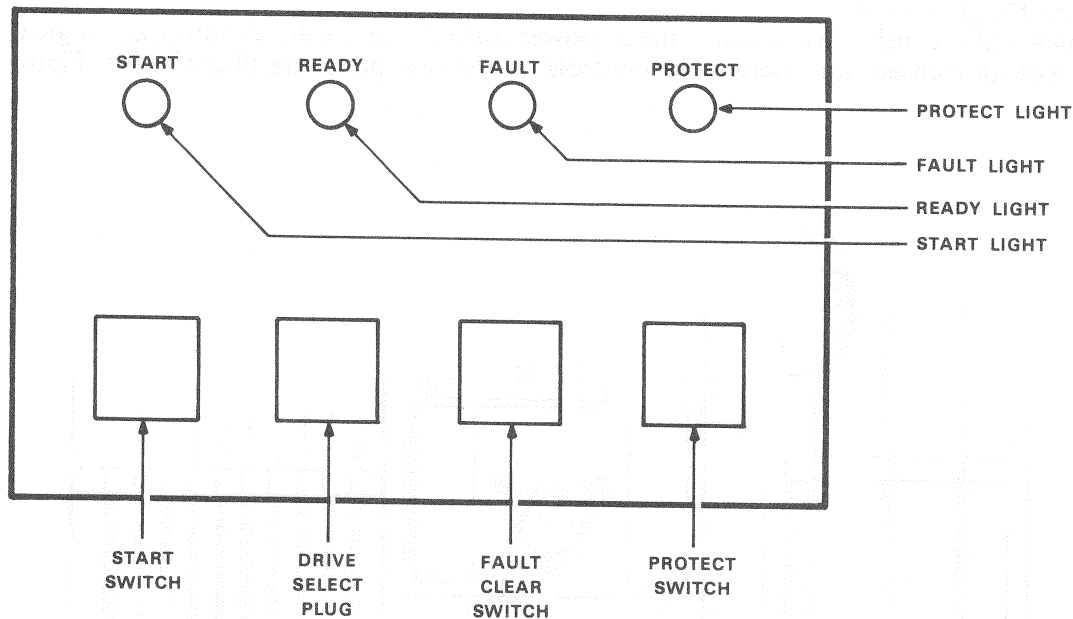
3.1.1.5 FAULT Indicator – The FAULT indicator lights up when one or more of the following fault conditions exist in the drive.

- Write fault
- Head select fault
- Read/write fault
- Read/write while off cylinder fault
- Voltage fault



CZ-0029

Figure 3-1 Location of Subsystem Controls



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Figure 3-2 Front Panel Controls and Indicators

If the fault condition that caused the FAULT indicator to come on has been removed, then the FAULT indicator can be extinguished in five different ways.

- Depressing the FAULT switch on the operator's control panel
- Pressing the MAINTENANCE FAULT CLEAR switch on the fault card in logic chassis location A04
- Issuing an Initialize signal from the controller
- Issuing a Fault Clear signal from the controller
- Powering down the drive

3.1.1.6 FAULT CLEAR Switch – This switch is a momentary contact pushbutton used to clear the FAULT indicator. Depressing the FAULT CLEAR switch will extinguish the FAULT indicator only if the fault condition no longer exists.

3.1.1.7 WRITE PROTECT Indicator – When this indicator is on, it signifies that the drive is in the write protect mode. While in this mode, data cannot be written on the disk pack.

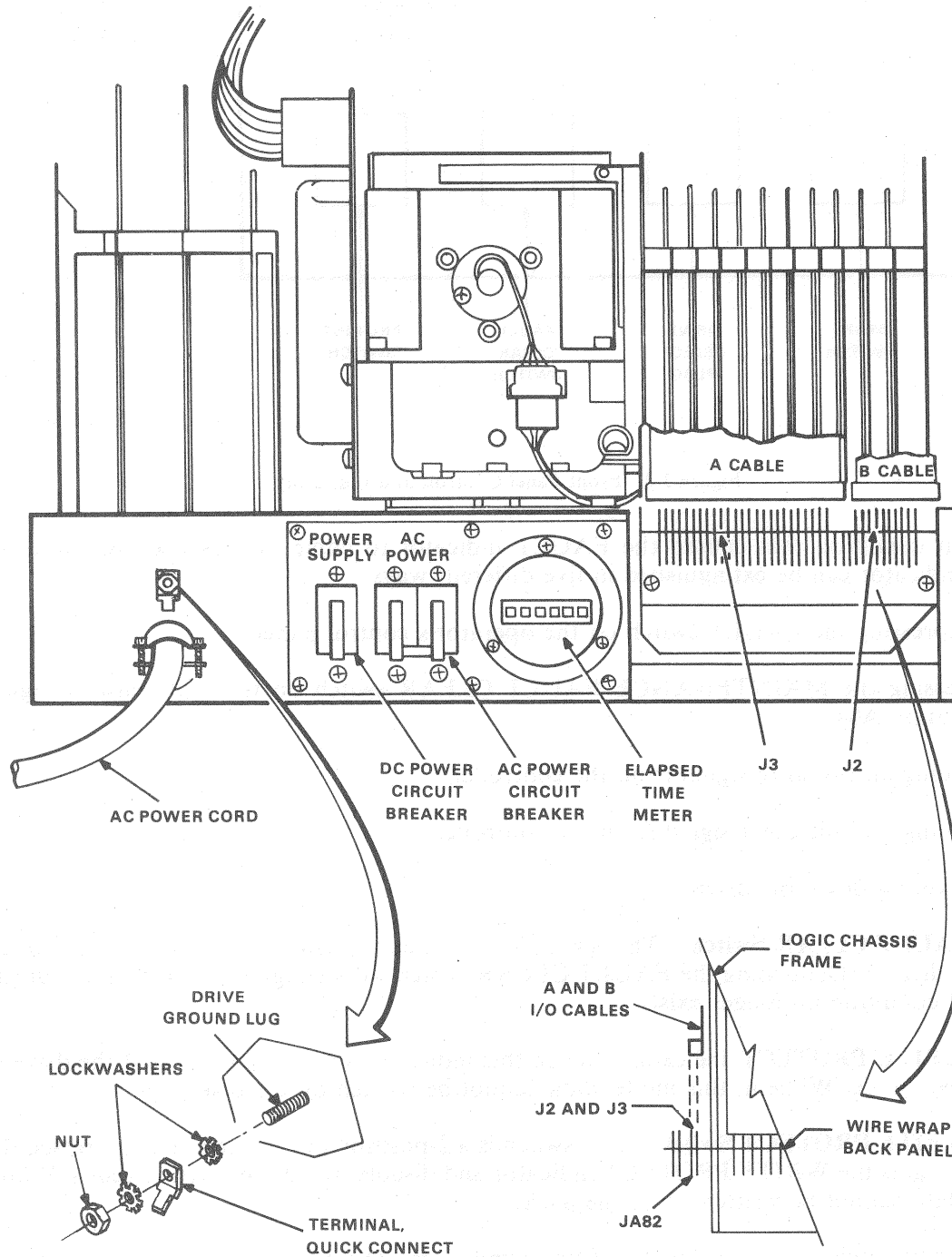
3.1.1.8 WRITE PROTECT Switch – This switch is a 2-position pushbutton. When pressed to the IN position, it lights the WRITE PROTECT indicator and disables the drive's write circuits. While in this position, data cannot be written on to the pack.

Releasing this switch back to its OUT position removes the Disable signal from the write circuits and extinguishes the WRITE PROTECT indicator.

3.1.1.9 PORT SELECT Switches – These switches are located on the front cabinet door in newer dual-port models. Refer to Table 2-12 for switch settings.

3.1.2 Rear Panel Controls

The rear panel of the disk drive contains the ac power controls for the drive motors and logic circuitry. It also houses an elapsed time meter. The controls on the rear panel are illustrated in Figure 3-3.



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Figure 3-3 Rear Panel Controls and Cable Connections

3.1.2.1 AC Power Circuit Breaker – The ac power circuit breaker applies ac power to the drive's dc power supply circuit breaker and the drive blower motor. It also provides ac power for the drive spindle motor. The spindle motor will not start unless the control panel START switch is pressed to enable the motor startup sequence.

3.1.2.2 DC Power Supply Circuit Breaker – This circuit breaker applies ac power to the dc power supply provided that the ac power circuit breaker is on and the power cord is plugged in. The dc power supply provides the dc voltages needed by the drive logic circuits.

3.1.2.3 Elapsed Time Meter – This meter records the accumulated ac power-on time. The meter starts when the ac power circuit breaker is set to ON.

3.1.3 Adapter Power Supply Controls

The adapter power supply is located under the disk drive inside the subsystem cabinet. Access to it can be gained most easily through the rear door of the cabinet. The adapter power supply location is shown in Figure 3-1.

On the top surface of the adapter power supply are located some ac power circuit breakers, an ac receptacle, a fuse, and a dc power connector (J9). Figure 3-4 shows these controls and connectors.

3.1.3.1 AC Receptacle – The ac receptacle on the top of the adapter power supply is used as the source of ac power for the disk drive power cord. When the drive power cord is plugged into this receptacle, the ac power to the drive is controlled by the MAIN AC POWER CIRCUIT BREAKER on top of the adapter power supply.

3.1.3.2 Main AC Power Circuit Breaker – This circuit breaker controls the ac power to the whole RM03 Disk Subsystem. When in the ON position, it routes ac power to both the adapter dc power supply circuit breaker and to the disk drive ac power cord.

3.1.3.3 Adapter DC Power Supply Circuit Breaker – This circuit breaker applies ac power to the adapter dc power supply provided the main ac circuit breaker is on. The dc power supply provides the dc voltages needed by the Massbus adapter circuits.

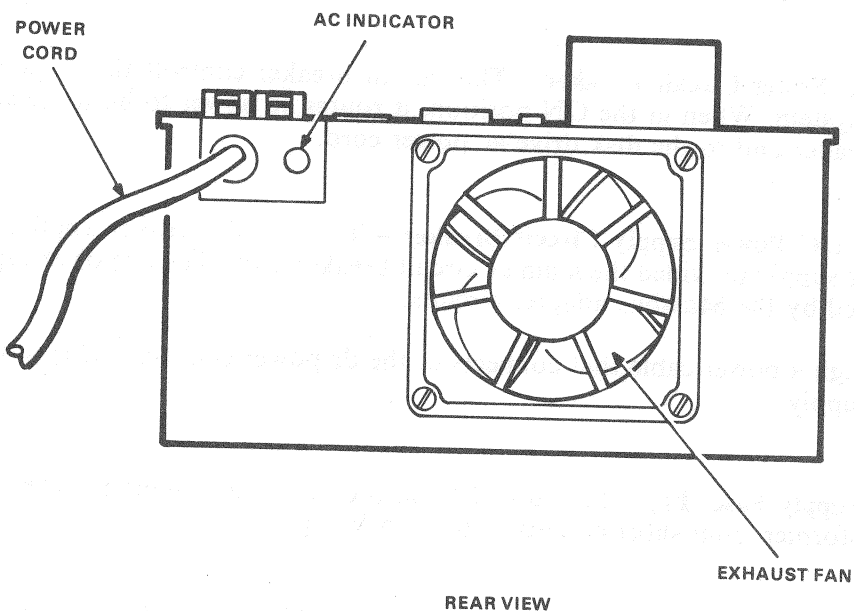
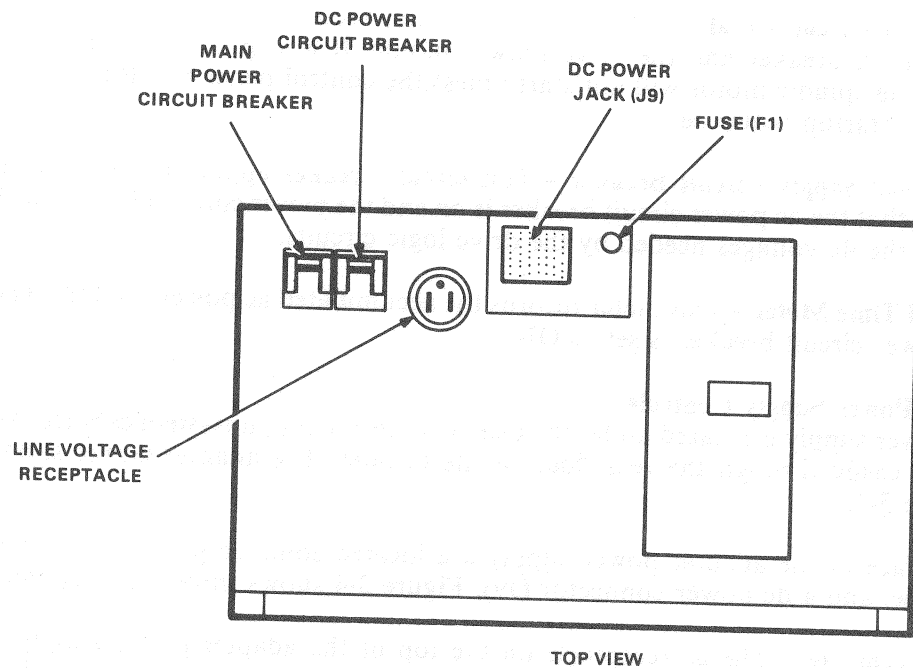
It does this through a power cable that connects to the dc power connector (J9) shown on top of the adapter power supply.

3.1.3.4 -15 V Supply Fuse (F1) – The fuse (F1) on the top of the adapter power supply is used to protect the transformer from short circuits in the -15 V supply.

3.1.3.5 AC Indicator – This light is located on the back side of the adapter power supply, in close proximity to the ac power cord. The indicator is on whenever the power cord is plugged into a source of ac power. It is a warning indicator that even though the subsystem is not energized, there is still ac voltage present up to the ac circuit breaker terminal.

3.2 DISK PACK LOADING AND DEVICE START-UP

To load a disk pack into the disk drive requires that the drive have power applied. Otherwise, the pack access cover cannot be raised due to a solenoid latch lock. If the drive is already powered on, skip over the following power application procedure and go directly to the disk pack installation (Paragraph 3.2.2).



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Figure 3-4 Adapter Power Supply Controls

3.2.1 Applying Subsystem Power

The procedures described here for energizing the disk subsystem assumes that it is connected to an ac power source as defined in the installation instructions of Chapter 2. It also assumes that the LOCAL/REMOTE switch, located on logic card A04, is set to REMOTE. The power application procedure is as follows.

- Verify that the two circuit breakers on top of the adapter power supply and the two circuit breakers on the disk drive rear panel are set to the OFF position.
- Switch on the ac power circuit breaker on the adapter power supply.
- Turn on the dc power supply breaker on the adapter power supply.
- Turn on the ac circuit breaker on the drive rear panel.
- Turn on the dc power supply circuit breaker on the drive rear panel.
- Ensure that the drive blower starts to operate and wait 2 minutes before proceeding.

CAUTION

Failure to allow blower to operate for 2 minutes before installing the disk pack will not allow sufficient purge time and may cause damage to disk pack or heads.

3.2.2 Disk Pack Installation

Assuming the drive is powered on, the disk pack must be installed prior to performing any drive operation. Disk pack installation consists of setting the pack on the drive spindle and locking the pack in place. This procedure is described in detail in the following steps.

NOTE

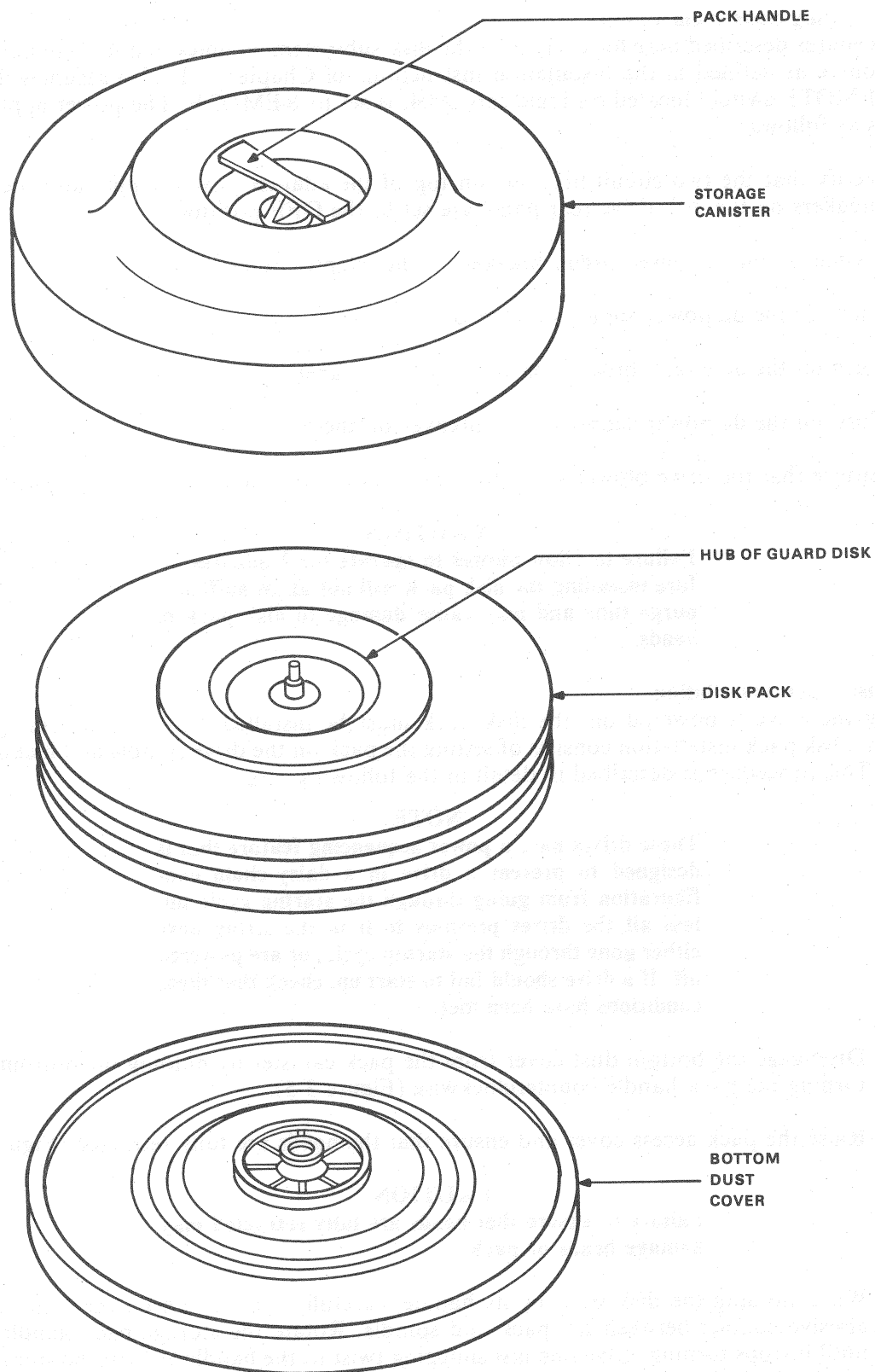
These drives have a power sequencing feature that is designed to prevent a drive in a daisy-chain configuration from going through the startup cycle unless all the drives previous to it in the string have either gone through the startup cycle, or are powered off. If a drive should fail to start up, check that these conditions have been met.

1. Disengage the bottom dust cover from the pack canister by holding the bottom cover and turning the pack handle counterclockwise (Figure 3-5).
2. Raise the pack access cover and ensure that the heads are fully retracted (Figure 3-6).

CAUTION

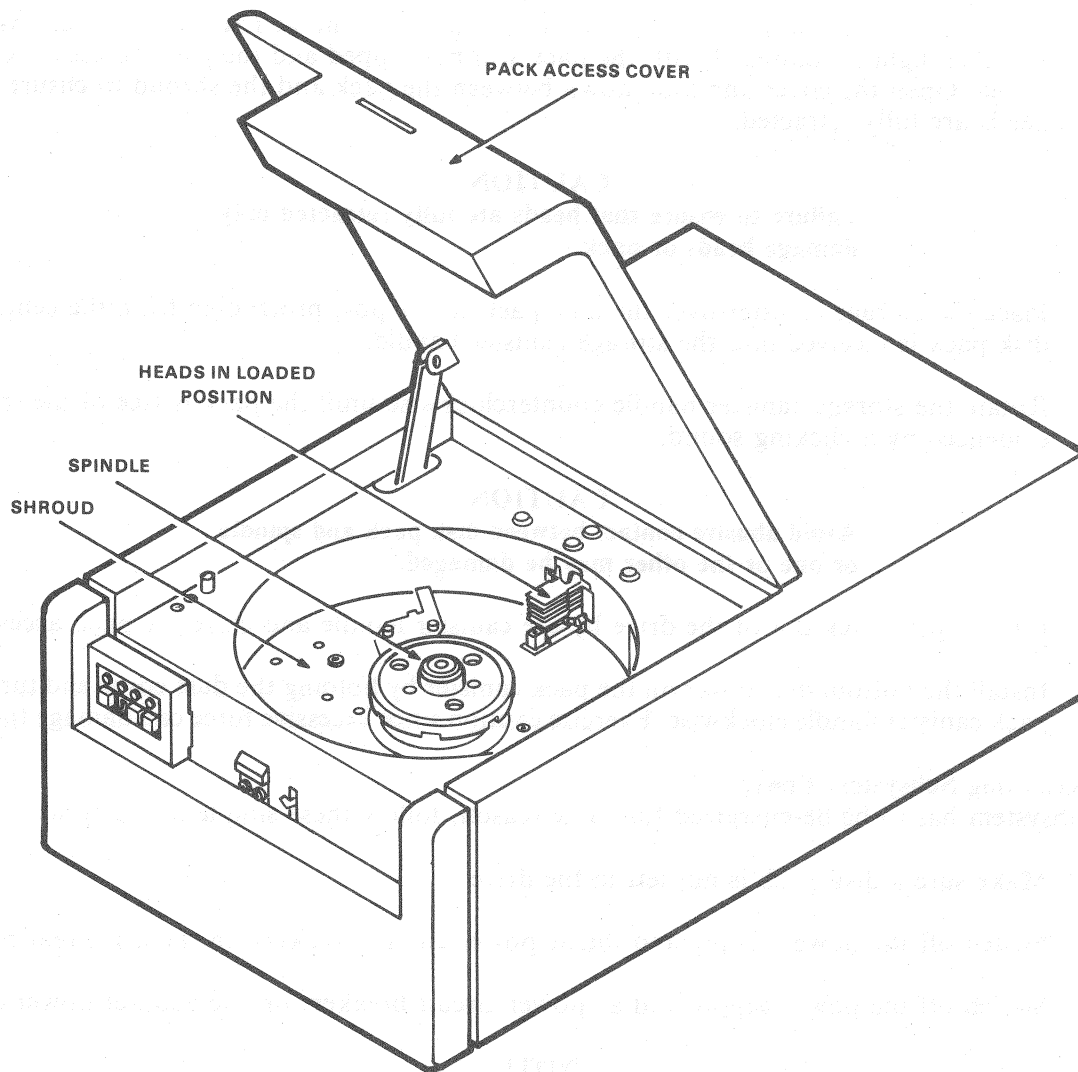
Failure to ensure that heads are fully retracted may damage heads or pack.

3. While holding the disk pack by its handle, carefully set it down on the spindle, avoiding abusive contact between the pack and spindle. Rotate the storage pack handle clockwise until it stops turning. Give one last snugging twist to the handle and lift the storage canister off the pack.
4. Set the storage canister into its bottom dust cover and set aside for later use.
5. Close the pack access cover.



MA-0612

Figure 3-5 RM03P Disk Pack



MA-0603

Figure 3-6 Pack Access Illustration

3.2.3 Startup Sequence

Once the disk pack is in place and the pack access cover is closed, press the START switch on the control panel to initiate the startup sequence. The START indicator should come on immediately. As the pack comes up to speed, the READY indicator will begin flashing at 1 second intervals. When the READY light finally remains on, the drive is then ready for operation.

3.2.4 Disk Pack Removal

Disk pack removal consists of lifting the disk pack off the spindle and storing it in its canister. To accomplish this, follow these simple procedures.

1. Press the START switch to unload the heads and stop the spindle motor. The START light will go Off immediately.

2. As the disk pack spins down, the READY light will blink at 1 second intervals. When the READY light is completely off, the pack will be stopped and the pack access cover can be raised. Open the cover and look down between the pack and the shroud to ensure that the heads are fully retracted.

CAUTION

Failure to ensure that heads are fully retracted may damage heads or pack.

3. Place the storage canister over the disk pack so the post protruding from the center of the disk pack is received into the storage canister handle.
4. Rotate the storage canister handle counterclockwise until the pack is free of the spindle as evidenced by a clicking sound.

CAUTION

Avoid abusive contact between disk pack and spindle or one or the other may be damaged.

5. Lift the disk pack out of the drive by the canister handle and close the pack access cover.
6. Install the bottom dust cover on the pack canister by holding the dust cover and turning the pack canister handle clockwise. Exercise caution since excessive force can damage the cover.

3.2.5 Removing Subsystem Power

If the subsystem has to be de-energized for some reason, follow these simple instructions.

1. Make sure a disk pack is not left in the drive.
2. Switch off the power supply and the ac power circuit breakers on the drive rear panel.
3. Switch off the power supply and ac power circuit breakers on the adapter power supply.

NOTE

The adapter power supply power cord must be removed from its power source to completely remove all ac voltages. Once this is done, the ac power indicator on the rear of the adapter power supply will go off.

3.3 OPERATOR MAINTENANCE

3.3.1 Disk Pack Storage

To ensure maximum disk pack life and reliability, observe the following precautions.

- Store disk packs in machine-room atmosphere (Table 1-7).
- If disk pack must be stored in different environment, allow 2 hours for adjustment to computer environment before use.
- Never store disk pack in direct sunlight or in dirty environment.
- Store disk packs flat, not on edge. They may be stacked with similar packs when stored.

- Always be sure that both top and bottom of storage canister are on disk pack and locked together whenever it is not actually installed in a drive.
- When marking packs, use pen or felt-tip marker that does not produce loose residue. Never use a lead pencil. Write label before it is applied to disk pack.
- Cleaning of disk surfaces is not recommended. If disks must be cleaned, the cleaning must be done by trained service personnel.
- Do not touch disk surfaces.

3.3.2 Disk Pack Handling

Because it is possible for a damaged disk pack to cause damage to the heads of a drive, or damaged heads to cause damage to a disk pack, it is important that the following be observed.

- Be aware of a sudden increase in error rate related to a specific drive or pack.
- Be aware of any unusual noise such as screeching or pinging while heads are loaded on a pack.
- Be aware of a burning odor coming from a drive.
- Be alert to the possibility of contamination such as dust, dirt, grease, oil, or smoke which could accumulate on the pack or heads.

If any of these conditions exist or if there is any doubt about the pack or drive's functional condition, call in trained service personnel.

The operator should keep a copy of the Error log Printouts on a daily basis.

CAUTION

Do not attempt to operate a suspect disk pack on another drive or operate a new disk pack on a drive with suspect heads. To do so may cause further damage.

The first part of the report is a summary of the work done during the last year.

The second part is a detailed account of the experiments carried out.

The third part is a discussion of the results.

The fourth part is a conclusion.

The work has been carried out in the laboratory of the Department of Physics, University of Cambridge.

The results of the work are given in the following tables.

The first table gives the values of the various quantities measured.

The second table gives the values of the various quantities calculated.

The third table gives the values of the various quantities derived.

The fourth table gives the values of the various quantities compared.

The fifth table gives the values of the various quantities compared.

CHAPTER 4

PROGRAMMING INSTRUCTION

4.1 BASIC SYSTEM OPERATION

The following basic decisions are made by the processor whenever a data transfer occurs.

1. Which drive is to be used and at what position on that drive is the desired data location?
2. What method is to be used to access this data location?
3. What is the direction of transfer (read or write)?

The commands generated by the processor to accomplish these decisions are applied to the system through the controller. Some of these commands are used to condition the controller circuits for the type of operation, and other commands are routed to the drive where they are used to position the heads over the correct location.

Up to eight RM03s can be connected to a single RH70 controller and up to eight RM02s can be connected to a single RH11 controller. Since all of these drives have the same Massbus address, the processor must designate to the controller which drive it wishes. Only the selected drive decodes the position commands (cylinder location, sector number, and track number) required to mechanically position its heads.

Prior to issuing the positioning commands to the drive, the processor establishes how these commands are to be executed. The drive starts its mechanical positioning after receiving the cylinder, sector, and track values plus a command containing the GO bit. The drive notifies the processor through the controller when it locates the desired position or if it could not find it. No flag is given on an implied seek in a data transfer command. If no error condition exists, the processor now initiates the data transfer sequence.

Prior to transfer data, the processor configures the controller for the following.

1. Number of data words to be transferred
2. Format of these words (16 bits/word or 18 bits/word)
3. If a write operation, the bus address of the starting memory location where data is taken from and placed on the disk
4. If a read operation, the bus address of the first memory location where data taken from the disk is to be stored
5. The method of notifying the processor at the completion of the data transfer

The processor now initiates a data transfer command which contains the GO bit and the transfer commences.

NOTE

The data transfer command may or may not contain the same position information (cylinder, sector, and track values) just previously sent to the drive.

When the heads are at the correct location and the command is a read operation, serial data is read off the disk, converted to parallel in the drive and applied onto the Massbus lines to the controller. This first word is routed through the controller to the computer bus, then to the memory location established by the processor. As successive words are read, the controller monitors the handling of each word and increments the memory address to the next location and decrements the word count for each word. The controller terminates the read operation in the drive when the word count is complete.

A write operation is very similar to a read operation. The major difference is the direction of data flow: from memory to the disk. Again, the correct disk position must be located, the number of words to be transferred must be supplied to the controller, the format must be established, and the memory location where these words are to be taken from must be determined. At the completion of a write operation the controller interrupts the processor to indicate that the data transfer is finished.

4.1.1 Computer Bus Protocol

The protocol convention used on the computer bus varies with the type of computer/controller configuration. Refer to the appropriate manuals for the correct convention used in a particular system.

4.1.2 Massbus Protocol for Control Sequences

All control communications on the Massbus interface lines between the controller and the drive must conform to the Massbus protocol sequence. The following six groups of lines establish the control sequence between the controller and the drive.

1. Drive Select lines
2. Register Select lines
3. Control lines
4. Control to Drive line
5. Demand line
6. Transfer line

These control lines are used to write control and status information into appropriate drive registers prior to a data transfer operation or are used to read status or error information from the drive registers.

NOTE

The sequence in which these lines are used is commonly referred to as the Massbus "handshake" or protocol.

4.1.3 Access to System Registers

As previously stated, the processor must condition both the controller and the drive with specific positioning and format information before any data can be transferred in the system. To accomplish these setup requirements, there are addressable registers available to the processor that can be accessed by using the proper protocol procedures and the correct address for each register.

The registers in the controller are called *local registers* and those in the drive are referred to as *remote registers*. The procedures required to read or write local registers are contained in the specific controller manual for your system. The read/write procedures for the remote registers in the drive are described in the following paragraphs.

Specific bit locations in these drive registers are designated as follows.

Read Only – Indicate that the program can read the status of these bits but cannot load them

Write Only – Indicate that the program can load them but will read back a 0

Read/Write – Indicate that the program may load them and also read them back

4.1.4 Writing A Remote Register

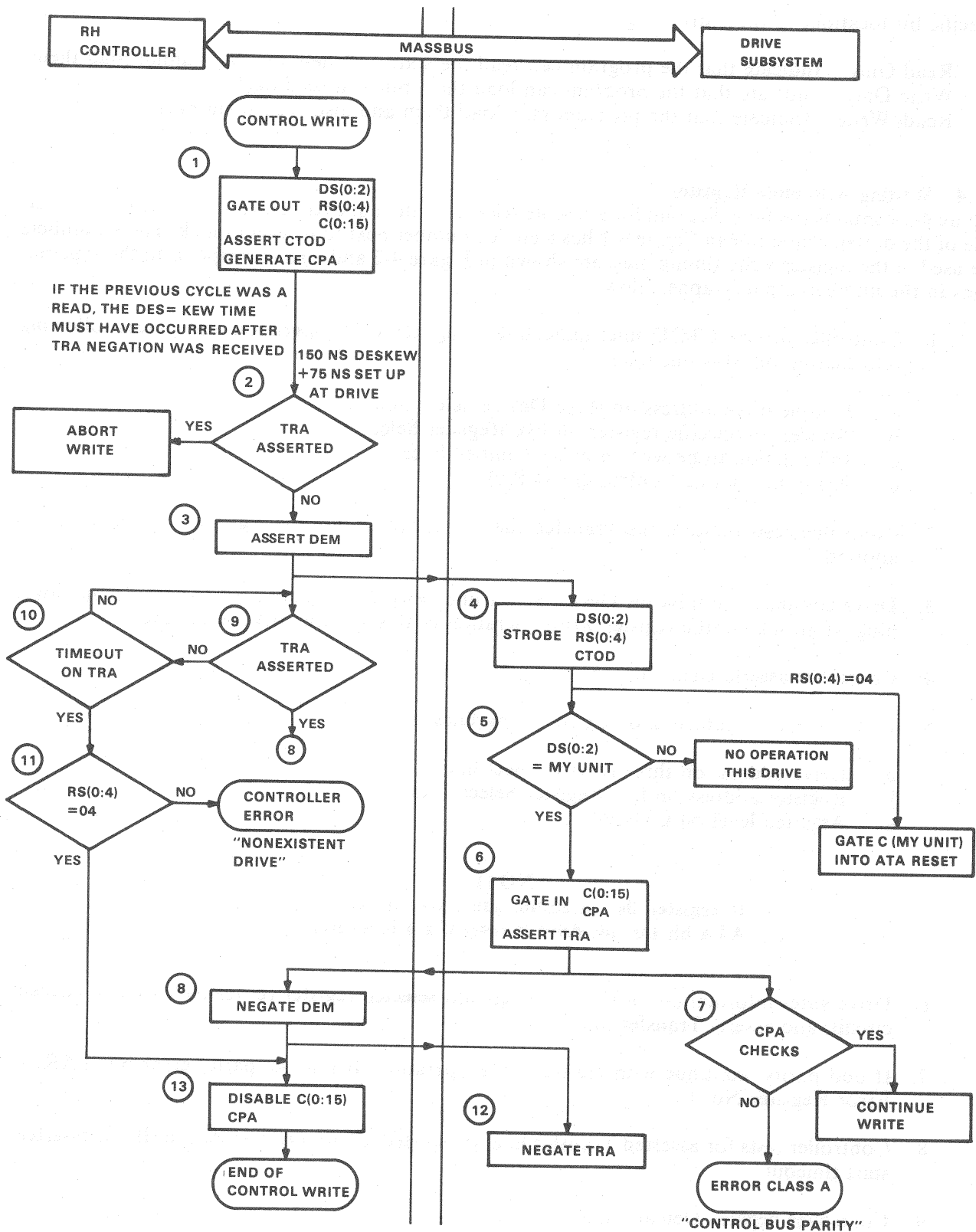
Figure 4-1 contains the flow diagram for a remote register write sequence. The events shown on the left side of the dotted center line in Figure 4-1 has a circled number next to its event block. These numbers are used in the register write timing diagram shown in Figure 4-2 and also correspond to the explanations in the numbered paragraphs below.

1. Controller asserts CTOD line, indicating a register write operation and places following information on Massbus lines:
 - a. Unique drive address on three Device Select lines
 - b. Address of specific register on five Register Select lines
 - c. Information to be written on 16 Control lines
 - d. Parity bit on one Control line (CPA).
2. Controller tests to see if the Transfer line is asserted. If yes, the register write operation is aborted.
3. Drive compares address on Device Select lines with code established by front panel logic plug. If no match, the register write operation in this specific drive terminates.
4. Controller asserts Demand line.
5. Drive strobes in information on following lines:
 - a. Drive address on three Device Select lines
 - b. Register address on five Register Select lines
 - c. Asserted level on CTOD line.

NOTE

If register 04 (attention summary) is selected, the ATA bit for this drive is reset if a 1 is written.

6. Drive gates information on Control lines into selected register routes parity bit to checker circuit, and asserts Transfer line.
7. If odd parity, continue with register write operation. If not, set parity error bit (PAR) in Error Register No. 1.
8. Controller tests for asserted Transfer line. If asserted, abort write operation. If not asserted, start timeout.
9. Controller negates Demand line.
10. If Transfer line is still not asserted by the drive at end of timeout (indicating that none of the drives recognized the device address), the controller tests to see if register 04 was selected. (No specific device address is issued with an 04 write because all drives share this register.)



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Figure 4-1 Remote Register Write Sequence Diagram

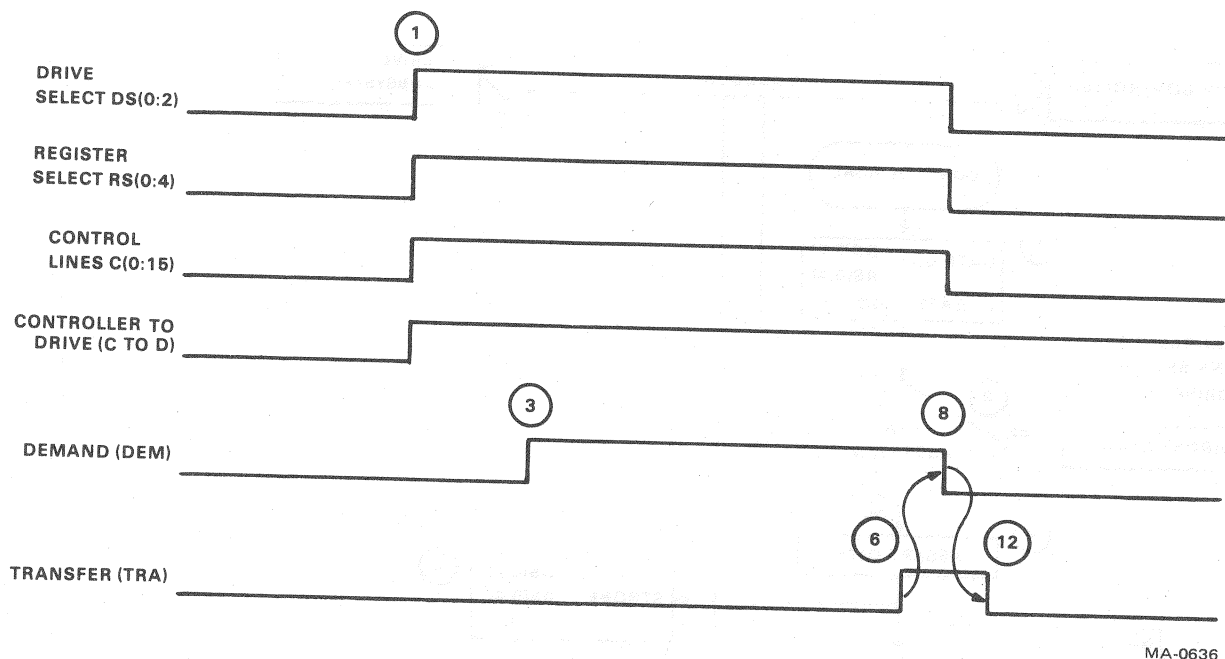


Figure 4-2 Remote Register Write Timing Diagram

11. The test for register 04 determines if the controller initiated a write into 04. The controller times out if the operation is an 04 write. If the controller times out and it is not an 04 write, then the controller addressed a nonexistent drive.
12. Drive negates Transfer line indicating that the register write operation is terminated.
13. Controller disables the data and parity bit on the Control lines. The remote-register-write sequence is finished.

4.1.5 Reading A Remote Register

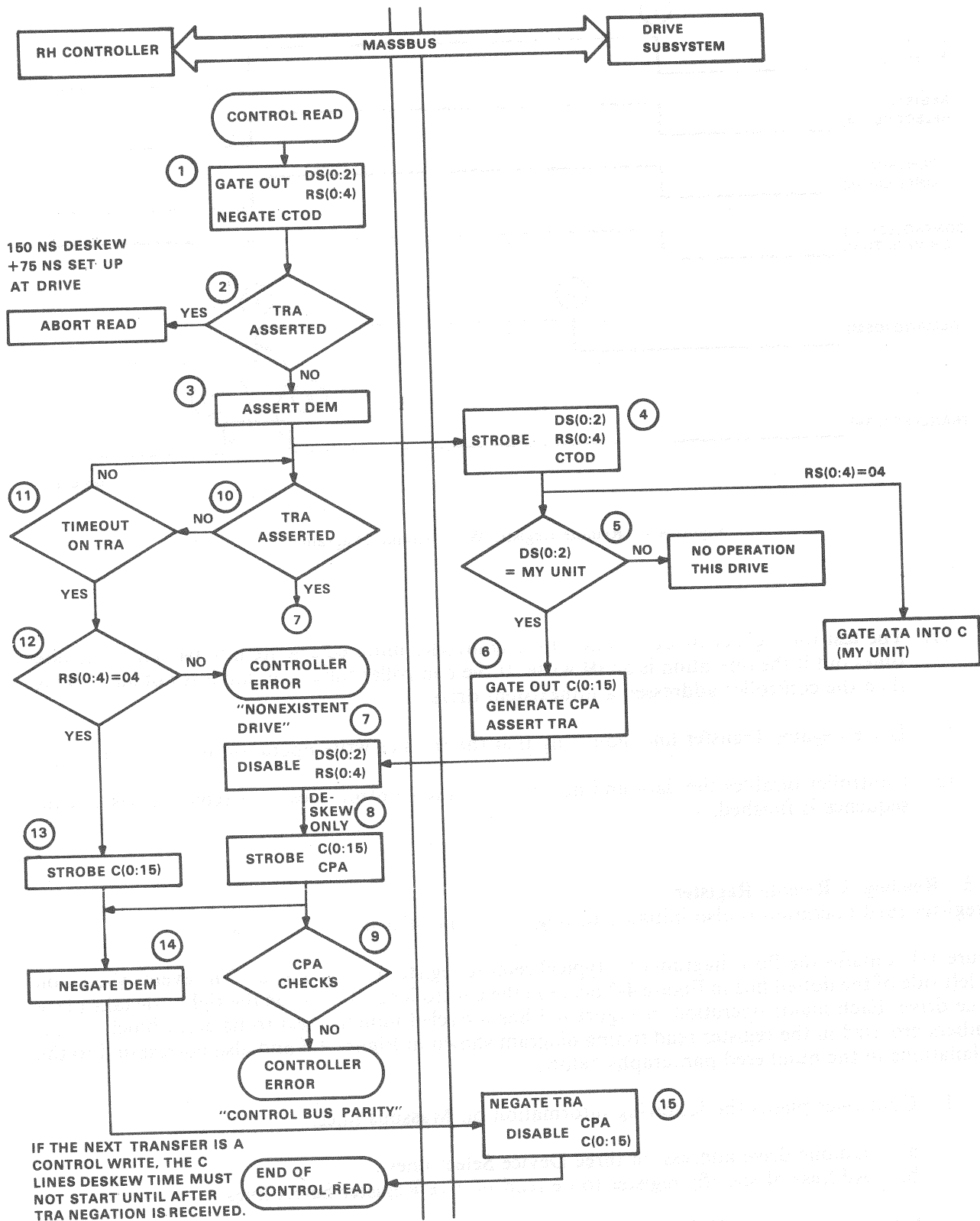
A register read operation is also initiated through the controller by the processor.

Figure 4-3 contains the flow diagram of a typical remote register read sequence. The events shown on the left side of the dotted line in Figure 4-3 occur in the controller and those on the right side take place in the drive. Each major operation in Figure 4-3 has a circled number next to its event block. These numbers are used in the register read timing diagram shown in Figure 4-4 and also correspond to the explanations in the numbered paragraphs below.

1. Controller places the following information on Massbus lines:
 - a. Unique drive address on three Device Select lines
 - b. Address of specific register to be read on five Register Select lines

Controller negates CTOD line, indicating a register read operation.

2. Controller tests to see if Transfer line is asserted. If yes, the register read operation is aborted.



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Figure 4-3 Remote Register Read Sequence Diagram

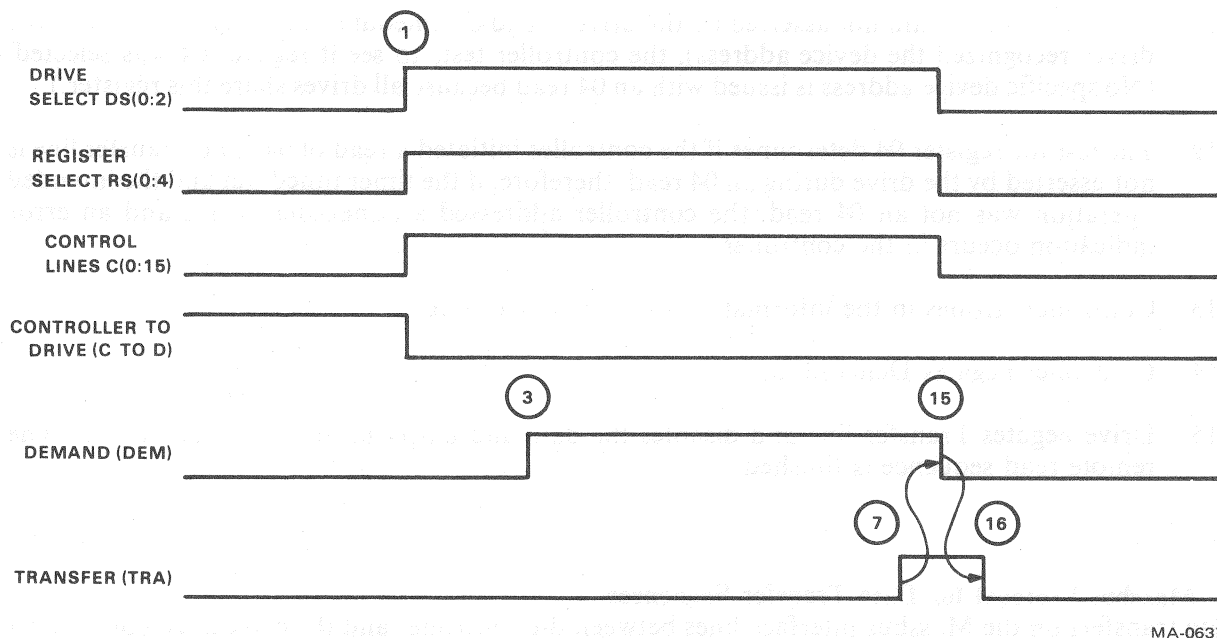


Figure 4-4 Remote Register Read Timing Diagram

3. Drive compares address on Device Select lines with code established by front panel logic plug. If no match, the register read operation in this specific drive is terminated.
4. Controller asserts Demand line.
5. Drive strobes in information on following lines:
 - a. Drive address on three Device Select lines
 - b. Register address on five Register Select lines
 - c. Negated level on CTOD line.

4. Controller asserts Demand line.

5. Drive strobes in information on following lines:

- Drive address on three Device Select lines
- Register address on five Register Select lines
- Negated level on CTOD line.

- b. Register address on five Register Select lines

- c. Negated level on CTOD line.

NOTE

If register 04 (attention summary) is selected, the status of this register is gated onto the Control line that corresponds to the device select address of the drive.

6. Drive gates information in selected register onto the Control lines, generates the parity bit, and asserts Transfer line.
7. Controller disables the addresses on the Device Select and Register Select lines.
8. Controller strobes in information and parity bit on Control lines.
9. Controller tests for odd parity. If not, the controller sets the control bus parity error indicator.
10. Controller tests for asserted Transfer line. If asserted, the read operation is aborted. If not asserted, timeout is started.

7. Controller disables the addresses on the Device Select and Register Select lines.

8. Controller strobes in information and parity bit on Control lines.

9. Controller tests for odd parity. If not, the controller sets the control bus parity error indicator.

10. Controller tests for asserted Transfer line. If asserted, the read operation is aborted. If not asserted, timeout is started.

11. If Transfer line is still not asserted by the drive at end of timeout (indicating that none of the drives recognized the device address), the controller tests to see if register 04 was selected. (No specific device address is issued with an 04 read because all drives share this register.)
12. The test for register 04 determines if the controller initiated a read of 04. The Transfer line is not asserted by the drive during an 04 read; therefore, if the timer timed out and the intended operation was not an 04 read, the controller addressed a nonexistent drive and an error indication occurs in the controller.
13. Controller strobes in the information on the Control lines.
14. Controller negates Demand lines.
15. Drive negates Transfer line and disables the data and parity bit on the Control lines. The remote read sequence is finished.

4.1.6 Massbus Protocol for Data Transfer Sequences

All data transfers on the Massbus interface lines between the controller and the drive must conform to the Massbus protocol sequence. The following six groups of lines establish the data transfer sequence between the controller and the drive.

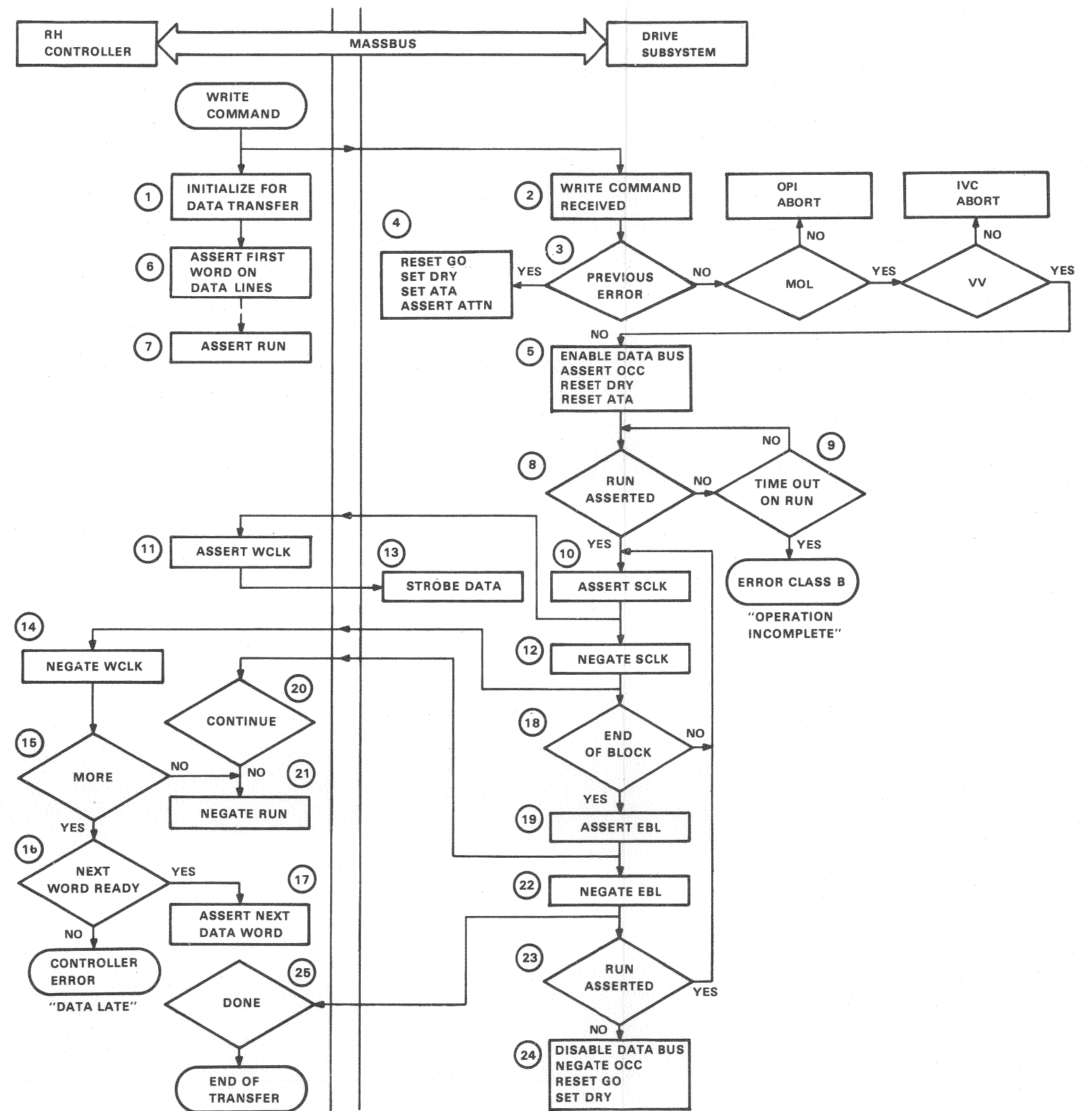
1. Run line
2. Occupied line
3. Sync Clock line
4. End of Block line
5. Data lines
6. Write Clock line

These lines are used when data is read or written and transferred over the Massbus interface to the controller.

4.1.7 Massbus Write Data Sequence

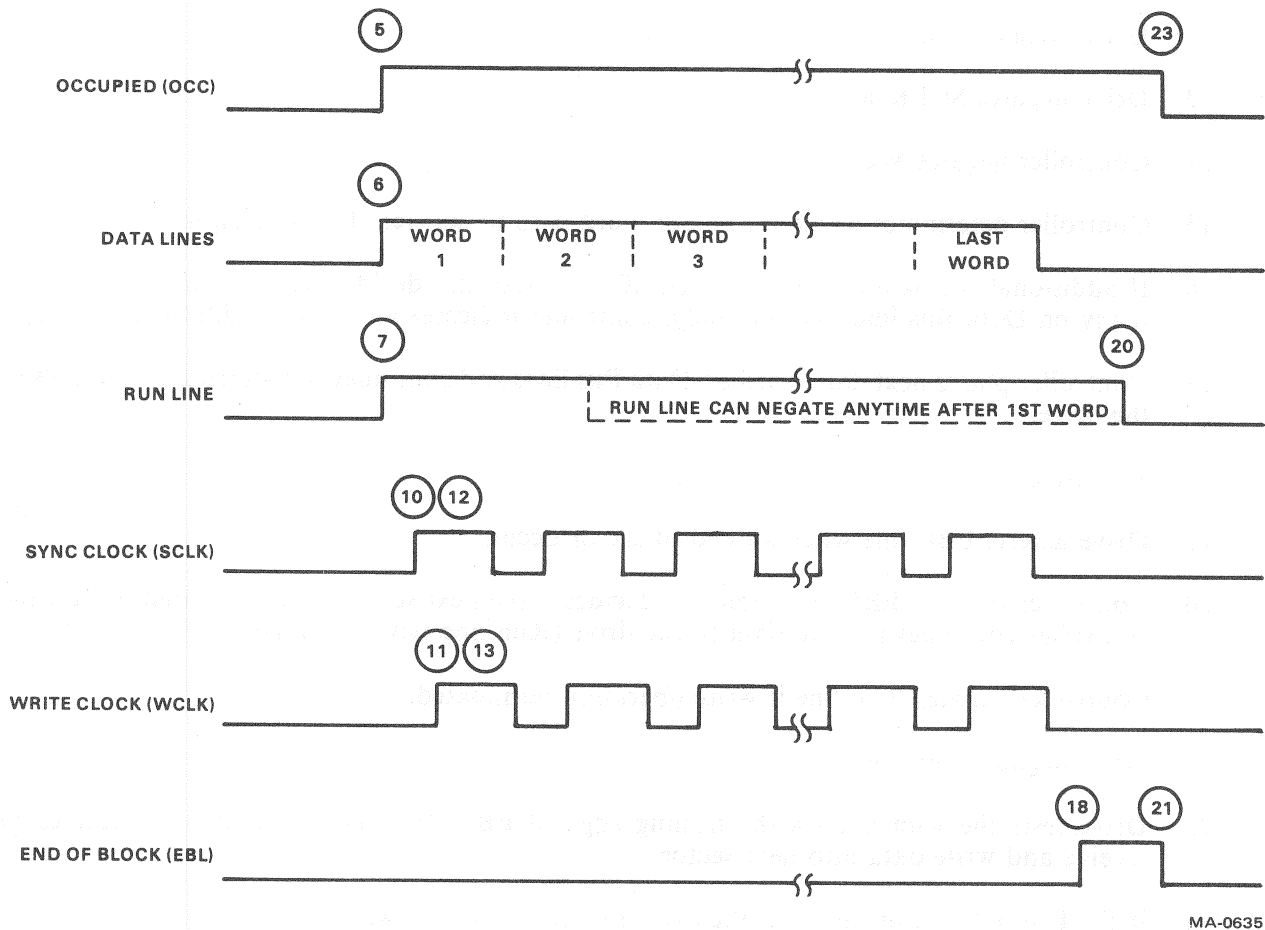
Figure 4-5 contains the flow diagram for the Massbus sequence as data is transferred from the controller and written on the disk in the drive. The events shown on the left side of the dotted center line occur in the controller and those on the right take place in the drive. Each major operation in Figure 4-5 has a circled number next to its event block. These numbers are used in the write data timing diagram shown in Figure 4-6 and also correspond to the explanations in the numbered paragraphs below.

1. Controller prepares for a data transfer operation from the controller to the drive.
2. Drive decodes valid write command and starts sequencer.
3. Drive tests for error conditions in drive.
4. If error exists, the drive performs the following:
 - a. Resets GO bit
 - b. Sets drive ready (DRY) bit (07) in drive status register
 - c. Sets attention active (ATA) bit (15) in drive status register
 - d. Asserts Attention line.



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Figure 4-5 Massbus Write Data Transfer Sequence Diagram



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Figure 4-6 Massbus Write Data Transfer Timing Diagram

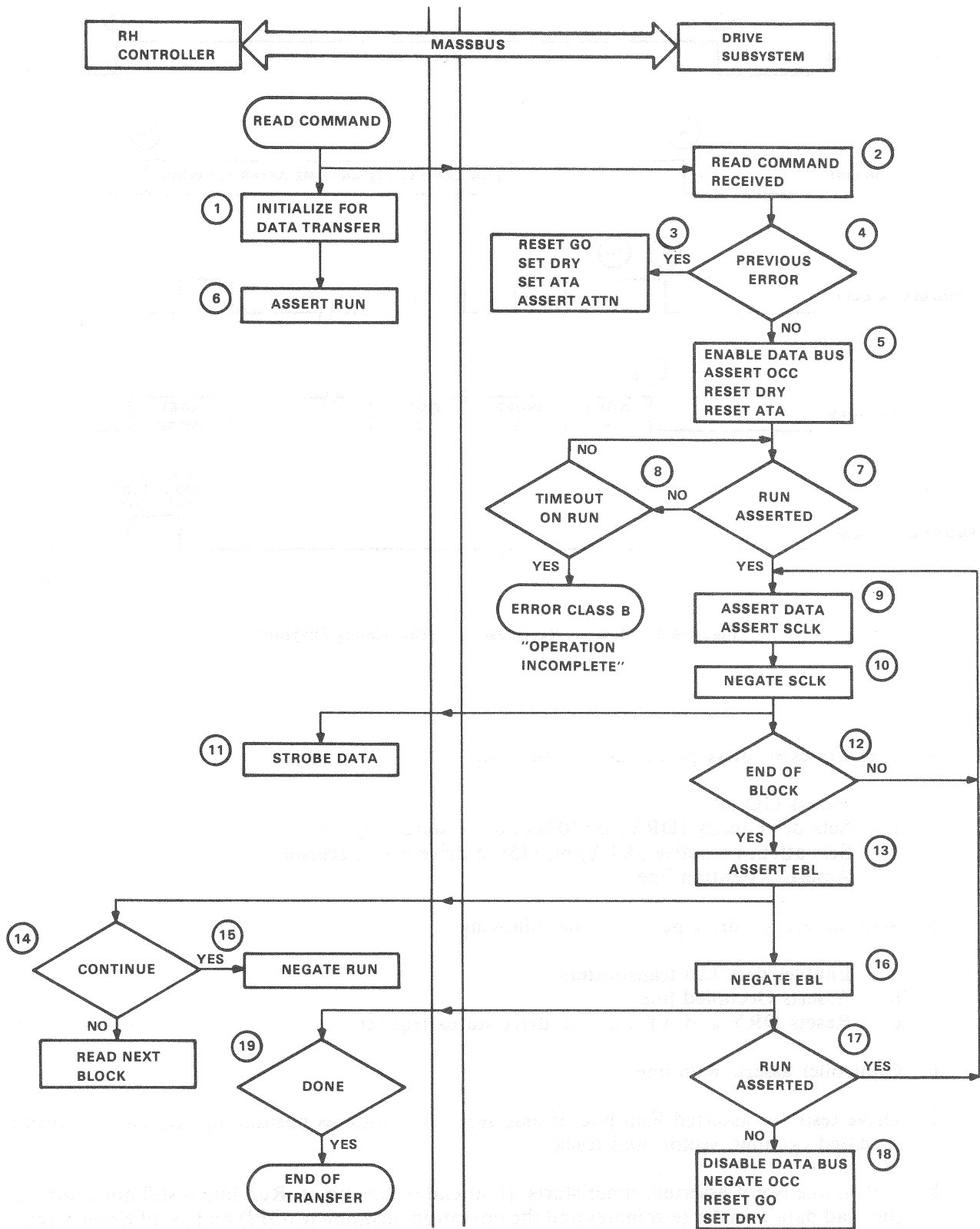
5. With no errors, the drive performs the following:
 - a. Enables data bus receivers
 - b. Asserts Occupied line
 - c. Resets DRY and ATA bits in drive status register.
6. Controller places first word to be written on Data Bus lines to the drive.
7. Controller asserts Run line.
8. Drive tests for asserted Run line. If asserted, drive initiates positioning sequence to locate specific cylinder, sector, and track.
9. If Run line is not asserted, timeout starts. If, at end of timeout, Run line still not asserted, the write data transfer terminates and the operation incomplete (OPI) bit (13) of Error Register No. 1 is set.
10. When the drive is ready to accept first data word, it asserts Sync Clock (SCLK) line.
11. Controller receives the SCLK assertion and asserts the Write Clock (WCLK) line.

12. Drive strobes in first word to be written.
13. Drive negates SCLK line.
14. Controller negates WCLK.
15. Controller determines whether another word is to be written. If not, Run line is negated.
16. If additional words are to be transferred, the controller decides whether the next word is ready on Data Bus lines. If not ready, controller indicates an error condition (data late).
17. Controller places next data word on Data Bus lines and continues transferring data words to the drive.
18. The drive transfers 256 words of data.
19. Drive asserts EBL line when an end of sector occurs.
20. Controller receives EBL assertion and decides if the next sector is to be written. If yes, the controller continues to send data to the drive (Run line remains active).
21. Controller negates Run line if write operation terminated.
22. Drive negates EBL line.
23. Drive tests the Run line on the trailing edge of EBL. If asserted, the drive continues to receive and write data into next sector.
24. If the Run line is not asserted, the drive performs the following:
 - a. Disables the transceivers on the Data Bus lines
 - b. Negates the Occupied line
 - c. Resets the GO bit
 - d. Sets the DRY bit.
25. When the controller receives the negated EBL line, it determines whether another operation is to be performed on this drive or if an end-of-transfer interrupt should be sent to the processor.

4.1.8 Massbus Read Data Sequence

Figure 4-7 contains the flow diagram for the Massbus sequence as data is transferred from the drive to the controller. The events shown on the left side of the dotted center line occur in the controller and those on the right take place in the drive. Each major operation in Figure 4-7 has a circled number next to its event block. These numbers are used in the read data timing diagram shown in Figure 4-8 and also correspond to the explanations in the numbered paragraphs below.

1. Controller prepares for data transfer operation from drive to controller.
2. Drive decodes valid command and starts sequencer.
3. Drive tests for error conditions in drive.



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Figure 4-7 Massbus Read Data Transfer Flow Diagram

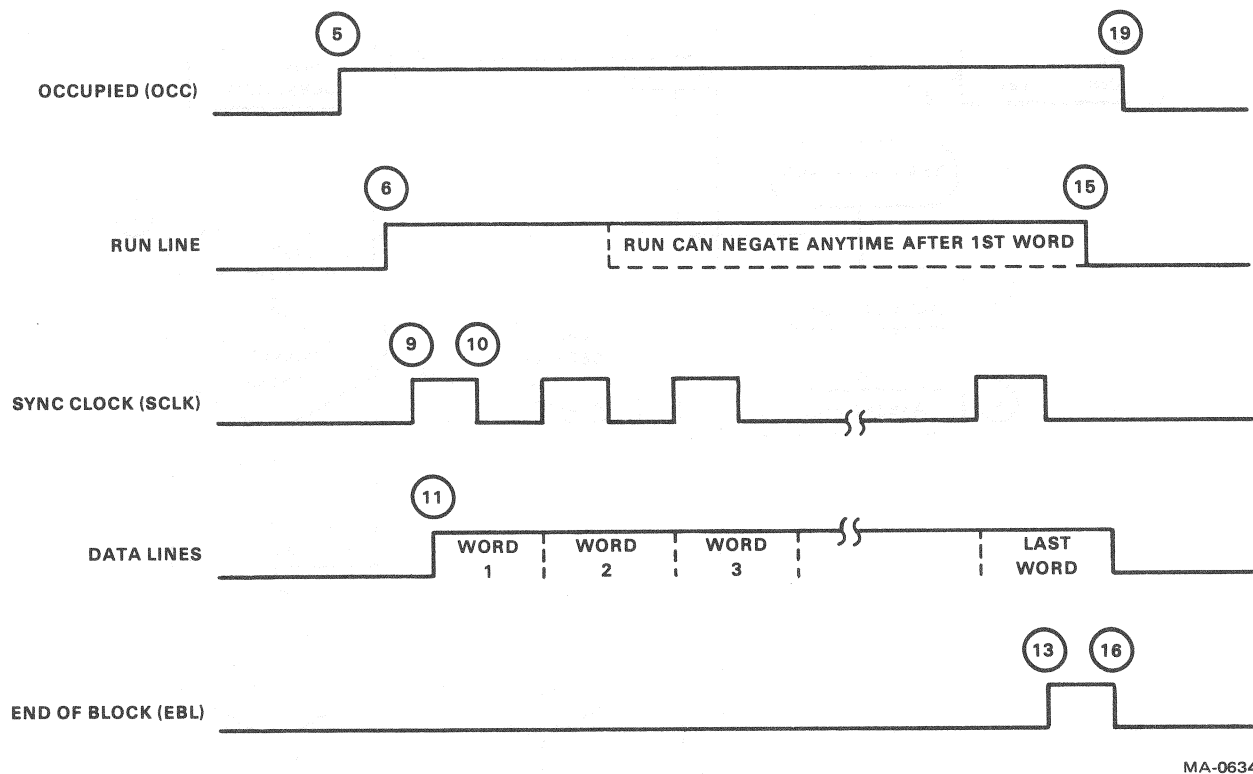


Figure 4-8 Massbus Read Data Transfer Timing Diagram

4. If errors exist, drive performs the following:
 - a. Resets GO bit
 - b. Sets drive ready (DRY) bit (07) in drive status register
 - c. Sets attention active (ATA) bit (15) in drive status register.
 - d. Asserts Attention line.
5. With no errors, drive performs the following:
 - a. Enables data bus transmitters
 - b. Asserts Occupied line
 - c. Resets DRY and ATA bits in drive status register.
6. Controller asserts Run line.
7. Drive tests for asserted Run line. If asserted, drive initiates positioning sequence to locate specified cylinder, sector, and track.
8. If Run line is not asserted, timer starts. If, at end of this timer, Run line is still not asserted, the read data transfer terminates and the operation incomplete (OPI) bit (13) of Error Register No. 1 is set.
9. After the drive has found the correct location, the first data word and a parity bit is placed on the Data lines. The drive asserts the Sync Clock (Sync) line.

10. After half a word time for the sync clock assertion to reach the controller the drive negates the Sync Clock line.
11. Upon receipt of the Sync Clock line negation, the controller strobes in the first word and parity bit on the Data lines. The controller tests for odd parity.
12. Drive tests for end of data block. If not, next data word is placed on Data Bus lines to the controller.
13. If, at end of block (256 data words transferred), End of Block (EBL) line is asserted.
14. Controller tests to determine whether next sector is to be read. If continue, controller keeps Run line asserted.
15. If controller determines to terminate the data transfer, it negates the Run line.

NOTE

The controller negates the Run line after the specified number of data words have been transferred. It does not wait until the end of the sector. The drive only tests the Run line at the end of a sector, and therefore transfers data in sector-length increments not in words or partial blocks.

16. Drive negates EBL line.
17. Drive tests Run line. If asserted, continues to transfer data in next sector.
18. If not asserted, the drive performs the following:
 - a. Disables the transceivers on the Data Bus lines
 - b. Negates the Occupied line
 - c. Resets the GO bit
 - d. Sets the DRY bit.

4.2 PROGRAMMING OVERVIEW

Twenty-two registers are used by the drive and the controller to communicate control commands, status data, error conditions, and maintenance information. Sixteen registers are located in the drive and the remaining are located in the various controllers that are used as a Massbus interface.

Table 4-1 contains these 22 registers, their mnemonics, Unibus and Massbus addresses, whether they are read only or read/write, and their basic function. Figure 4-9 contains the bit assignment summary of these registers.

4.2.1 Controller Registers

Six of the 22 registers required for drive operation are located in the controllers. The RH11 controller contains the following registers.

RMWC	Word Count
RMBA	Bus Address
RMCS2	Control and Status 2
RMDB	Data Buffer

Table 4-1 Controller and Drive Registers

Register Name	Unibus Address	Massbus Address	Mode	Function
RMCS1 Control	776700	00*	Read/Write	Contains function code, GO bit
RMWC Word Count	776702	*	Read/Write	Contains 2's complement of number of words to be transferred
RMBA Bus Address	776704	*	Read/Write	Contains memory address of location where data transfer is to begin
RMDA Desired Sector/Track Address	776706	05	Read/Write	Contains disk sector and track address where transfer is to occur
RMCS2 Status	776710	*	Read/Write	Contains controller status indication
RMDS Drive Status	776712	01	Read Only	Contains all non-error status plus error summary bit
RMER1 Error No. 1	776714	02	Read/Write	Contains individual error indications
RMAS Attention Summary	776716	04	Read/Write	Contains 1-bit-per-drive attention summary status
RMLA Look-Ahead	776720	07	Read Only	Contains current sector address under heads
RMDB Data Buffer	776722	*	Read Only	Contains input and output connection to silo for maintenance
RMMR1 Maintenance No. 1	776724	03	Read/Write	Contains diagnostic test functions
RMDT Drive Type	776726	06	Read Only	Contains drive character indications
RMSN Serial Number	776730	10	Read Only	Contains lowest four digits of drive serial number
RMOF Offset	776732	11	Read/Write	Contains bit for control of offset of drive heads
RMDC Desired Cylinder	776734	12	Read/Write	Contains address of cylinder for seek operation
RMHR Holding	776736	13	Read/Write	Not used; contents always all 0s

*Controller registers (RMCS1 is shared by drive and controller).

Table 4-1 Controller and Drive Registers (Cont)

Register Name	Unibus Address	Massbus Address	Mode	Function
RMMR2 Maintenance No. 2	776740	14	Read Only	Contains diagnostic test functions
RMER2 Error No. 2	776742	15	Read/Write	Contains drive error bits
RMEC1 ECC Position	776744	16	Read Only	Contains position of error burst
RMEC2 ECC Pattern	776746	17	Read/Only	Contains the error burst
RMBAE Bus Address	776750	*	Read/Write	Contains the bus address extension bits
RMCS Control and Status	776752	*	Read/Write	Contains status and error indications

*Controller registers (RMCS1 is shared by drive and controller).

1. The following information is being furnished to you for your information and use only. It is not to be distributed outside your organization.

Item	Quantity	Unit Price	Total Price
1.000	1.000	1.000	1.000
2.000	2.000	2.000	2.000
3.000	3.000	3.000	3.000
4.000	4.000	4.000	4.000
5.000	5.000	5.000	5.000
6.000	6.000	6.000	6.000
7.000	7.000	7.000	7.000
8.000	8.000	8.000	8.000
9.000	9.000	9.000	9.000
10.000	10.000	10.000	10.000

1. The following information is being furnished to you for your information and use only. It is not to be distributed outside your organization.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMCS1 (776700) 00	SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	G0	R/W
RMWC (776702) RH	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC 0	R/W
RMBA (776704) RH	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 9	BA 8	BA 7	BA 6	BA 5	BA 4	BA 3	BA 2	BA 1	BA 0	R/W
RMDA (776706) 05	0	0	0	TA 16*	TA 8*	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	R/W
	*RESERVED																
RMCS2 (776710) RH	DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0	R/W
RMDS (776712) 01	ATA	ERP	PIP	MOL	WRL	LBT	PGM	DPR	DRY	VV	0	0	0	0	0	OM	R
RMER1 (776714) 02	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	R/W
RMAS (776716) 04	0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0	R/W
RMLA (776720) 07	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	0	R
RMDB (776722) RH	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	R
RMMR1 (776724) 03	OCC	R/G	EBL	REX	ESRC	PLFS	ECRC	PDA	PHA	CONT	WC	EECC	WD	LS	LST	DMD	R
	DBCK	DBEM	DEBL	MSEN	MCLK	MRD	MUR	MOC	MSER	MDF	MS	DTG	MWP	MI	MSC	DMD	W

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
RMDT (776726) 06	0	0	MOH 1	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	R
RMSN (776730) 10	SN 8000	SN 4000	SN 2000	SN 1000	SN 800	SN 400	SN 200	SN 100	SN 80	SN 40	SN 20	SN 10	SN 8	SN 4	SN 2	SN 1	R
RMOF (776732) 11	0	0	0	FMT 16	ECI	HCI	0	0	OFF DIR	0	0	0	0	0	0	0	R/W
RMDC (776734) 12	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	R/W
RMHR (776736) 13	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W
RMMR2 (776740) 14	RQA	RQB	TAG	TEST BIT	CIC	CIH	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	R
RMER2 (776742) 15	BSE	SKI	OPE	IVC	LSC	LBC	0	0	DVC	0	0	0	DPE	0	0	0	R/W
RMEC1 (776744) 16	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	R
RMEC2 (776746) 17	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	R
RMBAE (776750) RH	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16	R/W
RMCS3 (776752) RH	APE	DPE HI	DPE LO	WCE HI	WCE LO	DBL	0	0	0	IE	0	0	IPCK 3	IPCK 2	IPCK 1	IPCK 0	R/W

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Figure 4-9 Register Summary

The RH10, RH20, and RH70 controllers contain all of these, plus the RMBAE (bus address extension) and RMCS3 (control and status 3) registers.

The following paragraphs describe the controller registers.

4.2.1.1 Control Register (RMCS1) – This read/write register is shared by both the RH controller and the drive. The bits assigned to the RH controller contain the operational status of overall system. Table 4-2 provides a description of these bits.

Table 4-2 Control Register (RMCS1) Bit Assignments Used by RH Controller

Name/Type	Set By/Cleared By	Description
Bit 00-05 Not used by RH controller		Used by drive (See Table 4-9 for description.)
Bit 06 IE (Interrupt Enable) Read/Write	IE is a control bit that can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	A program-controlled interrupt may occur by writing 1s into IE and RDY at the same time.
Bit 07 RDY (Ready) Read Only	This bit is normally set except during data transfers when it is reset.	When a data transfer command code (51-73) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set.
Bits 08, 09, A16, A17 (Unibus Address Extension Bits) Read/Write	Upper extension bits of the RMBA register. Cleared by INIT, controller clear, or by writing 0s in these bit positions.	These control bits cannot be modified while the RH controller is performing a data transfer (RDY negated).
Bit 10 PSEL (Port Select) Read/Write	When PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, controller clear, or by writing a 0 in this bit position.	A Unibus select control bit, this bit cannot be modified while the RH controller is performing a data transfer (RDY negated).
Bit 11 Not used by RH controller		Used by drive. (See Table 4-9 for description.)
Bit 12 Not used by either RH controller or drive	Always read as 0	

Table 4-2 Control Register (RMCS1) Bit Assignment Used by RH Controller (Cont)

Name/Type	Set By/Cleared By	Description
Bit 13 MCPE (Massbus Control Bus Parity Error) Read Only	Set by parity error on Massbus control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, controller clear, RH error clear, or by loading a data transfer command with the GO bit set.	Parity errors that occur on the Massbus control bus while writing a drive register are detected by the drive and cause the PAR error (RMER1 register, bit 03) to set.
Bit 14 TRE (Transfer Error) Read/Write	Set if any of the following conditions occur. 1. Data late (RMCS2 bit 15 is set.) 2. Write check error (RMCS2 bit 14 is set.) 3. Unibus parity error (RMCS2 bit 13 is set.) 4. Nonexistent drive (RMCS2 bit 12 is set.) 5. Nonexistent memory (RMCS2 bit 11 is set.) 6. Program error (RMCS2 bit 10 is set.) 7. Missed transfer (RMCS2 bit 9 is set.) 8. Massbus data bus parity error (RMCS2 bit 8 is set.) 9. Drive error occurs during a data transfer. Cleared by Unibus A INIT, controller clear, or by loading a data transfer command with GO bit set.	
Bit 15 SC (Special Condition) Read Only	Set by TRE or ATTN or Massbus control parity error. Cleared by Unibus A INIT, controller clear, or by removing the ATTN condition.	

4.2.1.2 Word Count Register (RMWC) – The word count register is located in the controller. This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented by 1 each time a word is transmitted to or from memory. A maximum of 65,535 words can be transferred at one time. Table 4-3 provides a description of each bit.

4.2.1.3 Address Register (RMBA) – This device register is used by the controller to address the memory location in which a transfer is to take place.

The RMBA register forms the lower 16 bits of address which combine with bit 09 and 08 of the control register RMCS1 to create the 18-bit memory address. This register is loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented by 2. If the BAI (bus address increment inhibit) bit (bit 03 of RMCS2) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address. Table 4-4 provides a description of each bit.

Table 4-3 Word Count Register (RMWC)

Name/Type	Set By/Cleared By	Description
Bit 00–15 WC (Word Count) Read/Write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it.	Incremented for each data transfer.

Table 4-4 Address Register (RMBA) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00 Not used	Always read as a 0.	
Bit 01–15 BA (Bus Address) Read/Write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by controller clear.	The BA register is incremented by 2 by the controller after each transfer of a word to or from memory.

4.2.1.4 Status Register (RMCS2) – This read/write register indicates the status of the controller and contains the drive unit number. The unit number specified in bits 00 through 02 of this register indicates which of the possible eight drives is selected. Table 4-5 provides a description of each bit.

Table 4-5 Status Register (RMCS2) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–02 U (Unit Select) Read/Write	These bits are written by the program to select a drive. Cleared by Unibus A INIT or controller clear.	The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The drive registers contain bits that come from the selected drive.
Bit 03 BAI (Unibus Address Increment Inhibit) Read/Write	When BAI is set, the RH controller will not increment the RMBA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by Unibus A INIT or controller clear.	When set during a data transfer, all data words are read from or written into the same memory location.
Bit 04 PAT (Parity Test) Read/Write	While PAT is set, the controller generates even parity on both the control bus and data bus of the Massbus. When clear, odd parity is generated. Cleared by Unibus A INIT or controller clear.	While PAT is set, the controller checks for even parity received on the data bus but not on the control bus.
Bit 05 CLR (Controller Clear) Write Only	When a 1 is written into this bit, the controller and all drives are initialized.	Unibus A INIT also causes Controller Clear to occur.
Bit 06 IR (Input Ready) Read Only	Set when a word may be written in the RMDB register by the program. Cleared by reading the RMDB register.	Serves as a status indicator for diagnostic check of the silo buffer. An attempt to write the RMDB register before IR is asserted will cause a data late error (bit 15 of this register sets).
Bit 07 OR (Output Ready) Read Only	Set when a word is present in RMDB and can be read by the program. Cleared by Unibus A INIT, controller clear, or by reading the RMDB register.	Serves as a status indicator for diagnostic check of the silo buffer. An attempt to read the RMDB register before OR is asserted will cause a data late error (bit 15 of this register sets).
Bit 08 MDPE (Massbus Data Bus Parity Error) Read Only	Set when a parity error occurs on the Massbus data bus while doing a read or write-check operation. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	MDPE causes a transfer error (bit 14 of RMCS1 sets). Parity errors on the Massbus data bus during write operations are detected by the drive and cause the PAR error (RMER1 register, bit 03).

Table 4-5 Status Register (RMCS2) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 09 MXF (Missed Transfer) Read/Write	Set if the drive does not respond to a data transfer command within 250 ms. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	MXF causes a transfer error (bit 14 of RMCS1 sets). This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive that has ERR (bit 14 of RMDS set) or if the drive fails to initiate the command for any reason (such as a parity error).
Bit 10 PGE (Program Error)	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	PGE causes a transfer error (bit 14 of RMCS1 sets). The data transfer command code is inhibited from being written.
Bit 11 NEM (Nonexistent Memory) Read Only	Set when the controller is performing a DMA transfer and the memory address specified in RMBA is nonexistent (does not respond to MYSN within 10 μ s). Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	NEM causes a transfer error (bit 14 of RMCS1 sets). The RMBA contains the address +2 of the memory location causing the error.
Bit 12 NED (Nonexistent Drive) Read Only	Set when the program reads or writes a drive register in a drive [selected by U (00:02)] that does not exist or is powered-down. (The RM03 fails to assert TRA within 1.5 μ s after assertion of DEM.) Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	NED causes a transfer error (bit 14 of RMCS1 sets).
Bit 13 UPE (Unibus Parity Error) Read/Write	Set if the Unibus parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	UPE causes a transfer error (bit 14 of RMCS1 sets). When the Unibus is selected to do 18-bit data transfers, the UPE error is disabled. When a Unibus parity error occurs, the RMBA register contains the address +2 of the memory word with the parity error [if BAI (bit 03 of this register) is not set]. This bit may be set by program control for diagnostic purposes.

Table 4-5 Status Register (RMCS2) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 14 WCE (Write Check Error) Read Only	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command with GO set.	WCE causes a transfer error (bit 14 of RMCS1 sets). If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RMBA (and extension) is the address of the word following the one that did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RMDB).
Bit 15 DLT (Data Late) Read Only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, controller clear, RH error clear, or loading a data transfer command GO set.	DLT causes a transfer error (bit 14 of RMCS1 sets). Buffering is 66 words deep in the controller. Can also be set by the program reading or writing the RMDB register.

4.2.1.5 Data Buffer Register (RMDB) – This read/write register is used to monitor the silo data buffer in the RH controller. If the program attempts to write into the data buffer while it is full or read the data buffer when it is empty, a data late (DLT) error occurs (bit 15 of RMCS2 is set). The RMCS2 register also provides status indicators showing whether the data buffer can be read or written. When RMCS2 bit 6 (IR) is set, the data buffer can be written. When RMCS2 bit 7 (OR) is set, the data buffer can be read.

The RMDB register can be read and written only as an entire word. Any attempt to write a byte will cause an entire word to be written. Reading the RMDB register is a “destructive” readout operation: The top data word in the silo buffer is removed by the action of reading the RMDB and a new data word (if present) replaces it a short time later. The action of writing the RMDB register causes one more data word to be inserted into the silo buffer (if it was not full). Table 4-6 provides a description of each bit.

4.2.1.6 Bus Address Extension Register (RMBAE) – The RMBAE register contains the upper 6 bits of the memory address which combine with the lower 16 bits located in RMBA register to form the complete 22 bit address. This register is loaded by the program in conjunction with the RMBA register to specify the starting memory address of a data transfer operation. The 6-bit field is incremented (decremented for specific function codes) each time a carry (borrow) occurs from the RMBA register during memory transfers.

Table 4-6 Data Buffer Register (RMDb) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-15 DB (Data Buffer) Read/Write	When read, the contents of a controller register are available. Upon completion of the read, the next sequential word in the silo will be available. When written, data is loaded into a controller register and allowed to sequence into silo if space is available.	Used by the program for diagnostic purposes. When the register is written into, IR is cleared until the data buffer is ready to accept a new word. When the register is read, it will cause OR to be cleared until a new word is ready. During a write-check error condition, the data word read from the disk that did not compare with the corresponding word in memory is frozen in RMDb for examination by the program.

Address bits A16 and A17 can also be set or cleared through the RMCS1 register. If an address extension field is written into RMBAE, the program should ensure that A16 and A17 are not altered when a command is loaded into RMCS1. This can be accomplished by either loading the command with a write low byte instruction to RMCS1 or by ensuring that the proper value appears in the A16 and A17 bit positions of RMCS1. Table 4-7 provides a description of each bit.

Table 4-7 Bus Address Extension Register (RMBAE) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-05 A (Bus Address) Read/Write	Loaded by the program to specify the starting memory address of a data transfer operation. Cleared by Unibus INIT or controller clear.	The RMBAE register is incremented (or decremented) each time a carry-out (borrow-out) of RMBA occurs.
06-15 Not used	Always read as 0s.	

4.2.1.7 Control and Status Register No. 3 (RMCS3) – The RMCS3 register contains parity error information associated with the memory bus. Bit position 13 of the RMCS3 (DPE) indicates that a parity error occurred during the memory transfer. Bits 13 through 15 of RMCS3 further localize the error for diagnostic maintenance. In addition, bits 0 through 3 provide the diagnostic program the ability to invert the sense of parity check and thereby verify correct operation of the parity circuits.

An interrupt enable bit (IE) in the RMCS3 register allows the program to enable interrupts without writing into a drive register as previously described. This bit also appears in the RMCS1 register for program compatibility and can be set or cleared by writing into either register. Table 4-8 provides a description of each bit.

Table 4-8 Control and Status Register No. 3 (RMCS3) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-03 IPCK (Inverted Parity Check) Read/Write	These bits are written by the program to control the data parity detection logic. When set, inverse parity is checked with data during memory transfers of write and write check operations.	Parity control is provided for each byte in double word addresses, i.e., IPCK 0 – Even word, even byte IPCK 1 – Even word, odd byte IPCK 2 – Odd word, even byte IPCK 3 – Odd word, odd byte
Bit 04, 05 Not used	Always read as 0s.	
Bit 06 IE (Interrupt Enable) Read/Write	IE is a control bit that can be set under program control. When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared by Unibus INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.	This bit can be set or cleared by writing into RMCS1 register. If written through RMCS3 register, write operation is not performed into a drive register simultaneously.
Bit 07-09 Not used	Always read as 0s.	
Bit 10 DBL (Double Word) Read Only	Set if the last memory transfer was a double-word operation. Cleared by Unibus INIT, controller clear, or loading a data transfer command with GO bit set.	
Bit 11 WCE LO (Write Check Error-Even Word) Read Only	Set when data fails to compare between memory and the drive. Cleared by Unibus INIT, controller clear, error clear, or loading a data transfer command with GO set.	When set, causes bit 14 (WCE) of RMCS2 to set.
Bit 12 WCE HI (Write Check Error-Odd Word) Read Only	Set when data fails to compare between memory and the drive. Cleared by Unibus INIT, controller clear, error clear, or loading a data transfer command with GO set.	When set, causes bit 14 (WCE) of RMCS2 to set.
Bit 13 DPE LO (Data Parity Error-Even Word) Read Only	Set if a parity error is detected on data from memory when the RH controller is performing a write or write check command. Cleared by Unibus INIT, controller clear, error clear, or loading a data transfer command with GO bit set.	When set, causes bit 13 (UPE) of RMCS2 to set.

Table 4-8 Control and Status Register No. 3 (RMCS3) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 14 DPE HI (Data Parity Error- Odd Word) Read Only	Set if a parity error is detected on data from memory when the RH controller is performing a write or write check command. Cleared by Unibus INIT, controller clear, error clear, or loading a data transfer command with GO bit set.	When set, causes bit 13 (UPE) of RMCS2 to set.
Bit 15 APE (Address Parity Error) Read Only	Set if the address parity error line indicated that the memory detected a parity error on address and control information during a memory transfer. Cleared by Unibus INIT, controller clear, error clear, or loading a data transfer command with GO set.	When set, causes bit 13 (UPE) of RMCS2 to set.

4.2.2 Drive Registers

The following paragraphs contain the descriptions of the registers in the RM02/03 Massbus adapter.

4.2.2.1 Control Register (RMCS1) – This register is utilized by both the drive and the controller to store the disk commands and operational status. The function (command) code designates a function for the drive selected in bits 00 through 02 of the RMCS2 register. Setting the GO bit causes the drive to recognize the function code in the control register. The actual execution of the command, however, does not begin until the Run line is asserted by a data transfer command. Table 4-9 provides a description of each bit.

Table 4-9 Control Register (RMCS1) Bit Assignments Used by Drive

Name/Type	Set By/Cleared By	Description																																																																													
Bits 0-5 GO bit and F0-F4 Read/Write	GO bit and F0-F4 establish the function (command) code control bits that determine the action performed by the drive as shown below. <table><tr><th>F4</th><th>F3</th><th>F2</th><th>F1</th><th>F0</th><th>GO</th><th>Octal</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>05</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>07</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>11</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>13</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>17</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>23</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>31</td></tr></table>	F4	F3	F2	F1	F0	GO	Octal	0	0	0	0	0	1	01	0	0	0	1	0	1	05	0	0	0	1	1	1	07	0	0	1	0	0	1	11	0	0	1	0	1	1	13	0	0	1	1	0	1	15	0	0	1	1	1	1	17	0	1	0	0	0	1	21	0	1	0	0	1	1	23	0	1	1	0	0	1	31	Execution of data commands begins when Massbus Run line is asserted. <
F4	F3	F2	F1	F0	GO	Octal																																																																									
0	0	0	0	0	1	01																																																																									
0	0	0	1	0	1	05																																																																									
0	0	0	1	1	1	07																																																																									
0	0	1	0	0	1	11																																																																									
0	0	1	0	1	1	13																																																																									
0	0	1	1	0	1	15																																																																									
0	0	1	1	1	1	17																																																																									
0	1	0	0	0	1	21																																																																									
0	1	0	0	1	1	23																																																																									
0	1	1	0	0	1	31																																																																									

Table 4-9 Control Register (RMCS1) Bit Assignments Used by Drive (Cont)

Name/Type	Set By/Cleared By	Description																																																	
Bits 0–5 (cont)	<table><tr><th>F4</th><th>F3</th><th>F2</th><th>F1</th><th>F0</th><th>GO</th><th>Octal</th></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>51</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>53</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>61</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>63</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>71</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>73</td></tr></table> The GO bit (bit 0) must be set to cause the drive to respond to a command. The GO bit is reset by the RM03 after command execution.	F4	F3	F2	F1	F0	GO	Octal	1	0	1	0	0	1	51	1	0	1	0	1	1	53	1	1	0	0	0	1	61	1	1	0	0	1	1	63	1	1	1	0	0	1	71	1	1	1	0	1	1	73	Write Check Data Write Check Header and Data Write Data Write Header and Data Read Data Read Header and Data All other commands are illegal (ILF).
F4	F3	F2	F1	F0	GO	Octal																																													
1	0	1	0	0	1	51																																													
1	0	1	0	1	1	53																																													
1	1	0	0	0	1	61																																													
1	1	0	0	1	1	63																																													
1	1	1	0	0	1	71																																													
1	1	1	0	1	1	73																																													
Bit 6–10 Not used by drive		Used by controller. (See Table 4-2 for description.)																																																	
Bit 11 DVA (Drive Available) Read Only	Set when device is not busy on another port. Reset by device from other port when device is busy on that port.	This bit is used in dual-controller configurations.																																																	
Bit 12–15 Not used by drive		Used by controller. (See Table 4-2 for description.)																																																	

4.2.2.2 Drive Status Register (RMDS) – This read-only register contains the various status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (00:02) of the RMCS2 register. The register is a read-only register. Table 4-10 provides a description of each bit. Writing into this register will not cause an error, and will not modify any of the status bits.

Table 4-10 Drive Status Register (RMDS) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00 OM (Offset Mode) Read Only	Set when an offset command is issued to drive. Reset by any of the following seven actions. 1. Power-Up 2. Mid-Transfer Seek 3. Read-In Preset 4. Write Data or Write Header and Data 5. Return to Centerline 6. Writing Desired Cylinder 7. Recalibrate	When set and a read command is received, the offset is performed prior to the execution of the read.

Table 4-10 Drive Status Register (RMDS) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 01-05 SP (Spare) Read Only	Always 0s	Spare bits for future expansions.
Bit 06 VV (Volume Valid) Read Only	Set by the pack acknowledge or read-in preset command from either port. Cleared by the drive whenever it cycles up from the off state.	When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed. Therefore, the program should not assume anything about the identity of the pack. There are two VV bits: VV-A for accesses to port A and VV-B for accesses to port B. When the PORT switch is in port A, the VV-A bit is displayed in the VV bit position of this register. Accesses from port B will read all 0s except for the RMAS register. The reverse situation holds true when port B is selected.
Bit 07 DRY (Drive Ready) Read Only	Set at the completion of every command, data handling, or mechanical motion. Cleared at the initiation of a command.	If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the RM03 to accept a new command. If a read or write command was issued, the setting of the DRY bit will indicate normal termination. If an error was made during the data transfer, the appropriate interface lines, error bits, and bit 15 (ATA) of this register will also be set. If a mechanical movement command was issued, the ATA bit will also be set when DRY is set. If an error occurs during the mechanical movement, the appropriate interface lines and error bits will also be set. The DRY bit is the complement of the GO bit. (DRY = GO negated.) This is true except when the drive is nonexistent; then the DRY bit is reset.

Table 4-10 Drive Status Register (RMDS) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 08 DPR (Drive Present) Read Only	Always set for single-controller operation. In dual-controller operation, this bit is set for the controller that has seized the drive and is reset for the other controller.	
Bit 09 PGM (Programmable) Read Only	Set during a cycle-up sequence from the off state as bit 12 (MOL) is asserted if the PORT SELECT switch is in the PROG position (indicating that the device is accessible from either Port A or Port B). Cleared when PORT SELECT switch is in either Port A or Port B position.	In single-controller system configuration, this bit will always be reset. Dual-controller operation permits access from two controllers. The dual-controller option has three states. 1. Connected to controller A 2. Connected to controller B 3. Neutral When the drive is connected to controller A, only controller A can access the drive registers. Similarly, when the drive is connected to controller B, only controller B can access the drive registers. In programmable state, the drive is not connected to either controller, but either controller can read its registers. The PGM bit is interrelated to the drive present (DPR, bit 08), which is set when the drive is switched to the controller reading the register.
Bit 10 LBT (Last Block Transferred) Read Only	Set by the drive on rising edge of EBL pulse when last addressable sector on the disk pack has been read or written. Cleared when a new track or sector address is received. Also cleared during power-up cycle.	After reading or writing sector 29 for 18-bit word format (or 31 for 16-bit word format) of cylinder 882 on track 4, the LBT bit is set. With this bit set, the desired cylinder address register contains 823 (illegal address), and the desired sector track address register contains 0 since it was incremented on the rising edge of the last EBL pulse.

Table 4-10 Drive Status Register (RMDS) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description																		
Bit 11 WRL (Write Lock) Read Only	Set when the drive will not accept write commands, or whenever MOL is reset and drive is powered up. Cleared when the PROTECT switch is not depressed (PROTECT light extinguished).	The drive is placed in write protect mode through a manual switch on the drive control panel. The status of the device is indicated by the illumination of the light over the switch. When the indicator is on, any attempt by the operating system to issue a write command on a write-locked device will cause the write lock error (WLE, bit 11 of RMER1) bit to set.																		
Bit 12 MOL (Medium On-Line) Read Only	Set by the drive upon the successful completion of the startup cycle as follows. 1. Pack mounted 2. Start spindle motor 3. Motor up to speed 4. Load heads 5. Drive ready Cleared when the heads are unloaded.	After power-up cycle, heads are positioned over cylinder no. 0 and MOL bit is set. Whenever the MOL bit changes state (set or reset), bit 15 (ATA) of this register is also set, except when the heads are unloaded.																		
Bit 13 PIP (Positioning in Progress) Read Only	Set by drive when a positioning command is accepted. These commands are seek, offset, return to centerline, recalibrate, and search. The PIP bit is also set during implied seeks, mid-transfer seeks, and offset operation during a read. In addition, PIP is set whenever MOL is reset and drive is powered up. Cleared when the function is completed.	This bit helps to distinguish the case of a drive being in busy (DRY negated) while no data transfer is underway (RDY asserted in the controller). The following chart shows the state of the PIP bit in relation to the type of operation being performed. <table> <tr> <th colspan="2"></th><th>ATA at End of Operation (No Error)</th></tr> <tr> <th>Operation</th><th>DRY PIP</th><th></th></tr> <tr> <td>No Operation</td><td>0 0</td><td>No</td></tr> <tr> <td>Recalibrate</td><td>0 1</td><td>Yes</td></tr> <tr> <td>Drive Clear</td><td>0 0</td><td>No</td></tr> <tr> <td>Search</td><td>0 0/1</td><td>Yes</td></tr> </table>			ATA at End of Operation (No Error)	Operation	DRY PIP		No Operation	0 0	No	Recalibrate	0 1	Yes	Drive Clear	0 0	No	Search	0 0/1	Yes
		ATA at End of Operation (No Error)																		
Operation	DRY PIP																			
No Operation	0 0	No																		
Recalibrate	0 1	Yes																		
Drive Clear	0 0	No																		
Search	0 0/1	Yes																		

Table 4-10 Drive Status Register (RMDS) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description		
Bit 13 (cont)	Operation Seek Offset Write Check Write Data Write Header and Data Read Data Read Header and Data Implied Seek Mid-Transfer Seek Return to Centerline Pack Acknowledge Read-In Preset Offset During	DRY 0 0 0 0 0 0 0 0 0 0 0 0 0 0	PIP 1 0 0 0 0 0 0 1 1 0 0 0 0 1	ATA at End of Operation (No Error) Yes Yes No No No No No No No Yes No No No
Bit 14 ERR (Error) Read Only	Set when either of the error registers (RMER1 or RMER2) indicates a drive error. Cleared by drive clear, INIT, writing 1s in error registers, or during a power-up cycle.	A composite error bit that is the logical OR of all drive error conditions. While ERR is set, only clearing commands are accepted by the drive in a programmable mode.		
Bit 15 ATA (Attention Active) Read Only	Set by a drive. Attention condition. These conditions are as follows: - Any error in error registers: - If GO bit set; at completion of command - If GO bit reset; at occurrence of error. - At completion of seek, search, recalibrate, offset, or return to centerline. - MOL bit changes state. These conditions also set the Attention Interface line (ATA line). These conditions are cleared by the following. - Drive clear command - Writing a 1 into attention summary register. - INIT command - Writing a 1 into the GO bit, if no error condition exists.	For dual-controller operation, the ATA bit is asserted on both ports each time the drive cycles up. There are two ATA bits: ATA-A, which is accessible to controller A, and ATA-B, which is accessible to controller B. When the PORT switch is in controller A, the ATA-A bit is displayed in the ATA bit position (bit 15) of the register. Accesses from controller B will read all 0s except for the RMAS register. The reverse situation holds true when controller B is selected.		

4.2.2.3 Error Register No. 1 (RMER1) – This register contains the error status indicators for the drive whose unit number appears in bits 00 through 02 of RMCS2. The logical OR of all the error bits in the RMER1 and RMER2 registers will be written into bit 14 of RMDS.

The RMER1 register is a read/write register and can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy (GO bit is asserted), an RMR (RMER1 register, bit 02) error is set, and the contents of the RMER1 register are not otherwise modified.

Errors can be classified into two categories: class A and class B.

- A class A error is handled at the completion of a non-data transfer command or, in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
- A class B error causes the command to terminate immediately or as soon as possible.

Table 4-11 provides a description of each bit.

Table 4-11 Error Register No. 1 (RMER1) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00 ILF (Illegal Function) Read/Write	Set provided the GO bit is set and there is no previous error when the function code in the control register does not correspond to a valid drive command. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	ILF is a class B error.
Bit 01 ILR (Illegal Register) Read/Write	Set when a read or write is attempted on a register address greater than 17. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	When a read is attempted on an illegal register, the complement of the contents of the holding register is placed on the Massbus lines. ILR is a class A error.
Bit 02 RMR (Register Modification Refused) Read/Write	Set when a write is attempted into any register (except RMAS or RMMR1) while the GO bit is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	The following registers can be written into before or after an operation. • Control register • Error registers • Maintenance register no. 1 • Attention summary register • Desired sector/track • Address register • Offset register • Desired cylinder address register The remaining drive registers are read-only registers.

Table 4-11 Error Register No. 1 (RMER1) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 03 PAR (Parity Error) Read/Write Bit 04 FER (Format Error) Read/Write Bit 05 WCF (Write Clock Fail) Read/Write	Set when writing into a register if even parity is detected on the Control Bus lines. Also set when bit 03 (DPE) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register. Set when reading a sector header if bit 10 (HC1) of RMOF register is re-set and bit 12 of the first header word does not match the state of bit 12 (FMT) of RMOF register. Cleared by drive clear, INIT, power-up cycle, or writing 0s in this register. Set if during a write data or write header and data command, the RM03 requests data from the controller and does not receive a response within one word time (approximately 1.6 μs for 16-bit format or 1.8 μs for 18-bit format. Cleared by drive clear, INIT, power-up cycle, or writing 0s into this register.	During an operation, the maintenance no. 1 and attention summary registers can be written into. When RMR is set, the drive continues to execute the command in progress. RMR is a class A error. Depending when PAR occurs, it is either a class A or B error. • Class A during a register write • Class B if DPE is set Error usually indicates that pack and drive are incompatible in data word length (e.g., drive configured for 16-bit format and an 18-bit format pack installed). With a write command, an FER error can be catastrophic; FER will cause the command to abort at once. Only the read header and data command can be used to retrieve the header information. FER is a class A error during a read header and data command and a class B error during all other commands. WCF is a class B error.

Table 4-11 Error Register No. 1 (RMER1) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 06 ECH (ECC Hard Error) Read/Write	Set at the conclusion of the error correction procedure (bit 15 of this register is set), indicating that the error was a non-ECC correctable error. Cleared by drive clear, INIT, power-up cycle, or writing 0s into this register.	ECH is a class B error.
Bit 07 HCE (Header Compare Error) Read/Write	Set if bit 10 (HC1) of RMOF register is reset and one or more of the following occurs while reading the header. • Bits 0–9 of the first header word do not match bits 0–9 of the desired cylinder address register (RMDC). • Bit 12 of the first header word does not match bit 12 (RMT) of the offset register (RMOF). • Bits 0–5 of the second header word do not match bits 0–5 of the desired track and sector (RMDA) register. • Bits 8–10 of the second header word do not match bits 8–10 of the desired track and sector (RMDA) register. • Bits 14 and 15 must be 1s; otherwise BSE is set. • Any bit other than those specified above that is not a zero in either the first or second word of the header. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	HCE is a class A error during a read header and data command and a class B error during all other commands.

Table 4-11 Error Register No. 1 (RMER1) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 08 HCRC (Header CRC Error) Read/Write	Set if bit 10 (HCI) of RMOF is reset and the CRC register in the drive is not zero after the complete header has been read. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	It is possible for the cylinder address and error sector/track address words of the header (first two words) to compare successfully but, because of an error in the first two header words or the CRC word, the HCE bit will be reset and the HCRC bit will be set. HCRC is a class A error during a read header and data command and a class B error during all other commands.
Bit 09 AOE (Address Overflow Error) Read/Write	Set when controller requests a data transfer (read or write) beyond the last sector (29 or 31) of the last cylinder of the pack. This results in a cylinder address overflow condition. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	AOE is a class B error.
Bit 10 IAE (Invalid Address Error) Read/Write	Set if the contents of either desired cylinder register (RMDC) or desired sector/track address register (RMDA) are invalid and at the receipt of one of the following commands: • Seek • Search • Read Header and Data • Read Data • Write Check Header and Data • Write Check Data • Write Header and Data • Write Data Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	NOTE When AOE is set, the sector count in the desired sector/track address (RMDA) register is incremented at EBL (end of block) even though the command was terminated prior to the data being transferred. IAE is a class B error which causes the command to terminate when the GO bit sets. Invalid addresses are: desired cylinder greater than 822; desired track greater than 4; and desired sector greater than 29 for 18-bit format or 31 for 16-bit format.
Bit 11 WLE (Write Lock Error) Read/Write	Set if a write command is issued when the drive is in the write lock mode. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	WLE is a class B error. The state of the WRITE LOCK switch is allowed to change only on a sector boundary during a write command.

Table 4-11 Error Register No. 1 (RMER1) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 12 DTE (Drive Timing Error) Read/Write	Set when more than one sector pulse occurs within a sector. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	A failure in either the drive or the sequencing circuits of the RM03 no longer guarantees that the written or read data is in the proper sequence. DTE is a class B error.
Bit 13 OPI (Operation Incomplete) Read/Write	Sets if any of the following occurs. 1. During a seek command, no activity on the drive interface is detected within 300 ns after the Tag line is reset. (The On Cylinder signal should go low.) 2. During a search command, the correct sector is not located within three revolutions of the disk. 3. During a data transfer command, the Run signal is not asserted within 32 ms after the GO bit is set. 4. If MOL is reset and a command is attempted, it will not execute. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	OPI is a class B error.
Bit 14 UNS (Drive) Read/Write	Set when a condition exists that prevents proper operation (such as low ac power). Also set when bit 07 (DVC) of RMER2 is set. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	
Bit 15 DCK (Data Check Error) Read/Write	Set after reading the entire data field of the sector if the ECC register bits 11-31 are non-zero. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	DCK is a class A error if bit 10 (HCI) of RMOF is set and a class B error if HCI is reset.

4.2.2.4 Maintenance Register No. 1 – The RMMR1 register provides maintenance and diagnostic information useful during maintenance operations. This register has two distinct 16-bit sections: a read-only section and a write-only section. The read-only section permits monitoring of drive logic signals during the maintenance operations. The write-only section of this register provides a method to control the logic functions of the drive.

The write-only section can be written only after the drive is configured in the maintenance mode of operation (bit 00 set). The read-only section can be read in both normal and maintenance operational modes. Table 4-12 provides a description of each bit in the read-only section and Table 4-13 describes the bits in the write-only section.

**Table 4-12 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Read-Only Bits**

Name/Type	Set By/Cleared By	Description
Bit 00 DMD (Diagnostic Mode) Read Only	Set when the write-only section of this bit location is set by a diagnostic program. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	
Bit 01 LST (SECT TRK and Track) Read Only	This bit decodes the desired track/sector register (RMDA) to indicate that the last sector and track has been counted. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	When set, used to enable the cylinder address counter and to cause a mid-transfer seek. Set at sector 31, track 4 for 16-bit format or sector 29, track 4 for 18-bit format.
Bit 02 LS LST SECT (Last Sector) Read Only	This bit decodes sector 29 or 31 conditions. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	When set, used to enable the track address counter and to cause a new head to be selected during spiral data operations (either reading or writing).
Bit 03 WD WRITE DATA (Write Data) Read Only	This bit represents the serial data being sent to the drive during a write operation. Depending on the time this bit is read, it can be considered the output of the data register, ECC generator, or CRC generator. Cleared by drive clear, INIT, or power-up.	
Bit 04 EECC EN ECC OUT (Enable ECC Out) Read Only	Set by the data sequencer. Cleared by drive clear, INIT, or power-up.	This bit is only set during write operations when the ECC pattern is being written.

**Table 4-12 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Read-Only Bits (Cont)**

Name/Type	Set By/Cleared By	Description
Bit 05 WC PROM STROBE (PROM Strobe) Read Only	Produced by the servo clock except during a read when it is derived from the read clock. Cleared by drive clear, INIT, or power-up.	One complete PROM cycle lasts 16 bit clocks when in 16-bit format or 18 bit clocks when in 18-bit format. These PROM strobes are used to generate the read or write data timing.
Bit 06 CONT CONTINUE (Continue) Read-Only	Set at the end of block (EBL) if the Run line is active. Cleared by drive clear, INIT, or power-up.	As long as Continue is set, the drive continues to perform data transfer.
Bit 07 PHA P HEADER AREA (Header Area) Read Only	This bit location contains a level generated by the data sequencer after detecting the header sync byte. Cleared during the CRC time of the header.	The header sync byte precedes the three header words.
Bit 08 PDA P DATA AREA (Data Area) Read Only	This bit location contains a level generated by the data sequencer after detecting the data sync byte. Cleared during the word time of the last data word in the sector.	The data sync byte precedes the 256 data words.
Bit 09 ECRC EN CRC OUT (Enable CRC Out) Read Only	Set by the data sequencer during the time the CRC pattern is being written in a write operation. Cleared by drive clear, INIT, or power-up.	
Bit 10 P LFS (Looking for Sync) Read Only	Set to enable looking for Sync. It is reset by the sequencer when the sync byte has been located. It is also cleared by drive clear, INIT, or power-up.	Until Sync is located, the word clock to the data sequencer is inhibited.
Bit 11 ESRC ENABLE SEARCH (Enable Search) Read Only	Set by the command sequencer after head positioning and selection has occurred. Cleared by drive clear, INIT, or power-up.	Setting the enable search enables the sector compare circuits which, in turn, activate the data sequencer once the correct rotational position is achieved.
Bit 12 REX REC EXC (Exception) Read Only	This bit reflects the status of the Massbus Exception line. Cleared by drive clear, INIT, or power-up.	

**Table 4-12 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Read-Only Bits (Cont)**

Name/Type	Set By/Cleared By	Description
Bit 13 EBL RM03 EBL (End of Block) Read Only	Set by the adapter to indicate that the last block of data on the disk has been transferred. Cleared by drive clear, INIT, or power-up.	
Bit 14 R/G RUN AND GO (Run and Go) Read Only	Set when the Massbus Run line is active and the GO bit is set. Cleared when the GO bit is reset.	
Bit 15 OCC OCCUPIED (Occupied) Read Only	Set by the adapter during a valid data transfer operation. Cleared on the trailing edge of the GO bit.	

**Table 4-13 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Write-Only Bits**

Name/Type	Set By/Cleared By	Description
Bit 00 DMD (Diagnostic Mode) Write Only	Set by a diagnostic program to configure the drive in the maintenance mode. Must be set before any other RMMR1 bits can be written. Cleared by drive clear, INIT, or power-up cycle. Also, when cleared, resets bits 01-15 of this register.	The maintenance register is enabled by setting the DMD bit. This bit completely isolates the drive mechanism and analog circuitry from the disk control logic. The DMD bit must remain set as long as the maintenance register is functioning. All read/write commands will function in the normal fashion except for the fact that the data will wrap around itself instead of actually being written on the disk.
Bit 01 MSC MR SECT COMP (Sector Compare) Write Only	Set by diagnostic program to simulate the sector compare count normally generated by the drive. Cleared by drive clear, INIT, power-up or when DMD is cleared.	During normal search operations, the 5-bit sector count from the drive is compared with the address in the RMDA register. The sector compare bit allows diagnostic software the capability of forcing a sector compare, thus allowing a successful search and further testing of the data path.

**Table 4-13 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Write-Only Bits (Cont)**

Name/Type	Set By/Cleared By	Description
Bit 02 MI MR INDEX (Index Pulse) Write Only	Set by a diagnostic program to simulate an index pulse from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	Used to check out the change of format logic.
Bit 03 MWP MR WRT PROT (Write Protect)	When set, simulates the function of the front panel WRITE PROTECT switch. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	Without having to operate the switch, this allows the diagnostic program to verify the write protect functions.
Bit 04 Not used		
Bit 05 MS MR SECT PULSE (Sector Pulse)	Set by a diagnostic program to simulate a sector pulse. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	Used to clock logic elements in the sector compare circuits.
Bit 06 MDF MR DRIVE FAULT (Drive Fault) Write Only	Set by a diagnostic program to simulate a Fault signal from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	Used to test error handling logic in the adapter.
Bit 07 MSER MR SEEK ERR (Seek Error) Write Only	Set by a diagnostic program to simulate a seek error fault condition in the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	A Seek error cannot be forced by specifying a cylinder address greater than 822 since the adapter would detect this as an invalid address and inhibit the execution of the seek.
Bit 08 MDC MR ON CYL (On Cylinder) Write Only	Set by a diagnostic program to simulate the On Cylinder signal sent from the drive when the servo has positioned the heads over a data track. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	
Bit 09 MUR MR UNIT READY (Unit Ready) Write Only	Set by a diagnostic program to simulate the Unit Ready signal from the drive. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	The Unit Ready signal indicates that the pack is up to speed, heads are loaded, and no drive fault exists.
Bit 10 MRD MR READ DATA (Read Data) Write Only	Simulates the serial data bit read from the drive. Cleared by drive clear, INIT, power-up or when DMD bit is cleared.	By using the read data bit, diagnostic software can wrap around data at the adapter level and verify the data path independent of the drive.

**Table 4-13 Maintenance Register No. 1 (RMMR1) Bit Assignments
for Write-Only Bits (Cont)**

Name/Type	Set By/Cleared By	Description
Bit 11 MCLK MAINT CLK (Maintenance Clock) Write Only	Set by a diagnostic program to establish the timing for the data path during the maintenance mode. Cleared by drive clear, INIT, power-up or when DMD bit is cleared.	This clock has two distinct functions depending on whether a read or write operation is being performed. With read gate on, simulates the Read Clock signal from the drive; with write gate on, simulates the Servo Clock signal from the drive.
Bit 12 MSEN SRCH TO DIS (Search Timeout Disable) Write Only	Set by a diagnostic program to inhibit the search timeout circuits. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	Normally the search timeout circuits generate an OPI signal if the drive was unable to locate the desired sector within two revolutions.
Bit 13 DEBL DEBL (Diagnostic EBL) Write Only	Set by a diagnostic program to check the increment logic circuits associated with the sector/track and cylinder registers. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	This bit also allows diagnostic programs to step through the command sequencer without going through a complete data transfer (independently of the read/write timing sequencer).
Bit 14 DBEN DEBUG EN (Debug Clock Enable) Write Only	Set by a diagnostic program and used as the source of the command sequencer clock, allowing the sequencer to be advanced at the diagnostic program rate. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	When the debug clock enable bit is reset, the command sequencer clock is derived from the system clock, causing the command sequencer to run at its normal rate.
Bit 15 DBCK DEBUG CLK (Debug Clock) Write Only	Set by a diagnostic program as the source for the command sequencer clock. Cleared by drive clear, INIT, power-up, or when DMD bit is cleared.	

4.2.2.5 Attention Summary Pseudo-Register (RMAS) – The attention summary register is not like the other addressable registers in the drive. While it is considered as being a 16-bit register, it is actually composed of up to eight flip-flops. Each bit is physically located in one of the eight possible drives that can be connected to a single controller. Each flip-flop is connected to the Control Bus line whose line number corresponds to the number assigned to the drive. The eight flip-flops are actually in parallel and it is this configuration that is called a pseudo-register.

The attention summary register allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in RMDS for the corresponding drive. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always 0.

The ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. (Loading a 0 has no effect.) This allows the program to inspect the RMAS register and later to reset the ATA bits that were set, without accidentally resetting other ATA bits that may have become set in the meantime.

This register can be read or written at any time, regardless of whether any particular drive is busy. Note that a drive never asserts ATA during the execution of a command.

There is no parity generation when reading the RMAS register because all devices on the Massbus respond to the attention poll regardless of their address.

When reading the attention summary register, bits 8–15 are unspecified. Table 4-14 provides a description of each bit.

Table 4-14 Attention Summary Register (RMAS) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–07 ATA (00:07) (Attention Active) Read/Write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by INIT or drive clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.	Any drive's ATA bit set is displayed in bit 15 of RMDS. Each drive responds in the bit position that corresponds to its unit select plug number; e.g., drive 02 sets bit position 02 in RMAS.
Bit 08–15 Not Used		

4.2.2.6 Sector/Track Address Register (RMDA) – This device register is used to address the sector and track on the disk to or from which a transfer is desired. The RMDA register is associated with the drive whose unit number appears in bits 00:02 of the status register RMCS2. Before a transfer, the RMDA is loaded by the program with the address of the first block to be transferred. The RMDA is incremented each time a block of data has been transferred so that consecutive blocks are automatically addressed when the word count indicates that more than one block is to be transferred.

The RMDA register contains a 5-bit sector address providing for 30 sectors per data track (18-bit format) or for 32 sectors per data track (16-bit format). The register also contains a 3-bit track address providing for five data tracks. The sector and track addresses are non-contiguous; however, when the sector count fills up with a count of 29 or 31 (depending on format), the next word read or written will cause the track address to increment and the sector address to clear. When the sector address and track address reach their full counts, the next word will cause both sector and track addresses to increment to 0 and a mid-transfer seek to occur.

The RMDA register can only be loaded with a 16-bit word. Any attempt to write a byte causes the entire word to be written. Any attempt to write in this register while the drive's GO bit is asserted will cause an RMR (register modify refused) error (RMER1, bit 02) and the register is not modified. Table 4-15 provides a description of each bit.

Table 4-15 Desired Sector/Track Address Register (RMDA) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-04 SA(1,2,4,8,16) (Sector Address) Read/Write	Set by the program to specify the sector on which a transfer is to start. Cleared by read-in preset command.	Incremented by the drive after each sector has been transferred.
Bit 05-07 SP (Spare) Read/Write	Always 0s.	Spare bits for future expansion.
Bit 08-12 TA(1,2,4,8,16) (Track Address) Read/Write	Set by the program to specify the track on which a transfer is to start. Cleared by read-in preset command. (TA8, TA16 are reserved for future expansion.)	Incremented by the drive when sector 31 (16-bit format) or sector 29 (18-bit format) is reached.
Bit 13-15 SP (Spare) Read/Write	Always 0s.	Spare bits for future expansion.

4.2.2.7 Drive-Type Register (RMDT) – This read-only register allows the program to distinguish between different classes of drives. The register is located in the drive whose unit number appears in bits 00 through 02 of RMCS2. Table 4-16 provides a description of each bit.

Table 4-16 Drive-Type Register (RMDT) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-08 DT (Drive Type) Read Only		This 9-bit field contains a unique number assigned to each device on the Massbus. The device type number for the drive is installed on the back panel. (20024 for single port or 24024 for dual port).
Bit 09, 10 Not Used	Always read as 0s.	
Bit 11 DRQ (Drive Request Required) Read Only		The status of this bit indicates the availability of the dual-port option as follows: 1 = Dual Port 0 = Single Port
Bit 12 Not Used	Always read as 0s.	
Bit 13 MOH (Moving Head) Read Only		Since the RM03 is a moving head device, this bit is hardwired to the 1 state.
Bit 14, 15 Not Used	Always read as 0s.	

4.2.2.8 Look-Ahead Register (RMLA) – This read-only register contains the count of the sector that is currently positioned under the heads. This value is represented as a binary number in bit locations 6-10, where bit 6 is the LSB. The maximum count for a 16-bit/word format is 31 and for an 18-bit/word format is 29.

The count value is reset to 0 by the index pulse at the beginning of the first sector and is incremented by one at each sector pulse. The count value is not valid for 200 μ s after either an index or sector pulse. Table 4-17 provides a description of each bit.

Table 4-17 Look-Ahead Register (RMLA) Bit Assignments

Name/Type	Set By/Cleared By
Bit 00-05 Not Used	Always read as 0s.
Bit 06-10 SC(1,2,4,8,16) (Sector Count) Read Only	Set to correspond with the sector count value. Reset by the index pulse.
Bit 11-15 Not Used	Always read as 0s.

4.2.2.9 Serial Number Register (RMSN) – This read-only register permits the program to identify drives attached to the same controller. The serial number provides a means of distinguishing between different drives with identical characteristics that are connected to the same controller. This information is useful during error logging of on-line software diagnostics to allow errors to be associated with a particular drive. The serial number register differs from the drive-type register in that the drive type refers to different classes of drives such as single- or dual-port operation.

The serial number register is actually a jumper card with a maximum of 16 jumper wires. The serial number code is established by cutting the proper wires either (at the factory or at installation time). The last four digits of the serial number is provided in BCD form without distinction between 50 or 60 Hz drives. The actual jumper card will be the same for all drives, but the number will be different for each drive. Table 4-18 provides a description of each bit.

4.2.2.10 Offset Register (RMOF) – The drive has the ability to offset the positioner approximately 200 μ in from the track centerline in either direction.

The positioner offsetting information is supplied to the drive directly from the software operating system prior to the issuance of the offset command. Table 4-19 provides a description of each bit.

Table 4-18 Serial Number Register (RMSN) Bit Assignments

Name/Type	Set By/Cleared By
Bit 00–03 SN (Serial Number) Read Only	Least-significant BCD digit of the last four numbers in the serial number.
Bit 04–07 SN (Serial Number) Read Only	Tens BCD digit of the last four numbers in the serial number.
Bit 08–11 SN (Serial Number) Read Only	Hundreds BCD digit of the last four numbers in the serial number.
Bit 12–15 SN (Serial Number) Read Only	Most-significant BCD digit of the last four numbers in the serial number.

Table 4-19 Offset Register (RMOF) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–06 Not Used	Always read as 0s.	
Bit 07 OFD (Offset Direction) Read/Write	Set when the offset direction is toward the spindle. When reset, the offset direction is away from the spindle.	The offset direction bit is valid if the following three conditions are met. 1. Read command is loaded into control register (RMCS1) (bits 0–5). 2. The RMCS1 GO bit is set. 3. The offset mode bit (RMDS bit 00) is set.
Bit 8, 9 Not Used	Always read as 0s.	
Bit 10 HCI (Header Compare Inhibit) Read/Write	Set by the software program to inhibit the reporting of header compare errors FER, HCE, and HCRC (bits 4, 7, and 8 respectively of RMER1). Cleared by a read-in preset command or by a software write.	When the drive sees this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the device logic depends only on the sector count field/desired address field comparison for sector identification. If the sector count field is out of sequence, the wrong sector may be affected. The meaning of the HCI bit is valid in both the read and write commands. It is strongly recommended, however, that the HCI bit be reset during a write operation.
Bit 11 ECI (Error Correction Inhibit) Read/Write	When set by the software, prevents the isolation and correction of a data check error. It also allows a data handling command to advance the heads to a sector beyond the sector where the data check error occurred. When reset, normal ECC action will occur. Cleared by a read-in preset command or by a software write.	If a data error is detected at the end of the data transmission in the read mode with the ECI bit reset, the drive goes into the ECC correction process at the end of the sector. Prior to beginning the correction routine, the device will also set the data check (DCK) error bit RMER1 bit 15, which will remain set until a drive clear command or an INIT pulse is received.

Table 4-19 Offset Register (RMOF) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 11 (cont)		When the results of the error correction process are available, the device will place the error pattern and the location of the error pattern within the data field in the appropriate ECC registers. The Run line is expected to drop while the EBL pulse is high and, at the fall of the EBL pulse, the EXC line will also reset. The resetting of the EXC line will cause the ATTN line to set and the command will terminate. If the error was non-ECC-correctable, the drive will also set the ECC hard error (ECH) bit and will handle the EBL, EXC, and ATTN lines as described above. If the ECI bit is set, the error correction process will be inhibited. The termination procedure will be done normally as if no data error occurred. Only the DCK bit will be set as soon as a data error is detected. This bit will remain set until a Drive Clear or an INIT pulse is received.
Bit 12 FMT FMT 16 (Format) Read/Write	Set to a 1 when 16-bit/word format is used (16 bits/word × 256 words/sector). Set to a 0 when 18-bit/word format is used (18 bits/word × 256 words/sector). Cleared by read-in preset command or by software write.	The bit controls the word length. Upon reading a header from the pack, the recorded bit is compared with this bit setting. If the bits do not compare, the format error (FER) bit 4 of RMER1 is set.
Bit 13-15 Not Used	Always read as 0s.	

4.2.2.11 Desired Cylinder Register (RMDC) – This read/write register contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command. Since the maximum number of cylinders in the RM02 or RM03 is 823, only 10 bits are necessary to specify the desired cylinder address. Table 4-20 provides a description of each bit.

Table 4-20 Desired Cylinder Register (RMDC) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–09 DC (Desired Cylinder) Read/Write	Set by the program to the decimal number representing the cylinder number where the head is to move. Bit DC1 is the least-significant bit and bit DC512 is the most-significant bit. Cleared by read-in preset.	The invalid address error bit (RMER1 bit 10) sets, when upon asserting the GO bit, the contents of the desired cylinder register contain an address larger than 822.
Bit 10–15 Not Used	Always read as 0s.	

4.2.2.12 Holding Register (RMHR) – This is an addressable register with no drive function. It is used only by diagnostic software. When writing into this register, all bits remain unchanged and new information is lost. When reading this register (or any illegal register), the complement of the register contents is read. Whenever writing any legal register, this holding register is concurrently written.

4.2.2.13 Maintenance Register No. 2 (RMMR2) – The RMMR2 register operates in conjunction with the Maintenance Register No. 1 to configure the RM02 or RM03 Massbus adapter in the maintenance mode. Table 4-21 provides a description of each bit.

Table 4-21 Maintenance Register No. 2 (RMMR2) Bit Assignments

Name/Type	Set By/Cleared By	Description																																												
Bit 00-09 BB (Bus In Lines) Read Only	These 10 bus lines represent the lines going to the drive which establish the cylinder address, head address, or control depending on which tag is issued as shown below. <table><thead><tr><th>Bus in Bits</th><th>Cylinder Address Tag</th><th>Head Select Tag</th><th>Control Select Tag</th></tr></thead><tbody><tr><td>0</td><td>1</td><td>1</td><td>Write Gate</td></tr><tr><td>1</td><td>2</td><td>2</td><td>Read Gate</td></tr><tr><td>2</td><td>4</td><td>4</td><td>Servo Offset Plus</td></tr><tr><td>3</td><td>8</td><td>Not Used</td><td>Servo Offset Minus</td></tr><tr><td>4</td><td>16</td><td>Not Used</td><td>Fault Clear</td></tr><tr><td>5</td><td>32</td><td>Not Used</td><td>Not Used</td></tr><tr><td>6</td><td>64</td><td>Not Used</td><td>Return to Zero</td></tr><tr><td>7</td><td>128</td><td>Not Used</td><td>Not Used</td></tr><tr><td>8</td><td>256</td><td>Not Used</td><td>Not Used</td></tr><tr><td>9</td><td>512</td><td>Not Used</td><td>Not Used</td></tr></tbody></table>	Bus in Bits	Cylinder Address Tag	Head Select Tag	Control Select Tag	0	1	1	Write Gate	1	2	2	Read Gate	2	4	4	Servo Offset Plus	3	8	Not Used	Servo Offset Minus	4	16	Not Used	Fault Clear	5	32	Not Used	Not Used	6	64	Not Used	Return to Zero	7	128	Not Used	Not Used	8	256	Not Used	Not Used	9	512	Not Used	Not Used	
Bus in Bits	Cylinder Address Tag	Head Select Tag	Control Select Tag																																											
0	1	1	Write Gate																																											
1	2	2	Read Gate																																											
2	4	4	Servo Offset Plus																																											
3	8	Not Used	Servo Offset Minus																																											
4	16	Not Used	Fault Clear																																											
5	32	Not Used	Not Used																																											
6	64	Not Used	Return to Zero																																											
7	128	Not Used	Not Used																																											
8	256	Not Used	Not Used																																											
9	512	Not Used	Not Used																																											

Table 4-21 Maintenance Register No. 2 (RMMR2) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 10 CNT/HD (Control or Head Select) Read Only	Set when the tag to the drive is either a control select or head select tag. Cleared by drive clear, INIT, or power-up.	
Bit 11 CNT/CYL (Control or Cylinder Select) Read Only	Set when the tag to the drive is either a control select or cylinder address tag. Cleared by drive clear, INIT, or power-up.	
Bit 12 TEST BIT (Test Bit) Read Only	Set when the command sequencer in the adapter is branching.	Used by diagnostics during a branch test sequence. It tells the control sequencer whether to branch or increment.
Bit 13 TAG (Tag) Read Only	Indicates the status of the Control Select Tag line.	
Bit 14 REQ B (Request B) Read Only	When set, indicates that a request for service has been received from port B. Cleared by drive clear, or by a release command in addition to RE-SET.	
Bit 15 REQ A (Request A)	When set, indicates that a request for service has been received from port A. Cleared by drive clear or by a release command in addition to RE-SET.	

4.2.2.14 Error Register No. 2 (RMER2) – This read/write register contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the Massbus interface. Whenever any of the bits in this register are set, the ERR bit (bit 14) in the status register (RMDS) is set and the ATA bit in the RMAS register is set. All Error Register No. 2 errors are considered catastrophic errors.

NOTE

All unsafe errors, with the exception of read/write unsafes, cause the drive to retract the heads from the pack area; prevent a head load from occurring; deselect all heads; and disable the read, write, recalibrate, seek, and offset commands.

All error bits reset when a drive clear command or an INIT pulse is received. If the heads are retracted from the disk pack upon receiving a drive clear or an initialize pulse, the drive attempts to reload the heads unless the error persists.

Errors are classified into two categories: class A and class B.

- A class A error is handled at the completion of a non-data transfer command, or in the case of a data transfer command, at a sector boundary provided the Run line is inactive.
- A class B error is handled immediately and causes immediate termination of a command or a termination as soon as possible. Table 4-22 provides a description of each bit.

Table 4-22 Error Register No. 2 (RMER2) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00-02 Not Used	Always read as 0s.	
Bit 03 DPE (Data Parity Error) Read/Write	Set during either a write data or write header and data command if the synchronous data bus parity is even. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	When DPE sets, it also causes bit 3 of RMER1 to set. DPE is a class B error.
Bit 04-06 Not Used	Always read as 0s.	
Bit 07 DVC (Device Check) Read/Write	Set by the drive to indicate either or both of the following drive errors occurred: dc power fault or head select fault. Cleared by drive clear, INIT, power-up cycle, or by writing 0s into this register.	DVC is a class B error.
Bit 08, 09 Not Used	Always read as 0s.	
Bit 10 LBC (Loss of Bit Check) Read/Write	Set when no transition occurs in the bit clock for a period longer than 400 ns.	The bit clock is derived from the read clock and the servo clock. LBC is a class B error.
Bit 11 LSC (Loss of System Clock)	Set when either of the following. 1. The GO bit is reset and there is no transition in the system clock for a period longer than 3 μs. 2. The GO bit is set and there are no PROM address changes.	LSC is a class B error.

Table 4-22 Error Register No. 2 (RMER2) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 12 IVC (Invalid Command) Read/Write	Set when volume valid (RMDS bit 6) is reset or unit ready is not active and any command other than read-in preset or pack acknowledge is received. Also set if Drive Clear or NO-OP is received. Cleared by INIT, power-up cycle, or by writing 0s into this register.	IVC is a class B error.
Bit 13 DPE (Operator Plug Error) Read/Write	Set when the drive address plug is removed. Cleared after replacing plug by drive clear, INIT, power-up cycle, or by writing 0s into this register.	While the plug is removed, the drive is considered to be nonexistent to the program. OPE is a class B error if the plug is removed during a data handling command and a class A error if it occurs at any other time.
Bit 14 SKI (Seek Incomplete) Read/Write	Set by the drive if any of the following three conditions occur. 1. The drive is unable to complete a move within 500 ms. 2. The carriage moves to a position outside of the recording field. 3. A cylinder address greater than 822 is requested during a seek operation. Cleared by either a drive clear or INIT, then a recalibrate command.	Due to a positioner malfunction it is possible for the seek not to complete. The drive will assume a positioner hardware problem and will: • Set the SKI bit (RMER2, bit 14) • Set the ATA bit (RMDS, bit 15) • Reset the PIP bit (RMDS, bit 13) • Set the RDY bit (RMCS1, bit 7) This indicates to the software that the seek operation did not complete and the exact positioner location is unknown.

Table 4-22 Error Register No. 2 (RMER2) Bit Assignments (Cont)

Name/Type	Set By/Cleared By	Description
Bit 14 (cont)		A SKI condition will cause the drive to determine that the drive is unsafe to operate and will cause the UNS (RMER1, bit 14) bit to set. The software can diagnose the trouble by monitoring the error registers. NOTE Since an error exists in an error register (SKI error bit is set), the software must issue a drive clear command to clear the error before attempting to retry.
Bit 15 BSE (Bad Sector Error)	Set whenever the drive detects a 0 in bit 14 or 15 of the first header word. A jumper disable for BSE is available on the backplane.	A bad sector is indicated when this bit is cleared. This is a class B error which causes termination of a read command after checking the CRC word. In the case of a read header and data command, this is a class A error.

4.2.2.15 ECC Position Register (RMEC1) – The drive has Error Correction Code (ECC) capabilities that detect and correct errors by reconstructing a portion of the data. In the specified code word length, the ECC code corrects an error that falls within an 11-bit burst.

Any errors outside the specified burst length are detected but not corrected. The ECC hardware, in this case, yields an ECC uncorrectable error (bit 6 of RMER1 sets). The drive logic contains the hardware to find the burst in which the read error is included and to determine the exact location of the burst within the data field.

The ECC pattern register (RMEC2) contains the actual error burst and the ECC position register (RMEC1) contains the address that determines the actual location of the error burst within the data field.

NOTE

The actual correction of the data field is done by the software with the help of the ECC position and ECC pattern registers.

Following the completion of the error correction procedure, the ECC position register contains the exact location of the error burst within the data field.

The EXC line is raised upon initiation of the error correction procedure and the ATA bit is set at the trailing edge of EBL and EXC. Table 4-23 provides a description of each bit.

Table 4-23 ECC Position Register (RMEC1) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–12 P (Position Bit) Read Only	Set by the ECC logic if a data check error occurred (bit 15 of RMER1 is set) at the end of a data transfer command and the error detected is considered to be correctable (bit 6 of RMER1 is reset). The 13 position bits establish the binary address of the first bit of the error burst within the data field. The maximum valid address is: • 4128 for 16-bit format • 4640 for 18-bit format. During ECC generation, these bits are pre-set to 4066₈ in 16-bit mode or to 5066₈ in 18-bit mode.	If the ECC logic determines that the error is a non-correctable hard error (bit 6 of RMER1 is set) or if the header compare inhibit bit (RMOF bit 10) is set, the contents of this register are irrelevant.
Bit 13–15 Not Used	Always read as 0s.	

4.2.2.16 ECC Pattern Register (RMEC2) – This read-only register is used in conjunction with the ECC position register (RMEC1) and contains the actual error burst available at the completion of the ECC process.

The software uses the contents of the ECC position register to find the actual location of the error burst in the data field. Then the error burst itself determines the bits in error within the 11-bit field. Table 4-24 provides a description of each bit.

Table 4-24 ECC Pattern Register (RMEC2) Bit Assignments

Name/Type	Set By/Cleared By	Description
Bit 00–10 PAT (Pattern Bit) Read Only	Set by the ECC logic if the detected error is correctable. The 11 pattern bits establish the error burst. Cleared by drive clear or INIT.	If the ECC logic determines that the error is a non-correctable hard error (bit 6 of RMER1 is set) or the error correction inhibit bit (RMOF bit 11) is set, the contents of this register are irrelevant.
Bit 11–15 Not Used	Always read as 0s.	

4.2.3 Command Codes

The programmer initiates operations by selecting a drive selecting the control register (776700), and loading the register with a function code and setting the GO bit. The function code specifies a specific command. Upon assertion of the GO bit, the RM03 proceeds to execute the command. The commands can be divided into three categories: positioning commands, data transfer commands, and housekeeping operations. These commands and their corresponding octal function codes are listed below.

Positioning Commands

	Function Codes (Octal)
Seek	5
Recalibrate	7
Offset	15
Return to Centerline	17
Search	31

Data Transfer Commands

Write Check Data	51
Write Check Header and Data	53
Write Data	61
Write Header and Data (Format)	63
Read Data	71
Read Header and Data	73

Housekeeping Operations

No-Op	1
Drive Clear	11
Release	13
Read-In Preset	21
Pack Acknowledge	23

4.2.4 Positioning Commands

Positioning commands are mechanical movement commands used to position the heads over the disk pack; they take milliseconds to complete. These commands assert the ATTN line after their normal completion. The positioning commands are described below.

4.2.4.1 Seek – This command causes the heads to be moved to the cylinder address specified by the desired cylinder register (RMDC). The current cylinder is made equal to the desired cylinder address following the completion of the command.

4.2.4.2 Recalibrate – This command positions the heads over cylinder 0.

4.2.4.3 Offset – An offset allows the heads to be moved off the track centerline. It is used in error recovery processing and moves the heads 200 μ in either toward the spindle (positive offset) or away from the spindle (negative offset).

4.2.4.4 Return to Centerline – This command is used to return to the track centerline after an offset operation. A return to centerline always follows a read command in offset mode.

4.2.4.5 Search – This command combines the seek command with a search for the desired sector address and can be considered a synchronization command between the software and the desired disk address.

4.2.5 Data Transfer Commands

These commands involve the transfer of data to or from the disk and usually require the completion of a positioning command by either a seek or search command or with an implied seek as part of the data command. The data transfer commands are described in the following six paragraphs.

4.2.5.1 Read Header and Data – A read header and data command transfers 2 words of header information and 256 data words per sector from the disk pack to the RH controller.

4.2.5.2 Read Data – A read data command transfers 256 data field words from the disk pack to the RH controller for each sector specified. If an error is detected in the header, this command will abort immediately following the CRC check and there will be no data transferred.

4.2.5.3 Write Check Header and Data – A read header and data command transfers the first 2 words of the header and 256 words of data to the RH controller. Errors in the header, however, cause termination of the command after the CRC word of the header is checked in the drive.

4.2.5.4 Write Check Data – This command is identical to a read data command.

4.2.5.5 Write Header and Data – A write header and data command, also referred to as a “format” command, writes all gaps, header, and data for specified sector(s). The drive generates the gaps including the sync byte, CRC, and ECC. The RH controller supplies 2 header words and 256 data words for each sector.

4.2.5.6 Write Data – A write data command transfers 256 words of data for each specified sector from the RH controller to the drive. This data field is preceded by a sync byte and followed by a 32-bit ECC, both generated by the drive. A header error will cause the command to abort immediately after checking the CRC word.

4.2.6 Housekeeping Commands

Housekeeping commands are used to place the drive logic into known or initial state. ATTN is not raised at the completion of the housekeeping commands unless there is a persistent error condition. The five housekeeping commands are listed below.

4.2.6.1 No-Op – Upon recognizing this code in the control register (RMCS1) and the GO bit, the drive resets the GO bit. This command is considered a filler command.

4.2.6.2 Drive Clear – A drive clear command clears bits in the following registers in the Massbus adapter.

Status (RMDS)	Bit 14 (ERR), bit 15 (ATA)
Error No. 1 (RMER1)	All bits
Error No. 2 (RMER2)	All bits
Attention Summary (RMAS)	All bits (on the selected drive)
Maintenance No. 1 (RMAS)	All bits
ECC Pattern (RMEC2)	All bits

This command also clears all error indications in the drive (provided the error condition no longer exists). A pulse on the Massbus Initialize line performs the same functions as the drive clear command.

4.2.6.3 Release – The release command releases the drive for use by the other port. It must be preceded by a drive clear command if there is an error condition.

4.2.6.4 Read-in Preset – The read-in preset command sets the volume valid (VV) bit (06) in the status register (RMDS) for the port that issued the command. This command also clears all bits in the desired sector/track address register (RMDA) and all bits in the desired cylinder address register (RMDC). It also clears the offset mode and the following bits in the offset register (RMOF).

OFD (bit 07) – Offset Direction

HCI (bit 10) – Header Compare Inhibit

ECI (bit 11) – Error Correction Code Inhibit

FMT 16 (bit 12) – Format

4.2.6.5 Pack Acknowledge – The pack acknowledge command sets the volume valid (VV) bit (06) in the status register (RMDS) for the port that issued the command. This command must be issued before any data transfer or positioning commands can be given if the pack has gone off-line and then on-line (i.e., MOL changes state). It is primarily intended to avoid unknown pack changes on a dual-controller drive configuration.

4.2.7 Operation of Error Correcting Code (ECC)

The drive contains error correcting code logic that has the capability to detect errors in the data being read off the disk and provide information to the software to permit data recovery.

The ECC code employed, called burst error correcting code, locates an error that falls within an 11-bit burst.

Any errors outside this 11-bit burst length are detected but not correctable. For uncorrectable errors, the ECC logic generates an ECC hard error (ECH) indication.

An uncorrectable error is defined as any error field larger than the 11-bit burst. Isolated dropped bits (for example, one bit in word 0 and one bit in word 225) are uncorrectable by this definition.

If the above conditions occur, the drive indicates the ECC uncorrectable error to the software by setting the ECC hard error bit (ECH) in error register no. 1 (RMER1).

The drive ECC logic performs the following.

1. Finds the 11-bit burst where the read error is located.
2. Determines the exact location of the burst within the data field.

This error information is provided to the controller through two registers.

ECC Pattern Register (RMEC2)

Contains the actual 11-bit error burst

ECC Position Register (RMEC1)

Contains the address of the first bit of the error burst within the data field.

The actual correction of the data field is done by the software using the data contained in these two registers.

In the event of an ECC hard error, the contents of the ECC pattern and ECC position registers are of no significance.

4.2.7.1 ECC Operation During a Data Write – The ECC generation is started with the first bit following the sync pattern for the data field and continues for the entire data field, ending with the last bit of the data field. This ECC (32 bits) is then shifted out unaltered immediately following the last data word (word 256) and placed onto the disk sector.

4.2.7.2 ECC Operation During A Data Read – The ECC field in the sector block always follows the 256-word data block. The data block is guaranteed to be 256 words in length, regardless of whether the 16- or 18-bit mode is employed. After transmitting the required 256 data words, the drive logic waits until the ECC field is shifted through the ECC register for a possible read error detection.

4.2.7.3 Error Detection and Isolation – The ECC operation stops as soon as the last bit of the 32-bit ECC field is read in from the disk. At this point, the ECC register (by nature of the code used) should contain all 0s. A non-zero result in these bits indicates a data error and causes a data check error indication [bit 15 of Error Register No. 1 (RMER1) sets].

If no error is detected in the data field after the last word has been read, the read command normally terminates without any time delay.

If an error has been detected in the data field (and ECC hardware is enabled), the procedure to correct this error is accomplished by the ECC hardware, which goes through a routine to isolate the 11-bit error burst in the data field. The exact location of this burst is available to the software.

NOTE

If an error has occurred and has been detected by the ECC hardware, following transmission of the data block, the data check (DCK) error bit remains set throughout the entire correction process (providing the ECI bit is reset).

The software will then take the ECC burst pattern and will proceed to find the bits in error and correct them.

4.2.7.4 ECC Inhibit/Enable Function – Error correction in the drive is enabled or inhibited by the error correction inhibit (ECI) bit (RMOF bit 11). If this bit is asserted, the drive logic inhibits error correction when an error is detected. The read operation continues as if no error occurred. If this bit is negated, the drive logic enables the ECC circuitry when a read error is detected.

4.2.8 Dual-Port Option

The dual port option in the drive provides the capability for two controllers to access the same drive. Figure 4-10 shows the dual-controller configuration. Note that the eight drives are daisy-chained and that the two controllers can be attached to the same or to two different central processors.

NOTE

Since both the PDP-11 and PDP-10 processors have the capability (through RH11 and RH10 controllers, respectively) to interface to the Massbus, it is possible for both of these processors to be connected (through their respective controllers) into the configuration in Figure 4-10. In this configuration, both processors can operate in their separate format modes (16 bits/word for the PDP-11, 18 bits/word for the PDP-10) as long as there is no attempt to mix formats on the same track.

The PORT SELECT switches establish the operational condition of a dual-ported drive. The operational condition is set when the drive powers up from a not-ready state to the ready state. These dual-port conditions are as follows.

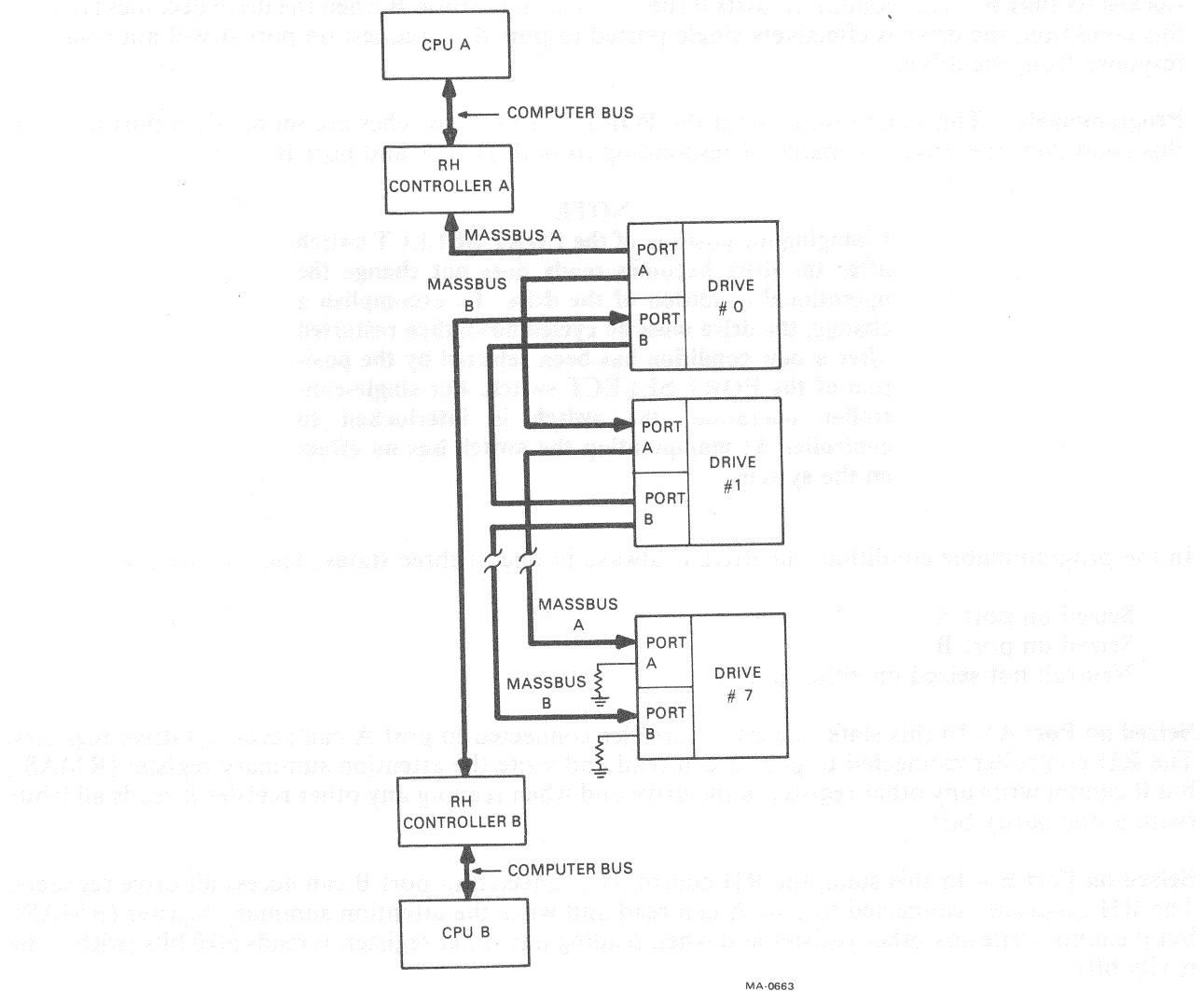


Figure 4-10 Dual-Port Configuration

Locked on Port A – This condition exists if the switch is in position A when the drive becomes ready. In this condition, the drive is effectively single ported to port A. A request on port B will not result in a response from the drive.

Locked on Port B – This condition exists if the switch is in position B when the drive becomes ready. In this condition, the drive is effectively single ported to port B. A request on port A will not result in a response from the drive.

Programmable – This condition exists if the PORT SELECT switches are set for dual-port mode. In this condition, the drive is capable of responding to both port A and port B.

NOTE

Changing the position of the PORT SELECT switch after the drive becomes ready does not change the operational condition of the drive. To accomplish a change, the drive must be cycled down then restarted after a new condition has been selected by the position of the PORT SELECT switch. For single-controller operation, the switch is interlocked to controller A; manipulating the switch has no effect on the system.

In the programmable condition, the drive is always in one of three states. These states are:

- Seized on port A
- Seized on port B
- Neutral; not seized on either port.

Seized on Port A – In this state, the RH controller connected to port A can access all drive registers. The RH controller connected to port B can read and write the attention summary register (RMAS), but it cannot write any other register in the drive and when reading any other register it reads all 0 bits (with a one parity bit).

Seized on Port B – In this state, the RH controller connected to port B can access all drive registers. The RH controller connected to port A can read and write the attention summary register (RMAS), but it cannot write any other register and when reading any other register, it reads all 0 bits (with a one parity bit).

Neutral State – In this state, the drive is not occupied by either port A or port B, but is equally available to either port on a first-come, first-served basis.

4.2.8.1 Dual-Port Register Bits – The following bits in the status register (RMDS) and control register (RMCS1) are used in dual-port operations.

Status Register

1. **Volume Valid (VV)** – The drive implements two volume valid bits: VV-A and VV-B. These are used to indicate when a disk pack has been changed; therefore, the program should not assume anything about the identity of the pack. VV-A is accessible to controller A only; VV-B is accessible to controller B only. The status of either bit is displayed in bit location 06. This bit can be examined by each controller and indicates the pack status for that controller. If controller A issues a pack acknowledge command, the VV bit for controller A is set. If controller B does not issue a pack acknowledge command, the VV bit for controller B is reset.

2. **Drive Ready (DRY)** – This bit (07) is reset by the controller that has seized the drive and is set on the completion of an operation. The DRY bit is the complement of the GO bit. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse) and causes the DRY bit to appear reset (indicating device busy).
3. **Drive Present (DPR)** – This bit (08) is set for the controller that has seized the drive. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse) and causes the DPR bit to appear reset. The DPR bit indicates that the drive is ready to communicate with the controller that has seized it.
4. **Programmable (PGM)** – This bit (09) is set when the drive is in the programmable condition and reset when the drive is locked on port A or locked on port B. During startup of the drive, the PGM bit is always set from the time power is applied until the medium on-line (MOL) bit (12) sets.
5. **Attention Summary (ATA)** – This bit (15) consists of two ATA flip-flops: ATA-A and ATA-B. When controller A has seized the drive, the ATA-A bit is displayed in the ATA position of the status register; ATA-A is accessible to controller A only. When controller B has seized the drive, the ATA-B bit is displayed in this bit position; ATA-B is accessible to controller B only.

The ATA-A bit is always accessible to controller A, regardless of the setting of the PORT SELECT switch; similarly, the ATA-B bit is always accessible to controller B.

A read of the attention summary register by either controller produces the normal response. Even though controller A is selected, controller B can read the drive registers; however, 0s will be read back to controller B, indicating that this controller is not logically connected to the drive.

Control Register

Device Available (DVA) – This bit (11) appears set to the port that has seized the drive and reset to the other port. If the second controller attempts to access the status register, the drive transmits all 0s (accompanied by the TRA pulse). This causes the DVA bit to appear reset to the second controller.

4.2.8.2 Dual-Port Commands – The following commands are used in dual-port operations.

1. **Pack Acknowledge** – Sets volume valid (VV) bit in status register for the port that issued the pack acknowledge command.
2. **Read-In Preset** – Sets volume valid (VV) bit in status register for the port that issued the read-in preset command.
3. **Release** – With the drive seized on a port, a release command to that port causes the RM03 to release to the neutral state (if the other port has not requested use of the RM03). If the other port has requested use of the drive, it switches to the other port rather than to neutral.
4. **Initialize (INIT) line** – The drive responds to an INIT issued separately from either port under the following conditions:
 - An INIT issued by port A clears the port A ATA bit but does not affect the port B ATA bit. The converse is true for port B.

- If the drive is seized on port A and an INIT is initiated by port B, the INIT from port B is ignored. The converse is true for a drive seized on port B.
- When the drive is in the neutral state, an INIT from either port is accepted.

NOTE

In the above three conditions an INIT clears all other registers and functions in a normal manner.

4.2.8.3 Dual-Port Unseized Status – The unseized state occurs when the drive is not connected to either controller and the PORT SELECT switch is in the PROG position.

The drive is switched to the alternate controller by the PORT SELECT switch or if in the unseized state when:

1. The alternate controller writes into any register (including illegal registers).
2. The alternate controller reads the control register.
3. The alternate controller writes the ATA bit associated with a specific drive in the attention summary register.

As an example, if the drive is in the unseized state and controller A reads the control register, it seizes the drive.

4.2.8.4 Dual-Port Seized Status – Seized operation occurs when the drive is logically connected to one controller through a port.

NOTE

The drive is seized by controller A when the PORT SELECT switch is in A position, by controller B when the PORT SELECT switch is in B position, or by either controller when the PORT SELECT switch is in PROG position.

If the drive is seized by controller B, for example, writing any control register from controller A is ignored by the logic; however, the drive stores the fact that controller A has requested use of the drive in the port request flip-flop. Every request by controller A to read the control register (RMCS1) causes the drive to send 0s (accompanied by the TRA pulse) to the controller, indicating that the device is reserved by the other controller. Since the system operates with odd parity, the RM03 forces a one parity bit with each transmission of 0s through port A.

NOTE

If the drive is seized by controller B, the drive present (DPR) bit is set for controller B and reset for controller A. No special handling is required by the drive to process the DPR bit, because, if controller A requests a read of the control register (RMCS1), the drive sends all 0s (accompanied by the TRA pulse). The same situation occurs for the DRY bit (0s sent to controller A, indicating that the device is busy).

If upon cycling up (indicated by setting of the MOL bit), the drive determines that the PORT SELECT switch is in the PROG position, it sets the programmable (PGM) bit. Although the drive is occupied by one controller or the other, the status of the PGM bit is not physically altered.

4.2.8.5 Switching from Unseized to Seized Status – When the drive is not seized by either controller, it is equally available to both. If a controller reads a drive register (including illegal registers), the drive immediately connects to that controller for the duration of the register read operation. This constitutes a momentary transition.

If a controller writes any register (including illegal registers), the drive immediately connects to that controller and remains seized to that controller until a release command or a 1-second timeout is received.

4.2.8.6 Switching from Seized to Unseized Status – Upon recognizing the release command from controller B, the drive checks the port A request flip-flop to determine if the drive has been requested by controller A. If this flip-flop is not set, the logic returns to the unseized state (PGM is already set) and the DVA bit is set in the control register. If the flip-flop is set, controller A seizes the drive and bypasses the unseized state.

NOTE

The drive times out if it is occupied by a controller and a release command is not received from that controller one second after termination of the last command transmitted to the drive. In this case, the drive returns to the unseized state. The 1-second timeout does not apply if the controller is selected by the position of the PORT SELECT switch.

For example, assume that controller B has seized the drive and controller A has requested it. When controller B issues the release command, the RM01:

1. Sets the PGM bit in the drive status register
2. Maintains the DPR bit set to controller A
3. Sets the drive available (DVA) bit for controller A
4. Sets the ATA bit to controller A.

Upon recognizing the assertion of the ATTN line, controller A takes advantage of the interrupt and initiates a command to the drive. With the drive seized by controller A, controller B receives the same responses that controller A was receiving when it requested the drive.

4.2.8.7 Dual-Port Register Access – Table 4-25 shows the controller action and the corresponding drive responses to each action. For example, if controller A attempts to read the control register and the drive is in the unseized state with the PORT SELECT switch in the A/B position, the drive immediately switches to controller A, sets the DVA bit, and reads the function code. If the drive is already seized by controller B, controller A reads all 0s.

4.2.8.8 Error Handling in Dual-Port Operations – If an error condition exists, a drive clear command or INIT must be issued to the seized port before a release command can be executed.

If the error is persistent, neither the drive clear command nor INIT clears the condition. For this condition the 1-second timeout circuit releases the seized port.

Following release from a persistent error condition, the next port that seizes the drive will see the ATA and ERR bits set indicating that the error condition occurred.

For example, assume that the drive is seized by controller A and a persistent error occurs that cannot be cleared by a drive clear or an INIT command.

Table 4-25 Register Accesses on Dual-Controller Operation

Action Performed by Controller A	Drive Response with Respect to Controller A		
	Programmable Mode	Seized by A	Seized by B
Read the control register.	Immediately switches to state A; reads the function code.	DVA = 1; reads the function code	DVA = 0; reads all 0s.
Write the control register.	Immediately switches to state A; loads the function code.	Loads the function code. (Switches to neutral if the function is released.)	The function code is ignored.
Read the status register.	Reads the status bits: PGM = 0; DPR = 1. No change of state.	Reads the status bits: PGM = 1; DPR = 1.	Reads all 0s: PGM = 1; DPR = 0.
Read any other drive register.	Reads the register; no change of state.	Reads the register.	Reads all 0s.
Write any other drive register.	Immediately switches to state A; loads the register.	Loads the register.	The word is ignored.

NOTES

1. It is assumed that the PORT SELECT switch is in the PROG position.

2. If controller A has seized the drive and controller B requests it, the drive switches to controller B as soon as a release command is issued. When this occurs, the port B ATTN line is asserted.

If controller B has requested the drive, the drive eventually is seized by controller B through the 1-second timeout. The ATA bit is set, but it has a double meaning. controller B determines that an error condition also exists by reading the status register and discovering the ERR bit set.

If controller B has not requested the drive, the drive reverts to the unseized state through the 1-second time-out. In this case, controller B receives no ATTN when the drive goes to the unseized state from controller A. Controller B is notified of the error condition when it attempts to seize the drive (by writing the drive registers).

NOTE

In the event of a persistent error, the software can clear the ATTN bit by writing a 1 into it.

Subsequent addressing of the attention summary register by the controller does not cause the ATTN bit (belonging to the drive with the persistent error) to be asserted. Any attempt to write on any of the other drive registers, however, causes the ATTN line to be asserted.

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

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