DEC-00-I6AA-D

ANALOG-DIGITAL CONVERTER AD08-A

INSTRUCTION MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

CONTENTS

ILLUSTRATIONS

TABLES

CONTENTS (continued)

ENGINEERING DRAWINGS

INTRODUCTION

This manual contains information relating to the operation, installation, and maintenance of the Type AD08-A Analog-to-Digital Converter (ADC).

The AD08-A A/D Converter is an I/O device used primarily with a PDP-8® or PDP-8/S computer for high-speed analog-to-digital conversions. The AD08-A is capable of converting analog signals from 0V to 10V in amplitude to a 10-bit digital word. The AD08-A uses the successive-approximation technique for data conversion with an accuracy of 0.1% ± 1/2 least significant bit (LSB) for quantizing error.

Physical Description

The AD08-A A/D Converter is packaged with its own digital and analog power supply in one DEC 1943 Mounting Panel. The power supplies are mounted in place of two connector blocks at the extreme right of the mounting panel.

Dimensions:

Height	5-1/4 in.
Width	19 in. (standard rack mount)
Depth	6-1/2 in. (not including I/O Cables)

Interface - The AD08-A includes six 6-foot cables for connection to the PDP-8 or the PDP-8/S I/O Bus. The interface is complete for this option, including IOT's and diagnostic software.

Power Requirements - DC Power for both the digital logic and the analog logic is supplied with the AD08-A.

General Specifications

Analog input voltage (standard)	0V to +10V full scale
with amplifier (option)	±10V max. full scale
with sample and hold (option)	±10V max. full scale
Input impedance (standard)	1000 ohms
with amplifier (option)	≥10,000 ohms (inverting) ≥100 M-ohms (non-inverting)
with sample and hold (option)	≥10,000 ohms
Digital output	Parallel Binary 1 = −3V 0 = 0V

® PDP is the registered trademark of the programmed data processors manufactured by the Digital Equipment Corporation of Maynard, Massachusetts.

Number notation	2's Complement 0V = 0000 +5V = 4000 +10V = 7774
Word Length	10 bits fixed
Accuracy	0.1% of full scale ± 1/2 LSB
Aperture time (standard) with sample and hold (option)	Same as conversion time 150 ns
Acquisition time with sample and hold (option)	12 μs
Conversion rate	100 KHz
Conversion time	10 μs
Resolution	1 part in 1024 (10 mV)

Power Requirements and Environmental Considerations

Warm-up time	5 min.
Temperature Coefficient	0.5 mV/°C
Operating Temperature	0 to 50°C
Input power	115 V 60 Hz 50 W
Power supply	DEC Part No. 12-03185, output voltage 15/15
Diode board	No. 5404220

Pertinent Documents

Source material, complementing the information in this manual, is found in the Digital Logic Handbook, C-105. This contains complete information on the functions and specifications of the various modules and accessories comprising the AD08-A system.

OPERATION

Method

The AD08-A A/D Converter operates on the principle of successive approximation.

To start conversion, the appropriate IOT command is given. The converter assumes that the value of the analog signal is at mid-scale and sets a 1 in the appropriate register. The equivalent analog signal is then generated by the converter, and a comparator compares the two analog values. If the analog input is greater than the value in the guess register, the output of the comparator goes to −3V and the appropriate bit remains in the 1 state.

This process is repeated for ten bits, with each bit weighing exactly 1/2 of the preceding bit. When conversion is completed, the buffer register in the converter contains the digital representation, in binary, of the analog input voltage.

The completion of conversion sets the end-of-conversion flag, which is sampled by initiation of a second IOT command. Once the computer determines conversion is complete, the accumulator (AC) must be cleared, and the digital value read into the computer by another IOT command. The digital value is then transferred into bits 0-9 of the AC.

Provision is made for using the Type A400 Sample-and-Hold Amplifier (AH02 option), preceding the ADC input, to reduce the effective aperture to less than 150 ns. The A400 may also be used to scale the signal input to accept ± 10V, ± 5V, or 0 to −10V. The A200 Amplifier (AH03 option) may be substituted for the A400 to accomplish the same signal scaling, without reducing the effective aperture.

The AH02 and AH03 options may also be used in combination to obtain both high-input impedance and small aperture. Power for the amplifier and/or sample-and-hold options is contained in the converter.

Converter Instructions

The AD08-A operates under direct control of the central processor. The following IOT instructions provide the necessary control:

Skip on A/D Flag (ADSF)

Octal code	6531
Event time	1
Indicators	IOT, FETCH, EXECUTE, END
Execution time	38 μs
Operation	The converter flag is sensed, and, if it contains a binary 1 (indicating that the conversion is complete), the contents of the program counter (PC) are incremented by 1, so that the next instruction is skipped.
Symbol	If A-D flag = 1, then PC + 1 = >PC

Convert Analog Voltage to Digital Value (ADCV)

Octal code	6532
Event time	2
Indicators	IOT, FETCH, EXECUTE, END
Execution time	38 μs

Convert Analog Voltage to Digital Value (continued)

Operation	The converter flag is cleared; the analog input voltage is converted to a digital value; and the A/D converter flag is set to 1. The preset switch position determines the number of binary bits in the digital-value word and the accuracy of the word.
Symbol	0 = > A/D flag at start of conversion, then 1 = > A/D flag when conversion is done.

Read A/D Converter Buffer (ADRB)

Octal code	6534
Event time	3
Indicators	IOT, FETCH, EXECUTE, END
Execution time	38 μs
Operation	The converter number contained in the converter buffer (ADCB) is transferred into the AC as a normalized word, shifted into the most significant bits (MSB); unused bits of the AC are cleared; and the A/D converter flag is cleared.
Symbol	ADCB = > AC 0 = > A/D converter flag

THEORY OF OPERATION

Block Diagram Analysis

The method of successive approximation is a technique where the digital output is obtained one bit at a time.

With the initiation of an A-D convert pulse, the control logic sets the MSB of the digital register to the 1 state, and all others to 0. (See figure 1.) Each bit of the register is transformed to a binary-weighted current by the D-to-A converter, with the MSB transformed to a one-half scale current, the next bit to one-quarter scale, etc.

The D-to-A converter output, which is the sum of all these currents is compared against the input current by the comparator. If the D-to-A output is too large, the control logic resets the associated bit of the ADC register to 0, and sets the next successive bit. If the D-to-A output is too small, the associated bit of the ADC register is kept, and the next successive bit is set. If the D-to-A output exactly equals the input, the associated bit may or may not be kept. If it is kept, all successive lower order bits are rejected, because they unbalance the comparator input. If the bit is rejected, then all lower order bits are retained, because their sum is less than the rejected bit by exactly 1 LSB. Therefore, the resolution of the converter is 1 LSB.

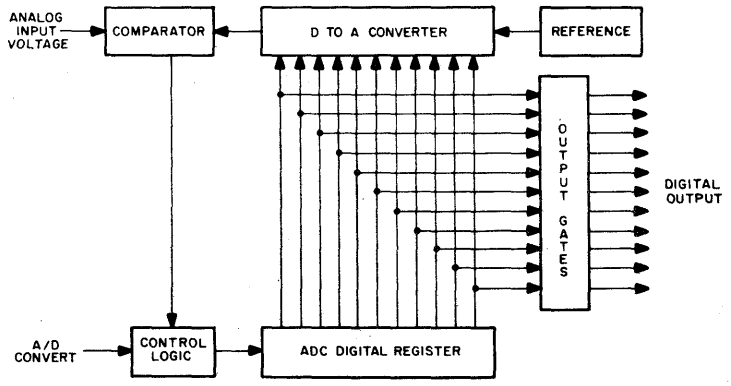


Figure 1 AD08-A Block Diagram

Block Schematic Analysis

The Type AD08-A A/D Converter is shown on drawing BS-AD08-A-1. The major functional element of the AD08-A is the A801 A/D Converter Module.

A typical sequence of operation starts when an ADCV pulse is applied to the W601-A8D. This pulse causes the A801 A/D Converter Module to convert the analog-input voltage on pin B12V to a 10-bit digital word. This digital word is applied to the output gates R123's through level shifters W512's. At the end of conversion, the A801 generates an A/D DONE pulse at pin B12M. This pulse is applied to the R202 A/D DONE flip-flop, after being level shifted and inverted. The A/D DONE level, in turn, is applied to the R111-B8L, to generate an interrupt level. A/D DONE is also applied to B8E, and ANDed with the ADSF pulse to give a skip pulse.

OPTIONS

AH03 Amplifier Option

The normal input impedance to the A/D Converter is 1000 ohms. Higher input impedance can be achieved using the AH03 Amplifier Option.

The AH03 option consists of an A200 Operational Amplifier, mounted on an A990 Amplifier Board with potentiometers for gain trim and balance. Feedback and input resistors are mounted on the module to allow for non-standard input voltages. An input impedance of greater than 10K ohms is also provided. (See A200 Specifications below).

Open loop gain	2×10^6
Rated output	
Voltage	±11V
Current	20 mA

Frequency response	
Unity gain, small signal	10 MHz
Full output voltage	300 KHz
Slewing rate	30V/μs
Overload recovery	200 Ms

Input voltage offset (adjustable to 0)	
Average vs temperature	20 μV/°C
Average vs supply voltage	15 μV/%
Average vs time	10 μV/day
Input current offset	±2 nA
Average vs temperature	0.4 nA/°C
Average vs supply voltage	0.15 nA/%

Input impedance	
Between inputs	6 megohm
Common mode	500 megohm
Input voltage	
Maximum	±15V
Maximum common mode	±10V
Common mode rejection	20,000
Power voltage	±15V
Current at rated load	35 mA

AH02 Sample and Hold Option

The AH02 Sample and Hold Option consists of an A400 Sample and Hold Module, with necessary components, to allow for non-standard input voltages and an R202 Control Flip-Flop. The AH02 option has an input impedance of greater than 10K ohms. (See A400 specifications below.)

Track time to 0.025% (full-scale step)	<12 μs
Aperture time	<150 ns
Droop (hold inaccuracy)	<1V/sec
Gain	1.000 (adjustable to 0.025%)
Input impedance	10K ohm ±0.1% (AT)
Full-scale input	±10V
Output current	10 mA
voltage	0 to −10V
impedance	<1.0 ohm
Temperature coefficent	
in sample	20 μV/°C offset
in hold	0.10V/sec/°C
Power requirements	±15V/50 mA

MAINTENANCE

Calibration

The AD08-A requires two analog calibration adjustments. These adjustments are used to balance out any offset in the system and to adjust full scale voltage.

The following program and procedure may be used to calibrate the converter for a 10V (less 1 LSB) full-scale system:

```
START
        20/7200     CLA
        21/6532     ADCV
        22/6531     ADSF
        23/5022     JMP-1
        24/6534     ADRB
        25/2100     ISZ (100)
        26/5025     JMP-1
        27/5020     JMP START
```

When a PDP-8 is used in place of a PDP-8/S, additional ISZ loops are necessary to slow down the P.R.F. Using the above program applies a noise-free analog voltage of +0.0049V to pin B12V. Adjust the 10-K offset potentiometer on the A801 A/D Module, location AB 12, until the AC indicators switch between 0000 and 0004. Change the analog voltage to +9.9854V. Adjust the 500 ohm reference potentiometer on the A801 A/D Module, location AB 12, until the AC indicators switch between 7770 and 7774. The offset adjustment must be rechecked. (See Table 1.)

Table 1
Theoretical Switching Point Voltages

Switching Point		Theoretical Voltage	Actual Voltage	Error
From	To	Volts	Volts	mV
0000	0004	+0.0049		
0004	0010	+0.0147		
0010	0014	+0.0245		
0770	0774	+1.2353		
0774	1000	+1.2451		
1000	1004	+1.2549		
1770	1774	+2.4853		
1774	2000	+2.4951		
2000	2004	+2.5049		
2770	2774	+3.7353		
2774	3000	+3.7451		
3000	3004	+3.7549		
3770	3774	+4.9853		
3774	4000	+4.9951		
4000	4004	+5.0049		
4004	4010	+5.0147		

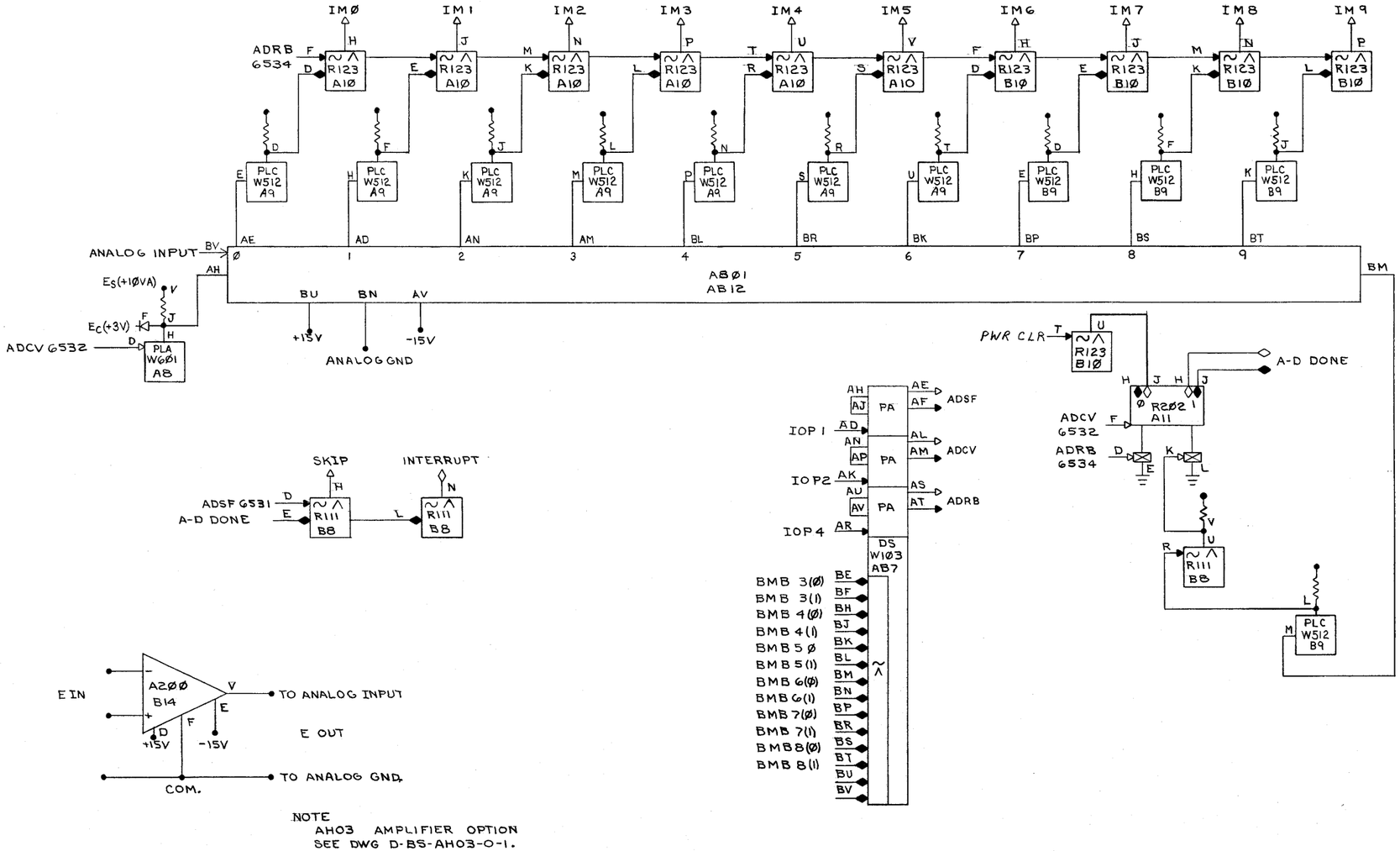
Table 1
Theoretical Switching Point Voltages (continued)

Switching Point		Theoretical Voltage	Actual Voltage	Error
From	To	Volts	Volts	mV
4770	4774	+6.2353		
4774	5000	+6.2451		
5000	5004	+6.2549		
5770	5774	+7.4853		
5774	6000	+7.4951		
6000	6004	+7.5049		
6770	6774	+8.7353		
6774	7000	+8.7451		
7000	7004	+8.7549		
7760	7764	+9.9658		
7764	7770	+9.9756		
7770	7774	+9.9854		

DRAWINGS

The engineering drawings in the following list are included in this manual as an aid to understanding and maintaining the AD08-A system. Where this book differs from the drawings supplied with the machine, the latter can be presumed correct.

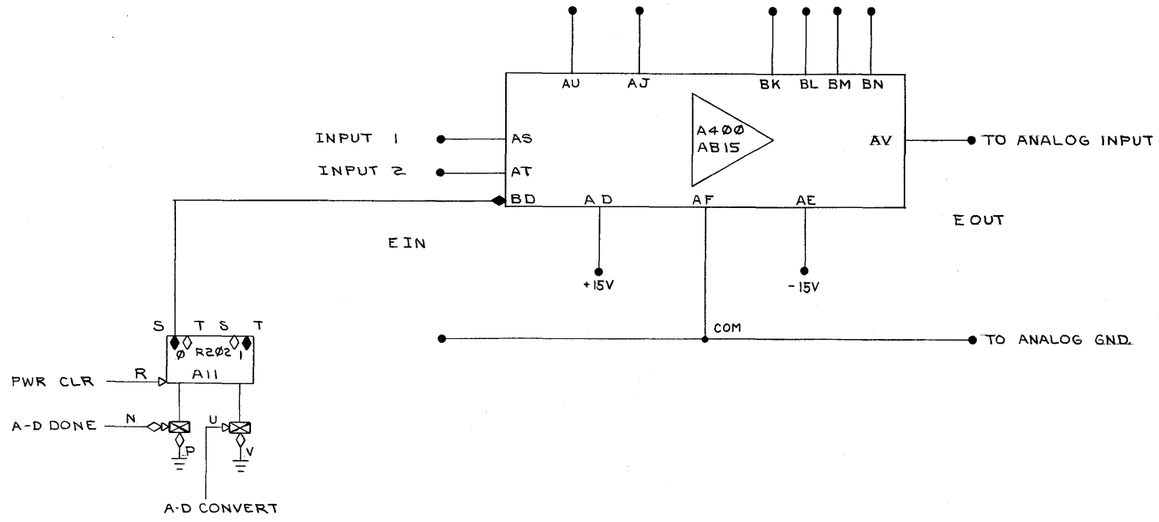
10 bit A/D Converter	D-BS-AD08-A-1
Sample and Hold Option	D-BS-AD08-A-2
I/O Connectors	D-IC-AD08-A-5
Standard Amplifier Configurations	D-BS-AH03-0-1
Module Utilization	D-MU-AD08-A-3

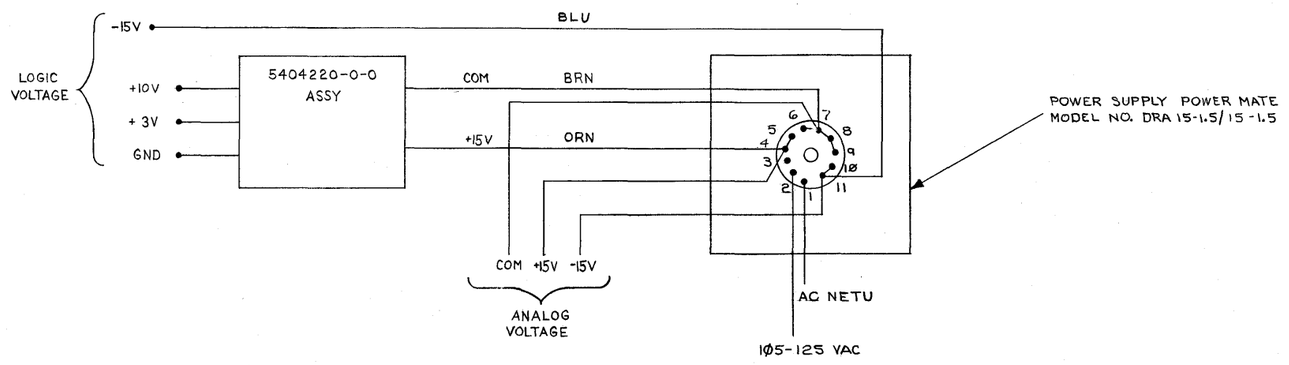

IM0
IM1
IM2
IM3
IM4
IM5
IM6
IM7
IM8
IM9
ADRB 6534
R123 A10
R123 B10
PLC W512 A9
PLC W512 B9
ANALOG INPUT
AE
AD
AN
AM
BL
BR
BK
BP
BS
BT
AB01
AB12
BM
AH
BV
BU
BN
AV
+15V
-15V
ANALOG GND
Es(+10VA)
Ec(+3V)
ADCV 6532
PLA W601 A8
SKIP
INTERRUPT
ADSF 6531
A-D DONE
R111 B8
IOP1
IOP2
IOP4
PA
DS W103 AB7
ADSF
ADCV
ADRB
BMB 3(0)
BMB 3(1)
BMB 4(0)
BMB 4(1)
BMB 5 0
BMB 5(1)
BMB 6(0)
BMB 6(1)
BMB 7(0)
BMB 7(1)
BMB 8(0)
BMB 8(1)
PWR CLR
R202 A11
A-D DONE
ADCV 6532
ADRB 6534
PLC W512 B9
A200 B14
E IN
TO ANALOG INPUT
E OUT
TO ANALOG GND
COM.
NOTE
AH03 AMPLIFIER OPTION
SEE DWG D-BS-AH03-O-1.

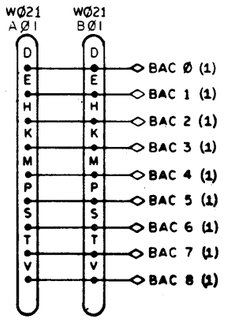
NOTE:

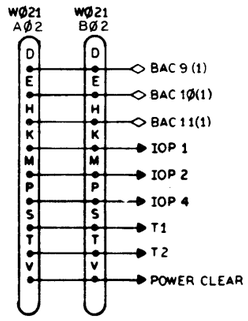
FOR NEGATIVE OFFSET VOLTAGE CONNECT AU TO BJ
CONNECT BN TO AF
CONNECT BL TO AD

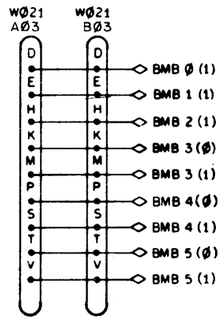
FOR POSITIVE OFFSET VOLTAGE CONNECT AU TO BJ
CONNECT BK TO AF
CONNECT BM TO AE

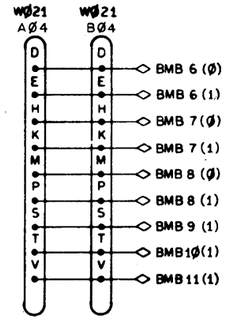


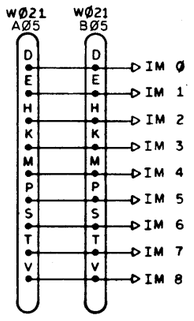


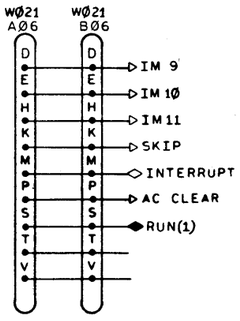












GROUND PINS C,F,J,L,N,R,U ON ALL WØ21 CONNECTORS

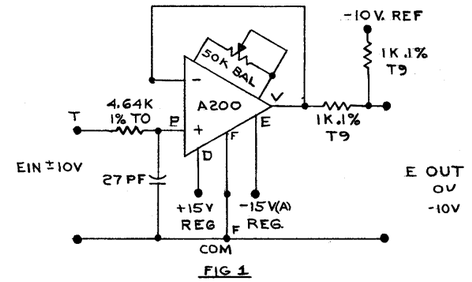


FIG 1

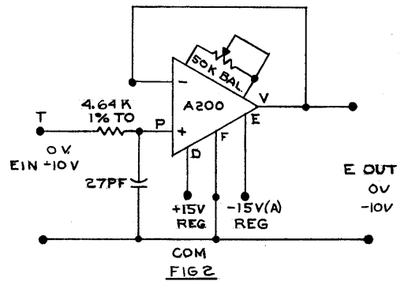


FIG 2

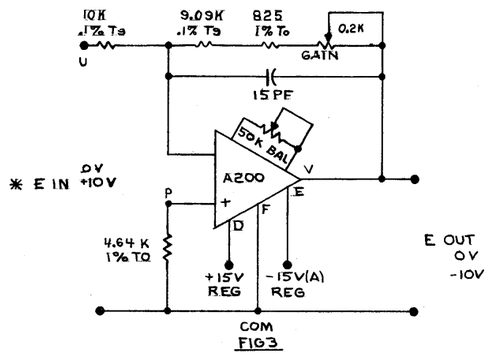


FIG 3

* WHEN EIN= 0V TO +10V OR 0V TO +5V, A SECOND INPUT BUFFER AMPLIFIER IS REQUIRED.

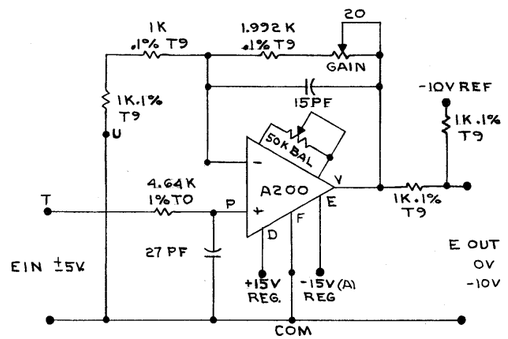


FIG 4

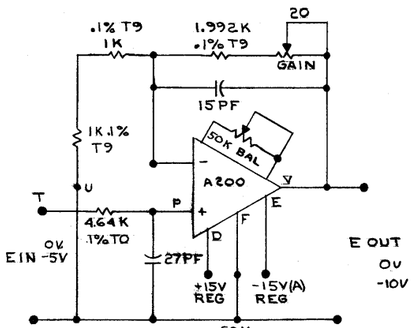


FIG 5

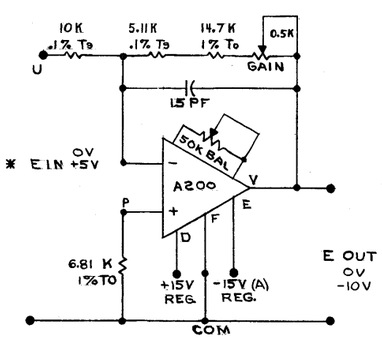


FIG 6

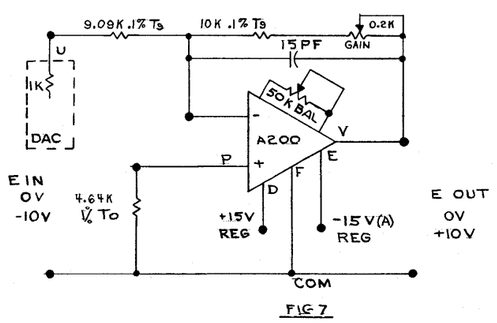


FIG 7

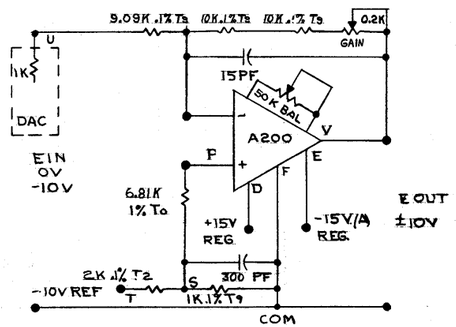


FIG 8

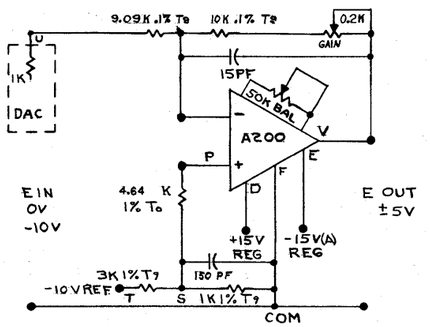
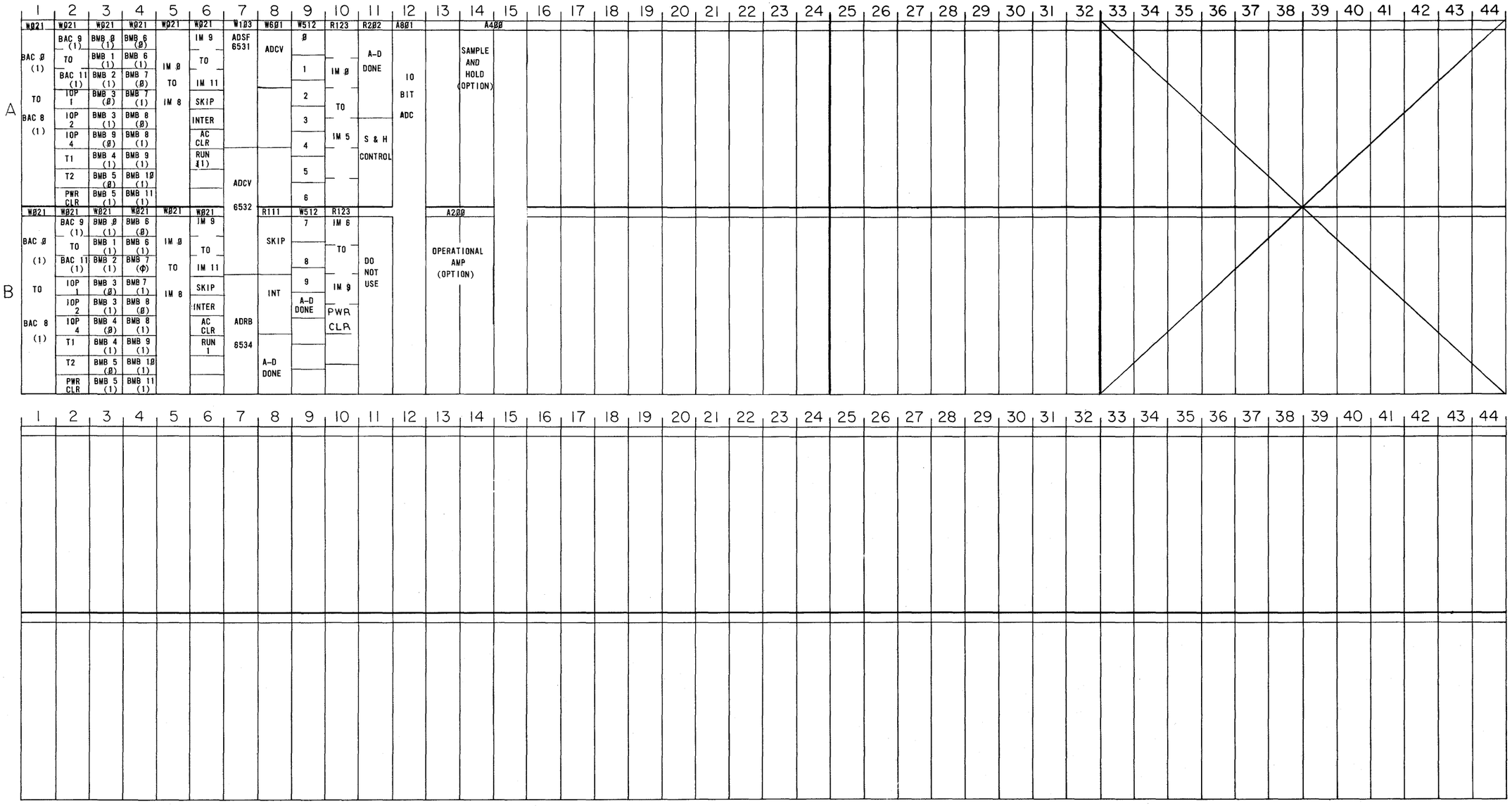


FIG 9


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44
A
B
W021
BAC Ø (1)
TO
BAC 8 (1)
BAC 9 (1)
TO
BAC 11 (1)
IOP 1
IOP 2
IOP 4
T1
T2
PWR CLR
BMB Ø (1)
BMB 1 (1)
BMB 2 (1)
BMB 3 (Ø)
BMB 3 (1)
BMB 9 (Ø)
BMB 4 (1)
BMB 5 (Ø)
BMB 5 (1)
BMB 6 (Ø)
BMB 6 (1)
BMB 7 (Ø)
BMB 7 (1)
BMB 8 (Ø)
BMB 8 (1)
BMB 9 (1)
BMB 10 (1)
BMB 11 (1)
IM Ø TO IM 8
IM 9
TO
IM 11
SKIP
INTER
AC CLR
RUN (1)
W103
ADSF 6531
ADCV
6532
ADRB
6534
W601
ADCV
R111
SKIP
INT
A-D DONE
W512
Ø
1
2
3
4
5
6
7
8
9
A-D DONE
R123
IM Ø
TO
IM 5
IM 6
TO
IM 9
PWR CLR
R202
A-D DONE
S & H CONTROL
DO NOT USE
A801
10 BIT ADC
A400
SAMPLE AND HOLD (OPTION)
A200
OPERATIONAL AMP (OPTION)