Digital Equipment Corporation
Maynard, Massachusetts

digital

DEC-8E-HR3B-D-VT8-E

VT8-E
HIGH SPEED VIDEO DISPLAY TERMINAL AND CONTROL OPTION

The information in this preliminary manual will become, in its final form, a part of the *PDP-8/E/F/M Maintenance Manual, Volume 3.*

PRELIMINARY

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CHAPTER 12
VT8-E HIGH SPEED VIDEO DISPLAY TERMINAL AND CONTROL

SECTION I INTRODUCTION

The VT8-E, a video display option for the PDP-8/E, PDP-8/F, and PDP-8/M, consists of a display monitor and three quad modules that plug into the OMNIBUS. The quad modules control the display monitor operation and can interface the VT8-E to either an LA30A-P DECwriter or an LS01-E Centronics Line Printer. Up to four VT8-E display options can be used simultaneously with the same computer.

The display monitor comprises a CRT with its associated power supply, deflection circuits and video circuits, and a Teletype® keyboard with its control logic. The monitor is contained in a desk-top enclosure (Figure 12-1).

Data is transferred from the monitor keyboard to the computer AC Register by program interrupts. Data to be displayed by the monitor is transferred from memory by Single Cycle Data Breaks to the VT8-E OMNIBUS control modules. The control modules convert the parallel data to serial video information that is displayed on the viewing screen. The monitor can display both alphanumeric characters and graphic symbols, either alone or in combination.

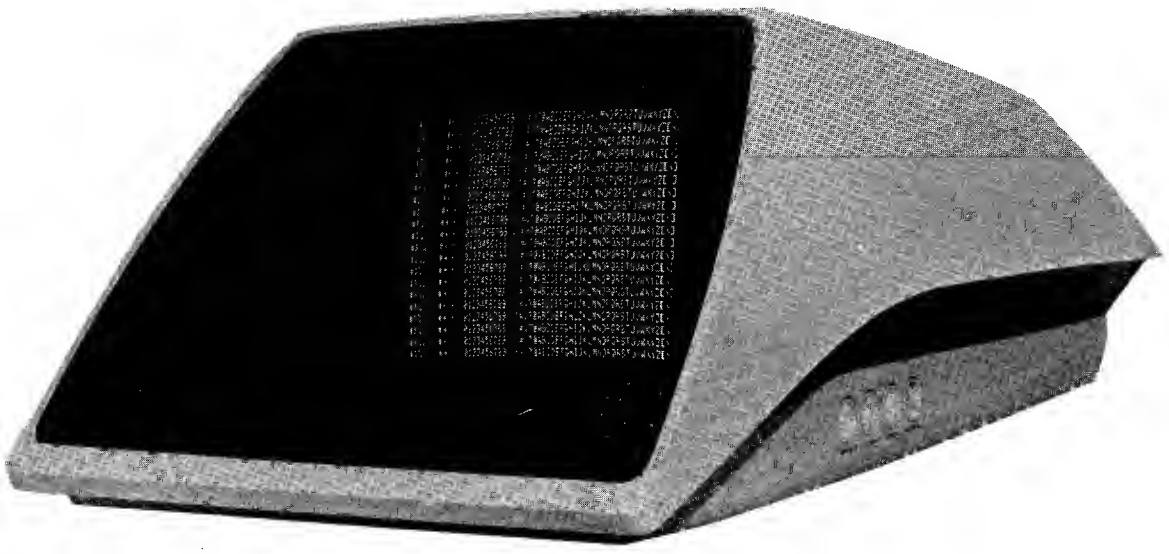


Figure 12-1 VT8-E Display Monitor

® Teletype is a registered trademark of Teletype Corporation.

Neither the LA30A-P nor the LS01-E line printers is discussed here. Details concerning these two printers should be obtained from the respective maintenance manuals. Publications and documents relevant to the VT8-E are:

a. *PDP-8/E and PDP-8/M Small Computer Handbook* — DEC, 1972

b. *PDP-8/E, PDP-8/F, and PDP-8/M Maintenance Manual, Volume 1*

c. VT8-E Diagnostic; MAINDEC-08-DHVTB-A (Graphic), MAINDEC-08-DHVTA-A (Alphanumeric)

d. DEC Engineering Drawings, E-CS-M8335-0-1, E-CS-M8336-0-1, and E-CS-M8337-0-1 (interface modules)

e. DEC Engineering Drawing, D-CS-5409917-0-1 (DEC Keyboard #2)

f. DEC Engineering Drawings, D-CS-3010326-1-0 (Motorola Raster Display)

12.1 SYSTEM OPERATING SPECIFICATIONS

Operating Temperature Range	5° to 43°C
Operating Humidity Range (without condensation)	10% to 90% (Relative)
Power Requirements (display monitor)	100—130 Vac, 50 or 60 Hz ±5% single phase at 2A 200—260 Vac, 50 or 60 Hz ±5% single phase at 1A
Power Consumption (display monitor)	55W at 115V 65W at 230V

12.1.1 CRT Operating Specifications (Motorola Raster Display)

Screen Size	10-1/8 in. X 7-5/8 in.
Phosphor	P4 (white)
Deflection Type	Magnetic
Deflection Method	Raster Scan
Input Impedance (at VIDEO IN input)	75Ω ± 5%
Video Input Signal	0.9 to 2.2V with separate horizontal and vertical SYNC.
Video Pulse Rise and Fall Time	40 ns (10% to 90% point), measured at cathode with 1.0V p-p input and 30V p-p output.
Video Output Amplitude	30V p-p (minimum), measured at cathode with 1.0V p-p input.
Resolution	Screen Center — 600 lines (minimum) Screen Corners — 400 lines (minimum) (using shrinking raster method)

Horizontal Sweep Frequency	15.6 kHz
Vertical Sweep Frequency	50 or 60 Hz (selectable)
Horizontal Retrace	11 μs (maximum)
Vertical Retrace	21 horizontal lines @ 15.6 kHz
High Voltage	11 kV (minimum) @ 50 μA beam current @ 24 Vdc power supply adjustment
High Voltage Regulation	12 MΩ (maximum), for a beam current change from 50 to 150 μA @ 24 Vdc power supply adjustment.
CRT Refresh Rate	50 or 60 Hz

12.1.2 Visible Display Specifications

Screen Refresh Rate	60 or 50 frames/sec (determined by local line frequency)
Refresh Method	Raster Scan

12.1.2.1 Alphanumeric Mode

Viewing Area	8-1/4 in. (horiz) X 6-1/4 in. (vert) (32 characters/line) 8-1/4 in. X 4-1/4 in. (64 characters/line)
Character Lines	20
Character Size	0.185 in. width 0.220 in. height (32 characters/line)
	0.090 in. width 0.150 in. height (64 characters/line)
Character Spacing	
Horizontal	0.0740 in. (32 characters/line) 0.0370 in. (64 characters/line)
Vertical	0.0946 in. (32 characters/line) 0.0645 in. (64 characters/line)
Character Set	64-character ASCII set (upper case)
Character Generation Method	5 X 7 dot matrix

12.1.2.2 Graphic Mode

Viewing Area	7 in. X 6-1/4 in. (if wired for 32 alphanumeric characters per line)

	7 in. X 4-1/2 in. (if wired for 64 alphanumeric characters per line)
Display Lines	200
Flicker-Free Points per Line	189

SECTION 2 INSTALLATION AND ACCEPTANCE TEST

The VT8-E Video Display and Control are installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment.

12.2 UNPACKING

The VT8-E Display Monitor is packed in a specially designed carton to avoid damage during shipment.

NOTE
Carefully examine the VT8-E for damage as it is unpacked. Any damage should be reported immediately.

Unpack the VT8-E Display Monitor as follows:

Step	Procedure
1	Remove the Display Monitor from the shipping container.
2	Remove the polyethylene cover.
3	Remove any tape, etc., from the display monitor cabinet.
4	Remove the display monitor from the shipping skid.
5	Place the display monitor in the desired location.
6	Verify all items listed on the Inventory List shipped with the VT8-E have been received.

12.2.1 Primary Power

The Display Monitor uses a single ac power cable (permanently connected) to connect the site power source to the display monitor. The monitor operates at 110–130 Vac, 50–60 Hz, single phase, or 200–260 Vac, 50–60 Hz, single phase.

Each wire in the ac power cable is color-coded as shown in Table 12-1. The display monitor is normally supplied with a 15A connector. The selected ac service outlet must be capable of at least 2A, 110 Vac, 50 or 60 Hz, or 1A, 200 Vac, 50 or 60 Hz.

Table 12-1
AC Power Cable

Line	Wire Color	Terminal Strip Nomenclature
Frame Ground	Green	Frame Ground
Neutral/Line 2	White	Neutral or Line 2
Line 1	Black	Line 1

12.2.2 VT8-E Installation

Install the VT8-E as follows:

Step	Procedure
1	Ensure PDP-8/E power is off.
2	Ensure the Display Monitor Power Select switch, located on the side of the Display Monitor, is set correctly for the power source (115 Vac or 230 Vac).
3	Use a meter to measure the voltages on the wall receptacle and ensure that the hot, neutral, and ground connections are the same as those on the Display Monitor power connector (Table 12-1).
4	On the M8336 and M8337, ensure the 5 jumpers are installed to select only 64 or 32 characters per line. All jumpers must be installed for the same mode.
5	On the M8335 module ensure the correct device code jumpers are installed. Table 12-2 contains a list of the split lugs which should be connected in each of the 6 groups (A–F) to select one of the 64 possible device codes. Split lug locations (by groups) are shown on D-CS-M8335-0-1 Engineering Drawing cover sheet.
6	On the M8337 and M8335 modules, ensure the jumpers are installed correctly to select the priority assigned to this VT8-E (Table 12-3). Only priorities 9 (highest), 10, and 11 (lowest) may be assigned to the VT8-E. Refer to M8337-0-1 and M8335-0-1 cover sheet for jumper locations.
7	Connect J1 of the 7009042 Cable Assembly to J1 on the M8336 module.
8	Connect J2 of the 7009042 Cable Assembly to J1 on the M8335 module.
9	If a line printer is used, connect the printer cable assembly to J2 on the M8335 module.
10	Install the VT8-E modules on the OMNIBUS as shown in Figure 12-2. Refer to Figure 2-3 in Volume 1 for recommended module installation priorities. The VT8-E is not a memory option. The VT8-E modules must be installed in this order; M8336 Front M8337 Middle M8335 Rear
11	Install H851 Top Connectors as follows (Figure 12-2): *a.* Between M8336H and M8337H *b.* Between M8337E and M8335E *c.* Between M8337F and M8335F
12	Route the 7009042 Cable Assembly to the Display Monitor and connect J3 Winchester Connector to the mating connector on the rear of the console.

13 If a line printer is used, route the printer cable to the line printer and connect it.

NOTE

If more than one VT8-E is installed in one system (up to four may be installed in one system), the second control goes on the OMNIBUS directly behind the first, and the third behind the second, etc. The two controls are interconnected by installing an H851 Top Connector between M8335J of the first control and M8336J of the second control. The controls must be assigned different device codes (Tables 12-2 and 12-3).

14 Turn on PDP-8/E power and run the acceptance test in Paragraph 12.2.4.

Table 12-2
Device Code Select Jumper Installation

Device Code	Group A	Group B	Group C	Group D	Group E	Group F
00	2-3	2-3	2-3	2-3	2-3	2-1
01	2-1	2-3	2-3	2-3	2-3	2-1
02	2-3	2-3	2-3	2-1	2-3	2-1
03	2-1	2-3	2-3	2-1	2-3	2-1
04	2-3	2-3	2-3	2-3	2-1	2-1
05	2-1	2-3	2-3	2-3	2-1	2-1
06	2-3	2-3	2-3	2-1	2-1	2-1
07	2-1	2-3	2-3	2-1	2-1	2-1
10	2-3	2-3	2-1	2-3	2-3	2-1
11	2-1	2-3	2-1	2-3	2-3	2-1
12	2-3	2-3	2-1	2-1	2-3	2-1
13	2-1	2-3	2-1	2-1	2-3	2-1
14	2-3	2-3	2-1	2-3	2-1	2-1
15	2-1	2-3	2-1	2-3	2-1	2-1
16	2-3	2-3	2-1	2-1	2-1	2-1
17	2-1	2-3	2-1	2-1	2-1	2-1
20	2-3	2-1	2-3	2-3	2-3	2-1
21	2-1	2-1	2-3	2-3	2-3	2-1
22	2-3	2-1	2-3	2-1	2-3	2-1
23	2-1	2-1	2-3	2-1	2-3	2-1
24	2-3	2-1	2-3	2-3	2-1	2-1
25	2-1	2-1	2-3	2-3	2-1	2-1
26	2-3	2-1	2-3	2-1	2-1	2-1
27	2-1	2-1	2-3	2-1	2-1	2-1
30	2-3	2-1	2-1	2-3	2-3	2-1
31	2-1	2-1	2-1	2-3	2-3	2-1
32	2-3	2-1	2-1	2-1	2-3	2-1
33	2-1	2-1	2-1	2-1	2-3	2-1
34	2-3	2-1	2-1	2-3	2-1	2-1
35	2-1	2-1	2-1	2-3	2-1	2-1
36	2-3	2-1	2-1	2-1	2-1	2-1

Table 12-2 (Cont)
Device Code Select Jumper Installation

Device Code	Group A	Group B	Group C	Group D	Group E	Group F
37	2-1	2-1	2-1	2-1	2-1	2-1
40	2-3	2-3	2-3	2-3	2-3	2-3
41	2-1	2-3	2-3	2-3	2-3	2-3
42	2-3	2-3	2-3	2-1	2-3	2-3
43	2-1	2-3	2-3	2-1	2-3	2-3
44	2-3	2-3	2-3	2-3	2-1	2-3
45	2-1	2-3	2-3	2-3	2-1	2-3
46	2-3	2-3	2-3	2-1	2-1	2-3
47	2-1	2-3	2-3	2-1	2-1	2-3
50	2-3	2-3	2-1	2-3	2-3	2-3
51	2-1	2-3	2-1	2-3	2-3	2-3
52	2-3	2-3	2-1	2-1	2-3	2-3
53	2-1	2-3	2-1	2-1	2-3	2-3
54	2-3	2-3	2-1	2-3	2-1	2-3
55	2-1	2-3	2-1	2-3	2-1	2-3
56	2-3	2-3	2-1	2-1	2-1	2-3
57	2-1	2-3	2-1	2-1	2-1	2-3
60	2-3	2-1	2-3	2-3	2-3	2-3
61	2-1	2-1	2-3	2-3	2-3	2-3
62	2-3	2-1	2-3	2-1	2-3	2-3
63	2-1	2-1	2-3	2-1	2-3	2-3
64	2-3	2-1	2-3	2-3	2-1	2-3
65	2-1	2-1	2-3	2-3	2-1	2-3
66	2-3	2-1	2-3	2-1	2-1	2-3
67	2-1	2-1	2-3	2-1	2-1	2-3
70	2-3	2-1	2-1	2-3	2-3	2-3
71	2-1	2-1	2-1	2-3	2-3	2-3
72	2-3	2-1	2-1	2-1	2-3	2-3
73	2-1	2-1	2-1	2-1	2-3	2-3
74	2-3	2-1	2-1	2-3	2-1	2-3
75	2-1	2-1	2-1	2-3	2-1	2-3
76	2-3	2-1	2-1	2-1	2-1	2-3
77	2-1	2-1	2-1	2-1	2-1	2-3

Table 12-3
Priority Jumper Installation

Priority	M8337 Install Jumper	M8335 Install Jumpers
9 (highest)	W1	P9 and P10
10	W2	P9′ and P10
11 (lowest)	W3	P9′ and P10′

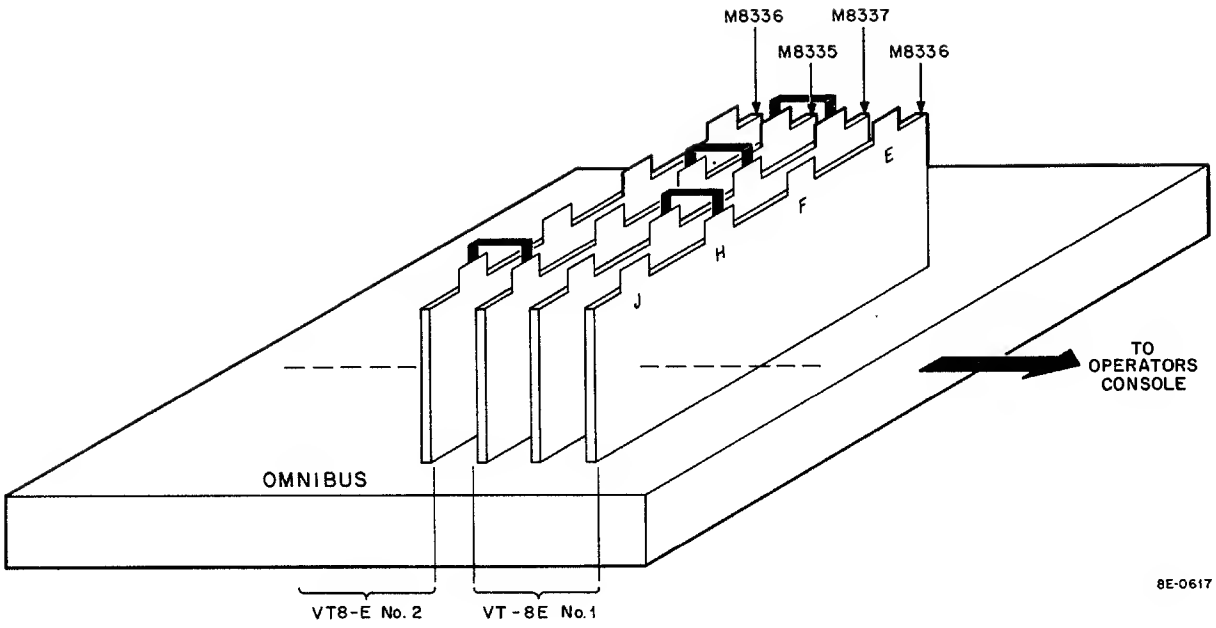


Figure 12-2 VT8-E Module Installation

12.2.3 Acceptance Test

The VT8-E is checked for proper operation by running the two diagnostic programs. Both MAINDECs referenced in the introductory remarks and the A-SP-VT8-E engineering specification give detailed instructions for their performance in the instructions shipped with the paper tapes. If problems arise, refer to the maintenance instructions, both in this manual and in Volume 1.

SECTION 3 OPERATION AND PROGRAMMING

This section provides a functional description of the VT8-E logic, operation and programming information, a list of IOT instructions, and some VT8-E programming examples.

12.3 FUNCTIONAL DESCRIPTION

Each of the functional groups of logic in the VT8-E are described in the following paragraphs (Figure 12-3). Their purpose, location (on what module), and function are provided to familiarize the reader with VT8-E operation. A detailed description of VT8-E logic and timing is given in Chapter 4. Refer to Chapter 9 of the *Small Computer Handbook* – DEC, 1972 for information about data transfers via IOT instructions and data breaks. A detailed block diagram of the VT8-E which shows data flow and the interrelationship of the functional groups is in the VT8-E Video Display Control Engineering Drawings.

12.3.1 VT8-E Printer/Keyboard Control Module (M8335)

The functional groups of logic on the M8335 module are discussed in the following paragraphs.

12.3.1.1 MD Bus Gating – Data from the MD lines is applied to the M8337 module by I/O PAUSE if IOT instructions are executed by the program or by MD EN during Single Cycle Data Breaks. Single Cycle Data Break is the method used to transfer data between memory and the display control (Paragraph 12.3.4.1).

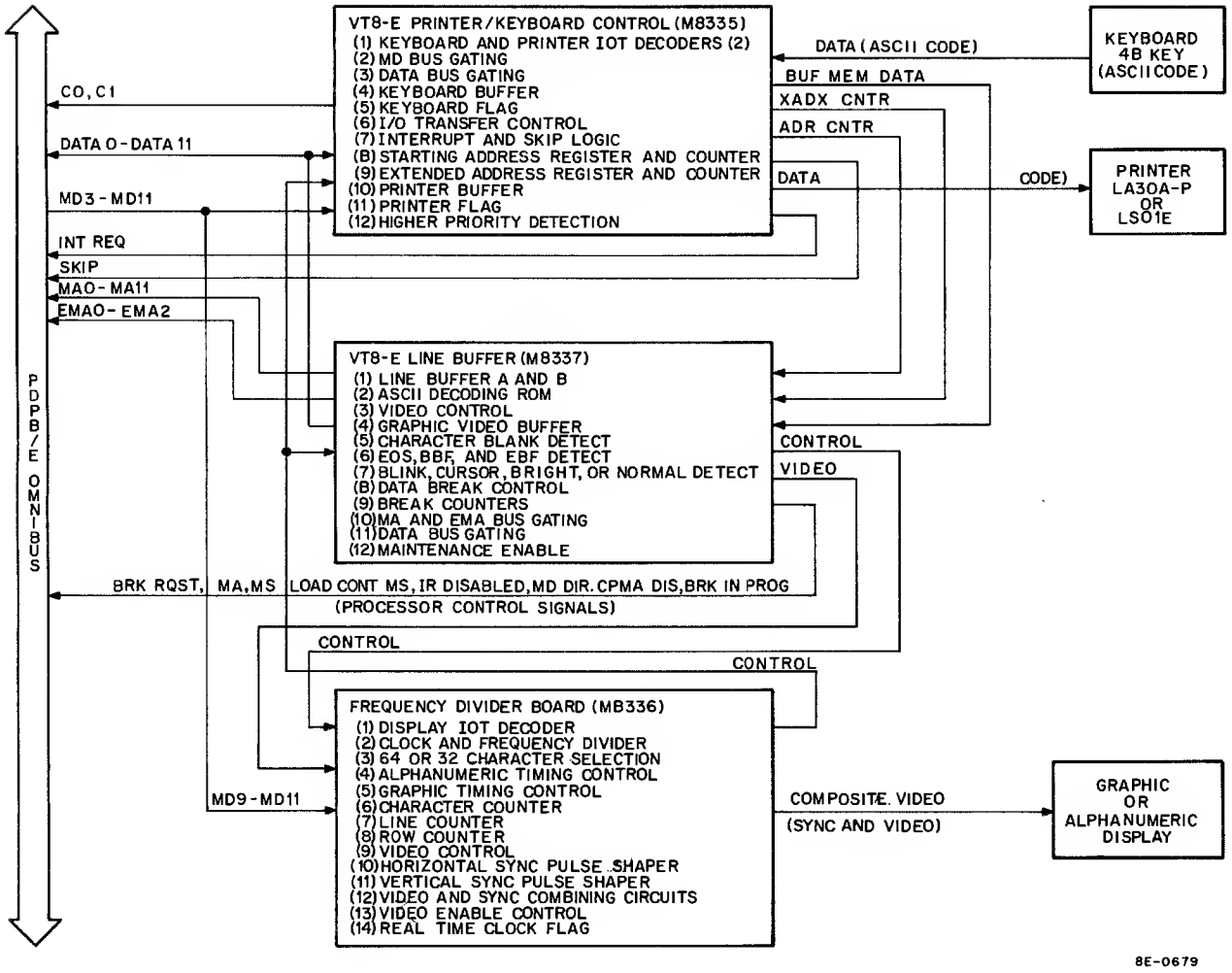


Figure 12-3 VT8-E Block Diagram

12.3.1.2 IOT Decoders – The M8335 module contains two IOT decoders, one for the printer and one for the keyboard. The decoders are assigned different device codes so that the printer IOT decoder is selected when printer IOTs are programmed, and the keyboard IOT decoder is selected when keyboard IOTs are programmed. The keyboard and printer may be assigned any two of the device codes listed in Table 12-2. The device codes assigned to the keyboard and printer must be different from each other and different from the display device code. The IOT decoders decode MD9–MD11 from the MD lines and generate control signals to control keyboard and printer operations; i.e., data transfers. The keyboard and printer instructions are listed in Paragraph 12.3.4.

12.3.1.3 Data Bus Gating – The Data Bus gates are enabled and DATA0–DATA11 are applied to the M8337 logic when the following occur:

a. If the program executes the PNPC or PNLP instructions to load the Printer Buffer.

b. If the program executes a DPLA instruction to load the Starting Address Register or a DPG0 instruction to load the Extended Starting Address Register.

c. During a Single Cycle Data Break. DAT0–DATA8, 9, or 10 monitored by the VT8-E during data breaks to determine if the VT8-E has the highest priority for a data break.

12.3.1.4 Keyboard Buffer – The Keyboard Buffer receives a 7-bit ASCII code from the keyboard when one of the keys on the keyboard is pressed. The keyboard also generates a KEYBOARD STROBE which enables the 7-bit ASCII code to be transferred to the buffer and sets the KYBD flag. When the KYBD flag is set, an INT RQST is made if interrupts are enabled, or a SKIP if the DKSF instruction is executed by the program. An INT RQST or SKIP notifies the program that data in the Keyboard Buffer is available to be read into the AC. The program must transfer the data in the buffer to the AC and clear the KYBD flag so that a new 7-bit ASCII character can be transferred from the keyboard to the buffer.

12.3.1.5 I/O Transfer Control – The I/O Transfer Control logic determines the direction of data flow on the Data Bus and whether the AC is cleared or not. C0 and C1 (the C lines) are asserted by IOT instructions which transfer data to or from the AC.

12.3.1.6 Interrupt and Skip Logic – The Interrupt and Skip logic allows the program to enable the interrupts and generate an INT RQST when the KYBD and PRINT DONE flags are set or to check the flags using a SKIP instruction; i.e., the DKSF instruction.

12.3.1.7 Interrupt Logic – The Keyboard and Printer Interrupt logic is enabled if bit 11 in the AC is set (1) when the DKIN instruction is executed by the program. If the interrupts are enabled, an INT RQST is made when the KYBD flag is set or the PRINT DONE flag is set. The KYBD flag is set when a keyboard key is pressed, and the PRINT DONE is set when the printer has finished printing a character.

12.3.1.8 Starting Address Register and Counter (SAR) – The Starting Address Register (SAR) is a 12-bit register that is loaded from the AC with the memory address of the first word to be transferred by the Single Cycle Data Break facility. The contents of SAR are transferred to the Starting Address Counter after the DPG0 instruction is executed by the program and the counter is incremented at the end of each data break to select the next sequential memory address. The contents of the counter are applied to the Memory Address lines (MA0–MA11) to address a location in memory.

12.3.1.9 Extended Starting Address Register – The Extended Starting Address Register (XSAR) is loaded from bits 6, 7, and 8 of the AC by the DPG0 instruction. The contents of XSAR are transferred to the XSAR Counter and used to select a field in memory for data transfers. The XSAR is incremented when the SAR overflows to select the next memory field. At this time the SAR starts reading memory locations in the newly selected memory field.

12.3.1.10 Printer Buffer – The Printer Buffer is a 7-bit register that is loaded from the AC by the PNLP instruction. The data from the AC contains a 7-bit ASCII code for a character to be printed. The seven data bits are transferred along with a PRINT STROBE pulse, and when the Print operation is completed, the PRINT DONE flag is set. If interrupts are enabled, an INT RQST is made at this time, or if the flag is checked by the PNSK instruction, the SKIP line is grounded. The program may perform a routine to transfer another character to the printer at this time.

12.3.1.11 PRINT DONE Flag – The PRINT DONE flag is set each time the printer completes a print operation to inform the program that the printer is ready to accept a new character.

12.3.1.12 Higher Priority Detection – The Higher Priority Detection logic monitors the Data Bus to determine if the VT8-E has the highest priority for a data break. If there are any peripherals connected to the OMNIBUS that have a higher priority than the VT8-E, one of the lines on the Data Bus will be low to prevent the VT8-E from doing a data break. As an example, if the peripheral assigned the highest priority wants to do a data break, DATA0 is asserted (low) and the VT8-E cannot do a data break until DATA0 goes high at the completion of the other peripheral's data break. When the VT8-E is ready to do a data break, DATA9, DATA10, or DATA11 will be asserted low to prevent peripherals with a lower priority from doing a data break before the VT8-E. As can be seen from the previous discussion, the VT8-E may be assigned one of the three lowest priorities.

12.3.2 VT8-E Line Buffer Module (M8337)

The functional groups of logic located on the VT8-E Line Buffer Module are discussed in the following paragraphs.

12.3.2.1 Line Buffers A and B – Line Buffers A and B provide temporary storage of 32 or 64 words from memory in the Alphanumeric mode or 32 words from memory in the Graphic mode. In the Alphanumeric mode the word from memory (Figure 12-7) selects the visible field, display mode, and character to be displayed. In the Graphic mode, the word from memory (16 words per line) consists of 1s (display a dot) and 0s (do not display a dot) to produce a line on the face of the CRT. The display mode (Alphanumeric or Graphic) is selected by bit 10 (0 → ALPHA and 1 → GRAPHIC) from the AC when the DPG0 instruction is executed by the program.

Each alphanumeric character is displayed on the face of the CRT in a 5 (width) X 7 (height) dot matrix. To display one row of characters (32 or 64 characters), the Display Monitor makes 10 horizontal sweeps across the face of the CRT. The first two scans are used to load the Line Buffers from memory via the Single Cycle Data Break. The third scan addresses a blank ROM location and the remaining seven scans display the alphanumeric data. The first of the seven scans displays the first line of each character in the row of characters to be displayed, the second scan the second line, etc., until seven scans are completed to display a row of characters (32 or 64). When the tenth scan is completed, the program must set up for a new break and initiate a new break cycle to reload the Line Buffers if additional rows of characters (20 maximum) are to be displayed. During the display operation the 7-bit ASCII code (Figure 12-7) is decoded by the ASCII decoding ROMS to generate the video signals to be displayed and the four control bits are decoded to determine the display mode and visible field. A display may be stopped after any number of characters have been displayed, if the display is less than 20 rows, to save computer time. This is done by setting CB1 and CB2 to 1s when the last character is displayed.

In the Graphic mode, data is displayed on the face of the CRT in a 189 (width) X 200 (height) dot matrix. Each line (189 dots) requires 16 12-bit words. The last three bits of the sixteenth word are not used. Each bit of the data word represents a dot or space on the face of the CRT. A logical 1 causes a dot and a logical 0 leaves a space. As an example, 16 words of data containing all 1s displays a row of dots on the face of the CRT. In the Graphic mode, 3200 (200 X 16) words must be defined because there is no way to generate End-of-Screen (EOS). If the full screen is not used, the remainder of the memory locations used should contain all 0s.

12.3.2.2 ASCII Decoding ROMs – The ASCII decoding ROMs decode the 7-bit ASCII code from the Line Buffers and generate a video signal for each line of each character to be displayed. After the start of a horizontal scan, data is shifted out of the Line Buffers to address (the buffer is in a recirculating mode, thus an end-around shift) a ROM character generator location and generate video for one line of the character. ROM character generator locations are addressed seven times (once for each horizontal scan). The video signals generated each time it is addressed are changed by the assertion of signals inside the ROM to change the video pattern and produce the desired character after seven scans. The video out of ROM (VIDEO1–VIDEO5) is applied to the Alphanumeric Video Buffer where it is shifted out to the Video Control logic as five serial video pulses. These pulses will cause dots or spaces to appear on the face of the CRT and after seven scans, an alphanumeric character is formed.

12.3.2.3 Graphic Video Buffer – In the Graphic mode, the contents of the Line Buffer are transferred one word at a time to the Graphic Video Buffer. From the Graphic Video Buffer the 12-bit word is converted to serial video pulses and applied to the Video Control logic. Dots are displayed for data 1s and spaces for data 0s.

12.3.2.4 Character Display Mode Detection Logic – The Character Display mode is determined by CB3 and CB4 (Figure 12-7) of the data word from memory. As shown in Figure 12-7, the character may be displayed in the Normal, Blink, Bold, or Cursor modes. The Mode Detection logic decodes CB3 and CB4 to assert the control signals necessary to select the four modes.

12.3.2.5 Visible Field Detection Logic – The visible field is determined by CB1 and CB2 (Figure 12-7) of the data word. As shown in Figure 12-7, the character may be displayed in the mode selected by CB1 and CB2 (NOP), a

blank field may be ended and the display enabled (EBL), a blank field may be started (BBF) or an End of Screen (EOS) may be selected to end the display. EOS is particularly helpful because it allows smaller displays to be displayed without using the entire core buffer. This saves core buffer space and reduces processor loading.

12.3.2.6 Single Cycle Data Break Control Logic – The Single Cycle Data Break Control logic is used to force the processor into the Direct Memory Access (DMA) state and transfer data between core memory and the VT8-E Line Buffers via the Memory Data lines. Memory is addressed by the outputs of Starting Address and Extended Starting Address counters which are applied to the Memory Address lines at the beginning of the break cycle.

12.3.2.7 Processor Control Signals – When the processor is forced into the DMA state, the VT8-E must generate control signals to control the processor. The control signals required to accomplish this are shown in Figure 12-3 and explained in Chapter 9 of the *Small Computer Handbook* – DEC, 1972.

12.3.2.8 Break Counters – The Break Counters are used to count the words in a data transfer. The counters overflow after 32 words are transferred in the 32 character mode or after 64 words are transferred in the 64 character mode to stop data transfers and release the processor.

12.3.2.9 MA and EMA Bus Gates – The MA and EMA Bus Gates apply the contents of the Starting Address Counter and Extended Starting Address Counter to the OMNIBUS MA lines during a data transfer. This allows the selection of a memory field and memory location to be used in a data transfer.

12.3.2.10 Data Bus Gates – The Data Bus gates are enabled when the DPMD instruction is executed by the program to transfer data to the Data Bus. This allows VT8-E registers and buffers to be read into the AC for display or evaluation by the program. To read the Display Buffers and Register with IOT instructions the Maintenance logic must be enabled.

12.3.2.11 Maintenance Enable – The Maintenance logic is enabled by the DPSM instruction. This allows the program to read the VT8-E registers and buffers using the maintenance instructions. It also allows data breaks to be taken by the VT8-E at a rate determined by the program.

12.3.2.12 Frequency Divider Board (M8336) – The functional groups of logic on the M8336 module are discussed in the following paragraphs.

12.3.2.13 Display IOT Decoder – The Display IOT Decoder decodes the Display instructions and generates the necessary control signals to set up for data breaks, maintenance operations, and data transfers using IOT instructions. The decoder is enabled when I/O PAUSE is asserted and the device code assigned to the display for this VT8-E is decoded and decodes bits MD9–MD11 of the IOT instruction. At this time the C lines are asserted to control the direction of the data transfer, INTERNAL I/O is asserted to prevent the processor from performing other IOTs, and the instruction is executed by the VT8-E.

12.3.3 VT8-E Clock and Frequency Divider (M8336)

The VT8-E Clock and Frequency Divider generates the necessary CRT sync pulses and control signals required to display data on the CRT. The timing chain consists of a 21.84 MHz crystal controlled oscillator and a chain of divide-by counters with selected outputs used to generate sync and control signals. Jumpers are provided to allow the selection of 64 or 32 character display control signals. These jumpers allow control signals of different frequencies to be selected for the display of 32 or 64 characters per row. The counters in the timing chain and their function are discussed in detail in Paragraph 12.4.2.2.

12.3.3.1 Real Time Clock Flag – The Real Time Clock flag is set (1) at the start of each vertical retrace. If interrupts are enabled, an interrupt request is made, or if a Skip instruction is being executed by the program, the SKIP bus is grounded and the program will skip an instruction.

12.3.3.2 Video and Sync Combining Circuits – The Video and Sync Combining circuits combine the horizontal and vertical sync with the video pulses from the ROM Character Generator to produce a composite video signal.

12.3.4 IOT Instructions

The following instructions are used to program the VT8-E.

12.3.4.1 Display Instructions – The Display instructions assume device code 05 is used. There are 64 possible device codes which can be used (Table 12-2) for the display. The device code for the display, keyboard, and printer must be different (e.g., device code 03 for the keyboard, 04 for the printer, and 05 for the display). If more than one VT8-E is installed in the same system, three new device codes must be selected for the second VT8-E. They must also be different from each other and different from the device codes assigned to other PDP-8/E options installed in the system.

Load Starting Address Register (DPLA)

Octal Code: 6050

Operation: Transfer the contents of the AC to the Starting Address Register (SAR) and clear the AC. The AC must contain the address of the first memory location to be used in a data transfer. The contents of the SAR are transferred to the Address Counters and incremented at the end of each Single Cycle Data Break. This allows the sequential selection of locations in memory for data transfers.

Load Extended Starting Address (DPGO)

Octal Code: 6051

Operation: Transfer the contents of AC10 and AC11 to the Mode Select logic, and AC6–AC8 to the Extended Starting Address Register (XSAR). AC10 and AC11 are used to select Alphanumeric or Graphic mode and enable or disable the interrupt system as follows:

AC10	AC11	
0	0	Alphanumeric Mode, Interrupt Disabled
0	1	Alphanumeric Mode, Interrupt Enabled
1	0	Graphic Mode, Interrupt Disabled
1	1	Graphic Mode, Interrupt Enabled

AC6–AC8 must contain the memory field to be used in a data transfer. The XSAR Register is incremented when the SAR overflows at the end of each memory field to select the next memory field. The SAR selects the first location (0000) in the new memory field. Data transfers may start immediately after this instruction is executed.

STOP the Display (DPSM)

Octal Code: 6052

Operation: STOP the display and inhibit video and VT8-E initiated data breaks. This instruction also transfers AC11 and AC6–AC8 from the AC to the Maintenance logic and the Extended Starting Address Register. If AC11 is 1, the Extended Address Register is loaded with the contents of AC6–AC8. If AC11 is 0, the contents of the Starting Address Register are transferred to the Address Counters and the VT8-E is set up for a maintenance break. The AC must contain the memory field in AC6–AC8 and AC11 must be 1 or 0 to determine which operations are to be done before this instruction is executed.

Maintenance Instruction (DPMB)

Octal Code: 6053

Operation: Transfer the contents of the memory location specified by the Address Counter to the Data Buffer. The Address Counter is incremented by 1 to select the next location in memory.

Maintenance Instruction (DPMD)

Octal Code: 6054

Operation: Jam-transfer the contents of the Data Buffer to the AC. Note that the DPMB and DPMS may be used to transfer data from memory to the Data Buffer and then to the AC where it is displayed. This could aid in troubleshooting the VT8-E.

Maintenance Instruction (DPMS)

Octal Code: 6055

Operation: Transfer the contents of the Extended Address Counter to AC6—AC8 and the state of the SENSE switch into AC0 (Figure 12-4). This allows the program to determine what memory field is selected and determine the condition of the SENSE switch. Bit 0 is a logical 1 when the SENSE switch is on and a logical 0 when the SENSE switch is off. This switch is located on the keyboard and the programmer determines its use and meaning.

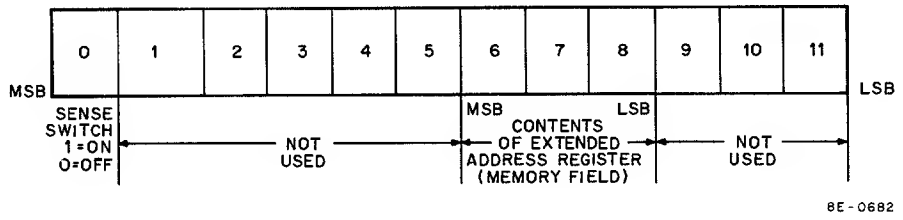


Figure 12-4 Extended Address and Sense Switch Data

Skip On Real Time Clock Flag (DPCL)

Octal Code: 6056

Operation: Skip the next instruction if the Real Time Clock flag is set (1) and clear the flag. Real Time Clock flag is set at the start of each vertical retrace.

Generate A Bell Tone (DPBL)

Octal Code: 6057

Operation: Generate a half-second audible tone for use as a bell. This tone can be heard by the operator and can be used to alert the operator that he must respond; i.e., supply data to the program via the keyboard.

12.3.4.2 Keyboard Instructions – The keyboard instructions assume a device code of 03 has been selected for the keyboard.

Clear Keyboard Flag (DKCF)

Octal Code: 6030

Operation: Clear the Keyboard flag. The Keyboard flag is set when the Keyboard transmitter is ready to transfer data, usually after one of the keyboard keys has been pressed.

Skip on Keyboard Flag (DKSF)

Octal Code: 6031

Operation: Skip the next sequential instruction if Keyboard flag is set. Keyboard flag sets when one of the keyboard keys has been pressed to supply data to the program.

Clear Keyboard Flag and AC (DKCC)

Octal Code: 6032

Operation: Clear the Keyboard flag and the AC.

Logically OR Keyboard Buffer and the AC (DKOB)

Octal Code: 6034

Operation: Logically OR the contents of the Keyboard Buffer with AC5—AC11, deposit the result in AC5—AC11, and transfer a 1 to AC4. AC0—AC03 remain unchanged. When DKOB is combined with the CLA instruction, the contents of the Keyboard Buffer are transferred to AC5—AC11.

Enable Keyboard Printer Interrupt (DKIN)

Octal Code: 6035

Operation: Enable Keyboard Printer interrupt if AC11 = 1 or disable if AC11 = 0. AC11 must be set to 1 or 0 before this instruction is executed by the program.

Read Keyboard Buffer (DKRB)

Octal Code: 6036

Operation: Jam-transfer the contents of the Keyboard Buffer to AC5—AC11 (Figure 12-5), set AC4 to 1, clear AC0—AC3, and clear the Keyboard flag. AC5—AC6 contains a 7-bit ASCII code which represents the key pressed on the keyboard.

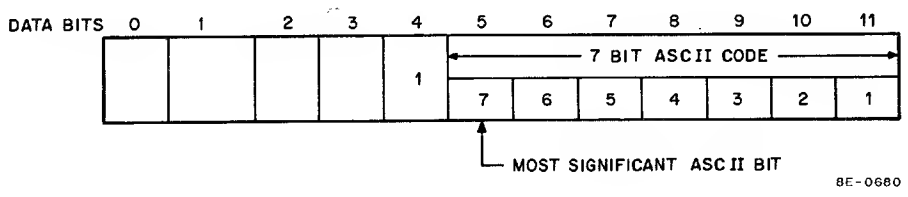


Figure 12-5 Keyboard Data Format

12.3.4.3 Printer Instructions – The following instructions assume a device code of 04 is used for the printer.

Set Printer Flag (PNSF)

Octal Code: 6040

Operation: Set the Printer flag

Skip on Print Done Flag (PNSK)

Octal Code: 6041

Operation: Skip the next sequential instruction if the Print DONE flag is set.

Clear Printer Flag (PNCF)

Octal Code: 6042

Operation: Clear the Printer flag.

NOTE
Octal Code 6043 is not used.

Load Printer Buffer (PNLP)

Octal Code: 6044

Operation: Load the Printer Buffer from AC5–AC11 (Figure 12-6) and Print. AC5–AC11 contains a 7-bit ASCII code which determines the character to be printed.

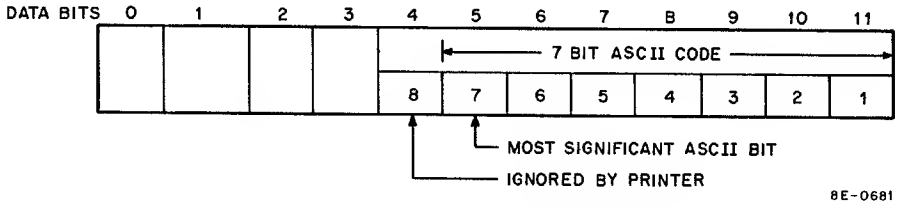


Figure 12-6 Printer Data Format

Skip on Keyboard or Printer Interrupt (PNSI)

Octal Code: 6045

Operation: Skip if the interrupt is enabled and either the Keyboard or Print DONE flag is set.

Load Printer Buffer (PNPC)

Octal Code: 6046

Operation: Load Printer Buffer from AC5–AC11 (Figure 12-6), Clear Print DONE flag, and Print. The 7-bit ASCII code determines the character to be printed.

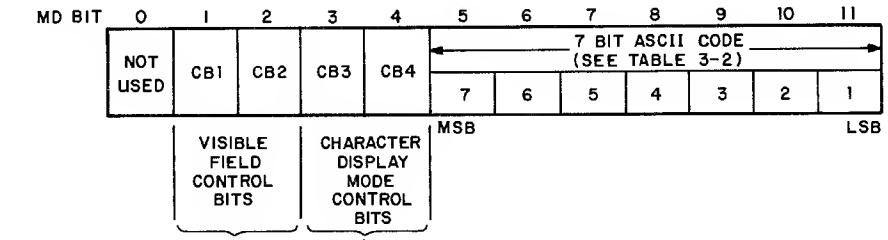
12.3.5 Display Data Format

The two types of data that can be displayed on the VT8-E CRT are alphanumeric and graphic data.

12.3.5.1 Alphanumeric Data Format – Alphanumeric data displayed on the CRT is determined by the 12-bit word (Figure 12-7) transferred from memory during a Single Cycle Data Break. This word determines the visible field, character display mode, and the character to be displayed as shown in Figure 12-6. The VT8-E can display 20 lines of alphanumeric information; 64 normal sized characters or 32 enlarged characters can be displayed on each line.

NOTE

EOS allows termination of the display and LF code 012 allows termination of the current row. Both termination methods save core memory and computer time for display with less than 20 lines.



CB1	CB2	VISIBLE FIELD CONTROL BITS		CB3	CB4	CHARACTER DISPLAY MODE CONTROL BITS	
0	0	NOP	IF IN VISIBLE FIELD, DISPLAY CHARACTER IN BITS 5-11 ACCORDING TO CB1, CB2.	0	0	NORMAL	DISPLAY THE CHARACTER IN BITS 5-1 AT NORMAL INTENSITY IF IN VISIBLE ZONE.
0	1	EBF	END BLANK FIELD. ENABLE VIDEO STARTING WITH THIS CHARACTER.	0	1	BLINK	BLINK THIS CHARACTER AT A 1.9Hz RATE (1.6Hz FOR 50Hz SYSTEMS) IF IN VISIBLE ZONE.
1	0	BBF	BEGIN BLANK FIELD. DISABLE VIDEO FOR THIS CHARACTER AND THOSE FOLLOWING. BLANK FIELD CAN BE TERMINATED BY EBF CONTROL CODE.	1	0	BOLD	DISPLAY THIS CHARACTER AT INCREASED INTENSITY IF IN VISIBLE ZONE.
1	1	EOS	END OF SCREEN. THE PREVIOUS CHARACTER IS THE LAST TO APPEAR ON THE SCREEN. VIDEO AND DATA BREAKS ARE INHIBITED UNTIL THE NEXT VERTICAL RETRACE. THIS ALLOWS ABREVIATED DISPLAY BUFFERS WHEN IT IS NOT DESIRED TO USE THE ENTIRE SCREEN. THIS SAVES CORE BUFFER SPACE AND REDUCES PROCESSOR LOADING.	1	1	CURSOR	DISPLAY THIS CHARACTER AS A CURSOR IF IN A VISIBLE ZONE. THE CHARACTER AND ITS DOT MATRIX COMPLEMENT ARE DISPLAYED ALTERNATLY AT A 3.7Hz RATE (3.1Hz FOR 50Hz SYSTEMS).

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Figure 12-7 Alphanumeric Display Data Format

12.3.5.2 Graphic Data Format – The VT8-E is capable of displaying graphic information on a 189 (width) X 200 (height) dot matrix. Each dot position corresponds to a bit of a data word in the core buffer. The first word of the buffer defines the first 12 dots on the first row. Bit 0 is the first to be displayed and bit 11 the last. If a bit is set to 1, a dot is displayed and if it is set to 0, no dot is displayed. Sixteen 12-bit words are required to display one line of graphic data. The last 3 bits of the sixteenth word are not used. As an example, 16 words of all 1s (7777) from memory would cause a line of 189 dots to be displayed on the face of the CRT. In the Graphic mode there is no way to terminate the buffer short of 3200 words (200 lines), thus the entire buffer must be defined even if a major portion is blank.

12.3.6 Display Monitor and Keyboard Switches and Controls

12.3.6.1 Display Monitor Switches and Controls – Table 12-4 lists the switches and controls found on the Display Monitor enclosure.

Table 12-4
Switches and Controls

Control/Switch	Location	Function
CONTRAST Control	Right-hand side	Used to adjust the picture for contrast.
BRIGHTNESS Control	Right-hand side	Used to adjust the CRT brightness (intensity).
VERTICAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
HORIZONTAL Control	Right-hand side	Used to synchronize the raster in the horizontal direction.
ON/OFF Switch	Keyboard upper-right corner	Applies primary power when in the ON position.
115V/230V	Right-hand side of CRT frame	Selects 115V or 230V as primary power for the display.
AC Circuit Breaker pushbutton	Rear panel	Resets circuit breaker after momentary fault (do not hold in).
SENSE switch	Right-hand side	Use determined by the programmer ON = logical 1 OFF = logical 0

12.3.6.2 Keyboard Controls – The basic function of the Keyboard is to provide a convenient, on-line method of transmitting ASCII-coded characters to the CPU for processing and, perhaps, display on the VT8-E CRT screen. The keyboard transmits an ASCII code directly to the computer each time a key is pressed, and the computer, in turn may transmit the character code to the VT8-E Control Logic. The Control Logic determines if the received data is to be displayed or used to control the displayed text format.

The keyboard can transmit either full ASCII or a 97-character subset. The selected code is determined by an internal selector switch. With the switch set to position 1, the keyboard transmits the full ASCII character set listed in Table 12-5. With the internal switch set to position 2, the keyboard transmits the 97-character ASCII subset listed in Table 12-6.

The VT8-E Display Monitor does not display lower case alphabetical characters. However, it can receive both upper and lower case characters, which are interpreted and displayed as upper case characters (Table 12-7).

Table 12-5
VT8-E Transmit Codes — Full ASCII Operation

Bit No. 7 6 5 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0			space	0	@	P	`	p
0 0 0 1			!	1	A	Q	a	q
0 0 1 0			"	2	B	R	b	r
0 0 1 1			#	3	C	S	c	s
0 1 0 0			$	4	D	T	d	t
0 1 0 1			%	5	E	U	e	u
0 1 1 0			&	6	F	V	f	v
0 1 1 1			'	7	G	W	g	w
1 0 0 0	C← (BS)	C→ (CAN)	(	8	H	X	h	x
1 0 0 1	HT		)	9	I	Y	i	y
1 0 1 0	LF	C↑ (SUB)	*	:	J	Z	j	z
1 0 1 1	C↓ (VT)	ALT	+	;	K	[	k	{
1 1 0 0			,	<	L	\	l	|
1 1 0 1	CR	HOME (GS)	-	=	M	]	m	}
1 1 1 0		ERASE LINE (RS)	.	>	N	^	n	~
1 1 1 1		ERASE SCREEN (US)	/	?	O	_	o	DEL (rub out)

CTRL

Shifted

Table 12-6
VT8-E Transmit Codes – Half ASCII Operation
(switch in position 2)

Bit No. 7 6 5 / 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 (0) 0	1 1 (0) 1
0 0 0 0			space	0	@	P	@	P
0 0 0 1			!	1	A	Q	A	Q
0 0 1 0			"	2	B	R	B	R
0 0 1 1			#	3	C	S	C	S
0 1 0 0			$	4	D	T	D	T
0 1 0 1			%	5	E	U	E	U
0 1 1 0			&	6	F	V	F	V
0 1 1 1			'	7	G	W	G	W
1 0 0 0	C← (BS)	C→	(	8	H	X	H	X
1 0 0 1	HT		)	9	I	Y	I	Y
1 0 1 0	LF	C↑	*	:	J	Z	J	Z
1 0 1 1	C↓		+	;	K	[	K	[
1 1 0 0			,	<	L	\	L	\
1 1 0 1	CR	HOME	-	=	M	]	M	ALT
1 1 1 0		ERASE LINE	.	>	N	^	N	^
1 1 1 1		ERASE SCREEN	/	?	O	_	O	DEL (rub out)

Shifted

Table 12-7
VT8-E Receiving Codes

Bit No. 7 6 5 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0 0	@	P	space	0	@	P	space	0
0 0 0 1	A	Q	!	1	A	Q	!	1
0 0 1 0	B	R	"	2	B	R	"	2
0 0 1 1	C	S	#	3	C	S	#	3
0 1 0 0	D	T	$	4	D	T	$	4
0 1 0 1	E	U	Z	5	E	U	%	5
0 1 1 0	F	V	&	6	F	V	&	6
0 1 1 1	G	W	'	7	G	W	'	7
1 0 0 0	H	X	(	8	H	X	(	8
1 0 0 1	I	Y	)	9	I	Y	)	9
1 0 1 0	J	Z	*	:	J	Z	*	:
1 0 1 1	K	[	+	;	K	[	+	;
1 1 0 0	L	\	,	<	L	\	,	<
1 1 0 1	CR	]	-	=	M	]	-	=
1 1 1 0	N	^	.	>	N	^	.	>
1 1 1 1	O	_	/	?	O	_	/	?

12.3.7 Programming Examples

The following VT8-E programming examples are programs that may be used to display alphanumeric or graphic data on the CRT.

12.3.7.1 Graphic Display Program Example – This program displays data from the Switch Register in a 189 X 200 dot matrix. A dot is displayed for those bits on the Switch Register that are set to 1s and a space is displayed for those bits in the Switch Register that are set to 0.

Memory Location	Instruction	Mnemonic			Operation
0200	6007	VTGRPH,	CAF		/CLEAR AND INITIALIZE.
0201	1216		TAD	BUF	/LOAD THE STARTING ADDRESS
0202	6050		DPLA		/OF THE DISPLAY BUFFER INTO THE VT8-E.
0203	1221		TAD	K2	/CODE FOR GRAPHIC
0204	6051		DPGO		/DISPLAY IN GRAPHIC MODE.
0205	1217	VT,	TAD	BUFM1	/SET AUTO INDEX FOR STORING
0206	3010		DCA	10	/THE DATA IN THE SR.
0207	1222		TAD	M6200	/LENGTH OF DISPLAY BUFFER
0210	3220		DCA	COUNT	/SET COUNTER FOR FILLING BUFFER.
0211	7604		LAS		/READ DATA PATTERN FROM THE SR.
0212	3410		DCA I	10	/STORE IN BUFFER
0213	2220		ISZ	COUNT	/BUFFER FILLED.
0214	5211		JMP	.-3	/NO, CONTINUE FILLING IT.
0215	5205		JMP	VT	/RELOAD BUFFER AGAIN.
0216	0400	BUF,	400		/STARTING ADDRESS OF BUFFER.
0217	0377	BUFM1,	400-1		/STARTING ADDRESS OF BUFFER -1.
0220	0000	COUNT,	0		/COUNTER FOR FILLING BUFFER.
0221	0002	K2,	2		/GRAPHIC ENABLE WORD.
0222	1600	M6200,	-6200		/COUNT FOR FILLING BUFFER.
			$		

12.3.7.2 Alphanumeric Display Program Example – This program echos the character typed on the console keyboard on the VT8-E display. The Switch Register is ORed with the character to display the character in the Normal, Blink, Bright, or Cursor mode. The display mode is selected from the Switch Register (Figure 12-7) as follows:

0000	Normal
0200	Blink
0400	Bright
0600	Cursor

Memory Location	Instruction	Mnemonic			Operation
0200	6007	VTALPH,	CAF		/CLEAR AND INITIALIZE.
0201	1233		TAD	BUFM1	/ADDRESS OF BUFFER - 1.
0202	3010		DCA	10	/SET AUTO INDEX FOR POSITIONING
					/THE END OF SCREEN CHARACTER.
0203	1233		TAD	BUFM1	/ADDRESS OF BUFFER - 1.
0204	3011		DCA	11	/SET AUTO INDEX FOR STORING CHARACTERS.
0205	1235		TAD	EOS	/GET THE END-OF-SCREEN CHARACTER (3000).
0206	3410		DCA I	10	/PUT END OF SCREEN IN DISPLAY BUFFER AREA.
0207	1240		TAD	M2400	/SET COUNTER SO PROGRAM IS RESTARTED
0210	3234		DCA	COUNT	/AFTER A FULL SCREEN IS DISPLAYED.
					/(64 CHARACTER MODE)
0211	1232		TAD	BUF	/LOAD THE STARTING ADDRESS
0212	6050		DPLA		/OF THE DISPLAY BUFFER INTO THE VT8-E.
0213	6051		DPGO		/GO DISPLAY.
0214	6031	INPUT,	KSF		/CHARACTER YET
0215	5214		JMP	.-1	/NO, WAIT.
0216	6036		KRB		/READ THE CHARACTER.
0217	0236		AND	K177	/KEEP ONLY 7 BITS.
0220	7421		MQL		/SAVE IN THE MQ REGISTER.
0221	1235		TAD	EOS	/MOVE THE END-OF-SCREEN
0222	3410		DCA I	10	/CHARACTER UP ONE IN THE BUFFER.
0223	7604		LAS		/READ DISPLAY MODE CONTROL BITS
					/FROM THE SR.
0224	0237		AND	K600	/SAVE ONLY THE CONTROL BITS.
0225	7501		MQA		/"OR" THE CHARACTER WITH THEM.
0226	3411		DCA I	11	/STORE CHARACTER WITH CONTROL BITS.
0227	2234		ISZ	COUNT	/FULL SCREEN (64 CHAR MODE)?
0230	5214		JMP	INPUT	/NO, GET ANOTHER CHARACTER.
0231	5200		JMP	VTALPH	/YES, RESTART THE PROGRAM.
0232	0400	BUF,	400		/STARTING ADDRESS OF BUFFER.
0233	0377	BUFM1,	400-1		/STARTING ADDRESS OF BUFFER - 1.
0234	0000	COUNT,	0		/FULL SCREEN COUNTER.
0235	3000	EOS,	3000		/END-OF-SCREEN CHARACTER.
0236	0177	K177,	177		/7 BIT MASK.
0237	0600	K600,	600		/CONTROL BIT MASK.
0240	5400	M2400,	-2400		/LENGTH OF BUFFER.

SECTION 4 DETAILED LOGIC DESCRIPTION

12.4 INTRODUCTION

A simple block diagram of the VT8-E Video Display and Control is shown in Figure 12-8. The interface supplies the monitor with video and sync signals, and an audio tone. The video is either alphanumeric character information or graphic information, or a combination of the two that is made possible by switching the display mode at the screen refresh rate.

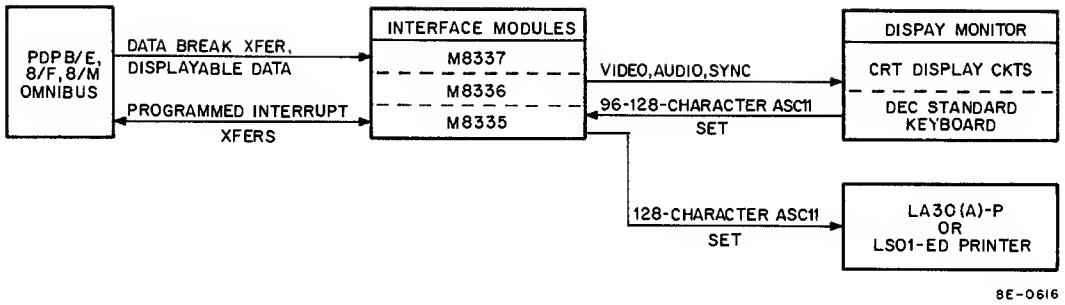


Figure 12-8 VT8-E Functional Block Diagram

The keyboard transfers data directly to the computer's AC Register by program interrupts or flags. Each character code transmitted can either be displayed or used to control the displayed text format. Data transmitted to the system printer is also transferred by program interrupts or flags. When the Interrupt System is disabled, flags are checked by the SKIP instructions.

The logic description is divided into two parts: one part concentrates on the interface logic for both the keyboard/printer and the display, while the second part concentrates on the keyboard and CRT circuits.

12.4.1 Keyboard/Printer Logic

A block diagram of the VT8-E Keyboard/Printer logic is shown in Figure 12-9. Pin assignments for OMNIBUS signals and connector signals can be found on Engineering Drawing E-CS-M8335-0-1.

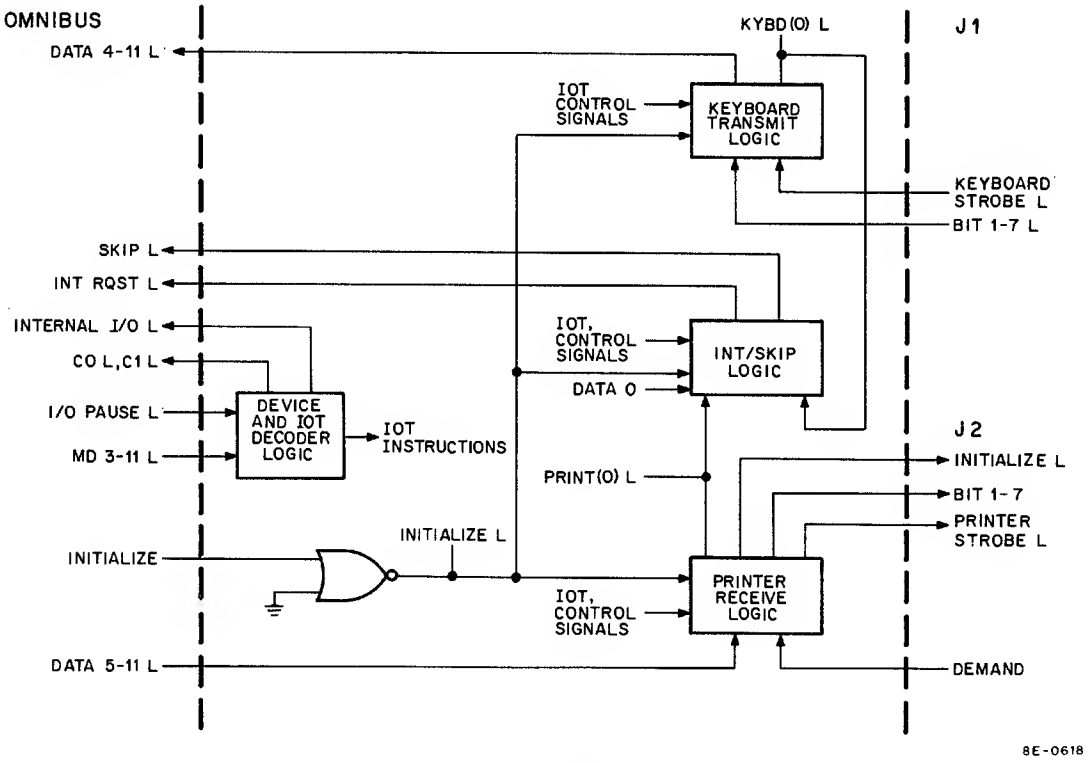


Figure 12-9 Printer/Keyboard Block Diagram

The VT8-E Keyboard/Printer logic has two distinct functions: transfer of data from the CPU AC Register to the Printer Buffer Register and transfer of data from the Keyboard Register to the AC Register. The transfer of data to the Printer Buffer is carried out by the Printer Receive logic. When the printer is able to receive data, it asserts the DEMAND signal. This signal sets the PRNT FLG flip-flop in the Printer Receive logic. The resulting PRNT (0) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal, if the VT8-E has been logically connected to the interrupt system. Alternatively, PRNT (0) L can be tested by a program skip instruction in the INT/SKIP logic. In either case, the computer ultimately proceeds to a program subroutine that begins the data transfer. When this subroutine is executed, the information is transferred from the AC Register to the DATA 5–11 lines and clocked into a 7-bit register in the Printer Receive logic. The register outputs are available at J1 as the BIT 1–7 signals. The logic then generates a PRINTER STROBE L signal that clocks the BIT 1–7 data into the Printer Buffer Register, clears the PRNT FLG flip-flop, and causes the printer to negate the DEMAND signal.

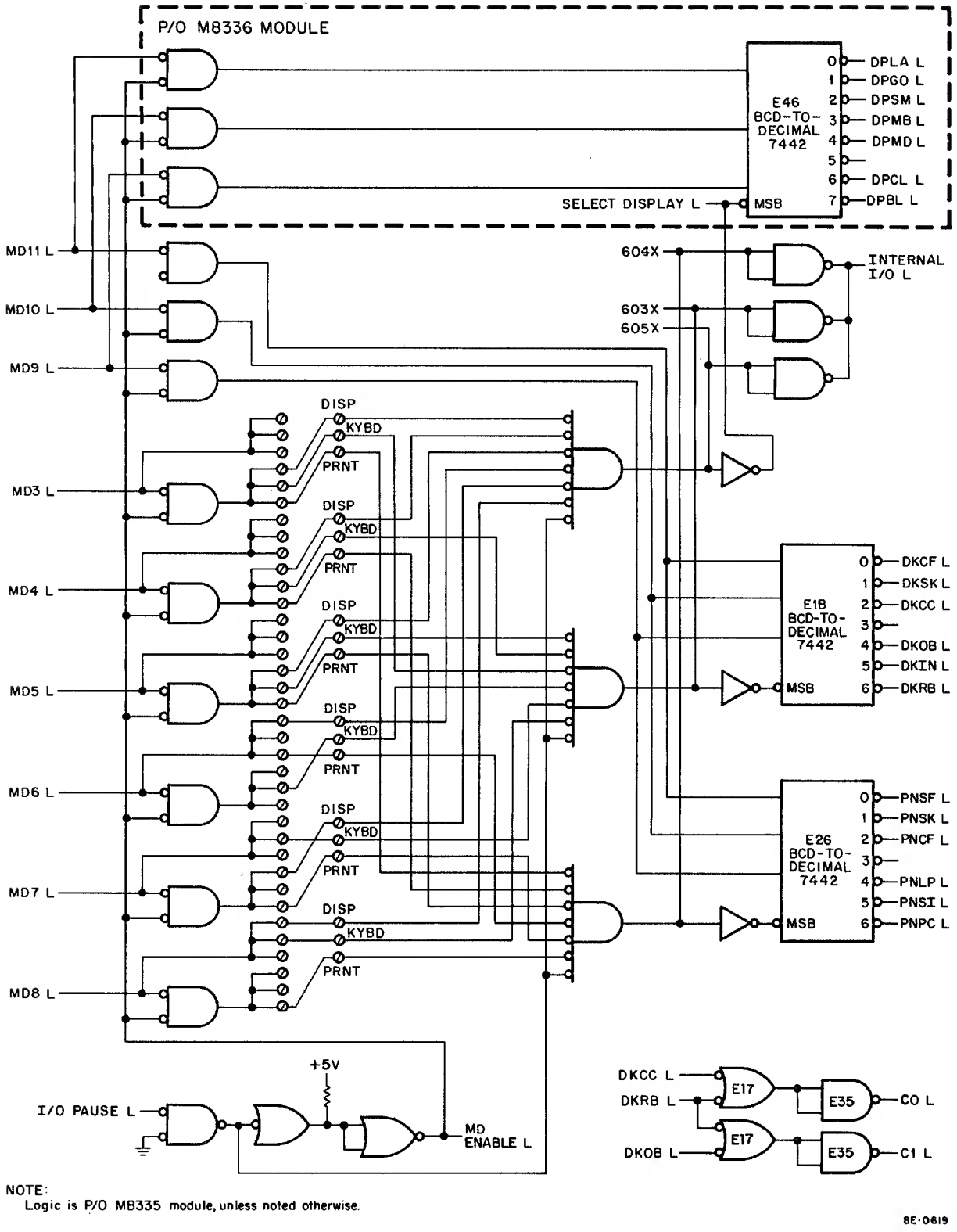
The transfer of data from the Keyboard Buffer Register to the AC Register is carried out by the Keyboard Transmit logic. When a keyboard key is pressed, information is applied, via the BIT 1–7 lines, to a 7-bit register in the Keyboard Transmit logic. When the keyboard generates a KEYBOARD STROBE L signal, the information is clocked into the 7-bit register and the KYBD FLG flip-flop is set. The KYBD (0) L signal can be tested in the INT/SKIP logic with a SKIP instruction, or the interrupt system can be used to cause the program to enter an appropriate subroutine. When the subroutine is executed, the information is gated from the register in the Keyboard Transmit logic to lines DATA 5–11 (the logic asserts the DATA 4 L signal separately so that the input character is compatible with the modified-ASCII Teletype code), then to the AC Register. The AC is loaded and, simultaneously, the KYBD FLG flip-flop is cleared.

12.4.1.1 IOT Decoder Logic – The IOT Decoder logic is shown in Figure 12-10, which includes the Video Display Decoding logic for reference. The VT8-E Keyboard/Printer uses 12 IOT instructions, 6 for the keyboard and 6 for the printer. (One of the listed printer IOTs, Skip on Printer or Keyboard Interrupt, apply to both functions and one of the keyboard IOTs, Interrupt Enable/Disable.) More than one keyboard/printer can be interfaced to the PDP-8/E at the same time. The VT8-E (or other control module) associated with each keyboard/printer must be assigned a unique device selection code for both the keyboard and the printer. Therefore, the M8335 module is fabricated with jumpers and solder terminals that allow the user to assign any one of 64 possible device selection codes to both the keyboard and the printer (care should be taken when assigning device selection codes to preclude multiple assignments of the same code). Figure 12-10 illustrates the octal codes and mnemonics that pertain when the VT8-E is manufactured. The octal codes and mnemonics for the instructions are listed in Paragraph 12.3.2. A complete list of device codes and the jumpers required to select each device code is shown in Table 12-2.

12.4.1.2 Printer Receive Logic – The Printer Receive logic is shown in Figure 12-11. Significant signals are related by the timing diagram in Figure 12-12. Refer to both figures when reading the logic description.

The printer routine is initiated by DEMAND changing to the true state, indicating that the printer is ready for another character. This sets the PRNT flag flip-flop. This flip-flop can also be set by the PNSF instruction at TP3 time. If the VT8-E is logically connected to the interrupt system, as this discussion assumes, the PRNT FLG (1) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The PNSI instruction in the routine causes the program to jump to a VT8-E routine that determines whether the printer or keyboard requested the interrupt (other options are open to the programmer, this is but one example). Ultimately, the VT8-E printer routine executes the PNPC instruction.

During TS2 of the PNPC instruction, information is gated from the AC Register to the DATA lines and remains on the DATA lines through TS3. When PNPC L is decoded in the IOT Decoder logic, it enables NOR gates E25C and E25D (Figure 12-11). NOR gate E25-D asserts the DATA EN signal; both DATA EN A L and DATA EN B L are derived from this signal. The difference between the DATA EN A L and DATA EN B L signals is significant only when considering the Display logic; for the present one must know only that one of these two signals gates lines DATA 9 and DATA 10 to the 7-bit register. The remaining DATA lines are gated to the register flip-flops as shown.



NOTE:
Logic is P/O MB335 module, unless noted otherwise.

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Figure 12-10 IOT Decoder Logic

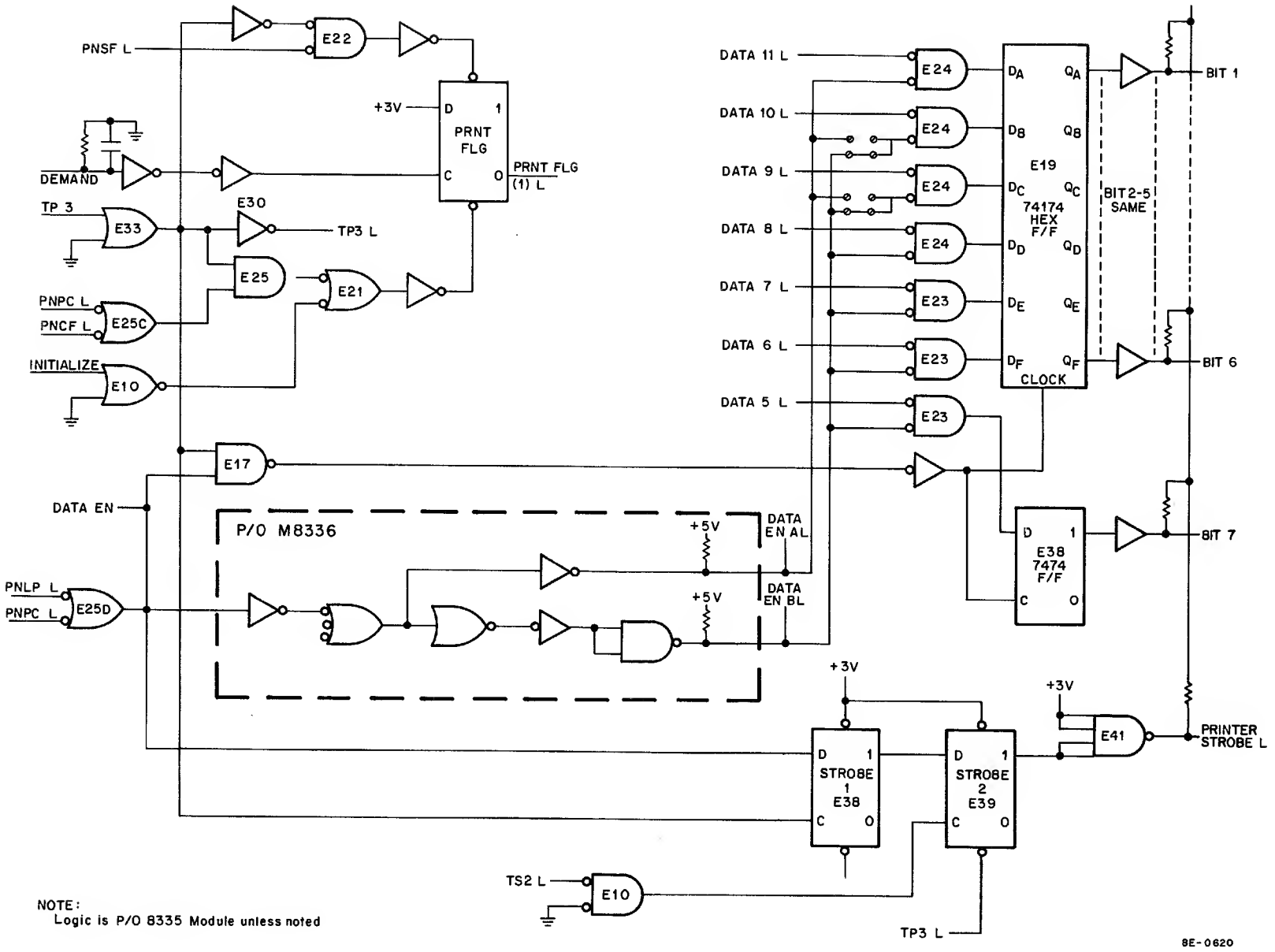
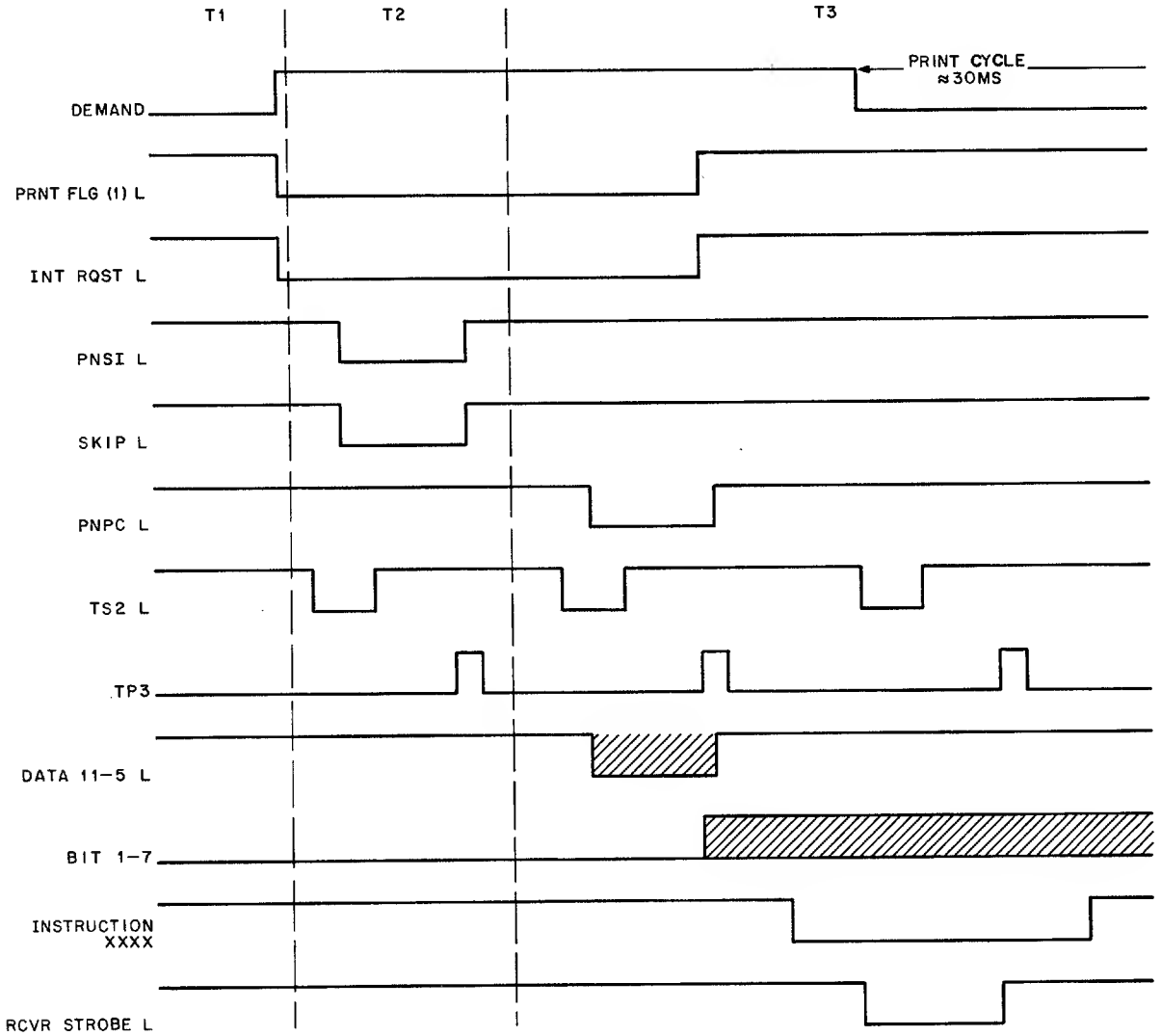


Figure 12-11 Printer Receive Logic

At TP3 time of the instruction, NAND gate E-17 is enabled and the information on the DATA lines is clocked into the 7-bit register. Simultaneously, flip-flop STROBE 1 sets and the PRNT FLG flip-flop is cleared. The register data is applied, via the BIT 1–7 lines, to the Printer Buffer Register. At the beginning of TS2 of the instruction following PNPC, flip-flop STROBE 2 sets and asserts PRINTER STROBE L. This signal loads the Printer Buffer Register and negates the DEMAND signal. Both STROBE 1 and STROBE 2 are cleared by the next TP3. When the print cycle ends approximately 30 ms later, the DEMAND signal is again asserted and a new transfer can be started.



NOTE:
T1, T2 and T3 are distinct time periods.
The amount of time between periods is
a function of program-routine execution time.

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Figure 12-12 Printer Receive Logic Timing

12.4.1.3 Keyboard Transmit Logic – The Keyboard Transmit logic is shown in Figure 12-13. Significant signals are related by the timing diagram in Figure 12-14. Refer to both figures when reading the logic description.

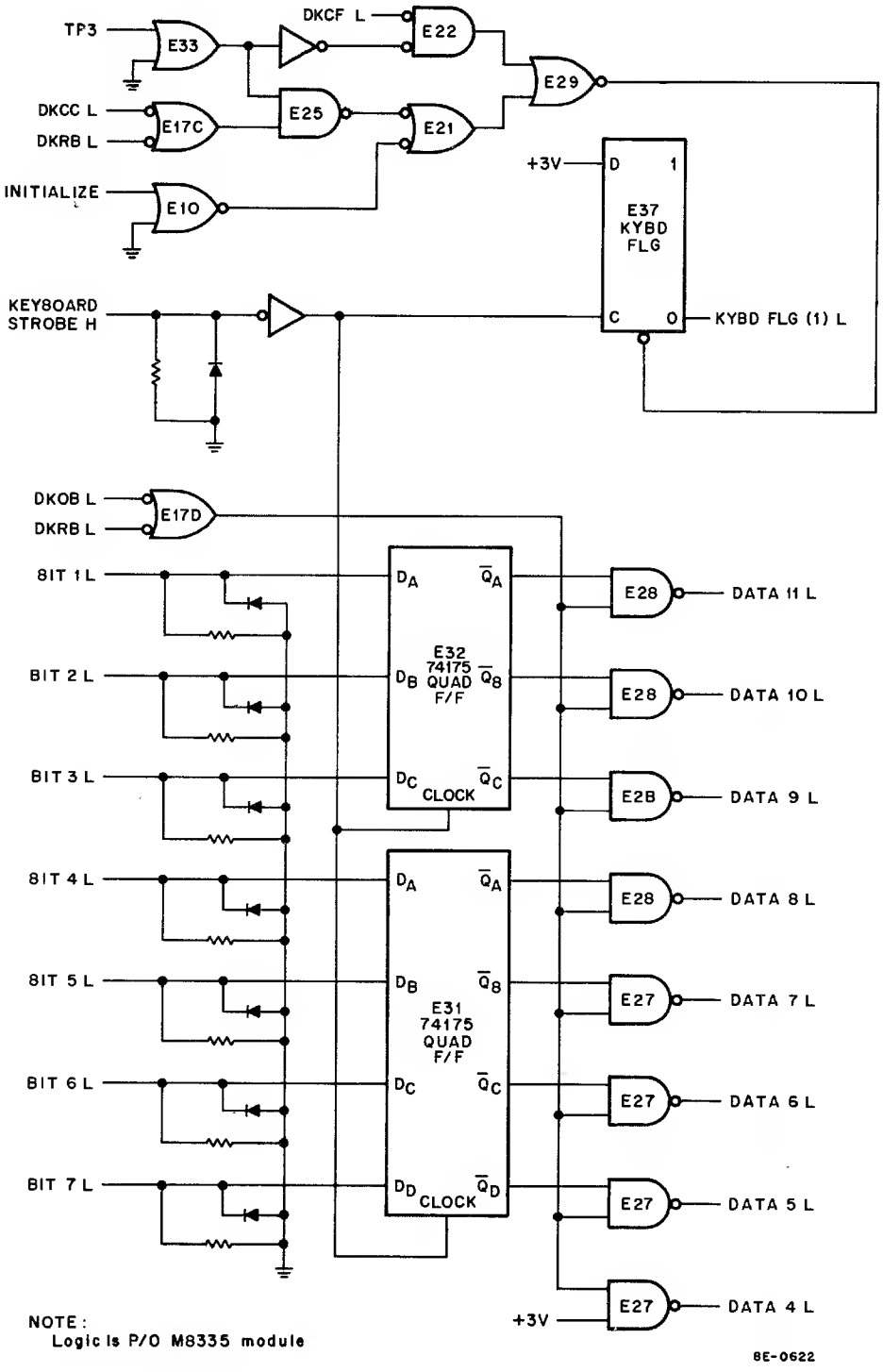


Figure 12-13 Keyboard Transmit Logic

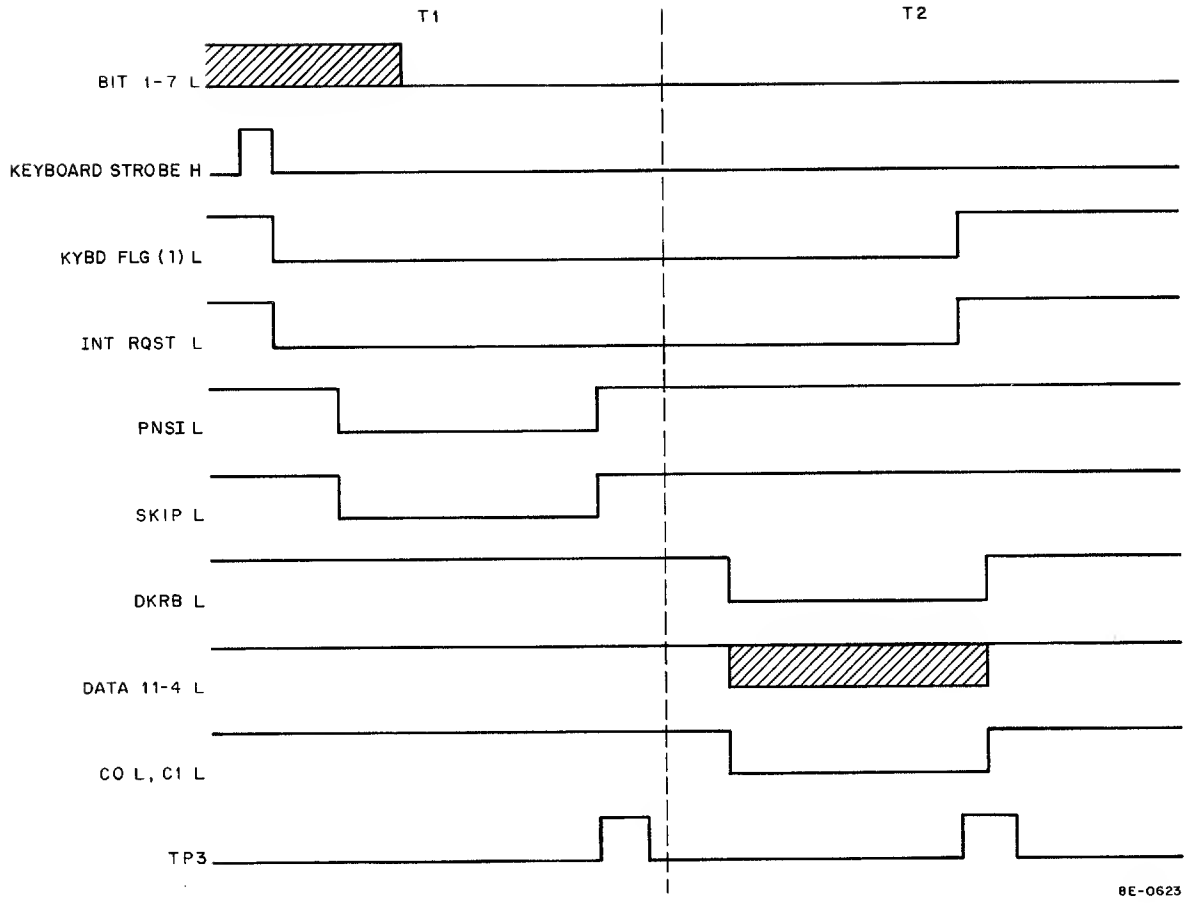


Figure 12-14 Keyboard Transmit Logic Timing

The user initiates the keyboard sequence by pressing a key on the keyboard. The character information is placed on the BIT 1–7 lines. After a period of time that allows the BIT lines to settle, the keyboard generates the KEYBOARD STROBE H signal. The trailing edge of this signal clocks the information into the 7-bit register and sets the KYBD FLG flip-flop. If the VT8-E is logically connected to the interrupt system, as assumed, the KYBD FLG (1) L signal causes the INT/SKIP logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The PNSI instruction in the routine causes the program to jump to a VT8-E routine that determines if the printer or keyboard requested the interrupt. Ultimately, the VT8-E keyboard routine executes the DKRB instruction.

When the DKRB instruction is decoded, the IOT Decoder logic generates the DKRB L signal and activates the OMNIBUS C0 and C1 lines. The DKRB L signal enables NOR gates E17C and E17D; the output signal from E17D gates the information from the register outputs to DATA lines 5–11, and also causes NAND gate E27 to assert the DATA 4 L signal. The DATA lines are gated to the AC Register and the information is clocked into the register at TP3 time. Also at TP3, the KYBD FLG flip-flop is cleared, readying the logic for a new data transfer.

12.4.1.4 INT/SKIP Logic – The INT/SKIP logic is shown in Figure 12-15. The PRNT FLG (1) L signal and the KYBD FLG (1) L signal can cause program skips when tested by instructions PNSK and DKSK, respectively. The signals can also be tested by the PNSI instruction, provided the ENA flip-flop, E37, has been set, logically connecting the VT8-E to the interrupt system. When E37 is set, the PNSI L signal enables NAND gate E29, which, in turn, enables NAND gate E34, if either the PRNT FLG (1) L signal or the KYBD FLG (1) L signal is asserted. Simultaneously, NAND gate E13 asserts the INT RQST L signal.

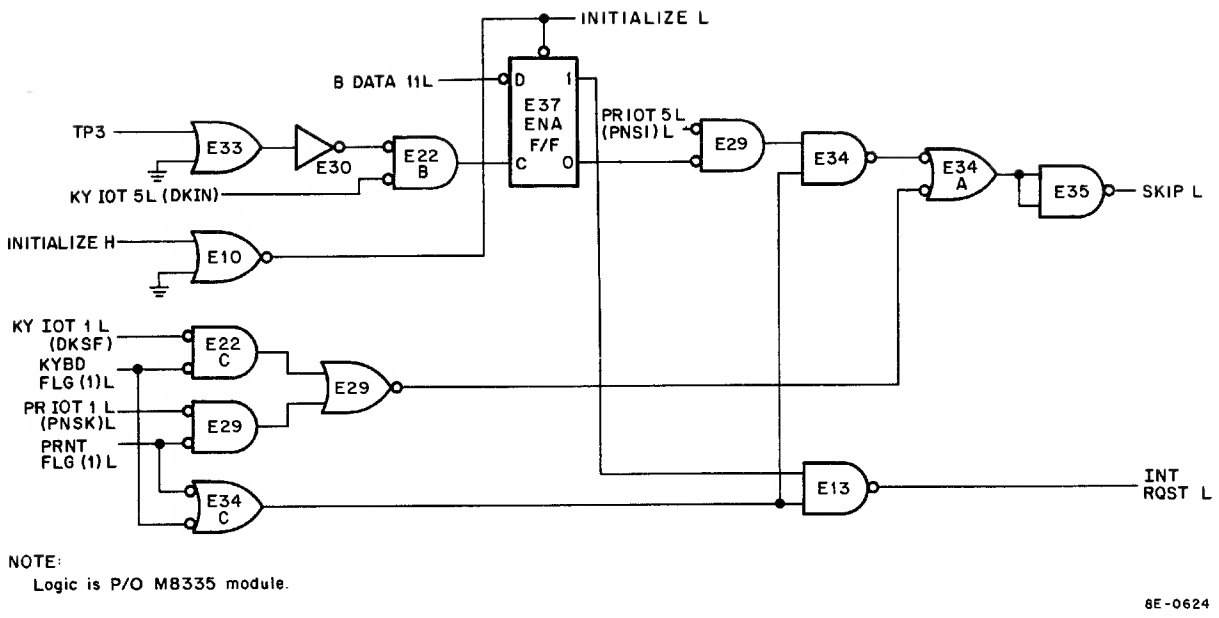


Figure 12-15 Keyboard/Print Interrupt and Skip Logic

The ENA flip-flop is set by the OMNIBUS INIT signal for the PDP-8 family computers. To clear the flip-flop, remove the VT8-E from the interrupt system, load AC11 with logic 0 and then program the DKIN instruction. The logic 0 in AC11 keeps the DATA 11 L signal negated. Thus, the D input of E37 remains high. At TP3 time, NAND gate E22B provides a clock pulse for E37, clearing the flip-flop. E37 can be set at any time with the same instruction merely by loading AC11 with logic 1.

12.4.2 Display Logic

Information displayed by the VT8-E is transferred by data breaks from the PDP-8/E memory. As with all data break devices, the start of the data transfer is under program control. However, the VT8-E is a 1-cycle data break device; consequently, it needs only a starting memory address to carry out the complete data transfer. The starting address, i.e., the memory address of the first data word to be transferred to the VT8-E, is placed in the AC Register by a program TAD instruction. Program IOT instructions gate this address onto the OMNIBUS DATA lines and cause it to be loaded into a starting address register in the VT8-E (Figure 12-16). At the same time, the VT8-E Data Break logic is readied for triggering.

When the CRT sweep is in a specified position, a synchronizing signal is generated by the VT8-E Timing logic. This signal enables the Data Break logic to request a data break and check priority. If no higher priority device has requested a break at this time, the Data Break logic asserts a number of OMNIBUS control signals, enabling direct communication between the interface and memory for one PDP-8/E timing cycle. At the same time, other Data Break logic signals gate the starting address onto the OMNIBUS MA lines. During the data break timing cycle, the data word in the addressed memory location is transferred on the MD lines and loaded into the interface Line Buffer Register. At TP4 time of the timing cycle, the Data Break logic increments the address in the Address Counter. The data word in this new address is transferred during the next data break timing cycle, which might occur immediately after the first (priority is checked during TS4 of each data break cycle; a higher priority device can interrupt the VT8-E data breaks).

After each transfer, the address in the Address Counter is incremented, and the data word in the new address is loaded into the Line Buffer Register. This register holds 32 or 64 data words, depending on the mode (graphic or alphanumeric) or the desired number of alphanumeric characters per line. The Data Break logic counts the number of data breaks; when the specified number of data words has been loaded into the Line Buffer Register, the Data Break logic ceases to request breaks.

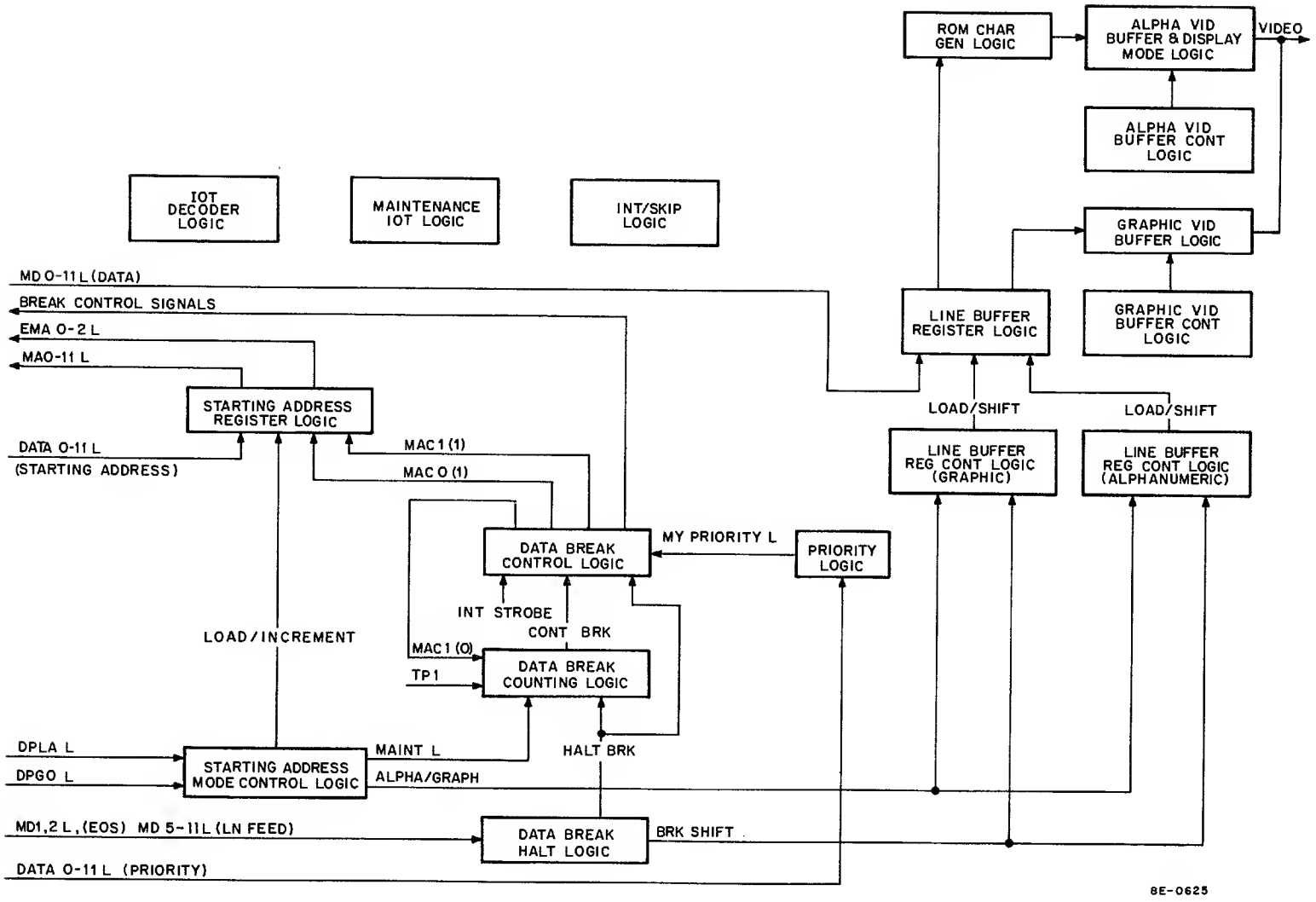


Figure 12-16 Display Logic Block Diagram

If the VT8-E logic has been programmed to display 32 alphanumeric characters per line; for example, each data word in the Line Buffer Register contains: the 7-bit ASCII code representation of an alphanumeric character (bits 5–11); data that controls how the character is displayed (bits 3 and 4); and data that controls the visible field (bits 1 and 2). Because the VT8-E displays only a 64-character set, bits 6–11 of the Line Buffer Register contain sufficient data to display all alphanumeric characters. Characters are formed on the CRT screen when the CRT video circuits selectively intensify points within a 5 X 7 dot matrix. The letter F is illustrated in Figure 12-17. Each horizontal scan line corresponds to one row of the letter. As the sweep scans along a line, video signals selectively intensify points as illustrated (5 video signals in row 1 of the letter F). If 32 alphanumeric characters per line are to be displayed, for example, row 1 of each character is swept out by the same scan line. The next scan line sweeps out row 2 of all 32 characters, and so on until the 7th scan line sweeps out row 7 of the characters, completing the character line.

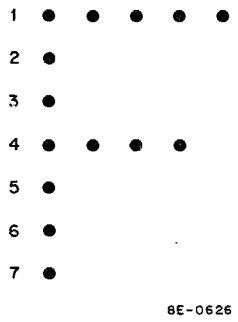


Figure 12-17 Video Presentation for the Letter F

The video signals are generated, indirectly, by a ROM Character Generator. After the start of a horizontal scan line, a 6-bit ASCII character is shifted from the Line Buffer Register (at this time, the register is in the recirculating mode; hence, an end-around shift is performed). The character addresses a ROM Character Generator location. This location contains the video information for one row of the character. For example, assume that the letter F is the first character to be displayed in a particular character line. The 6-bit ASCII representation of the letter F addresses a particular ROM Character Generator location. The information in this location causes row 1 of the letter to be painted during this scan line. The next character to be displayed is shifted from the Line Buffer Register and addresses its unique ROM Character Generator location; the information in the location causes row 1 of this character to be displayed just after character F. Row 1 of all 32 characters is displayed during this scan line.

After the start of the next horizontal scan line, the 6-bit ASCII representation of the letter F is again shifted from the Line Buffer Register. Meanwhile, certain ROM control signals have been asserted so that the addressed location differs from that of the first scan line. This location contains information that causes Row 2 of the letter F to be painted during this scan line. Row 2 of all other characters is displayed during this scan line in similar fashion. Consequently, the Line Buffer Register is shifted 32 times during each scan line; after 7 end-around shifts of the register, a character line has been displayed.

Each character line comprises ten scan lines, rather than the seven just described. The three additional lines occur at the beginning of the character line. During the first two scan lines, the Line Buffer Register is loaded from the OMNIBUS MD lines; during the third scan line, a blank ROM location is addressed. Figure 12-18 represents two character lines as they would appear on the CRT screen. Character line spacing (43% of character height) is provided by the three blank scan lines.

If the VT8-E has been programmed for a graphic display, one line of graphic data is displayed during each horizontal scan line. A line of graphic data is represented by 16 12-bit data words; each bit of a data word represents a dot or a

space on the CRT screen. The Line Buffer Register is loaded with two lines of graphic data by 32 data breaks. As the sweep scans along a line, video signals selectively intensify points to paint the graphic symbol. Although 16 12-bit data words contain 192 bits, only 189 points can be painted by each scan.

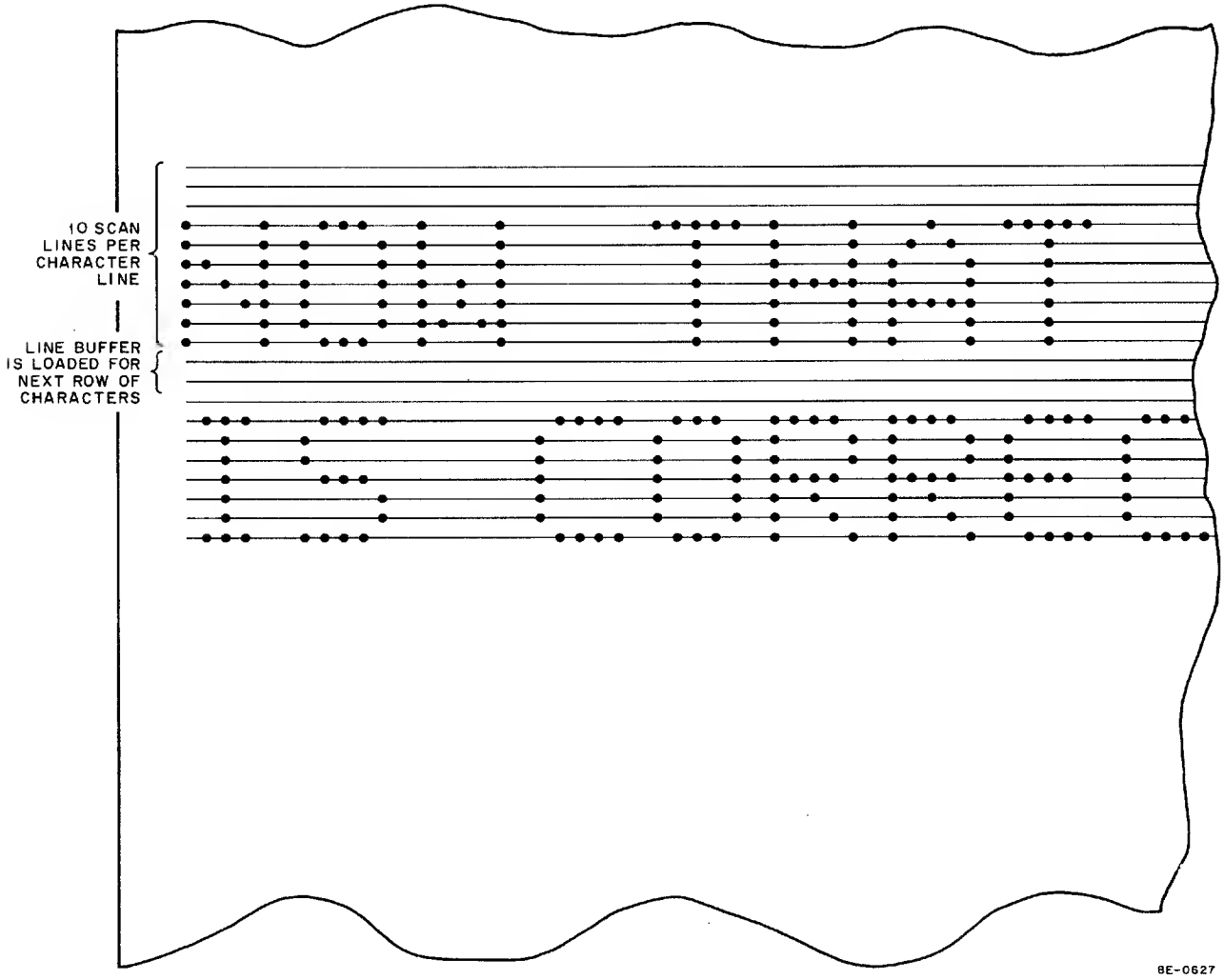


Figure 12-18 Two Alphanumeric Characters Displayed on the CRT

12.4.2.1 VT8-E Timing – The VT8-E Timing logic generates signals that sync the Display logic and the CRT sweep circuits. Figure 12-19 illustrates the CRT vertical and horizontal sweep signals and the VT8-E sync signals.

For 60 Hz operation, the VT8-E timing generates a V SYNC L signal every 16.7 ms. This sync signal causes a vertical retrace, which is carried out in approximately 20 scan lines. A VZONE flip-flop in the timing controls the displayable area in the vertical direction. When the flip-flop is set, the VZONE (1) signal enables a vertical display of 200 scan lines (the horizontal sweep rate is set at 15.6 kHz; a total of 60 scan lines is made non-displayable to remove distortion-prone areas on the CRT screen).

The timing generates an HSYNC signal every 64.1 μs. A HZONE flip-flop in the timing controls the displayable area in the horizontal direction. When the flip-flop is set, the HZONE (1) signal enables graphic or alphanumeric video to be painted in the distortion-free area of the screen (exceptions to this statement are pointed out in the detailed logic discussion).

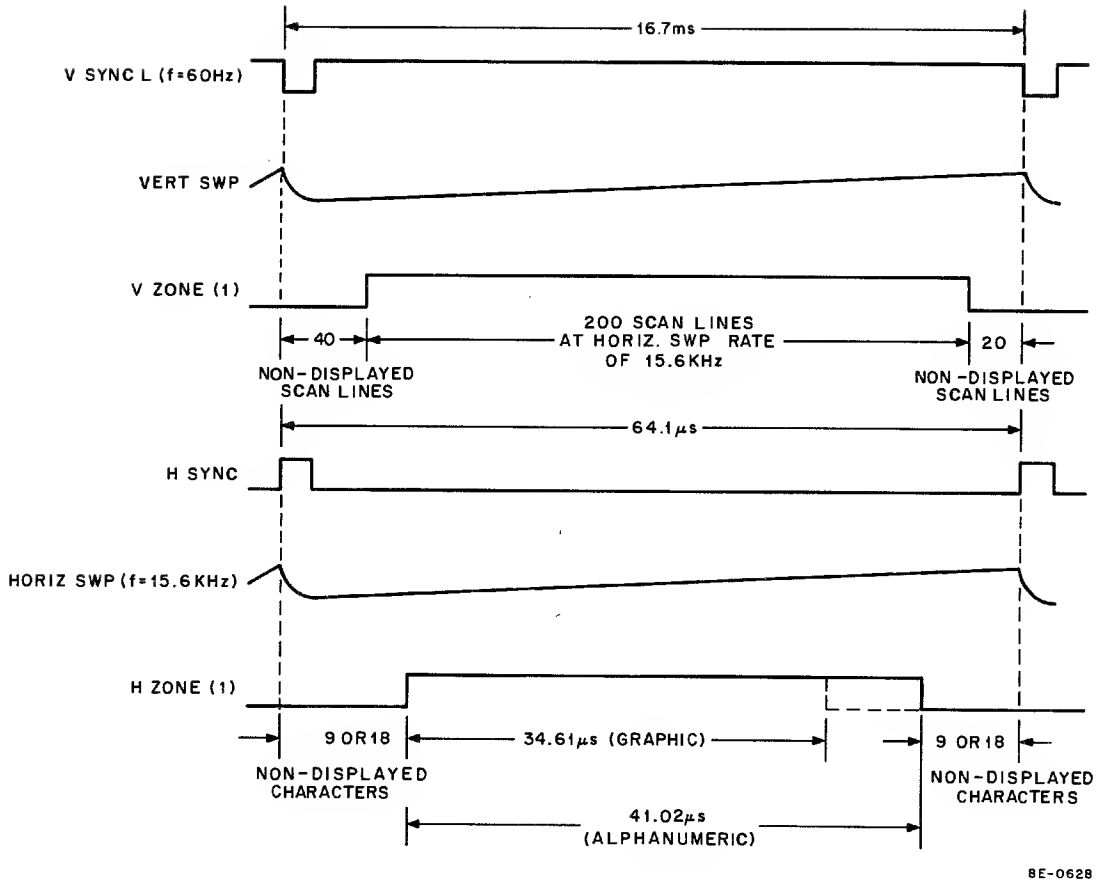
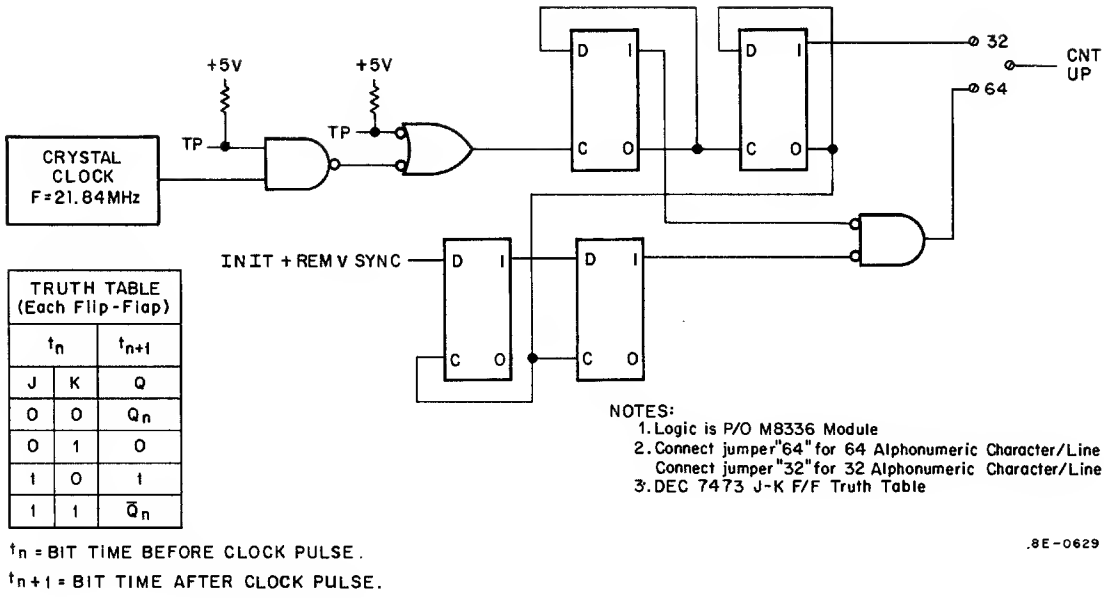


Figure 12-19 Sweep and Sync Signals

The VT8-E timing is such that either 50 or 100 alphanumeric characters could be displayed between HSYNC signals. The HZONE (1) signal reduces the number of characters to either 32 or 64, respectively (an equal number of characters is removed on both sides of the screen). Note that the HZONE (1) signal is of shorter duration for the graphic display. This is explained as follows. Clock pulses of the same basic frequency are used to shift the Alphanumeric Video Buffer Register and the Graphic Video Buffer Register. Seven shift signals are needed to display the rows of the 5 X 7 alphanumeric character matrix (five signals intensify the scan, two signals provide spacing between each character). Thus, 7 X 32, or 224 shift pulses are needed for an entire character line. An entire graphic line needs only 192 shift pulses. Consequently, it seems that the HZONE (1) signal should be reduced by an amount that allows 192 shift pulses to be generated (if the display area is not shortened, an improper display will result). This would mean reducing the graphic displayable area by an amount equal to 32 shift pulses. However, this is not a multiple of seven, which it must be to enable correct alphanumeric display. The closest number that is a multiple of 7 is 35. Thus, the horizontal zone for graphics allows only 189 shift pulses to be produced, cutting off the last 3 data bits in each scan line (note that 28 could not be used because then too many graphic shift pulses would be produced). The pulses are derived from a 5.46 MHz clock (t = 183.15 ns). Therefore, 189 shift pulses require an HZONE (1) signal of only 34.61 μs.

12.4.2.2 VT8-E Timing Logic – The VT8-E Timing logic generates the CRT sync pulses and the interface control signals. All timing and control signals are derived from a crystal-controlled transistor oscillator that produces pulses at a frequency of 21.84 MHz. These pulses are applied to a Clock Pulse Generator, shown in Figure 12-20. The generator divides the basic frequency by 2 and 4, producing well-shaped clock pulses of 10.92 MHz and 5.46 MHz. Two test points are available which allow the oscillator clock to be inhibited and external clocks injected to drive the timing chain.



TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

t_n = BIT TIME BEFORE CLOCK PULSE.

t_{n+1} = BIT TIME AFTER CLOCK PULSE.

Figure 12-20 Clock Pulse Generator

The clock pulses selected are applied to a chain of DEC 74161 4-Bit Counters that counts down the pulse frequency to 3.75 Hz (for 60 Hz operation). Selected outputs of the timing chain are gated to produce sync pulses and control signals.

A logic block representation of the DEC 74161 4-Bit Counter Integrated Circuit (IC) is shown in Figure 12-21. This IC, E17, is the first one in the timing chain. Because it is a 4-bit counter, E17 can produce one pulse at its CARRY output for each 16 pulses at its COUNT UP input. However, because the IC can be preset to any count, it can produce a CARRY output for any number of input pulses less than 16. The preset inputs are labeled A through D in Figure 12-21 (A is the LSB). They are wired so that E17 is preset with a count of 1001_2 whenever a signal is applied to the LOAD input and a clock pulse occurs. The CARRY signal is generated when the count is in the 1111_2 state and ENP and ENT are true. A Load signal is generated by the OR gate and E17 is preset to 1001_2. Seven more pulses at the clock input produce another CARRY signal and, again, the counter is preset. Thus, the counter divides by seven. The counter can also be preset by a REMOTE V SYNC IN L signal, enabling the timing to be controlled by some external device. The output of each bit, designated QA through QD (QA is the LSB), is available for gating to generate the sync and control signals.

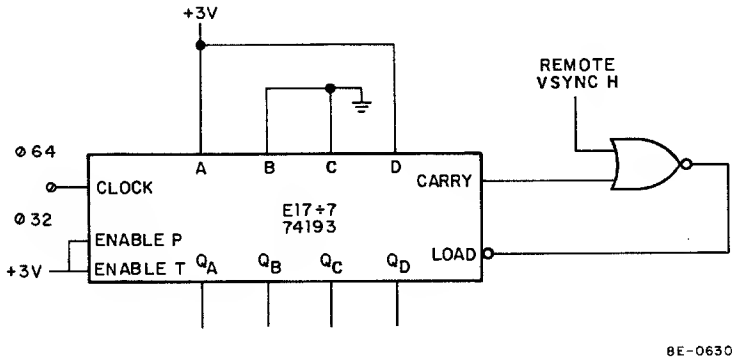
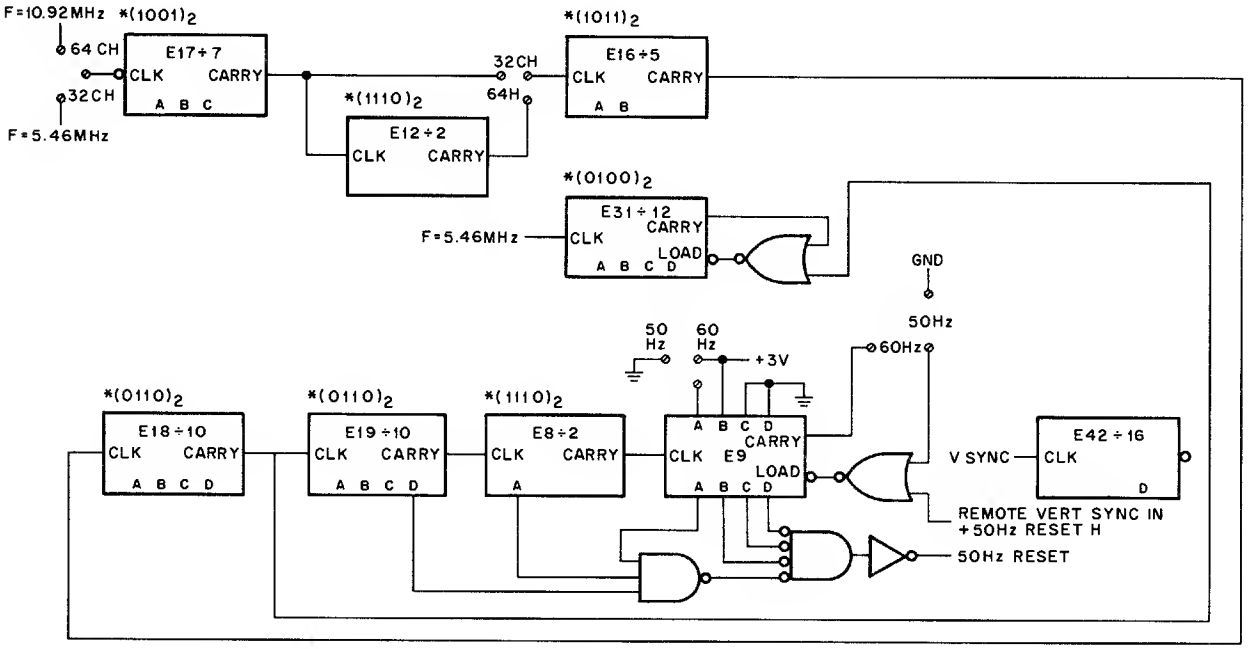


Figure 12-21 4-Bit Counter

Figure 12-22 shows the entire chain of 74161 ICs. Each IC in the figure is represented in shorthand form: i.e., the wiring of the PRESET inputs is not shown, the LOAD input circuits are not shown, and the destination of each output is now shown (only those output bits that are used are indicated on the ICs). The binary designations above each IC block represent the way the preset inputs are wired. For example, E16 is wired thus: PRESET input D is tied to +3V; PRESET input C is grounded; PRESET inputs B and A are tied to +3V. Therefore, E16 is preset with a count of 1011_2 and divides by 5.



*COUNTER IS PRESET TO THIS BINARY VALUE

NOTE:
Logic is P/O M8336 Module

IC OUTPUT FREQUENCY

IC	FREQ. OUTPUT	
	60Hz LINE	50Hz LINE
E17	780KHz(32) 1560KHz(64)	SAME AS 60Hz
E16	156KHz	
E18	15.6KHz	
E19	1.56KHz	
E8	78OHz	
E9	60Hz	50Hz
E42	3.75Hz	3.125Hz

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Figure 12-22 VT8-E Timing Chain

Each IC has a NOR gate at its LOAD input, exactly as shown in Figure 12-21; this gate ORs the CARRY output with REMOTE V SYNC and INIT (E17, E12, E16), or with REMOTE V SYNC and 50 Hz RESET (E18, E19, E8, E9). The bit output destinations are shown, in part, only for ICs E19, E8, and E9.

The table in Figure 12-22 indicates the frequency of the CARRY output pulses of each IC. The output frequency from E17 differs for 32 character/line and 64 character/line operation. The bit output signals from E17 determine the alphanumeric character rate, the rate at which characters are painted on the CRT screen. Thus, the rate is twice as fast for 64 character/line operation. E12 divides by two; therefore, the input of E16 is the same for both character rates.

When a 50 Hz line is used, the timing is modified in the last three ICs. For 60 Hz operation, E9 is preset with a count of 0011_2 and its CARRY output provides the LOAD input for E9. E8 and E9, together, divide the output of E19 by 26, producing a CARRY output pulse from E9 at a frequency of 60 Hz. This output is gated elsewhere in the logic to generate the V SYNC L signal that causes a CRT vertical retrace. For 50 Hz operation, the 50 Hz jumpers are connected, and E9 is preset with a count of 0010_2. Furthermore, the LOAD input of E9 is controlled by REMOTE V SYNC IN or 50 Hz RESET H. When E9 attains a count of 001_2 and both E19-D and E8-A are high, E9 is preset and a V SYNC pulse is generated. E8 and E9, together, divide the output of E19 by 31.2, producing pulses having a frequency of 50 Hz. The table shows the output of E9 as 50 Hz (the output is not actually from E9, as for 60 Hz operation, but it is convenient to think of it as so). As for 60 Hz operation, the output is gated to generate the V SYNC L signal.

Note that the REMOTE V SYNC IN or 50 Hz RESET line is activated when E9 is preset; thus, ICs E18, E19, E8, and E9 are preset at the moment of vertical retrace. This active step is not necessary during 60 Hz operation because all ICs automatically overflow to the preset state.

Figure 12-23 shows the logic that generates the horizontal and vertical sync signals, while Figure 12-24 shows the HZONE and VZONE flip-flops and those signals that control the two flip-flops. The timing diagram in Figure 12-25 shows the line timing for both alphanumeric and graphic display. Two hundred of the HZONE (1) signals are generated for each VZONE signal, as shown in Figure 12-19.

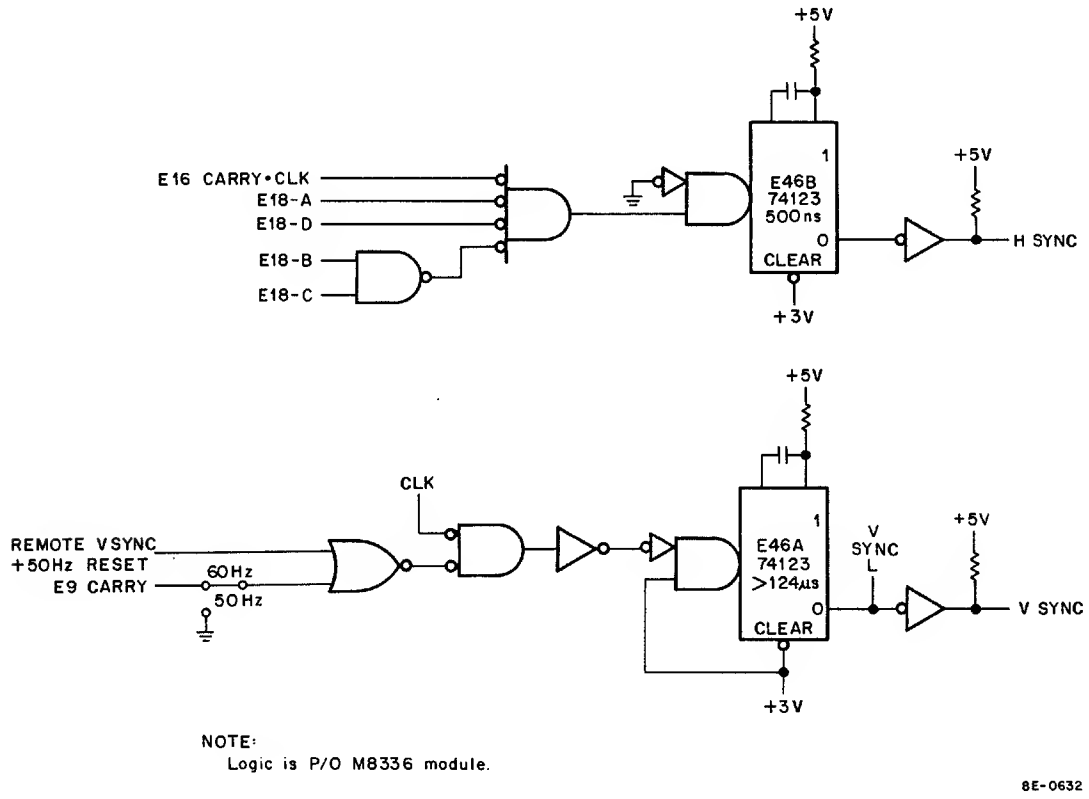


Figure 12-23 Horizontal and Vertical Sync Circuits

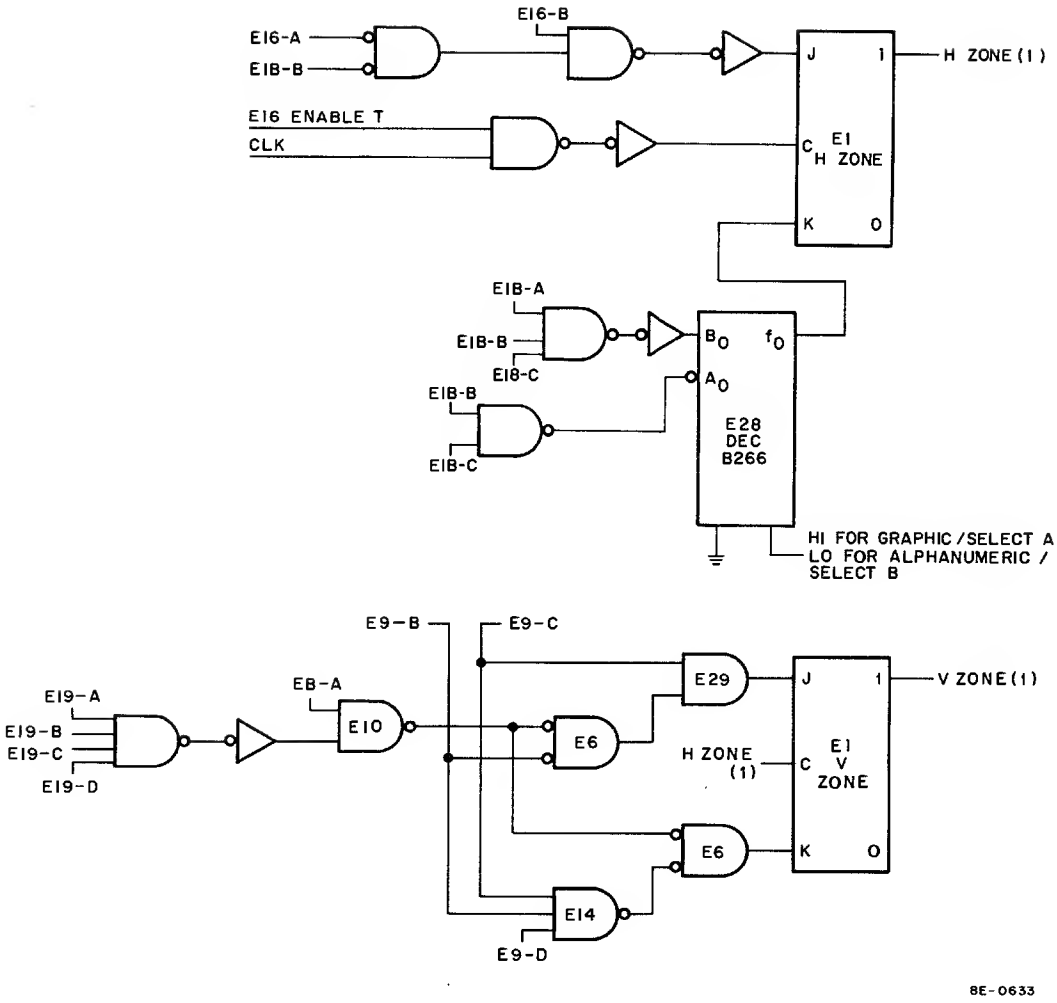


Figure 12-24 Horizontal and Vertical Zone Flip-Flops

12.4.2.3 Starting Address Register Logic – The Starting Address Register logic is shown in Figure 12-26. The logic includes two Starting Address Registers: one is a 12-bit register comprised of two DEC 74174 ICs (hex flip-flop); the other uses three bits of a DEC 74175 IC (quad flip-flop). The Address Counter is comprised of four DEC 74193 ICs (4-bit up-counters) connected in series and is preset from the Buffer Registers.

The control signals that load and clock the Starting Address Registers and the Address Counter are generated by the Starting Address Control logic, shown in Figure 12-27. When the program IOT instruction DPLA is issued, the 12-bit starting address is placed on the DATA lines. The DPLA L signal causes both the DATA EN A L and DATA EN B L signals to be asserted. The starting address is gated through the NAND gates to the DEC 74174 inputs and loaded into the buffer at TP3 time by the LD ST ADD signal.

The extended field must also be identified by the EMA bits. The extended field address bits are placed on lines DATA 6, 7, and 8 by the DPGO IOT instruction. The DPGO L signal causes the DATA EN signals to be asserted, gating the extended address to the DEC 74175 inputs. At TP3 time the XST ADD REG is loaded by the LD XST ADD signal (DPGO).

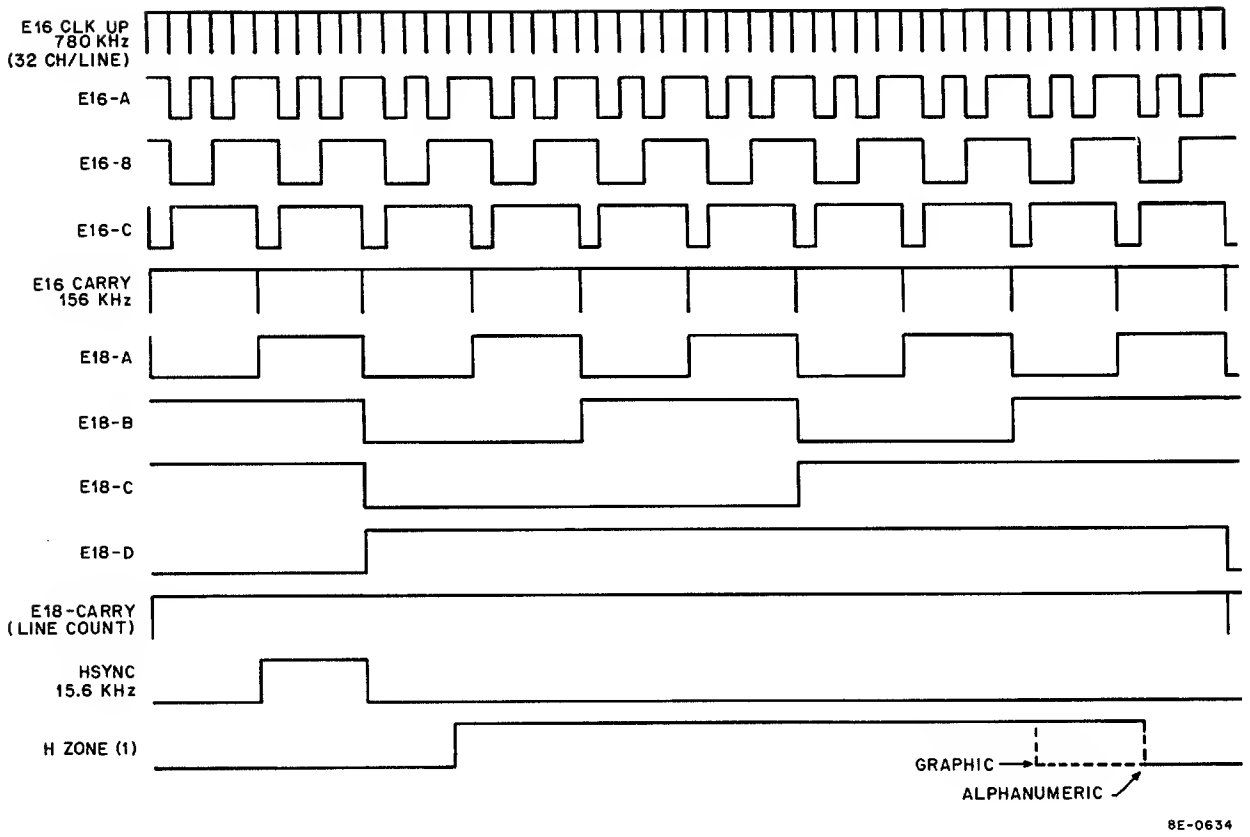
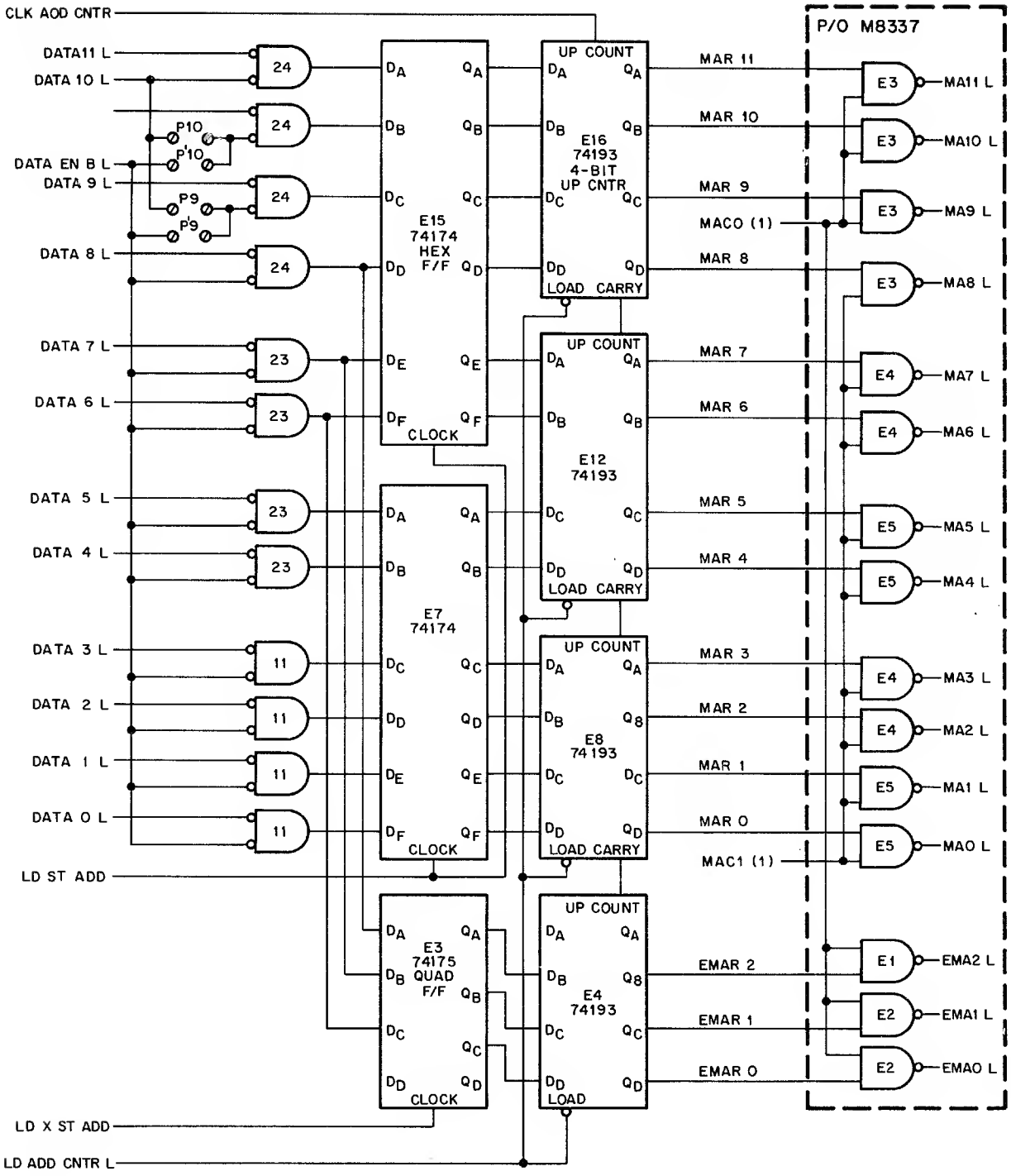


Figure 12-25 Alphanumeric and Graphic Line Timing

The DPGO L signal also clears the MAINT/GO flip-flop (Figure 12-27) at TP3 time, negating the MAINT L signal. This negated signal enables a vertical sweep synchronizing signal, E46(Q), to assert the LD ADD CNTR L signal. This signal loads the starting address (including the extended address) into the 15-bit Address Counter.

At approximately the same time that the Address Counter is loaded, the Data Break Counting logic is readied for triggering. When the sweep is in the specified position, the COUNTING signal is generated, enabling the Data Break Control logic to request a data break. If the VT8-E has highest priority, the MAC0 and MAC1 flip-flops in the Data Break Control logic are set. The MAC0(1) and MAC1(1) signals gate the 15-bit starting address from the Starting Address Register outputs onto the MA0–11 and EMA0–2 lines. At TP1 of the data break timing cycle, the MAC2 flip-flop in the Data Break Control logic is set. The MAC1(1) signal then enables the Starting Address Control logic to assert the CLK ADD CNTR signal at TP4 time of the data break timing cycle. Thus, the address in the Starting Address Register is counted up by one. The next data break timing cycle transfers the data word in the new address to the VT8-E.

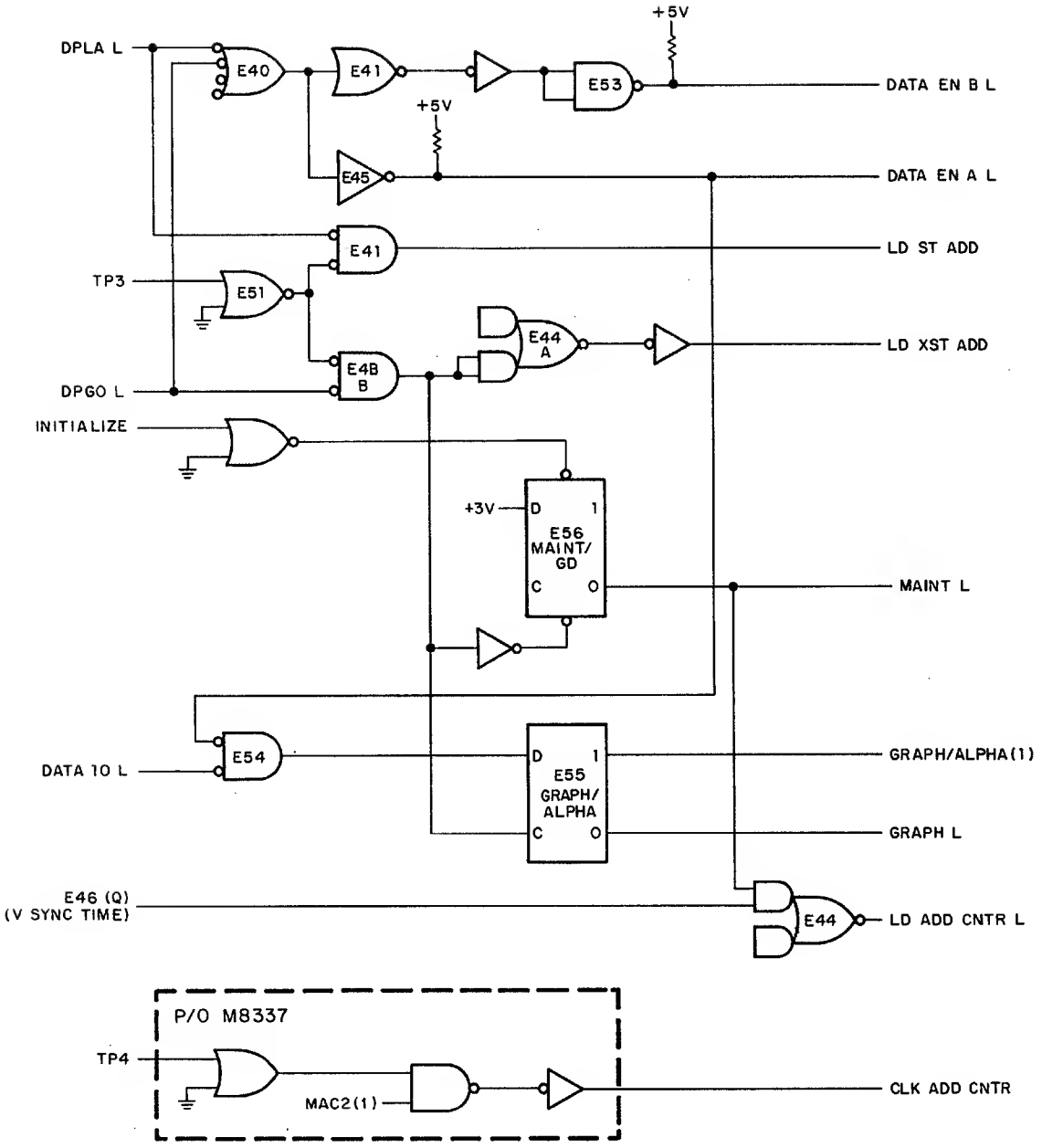
12.4.2.4 Data Break Counting Logic – The Data Break Counting logic is shown in Figure 12-28. This logic generates the COUNTING signal that enables the Data Break Control logic to request data breaks. When the PRESET BRK signal is generated, flip-flop E43A is set, asserting the COUNTING signal. The COUNTING signal enables the NBR flip-flop in the Data Break Control logic to be set at INT STROBE time. If the VT8-E has highest priority, data breaks begin. Each TP1 signal of a data break timing cycle causes NAND gate E42 (Figure 12-28) to assert the COUNT BRK signal. This signal is counted by the 4-bit up-counter, E53. When the correct number of data breaks has been performed, flip-flop E43A is cleared via NOR gate E33 and data breaks cease.



NOTE:
Logic is P/O MB335 unless noted.

8E-0635

Figure 12-26 Starting Address Register Logic



NOTE
Logic is P/D MB336 module unless noted.

8E-0636

Figure 12-27 Starting Address Register Control Logic

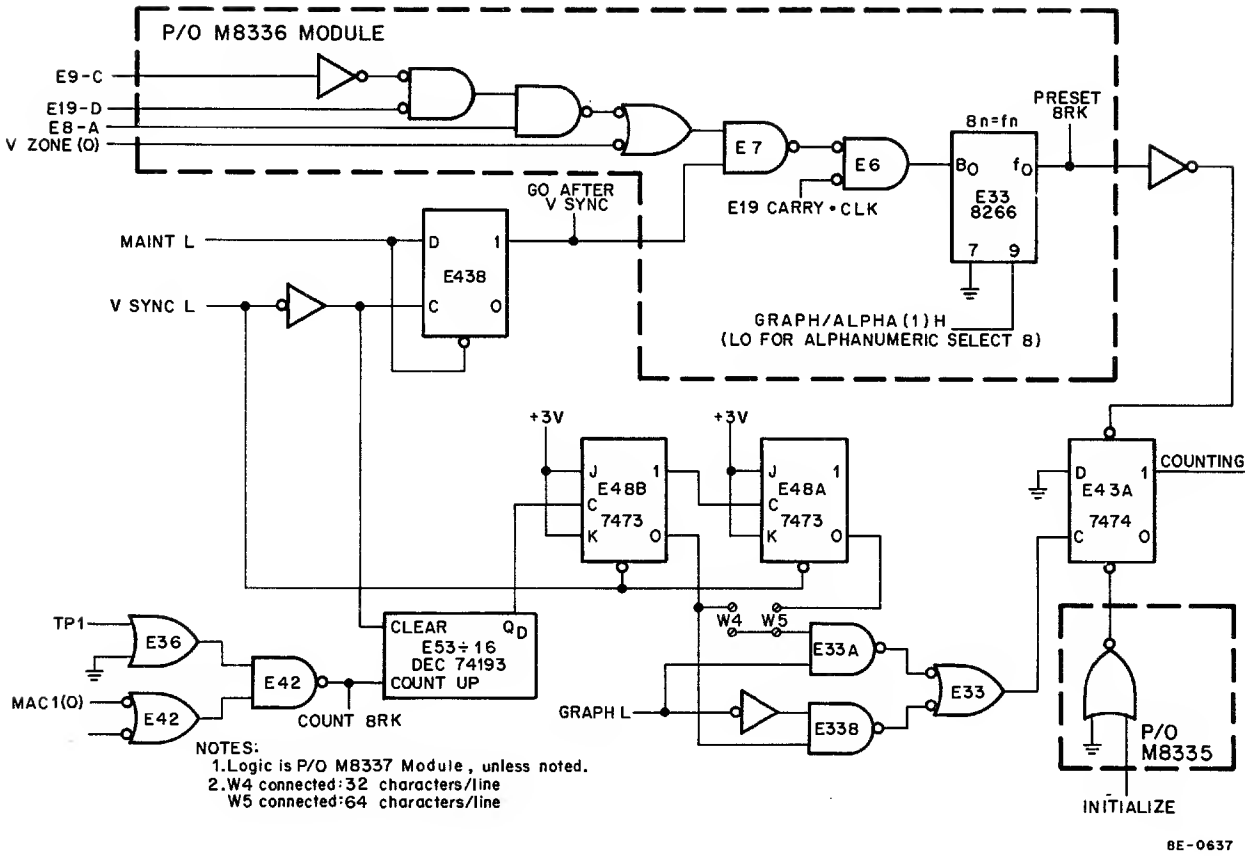


Figure 12-28 Data Break Control Logic

If the logic has been programmed for an alphanumeric display (assume 32 characters/line), 32 data words must be loaded into the Line Buffer Register during two scan lines of the character row. During each of the eight remaining scan lines, the Line Buffer Register is recirculated. Thus, new information is loaded once every ten scan lines and the PRESET BRK signal must be generated only once every ten scan lines.

Note that the logic within the dashed line in Figure 12-28 generates the PRESET BRK signal. The VSYNC L signal prepares this logic for triggering by setting flip-flop E43B, thereby asserting the GO AFTER VSYNC signal (the MAINT L signal is negated by the Starting Address Control logic when a DPGO instruction is issued). VSYNC L also clears the 4-bit up-counter and the two J-K flip-flops. When the VZONE flip-flop is set, NAND gate E7 is enabled. Each E19 CARRY signal that occurs causes PRESET BRK to be generated. Because E19 CARRY occurs once every ten scan lines, the Line Buffer Register is loaded once every ten scan lines, as required.

Figure 12-29 illustrates the timing of the counting network for an alphanumeric display of 32 characters/line. This timing applies to a graphic display, as well, although the GRAPH L signal would be asserted for such a display. If the logic has been programmed for a graphic display, the PRESET BRK signal must be generated differently. Sixteen data words are needed to display one line of graphic data. Thus, the Line Buffer Register can hold two lines of graphic data. Since a line of graphic data is displayed by one scan line, a PRESET BRK signal is required once every two scan lines. The logic in Figure 12-30 is used to generate the Graphic mode PRESET BRK signal. It is similar to the PRESET BRK logic in Figure 12-28. The VSYNC L signal is used in the same way and the data breaks are counted by the counting logic in the same way. The LN CNT signal occurs at the end of each scan line, but the E19-A signal is high for every other scan line. Consequently, the graphic PRESET BRK occurs once every two scan lines.

Figure 12-29 Data Break Counting for 32 Characters/Line

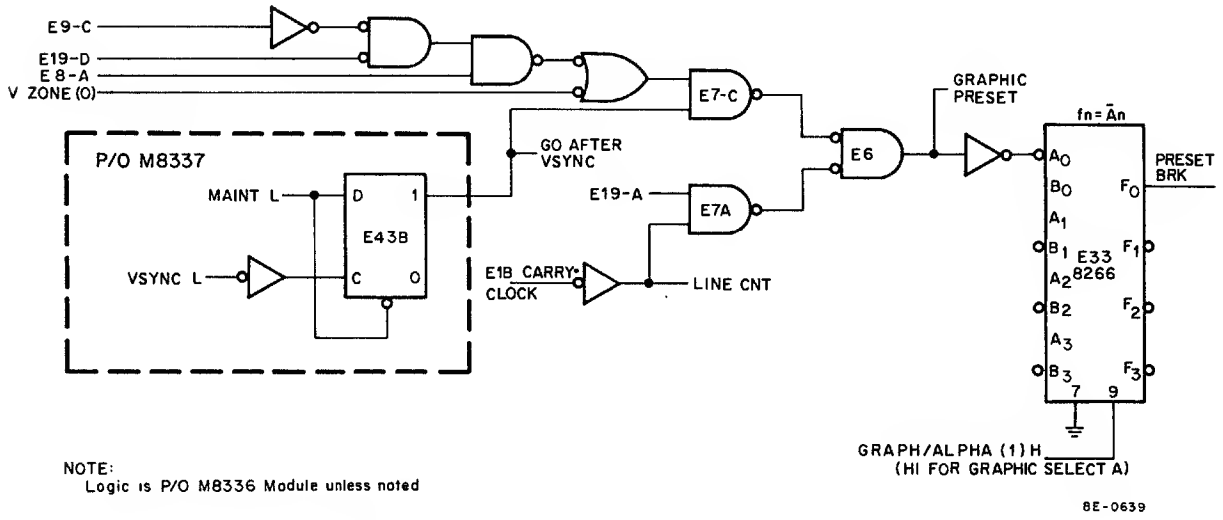


Figure 12-30 PRESET BRK Generation Graphic Mode

12.4.2.5 Data Break Control Logic – The Data Break Control logic is shown in Figure 12-31. When the COUNTING signal is asserted by the Data Break Counting logic, NAND gate E52 is enabled. (MAINT L is negated by the DPGO instruction and HALT BRK L is asserted only for line-feed or end-of-screen.) The NBR flip-flop is set at INT STROBE time, asserting the NBR (1) signal. This signal asserts OMNIBUS signals CPMA DISABLE L and BRK IN PROG L and causes the VT8-E priority to be placed on the DATA lines during TS4. CPMA DISABLE L causes the CPU CPMA Register to be disconnected from the OMNIBUS MA lines, while BRK IN PROG L ensures that only data break devices place priority information on the DATA lines during TS4.

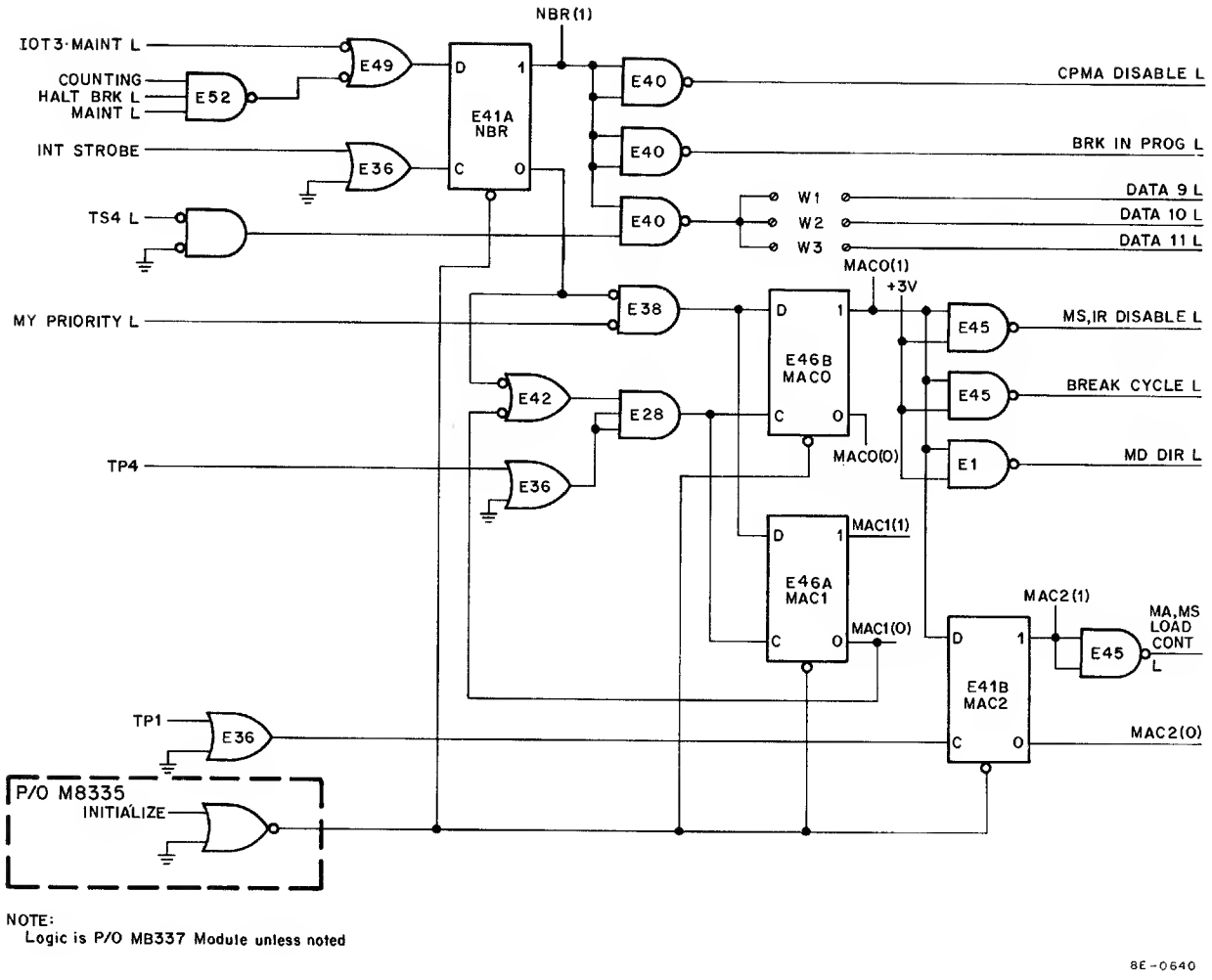


Figure 12-31 Data Break Control Logic

If the VT8- E has highest priority, MY PRIORITY L is asserted by the Priority logic (Figure 12-33). This signal is NANDed with the 0-output of the NBR flip-flop to produce a high logic level at the D-input of both the MAC0 and MAC1 flip-flops; the flip-flops are set at TP4 time via NAND gate E28. The MAC0(1) signal asserts MS, IR DISABLE L, BREAK CYCLE L, and MD DIR L, and enables the MAC2 flip-flop to be set at TP1 time of the data break cycle, thereby asserting MALC L. These OMNIBUS signals complete the CPU takeover process. MS, IR DISABLE L forces the CPU to enter the Direct Memory Access (DMA) state and disables the CPU IR Register. The MALC L signal prevents the CPMA Register from being clocked during the data break operation, while the BRK CYCLE L signal is applied to the programmer's console and can be monitored on the display panel.

The MD DIR L signal is asserted so that the data word transferred during the data break timing cycle is rewritten in the memory location during the write half of the memory timing cycle.

The MAC1(0) signal is applied to NOR gate E42 to ensure that MAC0 and MAC1 can be cleared by TP4 whenever NBR is cleared at INT STROBE time. The MAC1 and MAC2 outputs are used as gating signals elsewhere in the Display logic.

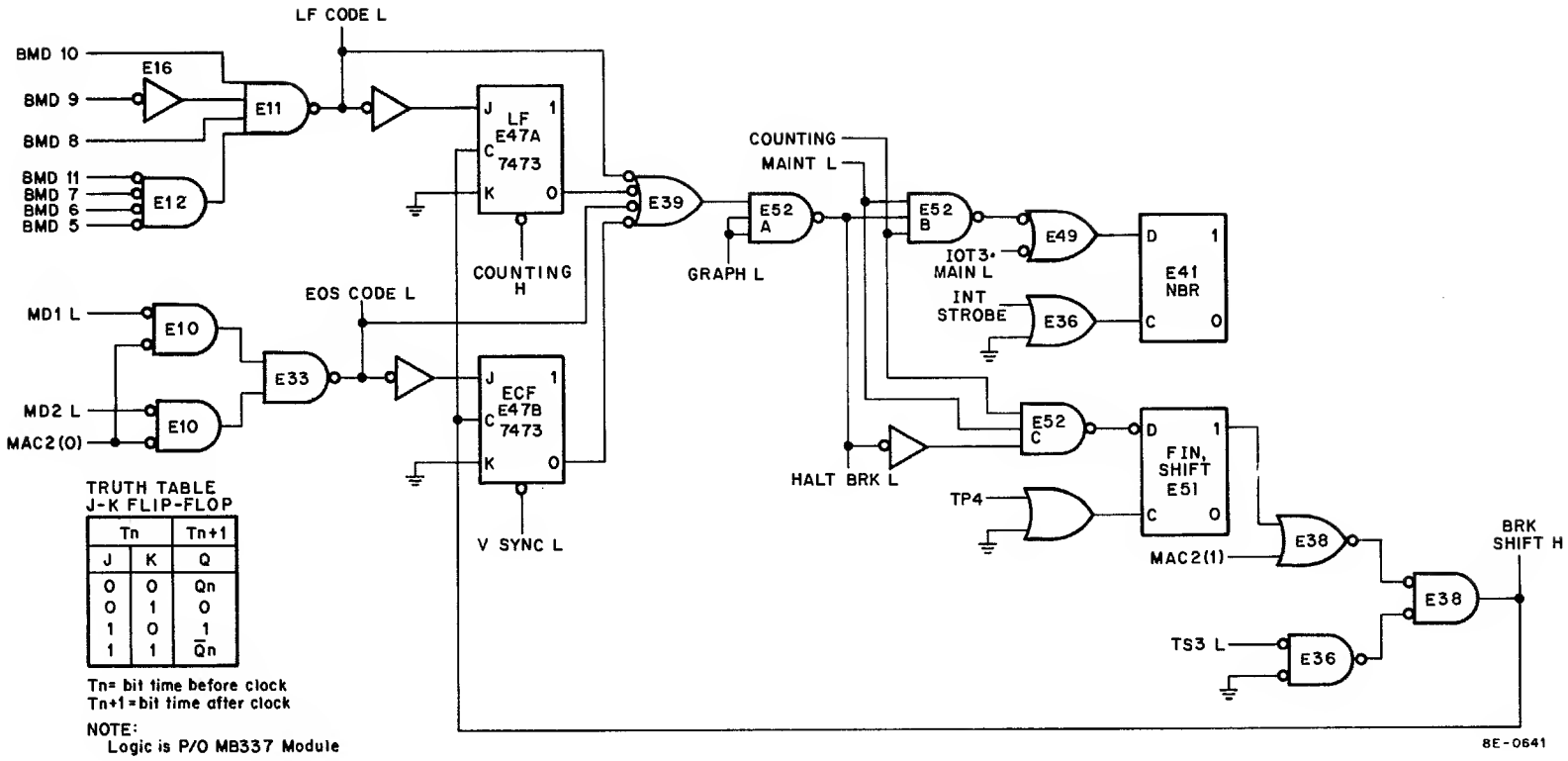


Figure 12-32 Data Break Halt, Line Feed/EOS Logic

12.4.2.6 Data Break Halt, Line Feed, and End-of-Screen Logic – The Data Break Halt, Line Feed, and End-of-Screen logic is shown in Figure 12-32. This logic is used to clear the NBR flip-flop and stop Single Cycle Data Breaks as follows:

a. If the line feed ASCII code (012) is detected on the MD lines, E47A sets. This clears NBR if the counter has not overflowed and the Maintenance mode is not enabled.

b. If the Character Counter overflows when 64 or 32 characters are transferred, counting is negated.

c. If the EOS code is detected (Figure 12-7) and EOS CODE L is asserted.

d. If V SYNC L is asserted at the end of the vertical scan.

If NBR is cleared by EOS CODE or LF CODE before the Character Counters have counted 64 or 32 characters, FIN SHIFT (E51) sets. This allows the counters to continue counting until they overflow (read all 0s) so that they will contain a 0 count when the next data break is initiated. FIN SHIFT also allows BRK SHIFTS to be generated in order to shift the line buffer data into the correct position. FIN SHIFT is clocked at each TP4 time and will clear at the first TP4 time after COUNTING is negated.

IOT3 • MAIN L is used to set NBR to cause one Single Cycle Data Break if the DPMB Maintenance instruction is executed by the program.

12.4.2.7 Priority Logic – The Priority logic is shown in Figure 12-33. Similar logic is contained on all interfaces that connect to the OMNIBUS. Priority is checked during TS4 immediately following the INT STROBE signal that sets the NBR flip-flop.

The VT8-E can have priority 10, 11, or 12. The device having the lowest priority (12) asserts the DATA 11 L signal during TS4. Assume that priority 11 is assigned. This priority causes the VT8-E to assert the DATA 10 L signal during TS4 L (jumper W2 in the Data Break Control logic is connected). Jumpers P10 and P9' must be connected in the Priority logic. Because the DATA EN B L signal is asserted when NBR(1) is high, any data break device with a higher priority can enable one of the NAND gates (the DATA EN A L signal is high throughout the priority check). Thus, MY PRIORITY L is not asserted and VT8-E data breaks do not begin.

If the VT8-E is assigned priority 10, jumpers P10 and P9 are connected. Higher priority devices can assert any of DATA lines 0 through 8, thereby preventing the VT8-E from beginning data breaks. However, any device with a lower priority, 11 or 12, must wait until the VT8-E relinquishes control of the CPU.

12.4.2.8 Line Buffer Register and Control Signal Logic – The Line Buffer Register logic is shown in Figure 12-34. The register comprises four DEC 2518 ICs (hex 32-bit Shift Registers) and is loaded from the MD lines during each data break cycle [MAC2 (0) is asserted low] by control signals generated in the Line Buffer Register Control logic (Figures 12-35 and 12-36).

If 32 alphanumeric characters are to be displayed, Component Registers B1 and B2 are used as a 12 X 32-bit Shift Register that is loaded with the 32 ASCII-coded characters. If 64 characters must be displayed, the A1 and A2 Component Registers are also used as a 12 X 32-bit Shift Register. However, the two 12 X 32-bit registers are loaded alternately, word by word from the MD lines. Consequently, they function together as a 12 X 64-bit Shift Register. If graphic data is displayed, the A and B Registers operate as two independent 12 X 32-bit Shift Registers. While one is displaying two scan lines of data, the other is refreshing for the next two scan lines.

When the LD B L signal, for example, is asserted, the 12 X 32-bit B Register can be loaded from the MD lines. Data gated to the LOAD inputs is shifted by the CLK B signal. When the LD B L signal is negated, the LOAD inputs are disabled; the CLK B signal produces an end-around shift of the data that has been loaded.

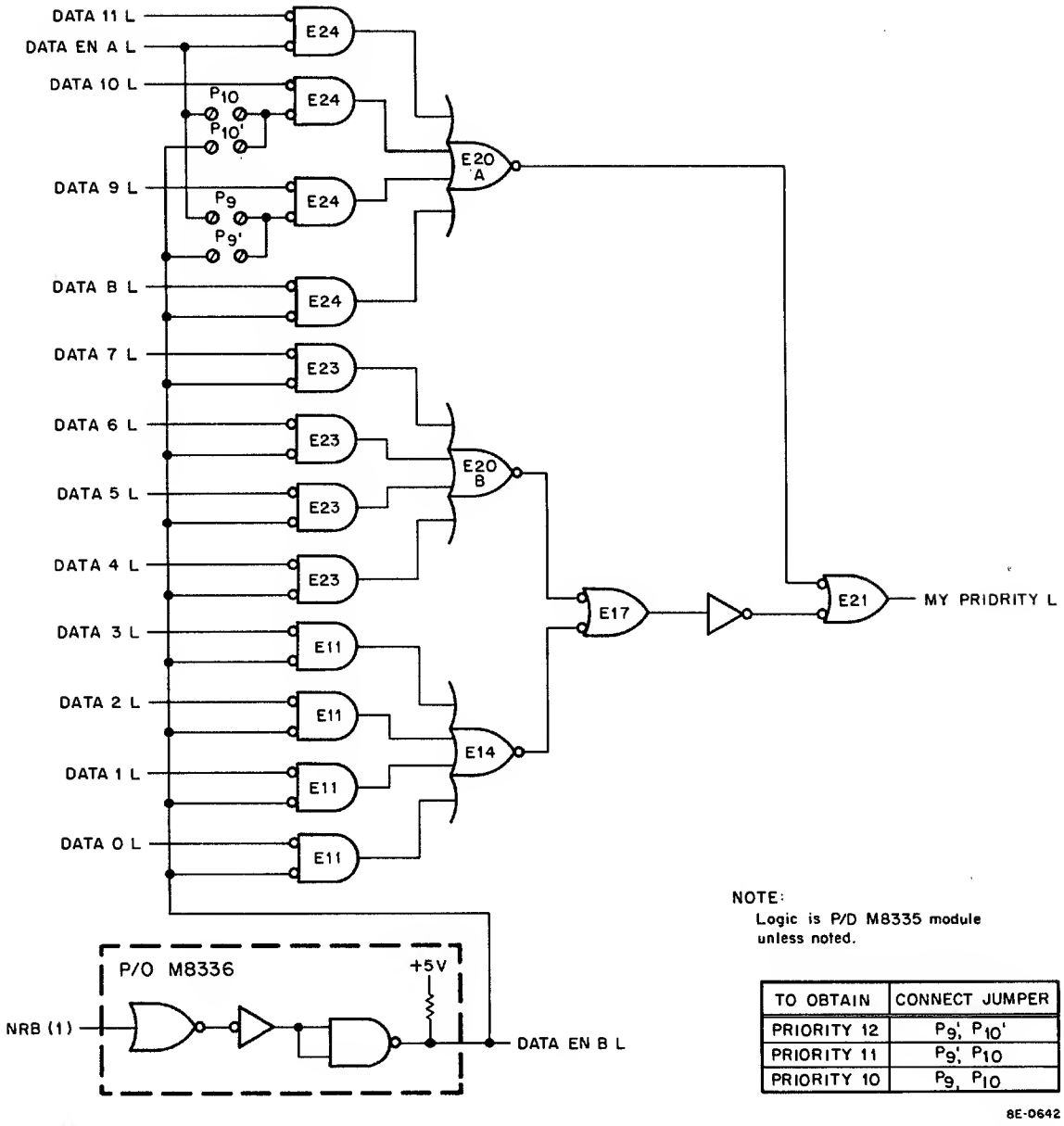


Figure 12-33 Priority Logic

Three DEC 74157 ICs (quad multiplexers) are included in the Line Buffer Register logic. The READ SELECT signal controls the multiplexers, causing either the A_n inputs or the B_n inputs to be gated to the f_n outputs. The outputs are transferred to the Video Buffer logic, alphanumeric or graphic, and converted to serial video information.

Figure 12-37 shows a timing diagram that illustrates how the Line Buffer Register and the multiplexer are controlled when 32 alphanumeric characters are to be displayed. The timing shown is relative; pulse durations, gate widths, etc., may or may not be actual.

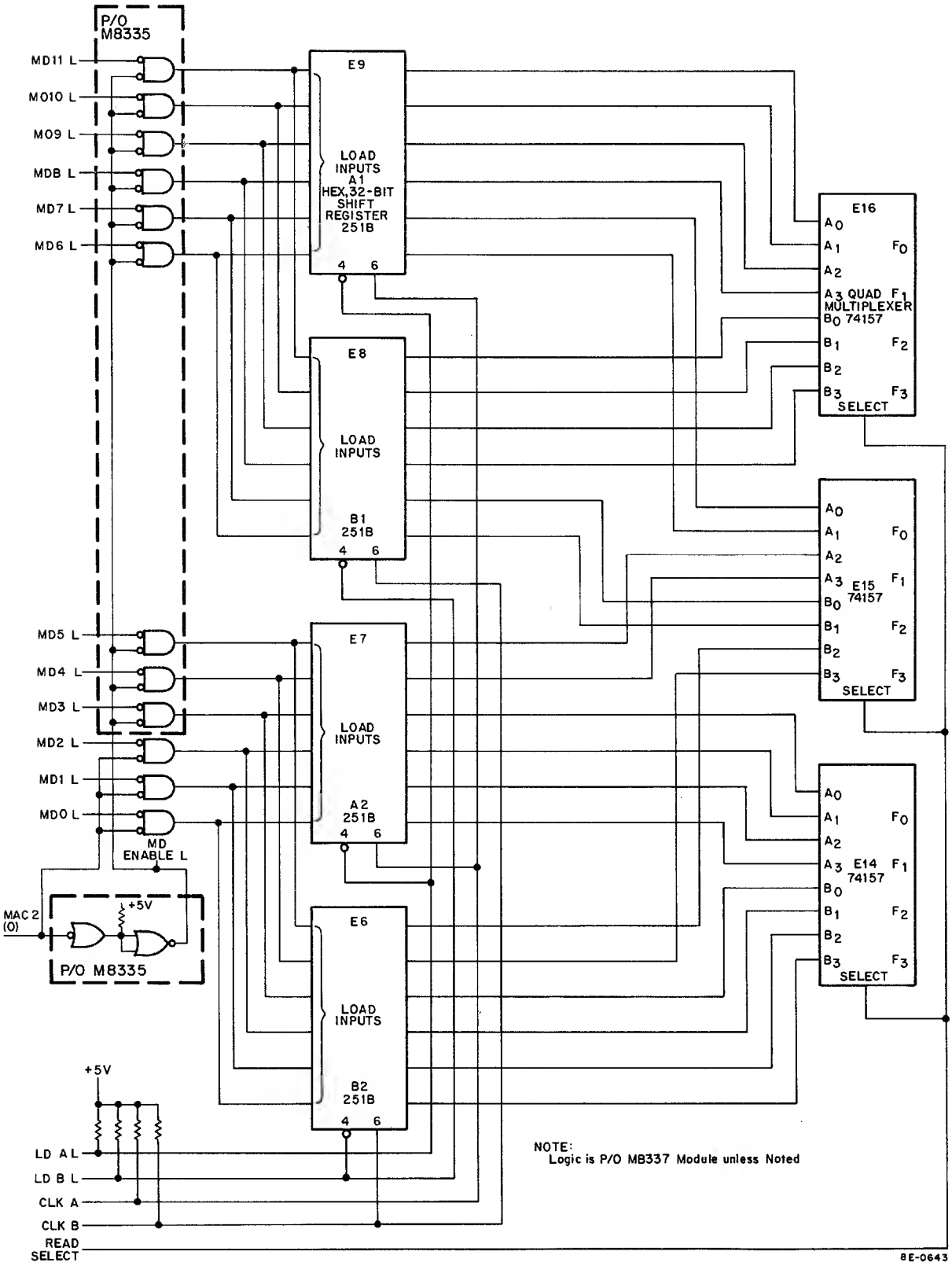


Figure 12-34 Line Buffer Register Logic

The period of time represented as t_1 is that period during which 32 data breaks are being performed (remember that two scan lines are set aside for this purpose). During t_1 the Line Buffer Register must be loaded from the MD lines. The Line Buffer Register Control logic (Figure 12-35) asserts the LD B L signal (the signal E19-D is low throughout t_1, keeping the VIS ZONE L signal high). Each data break cycle causes a data word to be gated to the B Register LOAD inputs. The BRK SHIFT signal that occurs during TS3 L of the break cycle is gated through NAND gate E37A, since the ALPHA CLK ALT is always cleared during a 32 character operation. This causes a CLK B signal to be produced. When 32 data words have been loaded into the register, the COUNTING signal goes low and data breaks cease (COUNTING goes low at TP1 of the break cycle, while BRK SHIFT is asserted during TS3 L).

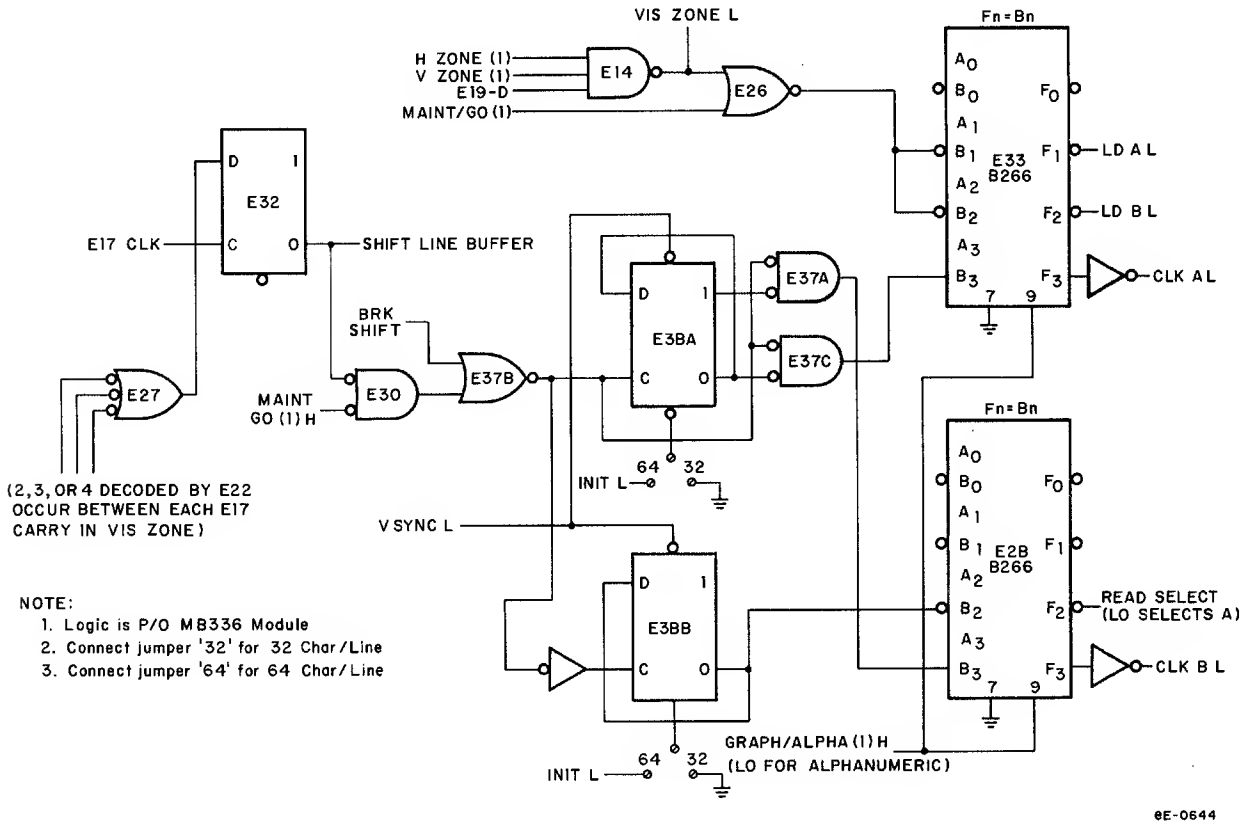


Figure 12-35 Line Buffer Register Control Logic

Throughout each of the next eight scan lines, the Line Buffer Register must be shifted end-around. Period t_2 represents the third scan line and the beginning of the fourth. The VIS ZONE L signal is asserted when HZONE(1) goes high. The LD B L signal is negated, placing the register in the recirculating mode. During the time that VIS ZONE L is low, the VT8-E timing generates 32 SHIFT LINE BUFFER signals. These signals enable NAND gate E37A, thereby generating the CLK B signal. The register is shifted end-around by 32 CLK B signals. (Note that 31 CLK B signals are sufficient to shift all 32 characters through the multiplexer, but 32 are needed for the recirculation.) Each time a character is placed on the register outputs, the multiplexer gates it to the ROM Character logic (only the 6-bit ASCII code, bits 6–11, is gated to the ROM). There it is converted to serial video information for display.

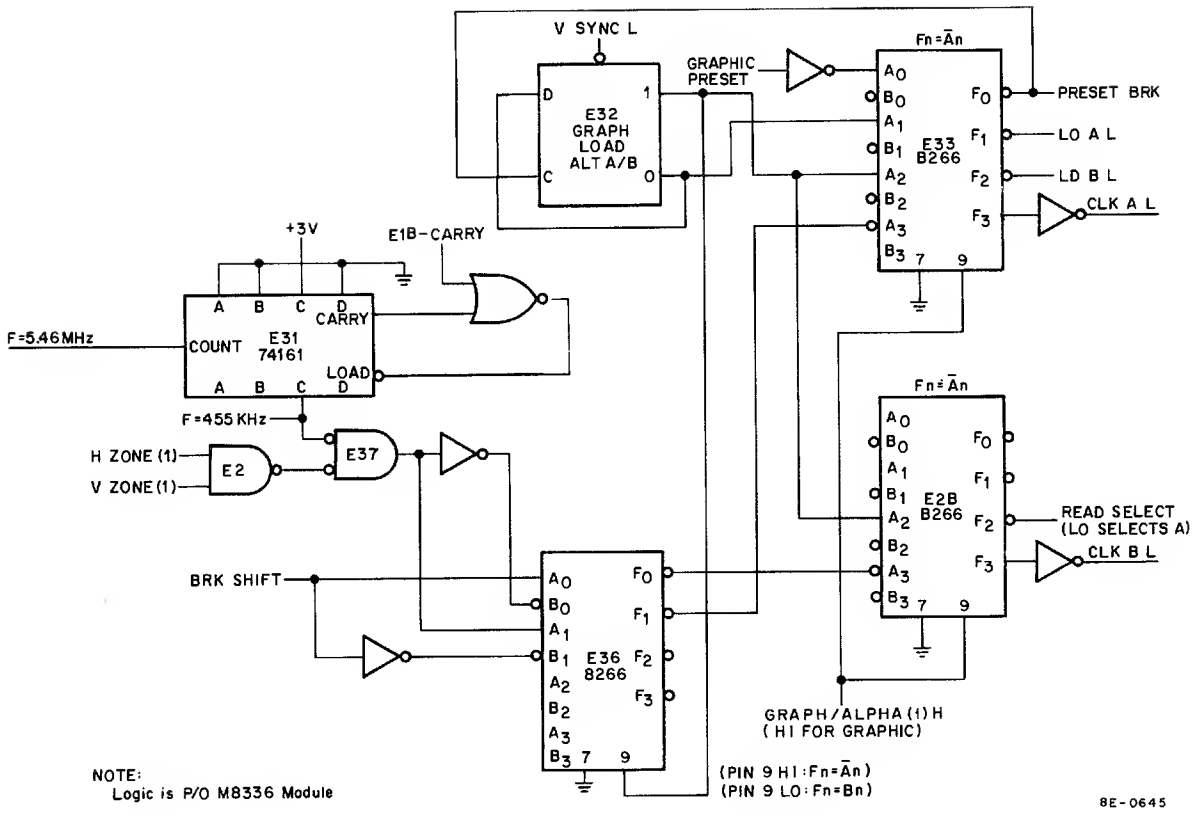


Figure 12-36 Line Buffer Register

The same operation is performed during each succeeding scan line. At the end of the tenth scan line, the character line has been displayed. Another PRESET BRK signal is generated and 32 more characters are loaded into the Line Buffer Register. Note that as these next 32 characters are shifted into the register, the 32 displayed by the just-completed character line are shifted out. Because video is not enabled unless VIS ZONE L is low, there is no danger of these earlier characters being displayed again.

Figure 12-38 shows a timing diagram that illustrates how the Line Buffer Register and the multiplexer are controlled when 64 alphanumeric characters are loaded from the MD lines. Both the A and B Registers are used, providing 64 bits of storage space. As the timing diagram illustrates, the A and B Registers are loaded alternately so that each contains 32 characters when 64 data breaks have been completed. The registers are alternately recirculated during each succeeding scan line (this timing is not shown, but is similar to that of Figure 12-37); when the characters have been displayed, 64 new characters are shifted into the register.

Figure 12-36 shows the logic that controls the Line Buffer Register and the multiplexer during a graphic display. Figure 12-39 shows a timing diagram that illustrates how the graphic data is transferred through the Line Buffer Register logic. Read Select changes every Graphic PRESET which corresponds to every other scan line within the visible zone. When displaying Reg A, CLK A L is generated once for every 12 graphic dot positions that are displayed. This shifts a new word to the output of the Shift Register. The word is then loaded into the Video Buffer after the 12 bits of the previous word have been displayed.

Both the A and B Registers are used when graphic data is displayed. One register is loaded from the MD lines with 32 data words; simultaneously, the information in the other register is displayed.

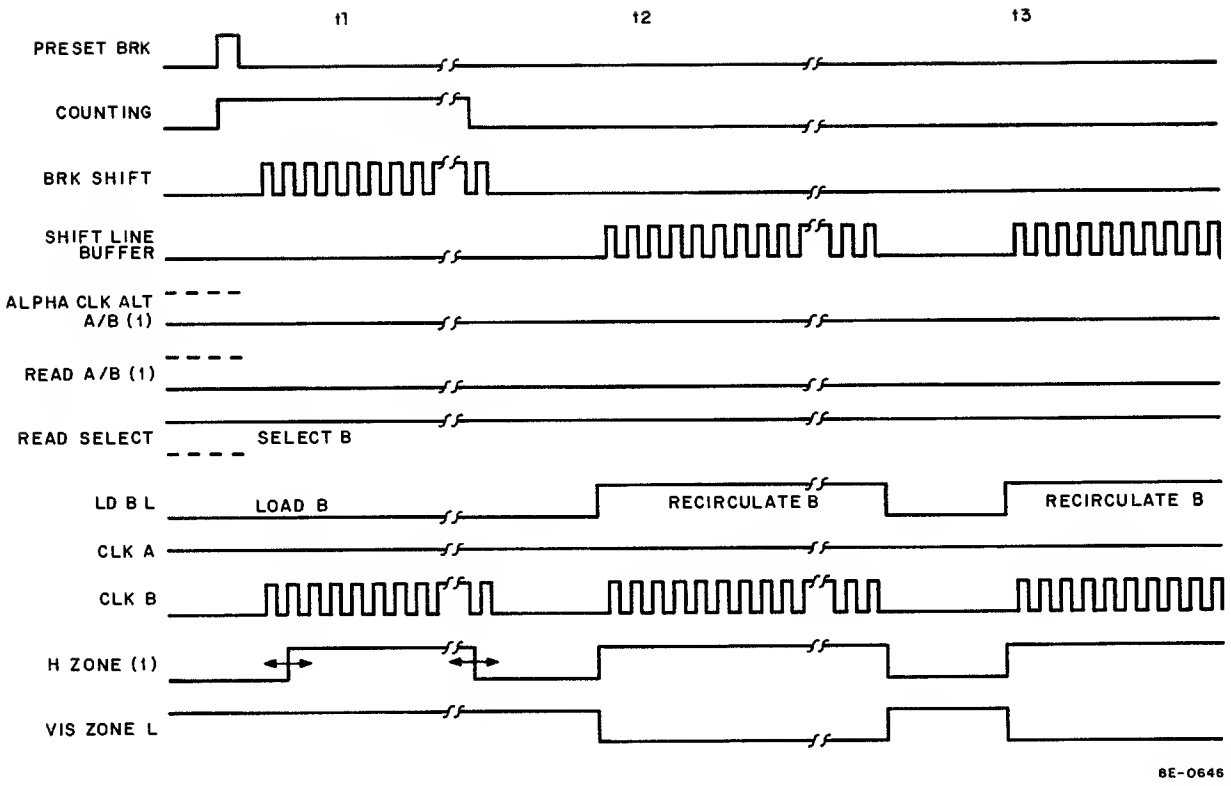


Figure 12-37 Line Buffer Timing for 32 Character Line

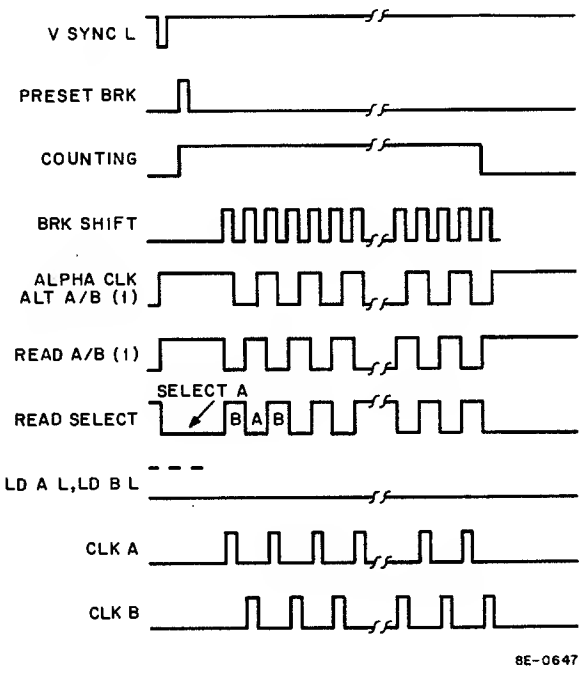


Figure 12-38 Line Buffer Timing for 64 Character Line

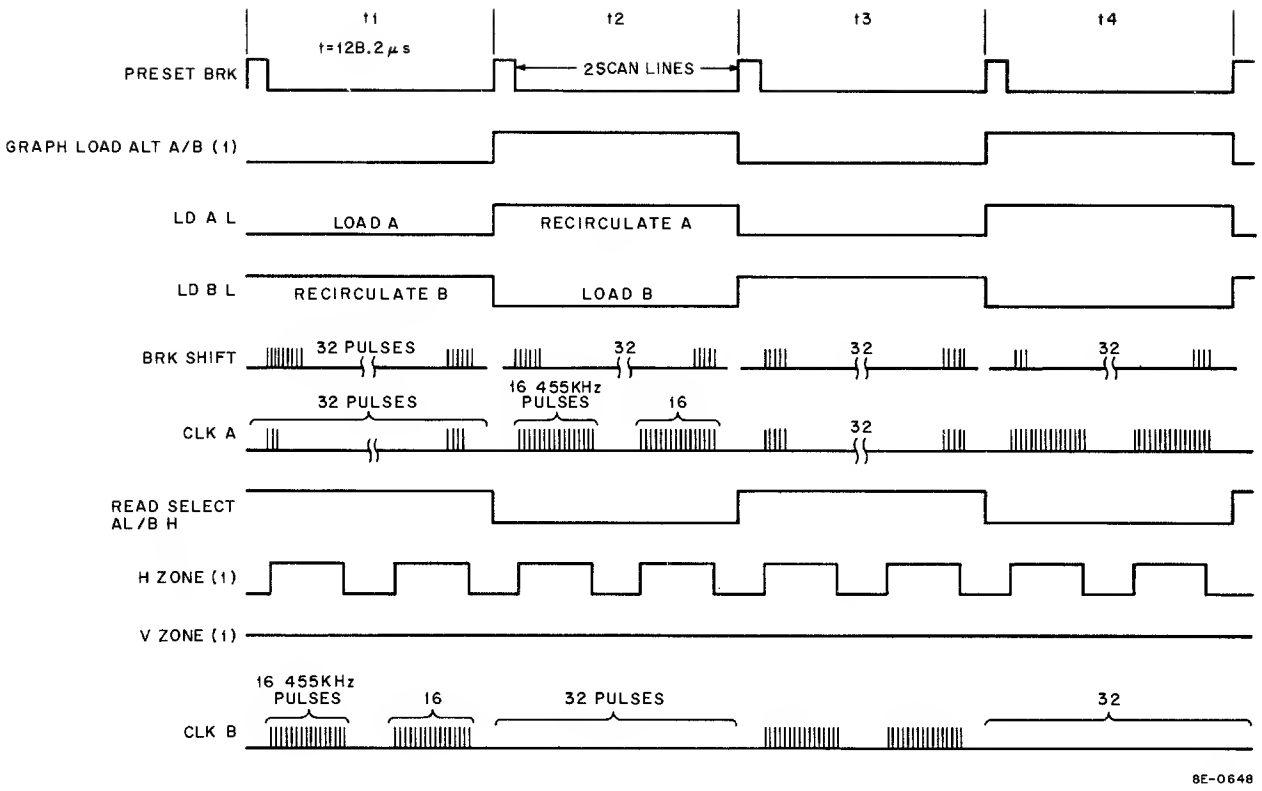


Figure 12-39 Line Buffer Timing

12.4.2.9 ROM Character Generator Logic – The ROM Character Generator logic is shown in Figure 12-40. Included in the figure is a representation of the alphanumeric Video Buffer Register. The major components of the character generator are three 23-XXA2 1024-bit read-only memories; each is organized to provide 256 4-bit word locations. A functional logic diagram of 23-XXA2 is shown in Figure 12-41.

ASCII-coded characters are gated from the Line Buffer Register to each ROM on the six lines designated BIT 6–11. The five most significant bits of the character, bits 6–10, are applied to a 1-of-32 decoder (Figure 12-41). The ROM ROW CNT signals, generated in the VT8-E timing, are applied to 1-of-8 decoders. These three signals select one of 256 4-bit data words. The LSB of the ASCII character, bit 11, is used to gate the 4-bit word out of the ROM to the Video Buffer Register, a DEC 7496 5-bit Shift Register. As Figure 12-40 shows, an odd ASCII character (bit 11 is logic 1) causes the ODD ROM outputs to be selected, while an even character causes the EVEN ROM to be selected. The XTRA ROM provides the necessary fifth bit of the data word and is selected for both even and odd characters.

Remember that ten horizontal scan lines are required to display one character line. During the first two scans, the characters are shifted into the Line Buffer Register. During each of the next eight scans, the Line Buffer Register is recirculated. Bits 6–11 of a character are the same during each scan. The ROM ROW CNT signals change during each scan, cycling through the counts 000_2 to 111_2, where ROM LS ROW CNT is the LSB. Consequently, eight consecutive locations are selected for each ASCII character. The first location is blank, the next seven contain the video information that is ultimately displayed.

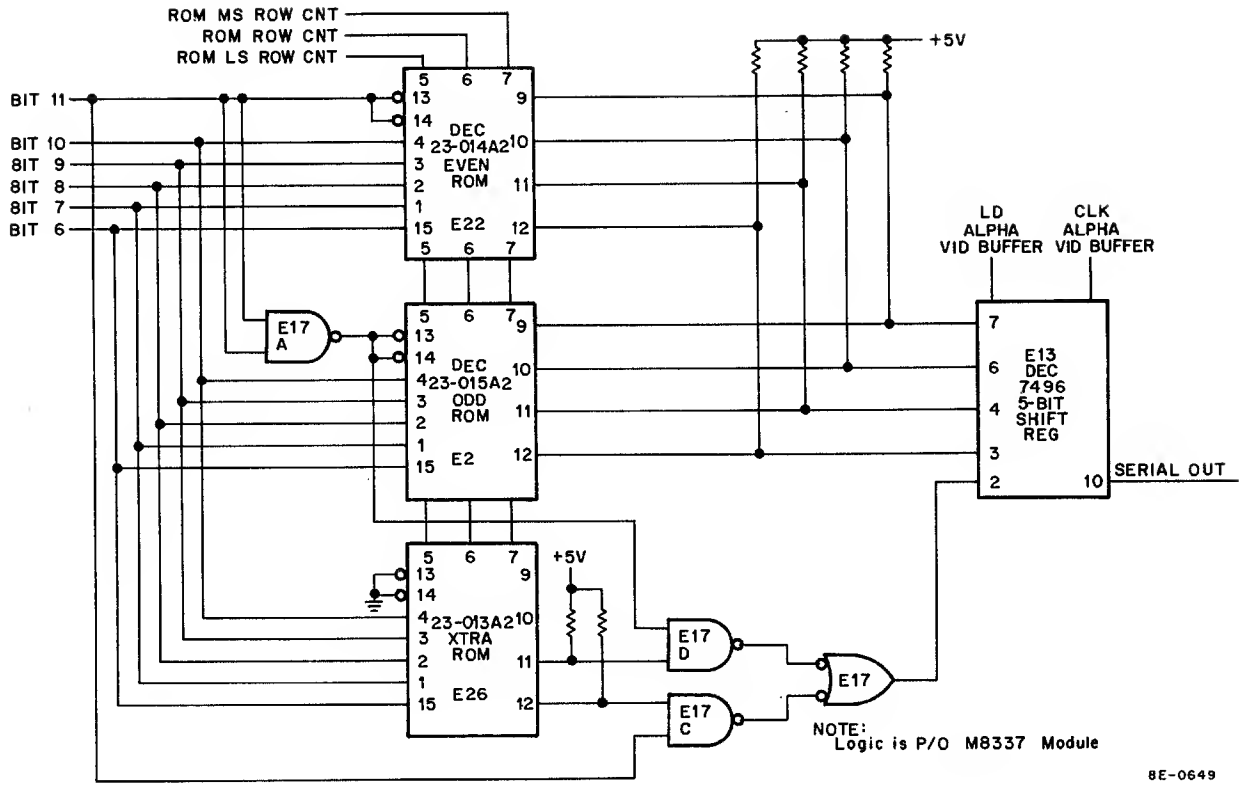


Figure 12-40 ROM Character Generation Logic

Consider the ASCII code for the character H: 001 000 (10_8). Bits 6–10 (001 00) are applied to the 1-of-32 decoder during each scan. During Scan Line 3, the ROM ROW CNT signals are low (000_2). The data in the addressed location is 0000, and no video is displayed. During Scan Line 4, the ROM ROW CNT signals are 001_2. The data in this location is 1000 and is displayed as video. Table 12-8 relates the eight scan lines, the ROM ROW CNT binary representations, and the data in the addressed locations.

The fifth data bit for each scan is taken from the XTRA ROM. Note that only two outputs are available from this ROM. If the character is even, the output at pin 11 is gated to the Video Buffer; if the character is odd, the output at pin 12 is gated. This ROM is addressed exactly as is the EVEN ROM, as indicated in Table 12-9. The fifth data bit for H is taken from pin 11 of the XTRA ROM. The result is shown below.

Scan Line	Data Bits Gated to Video Buffer
3	00000
4	10001
5	10001
6	10001
7	11111
8	10001
9	10001
10	10001

NOTE: The pattern is generated for H.

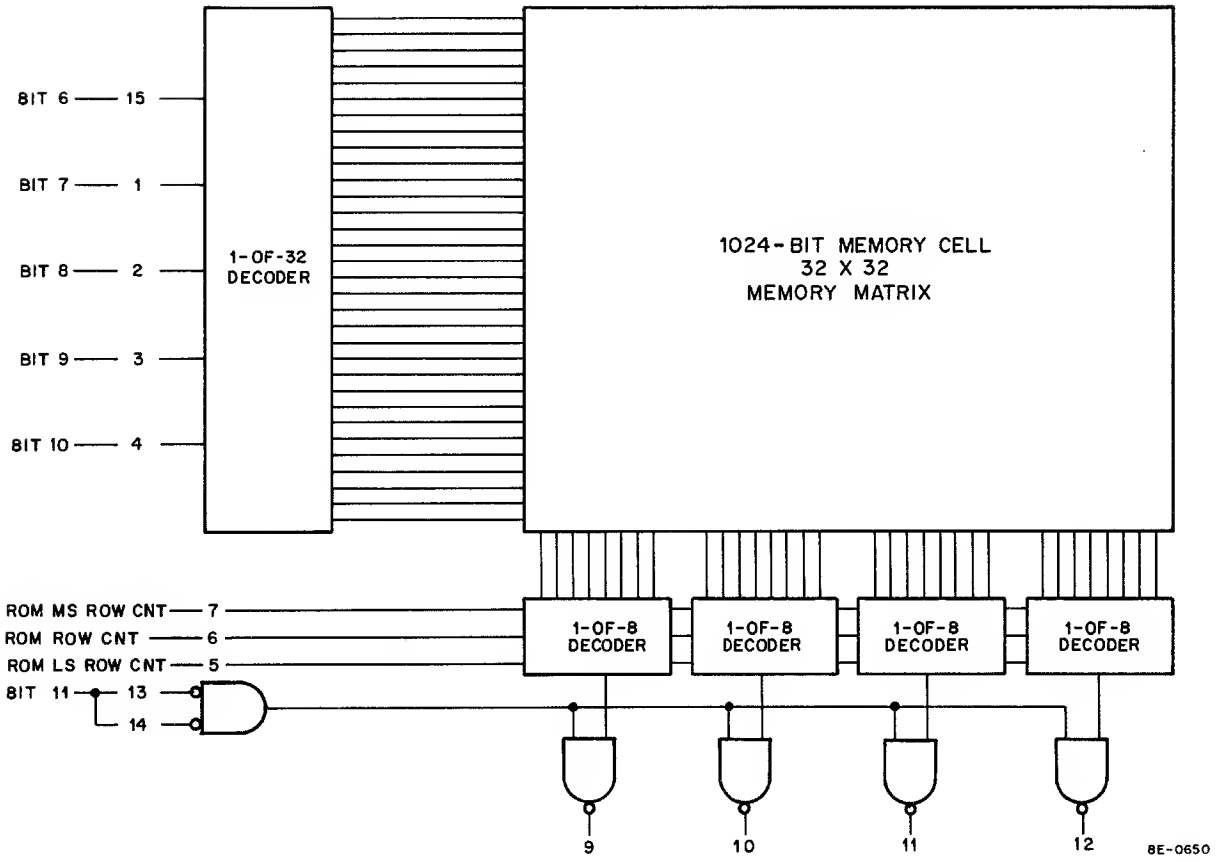


Figure 12-41 ROM Functional Logic Diagram

Table 12-8
Character H, EVEN ROM Data Bits

Scan Line	Bits 6–10	ROM ROW CNT Binary Representation	Data Word in Addressed Location
3	00100	000	0000
4	00100	001	1000
5	00100	010	1000
6	00100	011	1000
7	00100	100	1111
8	00100	101	1000
9	00100	110	1000
10	00100	111	1000

Table 12-9
Character H, XTRA ROM Data Bits

Scan Line	Bits 6–10	ROM ROW CNT Binary Representation	Data Word in Addressed Location
3	00100	000	0000
4	00100	001	0010
5	00100	010	0010
6	00100	011	0010
7	00100	100	0010
8	00100	101	0010
9	00100	110	0010
10	00100	111	0010
			PIN 11 PIN 12

The pattern table for each ROM is included in Appendix A. To locate the pattern for an ASCII character, use the following procedure:

Step	Procedure
1	If the character is even, divide the 6-bit binary representation by 2. The result gives the 6 most significant bits of the location.
2	Find this location in the Octal Location column of the EVEN ROM pattern table (Table A-1) for 4 of the data bits; find the same location in the Octal Location column of the XTRA ROM pattern table (Table A-3) for the fifth data bit. For example: When the binary representation of character T, 010 100 (24_8), is divided by 2, the result is 001 010 (12_8); octal locations 120–127 of the EVEN and XTRA ROMs contain the video information for the character.
3	If the character is odd, take the even binary representation immediately preceding the odd binary representation and divide by 2.
4	Find this location in the ODD and XTRA ROM pattern tables (Tables A-2 and A-3). For example: To find the pattern for character G, 000 111 (07_8), divide 000 110 (06_8) by 2; the result, 000 011 (03_8), identifies locations 030–037 as yielding G.

12.4.2.10 Alphanumeric Video Buffer Control Logic – Figure 12-42 shows the alphanumeric Video Buffer Control logic. The logic generates the signals that allow the Video Buffer to convert the parallel ROM bits to serial alphanumeric video bits. The logic is shown for 32 characters per line; if 64 characters per line are being displayed, the input clock frequency is 10.92 MHz. Figure 12-43 shows a timing diagram for the 32 character per line operation. Refer to both figures when reading the logic description.

The 5.46 MHz signal is gated by the logic to produce the LD ALPHA VIDEO BUFFER and CLK ALPHA VIDEO BUFFER signals. The E17 up-counter provides the necessary gating signals. The A, B, and C outputs of E17 are applied to the DEC 7442 BCD-to-Decimal Decoder, E22. When E22 decodes decimal 2, E26C is enabled and the next clock produces a LD ALPHA VIDEO BUFFER signal. When E22 decodes decimal 3 through 7, E26B is enabled

and 5 clock pulses are gated through to produce CLK ALPHA VIDEO BUFFER. A VID EN signal is also generated when E22 decodes decimal 3 through 7. This signal is asserted through the E28 multiplexer when the VIS ZONE L signal is low (note that the VIS ZONE L must be low for E22 to decode decimal 1 through 7).

Because E17 determines character rate, one LD ALPHA VIDEO BUFFER signal, one VID EN signal, and five CLK ALPHA VID BUFFER signals are generated each time a character is shifted from the Line Buffer Register. Remember that 32 SHIFT LINE BUFFER signals are used to recirculate the Line Buffer Register during each scan. Each SHIFT LINE BUFFER signal generates a CLK B signal that shifts a different character to the ROM Character Generator. The character generator produces five bits that represent the character. A LD ALPHA VIDEO BUFFER signal then parallel loads these bits into the Video Buffer Register.

Five CLK ALPHA VIDEO BUFFER signals shift the data bits out of the buffer to the video logic. The VID EN signal enables the video logic to generate signals for the display. Note that the LD ALPHA VID BUFFER signal, designated A in Figure 12-43, loads the character that is shifted from the Line Buffer Register by the CLK B signal designated A. While this character is being shifted from the Video Buffer, the new 5-bit character is being gated to the buffer inputs. Note, also, that the character horizontal spacing is determined by the gating of the 5.46 MHz signal. The character width is represented by five clock pulses (0.185 inches for 32 characters/line); the horizontal spacing is represented by the two clock pulses in each character period that are not gated (indicated by the dotted-line CLK ALPHA VIDEO BUFFER pulses). Thus, the spacing is 40 percent of the character width, or 0.074 inches.

Figure 12-44 shows the timing of the alphanumeric Video Buffer Control logic for 64 characters per line. The logic is the same as for 32 characters per line operation.

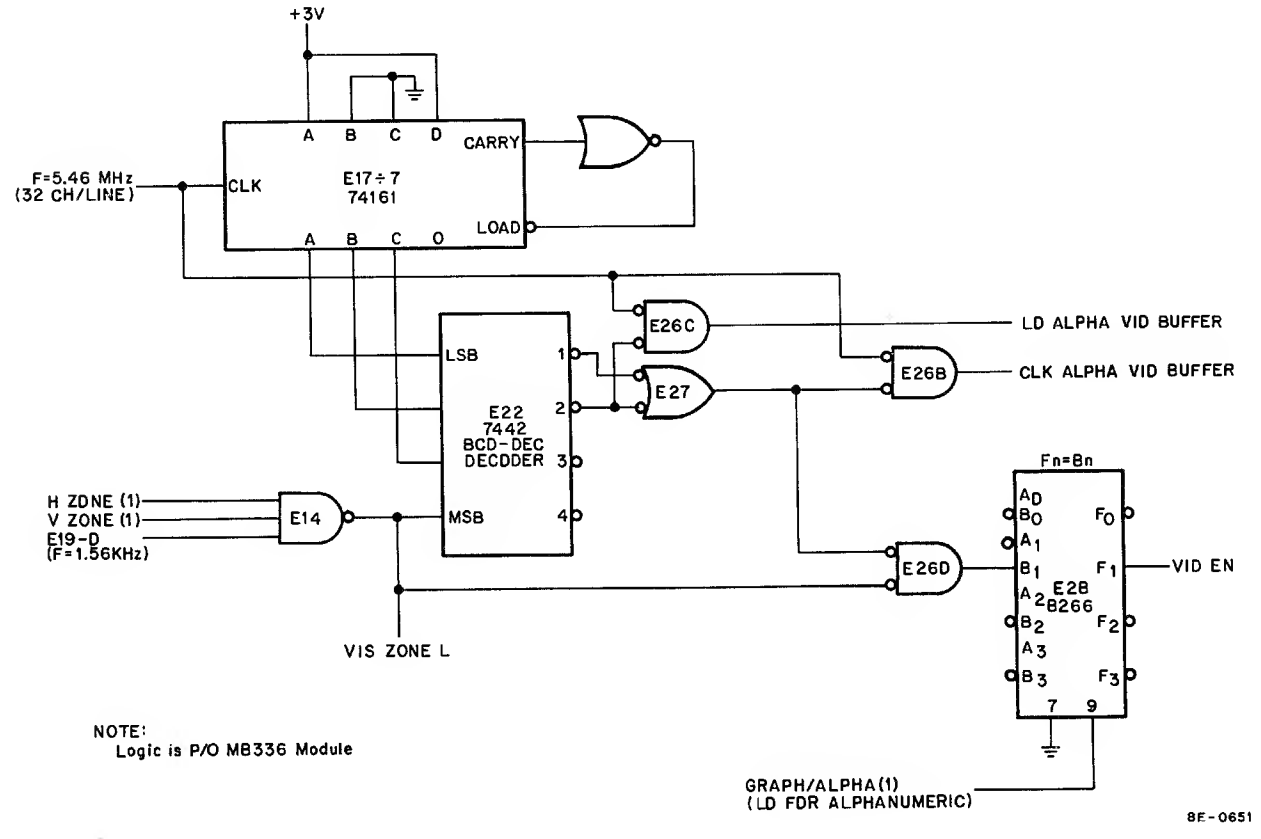


Figure 12-42 Alphanumeric Video Buffer

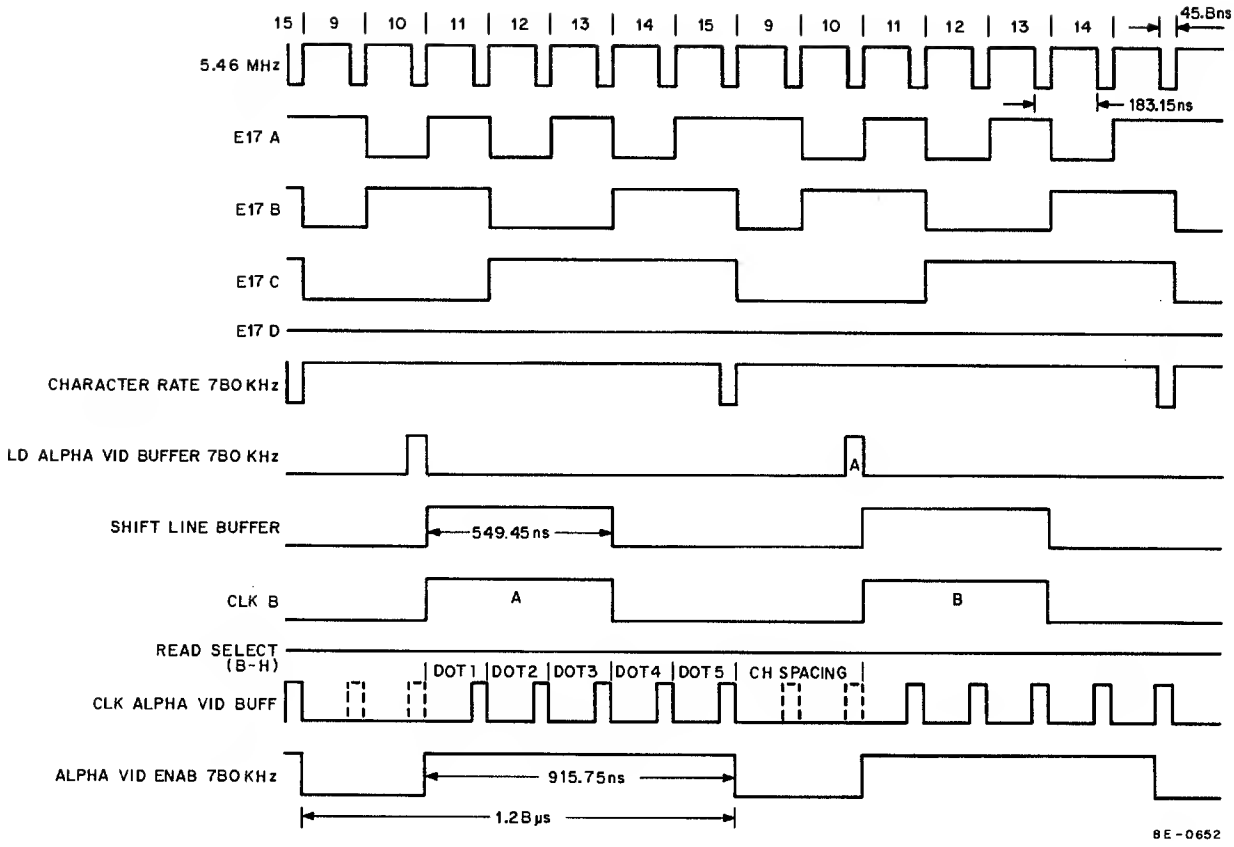


Figure 12-43 Character Timing for a 32 Character Line

12.4.2.11 Graphic Video Buffer and Control Logic – The Graphic Video Buffer and Control logic is shown in Figure 12-45. This logic converts the parallel data in the Line Buffer Register to the serial graphic video signals that are applied to the Display Mode logic.

When a data word is shifted from the Line Buffer Register, it is applied to the Graphic Video Buffer on the lines designated BIT 11–0. The Video Buffer Register comprises three DEC 7595 4-bit Shift Registers that can be parallel loaded and serial shifted. The DEC 74161 counter, E31, counts down the 5.46 MHz clock pulses to produce an LD GRAPH VID BUFFER signal at a frequency of 455 kHz. The derivation of this signal is shown in the timing diagram in Figure 12-46. Graphic Video Buffer is loaded by CLK GRAPH VID BUFFER when LD GRAPH VID BUFFER is true. This occurs every 12 clock pulses.

When the Video Buffer has been loaded, the LD GRAPH VID BUFFER signal goes low. The DEC 7495 Shift Register cannot be shifted while this signal is high. The next eleven CLK GRAPH VID BUFFER signals shift data out of the register (bit 0 is shifted out first). Note that bit 11 is not shifted from the register since only 11 shift pulses are available. Twelve CLK GRAPH VID BUFFER signals are also used to chop graphic video into distinct dots. This occurs at AND gate E28.

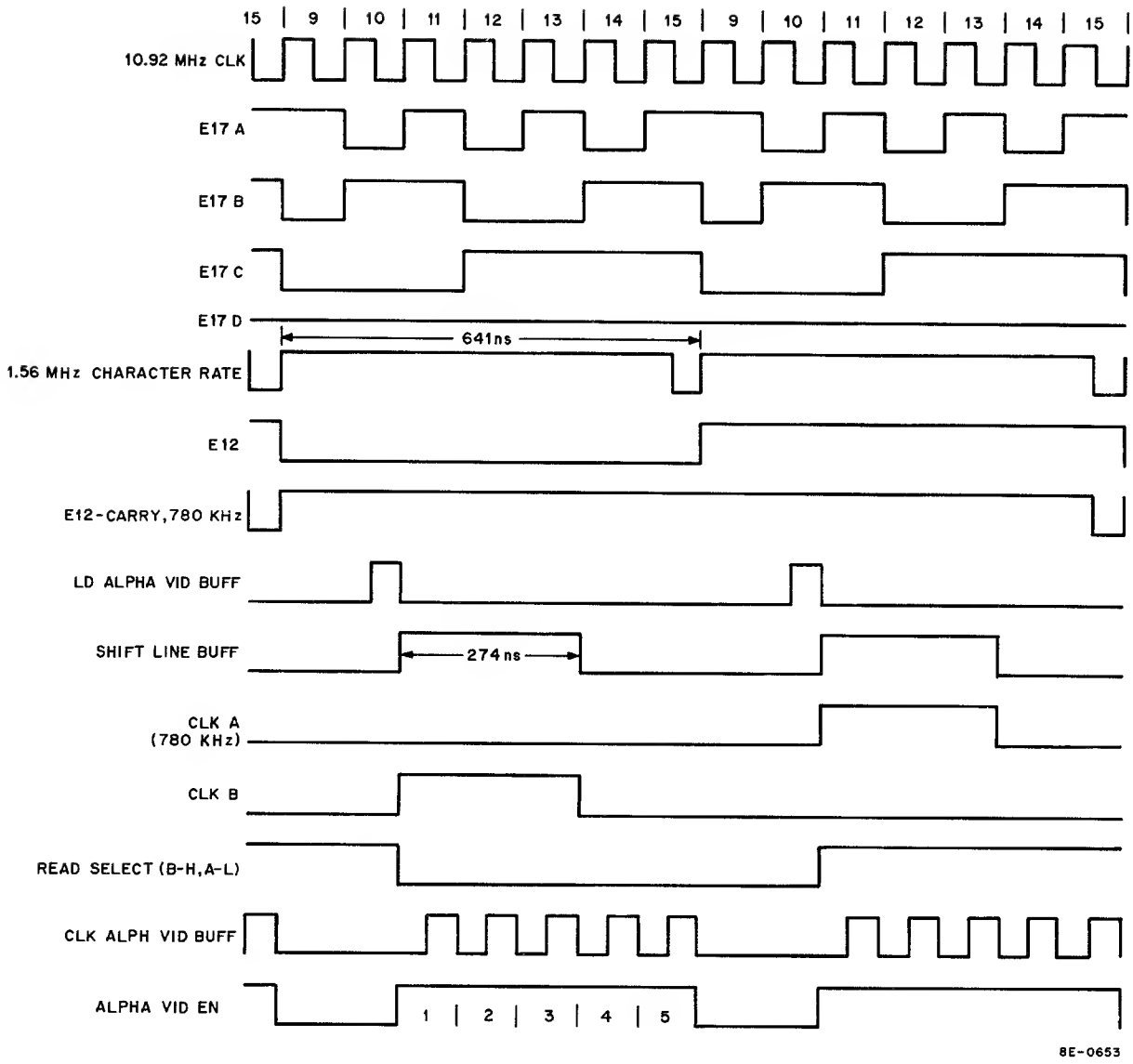


Figure 12-44 Character Timing for a 64 Character Line

12.4.2.12 Visible Field Logic – When an alphanumeric character is to be displayed, the data word transferred to the Line Buffer Register contains not only character information, but also information that controls the visible field and the mode of display. The 12-bit data word is shown in Figure 12-47.

The ASCII-coded character is contained in bits 5–11. Because the VT8-E displays a 64 character set, only bits 6–11 are used to generate character video. Control bits 1 and 2 (referred to as CB1 and CB2) are used to determine the visible field by selectively blanking the video display. Control bits 3 and 4 (referred to as CB3 and CB4) determine how the video is displayed.

Figure 12-48 shows the visible field bits logic. These bits control the visible field as outlined in the table accompanying the logic. When J-K flip-flop E44 is set, the BLANK L signal is asserted and the alphanumeric Video Buffer output is inhibited (Figure 12-50 shows how the BLANK L signal inhibits video). Flip-flop E44 is controlled in an intricate manner that can best be described by a timing diagram. This diagram is shown in Figure 12-49. The timing begins with the start of a character line, represented by the PRESET BRK signal.

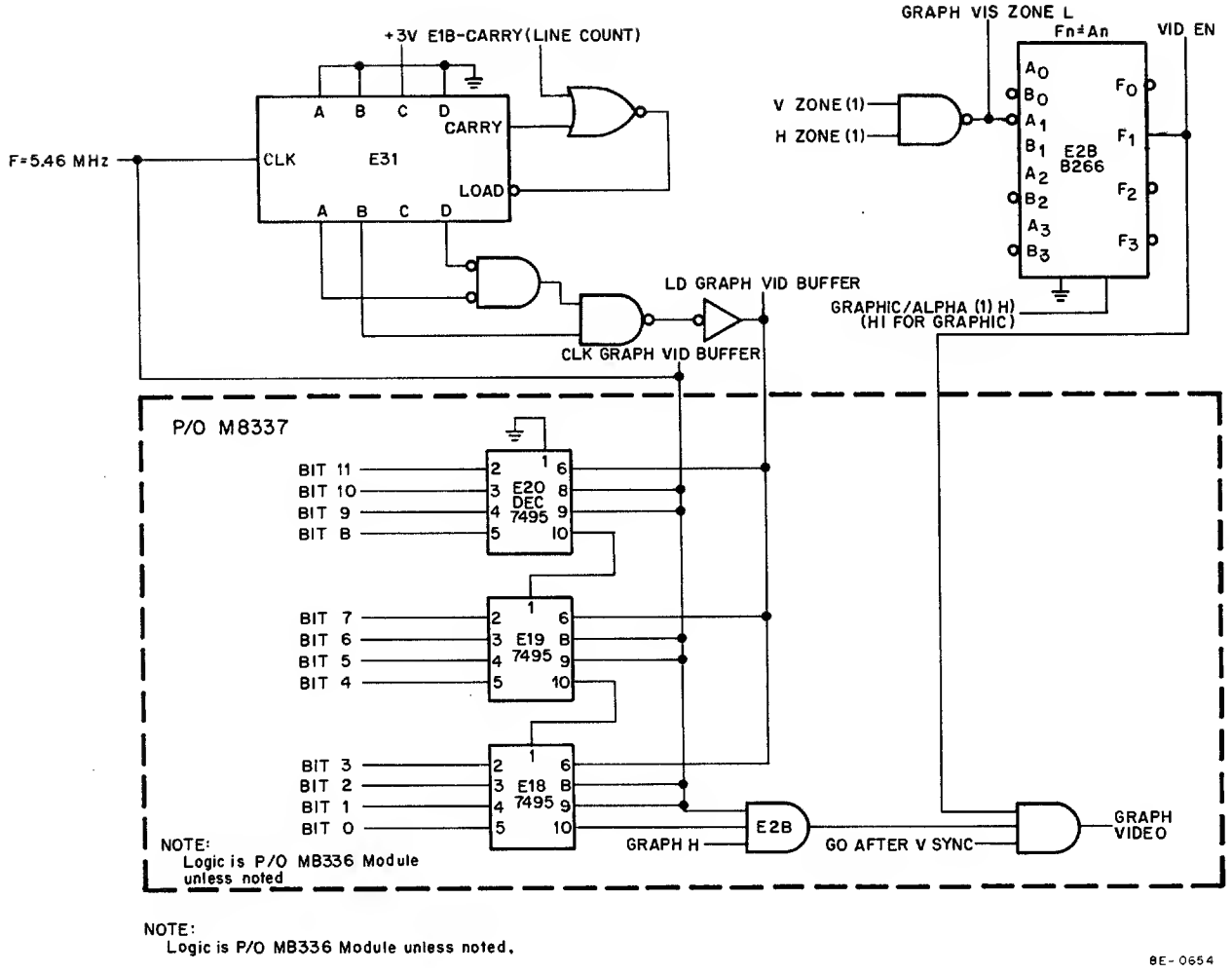


Figure 12-45 Graphic Video Buffer Control Logic

Assume that a character in the previous character line had directed the beginning of a blank field; i.e., CB1 of this character was high, while CB2 was low. When this character was shifted from the Line Buffer Register, the next LD ALPHA VID BUFFER signal to occur sets the J-K flip-flop E50B (Figure 12-47). Each succeeding character is either a NOP direction or another BBF direction (both have the same result in the present situation). At the beginning of the present character line, a PRESET BRK signal and a LINE CNT signal occur simultaneously. The leading edge of the LINE CNT signal clears the E44 flip-flop, while the trailing edge of the PRESET BRK signal sets flip-flop E50A. The next LINE CNT signal sets E44 again, because now E50A is set. All three flip-flops would remain in this state throughout the entire character line and into and through each succeeding character line if no EBF direction were received.

However, if an EBF direction is programmed into a data word, the blank field must be ended at the same point in Scan Lines 3 through 10 (although nothing is displayed in Scan Line 3). Assume that character 16 of the present character line directs an end to the blank field. The LD ALPHA VIDEO BUFFER signal corresponding to character 16 clears flip-flops E44 and E50B. For the rest of Scan Line 3, the BLANK L signal is negated. At the start of the fourth scan line, flip-flop E44 has to be set again to blank the first 15 characters. The LINE CNT signal sets the flip-flop, thereby blanking the first 15 characters of Scan Line 4. Again, the sixteenth character says EBF and clears flip-flop E44 (flip-flop B stays clear throughout). This procedure continues until the character line is completed. The second LINE CNT signal of the next character line clears flip-flop E44, which then remains clear until another BBF or an EOS is directed.

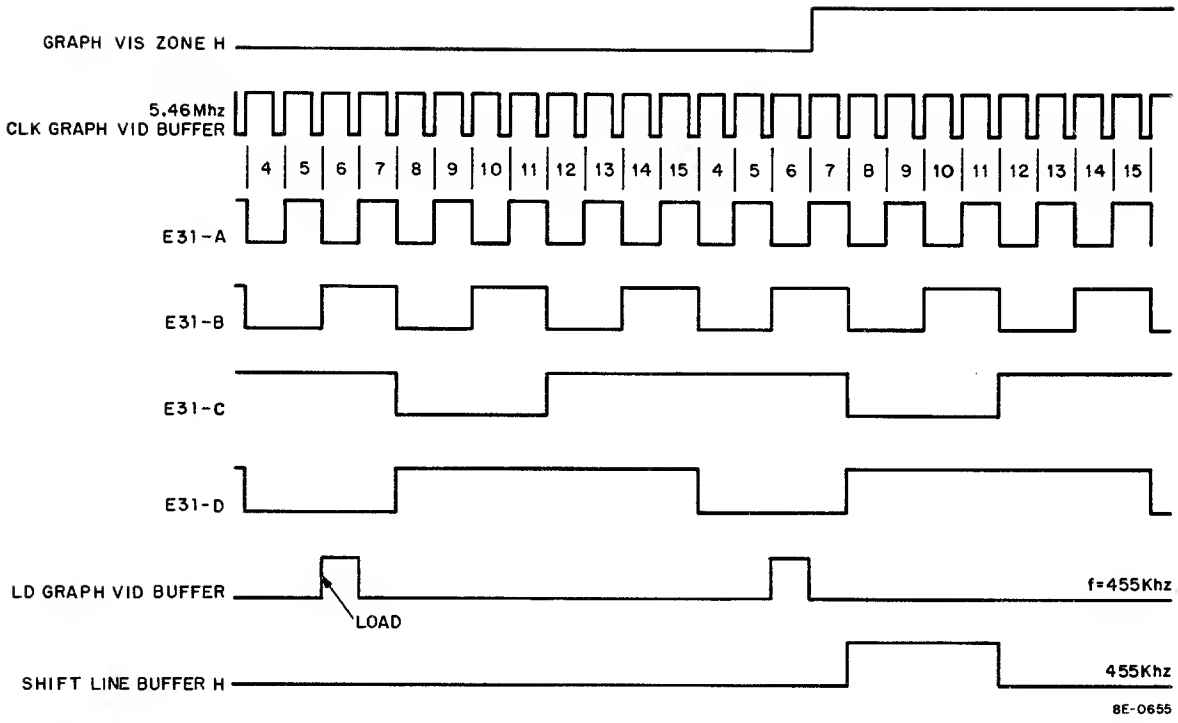


Figure 12-46 Graphic Word Timing

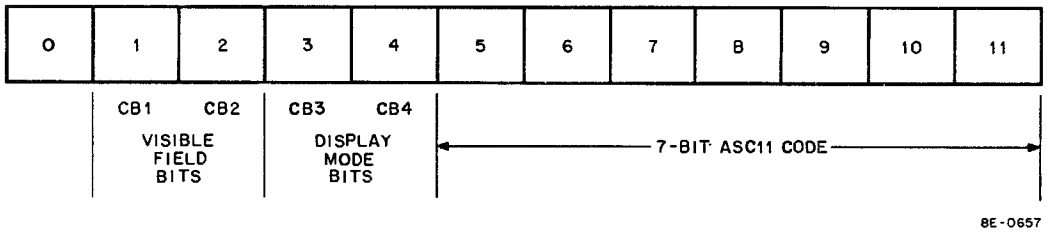
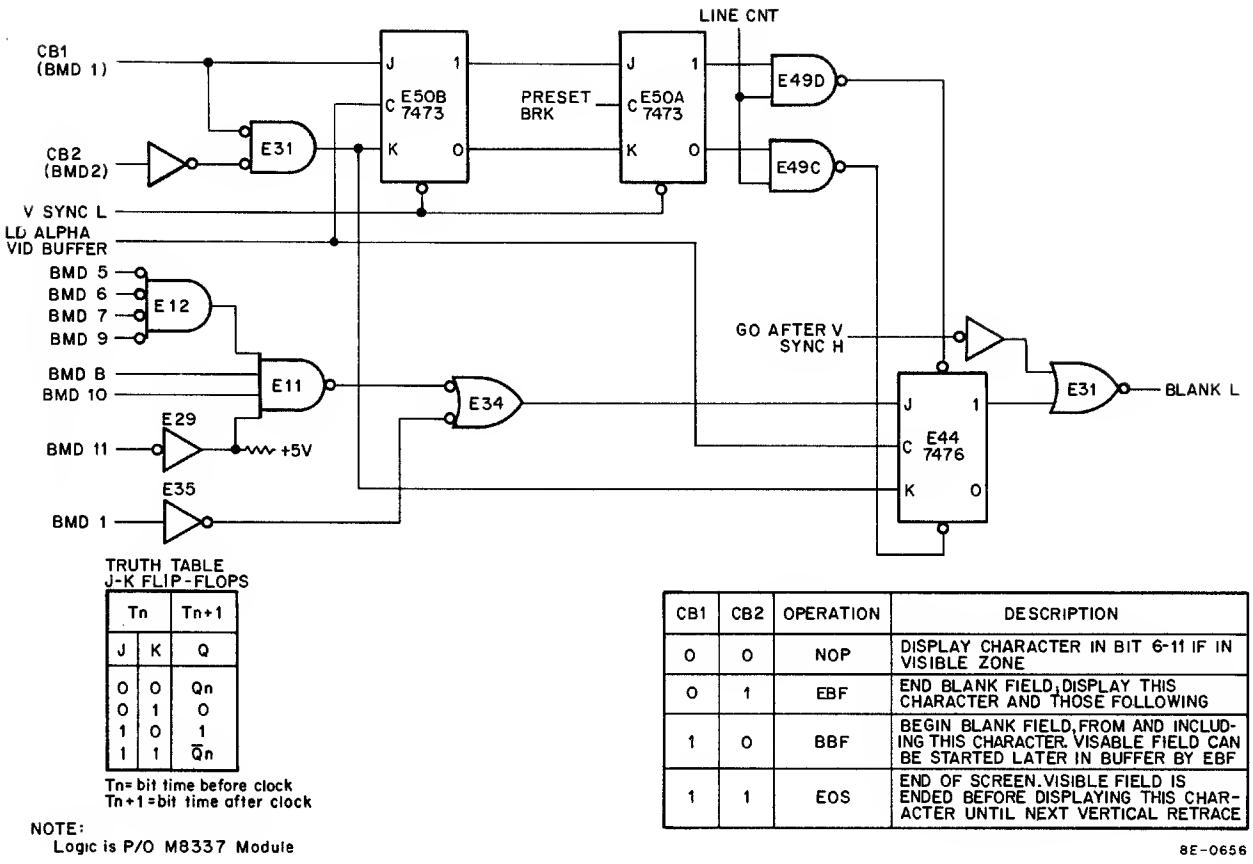


Figure 12-47 12-Bit Data Word Format

When the 7-bit ASCII code for line feed (012) is detected, NAND gate E11 is enabled, putting a high on the J input of flip-flop E44. The LD ALPHA VID BUFFER signal corresponding to the character 012 sets E44, and the rest of the character line is blanked. It would be contradictory to have the EBF control bits set for the line feed character. The K input of E44 should not be a 1 when the LF (012) character is detected.

12.4.2.13 Display Mode Logic – The Display Mode logic is shown in Figure 12-50. These bits determine how the alphanumeric video is displayed, as outlined in the table accompanying the logic.

When the character is to be displayed with normal intensity, the LD ALPHA VID BUFFER signal clears flip-flops E27A and E27B. NAND gate E30B gates the serial output of the alphanumeric Video Buffer Register to NAND gate E39. If the BLANK L signal is not asserted, the asserted ALPHA VID EN signal and the negated GRAPH L signal gate the five data bits to the VIDEO line. If the character is to be displayed at increased intensity, E27A is set, while E27B is cleared. NAND gate E34C is enabled, in addition to E30B. Inverters E29A and E29B have open-collector outputs. For increased intensity, both gates are inactive. Consequently, the VIDEO output is approximately 5V. For normal intensity E29B is active and there is a voltage drop in the neighborhood of 3.5V across the 1 kΩ resistor. Therefore the VIDEO output is approximately 3.5V.



TRUTH TABLE
J-K FLIP-FLOPS

Tn		Tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Q}$n

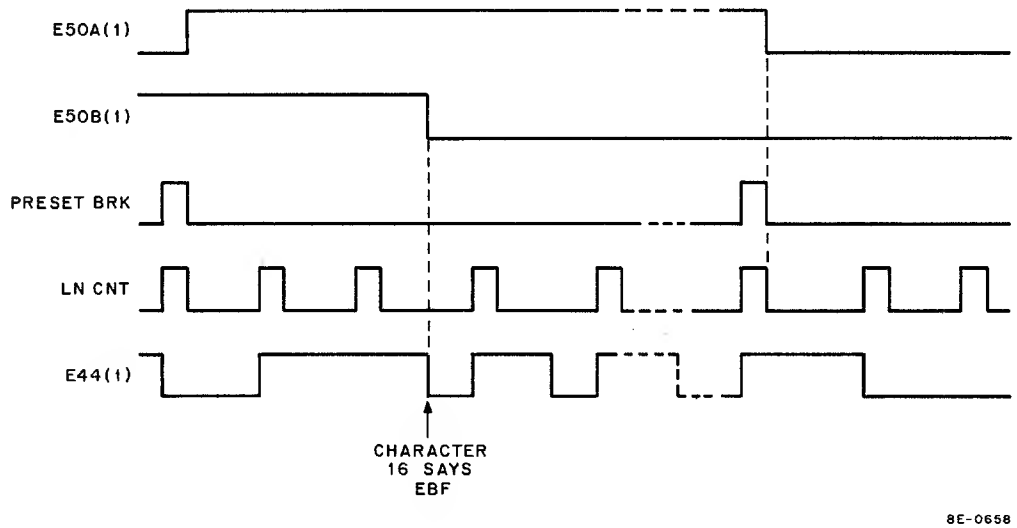
Tn= bit time before clock
Tn+1=bit time after clock

NOTE:
Logic is P/O M8337 Module

CB1	CB2	OPERATION	DESCRIPTION
0	0	NOP	DISPLAY CHARACTER IN BIT 6-11 IF IN VISIBLE ZONE
0	1	EBF	END BLANK FIELD, DISPLAY THIS CHARACTER AND THOSE FOLLOWING
1	0	BBF	BEGIN BLANK FIELD, FROM AND INCLUDING THIS CHARACTER. VISABLE FIELD CAN BE STARTED LATER IN BUFFER BY EBF
1	1	EOS	END OF SCREEN. VISIBLE FIELD IS ENDED BEFORE DISPLAYING THIS CHARACTER UNTIL NEXT VERTICAL RETRACE

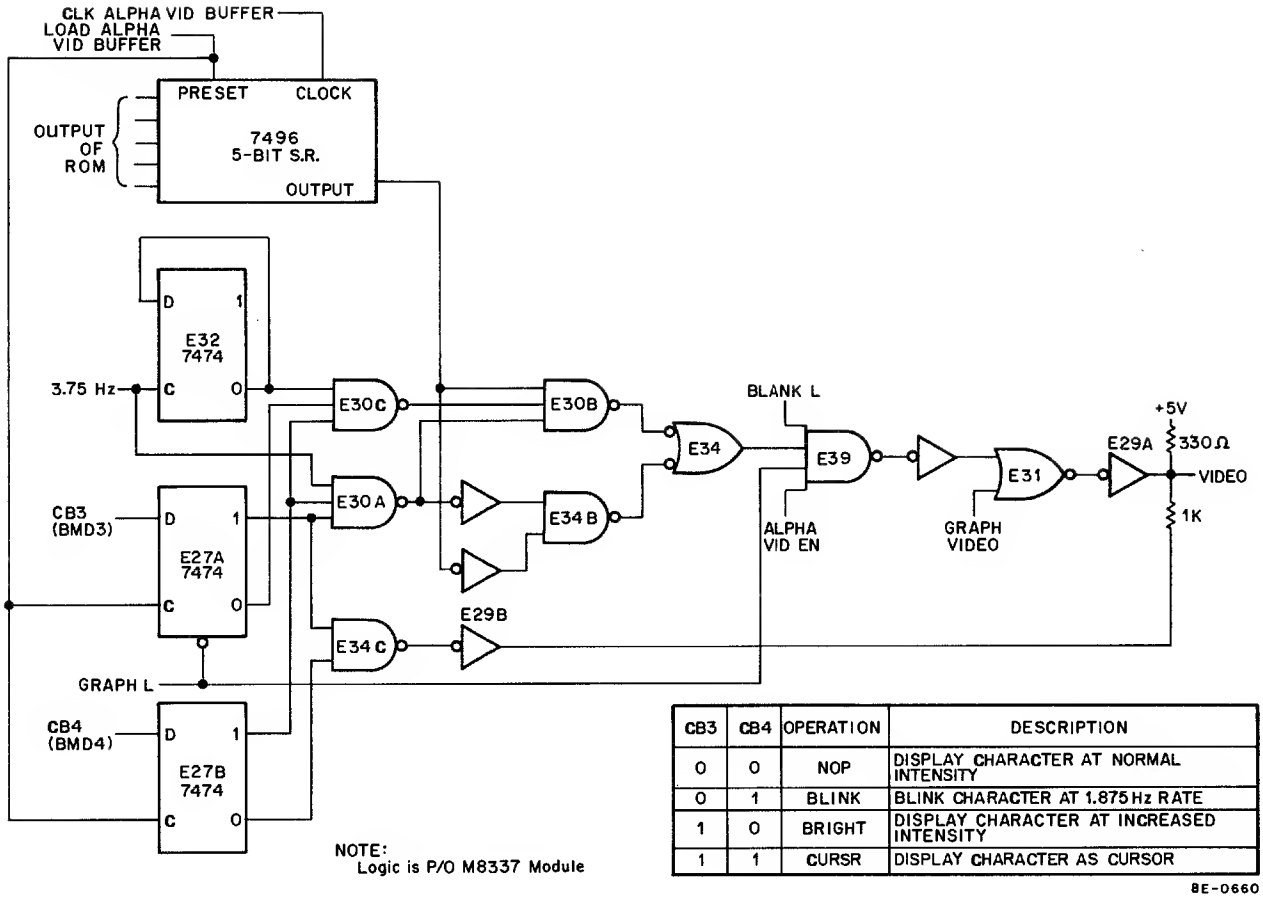
8E-0656

Figure 12-48 Display Control Logic



8E-0658

Figure 12-49 BBF and EBF Timing



CB3	CB4	OPERATION	DESCRIPTION
0	0	NOP	DISPLAY CHARACTER AT NORMAL INTENSITY
0	1	BLINK	BLINK CHARACTER AT 1.875 Hz RATE
1	0	BRIGHT	DISPLAY CHARACTER AT INCREASED INTENSITY
1	1	CURSR	DISPLAY CHARACTER AS CURSOR

Figure 12-50 Display Mode Logic

A character is blinked at a 1.875 Hz rate when CB3 is logic 0 and CB4 is logic 1. The 3.75 Hz signal clocks flip-flop E32. The 0-output of the flip-flop alternately enables and disables NAND gate E30C, resulting in a VIDEO signal that blinks at the desired rate. If CB3 and CB4 are both logic 1, NAND gate E30A is alternately enabled and disabled by the 3.75 Hz signal. NAND gate E30B is enabled by the character bit, while NAND gate E34B is enabled by the character's bit matrix complement. Thus, the character is displayed as a cursor.

12.4.2.14 Maintenance IOT Logic – The Maintenance IOT logic, shown in Figure 12-51, is enabled at TP3 time if the program executes the DPSM instruction to set the MAINT/GO flip-flop (E56). Refer to Paragraph 12.3.4 for a description of the IOT instructions enabled when the VT8-E is in the Maintenance mode. These instructions allow the registers and buffers in the VT8-E to be read into the AC. Data may also be transferred from memory using the DPMB instruction. DPMB sets the BRK RQST flip-flop on the M8337 module and the VT8-E executes one Single Cycle Data Break to transfer data from the memory location determined by the Starting Address Register to the Line Buffer.

12.4.2.15 Display Interrupt and Skip Logic – The Interrupt and Skip logic is shown in Figure 12-52. Interrupts are enabled if bit 11 in the AC is 1 when the DPGO instruction is executed by the program. This sets INT ENA and the VT8-E makes an INT RQST when the Real Time Clock (RTC) flag sets at the start of a vertical retrace and signifies the end of the display frame.

The Skip Bus (SKIP L) is asserted at I/O PAUSE time of the DPCL instruction cycle to cause the program to skip the next sequential instruction. The program may at this time switch modes (Alphanumeric/Graphic) without disturbing the visible presentation.

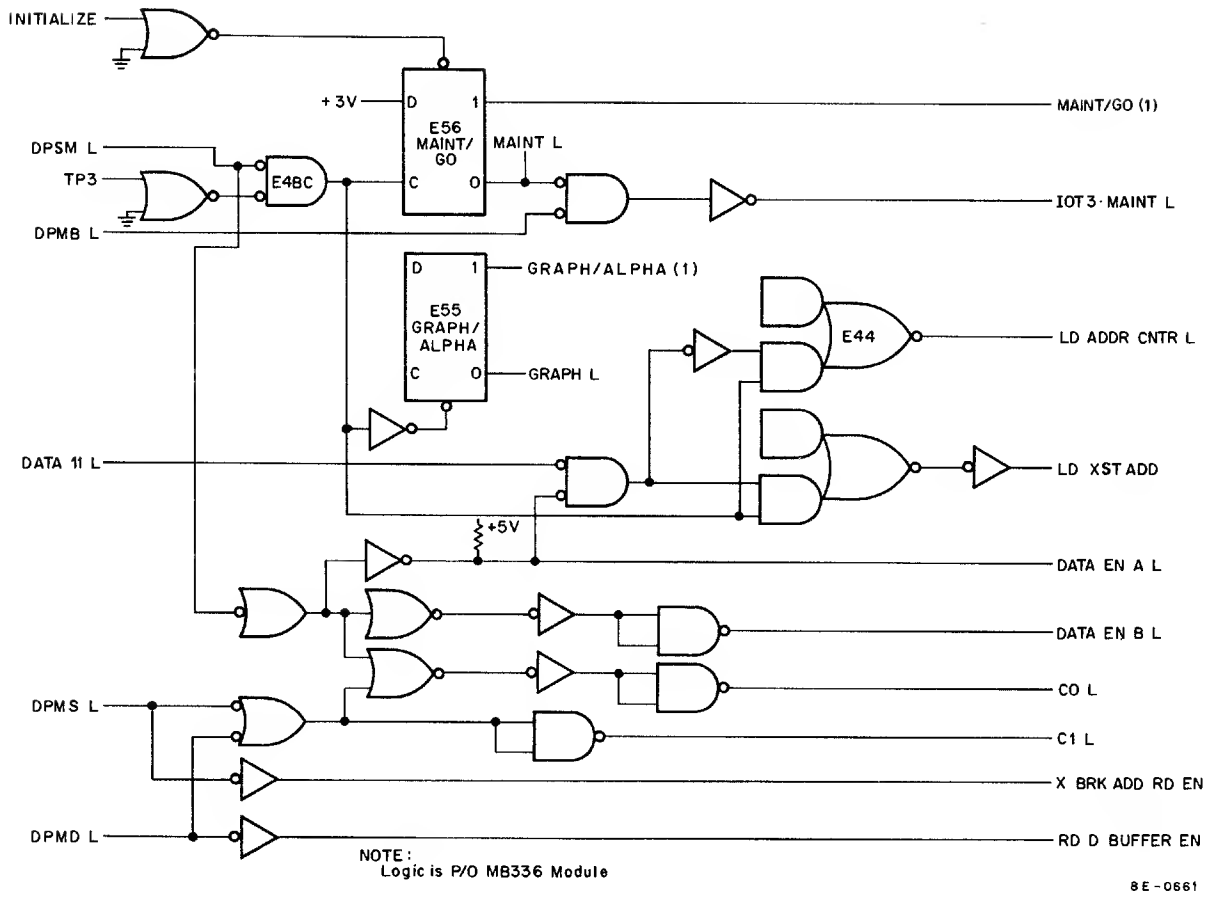


Figure 12-51 Maintenance IOT Logic

12.4.2.16 Bell Logic – The Bell logic is shown in Figure 12-53. BELL EN, a 74123 IC, outputs a 476 ms pulse when the DPBL instruction is executed by the program to enable the 1.56 kHz signal from E11–0 to be applied to the bell. The volume of the tone is adjusted by potentiometer R25 on the M8336 module.

12.5 DISPLAY MONITOR CIRCUITS

12.5.1 Keyboard Logic

The keyboard (Drawing D-CS-3010166-0-0) provides the VT8-E output to the computer. There are 128 ASCII characters or codes that can be generated by the keyboard. A 2-way slide switch is mounted on the Keyboard Logic circuitry board to allow the keyboard to be set for upper/lower case ASCII (128 codes) or lower case ASCII (96 codes) operation. Each key has a variable capacitance that is actuated when the key is pressed, causing an excitation voltage to be applied to one side of the capacitor, generating base drive for the transistor amplifier. A sequential scanning technique is used, employing a MOS integrated circuit that consists of an 8-bit and an 11-bit ring counter (to compose an 8 X 11 matrix), and circuitry to sample the conductance of each transistor amplifier (one per key). As the two (8-bit and 11-bit) registers cycle, the 8-bit counter provides a collector voltage to as many as eleven of the key output amplifiers. Up to eight of the transistor emitters are connected to each of the sensing circuits gated by the 11-bit counter. The two sets of lines that form the 8 X 11 matrix are theoretically capable of sampling up to 88 keys.

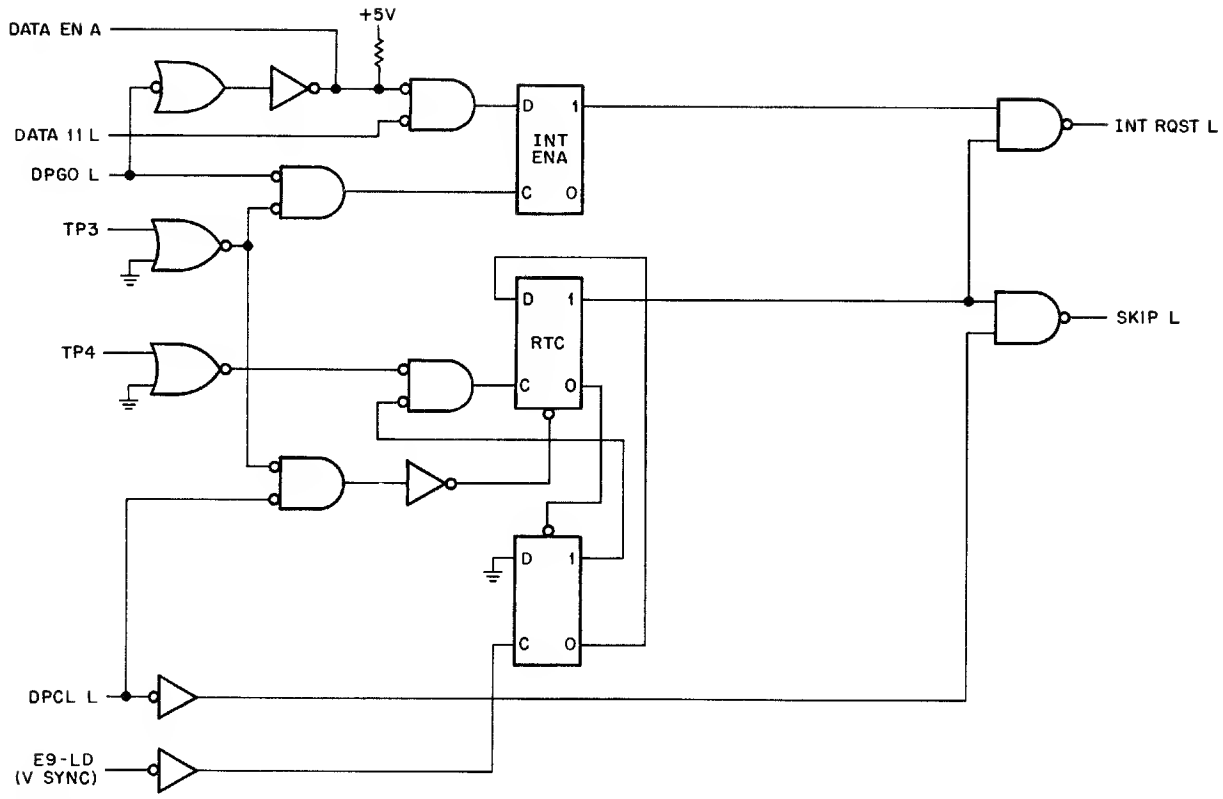


Figure 12-52 Display Interrupt and Skip Logic

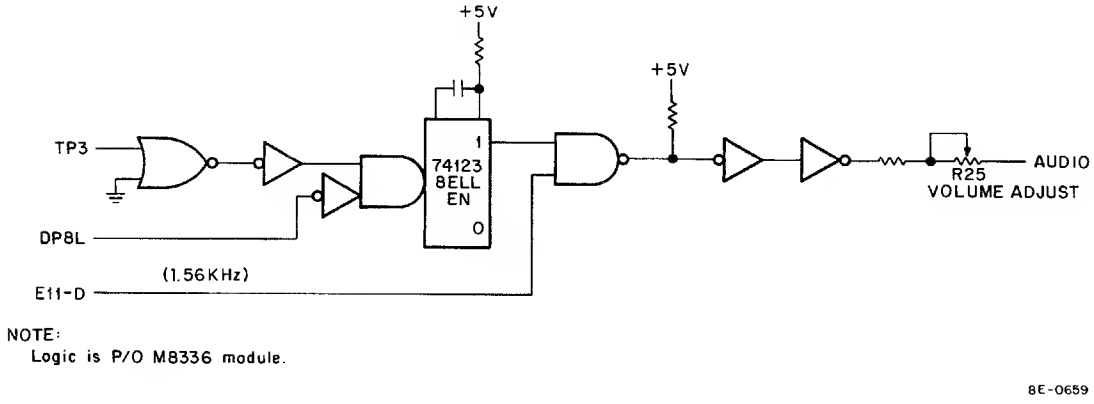


Figure 12-53 Bell Logic

The VT8-E uses the small 8-key keyboard as an extension of the main keyboard to generate cursor control codes to position the cursor and to erase text. The keys used for cursor control or positioning are: cursor up (↑), cursor down (↓), cursor left (←), cursor right (→), and HOME. The erase-to-end-of-line (EOL) and erase-to-end-of-screen (EOS) keys are used in conjunction with the LOCK key. The EOL and EOS codes will not be transmitted unless they are used in conjunction with the LOCK key.

12.5.2 Motorola CRT Display

The following circuit descriptions refer to the detailed circuit schematic of the Motorola CRT Display Module shown in Drawing D-CS-3010326-0-3.

12.5.2.1 Video Amplifier – The Video Amplifier has four stages incorporating devices Q1, Q2, Q3, and Q4. The first stage, Q1, functions as an emitter follower to provide a high impedance input with the 75Ω terminating resistor removed. The high impedance operation permits use of bridging connections to drive a number of monitors from the same signal source. The low output impedance of the first stage permits use of a low resistance contrast control which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the Sync Separator. C3 provides high frequency roll off to limit the collector output to the band-width required to pass synchronization signals. Q2 is a common emitter stage and is directly coupled to Q4. Q3 and Q4 are connected in a cascade configuration. This common emitter/common base connection greatly reduces the effect of Miller capacity compared with a conventional single transistor video output stage. C6 provides a ground for video at the base of Q3, the grounded base transistor of the video output cascade pair.

The video bias control (R10) is used to set the quiescent collector voltage of Q3, C5, C7, C8, and R15 for high frequency compensation. Restoration of dc voltage is accomplished by setting the video bias control so that sync tips, which are negative-going at the collector of Q3, just go into saturation. Variations in video drive result in variations in the base current of Q2 during sync time due to the low load reflected back when Q3 is saturated. The charge on C4 will thus depend on the amplitude of output collector current during sync time. The result is a clamping action which holds sync tips at the same level despite video signal variations. The Video Amplifier output is direct coupled to the control grid of the CRT. R18 is used to isolate Q3 from transients that may occur as a result of CRT arcing.

12.5.2.2 Sync Separator – The Sync Separator uses a single stage, Q5, to recover sync from the composite video signal. A single-stage Sync Separator is adequate due to the high impedance of the following stages. The video input to the Sync Separator is black positive. C11 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak-to-peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R24 sets the clipping level.

12.5.2.3 Phase Detector – The Phase Detector uses two diodes in a key clamp circuit. Two inputs are required to generate the required output, one from the Sync Separator and one from the horizontal deflection system. The required output must be of the correct polarity and amplitude to correct phase differences between the input sync and the horizontal time base. The horizontal collector pulse is integrated into a sawtooth by R45 and C15. During sync time, both diodes in D7 conduct, shorting C15 to ground.

The sawtooth on C15 is thus clamped to ground at sync time. If the horizontal time base is in phase with the sync, the sync pulse will occur when the sawtooth is passing through its ac axis and the net charge on C15 will be 0 (Figure 12-54). If the horizontal time base is lagging the sync, the sawtooth on C15 will be clamped to ground at a point negative from the ac axis. This will result in a positive dc charge on C16 (Figure 12-54). This is the correct polarity to cause the Horizontal Oscillator to speed up to correct the phase lag.

Likewise, if the horizontal time base is leading the sync, the sawtooth on C15 will be clamped at a point positive from its ac axis, resulting in a negative charge on C15. This is the required polarity to slow the horizontal oscillator (Figure 12-54). R33, C17, C16, and R32 comprise the Phase Detector Filter. The bandpass of this filter is chosen to correct the Horizontal Oscillator phase without ringing or hunting.

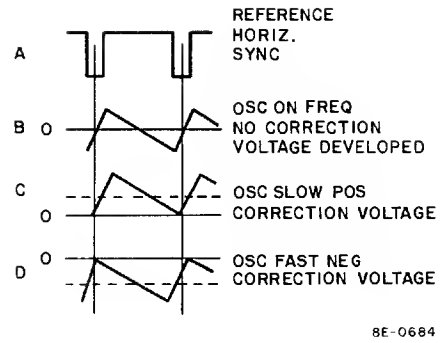


Figure 12-54 CRT Horizontal Oscillator Waveforms

12.5.2.4 Horizontal Oscillator – Q6 is employed in a modified type of Hartley oscillator. The operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the Phase Detector and also by the setting of the horizontal hold control. The horizontal hold range is set by adjusting the core of L1.

12.5.2.5 Pulse Shaper and Horizontal Drive – Q7 is used as a buffer stage between the Horizontal Oscillator and the Horizontal Driver. It provides isolation for the Horizontal Oscillator as well as a low impedance driver for the Horizontal Driver. R38 and C20 form a time constant which shapes the oscillator output to the required duty cycle (approximately 50 percent), to drive the Horizontal Output circuitry. The Horizontal Driver stage, Q8, operates as a switch to drive the Horizontal Output transistor through T1. Because of the low impedance drive and fast switching times furnished by Q7, very little power is dissipated in Q8. C21 and R42 provide damping to suppress ringing of the primary to T1 when Q8 goes into cutoff.

12.5.2.6 Horizontal Output – The secondary of T1 provides the required low drive impedance for Q9. R44 and C24 form a time constant for fast turn-off of the base of Q9. Q9 operates as a switch that, once each horizontal period, connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of T2. The required sawtooth of the deflection current through the horizontal yoke is formed by the L-R time constant of the yoke and output transformer primary. The Horizontal Retrace pulse charges C27 through D2 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q9, should they occur, are limited to the voltage on C27, since D2 will conduct if the collector voltage exceeds this value.

The damper diode, D1, conducts during the period between retrace and turn-on of Q9. C28 is the retrace tuning capacitor. C29 blocks dc from the deflection yoke. L3 is a magnetically-biased linearity coil that shapes deflection current for optimum trace linearity. L4 is a series width control. C31 and R49, C42 and R68 are damping network components for the linearity and width controls. C43D is charged through D5 developing the video supply voltage.

12.5.2.7 Vertical Oscillator Driver and Output – Sync from the collector of Q5 is integrated by R26 and C35. Q10 and Q11 are connected as a regenerative switch. The series combination of C37 and C38 charges through R58 and D3 until Q10 turns on. This occurs when the emitter of Q10 exceeds its base voltage and causes current to flow into the base of Q11, turning that device on. When Q10 and Q11 conduct, C37 and C38 are discharged to nearly 0. Q10 and Q11 then shut off and the cycle repeats. The setting of the vertical hold control determines the repetition rate of the charge and discharge of C37 and C38. The waveform generated is a positive-going ramp or sawtooth with a fast retrace to 0. D3 provides a small incremental voltage above ground to overcome the forward base-emitter drop of the two following stages. Q12 is an emitter follower used to transform the high impedance drive sawtooth to a low impedance drive for Q13.

T3 matches the collector of Q13 to the vertical yoke. When Q13 is cut off during Vertical Retrace, a high voltage pulse is developed across the primary of T3. To limit this pulse to a safe value a varistor, R81, is connected across

the primary. R66 and C41 provide damping to shape the collector pulse so it may be used for retrace blanking. Since the primary impedance of T3 decreases with current, the degree to which the primary shunts the reflected load impedance varies with collector current. This would result in severe vertical non-linearity unless some compensation is employed.

Resistors R60 and R59 couple the emitter voltage of Q13 to the junction of C37 and C38. Since this path is resistive, the waveform coupled back will be integrated into a parabola by C38. This results in a pre-distortion of the drive sawtooth as shown in Figure 12-55. This is done to compensate for the non-linear charging of C37 and C38 and the changing impedance of the primary of T3. An additional feedback path through R62 and C40 serves to optimize the drive waveshape for best linearity.

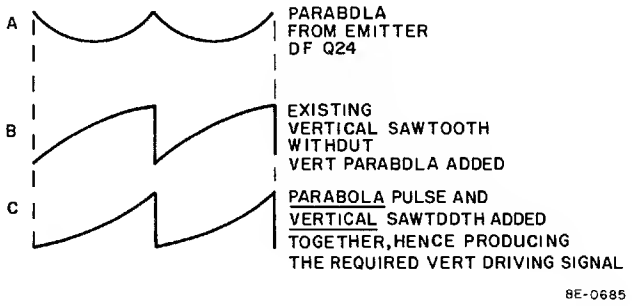


Figure 12-55 CRT Vertical Oscillator Waveforms

12.5.2.8 Retrace Blanking – Both Vertical and Horizontal Retrace blanking are provided by positive pulses applied to the CRT cathode. The collector pulse from the Horizontal Output transistor is placed across R23 through R46. The vertical collector voltage is differentiated by C30 to remove the sawtooth portion of the waveform. The remaining pulse appears across R23. The mixed vertical and horizontal pulses on R23 are coupled to the CRT cathode by C10.

12.5.2.9 Power Supply – The regulated power supply uses a series pass circuit. Q16 is the series pass transistor, Q14 is the driver, and Q15 is the reference amplifier. The output voltage of the regulator appears at the emitter of Q16 and is fed into a voltage divider consisting of R71, R74, and R73. The voltage appearing on the arm of potentiometer R74 is used as an error input to Q15. R74 is thus used as the output voltage adjustment.

Zener diode D13 establishes a reference voltage at the emitter of Q15. R72 establishes the minimum bias current for D13 to ensure proper Zener operation.

The voltage at the arm of R74 is compared with the reference voltage at D13 by Q15. If the voltage at the base of Q15 increases due to an increase in input voltage to the power supply for example, Q15 conducts more current. This decreases the current available to the base of Q14, so Q14 and Q16 conduct less current, resulting in less voltage at the emitter of Q16. In this manner, input voltage changes are reduced by the overall gain of the regulator, which is quite high. R79 reduces the power dissipation in Q16 by carrying some of the supply current. This does not impair regulation over the operating range of the power supply due to the large amount of gain available.

SECTION 5 MAINTENANCE

12.6 INTRODUCTION

VT8-E maintenance theory is directed to the module replacement level. The maintenance effort is divided into two basic categories: preventive maintenance and corrective maintenance.

Preventive maintenance consists of routine periodic checks such as visual inspections, standard maintenance procedures that involve cleaning and lubricating, and diagnostic tests that expose possible weakening conditions to allow corrective action to be taken, eliminating the causative factor(s) of possible failures.

Corrective maintenance consists of isolating the fault or problem and making necessary adjustments and/or replacements when a malfunction occurs. This involves the use of diagnostic routines prepared on paper tape and designed to test the functional units of the system. The procedures and techniques of periodic checking aid in fault isolation. Power requirements can be checked through the checkout procedures for power requirements contained in Paragraph 12.2.2.

12.6.1 Equipment Required

Maintenance procedures for the VT8-E Video Display and Control require the standard equipment (or equivalent), standard hand tools, and test probes listed in Table 12-10.

Table 12-10
Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 620
Oscilloscope	Tektronix	Type 453
X10 Probe	Tektronix	P6010
Recessed Tip	Tektronix	013-0090-00
Diagnostic Self-Test Routines		

12.6.2 Diagnostic Programming

The diagnostic routines, supplied as paper tapes, are used to test the various VT8-E functions and modules. A complete description with instructions is provided with each tape.

12.6.3 Preventive Maintenance

Preventive maintenance consists of tasks performed periodically; its major purpose is to prevent failures caused by minor damage or progressive deterioration due to aging. A preventive maintenance log book should be established and necessary entries made according to a regular schedule. This data, compiled over an extended period of time, can be very useful in anticipating possible component failures resulting in module replacement on a projected module or component reliability basis.

Preventive maintenance tasks consist of mechanical and electrical checks. All maintenance schedules should be established according to the environmental conditions at the particular installation site. Mechanical checks should be performed as often as required to allow the fan and air filter to function efficiently. All other preventive maintenance tasks should be performed on a regular schedule determined by reliability requirements. A recommended schedule is every 600 operating hours or every four months, whichever occurs first.

12.6.3.1 Mechanical Checks – Use the following procedure to perform a mechanical check on the equipment.

Step	Procedure
1	Unplug the VT8-E main power and remove the cover.
2	Clean the exterior with a clean cloth moistened in a mild detergent. Only a very soft cloth should be used to avoid scratching the protective screen used on the face of the CRT.
3	Clean the interior using a vacuum cleaner and ensure that the cabinet air exhaust vents are thoroughly clean and unobstructed to promote adequate cooling. Should the vents become obstructed, premature component failure may occur due to an increase in the VT8-E internal temperature.
4	Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechancial security: jacks, connectors, keyboard, etc. Tighten or replace as required.

12.6.4 Troubleshooting

12.6.4.1 System Troubleshooting – Begin troubleshooting by repeating the operation in which the malfunction was initially observed, using the same program or function. Thoroughly check the program for proper settings and determine if the fault is definitely located in the VT8-E.

If the fault is isolated to the VT8-E, but cannot be immediately localized to a specific logic function, an effort should be made to further isolate the fault to one of the VT8-E modules, e.g., keyboard, M8335 module, CRT module, etc. Some helpful aids during functional analysis are the VT8-E engineering drawings, circuit schematics, timing diagrams, and the applicable VT8-E diagnostic programs.

12.6.4.2 Module Troubleshooting – Once the fault has been isolated to a specific module, carefully remove the suspected module. Inspect the receptacle for wear or damaged contacts. When the operability of the module is verified, repair the faulty module or replace it with a module known to be operating properly and run the last diagnostic program. If the system performs properly, return the system to an operating status and log an entry to record all pertinent data concerning the fault or malfunction. When the individual defective part(s) within a module is located and repaired or replaced, the module should be verified by a validation test.

12.6.4.3 VT8-E Assembly/Disassembly – The following procedures are provided for removal, replacement, and installation of the various VT8-E modular components. Special and cautionary notes contained within the procedures afford special attention and should be adhered to. Only procedures for the removal of the VT8-E modular components are provided; for installation, the procedures should be performed in their reverse order.

12.6.4.3.1 VT8-E Module Boards – The M8335, M8336, or M8337 module boards should be inserted straight into the OMNIBUS, never at an angle. When inserting a module board be certain it is fully seated in the OMNIBUS.

12.6.4.3.2 Cover Removal – The VT8-E cover is secured with four Phillips-head screws. Screw locations are center-front, center-rear, and midway on the two sides. The screws are inserted up through the lower casting and into four cover-retaining brackets. To remove the cover, remove the four retaining screws and lift the cover off.

NOTE

When the cover is removed, the 3-position interlock switch on the left-hand side (viewing from the front) will go from the fully depressed position (ON) to the middle position (OFF) and must be pulled up to the third position (ON).

To install the cover, place the cover back on the lower casing, insert and tighten the four Phillips-head retaining screws. The interlock switch should be in the fully depressed (ON) position.

12.6.4.3.3 VT8-E Keyboards Removal – The VT8-E contains two keyboards, a large teletypewriter-type keyboard, and a small 8-key cursor control keyboard. The small keyboard is secured by four Phillips-head screws that are inserted down through the four corners of the mounting board into the mounting bracket. The large keyboard is secured by four Phillips-head screws that are inserted down through the keyboard mounting bracket. These four screws should not be confused with the smaller and brighter Phillips-head screws that secure the keyboard to the keyboard logic board. The smaller, brighter screws should not be removed.

Use the following procedure to remove the small keyboard:

Step	Procedure
1	Disconnect the ribbon cable from the small keyboard input connector.
2	Remove the four Phillips-head retaining screws from the four corners of the small keyboard mounting board.
3	Slide the keyboard to the left and lift it out.

Use the following procedure to remove the large keyboard:

Step	Procedure
1	Disconnect the 44-pin Berg connector from the keyboard output connector.
2	Remove the four, larger keyboard Phillips-head retaining screws from the keyboard mounting bracket and remove the keyboard

12.6.4.3.4 CRT Removal – The CRT is secured to the VT8-E lower casting with four Phillips-head screws that are inserted through the bottom of the VT8-E and into the bottom four corners of the CRT chassis. Use the following procedure to remove the CRT:

CAUTION

Protective goggles and heavy gloves should be worn when removing and/or carrying the CRT. Never grasp the CRT by the neck, nor chip or scratch any part of the tube.

Step	Procedure
1	Press the interlock switch down to ensure main power is off.
2	Viewing the VT8-E from the front, locate (15-pin and 12-pin) Mate-N-Lok connectors P1 and P2 on the lower right-hand side of the CRT chassis and disconnect both connectors.
3	Locate and remove the four Phillips-head retaining screws on the bottom of the VT8-E, used to secure the CRT chassis to the lower casting.

NOTE

Upon removal, the CRT should be placed face-down on a soft clean cloth or pad. Under no circumstances should the CRT be grasped by the neck

4	Lift the CRT out of the lower casing.

APPENDIX A
ROM PATTERN TABLES

Table A-1
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	24	030	0000
1	001	0111	25	031	1111
2	002	1000	26	032	1000
3	003	1011	27	033	1000
4	004	1010	28	034	1111
5	005	1011	29	035	1000
6	006	1000	30	036	1000
7	007	0111	31	037	1000
8	010	0000	32	040	0000
9	011	1111	33	041	1000
10	012	1000	34	042	1000
11	013	1000	35	043	1000
12	014	1111	36	044	1111
13	015	1000	37	045	1000
14	016	1000	38	046	1000
15	017	1111	39	047	1000
16	020	0000	40	050	0000
17	021	1110	41	051	0011
18	022	1001	42	052	0001
19	023	1000	43	053	0001
20	024	1000	44	054	0001
21	025	1000	45	055	1001
22	026	1001	46	056	1001
23	027	1110	47	057	0110

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
48	060	0000	84	124	0010
49	061	1000	85	125	0010
50	062	1000	86	126	0010
51	063	1000	87	127	0010
52	064	1000	88	130	0000
53	065	1000	89	131	1000
54	066	1000	90	132	1000
55	067	1111	91	133	1000
56	070	0000	92	134	1000
57	071	1000	93	135	1000
58	072	1000	94	136	0101
59	073	1100	95	137	0010
60	074	1010	96	140	0000
61	075	1001	97	141	1000
62	076	1000	98	142	1000
63	077	1000	99	143	0101
64	100	0000	100	144	0010
65	101	1111	101	145	0101
66	102	1000	102	146	1000
67	103	1000	103	147	1000
68	104	1111	104	150	0000
69	105	1000	105	151	1111
70	106	1000	106	152	0000
71	107	1000	107	153	0001
72	110	0000	108	154	0010
73	111	1111	109	155	0100
74	112	1000	110	156	1000
75	113	1000	111	157	1111
76	114	1111	112	160	0000
77	115	1001	113	161	0000
78	116	1000	114	162	1000
79	117	1000	115	163	0100
80	120	0000	116	164	0010
81	121	1111	117	165	0001
82	122	0010	118	166	0000
83	123	0010	119	167	0000

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
120	170	0000	156	234	0100
121	171	0111	157	235	1010
122	172	1000	158	236	1001
123	173	0000	159	237	0110
124	174	0000	160	240	0000
125	175	0000	161	241	0001
126	176	0000	162	242	0010
127	177	0000	163	243	0100
128	200	0000	164	244	0100
129	201	0000	165	245	0100
130	202	0000	166	246	0010
131	203	0000	167	247	0001
132	204	0000	168	250	0000
133	205	0000	169	251	0010
134	206	0000	170	252	1010
135	207	0000	171	253	0111
136	210	0000	172	254	1101
137	211	0101	173	255	0111
138	212	0101	174	256	1010
139	213	0101	175	257	0010
140	214	0000	176	260	0000
141	215	0000	177	261	0000
142	216	0000	178	262	0000
143	217	0000	179	263	0000
144	220	0000	180	264	0000
145	221	0010	181	265	0010
146	222	0111	182	266	0010
147	223	1000	183	267	0100
148	224	0111	184	270	0000
149	225	0000	185	271	0000
150	226	1111	186	272	0000
151	227	0010	187	273	0000
152	230	0000	188	274	0000
153	231	0100	189	275	0000
154	232	1010	190	276	0000
155	233	1010	191	277	0010

Table A-1 (Cont)
ROM Pattern Table
(EVEN ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
192	300	0000	224	340	0000
193	301	0111	225	341	0111
194	302	1000	226	342	1000
195	303	1001	227	343	1000
196	304	1010	228	344	0111
197	305	1100	229	345	1000
198	306	1000	230	346	1000
199	307	0111	231	347	0111
200	310	0000	232	350	0000
201	311	0111	233	351	0000
202	312	1000	234	352	0000
203	313	0000	235	353	0010
204	314	0011	236	354	0000
205	315	0100	237	355	0010
206	316	1000	238	356	0000
207	317	1111	239	357	0000
208	320	0000	240	360	0000
209	321	0001	241	361	0001
210	322	0011	242	362	0010
211	323	0101	243	363	0100
212	324	1001	244	364	1000
213	325	1111	245	365	0100
214	326	0001	246	366	0010
215	327	0001	247	367	0001
216	330	0000	248	370	0000
217	331	0011	249	371	0100
218	332	0100	250	372	0010
219	333	1000	251	373	0001
220	334	1111	252	374	0000
221	335	1000	253	375	0001
222	336	1000	254	376	0010
223	337	0111	255	377	0100

Table A-2
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	36	044	0010
1	001	0010	37	045	0010
2	002	0101	38	046	0010
3	003	1000	39	047	0111
4	004	1000	40	050	0000
5	005	1111	41	051	1000
6	006	1000	42	052	1001
7	007	1000	43	053	1010
8	010	0000	44	054	1100
9	011	0111	45	055	1010
10	012	1000	46	056	1001
11	013	1000	47	057	1000
12	014	1000	48	060	0000
13	015	1000	49	061	1000
14	016	1000	50	062	1101
15	017	0111	51	063	1010
16	020	0000	52	064	1010
17	021	1111	53	065	1000
18	022	1000	54	066	1000
19	023	1000	55	067	1000
20	024	1111	56	070	0000
21	025	1000	57	071	0111
22	026	1000	58	072	1000
23	027	1111	59	073	1000
24	030	0000	60	074	1000
25	031	0111	61	075	1000
26	032	1000	62	076	1000
27	033	1000	63	077	0111
28	034	1000	64	100	0000
29	035	1011	65	101	0111
30	036	1000	66	102	1000
31	037	0111	67	103	1000
32	040	0000	68	104	1000
33	041	0111	69	105	1010
34	042	0010	70	106	1001
35	043	0010	71	107	0110

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
72	110	0000	108	154	1100
73	111	0111	109	155	1100
74	112	1000	110	156	1100
75	113	1000	111	157	1111
76	114	0111	112	160	0000
77	115	0000	113	161	1111
78	116	1000	114	162	0001
79	117	0111	115	163	0001
80	120	0000	116	164	0001
81	121	1000	117	165	0001
82	122	1000	118	166	0001
83	123	1000	119	167	1111
84	124	1000	120	170	0000
85	125	1000	121	171	0000
86	126	1000	122	172	0000
87	127	0111	123	173	0000
88	130	0000	124	174	0000
89	131	1000	125	175	0000
90	132	1000	126	176	0000
91	133	1000	127	177	1111
92	134	1010	128	200	0000
93	135	1010	129	201	0010
94	136	1101	130	202	0010
95	137	1000	131	203	0010
96	140	0000	132	204	0010
97	141	1000	133	205	0010
98	142	1000	134	206	0000
99	143	0101	135	207	0010
100	144	0010	136	210	0000
101	145	0010	137	211	0101
102	146	0010	138	212	0101
103	147	0010	139	213	1111
104	150	0000	140	214	0101
105	151	1111	141	215	1111
106	152	1100	142	216	0101
107	153	1100	143	217	0101

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
144	220	0000	180	264	1111
145	221	1100	181	265	0000
146	222	1100	182	266	0000
147	223	0001	183	267	0000
148	224	0010	184	270	0000
149	225	0100	185	271	0000
150	226	1001	186	272	0000
151	227	0001	187	273	0001
152	230	0000	188	274	0010
153	231	0010	189	275	0100
154	232	0010	190	276	1000
155	233	0010	191	277	0000
156	234	0000	192	300	0000
157	235	0000	193	301	0010
158	236	0000	194	302	0110
159	237	0000	195	303	0010
160	240	0000	196	304	0010
161	241	0100	197	305	0010
162	242	0010	198	306	0010
163	243	0001	199	307	0111
164	244	0001	200	310	0000
165	245	0001	201	311	1111
166	246	0010	202	312	0000
167	247	0100	203	313	0001
168	250	0000	204	314	0011
169	251	0000	205	315	0000
170	252	0010	206	316	1000
171	253	0010	207	317	0111
172	254	1111	208	320	0000
173	255	0010	209	321	1111
174	256	0010	210	322	1000
175	257	0000	211	323	1111
176	260	0000	212	324	0000
177	261	0000	213	325	0000
178	262	0000	214	326	1000
179	263	0000	215	327	0111

Table A-2 (Cont)
ROM Pattern Table
(ODD ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
216	330	0000	236	354	0000
217	331	1111	237	355	0010
218	332	0000	238	356	0010
219	333	0001	239	357	0100
220	334	0010	240	360	0000
221	335	0100	241	361	0000
222	336	0100	242	362	0000
223	337	0100	243	363	1111
224	340	0000	244	364	0000
225	341	0111	245	365	1111
226	342	1000	246	366	0000
227	343	1000	247	367	0000
228	344	0111	248	370	0000
229	345	0000	249	371	0111
230	346	0001	250	372	1000
231	347	1110	251	373	0001
232	350	0000	252	374	0010
233	351	0000	253	375	0010
234	352	0000	254	376	0000
235	353	0010	255	377	0010

Table A-3
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
0	000	0000	36	044	0010
1	001	0000	37	045	0010
2	002	0010	38	046	0010
3	003	0011	39	047	0010
4	004	0011	40	050	0000
5	005	0011	41	051	0011
6	006	0001	42	052	0000
7	007	0011	43	053	0000
8	010	0000	44	054	0000
9	011	0000	45	055	0000
10	012	0011	46	056	0000
11	013	0010	47	057	0001
12	014	0000	48	060	0000
13	015	0010	49	061	0001
14	016	0011	50	062	0001
15	017	0000	51	063	0001
16	020	0000	52	064	0001
17	021	0001	53	065	0001
18	022	0000	54	066	0001
19	023	0010	55	067	0011
20	024	0010	56	070	0000
21	025	0010	57	071	0010
22	026	0000	58	072	0011
23	027	0001	59	073	0011
24	030	0000	60	074	0011
25	031	0010	61	075	0011
26	032	0001	62	076	0011
27	033	0000	63	077	0010
28	034	0000	64	100	0000
29	035	0001	65	101	0000
30	036	0001	66	102	0011
31	037	0000	67	103	0011
32	040	0000	68	104	0001
33	041	0010	69	105	0001
34	042	0010	70	106	0000
35	043	0010	71	107	0001

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
72	110	0000	108	154	0000
73	111	0000	109	155	0000
74	112	0011	110	156	0000
75	113	0010	111	157	0011
76	114	0000	112	160	0000
77	115	0001	113	161	0001
78	116	0011	114	162	0001
79	117	0010	115	163	0001
80	120	0000	116	164	0001
81	121	0011	117	165	0001
82	122	0001	118	166	0011
83	123	0001	119	167	0001
84	124	0001	120	170	0000
85	125	0001	121	171	0000
86	126	0001	122	172	0010
87	127	0000	123	173	0000
88	130	0000	124	174	0000
89	131	0011	125	175	0000
90	132	0011	126	176	0000
91	133	0011	127	177	0001
92	134	0011	128	200	0000
93	135	0011	129	201	0000
94	136	0001	130	202	0000
95	137	0001	131	203	0000
96	140	0000	132	204	0000
97	141	0011	133	205	0000
98	142	0011	134	206	0000
99	143	0000	135	207	0000
100	144	0000	136	210	0000
101	145	0000	137	211	0000
102	146	0010	138	212	0000
103	147	0010	139	213	0001
104	150	0000	140	214	0000
105	151	0011	141	215	0001
106	152	0010	142	216	0000
107	153	0000	143	217	0000

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
180	264	0001	144	220	0000
181	265	0000	145	221	0000
182	266	0000	146	222	0011
183	267	0000	147	223	0000
184	270	0000	148	224	0000
185	271	0000	149	225	0010
186	272	0001	150	226	0001
187	273	0000	151	227	0001
188	274	0000	152	230	0000
189	275	0000	153	231	0000
190	276	0000	154	232	0000
191	277	0000	155	233	0000
192	300	0000	156	234	0000
193	301	0000	157	235	0010
194	302	0010	158	236	0000
195	303	0010	159	237	0010
196	304	0010	160	240	0000
197	305	0010	161	241	0000
198	306	0010	162	242	0000
199	307	0000	163	243	0000
200	310	0000	164	244	0000
201	311	0001	165	245	0000
202	312	0011	166	246	0000
203	313	0010	167	247	0000
204	314	0000	168	250	0000
205	315	0001	169	251	0000
206	316	0001	170	252	0010
207	317	0010	171	253	0000
208	320	0000	172	254	0011
209	321	0001	173	255	0000
210	322	0000	174	256	0010
211	323	0000	175	257	0000
212	324	0001	176	260	0000
213	325	0011	177	261	0000
214	326	0001	178	262	0000
215	327	0000	179	263	0000

Table A-3 (Cont)
ROM Pattern Table
(XTRA ROM)

Decimal Location	Octal Location	Binary Data	Decimal Location	Octal Location	Binary Data
216	330	0000	236	354	0000
217	331	0011	237	355	0000
218	332	0001	238	356	0000
219	333	0000	239	357	0000
220	334	0000	240	360	0000
221	335	0010	241	361	0000
222	336	0010	242	362	0000
223	337	0000	243	363	0001
224	340	0000	244	364	0000
225	341	0000	245	365	0001
226	342	0011	246	366	0000
227	343	0011	247	367	0000
228	344	0001	248	370	0000
229	345	0011	249	371	0000
230	346	0010	250	372	0001
231	347	0000	251	373	0000
232	350	0000	252	374	0010
233	351	0000	253	375	0000
234	352	0000	254	376	0000
235	353	0000	255	377	0000

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VT8-E High-Speed Video Display Terminal
And Control Option
DEC-8E-HR3B-D-VT8-E

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