DEC-8I-H2CA-D

PP8/I

HIGH-SPEED PAPER-TAPE PUNCH OPTION FUNCTIONAL DESCRIPTION

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PP8/I
HIGH-SPEED
PAPER-TAPE PUNCH

INTRODUCTION

The PP8/I Paper-Tape Punch (Figure 1) consists of a 50-character-per-second, Royal-McBee Model 500 electro-mechanical punch, and its associated control logic elements. Eight-bit parallel data is accepted from the PDP-8/I, stored in a buffer register, and punched in one-inch-wide paper tape.

The control logic of the PP8/I is contained on one, double-height, integrated-circuit, module located in the central processor mainframe. Figure 2 shows the functional relationship between the PDP-8/I, the PP8/I control logic, and the paper-tape punch.

The following paragraphs describe the operation of the control logic portion of the tape punch as it relates to the PDP-8/I and the punch mechanism. Maintenance procedures and a description of the punch mechanism and its operation are provided in the Royal-McBee Model 500 Maintenance Manual.

LOGIC DESCRIPTION

The PP8/I Paper-Tape Punch punches the data received from the PDP-8/I accumulator into the paper tape. The 12-bit instructions from the PDP-8/I are decoded to generate control pulses that operate the punch mechanism. The decoding is performed as follows:

When an IOT (Input/Output Transfer) is initiated, the PDP-8/I memory-buffer bits 0 through 2 contain operation code 6_8 and memory-buffer bits 3 through 8 contain a 6-bit device code; for the PP8/I, this device code is 02_8.

Memory-buffer bits 9, 10, 11 of the instruction generate PDP-8/I IOP pulses. These pulses (IOP1, IOP2, IOP4), when gated by device code 02_8, are sent to the punch control logic to generate pulses that control the PP8/I functions.

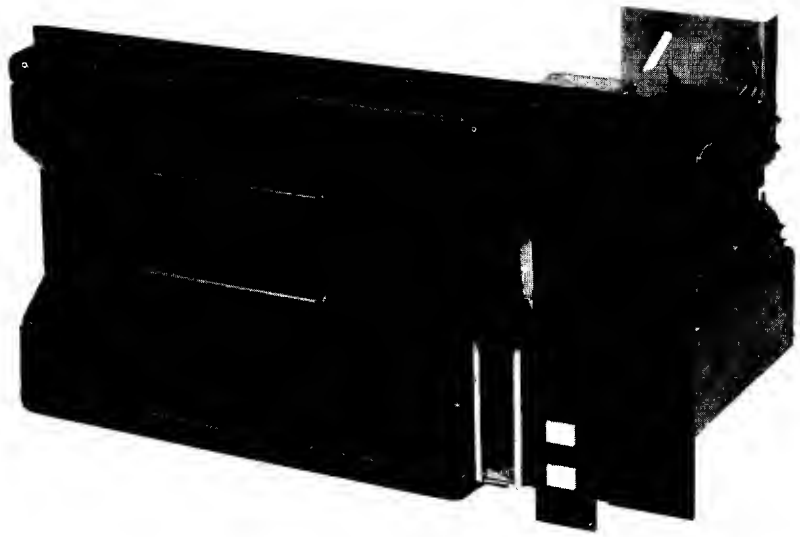


Figure 1 PP8/I High-Speed Paper-Tape Punch

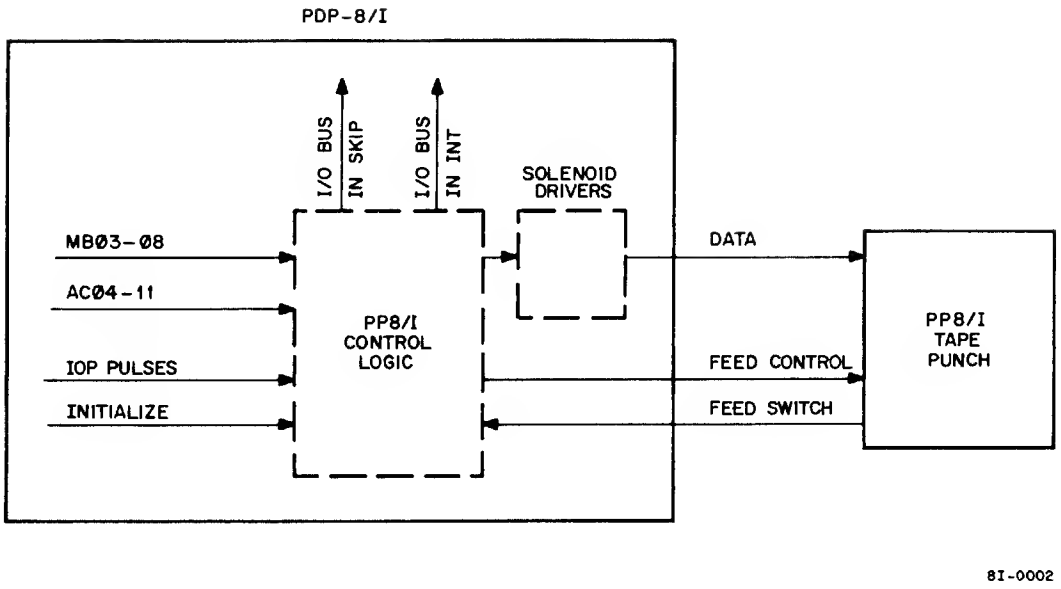


Figure 2 Block Diagram PP8/I Paper-Tape Punch

When the PDP-8/I is turned on or the START key is pressed, the PDP-8/I INITIALIZE level is generated and applied to the control logic (Drawing D-BS-PP8/I-0-1). INITIALIZE clears the punch buffer flip-flops PB0 through PB7, the PUN ACTIVE flip-flop, and the PUN FLAG flip-flop by applying a direct clear input level to each flip-flop.

In the PP8/I Punch, a single, continuously-rotating shaft drives both the punch and tape-feed mechanical operations. Primary power, applied to the punch mechanism, activates a drive motor that operates continuously as long as power is applied. A reluctance pickup senses the rotation of the shaft and sends SYNC PUN pulses to the control logic. These pulses synchronize the timing between the computer and the rotating shaft. First, the shaft causes the punches to be driven through the paper tape; then it causes the tape to be fed to the next position for punching the next character.

The punch cycle is initiated by activating the feed-hole solenoid driver. This is accomplished either by executing a 6024 instruction or by pressing the manual FEED switch (FEED switch with Royal-McBee only) on the punch panel. In either case, the feed-hole and data are punched and the tape is advanced one position regardless of the data stored in the punch buffer register. The data is punched according to the status of the punch register. The PB0 through PB7 flip-flops that are set, enable the solenoid drivers which then activate the respective hole punches.

Program Instructions

Table 1 describes the program instructions that control the operation of the PP8/I Tape Punch.

The PP8/I instructions and logic implementation are described below.

PCF(6022)

This instruction, used at the start of the program, clears the PUN FLAG flip-flop, the

Table 1
PP8/I Instructions

Mnemonic	Octal Code	Operation
PSF	6021	Skip if Punch Flag is a 1. If Punch Flag = 1, then PC+1 = > PC
PCF	6022	Clear Punch Flag and Punch Buffer. 0 = > Punch Flag, PB
PPC	6024	Load the Punch Buffer from bits 4 - 11 of the AC and punch the character. (This instruction does not clear the punch flag or punch buffer.) AC 4-11 V PB = > PB
PLS	6026	Clear the Punch Flag, clear the Punch Buffer, load the Punch Buffer from the content of bits 4-11 of the AC, punch the character, and set the Punch Flag to 1 when done. 0 = > Punch Flag, PB AC 4-11 = > PB 1 > Punch Flag when done

PUN ACTIVE flip-flop, and the Punch Buffer flip-flops (PB) PB0 through PB7. PCF is generated by combining the device codes with IOP2(1). The resulting pulse is applied to the Direct Clear flip-flop inputs. Normally, this instruction is combined with PPC for the remainder of the program.

PPC (6024)

The PPC instruction, performed after the PCF instruction in the program, consists of the device selection code and IOP4(1) pulse. This control pulse is applied to the clock input of the PB flip-flops, permitting the transfer of PDP-8/I accumulator data (AC04 through AC11) into the PB register through the flip-flop data inputs. The pulse also sets the PUN ACTIVE flip-flop to precondition the unit for punching data into the tape. The PUN ACTIVE(1) output (+3V), is applied to the data input of the PUN FLAG. This allows the PUN FLAG to set when the PUN DONE signal pulses the clock input. The PUN ACTIVE(0) output (0V) is ORed with the PUN Feed switch. When either signal is at 0V, the ORed output combines with the SYNC PUN pulse to trigger a delay. (The delay depends on the model of the punch used. With the Royal-McBee Punch, the delay is adjusted to 10 ms. For the BRPE II Punch (Teletype Corporation), the delay adjustment is 4.5 ms.) The delay al-

lows completion of the punch operation before the PDP-8/I attempts another PCF instruction.

When the delay input is triggered, the output changes from +3V to 0V for the duration of the time delay. This output is inverted activating the FEED-HOLE solenoid driver NAND gate. The solenoid drivers for holes 1 through 8 activate when the controlling gates are enabled by both the leading edge of the inverted delay output, and active PB flip-flops (+3V on the 1 side). The solenoid drivers then release the punch mechanisms and the tape is punched.

When the delay has elapsed, PUN DONE is generated. This transition from low to high sets the PUN FLAG flip-flop and clears the PUN ACTIVE flip-flop by pulsing their clock inputs.

PSF (6021)

When the PUN FLAG is set, the (1) output activates the I/O BUS IN INTerrupt line (0V), and enables the I/O BUS IN SKIP Gate. I/O BUS IN INT indicates to the PDP-8/I that some device is requesting service. The PDP-8/I then enters a programmed search subroutine to determine the device that caused the interrupt. This search is performed by a series of "flag checking" skip instructions. A skip instruction is executed for each device attached to the interrupt line. The PP8/I PUN FLAG status is checked by the PSF instruction. When the PUN FLAG is set and this instruction is executed, the I/O BUS IN SKIP gate is activated causing the PDP-8/I program counter to increment by one, thereby skipping the next sequential instruction in the program. The PDP-8/I then recognizes that the high-speed punch has finished punching a character and a programmed service routine is entered to issue a new punch instruction. Normally, the PLS (6026) instruction is used next to continue punching.

PLS (6026)

This instruction decodes to IOP2(1) and IOP4(1) in the same computer cycle. The first pulse clears the PB, PUN FLAG, and the PUN ACTIVE flip-flops, and the second initiates the punch cycle as described previously.

In PP8/I options that contain revision D of the M710 Punch Control module however, the contents of the PUN FLAG flip-flop are preserved during a feed operation. (This is important when feed operations are accomplished during a program loop that is searching for the punch flag.) In activating the punch, the FEED switch signal clears only the PB flip-flop, leaving PUN ACTIVE and PUN FLAG unaltered. This change was accomplished by clocking the PUN FLAG unaltered. This change was accomplished by clocking the PUN FLAG flip-flop with the PUN ACTIVE (0) signal rather than with the PUN DONE signal. Thus, when a programmed operation occurs, the clocking of PUN ACTIVE to a logic zero by PUN DONE sets the PUN FLAG flip-flop; during a feed operation, however, PUN ACTIVE is not altered.

Another logic change in revision D eliminates the clearing of the PB flip-flop upon INITIALIZE and IOB3(1). This does not alter the external operation however, because the transfer of information through the PB flip-flop is a jam transfer.

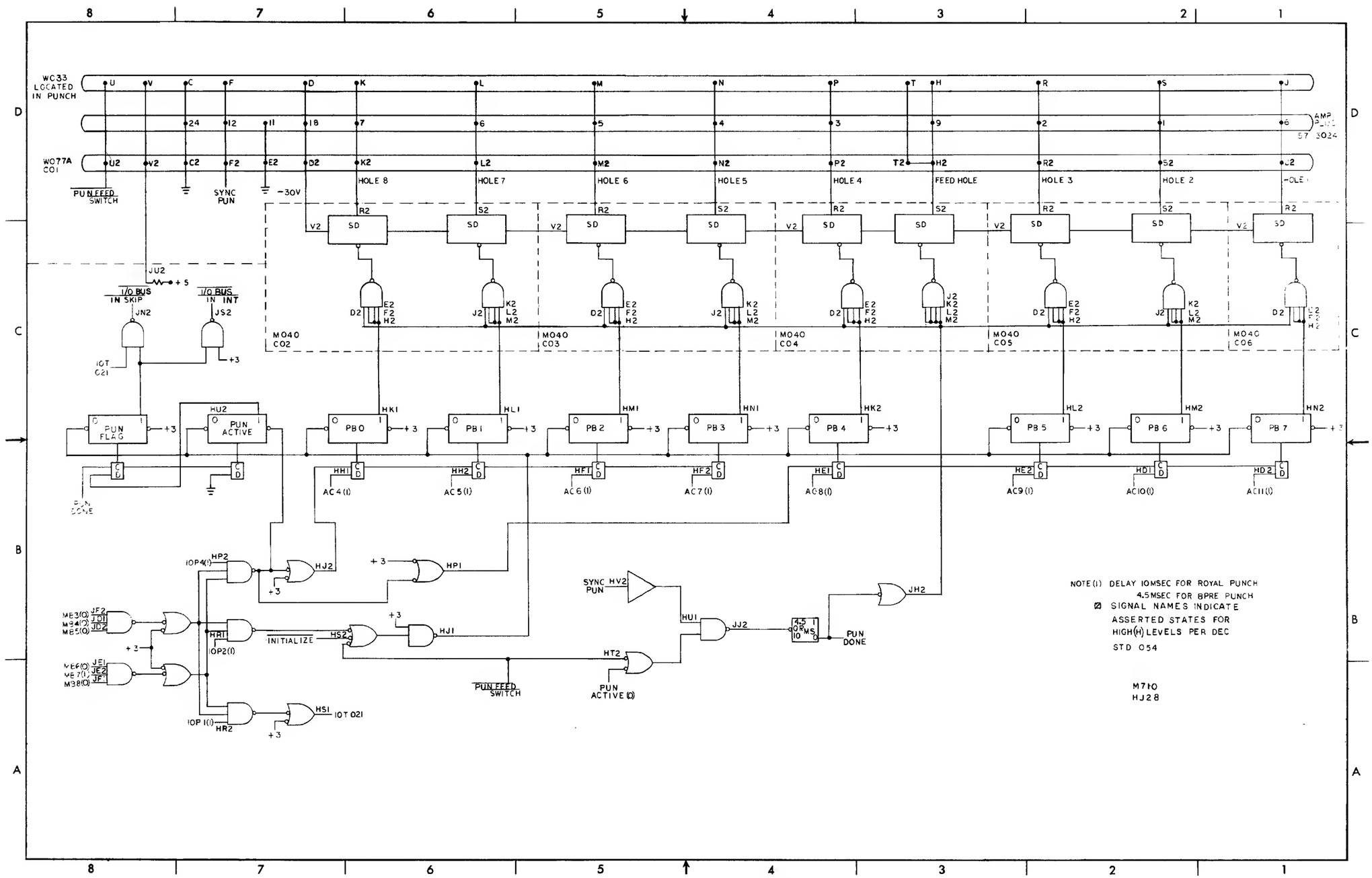
Maintenance

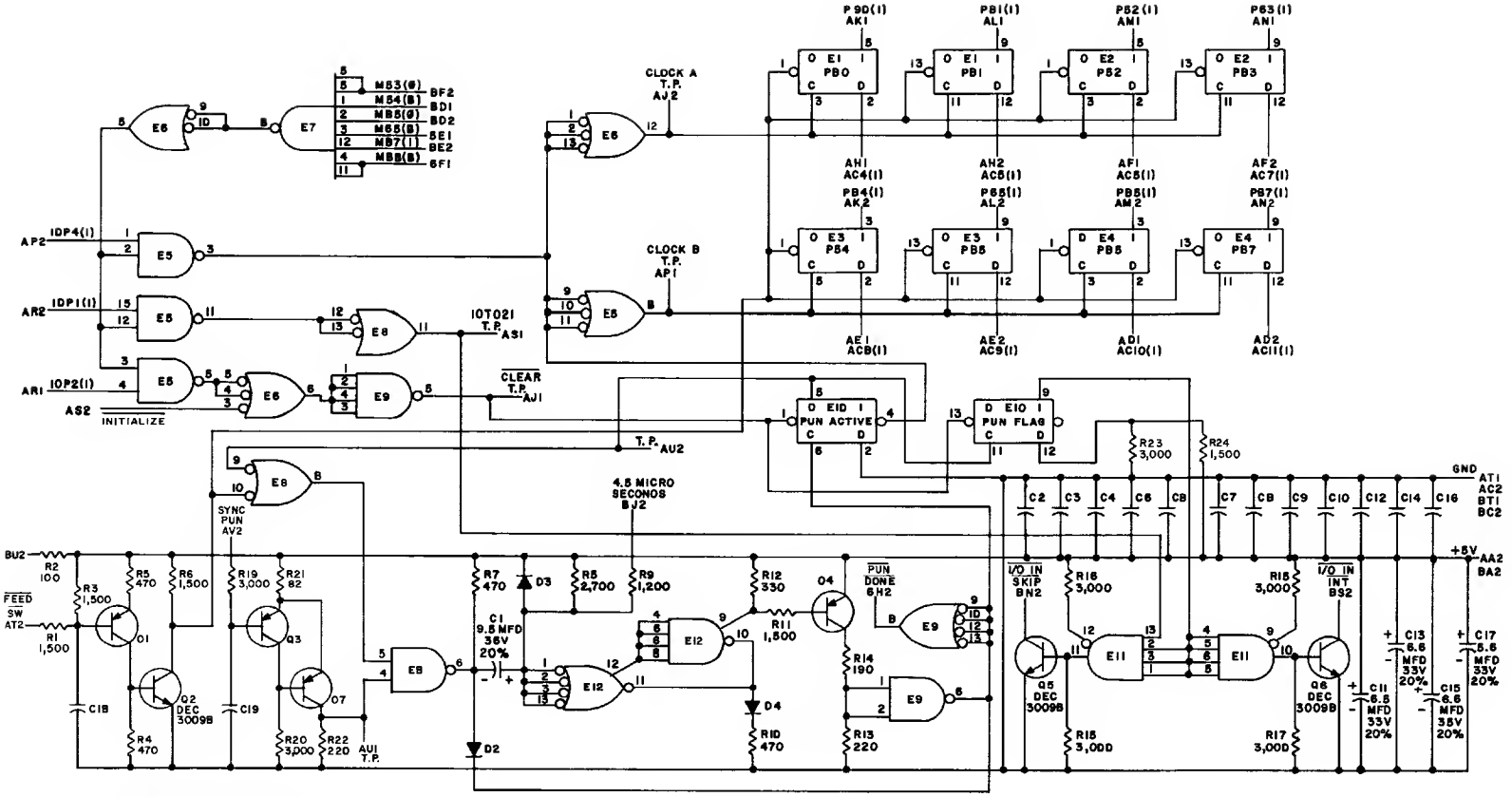
The maintenance procedures pertaining to the PDP-8/I also apply to the PP8/I control logic. The recommended maintenance pro-

cedures for the Royal-McBee or Teletype Corporation punches are found in their respective manuals.

ENGINEERING DRAWINGS

The following engineering drawing D-BS-PP8I-0-1, and the circuit schematic C-CS-M710-0-1 pertaining to the PP8/I option are contained in this section.


WC33 LOCATED IN PUNCH
WO77A CO1
PUN FEED SWITCH
SYNC PUN
-30V
HOLE 8
HOLE 7
HOLE 6
HOLE 5
HOLE 4
FEED HOLE
HOLE 3
HOLE 2
HOLE 1
AMP PLUG 57 3024
M040 CO2
M040 CO3
M040 CO4
M040 CO5
M040 CO6
SD
I/O BUS IN SKIP
I/O BUS IN INT
IOT 021
PUN FLAG
PUN ACTIVE
PUN DONE
PB 0
PB 1
PB 2
PB 3
PB 4
PB 5
PB 6
PB 7
AC4(1)
AC5(1)
AC6(1)
AC7(1)
AC8(1)
AC9(1)
AC10(1)
AC11(1)
IOP4(1)
IOP2(1)
IOP1(1)
INITIALIZE
PUN FEED SWITCH
SYNC PUN
PUN ACTIVE (2)
4.5 OR 10 MS
PUN DONE
IOT 021
NOTE (1) DELAY 10MSEC FOR ROYAL PUNCH
4.5MSEC FOR BPRE PUNCH
(2) SIGNAL NAMES INDICATE ASSERTED STATES FOR HIGH(H) LEVELS PER DEC STD 054
M710 HJ28



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
TRANSISTORS ARE DEC55345
CAPACITORS ARE .01 MFD
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E1, E2, E3, E4, E10 ARE DEC7474N
E5, E6 ARE DEC74D0N
E8 IS DEC741ON
E7 IS DEC743ON
E9 IS DEC744ON
E11, E12 ARE DEC745ON
DIODES ARE D654

C-CS-M710-0-1 Punch Control M710