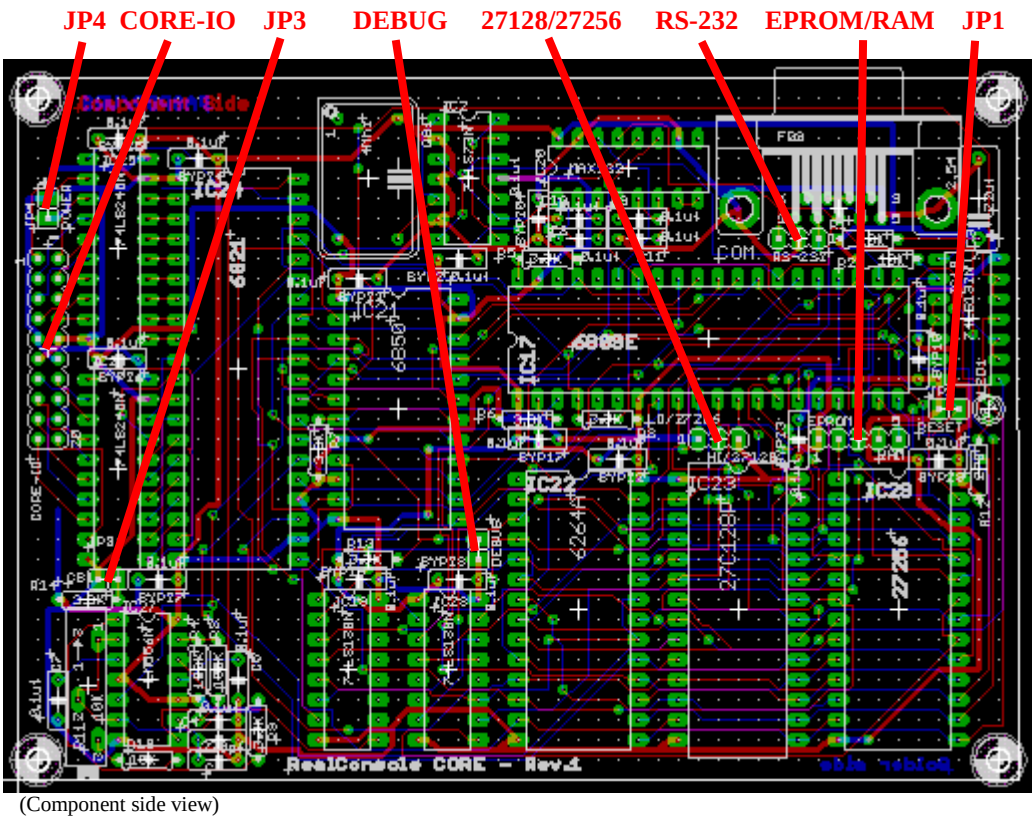
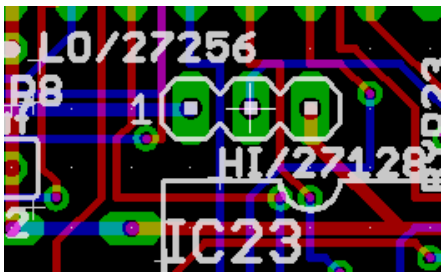
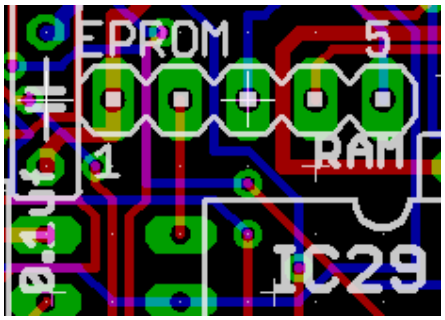
Configuration of the Core Board

The Core Board has the following jumpers / connectors.



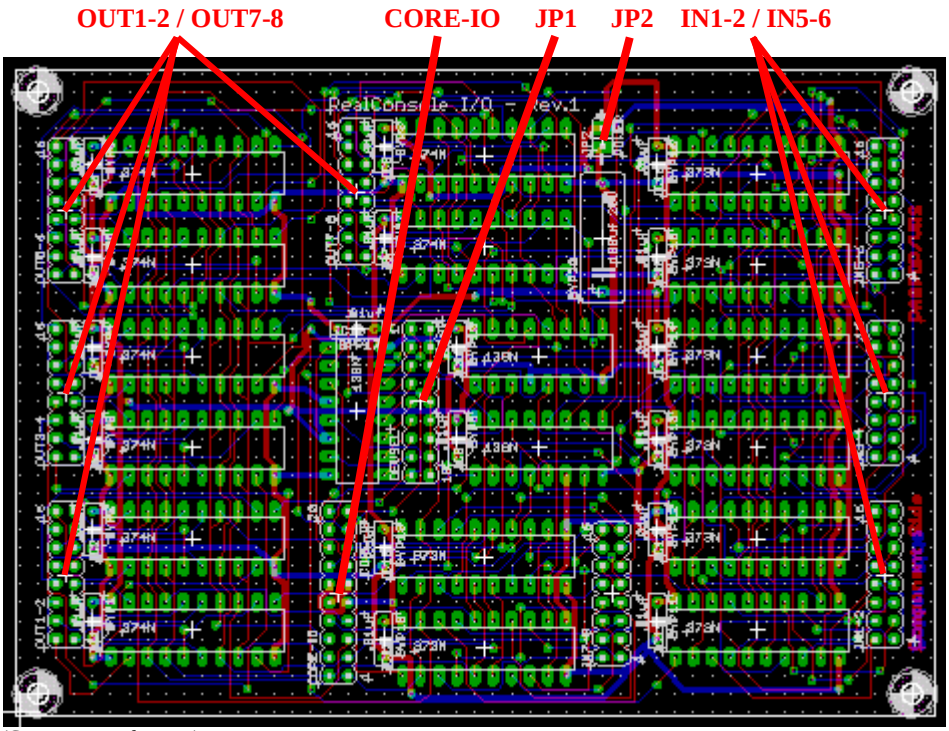
(Component side view)

JP1	External RESET push-button. Normally Open button to reset the Core Board externally.
DEBUG	External Tester / Debug Monitor start-up. Normally Open button. After power-up or reset the Core Board starts the Tester application; when during reset or power-up the button contacts are closed, the Debug Monitor is started.
JP3	PIA 6821 CB1 input pin. The CB1 pin has a pull-up resistor of 3300 Ω. The other pin is connected to GND. The CB1 pin is available for another application on the Core Board.
JP4	+5 V / GND power supply connector (optional, as there is also a power connector on the I/O Board) **Make sure you connect the power supply correctly …!!**
RS-232	Serial port connection (parallel to COM connector) If the Tester is built inside a box you can use the 3-pin RS-232 header instead of the 9-pin connector. *Note 1: if you use the 3-pin RS-232 header you can simply swap to null-modem or straight connection (DTE or DCE) by connecting the 3-pin connector the other way around.* *Note 2: The Core Board (thus the Tester) does not support DTR/DSR or RTS/CTS flow control.*

27128 / 27256	Boot EPROM type selection / “bank” selection. If the IC23 is a 27128 you must connect the 2 pins at the text “HI/27128”. If IC23 is a 27256 (cheaper) you have the option of selecting the upper or the lower half of the EPROM. In the “HI/27128” position the upper half (E000-FFFF) is active, and in the “LO/27256” position the lower half is active (C000-DFFF). *Remark: the selected half must contain the boot code.*  ▪ **Jumper on Pin #1 - #2 (“LO”)** – EPROM type = 276256 (lower 16k byte visible) ▪ **Jumper on pin #2 - #3 (“HI”)** – EPROM type = 27128 or – EPROM type = 27256 (upper 16k byte visible)
EPROM / RAM	Device selection of IC29, either 27256 EPROM or 62256 RAM. 2 jumpers on pins #1-#2 and #3-#4 is for EPROM, #2-#3 and #4-#5 is for RAM.  ▪ **Jumpers on #1 - #2 <u>and</u> #3 - #4** IC29 = 27256 EPROM ▪ **Jumpers on #2 - #3 <u>and</u> #4 - #5** IC29 = 62256 RAM **Note: 2 jumpers used !**
CORE-IO	Interface connection between the Core and the I/O board.

Configuration of the I/O Board

The I/O Board has the following jumpers and connectors.



(Component side view)

OUT1-2 **OUT3-4** **OUT5-6** **OUT7-8**	Output port connectors to the Tester Board.
IN1-2 **IN3-4** **IN5-6**	Input port connectors from the Tester Board. Note. The connector IN7-8 is *not* used.
JP2	+5 V / GND power supply connector. **Make sure you connect the power supply correctly !!**
CORE-IO	Interface connection between the Core and the I/O Board.
JP1	Board "number" selection. This 18-pin header selects the I/O Board number. Install only **one** jumper. **jumper between pins** — **I/O Board** 17 - 18 — #0 15 - 16 — #1 13 - 14 — #2

Configuration of the Tester Board

Configure the hardware as a “single-height FlipChip” Tester.

The Tester Board does not need any configuration actions if the Tester that you build is used for single-height FlipChips only. The firmware uses 2 input pins of the input port IN5 to determine the Tester configuration. The firmware identifies the connected hardware as a “single-height” setup if the 2 input pins are left open. That means this single I/O - Tester Board setup must be jumpered as Board #0.
If you build the Tester for single-height FlipChips, check the following.

- The I/O Board must be set as I/O Board #0, must have a header installed for IN5-6, and must have the 5th 74LS373 input latch installed.
- The Tester Board must have the 7410-1k-0.1µF components installed.

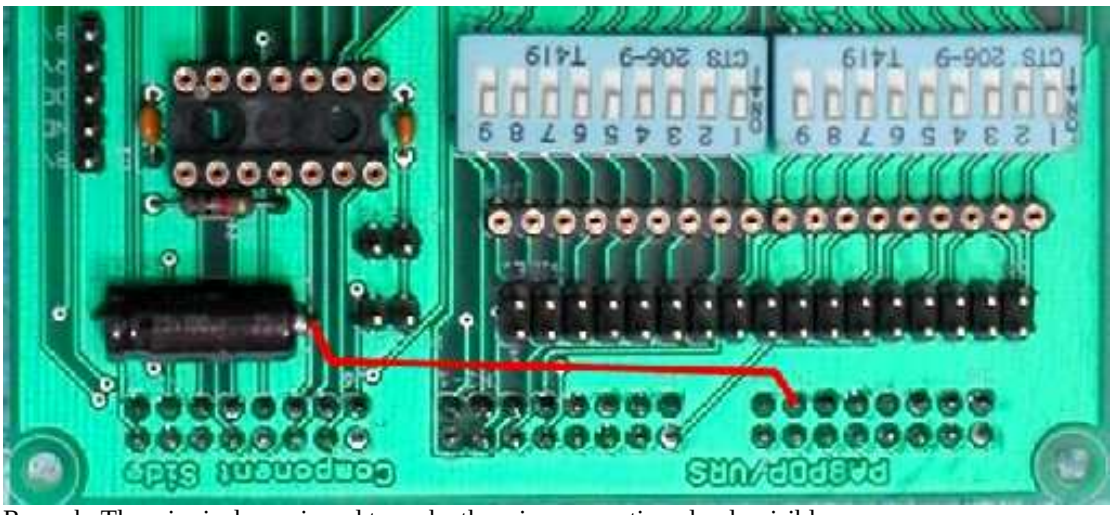
Configure the hardware as a “double-height FlipChip” Tester.

If you build the Tester for double-height FlipChips, check the following.

- The I/O Board that is connected to the Tester Board with the 7410-1k-0.1µF components installed must be set as I/O Board #0, must have a header installed for IN5-6, and must have the 5th 74LS373 input latch installed.
- The I/O Board that is connected to the Tester Board with the 7410-1k-0.1µF components *not* installed must be set as I/O Board #1, does not need a header for IN5-6 (because the connections through IN5-6 are not used), and does not need the 5th 74LS373 input latch.

You must solder one wire on the component side of the Tester Board that is connected to I/O Board #0. This wire notifies the firmware that a “double-height” hardware setup is connected. The wire connects one input pin of the input port IN5 to GND.

1. Solder a short (black) wire on the solder island of pin #4 of connector IN5-6.
2. Solder the other end of the short wire the “-“ connection of the electrolytic polarised capacitor.



Remark. The wire is drawn in red to make the wire connection clearly visible.