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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 9/16/74

TITLE AR11 Circuit Description

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	DATE	SIZE	CODE	NUMBER	REV
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1.0 INTRODUCTION

1.1 The AR11 is a one-module real-time analog subsystem that interfaces with the PDP-11 family of computers via a hex SPC slot.

Included on the AR11 module are the following:

- 1.1.1 Bus Control, with switch-selectable address.
- 1.1.2 Interrupt Control, with switch-selectable vector.
- 1.1.3 A/D Converter, with 16-channel multiplexer and sample-and-hold.
- 1.1.4 Real-time Clock, with five crystal-based frequencies, external input, and an 8-bit counter.
- 1.1.5 Display Control, with two 10-bit D/A converters.
- 1.1.6 Analog Power Supply.

1.2 The following material should be referenced when using this document:

- 1.2.1 M7809 (AR11) circuit schematics D-CS-M7809-0-1.
- 1.2.2 AR11 User's Guide DEC-11-HARUG-A-D
- 1.2.3 PDP11 Processor Handbook
- 1.2.4 Manufacturer's manual for XY display scope or storage scope being used with the AR11.

1.3 Reading M7809 Prints

At the bottom right corner of each M7809 circuit schematic page is the page title, e.g. BAS (BUS ADDRESS SELECT). The symbol preceding the parentheses is the page mnemonic. Each

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signal generated on a given page has that page's mnemonic in front of it for page cross-reference purposes. For example, BAS ENABLE L originates on the BUS ADDRESS SELECT page, and is low when ENABLE is asserted.

2.0 BUS CONTROL

The AR11 Bus Control consists of BAS (BUS ADDRESS SELECT), BIO (BUS IN/OUT) and DM (DATA IN MULTIPLEXERS), pages 3, 4 and 5 of the M7809 schematics.

2.1 Bus Address Select

The purpose of the bus address select logic is to recognize one of the eight AR11 register addresses on the Unibus address lines, select the register for input or output data transfer upon receipt of MSYN L from the processor, and to acknowledge receipt of MSYN L by sending SSYN L back to the processor.

BUS address lines A17 L through A04 L are used to recognize that one of eight AR11 registers is being addressed. Bus address lines A03 L through A01 L are decoded to determine which of these eight registers is being addressed. BUS A00 L is used to determine high or low byte within the word, in conjunction with BUS C00 L, which is low for a computer output byte operation and high for an output word operation.

BUS A11 L through A04 L are compared with the state of the address select switches using "exclusive or" circuits E87 and E94.

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The "exclusive or" output is high when A11 through A04 match the switch address. When this occurs, and the E62-3 output is high, the AR11 has recognized its address, and BAS ENABLE L is asserted. The E62-3 output is high with BUS MSYN L asserted and 77XXXX (W2 connected) or 76XXXX (W2A connected) on the bus address lines. Thus, as a function of the address switches, the AR11 can have any address from 760000 through 767760 with W2A connected and from 770000 through 777760 with W2 connected.

AR11 address selection is further illustrated in figure 1:

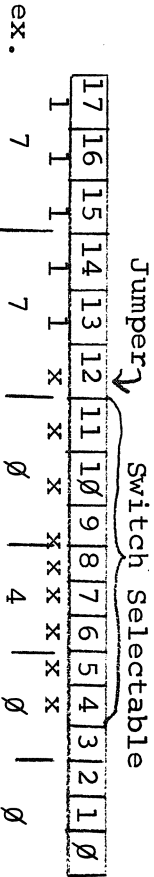


Figure 1: AR11 Address Selection

Location of the address switches on the module is shown in figure 2. The switches are set "on" for a 0 and "off" for a 1, i.e. to set up 770400, all switches are "on" except for the bit 8 switch.

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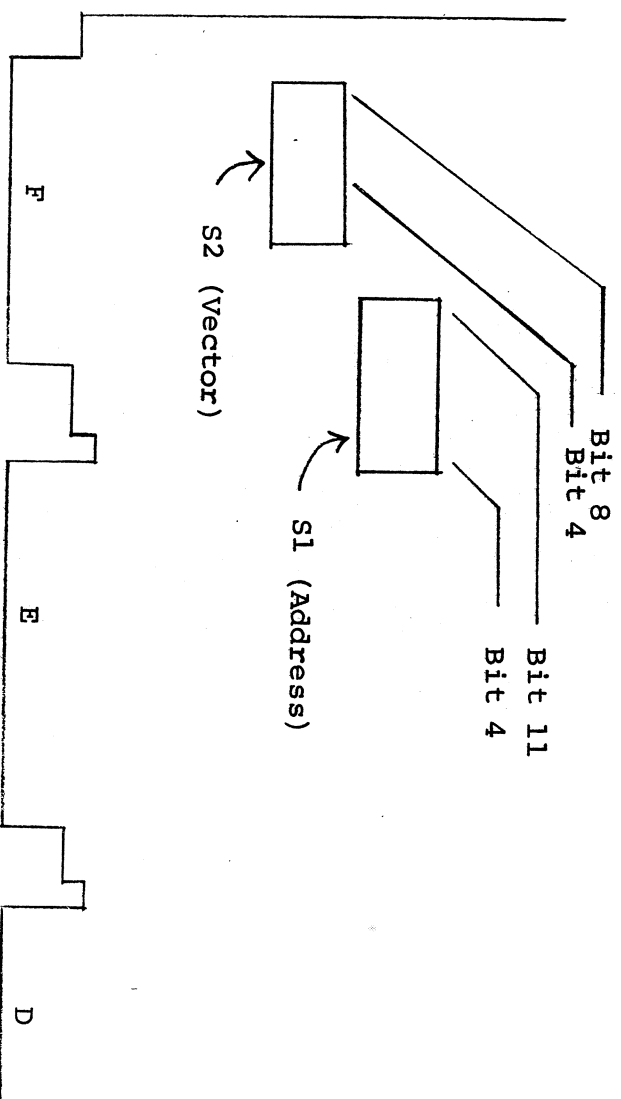


Figure 2: Switch Location

When BAS ENABLE L is asserted, the address decoder E74 is enabled. As a function of address lines BAS A03H through BAS A01H, E74 selects one of the eight AR11 registers and asserts the corresponding select line, per Table 1.

After a delay of approximately 75 nsec, determined by the (R1 + R2) C1 time constant, BAS ENABLE L causes the slave synch line SSYN L to be asserted, informing the processor that the selected data has been received or is present on the data lines.

BUS INIT L is buffered to produce BAS INIT L, BAS B INIT L, and BAS INIT H, which clear all the registers and flags, with the exception of the scope control ready flag. The INIT signal occurs

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on start key depression, power up, or RESET instruction.

TABLE 1: REGISTER ADDRESSES

	A03 H	A02 H	A01 H	Address Selected
L	L	L	L	A/D Status
L	L	H		A/D Buffer
L	H	L		Clock Status
L	H	H		Clock Preset Buffer
H	L	L		Display Status
H	L	H		X Buffer
H	H	L		Y Buffer
H	H	H		Clock Counter

2.2 Bus In/Out

The Unibus has bidirectional data paths, which are interfaced to the ARLL using 8641 (8838) receiver/transmitter chips. The outputs of the data multiplexers (DM BIT ØØ H, DM BIT Ø1 H, etc.) are impressed on the Unibus data lines (BUS DØØ L, BUS DØ1 L, etc.) for computer input operations. This occurs when BAS IN L and BAS ENABLE L are asserted, signifying an input operation when the ARLL has recognized its address.

The data lines enter the AR11 from the Unibus through the inverters, and become the BIO OUT XX H signals.

2.3 Data In Multiplexers

The DATA IN MULTIPLEXERS use 74151 and 74157 multiplexer chips to sort out the data from the eight different registers. The selected register outputs become the DM BIT XX H signals, which are passed on to the Unibus by the BUS IN/OUT logic.

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A03 H, A02 H and A01 H are used as address inputs by the 74151 one-of-eight multiplexers, to select the desired register, for bits 0 through 9. Bits 10 through 13 are only contained in the A/D Status Register and Display Status Register. Therefore, they are able to use a 74157 quad one-of-two multiplexer chip. When A02 H and A01 H are low, E55-15 is low, enabling the 74157. When this occurs, either the A/D or Display Status register is being selected. BAS AD STAT L goes to pin 1 of the 74157, to select which of the two registers is active.

3.0 INTERRUPT CONTROL

The interrupt control handles three distinct interrupts. These may come from the A/D (INT A H), the Realtime clock (INT B H) or the scope control (INT C H). The A/D and clock interrupts are handled on priority level 6, with the A/D higher in priority (closer to the processor) than the clock. The scope control interrupt is on priority level 4. The priority levels cannot be changed. Since the three interrupt circuits act in essentially the same manner, only the A/D interrupt will be discussed.

Flip-flops FF1A and FF2A start out in the cleared (zero) state, since the interrupt line ADC INT A H has been low. Therefore, E84-6 is high, so that when ADC INT A H goes high (A/D interrupt), BR6 L goes low, requesting an interrupt on priority level 6. Some time later, the interrupt request is granted, and BG6 H goes high. BG6 H is buffered by E91, so that E91-3 goes high. This transition sets FF1A, and

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initiates a 100-nsec. delay through E92, Q3, and E83. Before the end of this delay, FF1A (1) H goes high, so that E83-1 holds the bus grant output low at the end of the delay (i.e. the bus grant stops at the interrupting device and is not passed on). If the A/D had not been the interrupting device, FF1A would be held at 0 due to INT A H being low, FF1A (1) H would be low, and at the end of the 100-nsec. delay, the bus grant BG6 would be passed on (IV BG 6 PASS, to the INT B circuitry). When FF1A is set, since FF2A is still at 0, pins 8 and 9 of E83 are both high, causing BUS SACK L to go low. This indicates to the processor that the bus grant has been received. The processor then removes the bus grant so that BG6 IN H goes low. This causes a positive transition at E82-12 which sets FF2A. With both FF1A and FF2A set, E83-13 goes low, asserting BUS BBSY L, indicating that the interrupting device has taken control of the bus. At the same time, E74-6 goes low, which, through E37, enables E95 and E96. This gates the interrupt vector address onto the BUS D08:D02 lines and asserts BUS INTR L. The processor responds with BUS SSYN L when it has received the vector. This signal goes through E89 to reset the A INT flip-flop (IV A INT DONE L). This causes ADC INT A H to go low, so that E71-11 goes low, and FF1A and FF2A both are reset. Resetting FF1A and FF2A removes the vector from the bus, disqualifies BUS BBSY L and BUS INTR L, and returns the circuitry to its original state.			
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The starting interrupt vector may be set in increments of 2 $\emptyset$ up to a maximum of 76 $\emptyset$, using S2. Vector selection is illustrated in figure 3:

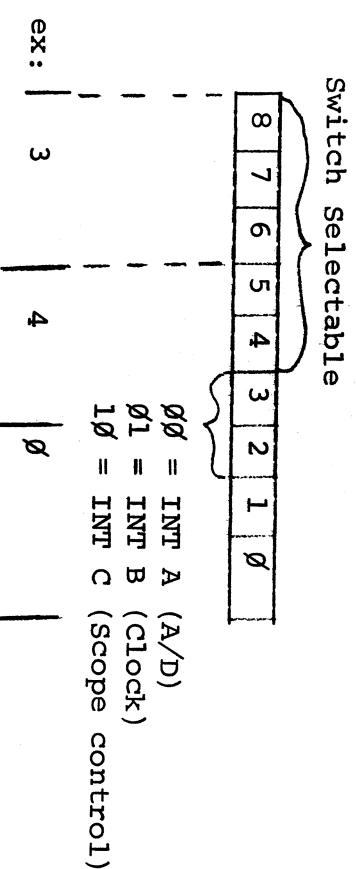


Figure 3: AR11 Vector Address Selection

- Location of the vector switches on the module is shown in figure 2. The switches are set "on" for a 1 and "off" for a $\emptyset$ (note that this is opposite to the address switches), i.e. to set up a vector of 34 $\emptyset$, bits 7, 6 and 5 are "on" and bits 8 and 4 are "off".

Bits 3 and 2 are gated onto the bus by E96 as a function of which of the three interrupts is active.

4.0 REAL-TIME CLOCK

The real-time clock consists of a free-running 1 MHz crystal oscillator circuit, a series of four decade counter dividers to generate additional frequencies of 100 KHz, 10 KHz, 1 KHz, and 100 Hz, a multiplexer to select a single frequency for input to a counter, and three registers (clock preset buffer, clock counter, and status).

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4.1 Crystal Oscillator

The oscillator consists of two 8640 gates, connected as inverters with ac-coupled inputs and resistive feedback in a cross-coupled configuration through the 1 MHz crystal. The crystal acts as a low impedance only at 1 MHz and as a high-impedance at all other frequencies. Consequently, at 1 MHz, the two gates are set up in a cross-coupled configuration and oscillation occurs. The output signal RTS PS CLK, available on TP C, is a clean TTL

1 MHz signal. This signal is used directly as a power supply clock, and gated in E81 by the enable counter signal RTC ENA CNTR (1) L before going to the dividers. When the counter is not enabled (RTC ENA CNTR (1) L is high) the counter output can be simulated by the maintenance signal RTC TEST COUNTER H through E81.

4.2 Divider Chain and Multiplexer

The 1 MHz signal is used to generate 100 KHz, 10 KHz, 1 KHz and 100 Hz signals using 74190 decade up/down counters E98 through E101, running in the upcount mode. Each counter increments on the low-to-high transition of the pin 14 input. The pin 13 output goes low when the pin 14 input is low and the counter state is 9, providing a low pulse to the next stage.

The five crystal-based frequencies generated in this manner go to the multiplexer E97, along with the external input and

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auxiliary clock input. One of these frequencies is selected according to the rate select bits (RTC RATE 0 (1) H, RATE 1 (1) H and RATE 2 (1) H) on E97 pins 11, 10 and 9. The selected rate appears in inverted form on the pin 6 output ($\bar{F}$) of the E97 multiplexer. Since the signals from the divider chain are low-going pulses ($\frac{1}{2}$ μ sec), the signal on E97-6 is a positive pulse. Under normal conditions, E90-7 is high, so that the multiplexer output goes through E90 and appears as a low-going pulse RTC CLK OUT L, which is the input to the clock counter. If BAS MAINT CLK CTR L is low, E90 serves to "stretch" the RTC CLK OUT L pulse, to prevent the counter from changing state while it is being read by the processor.

4.3 Clock Counter and Buffer

The clock counter is an 8-bit presetable counter register consisting of 74193 4-bit up/down counters E40 and E41, used in the upcount mode. Count input is RTC CLK OUT L, on E40 pin 5. Every 16th count, E40-12 propagates the signal into the E41 pin 5 input. The counter register is cleared on INIT, and loaded from the preset register on RTC LD CLK CNTR L, which occurs on overflow in continuous interval mode (mode 1) or when the clock buffer is loaded when the clock is disabled.

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The clock buffer register is loaded from the BIO OUT 07:00 H lines when its address is selected (BAS CLK BUF L goes low). The buffer register load pulse is gated through E71 when the counter is not enabled (RTC ENA CNTR (0) H is high), so that the clock counter is also loaded.

In continuous interval mode, RTC CLK MODE 1 L is low (E81-5) so that E81 acts to invert the signal on E81-6. In single interval mode, E81-5 is high so that E81-4 is low and the clock counter is never loaded via E57-12.

In continuous interval mode the low-going overflow pulse RTC CLK OVRFLW L appears at E81-3 and is inverted at E81-1.

This high-going pulse is ac-coupled through C7, so that its trailing edge causes a low at E81-6. This causes a high pulse at E81-4 which occurs just after the overflow pulse, and causes the clock counter to be reloaded from the clock buffer register.

The clock overflow signal occurs whenever the counter goes from 377 to 0. The pulse actually goes low during the 377 state, and its trailing edge corresponds to the 377 to 0 transition. Consequently, the counter is reloaded with the preset value at the beginning of the 0 state.

4.4 Clock Status Register

The clock status register is a read/write register whose bits control the functions performed by the clock. The high byte of

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this register consists of one-half of E58 (bit 15) and E75 (bits 8, 11 and 14). The high byte is loaded on a pulse from E57-10, the and function of BAS CLK STAT L and BAS OUT HIGH L. The low byte of this register consists of one-half of E58 (bit 7), one half of E70 (bit 0), and E76 (bits 1, 2, 3 and 6). The low byte is loaded on RTC LD CLK LOW H, E57-4, the and function of BAS CLK STAT L and BAS OUT LOW L.

Bit 15, the external flag, is loaded from BIO OUT 15 H when the register is loaded. It is set by the external signal ADC EXT ST (1) L and reset by BAS B INIT L. Bit 14, part of the 74175 E75, is loaded from BIO OUT 14 H. When bit 14 = 1, E68 is enabled to set the clock interrupt flip-flop E70 on the occurrence of the external input ADC EXT ST (1) L. Bit 11, RTC TEST COUNTER H, is used for maintenance purposes to test the clock divider chain. Bit 8, clock mode, determines whether the clock is in continuous interval mode (1) or single interval mode (0).

Bits 3, 2, and 1, part of the 74175 E76, are loaded from BIO OUT 03:01 H when the low byte of the register is loaded. These bits determine the selected rate according to Table 2. Bit 6, also part of E76, is used by E68 to enable the clock overflow to cause an interrupt.

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TABLE 2 - Rate Select

Bit 3	Bit 2	Bit 1	Frequency
Rate 2	Rate 1	Rate 0	
0	0	0	—
0	0	1	1 MHz
0	1	0	100 KHz
0	1	1	10 KHz
1	0	0	1 KHz
1	0	1	100 Hz
1	1	0	External
1	1	1	Aux-pin EL2

Bit 7, the clock done flag, is loaded from BIO OUT 07 H when the low byte of the register is loaded. It is set by RTC CLK OVLW L and reset by BAS INIT L. Bit 0, the clock enable bit, is loaded from BIO OUT 00 H when the low byte of the register is loaded. It is reset from E69-10, the or function of BAS INIT H and clock overflow in single interval mode, from E69-1.

5.0 ANALOG POWER

The analog power supply is shown on page 8 of the M7809 schematic, labelled HQP (High Quality Power). The power supply is a dc-to-dc converter, which develops +14V dc (nominal) from the +5V logic supply. Instead of using a step-up transformer, the power supply uses diodes and capacitors in an extension of the basic voltage doubler technique.

5.1 Voltage Doublers

A basic voltage doubler is shown in figure 4. Its input

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is a square wave running between ground and +5V. During the time that the input is at ground, diode D1 conducts, and C1 charges to +4.3 volts (+5 volts minus the D1 diode drop). In the next half-cycle, the input is at +5V. Since the voltage across the capacitor C1 remains constant, V₁ goes to +9.3 volts, and D1 becomes back-biased. During this interval, D2 conducts, and V_{out} charges to one diode drop less than V₁, or +8.6 volts.

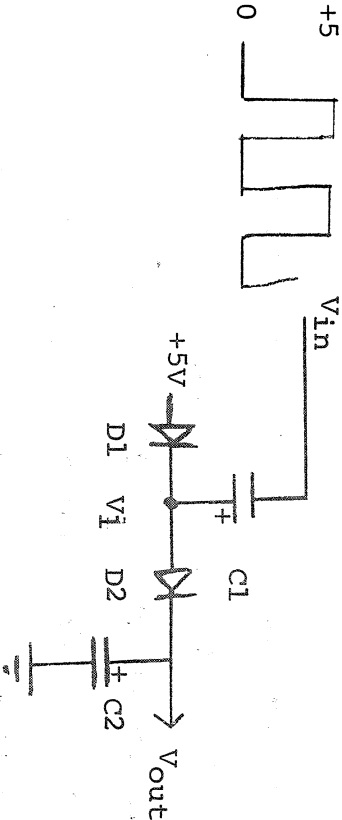


Figure 4: Voltage Doubler

In the next half-cycle, we are back to the beginning, with Vin at ground and D1 conducting, charging C1. At this time, V₁ is at +4.3 volts, and D2 is back-biased. The output voltage remains at +8.6 volts, i.e. we have transformed the +5V input to a +8.6 volt output. Note that if we ignore the two diode drops, we have effectively doubled the input voltage. A good way of looking at the process is that the circuit represents a "bucket brigade". During one half-cycle, charge is passed to C1 through D1. During the next half-cycle, charge is then transferred from C1 to C2

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through D2. Obviously, if we cascade multiple sections, higher voltages can be attained, as charge is passed in "bucket brigade" fashion from one capacitor to the next and ultimately from the last capacitor into the load.

5.2 Square Wave Driver

The 5V square wave input voltage for the AR11 power supply is produced by transistors Q5 and Q6. Transistor Q5 is a PNP which pulls the voltage up to +5 Volts. Transistor Q6 is an NPN which pulls the voltage down to ground. In such circuits, with both active pullup and active pulldown, it is important to guarantee that the two transistors are never on at the same time, even for an instant during switching. This is especially difficult since in general transistors turn off more slowly than they turn on. In the AR11, to guarantee that one turns off before the other turns on, a full 1-μsec interval is allowed.

The signal RTC PS CLK, a 1 MHz (1 μsec) square wave, is applied to pin 14 of E49, a 7493 divide-by-16 counter. The most significant bit of this counter is applied through E48 to the input of flip-flop E45, whose outputs are square waves with a 32-μsec. period. During each half-cycle of the 32-μsec square wave, the 7493 E49 counts from 0 to 15, remaining in each state for 1 μsec. The 7420 E37 decodes the 15 state, so that its pin 8 output goes low for the last microsecond of each half cycle. This

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causes both the pin 8 and the pin 6 outputs of E56 to go high, so that all the E27 outputs are low. When HQP A L (E27-2) is low, Q4 turns on, thereby turning off Q5. When HQP C L (E27-8, 10, 12) is low, Q6 turns off. Thus for the last microsecond of each half-cycle, both Q5 and Q6 are turned off, allowing the one which had been on to turn off completely before the other turns on. The resulting waveforms are shown in figure 5. Note that the square wave drive signal (TP PD) shows a definite intermediate state at the time when both Q5 and Q6 are off.

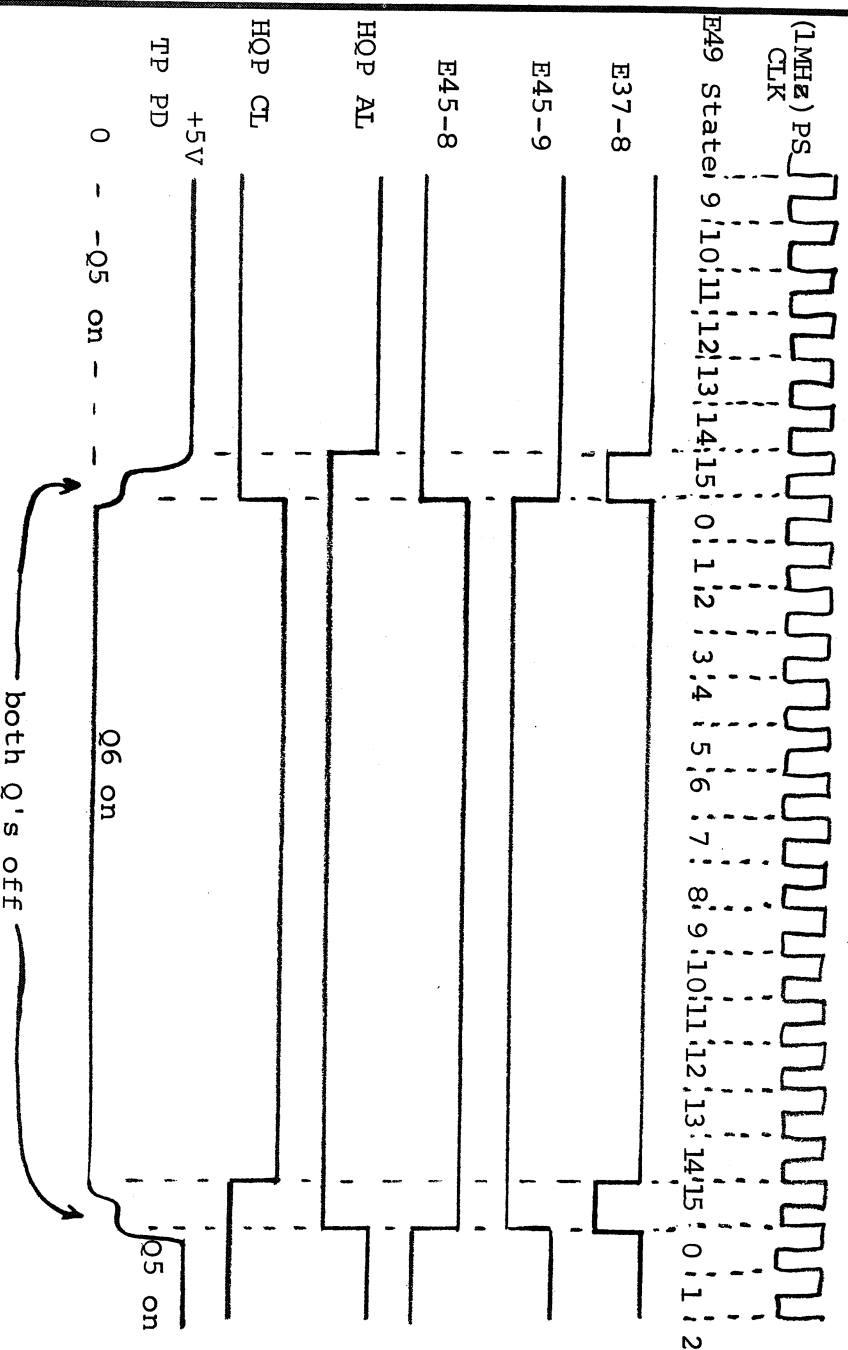


Figure 5: Square Wave Timing Waveforms

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5.3 First Stages

The first stage of the power supply "doubler chain" consists of D4 through D9 and C12 through C14. These are driven directly by the output of Q5 and Q6, as seen at TP PD. Since the diode-capacitor chain functions as a "distributed transformer", the early low-voltage stages run at the highest current levels. Consequently, the TP PD voltage is not the idealized zero-to-+5V signal, but actually only exhibits about a 4.5V swing. The diodes (even though doubled up) exhibit a drop of roughly .85 volts. By the analysis of section 5.1, this results in +7.3 volts dc at the positive end of C13. When TP PD is low, this results in 7.3 - .85 = 6.45 volts at the cathode of D8 and D9. When TP PD goes high, we get 6.45 + 4.5 ≈ 11 volts at the cathode of D8 and D9. Referring to figure 4, TP PD is high when HQP A L is high. At this time HQP BL is also high, so that Q7 is off, allowing Q8 to be turned on. In the opposite half-cycle, HQP B L is low, turning on Q7 and thereby turning off Q8. Meanwhile E27-6 goes high allowing Q9 to turn on. This results in a 10 Volt square wave at the collectors of Q8 and Q9. As in the case of TP PD, the collectors of Q8 and Q9 exhibit the 1-μsec intermediate state, when both transistors are off.

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5.4 Output Stages

The 0V square wave at the collectors of Q8 and Q9 is the input signal for the output diode-capacitor chains. By following an analysis similar to that of section 5.1, allowing roughly .75 Volts for each diode drop, but ignoring the effect of zener diodes D13 and D14, output voltages in the range of ± 16 Volts to ± 17 Volts are arrived at, which would be somewhat higher than desired. However, zener diodes D13 and D14 (whose nominal values add to 15V) act as a regulating negative feedback loop. As the minus supply becomes more negative than -14 Volts, the zeners begin to turn on. This "steals" base drive current from Q9 when it is on, keeping Q9 out of hard saturation and thereby dropping the magnitude of the Q8-Q9 output square wave. This negative feedback loop automatically adjusts the square wave voltage so as to maintain the negative output near -14 Volts. Since the positive supply is also based on the same square wave, it also ends up near +14 Volts.

The two outputs are "smoothed" by LC filters (L2-C25, C24 on the minus side; L1-C21, C23 on the plus side) with a break frequency of roughly 4 KHz, which tend to reduce the ripple and remove high frequency components present due to the switching transients.

The M7809's digital and analog grounds are connected in the middle layer at a single point near the return (ground) end of

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these filter capacitors.

6.0 ANALOG BIAS CURRENT SOURCES

All analog circuitry in the AR11 is biased by means of current sources, in order to be immune to variations in power supply voltage. The current sources are all shown on page 9 of the M7809 schematics, ABS (Analog Bias Sources).

The reference upon which all the current sources are based is D49, a 1N825 6.2V reference zener diode. This zener is specified to have minimum thermal drift when run at a current level of 7.5 mA. A simplified version of ABS is shown in figure 6, in which Q14 through Q19, Q28 and Q29 have been combined as a single transistor Q_A, and Q25 through Q27 and Q74 have been combined as Q_B.

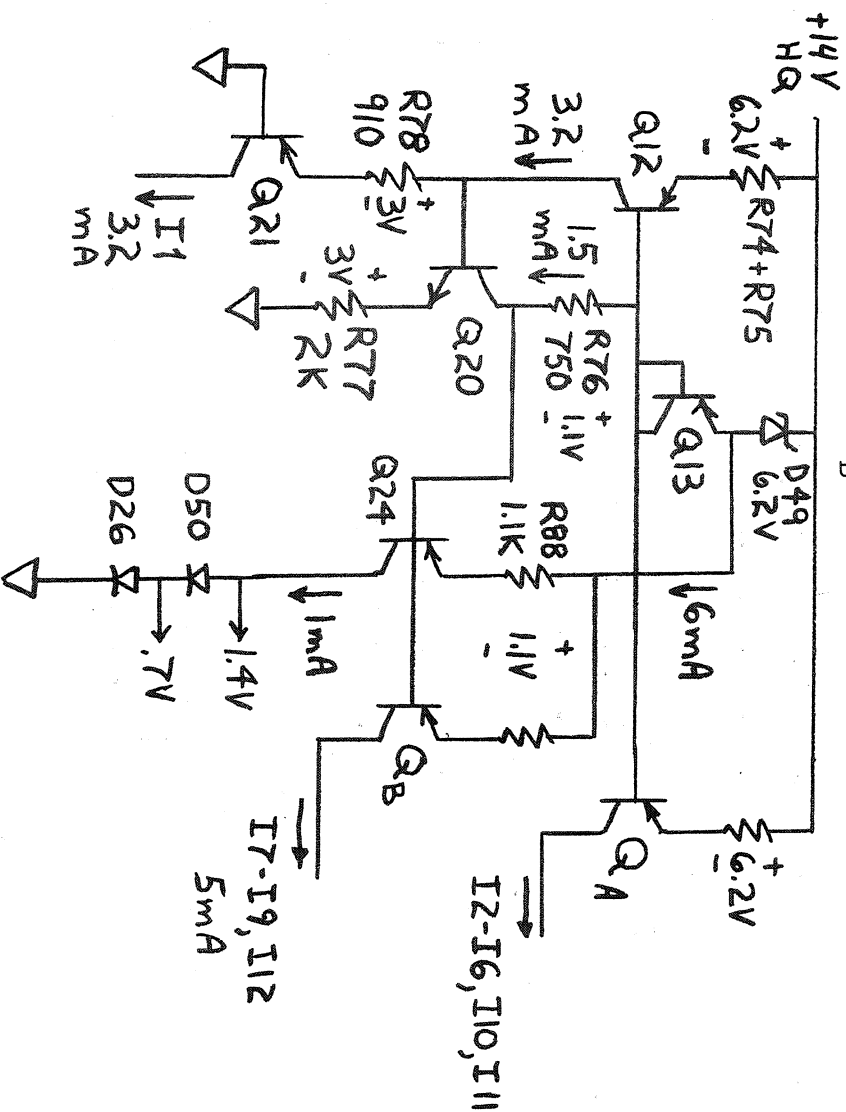


FIGURE 6: SIMPLIFIED ABS

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In analyzing this circuit, we start at zener diode D49, and assume that it is operating at 6.2Volts, its nominal value.

Transistor Q13 has base and collector tied together, so that its base-emitter (b-e) junction acts as a diode. Since the Q13 b-e drop matches the b-e drop of Q12, there is also 6.2 Volts across R74 and R75. Potentiometer R75 is adjusted so that $I_e = 6.2 / (R74 + R75) = 3.2 \text{ mA} \approx I_c$. Consequently, the collector of Q12 is a 3.2 mA current source, as shown in figure 5. This current goes through R78 and Q21 and appears as I1 at the collector of Q21.

Along the way, it sets up a 3 Volt drop across the 910-ohm R78. Since the b-e drops of Q21 and Q20 match, we also have 3 Volts across the 2K R77. This causes the collector of Q20 to be a 1.5 mA current source. This 1.5 mA comes down from the positive supply through the reference zener D49, Q13, and R76. The 1.5 mA through the 750-ohm R76 establishes a 1.1 Volt drop across R76. Since the b-e drop of Q13 matches those of Q24 and Q_B, we also have 1.1 Volts across the emitter resistors of Q24 and Q_B. With an emitter resistor (R88) of 1.1K, Q24 becomes a 1 mA current source. This 1 mA goes to ground through D26 and D50, thereby setting up voltages of .7 Volts and 1.4 Volts for use on pages 11 and 12 of the M7809 schematics. Likewise, the 1.1 Volts across the emitter resistor of Q_B (actually R89, R90, R91, R105) sets up current sources I7, I8, I9, and I12, which total 5 mA. This 5 mA, the 1 mA in Q24, and the 1.5 mA in Q20, combine to make the desired

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7.5 mA in D49, the reference zener. Since the Q13 b-e drop matches the b-e drop of Q_A we have 6.2 Volts across the emitter resistor of Q_A (actually R83 + R171, R84 + R172, R85 + R173, R86 + R174, R87, R92, R93). This sets up current sources I2, I3, I4, I5, I6, I10 and I11.

7.0 SCOPE CONTROL

The scope control circuitry is shown on four pages of the M7809 schematic: p. 13 DIR (Display Registers), p. 14 DIL (Display Logic), p. 15 DACX and p. 16 DACY. Since the X and Y D/A converters are identical, only the X D/A converter will be described.

7.1 DIR (Display Registers)

The X Buffer Register consists of 74175 E7 (bits 6-9) and 74174 E8 (bits 0-5). It is loaded from BIO OUT 09:00 H on DIL LD X BUF H, which originates on the display logic page. It is cleared on BAS INIT L.

The Y Buffer Register consists of 74175 E1 (bits 6-9) and 74174 E2 (bits 0-5). It is loaded from BIO OUT 09:00 H on DIL LD Y BUF H, and cleared on BAS INIT L.

Since the 74174 IC has its outputs available only in (1) H form, 7404 hex inverters E3 and E9 are employed to provide Y5 through Y0 and X5 through X0 in (1) L form for use by the D/A converters.

Display Status Register bits 9-11 are contained in 74175 E13.

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They are loaded from BIO OUT 11:Ø9 H on DIL LD DISP HIGH H, and cleared on BAS INIT L. Bits 9, 10, and 11 are CHØ2 STORE, and WRITE THRU. CHØ2 H is inverted by open collector inverter E15, pulled up to +5V by R115 and output through J1-B as CHØ2 L. STORE (1) L is inverted by E15 and output through J1-E as NON STORE L (note the inversion). WRITE THRU H is inverted by E15 and output through J1-A as WRITE THRU L.

Display Status Register bits 2, 3 and 6 are contained in 74175 E14. They are loaded from BIO OUT Ø2, Ø3 and Ø6 H on DIL LD DISP LOW H, and cleared on BAS INIT L. Bits 2 and 3 are DIR DISP MODE Ø (1) H and MODE 1 (1) H, used on the display logic page to control the intensification mode. Bit 6 is DIR DISP INT ENA (1) H, used on the display logic page to enable an interrupt upon completion of intensification of a point.

7.2 DIL (Display Logic)

The display logic page contains scope intensification circuitry, storage scope, erase controls, ready(done) bit, interrupt control, and gates which generate load pulses for the various display registers.

On the left side of the page, the load pulses are generated by E19 and E24, using the register select and output byte signals from the BAS (Bus Address Select) page.

A scope intensification pulse is generated (after appropriate delay) under the following conditions:

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INTENSIFICATION MODE	BIT 3		BIT 2		CONDITION
	MODE 1	(1) H	MODE Ø	(1) H	
Ø			Ø		Set bit Ø
1			Ø	1	Load X
2			1	Ø	Load Y
3			1	1	Load X or Load Y

TABLE 3: Intensification Modes

These conditions are decoded by 7453 E20. For example, if we are in mode 2, MODE 1 (1) H is high, so that when we get LD Y BUF H (load Y buffer register) pins 1 and 13 of E20 are both high, and pin 8 goes low. The low on E20-8 causes a high on E15-2 which causes two things to happen: the signal causes a low on E19-10, which resets E25, the ready (done) flip-flop. It also fires one-shot E21. The resultant E21 delay is to provide time for the D/A outputs and scope beam to settle before intensifying the point on the scope. The E21 delay is nominally 20 µsec, but can be set to 80 µsec for slow storage scope applications by connecting W3. At the end of the E21 delay, a low-to-high transition occurs on E21-4, which fires the other one-shot in E21. This one-shot determines the intensification pulse duration-nominally 2 µsec, but jumperable to 6 µsec for slow storage scopes by means of W6. Either the high or low output of the second one-shot can be applied to E15-13 as a function of whether W4A or W4 is connected, depending on whether a high or low intensification

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TITLE AR11 Circuit Description

pulse is desired. After the E15 inversion, the pulse is applied to the base of Q51, which amplifies and re-inverts the pulse for output to the scope. Q52 acts as a 20 mA current source pullup for the output pulse. The output pulse is clamped at 3.3 Volts by zener diode D32, or at 1.4 Volts by diodes D33 and D34 if W5 is connected. The high-going intensification pulse from E21-5 passes through E19 and sets the ready (done) flip-flop E25 on its trailing edge.

Bit 12 of the Display Status Register is implemented by the erase flip-flop E23. It is loaded from BIO OUT 12 H on the DIL LD DISP HIGH H pulse. Setting the Erase flip-flop initiates two actions: ERASE (1) H resets the ready (done) flip-flop E25 through E19, and the inverted (through E15) erase signal DIL ERASE L is applied to the external storage scope through J1-C. The storage scope responds with a low signal ERASE RET L on J1-H. This turns off Q53, so that DIL ERASE CLR H is pulled up to +5V through R121. ERASE CLR H goes through E24 and resets the Erase flip-flop E23 through pin 1. After the interval of time necessary to erase its screen (typically one-half second), the storage scope brings ERASE RET L back to a high voltage level. This turns on Q53, bringing DIL ERASE CLR H low. The resulting low-to-high transition on E19-13 sets the ready (done) flip-flop E25.

When DIR DISP INT ENA (1) H is high, the display interrupt is enabled. In this case, setting the ready (done) flip-flop,

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as a result of either an intensification pulse or completion of an erase operation, sets the display interrupt flip-flop E25.

The resulting interrupt signal DIL INT C H is processed by the IV circuitry. Upon completion of the interrupt, IV DISP INT DONE H resets E25 through E24. Both the erase and interrupt flip-flops are also reset by BAS INTT H, acting through E24.

7.3 D/A Converters

The following description applies to both the X and Y D/A converters, which are identical. Designations of components and signal names apply to the X D/A, page 15 of the M78Ø9 prints.

The D/A converter consists of a 10-bit converter with high output impedance (about 8K) plus a buffer amplifier to lower the output impedance and provide the current needed to drive the capacitive load of the cable to the scope.

7.3.1 Converter

The converter consists of an 8-bit current-output IC D/A (bits Ø-7), two discrete component higher-order current sources (bits 8 and 9) and an offsetting current source I4 (.625 mA), working in conjunction with precision resistors R148, R140, R141 and R145 to give a +5 Volt output.

The IC D/A E10 is powered from DACX +5V HQ, which is the +5 Volt power line filtered by L3 and (C34 + C35). Reference current for this D/A is ABS I2-3.27 mA, running into pin 13.

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Consequently, its full scale output current (all logic inputs-pins 5 through 12 - high) is 3.27 mA. Resistance seen by this output current is R145 - 768 ohms. Consequently, bits 0-7 have a total weight of (3.27 mA) (768 ohms) = 2.5 Volts, or one-quarter of full-scale. Now let's examine the two high-order current sources. Assume that X9 (1) L and X8 (1) L are both high, so that E16-2 and -12 are low, and therefore Q54 and Q55 are both off. Voltage reference ABS VB2 is set up on the ABS page-it is 4 Volts plus one transistor b-e drop above the -14V HQ supply. Consequently, the emitters of Q58 and Q59 are 4 Volts above the -14 VHQ supply. It is important to note that this voltage tracks along with the negative supply, so that the voltage across (R136 + R139) and across (R137 + R138) is a constant 4 Volts, independent of the exact level of the negative supply voltage. The values of (R136 + R139) and (R137 + R138) are adjusted so that 1.25 mA current flows in the output line of each current source. Because of the high-current-gain complementary NPN-PNP configuration, Q58 and Q59 base currents are negligible. The 1.25 mA output current from the bit 8 source (Q59, Q57) sees a resistance of (R141 + R145), approximately 2K. Consequently bit 8 has a weight of (1.25 mA) (2K) = 2.5 Volts, or one quarter of full-scale. The 1.25 mA output current from the bit 9 source			
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(Q58, Q56) sees a resistance of (R140 + R141 + R145), approximately 4K, so that bit 9 has a weight of (1.25 mA) (4K) = 5V, or one-half of full-scale. Assume an all 1's (1777) input to the D/A. DIR X9 (1) L and X8 (1) L are now low, so that E16-2 and -12 are high, and Q54 and Q55 are on. In this case, the Q54 and Q55 emitters clamp at +.7 Volts, leaving 4.3 Volts across R130 and R131. Q54 and Q55 become current sources, with a value $I = (4.3V/3K) = 1.43 \text{ mA.}$ Since this current is greater than 1.25 mA, all the current from (R136 + R139) and (R137 + R138) is "stolen", Q58 and Q59 turn off, and the bit 9 and bit 8 currents are zero. Since the input is all 1's, E10-5 through -12 are all low, so that the E10-4 output current is also zero. This leaves only I4-.625 mA flowing. I4 goes to ground through (R148 + R140 + R141 + R145), approximately 8K. Consequently, the voltage at the base of Q61 during the 1777 condition is (.625 mA) (8K) = +5 Volts. If we go to all 0's, Q54 and Q55 turn off, allowing the 1.25 mA bit 8 and bit 9 current sources to turn on. E10-5 through -12 are now all high, so that the E10-4 output current is 3.27 mA. These sum up linearly, giving a voltage (as seen at the base of Q61) of +5V (due to I4) -5V (due to bit 9) -2.5V (due to bit 8) -2.5V (due to bits 0-7) = -5 Volts.			
SIZE	CODE	NUMBER	REV
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Note that the all 0's case, with -5 Volts output, actually represents all bit currents <u>on</u>, and the all 1's case, with +5 Volts output, actually represents all bit currents <u>off</u>, with only the offset current I4 on. Since the circuit is linear, any digital combination between 0000 and 1777 results in the proper corresponding voltage between -5 Volts and +5 Volts. The impedance seen at the base of Q61 is the sum of R148 + R140 + R141 + R145, or 8K. If WX is shorted, this 8K is now in parallel with (R134 + R135) = 886 ohms, for a resulting equivalent resistance of 800 ohms. Since this is exactly one-tenth of the original 8K, shorting WX has resulted in one-tenth the output voltage range, or <u>±</u>.5 Volts. Connecting a resistor in place of WX can result in any resistance desired between 8K and 800 ohms, and therefore in any voltage range desired between <u>±</u>5 Volts and <u>±</u>.5 Volts. 7.3.2 Buffer Amplifier The voltage seen at the base of Q61 has 8K source impedance, and is therefore unsuitable for output drive. To provide output drive, a buffer amplifier consisting of Q61, Q62 and Q63 is provided. Bias current for this buffer amplifier is I10, a 1 mA current source. If the input voltage (Q61-base) equals the			
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output voltage (Q62-base), I10 splits equally and ½ mA shows up in the collector of both Q61 and Q62. The Q61 collector current goes through D38 and R142 to the minus supply. Since the D38 diode matches the Q63 b-e drop and R142 and R143 have equal values, the Q63 collector current equals the Q61 collector current. For equal split of I10 between W61 and Q62, we therefore, have the current out of Q62 equal to the current into Q63, so that there is no net current into or out of C33. This gives us a stable output voltage. If the Q61-base voltage is lower than the Q62-base voltage, more of I10 goes through Q61 than Q62, so that the Q63 current is higher than the Q62 current and we have a net current flow out of C33. Consequently, the C33 voltage (which is also the voltage on the base of Q62) drops, until the Q62-base voltage equals the Q61-base voltage, at which point I10 again splits equally and a stable condition is reached. In this manner, the output voltage (Q62-base) follows the input voltage (Q61-base). Output impedance of this amplifier is approximately 50 ohms. The 47-ohm protection resistor R144 brings the output impedance up to 100 ohms. The Q61 and Q62 b-e junctions are protected for large steps by diodes D35 and D36. The amplifier is protected from "outside-world" overvoltages by fusible resistor R144 and diodes D37 and D39.			
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8.0 A/D CONVERTER					
The A/D circuitry is contained on three pages of the M7809 schematic: page 10, ADC (A/D Control), which contains all the A/D logic; page 11, ADCS (A/D Channel Select), which contains the input protection circuitry and analog multiplexer; and page 12, AD (A/D), which contains the sample-and-hold circuit and the actual A/D converter.					
8.1 A/D Control					
The A/D Status Register high byte is contained in 74174 E63. It is cleared on BAS B INTT L, and loaded from BIO OUT 13, 11:08 H when the A/D Status Register and a high byte output operation are selected. The four-bit channel address and unipolar/bipolar bit are contained in the high byte of the status register.					
The A/D Status Register low byte is contained in 74175 E77. It is cleared on BAS B INTT L, and loaded from BIO OUT 06:04 H when the A/D Status Register and a low byte output operation are selected. Bit 6 is used to enable an interrupt on setting of the A/D done flag. Bit 5 enables an A/D conversion to start on overflow from the real-time clock. Bit 4 enables an A/D conversion to start on an external input.					
Bit 0 of the A/D Status Register is used for a program-controlled A/D conversion start. The A/D Status Register low byte load pulse goes through 7404 inverter E48 to one-shot E34. This one shot triggers on the register load pulse if BIO OUT 00 H 1s					
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high, i.e. if a "1" is being loaded into the A/D Status Register bit 0. The one-shot time is nominally 8 μ sec., which is long enough to allow for the analog multiplexer to settle to its new value before signalling the sample-and-hold to hold the signal, at which point the conversion begins. If it is desired to switch between bipolar and unipolar channels, a 7.5 Volt inter-channel difference is possible instead of the normal maximum of 5 Volts. In this case, W1 is connected, lengthening the one-shot time to 11 μ sec, which is sufficient for the 7.5 Volt difference.					
At the end of the E34 delay, E34-12 goes high, setting the E44 "Hold" flip-flop, which commands the sample-and-hold circuit to hold the analog value for conversion. At the next occurrence of the HQP AD CLK H low-to-high transition (which could be anywhere from 0 to 2 μ sec later), the E44 "Enable A/D" flip-flop is set, which signals the AM2504 successive approximation register (SAR) E26 to begin the A/D conversion. The SAR then sequences through the ten A/D bits, for each bit making its logical decision on the low-to-high transition of HQP AD CLK H, as a function of ADC COMP L. The AD CLK is a 2- μ sec clock signal derived from the 1 MHz crystal oscillator by the E49 power supply counter. Consequently, it takes two microseconds for each "bit decision". The decision signal (COMP L) is derived from the output of the comparator (AD COMP H) by 7405 inverter E47. By jumpering AD COMP H (TP1) to ground, it is possible to bypass the analog circuitry					
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and simulate that comparator output which results in a 1777 con-
version. By jumpering ADC COMP L (TPØ) to ground, it is possible
to bypass the analog circuitry and simulate that comparator out-
put which results in a ØØØØ conversion.

After the least significant bit (ADØØØ) has been resolved,
ADC EOCP L goes low, so that E47-2, 6 are pulled high by R35.
After one microsecond, HØP AD CLK H goes low, so that E47-2, 6
are pulled low by E47-2. This causes a low-to-high transition
on E48-8, which loads the A/D Buffer Register (E39 and E43) with
the converted value information contained on the SAR outputs
AD ØØ:Ø9 H.

ADC EOCP L is inverted by E48 to create ADC EOCP H. This
is or'ed with BAS INIT H in E46 to create ADC CLR L. This signal
resets the "Hold" and "Enable A/D" flip-flops to their original
(Ø) states, and is input to SAR E26-14. This signal is present
for two microseconds, until the next low-to-high transition of
HØP AD CLK H, which then resets the SAR E26.

Bit Ø of the A/D Status Register is held at "1" throughout
the 8-µsec A/D Start delay and the conversion interval by or-gate
E28, which creates ADC AD STAT ØØ (1) H from HOLD (1) L and the
output of the 8-µsec A/D Start delay one-shot.

ADC EOCP H also sets the "AD DONE" flip-flop E45 on its
leading edge. Its output ADC AD DONE (1) H is used as bit 7 of
the A/D Status Register. When an A/D interrupt is enabled,

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ADC AD INT ENA (1) H is high, so that setting the "AD DONE"
flip-flop causes E56-11 to go low and E48-4 (ADC INT A H) to go
high. This causes the A/D interrupt. When the interrupt is
complete IV A INT DONE L goes low. This causes E56-3 to go high
and E46-10 to go low, thereby resetting AD DONE. If the A/D in-
terrupt is not enabled, AD DONE is not reset until a read opera-
tion is performed on the A/D Buffer Register. When this occurs,
BAS IN L and BAS AD BUF L both go low, so that E46 goes high and
E46-10 goes low, thereby resetting the "AD DONE" flip-flop. This
flip-flop is also reset by BAS B INT L, acting through E56 and
E46.

An A/D conversion may also be started by either an external
start signal or a clock overflow. The external start signal
(J1-U) high-to-low transition fires one-shot E34 to create a
500-nsec ADC EXT ST (1) pulse. ADC EXT ST (1) L is used as the
external input by the real-time clock counter. ADC EXT ST (1) H
is used by the real-time clock for its external interrupt and by
the A/D for external starts. If the A/D external start is enabled,
ADC EXT ENA (1) H is high, and ADC EXT ST (1) H on E68-3 causes
E68-6 to go low, thereby setting the "HOLD" flip-flop and initiat-
ing the conversion sequence. If the clock overflow start is ena-
bled, ADC AD CLK ENA (1) H is high, so that RTC CLK OVLW H on
E68-4 causes E68-6 to go low, thereby setting HOLD and initiating
the conversion sequence.

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8.2 A/D Analog Block Diagram Description

The AR11 uses a unique auto-zeroing A/D configuration, in which the same amplifier front end is shared between the sample-and-hold and A/D comparator is such a manner as to cancel out its own offset and drift.* This configuration is shown in figure 7.

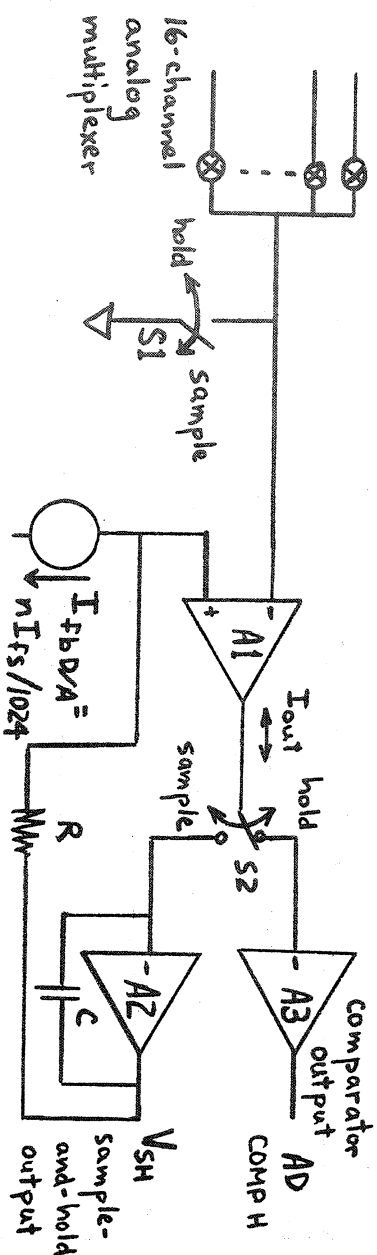


FIGURE 7: A/D Analog Block Diagram

*Patent pending

Amplifier A1 is the front end which is shared between the comparator and sample-and-hold. This amplifier is an operational transconductance amplifier, i.e. its input stage is that of an ordinary operational amplifier, but its output is a current source I_{out} instead of a voltage source.

First let's consider the tracking, or "sample" mode of operation, in which S1 is open, S2 is down, and the feedback current source is off, i.e. $I_{FBD/A} = 0$. Under these conditions, A1 output current I_{out} is integrated and converted to a voltage by sample-and-hold output stage A2, so that the A1-A2 combination acts like an operational amplifier. The A2 output is fed back

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to the A1 input, so that the A1-A2 op amp is in a follower configuration, with the A2 output voltage tracking the selected analog input present on the inverting A1 input.

When it is time to do an A/D conversion, S2 switches from the down to the up position on setting of the "HOLD" flip-flop.

This leaves integrator A2 with zero input, so that feedback capacitor C holds the A2 output voltage constant. This will now serve as the A/D input voltage. On setting of the "ENABLE AD" flip-flop zero to two microseconds later, the 16-channel analog multiplexer is disabled, so that the selected channel switch opens up, and S1 closes, putting a ground reference on the inverting input of A1. Under these conditions, A1 serves as the comparator input stage. A1 output current I_{out} is converted to a logic-compatible voltage level AD COMP H by output stage A3. The successive approximation logic now looks at AD COMP H and proceeds to find that value of n ($0 \leq n \leq 1023$) which results in zero input to amplifier A1. This occurs at $I_{FBD/A} = n I_{FS}/1024 = V_{SH}/R$; $n = 1024 V_{SH}/R I_{FS}$. If we set the scaling such that $R I_{FS} = V_{FS}'$, the desired full-scale input voltage, we have $n = 1024 V_{SH}/V_{FS}'$. During "sample", V_{SH} was tracking the input voltage V_{in} , i.e. $V_{SH} = V_{in}$. Consequently, $n = 1024 V_{in}/V_{FS}'$, which is the desired A/D relationship. For $V_{FS} = 5$ Volts, input voltages of 0 to 5 Volts ($1023/1024$) result in conversions of 0 to 1023, i.e. we have a unipolar input range.

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A	SP	AR11-0-5	

SIZE	CODE	NUMBER	REV
A	SP	AR11-0-5	

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TITLE AR11 Circuit Description			
Now assume identical conditions in "sample" mode except that instead of $I_{FBD/A} = 0$ we turn on the most significant bit (MSB) so that $I_{FBD/A} = I_{FS}/2$. Under these conditions, V_{SH} tracks the selected input voltage with an offset of $RI_{FS}/2 = V_{FS}/2$. If $V_{FS} = 5$ Volts, $V_{SH} = V_{in} + 2.5$, so that an input range to -2.5 to $+2.5$ corresponds to $V_{SH} = 0$ to $+5$ Volts. By turning on the MSB during "sample" we have transformed the unipolar input range into a bipolar input range, with the MSB of the feedback D/A acting as its own bipolar offset reference source. The unipolar/bipolar bit of the A/D Status Register controls the input range by controlling the state of the MSB during "sample". 8.3 ADCS (A/D Channel Select) Page 11 of the M7809 schematic, ADCS (A/D Channel Select) contains the 16-channel analog multiplexer and switch S1 shown in figure 7 above. Each of the 16 analog input channels comes in through a 1K fusible resistor, which works in conjunction with the diodes of E5 and E11 to protect the AR11 analog multiplexers from input overvoltage conditions. The 16-channel multiplexer consists of two eight-channel PMOS multiplexer IC's E6 and E12. Each of these has three address lines A0:A2 which select one of eight switches, plus an enable line OE which enables the selected switch when high and turns off all switches when low.			
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Switch S1 of figure 7 is implemented by FET Q11. During "sample", ADC ENA A/D (1) L is high, so that E18-12 is low and Q10 is off; R73 pulls the gate of Q11 down to -14V HQ and Q11 is off. When it is time to do a conversion, ADC ENA A/D (1) L goes low, E18-12 goes high, and Q10 turns on, with an emitter current of 12 Volts/20K = .6 mA. This current comes out the Q10 collector and turns on D15, so that Q10-C clamps at +.7 Volts. The gate of Q11 is at ground because of the D45 diode drop, so that Q11 turns on, bringing ADCS MUX NODE to ground. This provides a zero reference for A1 (of figure 7) during the conversion. ADC ENA A/D (1) L also goes to E28-10, 12, causing E28-8, 11 to go high and E18-2, 4 to go low. Thus both ADCS AD MUX 0 ENA H and MUX 1 ENA H are low and both multiplexers (E6 and E12) are disabled during the conversion. This allows Q11 to ground ADCS MUX NODE without having to sink any current except the bias current of A1. During "sample", ADC ENA A/D (1) L is high, so that E28 pins 9 and 13 are enabled. This allows address bit ADC AD MUX 03 H to select which of the two multiplexers is enabled - E6 is enabled on MUX 0 ENA H when AD MUX 03 H is high, E12 is enabled on MUX 1 ENA H when AD MUX 03 H is low. The three low-order address bits ADC AD MUX 00:02 H are inverted by E18 to provide the address MUX A0:A2 L to the multiplexer IC's E6 and E12. Since E6 and E12 are PMOS chips, their			
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logic thresholds are referenced to the +14V HQ supply. Therefore MUX AØ:A2 L, AD MUX Ø ENA H, and AD MUX 1 ENA H are all 14V logic swings, implemented by open collector inverters in E18 and 20K pullup resistors to +14V HQ. 8.4 AD (Converter and Sample-and-Hold) Page 12 of the M78Ø9 schematic (AD) contains the feedback D/A converter and the following circuits from figure 7: operational transconductance amplifier A1, sample-and-hold output amplifier A2, comparator output stage A3, and switch S2. The feedback resistor R of figure 7 is actually made up of R109 and R111. The feedback D/A converter is made up of an integrated circuit 8-bit current output D/A E22 and two higher-order discrete component bits, which function in the same manner as described in the D/A converter section. The two higher-order current sources are both nominally equal to 4 Volts/1.25K = 3.2 mA. The MSB (bit 9) current source "sees" the total resistance R109 + R111, approximately 800 ohms, so that its value is 2.5 Volts, or one-half of full-scale. The bit 8 current source "sees" only R111, approximately 400 ohms, so that its value is 1.25 Volts, or one-quarter of full-scale. During "sample", ADC ENA AD (1) L is high, so that ADC UNITAR H on E17-9 controls the level of E17-10. Since the SAR (E26) was reset at the end of EOCp on the previous conversion, ADC ADØ9 H is high, and E17-13 is high for unipolar and low for			
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bipolar. When E17-13 is high, Q30 is on so that the R99, R101 current is "stolen" from Q37 and the MSB current source is off. For bipolar range, E17-13 is low, Q30 is off, and the MSB current source is on during "sample", providing the needed half-scale offset. During "sample" AD ENA AD H is low, so that E17-4 is high, Q31 is on, and the bit 8 current source is off. During the conversion, the bit 9 and bit 8 current sources are controlled by ADC ADØ9 H and ADC AD Ø8 H from the SAR, acting through E17. When AD Ø9 H and AD Ø8 H are high, the corresponding current sources are on. The reference current for E22 is ABS I1 - 3.2 mA. Consequently the E22-4 full-scale output current is 3.2 mA, which is present for E22-5 through -12 all high, i.e. ADC ADØ7:ØØ H from the SAR E26 all "1". During "sample", ADC ENA A/D (1) L is high, so that E17-1 is at ground. This turns on Q32, so that the gates of Q60 and Q70 are at +14V HQ. Therefore Q60 and Q70 are off and the E22 output current is diverted into D48, so that the bit Ø-7 current is effectively off. During the conversion ENA A/D (1) L is low, E17-1 is high, Q32 is off, and Q60 and Q70 are held on by R96 between gate and source. The E22 bit Ø-7 output current then goes through Q60 and Q70, D18 and D19, and "sees" R111, approximately 400 ohms, so that its value is (3.2 mA) (400 ohms) or 1.25 Volts, which is the desired one-quarter of full-scale.			
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Operational transconductance amplifier A1 is made up of Q35, Q36 and Q40, biased by current source ABS I6-2 mA. If the base voltages of Q35 and Q36 are equal, I6 will split up with 1½ mA going into Q35 and ½ mA going into Q36, due to the unbalanced emitter resistors R106 and R107. The 1½ mA current from the collector of Q35 is "reflected" by Q40, because the D27 diode drop matches the Q40 b-e drop and R112 and R113 are equal in value. Since the Q36 collector is sourcing ½ mA, and Q40 is sinking 1½ mA, there is a net 1 mA current flowing in the direction from the Q46, Q47 emitters into the Q36, Q40 collectors. This is balanced by the 1 mA current source ABS I8, which flows down through Q44 and Q47 during "sample" and through Q43, Q45 and Q46 during "hold". The difference between this nominal 1 mA and the actual Q36, Q40 current, due to a non-zero Q35-Q36 base difference voltage, acts as the error current into sample-and-hold output stage A2 (Q49, Q50, C28) during "sample" and into comparator output stage A3 (Q48) during "hold".

Switch S2 of figure 7 is actually the current switching network consisting of Q41 through Q47. If ADC HOLD (1) L is high, the circuit is in the sample state. In this condition the bases of Q41 and Q43 are at +5 Volts. The bases of Q42 and Q44 are at +3 Volts, set up by I12-1.5 mA and the 2K pot R114. Since the Q44 base voltage is lower than the Q43 voltage, Q44 is on and I8 takes the right-hand path. Since the Q42 base voltage is lower

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than the Q41 voltage, Q42 is on and I7-.5 mA goes down into R117 instead of R116. Therefore the base of Q47 is higher than the base of Q46, and Q47 is on, allowing I8 to continue on into the A1 output. During "hold", HOLD (1) L is low, so that the Q41, Q43 base voltage is +1.4 Volts. Since the 3-Volt Q42, Q44 base voltage is now higher, I7 and I8 take the left-hand paths, through Q41 and Q43 respectively. Common base stage Q45 transmits the I8 current from Q43 on into Q46, which is now on instead of Q47 because I7 is now going into R116 instead of R117.

During "hold", diodes D28 and D29 and transistor Q45 form a feedback path for amplifier A3 (Q48) clamping the comparator output AD COMP H at +2 Volts high and +.8 Volts low.

8.5 Successive Approximation Waveforms

The AR11 A/D converter uses a successive approximation algorithm in which, initially, all ten bit current sources are on. The current sources are then turned off one at a time (MSB first), and after a two-microsecond settling time, a decision is made (on the basis of all the remaining current sources which are still on) as to whether to leave the current source off or to turn it back on. At the "decision time", if the approximation voltage (TP A) is below zero, the bit current source in question is left in the off state, and a "Ø" results; if the approximation voltage (TP A) is above zero, the bit current source in question is turned

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back on, and a "1" results. Negative voltage at TP A results in AD COMP H at +2 volts; positive voltage at TP A results in AD COMP H at +.8 volts. The approximation voltage (TP A) is a staircase with both plus and minus steps, "zeroing in" on a threshold voltage near zero. Each of the ten steps has one-half the magnitude of the previous step.

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