

408370
AR11 ENGINEERING
DRAWINGS AND
MAINTENANCE
INFORMATION

digital equipment corporation · maynard, massachusetts

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE

THIS IS PRINT SET

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DRAWING DIRECTORY
ANALOG REALTIME SUBSYSTEM
ACCESSORY LIST
**WRAP AROUND MAINT. KIT
AR11
WRAP AROUND MODULE
**CABLE, BC11L
SYS. INSTALL./ACCEPT.
CIRCUIT DESCRIPTIONS
TROUBLE SHOOTING INFO.
MULTI-LAYER REMORK STD.

B-DD-AR11-0
A-PL-AR11-0-0
A-AL-AR11-0-1
A-PL-BG5036-0-0
D-CS-M7809-0-1
D-CS-G5036-0-1
D-UA-BC11L-0-0
A-SP-AR11-0-4
A-SP-AR11-0-5
A-SP-AR11-0-6
A-SP-7665169-0-0

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B-DD-AR11-0
 A-PL-AR11-0-0
 A-AL-AR11-0-1
 A-PL-BG5036-0-0
 D-CS-M7809-0-1
 D-CS-G5036-0-1
 D-UA-BC11L-0-0
 A-SP-AR11-0-4
 A-SP-AR11-0-5
 A-SP-AR11-0-6
 A-SP-7665169-0-0

****INDICATES OPTION**

REVISIONS									
DATE		CHG. NO.		REV					

[illegible]

DRB 108

MAYNARD, MASSACHUSETTS

LEGEND

D	DOCUMENT
DN	DOCUMENT CHANGE
	NOTICE

PA	PAPER TAPE ASCII
PB	PAPER TAPE BINARY
PM	PAPER TAPE
	READ-IN-MODE

[illegible]

PARTS LIST

DATE 8-19-74

8-19-74

CHECKED	PK
DATE	8-27-79
PROD	7.0, 6.0
DATE	9-10-80

CHECKED	PCG
DATE	8-27-79
PROD	7.0. 6.0. 7.0.
DATE	9-10-84

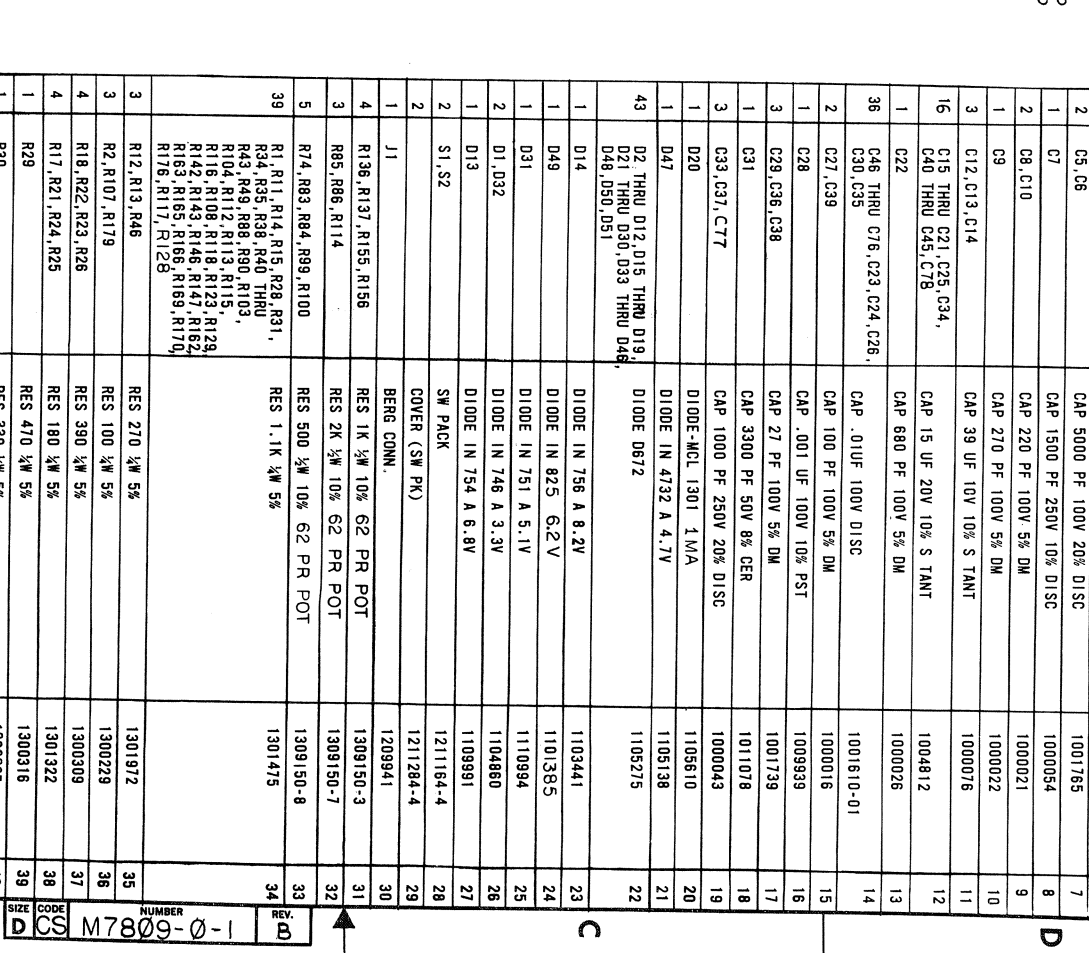
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ISSUED	1

[illegible]

DEC FORM DEC 16--(325)--1031--N870
DRA 110

408370

1



RES 47K 3W 5%	1302177	44	
RES 82 3W 5%	1301781	45	
RES 150 3W 5%	1300250	46	
DESCRIPTION		PART NO.	ITEM NO.

PARTS LIST									
DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE	DATE
17-5-78	17-5-78	17-5-78	17-5-78	17-5-78	17-5-78	17-5-78	17-5-78	17-5-78	17-5-78
TITLE									
AR11									
digital									

SIZE CODE	NUMBER	REV.
D CS	M7809-0-1	B

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000
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NOTES:

DEC 74174	8	16
DEC 7493	10	5
DEC 74123	8	16
AM 2504	12	24
DEC 74175	8	16
DEC 74193	8	16
DEC 74190	8	16
DEC 74157	8	16
DEC 74151	8	16
DEC 8641 (8838)	8	16
DEC 8640 (380)	1	8
DEC 384	1	8
DEC 314	1	8
DEC 8251 B	8	16
DEC 8837	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14
RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

3	4	5	6	7	8
3	E15, E18, E92	IC DEC 7416	1909928	96	3
7	E17, E73, E83, E84, E85, E95, E96	IC DEC 8881	1909705	97	3
4	E50, E51, E52, E67	IC DEC 8641 (8838)	1911117	98	12
7	E19, E24, E38, E46, E57, E69, E81	IC DEC 7402	1909004	99	2
11	E29 THRU E33, E42, E54, E66, E78, E88, E97	IC DEC 74151	1909396	100	3
1	E55	IC DEC 74157	1910655	101	16
9	E23, E25, E44, E45, E58, E59, E60, E61, E70	IC DEC 7474	1905347	102	2
1	E71	IC DEC 7408	1910155	103	4
1	E82	IC DEC 7427	1910878	104	1
1	E37	IC DEC 7420	1905577	105	8
4	E98, E99, E100, E101	IC DEC 74190	1910095	106	1
2	E40, E41	IC DEC 74193	1910018	107	1
10	E1, E7, E13, E14, E39, E64, E65, E75, E76, E77	IC DEC 74175	1910651	108	1
1	E88	IC DEC 7451	1905828	109	2
1	E26	IC AM 2504	1911628	110	1
2	E21, E34	IC DEC 74123	1910436	111	2
2	E16, E47	IC DEC 7405	1909330	112	2
1	E27	IC DEC 7406	1910741	113	1
1	E49	IC DEC 7493	1909054	114	2
2	E6, E12	IC DG 501C (AM3705C, IM7118C)	1911598	115	2
3	E4, E10, E22	IC MC 140818	1911629	116	4
1	E20	IC DEC 7453	1905582	117	2
4	E2, E8, E43, E63	IC DEC 74174	1910010	118	2
2	E5, E11	DIODE PK 2501	1910010	119	2
12		EYELETS FOR HANDLE	906732	120	2
27		SPLIT LUGS	9006735	121	2
1		HANDLE (HEX)	1210711	122	2
2		CRYSTAL SOCKET	1202812	123	2
1		CRYSTAL HOLDER BRKT.	5303154	124	2
1		REAR SUPPORT BRKT.	5302825	125	4
2	W2, W4	INSULATED JUMPER	9009185	126	2
3		SCREWS FOR BRKT. (PAN HEAD)	906001-1	127	2
3		HEX NUTS (2-56)	906555	128	11
4		WIFE, 30 AWG	9105740	129	3

RES 47 1/4W 1% FUSIBLE

RES 7.5K 1/4W 5%

RES 20K 1/4W 5%

RES 100K 1/4W 5%

RES 1.69K 1/8W .1% 25 PPM/°C

RES 1K 1/4W 1% FUSIBLE

RES 750 1/4W 5%

RES 2K 1/4W 5%

RES 910 1/4W 5%

RES 1.2K 1/4W .5% 25 PPM/°C

RES 1.8K 1/4W .1% 25 PPM/°C

RES 3K 1/4W 5%

RES 2.2K 1/4W 5%

RES 560 1/4W 5%

RES 5.6K 1/4W 5%

RES 1K 1/4W .1% 25 PPM/°C

RES 33 1/4W 5%

RES 392 1/4W .1% 25 PPM/°C

RES 15K 1/4W 5%

RES 68 1/4W 5%

RES 422 1/4W 1% 25 PPM/°C

RES 464 1/4W 1% 100 PPM/°C

RES 3K 1/8W .1% 25 PPM/°C

RES 1.21K 1/8W 1% 50 PPM/°C

RES 383 1/8W 1% 100 PPM/°C

RES 178 1/8W 1% 100 PPM/°C

RES 768 1/8W 1% 25 PPM/°C

RES 3.987 1/8W 1% 25 PPM/°C

RES 9.09K 1/8W 1% 25 PPM/°C

FET 2N5460

TRANSISTOR 30099

TRANSISTOR D4506

TRANSISTOR D4403

TRANSISTOR 65340

FET 2N5245

TRANSISTOR 2M4250

THRU Q29, Q33 THRU Q36, Q41 THRU Q45, Q56, Q57, Q61, Q62, Q66, Q67, Q71, Q72, Q74

Q20, Q23, Q37 THRU Q40, Q46, Q47, Q53, Q58, Q63, Q68, Q69, Q73, Q88, Q95

INDUCTOR 100 OH

INDUCTOR .22 OH

CRYSTAL 1 MHZ

IC DEC 8837

IC DEC 8242

IC DEC 8251 B

IC DEC 314

IC DEC 384

IC DEC 8640 (380)

IC DEC 7400

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

IC DEC 7404

digital

AR11

SIZE CODE

CS M7809-0-1

NUMBER

REV. B

digital

AR11

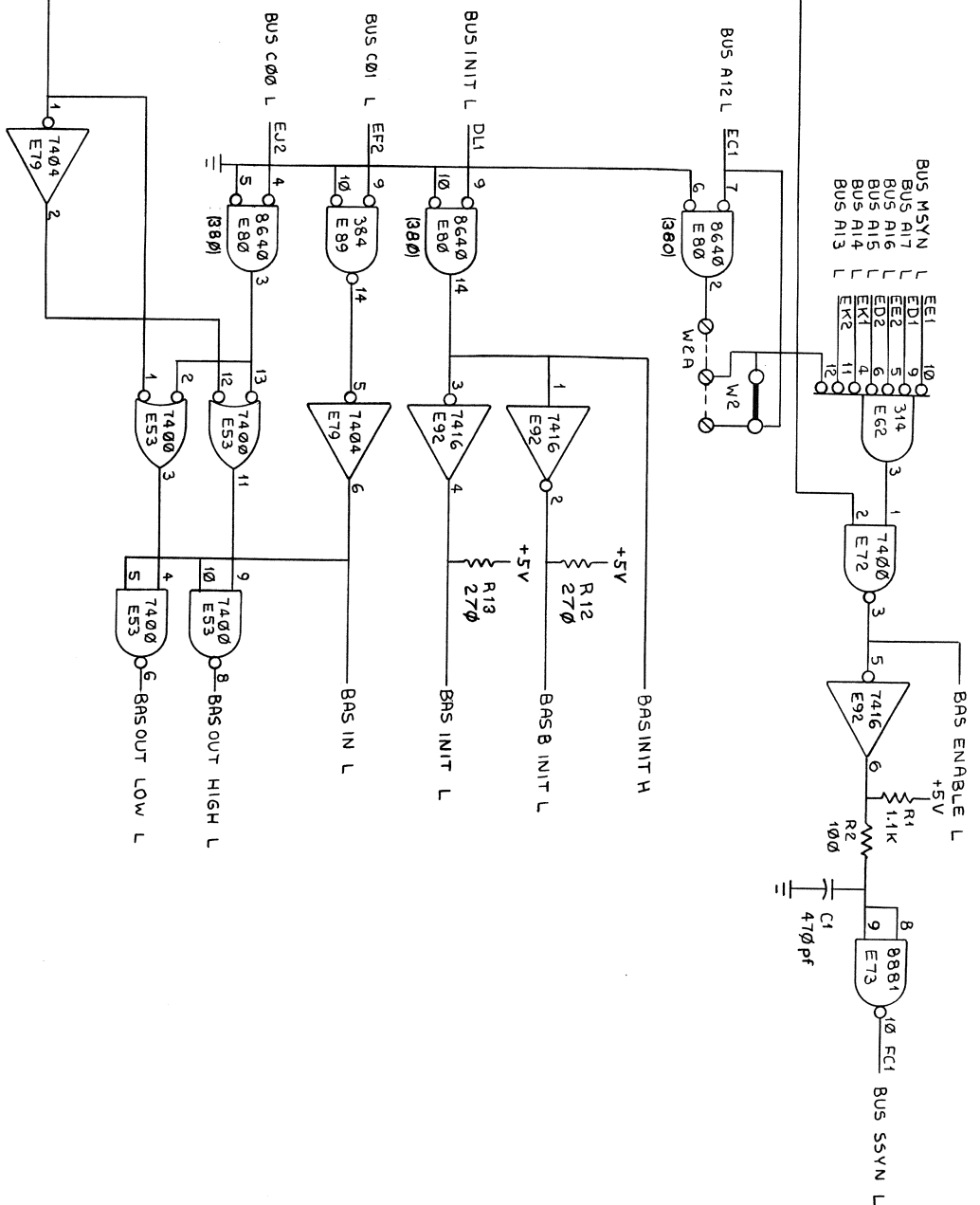
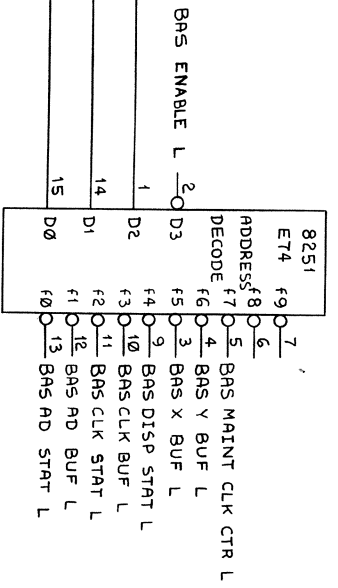
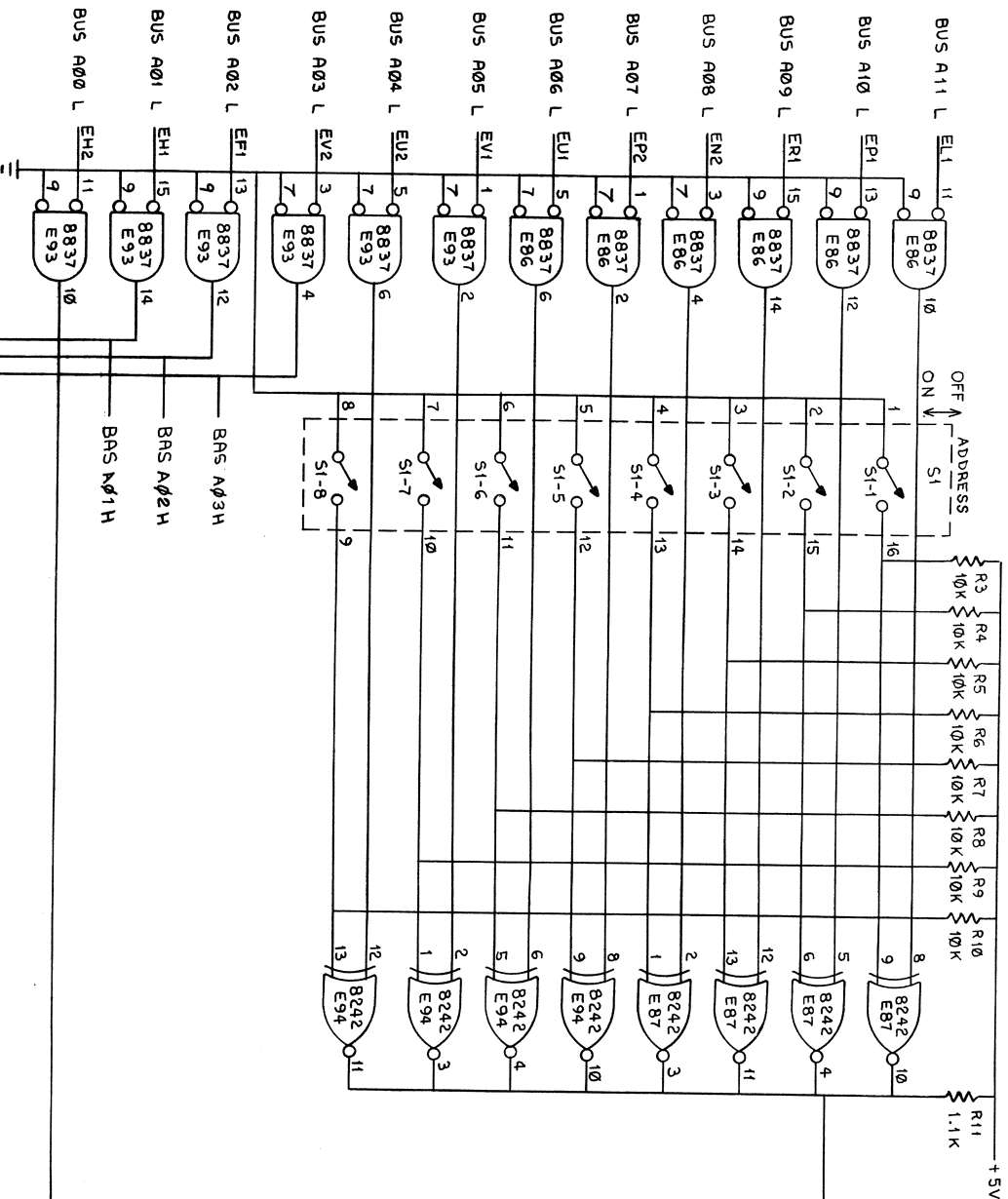
SIZE CODE

CS M7809-0-1

NUMBER

REV. B

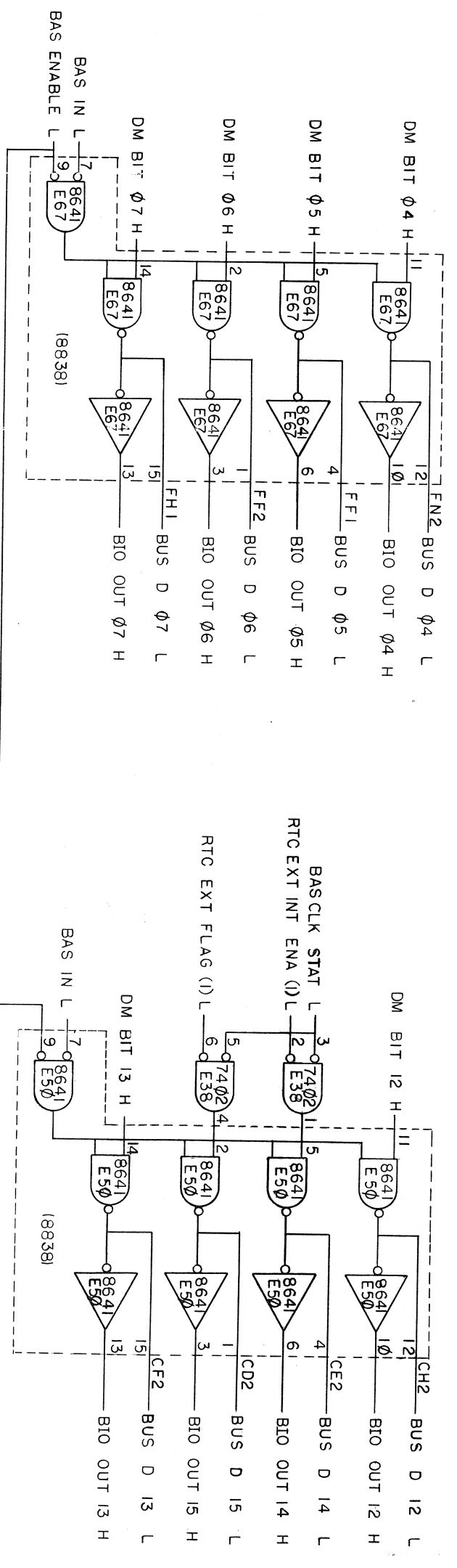
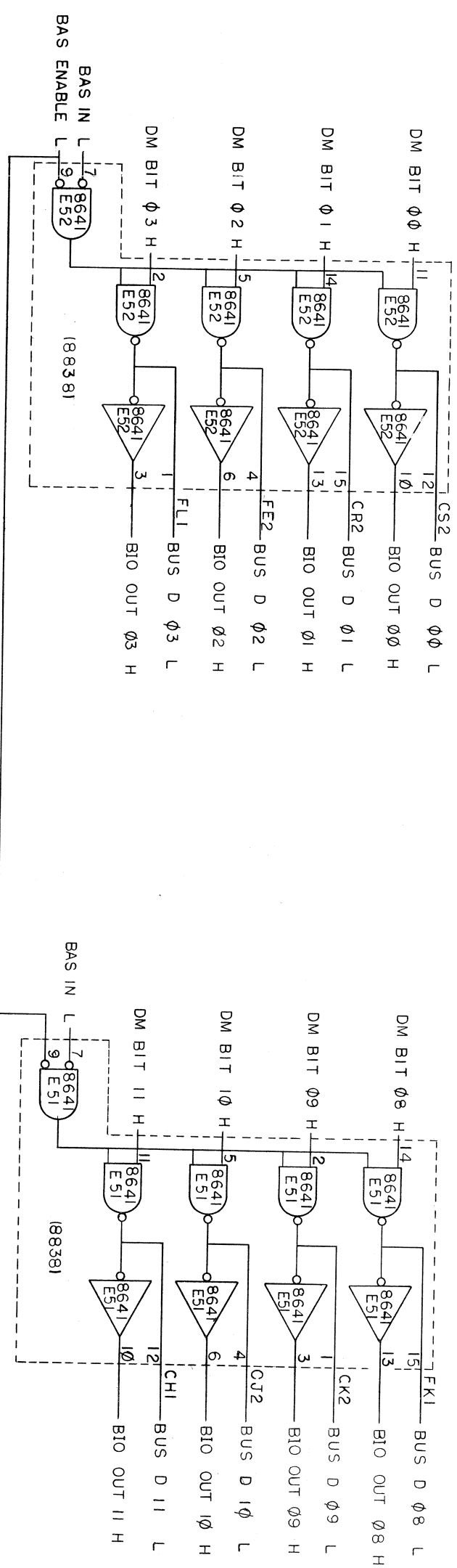
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REVISIONS	
CHK	CHANGE NO.
REV.	

BAS (BUS ADDRESS SELECT)																	
TITLE										SIZE CODE		NUMBER		REV			
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SCALE										NONIE		SHEET		3		OF 16	
										PART							

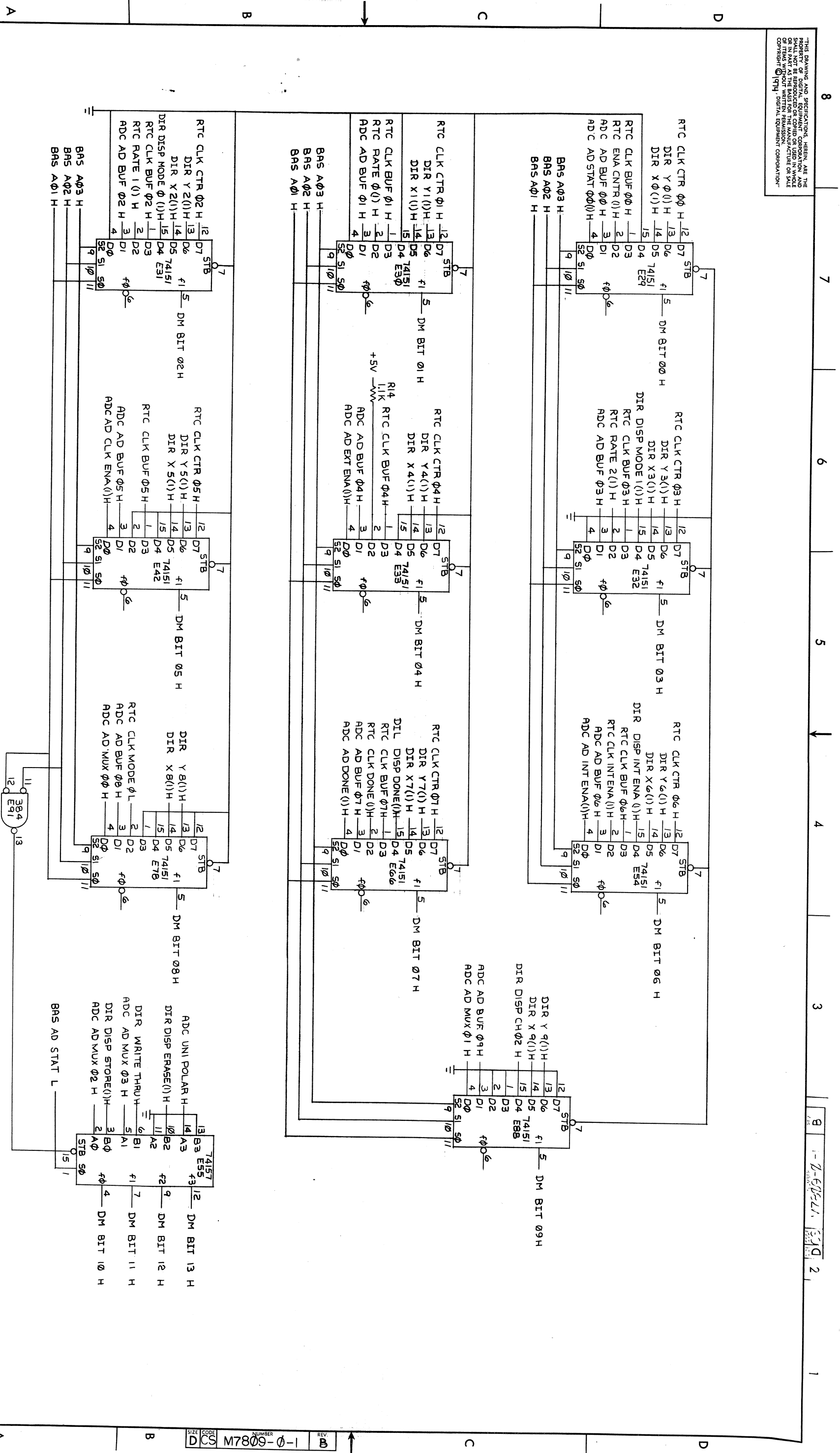
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE		NUMBER		REV.	
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SCALE NONE		SHEET 4 OF 16		DIST.			

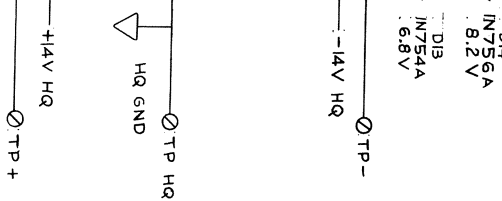
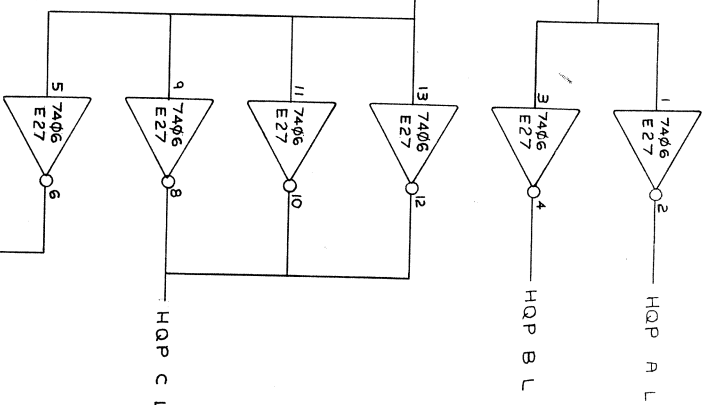
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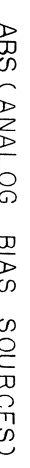






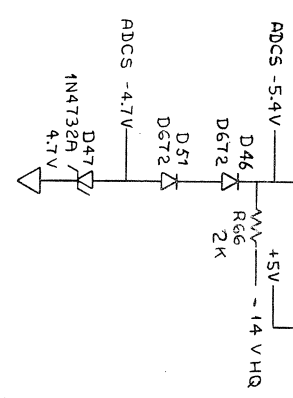
1

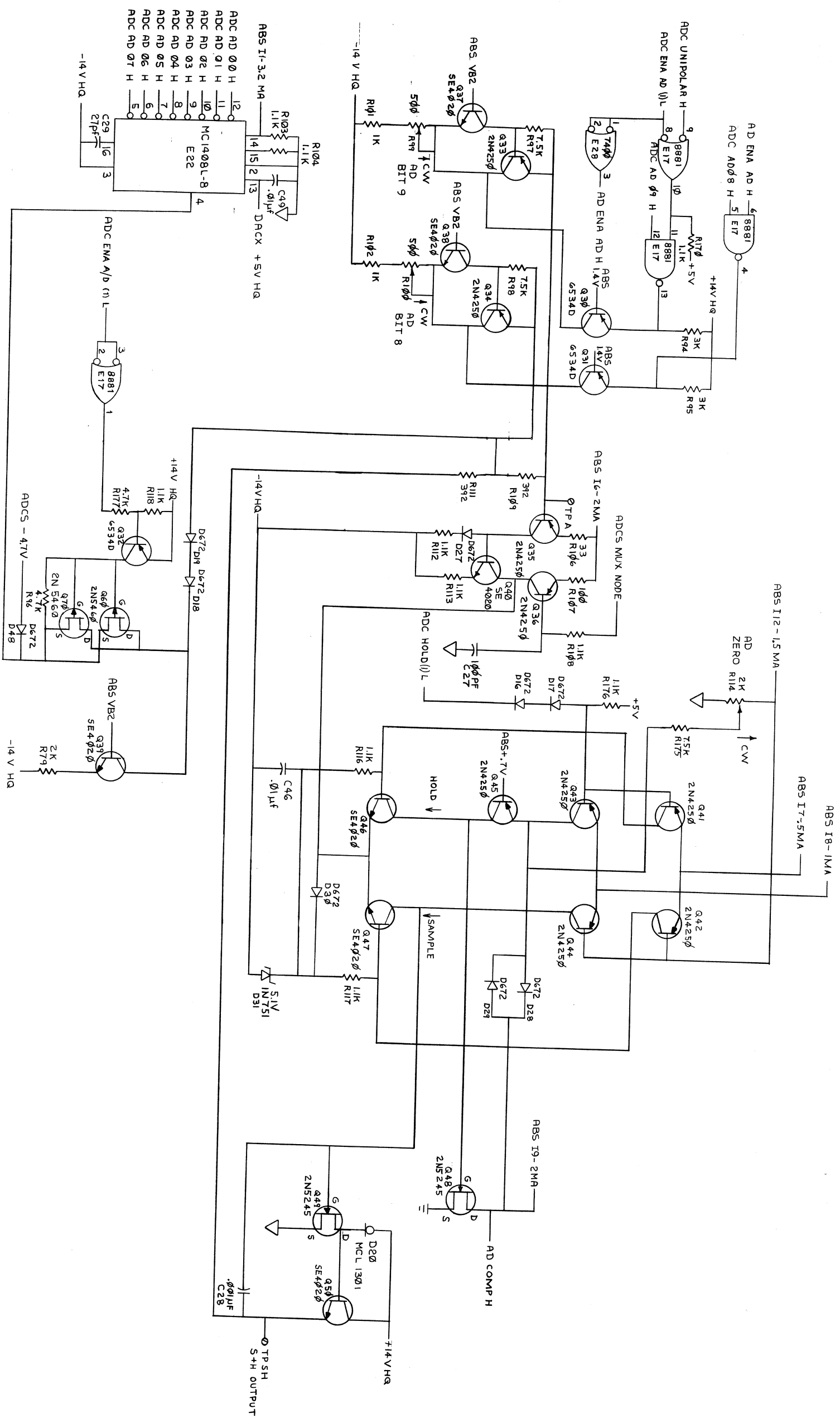
[illegible]

DEC FORM NO. 1

SIZE D	CODE CS	NUMBER M7809-0-1	REV. B
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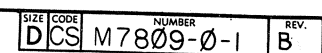


AD (A/D)



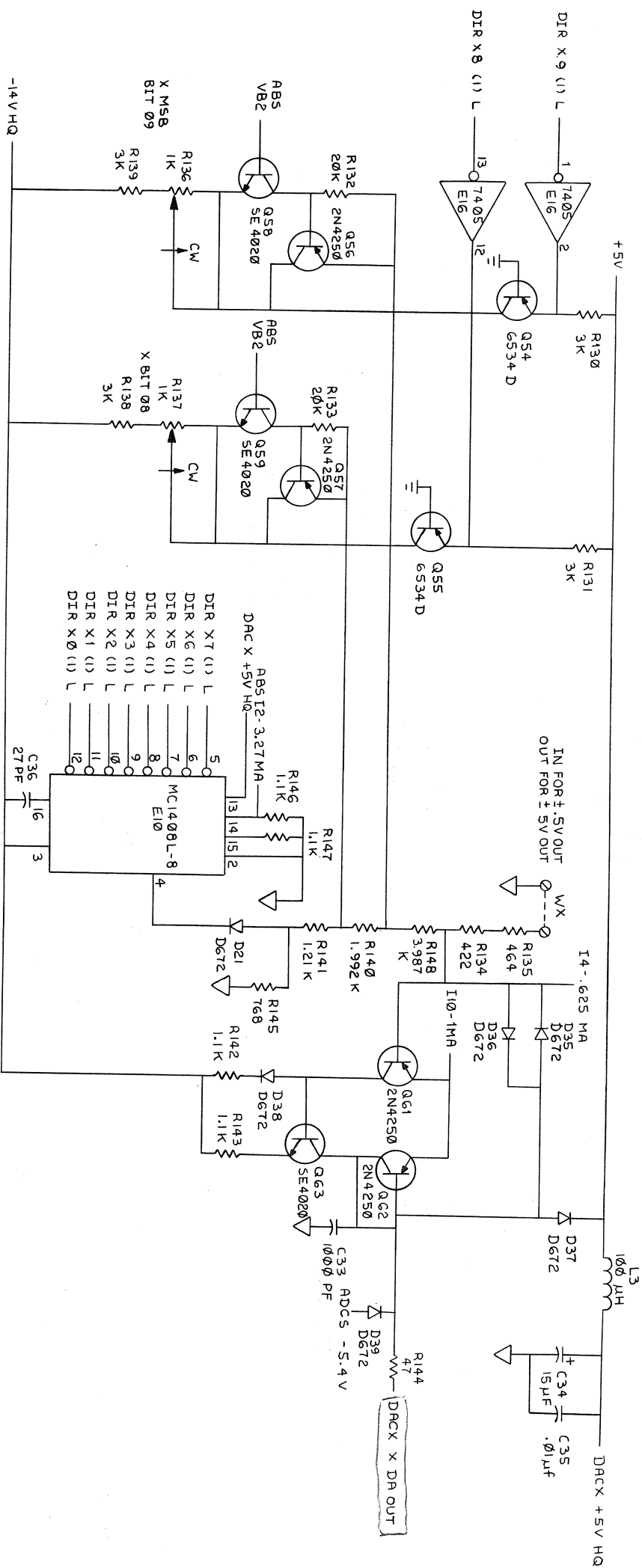
SIZE	CODE	REV.
D	CS	B

2	SIZE CODE	NUMBER	REV.
D	CS	17809-0-1	B



TITLE	SIZE CODE		NUMBER	REV.
AR 11	D	CS	M7809-0-1	B
SCALE	NONE	SHEET	14 OF 16	DIST.

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REVISIONS		
CHK	CHANGE NO.	REV.

8

8

7

6

5

4

3

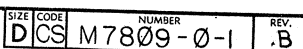
2

1

DACX (D/A CONVERTERS)

TITLE		NUMBER		REV.
AR11		M7809-0-1	B	
SCALE	NONE	SHEET	15 OF 16	
		DIST.		

SIZE	CODE	NUMBER	REV.
D	CS	M7000	0

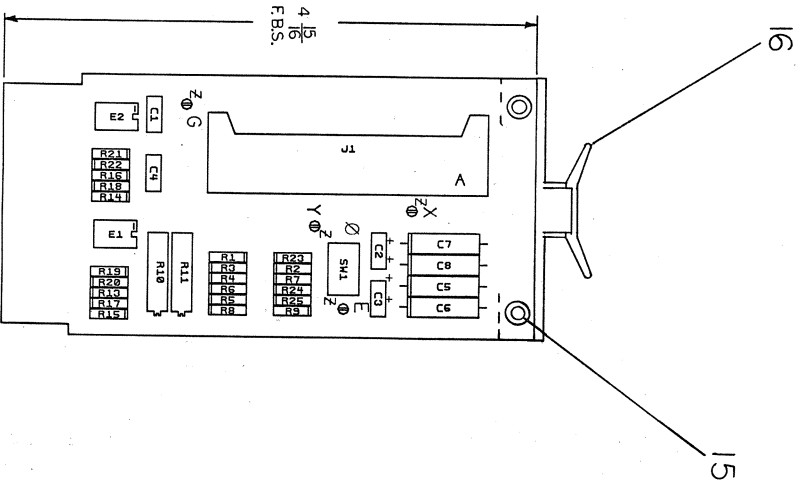


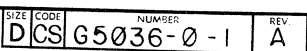
DACY (D/A CONVERTERS)

TITLE		SIZE CODE		NUMBER		REV	
AR11		D CS		M7809-0-1		B	
SCALE	NONE	SHEET	16	OF	16	DIST.	

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NOTES:

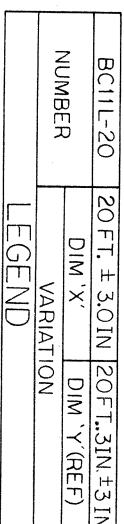




TITLE		SIZE CODE	NUMBER	REV.
WRAP AROUND		D	CS 65236-0-1	A
SCALE	N 1/2" = 1'	SHEET	2 OF 2	DIST.
8 7 6 5 4 3 2 1				

WIRE TABLE (CON'T.)

VIEW A-A
SCALE: NONE
* NOT USED



PARTS LIST			
QTY.	DESCRIPTION	PART NO.	ITEM NO.
38	PIN, BERG (4770c)	1210089-6	2
1	CONN. HOUSING, 40 PIN	1210918-15	1

REVISIONS		
CHK	CHANGE NO.	REV

NOTES:

1. PLACE CABLE TIES APPROXIMATELY EVERY 10 IN. AND WHEREVER INDICATED.
2. USE ITEM #9 (CABLE MARKERS) TO IDENTIFY CABLES BY NUMBER. POSITION APPROXIMATELY 2 FT. FROM EACH END.
3. SHIELD WIRE (FROM #24 TWP) AND BLACK WIRE TO BE CUT APPROXIMATELY .7" FROM CABLE IN SULATION.
4. BLACK WIRE (STRIPPED) AND SHIELD TO BE TWISTED AND SOLDERED TO BLACK IPVC (ITEM #7, APPROXIMATELY 12" LG).

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 9/26/74

TITLE	AR11	System Installation/Acceptance Procedure
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REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

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TITLE
AR11 System Installation/Acceptance Procedure

1.0 SCOPE

This procedure covers the installation and acceptance of an AR11 in a PDP11 system. It is anticipated that the procedure will be used in one of the following situations:

- 1.1 Installation and acceptance of an AR11 on a PDP11 system in an in-house FA & T system integration area.
 - 1.2 Add-on installation and acceptance of an AR11 on an existing PDP11 system in the field.
 - 1.3 Acceptance of an AR11 on a new PDP11 system upon installation at a customer site.
 - 1.4 On-going AR11 verification testing at intervals over the life of a given system.
- 2.0 AR11 MOUNTING/CONFIGURATION CONSIDERATIONS
- 2.1 The AR11 is a one-module option which interfaces with a PDP11 through a hex SPC slot. A hex SPC slot is one of the following:
 - 2.1.1 One of the two middle slots of a DD11-B, C or E four-slot prewired system unit.
 - 2.1.2 One of the seven middle slots of a DD11-D or F nine-slot prewired double system unit.
 - 2.1.3 Any processor-mounted SPC slot with physical room for a hex module.

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TITLE AR11 System Installation/Acceptance Procedure					
2.2 The AR11 may be mounted in any hex SPC slot and will operate within specification with no configuration restrictions whatsoever regarding physical proximity to processor, memory, or other options.					
AR11 analog performance may be further optimized beyond specification levels by mounting in an electrically quiet environment. Consequently, if a choice is available in configuring a system, the AR11 should be mounted away from the processor and memory modules.					
2.3 Cabling					
The AR11 is interfaced to the outside world by means of either a BC08-R flat cable to an H322 distribution panel, a BC11-L Berg-to-open end cable, or a user-built cable. In either of the latter two cases, in a 10½" or 5¼" mounting box, the next slot (on the component side of the AR11) should not contain another hex SPC module, in order to leave room for the AR11 cable to double back and exit past the top of the module.					
2.4 Bus Addresses					
The AR11 starting address may be set at any address between 7600000 and 7777600 (in increments of 20) by means of a jumper and switches on the module. The preferred starting address is 7704000.					
Use of any other starting address will necessitate patches to the AR11 diagnostics, as well as to system software (such as RT-11 lab applications and SPARTA) which supports the AR11. The AR11 diagnostics (Test I - logic and Test IIT - wraparound) support multiple					
SIZE		CODE	NUMBER	REV	
A		SP	AR11-0-4		

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE AR11 System Installation/Acceptance Procedure					
AR11's automatically, provided that the AR11's occupy a sequential block of addresses 20 apart, and provided that the address following the last AR11 is unused. For example, in a system with a single AR11 at 7704000, the address 7704200 should not be used; a system with three AR11's should have the AR11's at 7704000, 7704200 and 7704400, with the address 7704600 unused. If, in configuring a system, it is necessary to use the address which is 20 higher than the last AR11 address, patches will be necessary to diagnostics Test I and Test IIT, and these diagnostics will then test only one AR11 at a time. (See section 4 for patches)					
2.5 Vectors					
The AR11 vector space may start in increments of 20 up to a maximum of 760 by means of switches on the module. The preferred vector is 340. Use of any other vector will necessitate patches to the AR11 diagnostics, as well as to system software which supports the AR11. For AR11 diagnostics Test I and Test IIT to work properly with multiple AR11's in a system, the AR11 vectors should be in sequential order, 20 apart. For example, in a system with three AR11's at 7704000, 7704200, and 7704400, the vectors should be 340, 360 and 400 respectively.					
3.0 AR11 INSTALLATION					
3.1 Based on the above considerations, choose a hex SPC mounting slot, starting address, and vector for the AR11 to be installed.					
SIZE		CODE	NUMBER	REV	
A		SP	AR11-0-4		

TITLE AR11 System Installation/Acceptance Procedure

3.2 Set up the starting address in the following manner:

3.2.1 For addresses between 770000 and 77776, leave W4 connected. For addresses between 760000 and 76776, disconnect W4 and connect W4A.

3.2.2 Set up address switches (S1) per figure 1 and figure 2. Switches are set "on" for a 0 and "off" for a 1.

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	X	X	X	X	X	X	X	X	X	0	0	0	0	0
ex:	7				7									4				

jumper

switch selectable

Figure 1: AR11 Address Selection

3.3.3 Example

To set up starting address 770400, leave W4 connected, set all S1 switches "on" except for the bit 8 switch.

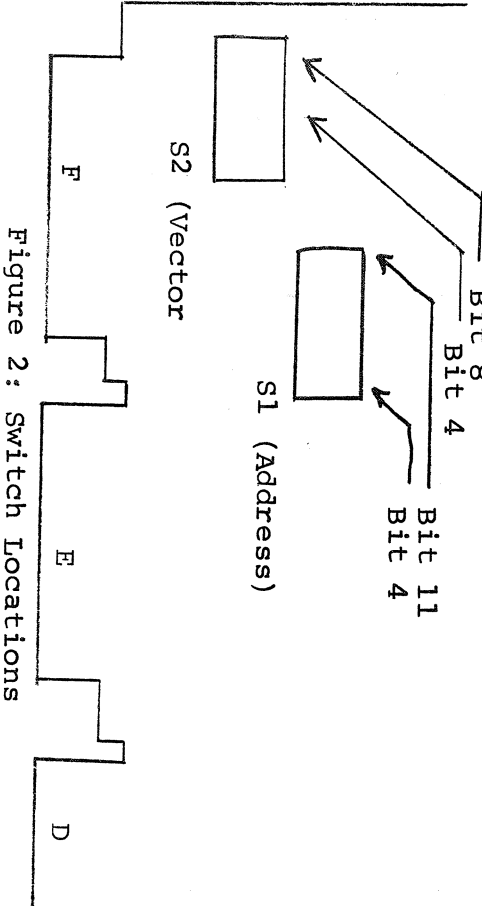


Figure 2: Switch Locations

TITLE AR11 System Installation/Acceptance Procedure

3.3 Set up the vector in the following manner:

3.3.1 Set up vector switches (S2) per figure 2 and figure 3. Switches are set "on" for a 1 and "off" for a 0. (Note that this is opposite to the address switches.)

8	7	6	5	4	3	2	1	0

Switch selectable

00 = A/D interrupt
01 = Clock interrupt
10 = Display interrupt

Figure 3: AR11 Vector Selection

3.3.2 Example

To set up a vector of 340, the bit 7, 6, and 5 switches are "on" and the bit 8 and 4 switches are "off".

3.4 Re-install the covers on switch-packs S1 and S2.

3.5 Install the module in the selected hex SPC slot.

3.6 If the system contains an H322 signal distribution panel, connect the AR11 and H322 by means of a BC08-R Berg-to-Berg cable.

If the system includes a BC11-L Berg-to-Berg end cable, do not install the cable at this time. Instead, install the BC08-R cable which is to be used with the G5036 wraparound module for acceptance testing. The BC11-L is to be installed upon completion of acceptance testing.

3.7 Install the 17-00021 electromagnetic shields on both sides of the AR11.

SIZE	CODE	NUMBER	REV
A	SP	AR11-0-4	

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CONTINUATION SHEET

TITLE AR11 System Installation/Acceptance Procedure

3.8 Conduct an acceptance test per section 4 below.

4.0 AR11 ACCEPTANCE

4.1 Test Flow

AR11 acceptance testing flow is shown in figure 4.

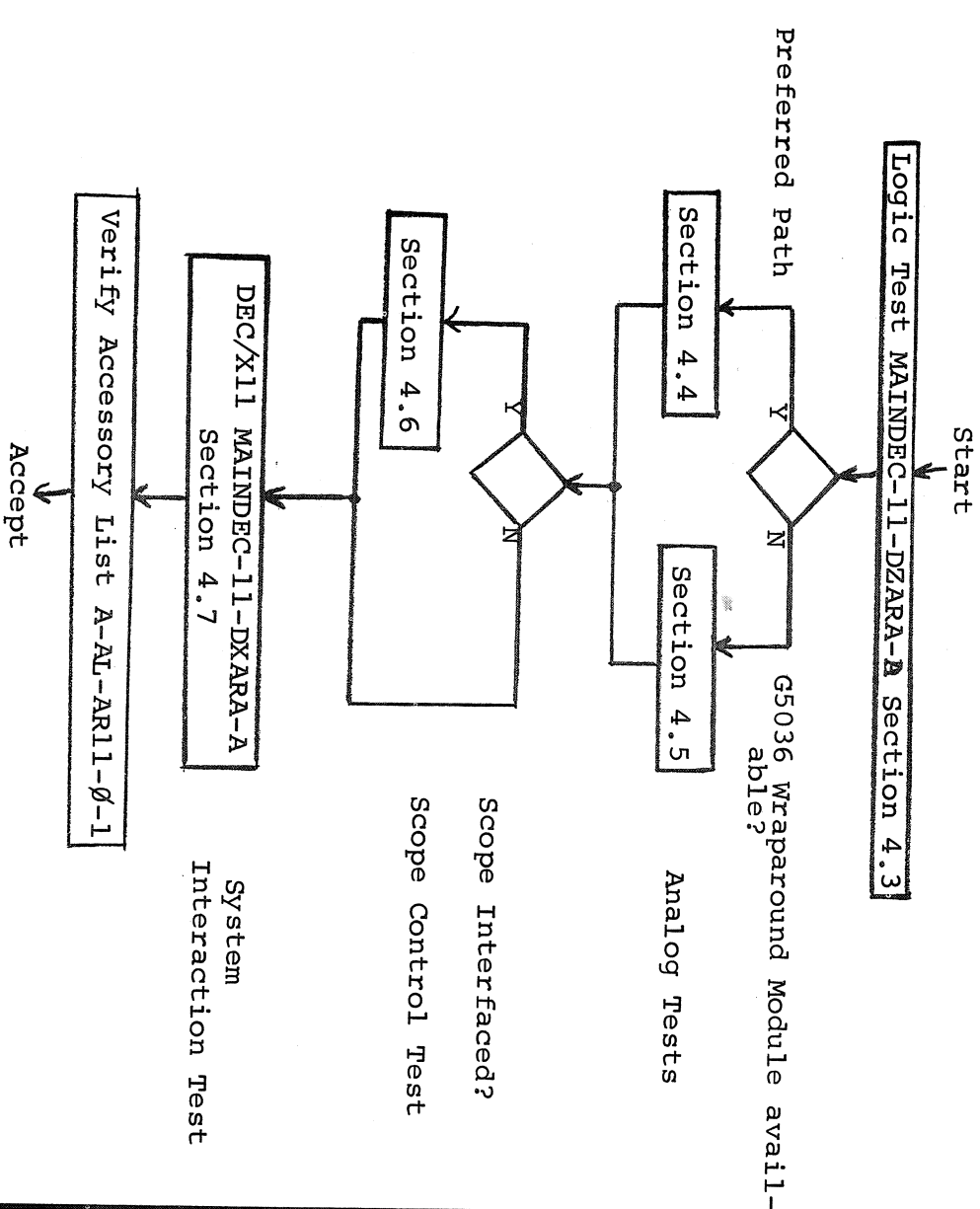


Figure 4: AR11 Acceptance Flow

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CONTINUATION SHEET

TITLE AR11 System Installation/Acceptance Procedure

In every case, AR11 acceptance begins with a complete test of the AR11 logic, described in section 4.3 below.

If a G5036 wraparound module is available, the preferred path is taken for analog testing, described in section 4.4 below. This is the normal path taken for in-house acceptance, field installation acceptance, and on-going AR11 analog verification testing by field service personnel and by users who have purchased the BG5036 maintenance kit. The analog testing path described in section 4.5 below is for on-going AR11 analog verification testing by users who have not purchased the BG5036 maintenance kit.

The scope control test, described in section 4.6, is to be run on those systems in which the AR11 is interfaced to an XY display scope or storage scope.

The DEC/X11 system interaction test, described in section 4.7, is to be run on all systems with AR11. The AR11 DEC/X11 module tests for the presence of the wraparound module and chooses one of two routines accordingly. If the G5036 wraparound module is available, it should be connected to the AR11 during DEC/X11 testing. However, DEC/X11 can be run without the wraparound module without sacrificing validity, by users who have not purchased the BG5036 maintenance kit.

4.2 Equipment and Diagnostics Required

4.2.1 PDP11 system, with AR11 and console device.

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TITLE AR11 System Installation/Acceptance Procedure

4.2.2 Calibrated DC Voltage Source EDC model MV116 or equivalent.

4.2.3 BG5036 maintenance kit: *

4.2.3.1 G5036 wraparound module

4.2.3.2 BC08-R Berg-to-Berg cable

4.2.4 MAINDEC-11-DZARA-A AR11 Test I (logic)

4.2.5 MAINDEC-11-DZARB-A AR11 Test II (analog)

4.2.6 MAINDEC-11-DZARC-A AR11 Test III (wraparound) *

4.2.7 MAINDEC-11-DXARA-A AR11 DEC/X11 module

*Not required for user's on-going verification testing

4.3 Logic Test

Load and run the logic test diagnostic MAINDEC-11-DZARA-A.

Under the following conditions, no patches are required: First (or only) AR11 at address 770400, vector at 340; additional AR11 addresses and vectors 20 apart and sequential, e.g. 770420 and 360, 770440 and 400, etc; address 20 higher than last AR11 address unused, e.g. 770420 in system with one AR11, 770460 in system with three AR11's. Otherwise, patch:

- 1360/ AR11 starting address (first AR11)
- 1362/ AR11 vector (first AR11)
- 1526/ 5003 ; inhibit testing more than one AR11.

Without patch (c), the diagnostic automatically tests all

the AR11's installed in the system (with sequential addresses 20

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TITLE AR11 System Installation/Acceptance Procedure

apart) in each pass. The diagnostic must complete at least three passes without error with iterations or ten passes without error without iterations (SW11 = 1).

4.4 Analog Tests (using G5036 wraparound module)

4.4.1 For each AR11 in the system connect the AR11 to a G5036 wraparound module by means of a BC08-R Berg-to-Berg cables. For AR11's which are interfaced to H322 signal distribution panels, the BC08-R cable which normally connects to the H322 should be disconnected from the H322 and connected to the G5036. For AR11's without an H322, the BC08-R cable should come out of the processor box and cabinet. Maximum BC08-R cable length should be 12 feet.

*Important Note: The BC08-R cable should be connected "upside-down" at the G5036 end, i.e. A to VV rather than A to A.

4.4.2 Set the switch on the G5036 module to the "E" position. Connect the EDC voltage source signal output to the "E" split lug on the G5036. Connect the EDC voltage source return to the "G" split lug on the G5036. The EDC should be floating to avoid ground loops. The EDC leads should be short and shielded if possible. The EDC output is now connected to the AR11 A/D channel 0 input.

4.4.3 Load the analog test diagnostic MAINDEC-11-DZARB-A.

This diagnostic only tests one AR11 at a time. For an AR11 at address 770400 and vector 340, no patches are needed.

SIZE	CODE	NUMBER	REV
A	SP	AR11-0-4	

SIZE	CODE	NUMBER	REV
A	SP	AR11-0-4	

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TITLE AR11 System Installation/Acceptance Procedure			
Otherwise, patch: a) 12Ø4/ AR11 starting address b) 12Ø6/ AR11 vector Start the program at location 2ØØ, select Test C (calibration test), and when requested, type 'I' for internal A/D starts. Set SW1Ø = 1 to force console printout of the converted value. Select channel Ø bipolar by leaving all other front console switches at Ø. Set up the EDC for the input voltage indicated in column A and monitor the conversion result. It should be the value in column B, with a <u>+1</u> tolerance. A B -1.875 Volts Ø2ØØ +1 0 1ØØØ +1 +1.875 Volts 16ØØ +1 4.4.4 Set the switch on the G5036 module back to the "Ø" position. The AR11 A/D channel Ø input now sees a ground, the desired input for wraparound testing. The EDC may now be disconnected. 4.4.5 Load and run the wraparound diagnostic MAINDEC-11-DZARC-A. No patches are required if the following conditions are met: First (or only) AR11 at address 77Ø4ØØ, vector at 34Ø; additional AR11 addresses and vectors 2Ø apart and sequential, e.g. 77Ø42Ø and 36Ø, 77Ø44Ø and 4ØØ, etc.; address 2Ø higher than			

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE AR11 System Installation/Acceptance Procedure			
last AR11 address unused, e.g. 77Ø42Ø in systems with one AR11, 77Ø46Ø in system with three AR11's. Otherwise, patch: a) 1334 / AR11 starting address (first AR11) b) 1336 / AR11 vector (first AR11) c) 145Ø / 5ØØ3 ; inhibit testing more than one AR11. Without patch (c), the diagnostic automatically tests all the AR11's installed in the system (with sequential addresses 2Ø apart) in each pass. The diagnostic must complete at least two passes without error. The wraparound diagnostic tests the following: a) Scope intensify pulse, A/D external start b) Storage scope hand-shaking logic-erase return, etc. c) Scope control output logic high and low levels d) Analog power supply levels e) Functional check on all 16 channels of A/D input f) A/D input bias current g) Calibration of XD/A vs. A/D, YD/A vs. A/D h) Linearity of XD/A vs. A/D, YD/A vs. A/D i) Differential Linearity of A/D, XD/A, YD/A j) A/D inter-channel settling, plus full-scale and minus full-scale k) Noise levels - rms and peak - A/D bipolar, A/D unipolar, XD/A, YD/A			

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TITLE ARI1 System Installation/Acceptance Procedure

- 1) Offset - A/D bipolar, A/D unipolar, XD/A, YD/A

Numerical results of the above tests can be printed out, for the edification of the test operator, by setting front console SW12 = 1.

4.5 Non-wraparound Analog Tests

This section may be performed in lieu of section 4.4 for on-going ARI1 analog verification testing by users who have not purchased the BG5036 maintenance kit.

4.5.1 Load the analog test diagnostic MAINDEC-11-DZARB-A.

This diagnostic tests only ~~one~~ ARI1 at a time. For an ARI1 at address 770400 and vector 340, no patches are needed.

Otherwise, patch:

- a) 1204 / ARI1 starting address
b) 1206 / ARI1 vector

4.5.2 A/D Calibration and Linearity

Start the program at location 200, select Test C (calibration test), and when requested, type 'I' for internal A/D starts. If the ARI1 is interfaced to a scope, the results will appear on the screen. If the ARI1 is not interfaced to a scope, set front console SW10 = 1 to force console printout of the converted values.

Connect the EDC output to the input of the A/D channel

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TITLE ARI1 System Installation/Acceptance Procedure

to be tested. Connect the EDC return to one of the A/D input grounds. The EDC should be floating to avoid ground loops. The EDC leads should be short and shielded if possible. Select the desired A/D input channel using front console SW03:SW00.

Set up the EDC for each input voltage indicated in column A and monitor the conversion result. It should be the value in column B, with a ± 1 tolerance.

A	B	C
-2.500 Volts	0000 ± 1	0
-1.875 Volts	0200 ± 1	+ .625 Volts
-1.250 Volts	0400 ± 1	+1.250 Volts
-.625 Volts	0600 ± 1	+1.875 Volts
0	1000 ± 1	+2.500 Volts
+ .625 Volts	1200 ± 1	+3.125 Volts
+1.250 Volts	1400 ± 1	+3.750 Volts
+1.875 Volts	1600 ± 1	+4.375 Volts

Set front console SW05 = 1, for unipolar input range.

Set up the EDC for each input voltage indicated in column C and monitor the conversion result. It should be the value in column B, with a ± 1 tolerance.

4.5.3 A/D Noise

The ARI1 A/D's noise level can be measured in one of two manners. Each involves a burst of 512 conversions. If the average of the 512 conversions is centered within a nominal-width (1 LSB) state, the "tails" of the noise distribution can be observed in the (average +1) and (average -1) states. For

SIZE	CODE	NUMBER	REV
A	SP	ARI1-0-4	

SIZE	CODE	NUMBER	REV
A	SP	ARI1-0-4	

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TITLE AR11 System Installation/Acceptance Procedure

rms noise levels less than the $\frac{1}{4}$ LSB spec, at least 490 conversions are in the center (average) state.

4.5.3.1 The first method of noise measurement can only be done when the AR11 is interfaced to an oscilloscope. Using this method, it is easy to center the EDC voltage within a single state, but it is necessary to count the number of conversions in the (average +1) and (average -1) states.

Select Test C (calibration test), and when requested, type 'I' for internal A/D starts. Select the desired A/D input channel using front console SW $\emptyset$ 3: $\emptyset\emptyset$. Connect the EDC output to the input of the channel being tested as in section 4.5.2 above. A burst of 512 conversion is displayed across the screen, with four ± 8 LSB "markers" superimposed on the trace. Adjust the EDC voltage so that the trace is exactly centered within a state (equal number of plus and minus "glitches"). At this input voltage, set SW $\emptyset$ 6 = 1, to discontinue sampling and freeze the last 512-point burst on the screen. Count the number of conversions in the (average +1) and (average -1) states. This number should be less than 22_{10} , i.e. there must be at least 490 conversions in the center state.

4.5.3.2 The second method of noise measurement does not

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TITLE AR11 System Installation/Acceptance Procedure

require the AR11 to be interfaced to a scope.

Select Test D (repeatability test), and when requested, select the desired channel, and select a count spread of $\emptyset$, to force printouts of all distributions. Connect the EDC to the desired channel as in section 4.5.2 above. Observe the distributions printed out, and adjust the EDC voltage such that the distribution is centered in the "Av" state, with equal numbers of conversions in the "+1" and "-1" columns. The number in the "Av" column must be 490 or greater.

4.5.4 Inter-channel Settling

Inter-channel settling is tested by connecting two voltages which are at opposite ends of the A/D input range to two different channels. For example, connect -2.4 Volts to the channel $\emptyset$ input and +2.4 Volts to the channel 1 input and run with bipolar input range (± 2.5 Volts) by selecting channels $\emptyset$ and 1, or connect +1 Volts to the channel $\emptyset$ input and +4.9 Volts to the channel 1 input and run with unipolar input range (0 to +5 Volts) by selecting channels 4 $\emptyset$ and 41. In the following description, it is assumed that -2.4 Volts and +2.4 Volts are connected to channels $\emptyset$ and 1.

Select Test E (recovery test), and when requested, type " $\emptyset$, 1" for the positive settling test and "1, $\emptyset$ " for the negative settling test. A series of eight conversion values is

SIZE	CODE	NUMBER	REV
A	SP	AR11- $\emptyset$ -4	

SIZE	CODE	NUMBER	REV
A	SP	AR11- $\emptyset$ -4	

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then typed out. In each case, the first value typed out should be within one count of the average of the remaining seven values. (If the remaining seven values are on the borderline between two states, change the input voltage by 2.5 mV and repeat the test.) 4.6 Scope Control Test This test is done only if the AR11 is interfaced to an oscilloscope. The analog test diagnostic MAINDEC-11-DZARB-A must be loaded (and patched for proper address and vector if necessary) per section 4.5.1 above. Select Test B (display). The program will loop through the following eight "pictures": horizontal line, vertical line, square, X, settling test square wave, character set, channel 1 - channel 2, descending horizontal line. Observe these pictures for linearity, dot spacing, and lack of noise or jitter. Set SW08 = 1 to select a fixed "picture". Set SW02 = 1 to select the settling test square wave. With SW07 = 0 observe settling in the horizontal direction; with SW07 = 1 observe settling in the vertical direction. Maximum settling error should be "1 dot". If the scope which is interfaced to the AR11 is a VR14, with SW08 = 1, set SW02:00 = 6. With the VR14 switched to "both", "Channel 1" and "Channel 2" should appear on the screen. With the					
SIZE	CODE	NUMBER	REV		
A	SP	AR11-0-4			

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TITLE AR11 System Installation/Acceptance Procedure					
VR14 switched to "channel 1", "Channel 1" should appear on the screen; likewise for "channel 2". 4.7 DEC/X11 System Integration Test The system exerciser is configured using the AR11 exerciser module MAINDEC-11-DXARA-A along with modules for all other options present. The G5036 wraparound module should be installed per section 4.4.1 above. The AR11 exerciser measures (and compares to spec limits) rms and peak noise levels on A/D, X D/A, and Y D/A. All A/D conversions are started on clock overflow after a random number has been loaded into the clock buffer register. Since the system is being exercised in the background at the time the A/D conversions start, the noise levels measured are true worst case levels, under conditions of full system interaction. For purposes of on-going verification testing by a user who has not purchased the BG5036 maintenance kit, the DEC/X11 module may be run without wraparound. Under this condition, the program senses the absence of the G5036 wraparound module and goes to a routine which takes conversionson each of the 16 channels and displays them on the screen of the scope driven by the AR11. Each channel is displayed in turn for about three seconds. 5.0 AFTER ACCEPTANCE 5.1 Remove the G5036 wraparound module. It is not shipped with the AR11.					
SIZE	CODE	NUMBER	REV		
A	SP	AR11-0-4			

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TITLE AR11 System Installation/Acceptance Procedure

5.2 If the system includes an H322 signal distribution panel, reconnect the BC08-R cable to the H322. If the system does not include an H322, remove the BC08-R cable. It is not shipped.

5.3 If the system includes a BC11-L cable, it should be installed at this time. If the AR11 is in a new version 10½" or 5¼" mounting box, so that the BC11-L cable cannot go straight out the back, the BC11-L cable must double back and exit past the top of the module.

5.4 Verify that all items on the AR11 accessory list A-AL-AR11-Ø-1 are present and properly packed for shipment.

				SIZE	CODE	NUMBER	REV
				A	SP	AR11-Ø-4	

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 9/16/74

TITLE AR11 Circuit Description

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	DATE	SIZE	CODE	NUMBER	REV
		A	SP	AR11-0-5	

ENGINEERING SPECIFICATION



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TITLE AR11 Circuit Description

1.0 INTRODUCTION

1.1 The AR11 is a one-module real-time analog subsystem that interfaces with the PDP-11 family of computers via a hex SPC slot.

Included on the AR11 module are the following:

- 1.1.1 Bus Control, with switch-selectable address.
- 1.1.2 Interrupt Control, with switch-selectable vector.
- 1.1.3 A/D Converter, with 16-channel multiplexer and sample-and-hold.
- 1.1.4 Real-time Clock, with five crystal-based frequencies, external input, and an 8-bit counter.
- 1.1.5 Display Control, with two 10-bit D/A converters.
- 1.1.6 Analog Power Supply.

1.2 The following material should be referenced when using this document:

- 1.2.1 M7809 (AR11) circuit schematics D-CS-M7809-0-1.
- 1.2.2 AR11 User's Guide DEC-11-HARUG-A-D
- 1.2.3 PDP11 Processor Handbook
- 1.2.4 Manufacturer's manual for XY display scope or storage scope being used with the AR11.

1.3 Reading M7809 Prints

At the bottom right corner of each M7809 circuit schematic page is the page title, e.g. BAS (BUS ADDRESS SELECT). The symbol preceding the parentheses is the page mnemonic. Each

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A	SP	AR11-0-5	

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TITLE AR11 Circuit Description

signal generated on a given page has that page's mnemonic in front of it for page cross-reference purposes. For example, BAS ENABLE L originates on the BUS ADDRESS SELECT page, and is low when ENABLE is asserted.

2.0 BUS CONTROL

The AR11 Bus Control consists of BAS (BUS ADDRESS SELECT), BIO (BUS IN/OUT) and DM (DATA IN MULTIPLEXERS), pages 3, 4 and 5 of the M7809 schematics.

2.1 Bus Address Select

The purpose of the bus address select logic is to recognize one of the eight AR11 register addresses on the Unibus address lines, select the register for input or output data transfer upon receipt of MSYN L from the processor, and to acknowledge receipt of MSYN L by sending SSYN L back to the processor.

BUS address lines A17 L through A04 L are used to recognize that one of eight AR11 registers is being addressed. Bus address lines A03 L through A01 L are decoded to determine which of these eight registers is being addressed. BUS A00 L is used to determine high or low byte within the word, in conjunction with BUS C00 L, which is low for a computer output byte operation and high for an output word operation.

BUS A11 L through A04 L are compared with the state of the address select switches using "exclusive or" circuits E87 and E94.

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TITLE AR11 Circuit Description

The "exclusive or" output is high when A11 through A04 match the switch address. When this occurs, and the E62-3 output is high, the AR11 has recognized its address, and BAS ENABLE L is asserted. The E62-3 output is high with BUS MSYN L asserted and 77XXXX (W2 connected) or 76XXXX (W2A connected) on the bus address lines. Thus, as a function of the address switches, the AR11 can have any address from 760000 through 767760 with W2A connected and from 770000 through 777760 with W2 connected.

AR11 address selection is further illustrated in figure 1:

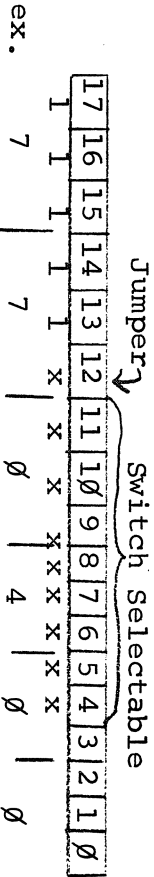


Figure 1: AR11 Address Selection

Location of the address switches on the module is shown in figure 2. The switches are set "on" for a 0 and "off" for a 1, i.e. to set up 770400, all switches are "on" except for the bit 8 switch.

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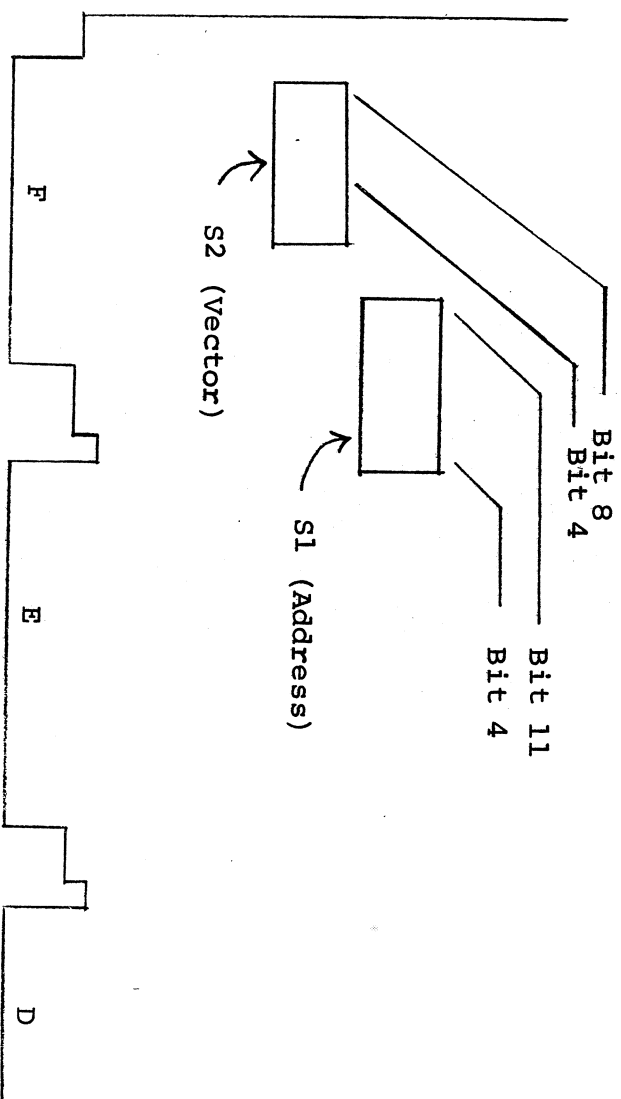


Figure 2: Switch Location

When BAS ENABLE L is asserted, the address decoder E74 is enabled. As a function of address lines BAS A03H through BAS A01H, E74 selects one of the eight AR11 registers and asserts the corresponding select line, per Table 1.

After a delay of approximately 75 nsec, determined by the (R1 + R2) C1 time constant, BAS ENABLE L causes the slave synch line SSVN L to be asserted, informing the processor that the selected data has been received or is present on the data lines.

BUS INIT L is buffered to produce BAS INIT L, BAS B INIT L, and BAS INIT H, which clear all the registers and flags, with the exception of the scope control ready flag. The INIT signal occurs

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on start key depression, power up, or RESET instruction.

TABLE 1: REGISTER ADDRESSES

A03 H	A02 H	A01 H	Address Selected
L	L	L	A/D Status
L	L	H	A/D Buffer
L	H	L	Clock Status
L	H	H	Clock Preset Buffer
H	L	L	Display Status
H	L	H	X Buffer
H	H	L	Y Buffer
H	H	H	Clock Counter

2.2 Bus In/Out

The Unibus has bidirectional data paths, which are interfaced to the AR11 using 8641 (8838) receiver/transmitter chips. The outputs of the data multiplexers (DM BIT 00 H, DM BIT 01 H, etc.) are impressed on the Unibus data lines (BUS D00 L, BUS D01 L, etc.) for computer input operations. This occurs when BAS IN L and BAS ENABLE L are asserted, signifying an input operation when the AR11 has recognized its address.

The data lines enter the AR11 from the Unibus through the inverters, and become the BIO OUT XX H signals.

2.3 Data In Multiplexers

The DATA IN MULTIPLEXERS use 74151 and 74157 multiplexer chips to sort out the data from the eight different registers. The selected register outputs become the DM BIT XX H signals, which are passed on to the Unibus by the BUS IN/OUT logic.

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A03 H, A02 H and A01 H are used as address inputs by the 74151 one-of-eight multiplexers, to select the desired register, for bits 0 through 9. Bits 10 through 13 are only contained in the A/D Status Register and Display Status Register. Therefore, they are able to use a 74157 quad one-of-two multiplexer chip. When A02 H and A01 H are low, E55-15 is low, enabling the 74157. When this occurs, either the A/D or Display Status register is being selected. BAS AD STAT L goes to pin 1 of the 74157, to select which of the two registers is active.

3.0 INTERRUPT CONTROL

The interrupt control handles three distinct interrupts. These may come from the A/D (INT A H), the Realtime clock (INT B H) or the scope control (INT C H). The A/D and clock interrupts are handled on priority level 6, with the A/D higher in priority (closer to the processor) than the clock. The scope control interrupt is on priority level 4. The priority levels cannot be changed. Since the three interrupt circuits act in essentially the same manner, only the A/D interrupt will be discussed.

Flip-flops FF1A and FF2A start out in the cleared (zero) state, since the interrupt line ADC INT A H has been low. Therefore, E84-6 is high, so that when ADC INT A H goes high (A/D interrupt), BR6 L goes low, requesting an interrupt on priority level 6. Some time later, the interrupt request is granted, and BG6 H goes high. BG6 H is buffered by E91, so that E91-3 goes high. This transition sets FF1A, and

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initiates a 100-nsec. delay through E92, Q3, and E83. Before the end of this delay, FF1A (1) H goes high, so that E83-1 holds the bus grant output low at the end of the delay (i.e. the bus grant stops at the interrupting device and is not passed on). If the A/D had not been the interrupting device, FF1A would be held at 0 due to INT A H being low, FF1A (1) H would be low, and at the end of the 100-nsec. delay, the bus grant BG6 would be passed on (IV BG 6 PASS, to the INT B circuitry). When FF1A is set, since FF2A is still at 0, pins 8 and 9 of E83 are both high, causing BUS SACK L to go low. This indicates to the processor that the bus grant has been received. The processor then removes the bus grant so that BG6 IN H goes low. This causes a positive transition at E82-12 which sets FF2A. With both FF1A and FF2A set, E83-13 goes low, asserting BUS BBSY L, indicating that the interrupting device has taken control of the bus. At the same time, E74-6 goes low, which, through E37, enables E95 and E96. This gates the interrupt vector address onto the BUS D08:D02 lines and asserts BUS INTR L. The processor responds with BUS SSYN L when it has received the vector. This signal goes through E89 to reset the A INT flip-flop (IV A INT DONE L). This causes ADC INT A H to go low, so that E71-11 goes low, and FF1A and FF2A both are reset. Resetting FF1A and FF2A removes the vector from the bus, disqualifies BUS BBSY L and BUS INTR L, and returns the circuitry to its original state.			
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AR11 Circuit Description

The starting interrupt vector may be set in increments of $2\emptyset$ up to a maximum of $76\emptyset$, using S2. Vector selection is illustrated in figure 3:

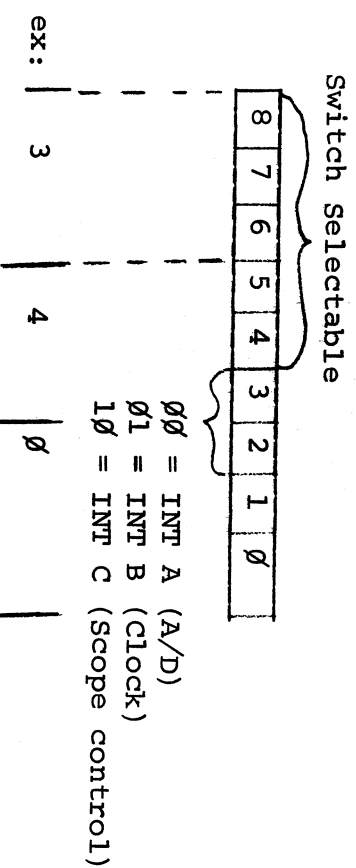


Figure 3: AR11 Vector Address Selection

Location of the vector switches on the module is shown in figure

- The switches are set "on" for a 1 and "off" for a $\emptyset$ (note that this is opposite to the address switches), i.e. to set up a vector of $34\emptyset$, bits 7, 6 and 5 are "on" and bits 8 and 4 are "off".

Bits 3 and 2 are gated onto the bus by E96 as a function of which of the three interrupts is active.

4.0 REAL-TIME CLOCK

The real-time clock consists of a free-running 1 MHz crystal oscillator circuit, a series of four decade counter dividers to generate additional frequencies of 100 KHz, 10 KHz, 1 KHz, and 100 Hz, a multiplexer to select a single frequency for input to a counter, and three registers (clock preset buffer, clock counter, and status).

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4.1 Crystal Oscillator

The oscillator consists of two 8640 gates, connected as inverters with ac-coupled inputs and resistive feedback in a cross-coupled configuration through the 1 MHz crystal. The crystal acts as a low impedance only at 1 MHz and as a high-impedance at all other frequencies. Consequently, at 1 MHz, the two gates are set up in a cross-coupled configuration and oscillation occurs. The output signal RTS PS CLK, available on TP C, is a clean TTL

1 MHz signal. This signal is used directly as a power supply clock, and gated in E81 by the enable counter signal RTC ENA CNTR (1) L before going to the dividers. When the counter is not enabled (RTC ENA CNTR (1) L is high) the counter output can be simulated by the maintenance signal RTC TEST COUNTER H through E81.

4.2 Divider Chain and Multiplexer

The 1 MHz signal is used to generate 100 KHz, 10 KHz, 1 KHz and 100 Hz signals using 74190 decade up/down counters E98 through E101, running in the upcount mode. Each counter increments on the low-to-high transition of the pin 14 input. The pin 13 output goes low when the pin 14 input is low and the counter state is 9, providing a low pulse to the next stage.

The five crystal-based frequencies generated in this manner go to the multiplexer E97, along with the external input and

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A	SP	AR11- $\emptyset$ -5	

SIZE	CODE	NUMBER	REV
A	SP	AR11- $\emptyset$ -5	

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auxiliary clock input. One of these frequencies is selected according to the rate select bits (RTC RATE 0 (1) H, RATE 1 (1) H and RATE 2 (1) H) on E97 pins 11, 10 and 9. The selected rate appears in inverted form on the pin 6 output ($\bar{F}$) of the E97 multiplexer. Since the signals from the divider chain are low-going pulses ($\frac{1}{2}$ μ sec), the signal on E97-6 is a positive pulse. Under normal conditions, E90-7 is high, so that the multiplexer output goes through E90 and appears as a low-going pulse RTC CLK OUT L, which is the input to the clock counter. If BAS MAINT CLK CTR L is low, E90 serves to "stretch" the RTC CLK OUT L pulse, to prevent the counter from changing state while it is being read by the processor.

4.3 Clock Counter and Buffer

The clock counter is an 8-bit presetable counter register consisting of 74193 4-bit up/down counters E40 and E41, used in the upcount mode. Count input is RTC CLK OUT L, on E40 pin 5. Every 16th count, E40-12 propagates the signal into the E41 pin 5 input. The counter register is cleared on INIT, and loaded from the preset register on RTC LD CLK CNTR L, which occurs on overflow in continuous interval mode (mode 1) or when the clock buffer is loaded when the clock is disabled.

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The clock buffer register is loaded from the BIO OUT 07:00 H lines when its address is selected (BAS CLK BUF L goes low). The buffer register load pulse is gated through E71 when the counter is not enabled (RTC ENA CNTR (0) H is high), so that the clock counter is also loaded.

In continuous interval mode, RTC CLK MODE 1 L is low (E81-5) so that E81 acts to invert the signal on E81-6. In single interval mode, E81-5 is high so that E81-4 is low and the clock counter is never loaded via E57-12.

In continuous interval mode the low-going overflow pulse RTC CLK OVRFLW L appears at E81-3 and is inverted at E81-1.

This high-going pulse is ac-coupled through C7, so that its trailing edge causes a low at E81-6. This causes a high pulse at E81-4 which occurs just after the overflow pulse, and causes the clock counter to be reloaded from the clock buffer register.

The clock overflow signal occurs whenever the counter goes from 377 to 0. The pulse actually goes low during the 377 state, and its trailing edge corresponds to the 377 to 0 transition. Consequently, the counter is reloaded with the preset value at the beginning of the 0 state.

4.4 Clock Status Register

The clock status register is a read/write register whose bits control the functions performed by the clock. The high byte of

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this register consists of one-half of E58 (bit 15) and E75 (bits 8, 11 and 14). The high byte is loaded on a pulse from E57-10, the and function of BAS CLK STAT L and BAS OUT HIGH L. The low byte of this register consists of one-half of E58 (bit 7), one half of E70 (bit 0), and E76 (bits 1, 2, 3 and 6). The low byte is loaded on RTC LD CLK LOW H, E57-4, the and function of BAS CLK STAT L and BAS OUT LOW L.

Bit 15, the external flag, is loaded from BIO OUT 15 H when the register is loaded. It is set by the external signal ADC EXT ST (1) L and reset by BAS B INIT L. Bit 14, part of the 74175 E75, is loaded from BIO OUT 14 H. When bit 14 = 1, E68 is enabled to set the clock interrupt flip-flop E70 on the occurrence of the external input ADC EXT ST (1) L. Bit 11, RTC TEST COUNTER H, is used for maintenance purposes to test the clock divider chain. Bit 8, clock mode, determines whether the clock is in continuous interval mode (1) or single interval mode (0).

Bits 3, 2, and 1, part of the 74175 E76, are loaded from BIO OUT 03:01 H when the low byte of the register is loaded. These bits determine the selected rate according to Table 2. Bit 6, also part of E76, is used by E68 to enable the clock overflow to cause an interrupt.

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TABLE 2 - Rate Select

Bit 3	Bit 2	Bit 1	Frequency
Rate 2	Rate 1	Rate 0	
0	0	0	—
0	0	1	1 MHz
0	1	0	100 KHz
0	1	1	10 KHz
1	0	0	1 KHz
1	0	1	100 Hz
1	1	0	External
1	1	1	Aux-pin EL2

Bit 7, the clock done flag, is loaded from BIO OUT 07 H when the low byte of the register is loaded. It is set by RTC CLK OVLW L and reset by BAS INIT L. Bit 0, the clock enable bit, is loaded from BIO OUT 00 H when the low byte of the register is loaded. It is reset from E69-10, the or function of BAS INIT H and clock overflow in single interval mode, from E69-1.

5.0 ANALOG POWER

The analog power supply is shown on page 8 of the M7809 schematic, labelled HQP (High Quality Power). The power supply is a dc-to-dc converter, which develops +14V dc (nominal) from the +5V logic supply. Instead of using a step-up transformer, the power supply uses diodes and capacitors in an extension of the basic voltage doubler technique.

5.1 Voltage Doublers

A basic voltage doubler is shown in figure 4. Its input

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is a square wave running between ground and +5V. During the time that the input is at ground, diode D1 conducts, and C1 charges to +4.3 volts (+5 volts minus the D1 diode drop). In the next half-cycle, the input is at +5V. Since the voltage across the capacitor C1 remains constant, V₁ goes to +9.3 volts, and D1 becomes back-biased. During this interval, D2 conducts, and V_{out} charges to one diode drop less than V₁, or +8.6 volts.

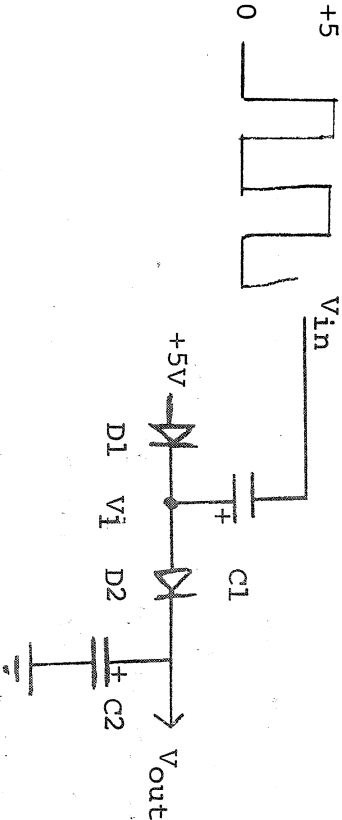


Figure 4: Voltage Doubler

In the next half-cycle, we are back to the beginning, with Vin at ground and D1 conducting, charging C1. At this time, V₁ is at +4.3 volts, and D2 is back-biased. The output voltage remains at +8.6 volts, i.e. we have transformed the +5V input to a +8.6 volt output. Note that if we ignore the two diode drops, we have effectively doubled the input voltage. A good way of looking at the process is that the circuit represents a "bucket brigade". During one half-cycle, charge is passed to C1 through D1. During the next half-cycle, charge is then transferred from C1 to C2

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TITLE AR11 Circuit Description

through D2. Obviously, if we cascade multiple sections, higher voltages can be attained, as charge is passed in "bucket brigade" fashion from one capacitor to the next and ultimately from the last capacitor into the load.

5.2 Square Wave Driver

The 5V square wave input voltage for the AR11 power supply is produced by transistors Q5 and Q6. Transistor Q5 is a PNP which pulls the voltage up to +5 Volts. Transistor Q6 is an NPN which pulls the voltage down to ground. In such circuits, with both active pullup and active pulldown, it is important to guarantee that the two transistors are never on at the same time, even for an instant during switching. This is especially difficult since in general transistors turn off more slowly than they turn on. In the AR11, to guarantee that one turns off before the other turns on, a full 1-μsec interval is allowed.

The signal RTC PS CLK, a 1 MHz (1 μsec) square wave, is applied to pin 14 of E49, a 7493 divide-by-16 counter. The most significant bit of this counter is applied through E48 to the input of flip-flop E45, whose outputs are square waves with a 32-μsec. period. During each half-cycle of the 32-μsec square wave, the 7493 E49 counts from 0 to 15, remaining in each state for 1 μsec. The 7420 E37 decodes the 15 state, so that its pin 8 output goes low for the last microsecond of each half cycle. This

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causes both the pin 8 and the pin 6 outputs of E56 to go high, so that all the E27 outputs are low. When HQP A L (E27-2) is low, Q4 turns on, thereby turning off Q5. When HQP C L (E27-8, 10, 12) is low, Q6 turns off. Thus for the last microsecond of each half-cycle, both Q5 and Q6 are turned off, allowing the one which had been on to turn off completely before the other turns on. The resulting waveforms are shown in figure 5. Note that the square wave drive signal (TP PD) shows a definite intermediate state at the time when both Q5 and Q6 are off.

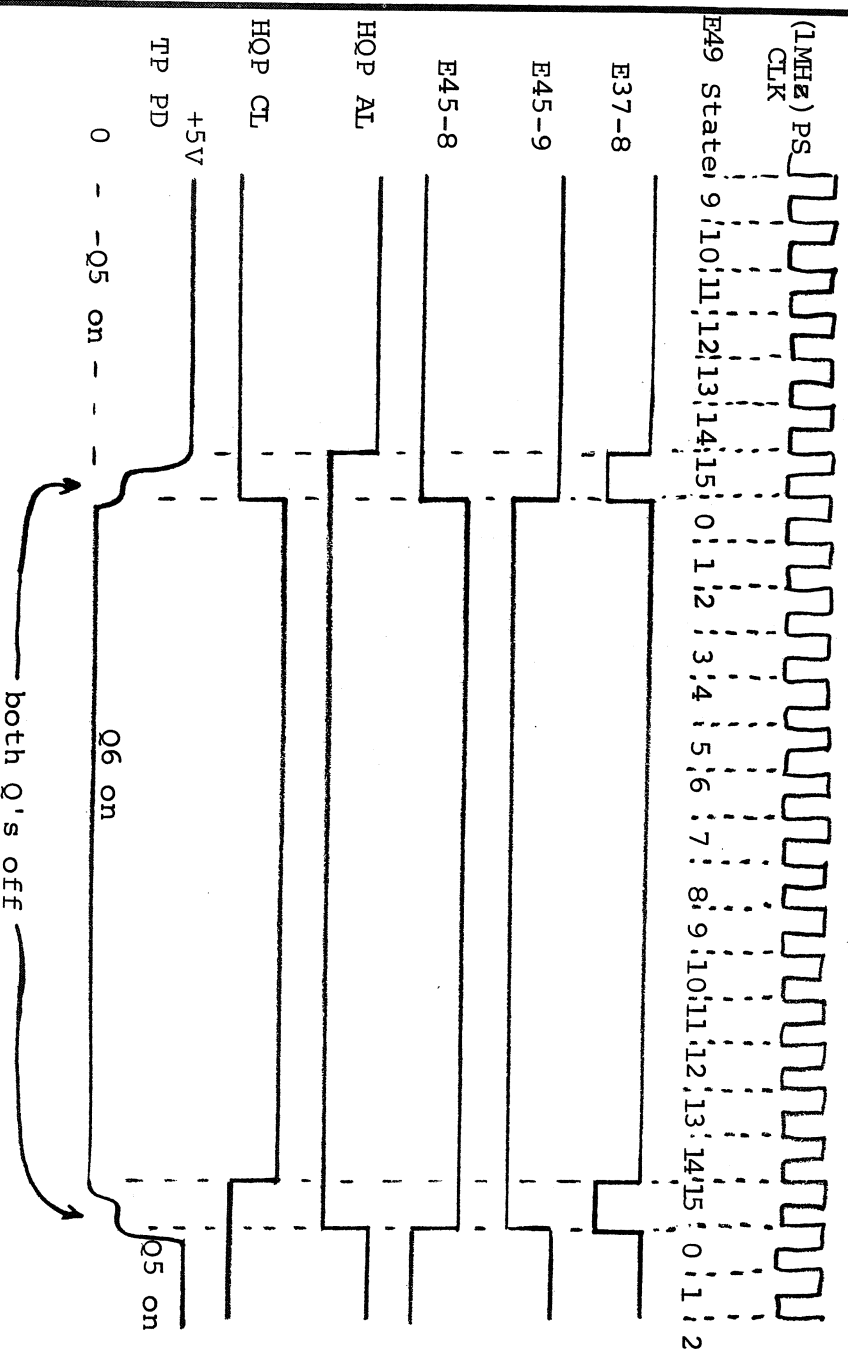


Figure 5: Square Wave Timing Waveforms

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5.3 First Stages

The first stage of the power supply "doubler chain" consists of D4 through D9 and C12 through C14. These are driven directly by the output of Q5 and Q6, as seen at TP PD. Since the diode-capacitor chain functions as a "distributed transformer", the early low-voltage stages run at the highest current levels. Consequently, the TP PD voltage is not the idealized zero-to-+5V signal, but actually only exhibits about a 4.5V swing. The diodes (even though doubled up) exhibit a drop of roughly .85 volts. By the analysis of section 5.1, this results in +7.3 volts dc at the positive end of C13. When TP PD is low, this results in 7.3 - .85 = 6.45 volts at the cathode of D8 and D9. When TP PD goes high, we get 6.45 + 4.5 = 11 volts at the cathode of D8 and D9. Referring to figure 4, TP PD is high when HQP A L is high. At this time HQP BL is also high, so that Q7 is off, allowing Q8 to be turned on. In the opposite half-cycle, HQP B L is low, turning on Q7 and thereby turning off Q8. Meanwhile E27-6 goes high allowing Q9 to turn on. This results in a 10 Volt square wave at the collectors of Q8 and Q9. As in the case of TP PD, the collectors of Q8 and Q9 exhibit the 1-μsec intermediate state, when both transistors are off.

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5.4 Output Stages

The 0V square wave at the collectors of Q8 and Q9 is the input signal for the output diode-capacitor chains. By following an analysis similar to that of section 5.1, allowing roughly .75 Volts for each diode drop, but ignoring the effect of zener diodes D13 and D14, output voltages in the range of ± 16 Volts to ± 17 Volts are arrived at, which would be somewhat higher than desired. However, zener diodes D13 and D14 (whose nominal values add to 15V) act as a regulating negative feedback loop. As the minus supply becomes more negative than -14 Volts, the zeners begin to turn on. This "steals" base drive current from Q9 when it is on, keeping Q9 out of hard saturation and thereby dropping the magnitude of the Q8-Q9 output square wave. This negative feedback loop automatically adjusts the square wave voltage so as to maintain the negative output near -14 Volts. Since the positive supply is also based on the same square wave, it also ends up near +14 Volts.

The two outputs are "smoothed" by LC filters (L2-C25, C24 on the minus side; L1-C21, C23 on the plus side) with a break frequency of roughly 4 KHz, which tend to reduce the ripple and remove high frequency components present due to the switching transients.

The M7809's digital and analog grounds are connected in the middle layer at a single point near the return (ground) end of

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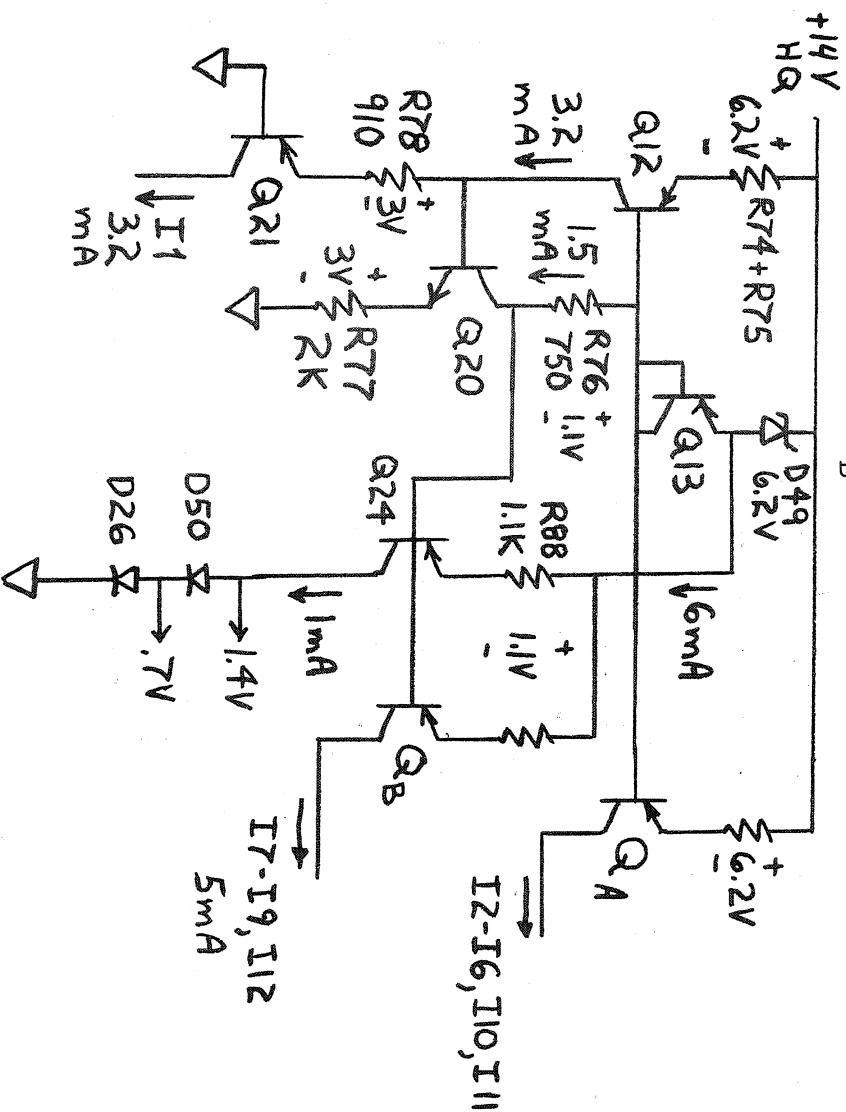
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these filter capacitors.

6.0 ANALOG BIAS CURRENT SOURCES

All analog circuitry in the AR11 is biased by means of current sources, in order to be immune to variations in power supply voltage. The current sources are all shown on page 9 of the M7809 schematics, ABS (Analog Bias Sources).

The reference upon which all the current sources are based is D49, a 1N825 6.2V reference zener diode. This zener is specified to have minimum thermal drift when run at a current level of 7.5 mA. A simplified version of ABS is shown in figure 6, in which Q14 through Q19, Q28 and Q29 have been combined as a single transistor Q_A, and Q25 through Q27 and Q74 have been combined as Q_B.



In analyzing this circuit, we start at zener diode D49, and assume that it is operating at 6.2Volts, its nominal value.

Transistor Q13 has base and collector tied together, so that its base-emitter (b-e) junction acts as a diode. Since the Q13 b-e drop matches the b-e drop of Q12, there is also 6.2 Volts across R74 and R75. Potentiometer R75 is adjusted so that $I_e = 6.2 / (R74 + R75) = 3.2 \text{ mA} \approx I_c$. Consequently, the collector of Q12 is a 3.2 mA current source, as shown in figure 5. This current goes through R78 and Q21 and appears as I1 at the collector of Q21.

Along the way, it sets up a 3 Volt drop across the 910-ohm R78. Since the b-e drops of Q21 and Q20 match, we also have 3 Volts across the 2K R77. This causes the collector of Q20 to be a 1.5 mA current source. This 1.5 mA comes down from the positive supply through the reference zener D49, Q13, and R76. The 1.5 mA through the 750-ohm R76 establishes a 1.1 Volt drop across R76. Since the b-e drop of Q13 matches those of Q24 and Q_B, we also have 1.1 Volts across the emitter resistors of Q24 and Q_B. With an emitter resistor (R88) of 1.1K, Q24 becomes a 1 mA current source. This 1 mA goes to ground through D26 and D50, thereby setting up voltages of .7 Volts and 1.4 Volts for use on pages 11 and 12 of the M7809 schematics. Likewise, the 1.1 Volts across the emitter resistor of Q_B (actually R89, R90, R91, R105) sets up current sources I7, I8, I9, and I12, which total 5 mA. This 5 mA, the 1 mA in Q24, and the 1.5 mA in Q20, combine to make the desired

7.5 mA in D49, the reference zener. Since the Q13 b-e drop matches the b-e drop of Q_A we have 6.2 Volts across the emitter resistor of Q_A (actually R83 + R171, R84 + R172, R85 + R173, R86 + R174, R87, R92, R93). This sets up current sources I2, I3, I4, I5, I6, I10 and I11.

7.0 SCOPE CONTROL

The scope control circuitry is shown on four pages of the M7809 schematic: p. 13 DIR (Display Registers), p. 14 DIL (Display Logic), p. 15 DACX and p. 16 DACY. Since the X and Y D/A converters are identical, only the X D/A converter will be described.

7.1 DIR (Display Registers)

The X Buffer Register consists of 74175 E7 (bits 6-9) and 74174 E8 (bits 0-5). It is loaded from BIO OUT 09:00 H on DIL LD X BUF H, which originates on the display logic page. It is cleared on BAS INIT L.

The Y Buffer Register consists of 74175 E1 (bits 6-9) and 74174 E2 (bits 0-5). It is loaded from BIO OUT 09:00 H on DIL LD Y BUF H, and cleared on BAS INIT L.

Since the 74174 IC has its outputs available only in (1) H form, 7404 hex inverters E3 and E9 are employed to provide Y5 through Y0 and X5 through X0 in (1) L form for use by the D/A converters.

Display Status Register bits 9-11 are contained in 74175 E13.

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TITLE AR11 Circuit Description

They are loaded from BIO OUT 11:Ø9 H on DIL LD DISP HIGH H, and cleared on BAS INIT L. Bits 9, 10, and 11 are CHØ2 STORE, and WRITE THRU. CHØ2 H is inverted by open collector inverter E15, pulled up to +5V by R115 and output through J1-B as CHØ2 L. STORE (1) L is inverted by E15 and output through J1-E as NON STORE L (note the inversion). WRITE THRU H is inverted by E15 and output through J1-A as WRITE THRU L.

Display Status Register bits 2, 3 and 6 are contained in 74175 E14. They are loaded from BIO OUT Ø2, Ø3 and Ø6 H on DIL LD DISP LOW H, and cleared on BAS INIT L. Bits 2 and 3 are DIR DISP MODE Ø (1) H and MODE 1 (1) H, used on the display logic page to control the intensification mode. Bit 6 is DIR DISP INT ENA (1) H, used on the display logic page to enable an interrupt upon completion of intensification of a point.

7.2 DIL (Display Logic)

The display logic page contains scope intensification circuitry, storage scope, erase controls, ready(done) bit, interrupt control, and gates which generate load pulses for the various display registers.

On the left side of the page, the load pulses are generated by E19 and E24, using the register select and output byte signals from the BAS (Bus Address Select) page.

A scope intensification pulse is generated (after appropriate delay) under the following conditions:

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TITLE AR11 Circuit Description

INTENSIFICATION MODE	BIT 3		BIT 2		CONDITION
	MODE 1	(1) H	MODE Ø	(1) H	
Ø			Ø		Set bit Ø
1			Ø	1	Load X
2			1	Ø	Load Y
3			1	1	Load X or Load Y

TABLE 3: Intensification Modes

These conditions are decoded by 7453 E20. For example, if we are in mode 2, MODE 1 (1) H is high, so that when we get LD Y BUF H (load Y buffer register) pins 1 and 13 of E20 are both high, and pin 8 goes low. The low on E20-8 causes a high on E15-2 which causes two things to happen: the signal causes a low on E19-10, which resets E25, the ready (done) flip-flop. It also fires one-shot E21. The resultant E21 delay is to provide time for the D/A outputs and scope beam to settle before intensifying the point on the scope. The E21 delay is nominally 20 µsec, but can be set to 80 µsec for slow storage scope applications by connecting W3. At the end of the E21 delay, a low-to-high transition occurs on E21-4, which fires the other one-shot in E21. This one-shot determines the intensification pulse duration-nominally 2 µsec, but jumperable to 6 µsec for slow storage scopes by means of W6. Either the high or low output of the second one-shot can be applied to E15-13 as a function of whether W4A or W4 is connected, depending on whether a high or low intensification

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A	SP	AR11-Ø-5	

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TITLE AR11 Circuit Description

pulse is desired. After the E15 inversion, the pulse is applied to the base of Q51, which amplifies and re-inverts the pulse for output to the scope. Q52 acts as a 20 mA current source pullup for the output pulse. The output pulse is clamped at 3.3 Volts by zener diode D32, or at 1.4 Volts by diodes D33 and D34 if W5 is connected. The high-going intensification pulse from E21-5 passes through E19 and sets the ready (done) flip-flop E25 on its trailing edge.

Bit 12 of the Display Status Register is implemented by the erase flip-flop E23. It is loaded from BIO OUT 12 H on the DIL LD DISP HIGH H pulse. Setting the Erase flip-flop initiates two actions: ERASE (1) H resets the ready (done) flip-flop E25 through E19, and the inverted (through E15) erase signal DIL ERASE L is applied to the external storage scope through J1-C. The storage scope responds with a low signal ERASE RET L on J1-H. This turns off Q53, so that DIL ERASE CLR H is pulled up to +5V through R121. ERASE CLR H goes through E24 and resets the Erase flip-flop E23 through pin 1. After the interval of time necessary to erase its screen (typically one-half second), the storage scope brings ERASE RET L back to a high voltage level. This turns on Q53, bringing DIL ERASE CLR H low. The resulting low-to-high transition on E19-13 sets the ready (done) flip-flop E25.

When DIR DISP INT ENA (1) H is high, the display interrupt is enabled. In this case, setting the ready (done) flip-flop,

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TITLE AR11 Circuit Description

as a result of either an intensification pulse or completion of an erase operation, sets the display interrupt flip-flop E25.

The resulting interrupt signal DIL INT C H is processed by the IV circuitry. Upon completion of the interrupt, IV DISP INT DONE H resets E25 through E24. Both the erase and interrupt flip-flops are also reset by BAS INTT H, acting through E24.

7.3 D/A Converters

The following description applies to both the X and Y D/A converters, which are identical. Designations of components and signal names apply to the X D/A, page 15 of the M78Ø9 prints.

The D/A converter consists of a 10-bit converter with high output impedance (about 8K) plus a buffer amplifier to lower the output impedance and provide the current needed to drive the capacitive load of the cable to the scope.

7.3.1 Converter

The converter consists of an 8-bit current-output IC D/A (bits Ø-7), two discrete component higher-order current sources (bits 8 and 9) and an offsetting current source I4 (.625 mA), working in conjunction with precision resistors R148, R140, R141 and R145 to give a +5 Volt output.

The IC D/A E10 is powered from DACX +5V HQ, which is the +5 Volt power line filtered by L3 and (C34 + C35). Reference current for this D/A is ABS I2-3.27 mA, running into pin 13.

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A	SP	AR11-Ø-5	

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TITLE			
AR11 Circuit Description			
Consequently, its full scale output current (all logic inputs-pins 5 through 12 - high) is 3.27 mA. Resistance seen by this output current is R145 - 768 ohms. Consequently, bits 0-7 have a total weight of (3.27 mA) (768 ohms) = 2.5 Volts, or one-quarter of full-scale. Now let's examine the two high-order current sources. Assume that X9 (1) L and X8 (1) L are both high, so that E16-2 and -12 are low, and therefore Q54 and Q55 are both off. Voltage reference ABS VB2 is set up on the ABS page-it is 4 Volts plus one transistor b-e drop above the -14V HQ supply. Consequently, the emitters of Q58 and Q59 are 4 Volts above the -14 VHQ supply. It is important to note that this voltage tracks along with the negative supply, so that the voltage across (R136 + R139) and across (R137 + R138) is a constant 4 Volts, independent of the exact level of the negative supply voltage. The values of (R136 + R139) and (R137 + R138) are adjusted so that 1.25 mA current flows in the output line of each current source. Because of the high-current-gain complementary NPN-PNP configuration, Q58 and Q59 base currents are negligible. The 1.25 mA output current from the bit 8 source (Q59, Q57) sees a resistance of (R141 + R145), approximately 2K. Consequently bit 8 has a weight of (1.25 mA) (2K) = 2.5 Volts, or one quarter of full-scale. The 1.25 mA output current from the bit 9 source			
SIZE	CODE	NUMBER	REV
A	SP	AR11-0-5	

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TITLE			
AR11 Circuit Description			
(Q58, Q56) sees a resistance of (R140 + R141 + R145), approximately 4K, so that bit 9 has a weight of (1.25 mA) (4K) = 5V, or one-half of full-scale. Assume an all 1's (1777) input to the D/A. DIR X9 (1) L and X8 (1) L are now low, so that E16-2 and -12 are high, and Q54 and Q55 are on. In this case, the Q54 and Q55 emitters clamp at +.7 Volts, leaving 4.3 Volts across R130 and R131. Q54 and Q55 become current sources, with a value $I = (4.3V/3K) = 1.43 \text{ mA.}$ Since this current is greater than 1.25 mA, all the current from (R136 + R139) and (R137 + R138) is "stolen", Q58 and Q59 turn off, and the bit 9 and bit 8 currents are zero. Since the input is all 1's, E10-5 through -12 are all low, so that the E10-4 output current is also zero. This leaves only I4-.625 mA flowing. I4 goes to ground through (R148 + R140 + R141 + R145), approximately 8K. Consequently, the voltage at the base of Q61 during the 1777 condition is (.625 mA) (8K) = +5 Volts. If we go to all 0's, Q54 and Q55 turn off, allowing the 1.25 mA bit 8 and bit 9 current sources to turn on. E10-5 through -12 are now all high, so that the E10-4 output current is 3.27 mA. These sum up linearly, giving a voltage (as seen at the base of Q61) of +5V (due to I4) -5V (due to bit 9) -2.5V (due to bit 8) -2.5V (due to bits 0-7) = -5 Volts			
SIZE	CODE	NUMBER	REV
A	SP	AR11-0-5	

ENGINEERING SPECIFICATION			CONTINUATION SHEET	
TITLE AR11 Circuit Description				
Note that the all 0's case, with -5 Volts output, actually represents all bit currents <u>on</u>, and the all 1's case, with +5 Volts output, actually represents all bit currents <u>off</u>, with only the offset current I4 on. Since the circuit is linear, any digital combination between 0000 and 1777 results in the proper corresponding voltage between -5 Volts and +5 Volts. The impedance seen at the base of Q61 is the sum of R148 + R140 + R141 + R145, or 8K. If WX is shorted, this 8K is now in parallel with (R134 + R135) = 886 ohms, for a resulting equivalent resistance of 800 ohms. Since this is exactly one-tenth of the original 8K, shorting WX has resulted in one-tenth the output voltage range, or <u>±</u>.5 Volts. Connecting a resistor in place of WX can result in any resistance desired between 8K and 800 ohms, and therefore in any voltage range desired between <u>±</u>5 Volts and <u>±</u>.5 Volts. 7.3.2 Buffer Amplifier The voltage seen at the base of Q61 has 8K source impedance, and is therefore unsuitable for output drive. To provide output drive, a buffer amplifier consisting of Q61, Q62 and Q63 is provided. Bias current for this buffer amplifier is I10, a 1 mA current source. If the input voltage (Q61-base) equals the				
SIZE	CODE	NUMBER	REV	
A	SP	AR11-0-5		

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TITLE AR11 Circuit Description				
output voltage (Q62-base), I10 splits equally and ½ mA shows up in the collector of both Q61 and Q62. The Q61 collector current goes through D38 and R142 to the minus supply. Since the D38 diode matches the Q63 b-e drop and R142 and R143 have equal values, the Q63 collector current equals the Q61 collector current. For equal split of I10 between W61 and Q62, we therefore, have the current out of Q62 equal to the current into Q63, so that there is no net current into or out of C33. This gives us a stable output voltage. If the Q61-base voltage is lower than the Q62-base voltage, more of I10 goes through Q61 than Q62, so that the Q63 current is higher than the Q62 current and we have a net current flow out of C33. Consequently, the C33 voltage (which is also the voltage on the base of Q62) drops, until the Q62-base voltage equals the Q61-base voltage, at which point I10 again splits equally and a stable condition is reached. In this manner, the output voltage (Q62-base) follows the input voltage (Q61-base). Output impedance of this amplifier is approximately 50 ohms. The 47-ohm protection resistor R144 brings the output impedance up to 100 ohms. The Q61 and Q62 b-e junctions are protected for large steps by diodes D35 and D36. The amplifier is protected from "outside-world" overvoltages by fusible resistor R144 and diodes D37 and D39.				
SIZE	CODE	NUMBER	REV	
A	SP	AR11-0-5		

ENGINEERING SPECIFICATION			CONTINUATION SHEET	
TITLE AR11 Circuit Description				
8.0 A/D CONVERTER				
The A/D circuitry is contained on three pages of the M7809 schematic: page 10, ADC (A/D Control), which contains all the A/D logic; page 11, ADCS (A/D Channel Select), which contains the input protection circuitry and analog multiplexer; and page 12, AD (A/D), which contains the sample-and-hold circuit and the actual A/D converter.				
8.1 A/D Control				
The A/D Status Register high byte is contained in 74174 E63. It is cleared on BAS B INTT L, and loaded from BIO OUT 13, 11:08 H when the A/D Status Register and a high byte output operation are selected. The four-bit channel address and unipolar/bipolar bit are contained in the high byte of the status register.				
The A/D Status Register low byte is contained in 74175 E77. It is cleared on BAS B INTT L, and loaded from BIO OUT 06:04 H when the A/D Status Register and a low byte output operation are selected. Bit 6 is used to enable an interrupt on setting of the A/D done flag. Bit 5 enables an A/D conversion to start on overflow from the real-time clock. Bit 4 enables an A/D conversion to start on an external input.				
Bit 0 of the A/D Status Register is used for a program-controlled A/D conversion start. The A/D Status Register low byte load pulse goes through 7404 inverter E48 to one-shot E34. This one shot triggers on the register load pulse if BIO OUT 00 H 1s				
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TITLE AR11 Circuit Description				
high, i.e. if a "1" is being loaded into the A/D Status Register bit 0. The one-shot time is nominally 8 μ sec., which is long enough to allow for the analog multiplexer to settle to its new value before signalling the sample-and-hold to hold the signal, at which point the conversion begins. If it is desired to switch between bipolar and unipolar channels, a 7.5 Volt inter-channel difference is possible instead of the normal maximum of 5 Volts. In this case, W1 is connected, lengthening the one-shot time to 11 μ sec, which is sufficient for the 7.5 Volt difference.				
At the end of the E34 delay, E34-12 goes high, setting the E44 "Hold" flip-flop, which commands the sample-and-hold circuit to hold the analog value for conversion. At the next occurrence of the HQP AD CLK H low-to-high transition (which could be anywhere from 0 to 2 μ sec later), the E44 "Enable A/D" flip-flop is set, which signals the AM2504 successive approximation register (SAR) E26 to begin the A/D conversion. The SAR then sequences through the ten A/D bits, for each bit making its logical decision on the low-to-high transition of HQP AD CLK H, as a function of ADC COMP L. The AD CLK is a 2- μ sec clock signal derived from the 1 MHz crystal oscillator by the E49 power supply counter. Consequently, it takes two microseconds for each "bit decision". The decision signal (COMP L) is derived from the output of the comparator (AD COMP H) by 7405 inverter E47. By jumpering AD COMP H (TP1) to ground, it is possible to bypass the analog circuitry				
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TITLE AR11 Circuit Description

and simulate that comparator output which results in a 1777 con-
version. By jumpering ADC COMP L (TPØ) to ground, it is possible
to bypass the analog circuitry and simulate that comparator out-
put which results in a ØØØØ conversion.

After the least significant bit (ADØØØ) has been resolved,
ADC EOCP L goes low, so that E47-2, 6 are pulled high by R35.
After one microsecond, HØP AD CLK H goes low, so that E47-2, 6
are pulled low by E47-2. This causes a low-to-high transition
on E48-8, which loads the A/D Buffer Register (E39 and E43) with
the converted value information contained on the SAR outputs
AD ØØ:Ø9 H.

ADC EOCP L is inverted by E48 to create ADC EOCP H. This
is or'ed with BAS INIT H in E46 to create ADC CLR L. This signal
resets the "Hold" and "Enable A/D" flip-flops to their original
(Ø) states, and is input to SAR E26-14. This signal is present
for two microseconds, until the next low-to-high transition of
HØP AD CLK H, which then resets the SAR E26.

Bit Ø of the A/D Status Register is held at "1" throughout
the 8-µsec A/D Start delay and the conversion interval by or-gate
E28, which creates ADC AD STAT ØØ (1) H from HOLD (1) L and the
output of the 8-µsec A/D Start delay one-shot.

ADC EOCP H also sets the "AD DONE" flip-flop E45 on its
leading edge. Its output ADC AD DONE (1) H is used as bit 7 of
the A/D Status Register. When an A/D interrupt is enabled,

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ADC AD INT ENA (1) H is high, so that setting the "AD DONE"
flip-flop causes E56-11 to go low and E48-4 (ADC INT A H) to go
high. This causes the A/D interrupt. When the interrupt is
complete IV A INT DONE L goes low. This causes E56-3 to go high
and E46-10 to go low, thereby resetting AD DONE. If the A/D in-
terrupt is not enabled, AD DONE is not reset until a read opera-
tion is performed on the A/D Buffer Register. When this occurs,
BAS IN L and BAS AD BUF L both go low, so that E46 goes high and
E46-10 goes low, thereby resetting the "AD DONE" flip-flop. This
flip-flop is also reset by BAS B INT L, acting through E56 and
E46.

An A/D conversion may also be started by either an external
start signal or a clock overflow. The external start signal
(J1-U) high-to-low transition fires one-shot E34 to create a
500-nsec ADC EXT ST (1) pulse. ADC EXT ST (1) L is used as the
external input by the real-time clock counter. ADC EXT ST (1) H
is used by the real-time clock for its external interrupt and by
the A/D for external starts. If the A/D external start is enabled,
ADC EXT ENA (1) H is high, and ADC EXT ST (1) H on E68-3 causes
E68-6 to go low, thereby setting the "HOLD" flip-flop and initiat-
ing the conversion sequence. If the clock overflow start is ena-
bled, ADC AD CLK ENA (1) H is high, so that RTC CLK OVLW H on
E68-4 causes E68-6 to go low, thereby setting HOLD and initiating
the conversion sequence.

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TITLE AR11 Circuit Description

8.2 A/D Analog Block Diagram Description

The AR11 uses a unique auto-zeroing A/D configuration, in which the same amplifier front end is shared between the sample-and-hold and A/D comparator is such a manner as to cancel out its own offset and drift.* This configuration is shown in figure 7.

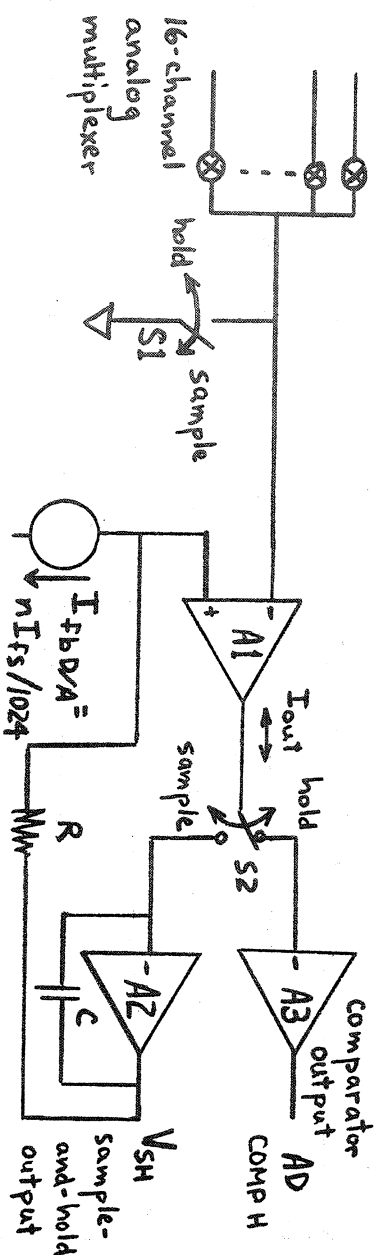


FIGURE 7: A/D Analog Block Diagram
*Patent pending

Amplifier A1 is the front end which is shared between the comparator and sample-and-hold. This amplifier is an operational transconductance amplifier, i.e. its input stage is that of an ordinary operational amplifier, but its output is a current source I_{out} instead of a voltage source.

First let's consider the tracking, or "sample" mode of operation, in which S1 is open, S2 is down, and the feedback current source is off, i.e. $I_{FBD/A} = 0$. Under these conditions, A1 output current I_{out} is integrated and converted to a voltage by sample-and-hold output stage A2, so that the A1-A2 combination acts like an operational amplifier. The A2 output is fed back

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to the A1 input, so that the A1-A2 op amp is in a follower configuration, with the A2 output voltage tracking the selected analog input present on the inverting A1 input.

When it is time to do an A/D conversion, S2 switches from the down to the up position on setting of the "HOLD" flip-flop.

This leaves integrator A2 with zero input, so that feedback capacitor C holds the A2 output voltage constant. This will now serve as the A/D input voltage. On setting of the "ENABLE AD" flip-flop zero to two microseconds later, the 16-channel analog multiplexer is disabled, so that the selected channel switch opens up, and S1 closes, putting a ground reference on the inverting input of A1. Under these conditions, A1 serves as the comparator input stage. A1 output current I_{out} is converted to a logic-compatible voltage level AD COMP H by output stage A3. The successive approximation logic now looks at AD COMP H and proceeds to find that value of n ($0 \leq n \leq 1023$) which results in zero input to amplifier A1. This occurs at $I_{FBD/A} = n I_{FS}/1024 = V_{SH}/R$; $n = 1024 V_{SH}/R I_{FS}$. If we set the scaling such that $R I_{FS} = V_{FS}'$, the desired full-scale input voltage, we have $n = 1024 V_{SH}/V_{FS}'$. During "sample", V_{SH} was tracking the input voltage V_{in} , i.e. $V_{SH} = V_{in}$. Consequently, $n = 1024 V_{in}/V_{FS}'$, which is the desired A/D relationship. For $V_{FS} = 5$ Volts, input voltages of 0 to 5 Volts ($1023/1024$) result in conversions of 0 to 1023, i.e. we have a unipolar input range.

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Now assume identical conditions in "sample" mode except that instead of $I_{FBD/A} = 0$ we turn on the most significant bit (MSB) so that $I_{FBD/A} = I_{FS}/2$. Under these conditions, V_{SH} tracks the selected input voltage with an offset of $RI_{FS}/2 = V_{FS}/2$. If $V_{FS} = 5$ Volts, $V_{SH} = V_{in} + 2.5$, so that an input range to -2.5 to $+2.5$ corresponds to $V_{SH} = 0$ to $+5$ Volts. By turning on the MSB during "sample" we have transformed the unipolar input range into a bipolar input range, with the MSB of the feedback D/A acting as its own bipolar offset reference source. The unipolar/bi-polar bit of the A/D Status Register controls the input range by controlling the state of the MSB during "sample". 8.3 ADCS (A/D Channel Select) Page 11 of the M7809 schematic, ADCS (A/D Channel Select) contains the 16-channel analog multiplexer and switch S1 shown in figure 7 above. Each of the 16 analog input channels comes in through a 1K fusible resistor, which works in conjunction with the diodes of E5 and E11 to protect the AR11 analog multiplexers from input overvoltage conditions. The 16-channel multiplexer consists of two eight-channel PMOS multiplexer IC's E6 and E12. Each of these has three address lines A0:A2 which select one of eight switches, plus an enable line OE which enables the selected switch when high and turns off all switches when low.			
SIZE	CODE	NUMBER	REV
A	SP	AR11-0-5	

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE AR11 Circuit Description			
Switch S1 of figure 7 is implemented by FET Q11. During "sample", ADC ENA A/D (1) L is high, so that E18-12 is low and Q10 is off; R73 pulls the gate of Q11 down to -14V HQ and Q11 is off. When it is time to do a conversion, ADC ENA A/D (1) L goes low, E18-12 goes high, and Q10 turns on, with an emitter current of 12 Volts/20K = .6 mA. This current comes out the Q10 collector and turns on D15, so that Q10-C clamps at +.7 Volts. The gate of Q11 is at ground because of the D45 diode drop, so that Q11 turns on, bringing ADCS MUX NODE to ground. This provides a zero reference for A1 (of figure 7) during the conversion. ADC ENA A/D (1) L also goes to E28-10, 12, causing E28-8, 11 to go high and E18-2, 4 to go low. Thus both ADCS AD MUX 0 ENA H and MUX 1 ENA H are low and both multiplexers (E6 and E12) are disabled during the conversion. This allows Q11 to ground ADCS MUX NODE without having to sink any current except the bias current of A1. During "sample", ADC ENA A/D (1) L is high, so that E28 pins 9 and 13 are enabled. This allows address bit ADC AD MUX 03 H to select which of the two multiplexers is enabled - E6 is enabled on MUX 0 ENA H when AD MUX 03 H is high, E12 is enabled on MUX 1 ENA H when AD MUX 03 H is low. The three low-order address bits ADC AD MUX 00:02 H are inverted by E18 to provide the address MUX A0:A2 L to the multiplexer IC's E6 and E12. Since E6 and E12 are PMOS chips, their			
SIZE	CODE	NUMBER	REV
A	SP	AR11-0-5	

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TITLE AR11 Circuit Description			
logic thresholds are referenced to the +14V HQ supply. Therefore MUX AØ:A2 L, AD MUX Ø ENA H, and AD MUX 1 ENA H are all 14V logic swings, implemented by open collector inverters in E18 and 20K pullup resistors to +14V HQ. 8.4 AD (Converter and Sample-and-Hold) Page 12 of the M78Ø9 schematic (AD) contains the feedback D/A converter and the following circuits from figure 7: operational transconductance amplifier A1, sample-and-hold output amplifier A2, comparator output stage A3, and switch S2. The feedback resistor R of figure 7 is actually made up of R109 and R111. The feedback D/A converter is made up of an integrated circuit 8-bit current output D/A E22 and two higher-order discrete component bits, which function in the same manner as described in the D/A converter section. The two higher-order current sources are both nominally equal to 4 Volts/1.25K = 3.2 mA. The MSB (bit 9) current source "sees" the total resistance R109 + R111, approximately 800 ohms, so that its value is 2.5 Volts, or one-half of full-scale. The bit 8 current source "sees" only R111, approximately 400 ohms, so that its value is 1.25 Volts, or one-quarter of full-scale. During "sample", ADC ENA AD (1) L is high, so that ADC UNITAR H on E17-9 controls the level of E17-10. Since the SAR (E26) was reset at the end of EOCF on the previous conversion, ADC ADØ9 H is high, and E17-13 is high for unipolar and low for			
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TITLE AR11 Circuit Description			
bipolar. When E17-13 is high, Q30 is on so that the R99, R101 current is "stolen" from Q37 and the MSB current source is off. For bipolar range, E17-13 is low, Q30 is off, and the MSB current source is on during "sample", providing the needed half-scale offset. During "sample" AD ENA AD H is low, so that E17-4 is high, Q31 is on, and the bit 8 current source is off. During the conversion, the bit 9 and bit 8 current sources are controlled by ADC ADØ9 H and ADC AD Ø8 H from the SAR, acting through E17. When AD Ø9 H and AD Ø8 H are high, the corresponding current sources are on. The reference current for E22 is ABS I1 - 3.2 mA. Consequently the E22-4 full-scale output current is 3.2 mA, which is present for E22-5 through -12 all high, i.e. ADC ADØ7:ØØ H from the SAR E26 all "1". During "sample", ADC ENA A/D (1) L is high, so that E17-1 is at ground. This turns on Q32, so that the gates of Q60 and Q70 are at +14V HQ. Therefore Q60 and Q70 are off and the E22 output current is diverted into D48, so that the bit Ø-7 current is effectively off. During the conversion ENA A/D (1) L is low, E17-1 is high, Q32 is off, and Q60 and Q70 are held on by R96 between gate and source. The E22 bit Ø-7 output current then goes through Q60 and Q70, D18 and D19, and "sees" R111, approximately 400 ohms, so that its value is (3.2 mA) (400 ohms) or 1.25 Volts, which is the desired one-quarter of full-scale.			
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TITLE AR11 Circuit Description

Operational transconductance amplifier A1 is made up of Q35, Q36 and Q40, biased by current source ABS I6-2 mA. If the base voltages of Q35 and Q36 are equal, I6 will split up with 1½ mA going into Q35 and ½ mA going into Q36, due to the unbalanced emitter resistors R106 and R107. The 1½ mA current from the collector of Q35 is "reflected" by Q40, because the D27 diode drop matches the Q40 b-e drop and R112 and R113 are equal in value. Since the Q36 collector is sourcing ½ mA, and Q40 is sinking 1½ mA, there is a net 1 mA current flowing in the direction from the Q46, Q47 emitters into the Q36, Q40 collectors. This is balanced by the 1 mA current source ABS I8, which flows down through Q44 and Q47 during "sample" and through Q43, Q45 and Q46 during "hold". The difference between this nominal 1 mA and the actual Q36, Q40 current, due to a non-zero Q35-Q36 base difference voltage, acts as the error current into sample-and-hold output stage A2 (Q49, Q50, C28) during "sample" and into comparator output stage A3 (Q48) during "hold".

Switch S2 of figure 7 is actually the current switching network consisting of Q41 through Q47. If ADC HOLD (1) L is high, the circuit is in the sample state. In this condition the bases of Q41 and Q43 are at +5 Volts. The bases of Q42 and Q44 are at +3 Volts, set up by I12-1.5 mA and the 2K pot R114. Since the Q44 base voltage is lower than the Q43 voltage, Q44 is on and I8 takes the right-hand path. Since the Q42 base voltage is lower

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TITLE AR11 Circuit Description

than the Q41 voltage, Q42 is on and I7-.5 mA goes down into R117 instead of R116. Therefore the base of Q47 is higher than the base of Q46, and Q47 is on, allowing I8 to continue on into the A1 output. During "hold", HOLD (1) L is low, so that the Q41, Q43 base voltage is +1.4 Volts. Since the 3-Volt Q42, Q44 base voltage is now higher, I7 and I8 take the left-hand paths, through Q41 and Q43 respectively. Common base stage Q45 transmits the I8 current from Q43 on into Q46, which is now on instead of Q47 because I7 is now going into R116 instead of R117.

During "hold", diodes D28 and D29 and transistor Q45 form a feedback path for amplifier A3 (Q48) clamping the comparator output AD COMP H at +2 Volts high and +.8 Volts low.

8.5 Successive Approximation Waveforms

The AR11 A/D converter uses a successive approximation algorithm in which, initially, all ten bit current sources are on. The current sources are then turned off one at a time (MSB first), and after a two-microsecond settling time, a decision is made (on the basis of all the remaining current sources which are still on) as to whether to leave the current source off or to turn it back on. At the "decision time", if the approximation voltage (TP A) is below zero, the bit current source in question is left in the off state, and a "0" results; if the approximation voltage (TP A) is above zero, the bit current source in question is turned

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TITLE AR11 Circuit Description

back on, and a "1" results. Negative voltage at TP A results in AD COMP H at +2 volts; positive voltage at TP A results in AD COMP H at +.8 volts. The approximation voltage (TP A) is a staircase with both plus and minus steps, "zeroing in" on a threshold voltage near zero. Each of the ten steps has one-half the magnitude of the previous step.

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A		SP	AR11-Ø-5	

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DATE 9/30/74

TITLE AR11 Troubleshooting Procedure

REVISIONS					
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY

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TITLE AR11 Troubleshooting Procedure

1.0 SCOPE

This document covers troubleshooting procedures for the AR11 one-module real-time analog subsystem. The AR11 consists of 16-channel 10-bit A/D converter with sample-and-hold, scope control with two 10-bit D/A converters and the associated logic, and programmable real-time clock. Since the AR11 is an SPC Unibus Option, it also contains a Unibus interface. Since the AR11 draws power only from the +5V logic power supply, it also contains a dc-to-dc converter to supply +14V power for the analog circuitry.

2.0 RELATED DOCUMENTS

The following material should be referenced when using this document:

- 2.1 AR11 User's Guide DEC-11-HARUG-A-D
- 2.2 M7809 (AR11) circuit schematics D-CS-M7809-0-1*
- 2.3 AR11 System Installation/Acceptance Procedure A-SP-AR11-0-4*
- 2.4 AR11 Circuit Descriptions A-SP-AR11-0-5*
- 2.5 AR11 Diagnostic Listings
 - 2.5.1 AR11 Test I (Logic) MAINDEC-11-DZARA-A
 - 2.5.2 AR11 Test II (Analog) MAINDEC-11-DZARB-A
 - 2.5.3 AR11 Test III (wraparound) MAINDEC-11-DZARC-A
 - 2.5.4. DEC/X11 Exerciser Module MAINDEC-11-DXARA-A
- 2.6 Manufacturer's manual for XY display scope or storage scope being used with the AR11.

*Included in AR11 customer print set

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TITLE AR11 Troubleshooting Procedure

3.0 AR11 MAINTENANCE PHILOSOPHY

The AR11 logic is to be repaired in the normal manner. The AR11 analog circuitry is to be repaired only in the AR11 option area. If any analog failures occur either in system integration (FA & T) or in the field, the AR11 is to be board-swapped and returned to the option area for repair. Likewise, no analog adjustments are to be attempted in FA & T or in the field. All potentiometers are sealed after final adjustment in the option area, and from then on are considered to be fixed resistors. All AR11's have been burned in to assure the reliability necessary for successful implementation of this board-swap maintenance philosophy.

It is the intent of this procedure and of the AR11 diagnostics to provide the tools necessary to troubleshoot and repair all digital logic problems, to verify analog performance, and, if A/D or D/A problems are detected, to isolate the problem to either the digital or analog circuitry so that a decision can be made whether to repair the board (digital problem) or to board-swap and return to the option area (analog problem). Field (and FA & T) repairs may be made on the dc-to-dc converter (analog power supply).

4.0 DESCRIPTION OF DIAGNOSTICS

4.1 AR11 Test I (logic) MAINDEC-11-DZARA-A

This diagnostic does a complete checkout of all AR11 logic - Unibus interface, interrupts and vectors, real-time clock,

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TITLE AR11 Troubleshooting Procedure

A/D logic, D/A and scope control logic.

The diagnostic is set up to automatically test multiple AR11's installed in a system provided that the following conditions are met: first (or only) AR11 address 77Ø4ØØ, vector 340; additional AR11's 2Ø higher and sequential, e.g. 77Ø420 and 36Ø, 77Ø44Ø and 4ØØ, etc.; address which is 2Ø higher than the last AR11 address must be unused, e.g. 77Ø42Ø in system with one AR11, 77Ø46Ø in system with three AR11's. Otherwise patch location ARADD with the address of the first AR11 and location ARVCT with the vector of the first AR11. If an unused address is not left after the last AR11, it is necessary to inhibit testing of more than one AR11 by patching 5ØØ3 into the 3\$ location after location RBEG.

Refer to the diagnostic listing for detailed instructions, switch settings, etc. If an error occurs, the printout identifies the address of the failing register, so that the faulty AR11 in a system with multiple AR11's can be identified. Set front console SWØ9 = 1 to loop on the error and troubleshoot using the diagnostic listing, AR11 schematic and AR11 Circuit Descriptions.

4.2 AR11 Test II (analog) MAINDEC-11-DZARB-A

This diagnostic has three major uses - a calibration check (used with an EDC calibrated DC voltage source) for normal AR11 acceptance testing; on-going analog verification testing by users who do not have the BG5036 wraparound maintenance option; and

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TITLE AR11 Troubleshooting Procedure			
checkout of the scope control and scope when the AR11 is interfaced to an oscilloscope. These applications are described in detail in sections 4.4, 4.5 and 4.6 of the AR11 System Installation/Acceptance Procedure. This diagnostic tests only one AR11 at a time. For an AR11 with address 77Ø4ØØ and vector 34Ø, no patches are needed. Otherwise, patch location ARADD with the address of the AR11 and location ARVCT with the vector. Program start location is 2ØØ. Refer to the diagnostic listing for detailed instructions. 4.3 AR11 Test III (wraparound) MAINDEC-11-DZARC-A The wraparound diagnostic enables the AR11 to test itself, in conjunction with a G5036 wraparound module, which is connected to the AR11 through a BC08-R cable. The two D/A converters are combined in various manners using resistive dividers on the G5036 module and sent back into the A/D inputs. Consequently, both X and Y D/A's are tested by the A/D converter, and the A/D is tested by the D/A converters. Because the D/A's are divided down before going into the A/D, test resolution far better than 1 LSB is attained. In addition, the analog power supply levels (+14 Volts) are divided down and used as inputs, allowing test of the dc-to-dc converter; the four scope control logic outputs (ERASE L, NON-STORE L, CHØ2 L, and WRITE-THRU L) are used as inputs, allowing parametric tests of their high and low output levels; the CHØ2 L output			
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TITLE AR11 Troubleshooting Procedure			
is fed back into the ERASE RET input, allowing test of the storage scope erase return handshaking logic; and the scope INTENSIFY output is fed back into the A/D external start input, allowing tests of both functions. Since all A/D input channels are used (at different input voltage levels), the wraparound module also provides a complete functional check on the A/D input multiplexer. Use of the various A/D channels by the wraparound test is as follows: CHØ: Switchable between "Ø", a hard ground used in the wrap-around program, and "E", a split lug useful for connecting an (EDC) calibrated DC voltage source. CH1: Ground through 100K resistor, used for bias current test. CH2: +5 VHQ power, divided down to +1 Volt nominal. CH3: Positive analog supply, divided down to +2.5 Volts nominal. CH4: Negative analog supply, divided down to -2.5 Volts nominal. CH5: Coarse X and fine Y, Voltage $\frac{1}{2}X$ + 1/100Y, Code X + 1/50Y. CH6: Coarse Y and fine X, Voltage $\frac{1}{2}Y$ + 1/100X, Code Y + 1/50X. CH7: Fine Y, Voltage 1/100Y, Code 1/50Y CH1Ø: Fine X, Voltage 1/100X, Code 1/50X CH11: DirectX CH12: DirectY CH13: ERASE L CH14: WRITE-THRU L CH15: NON-STORE L CH16: CHANNEL Ø2 L			
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TITLE AR11 Troubleshooting Procedure					
CH17: +5 VHQ power, divided down to +4 Volts nominal. Using the above inputs, the wraparound diagnostic MAINDEC-11-DZARC-A test the following: a) Scope intensify pulse, external A/D start b) Storage scope handshaking logic - Erase return, etc. c) Scope control output logic high and low levels d) Analog power supply levels e) Functional check on all 16 channels of A/D input f) A/D input bias current g) Calibration of X D/A vs. A/D, Y D/A vs. A/D h) Linearity of X D/A vs. A/D, Y D/A vs. A/D i) Differential Linearity of A/D, X D/A, Y D/A j) A/D inter-channel settling, plus full-scale and minus full-scale k) Noise levels - rms and peak - A/D bipolar, A/D unipolar, X D/A, Y D/A l) Offset - A/D bipolar, A/D unipolar, X D/A, Y D/A In each of the above tests, the numerical results are compared to spec limits, and if everything passes, "END PASS" is printed out. A failure results in a corresponding error printout. Numerical results can be printed out by setting front console SW12 = 1. The wraparound diagnostic is set up to automatically test multiple AR11's installed in a system, provided that the following					
SIZE A		CODE SP	NUMBER AR11-Ø-6	REV	

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TITLE AR11 Troubleshooting Procedure					
conditions are met: first (or only) AR11 address 77Ø4ØØ, vector 34Ø; additional AR11's 2Ø higher and sequential, e.g. 77Ø42Ø and 36Ø, 77Ø44Ø and 4ØØ, etc.; address which is 2Ø higher than the last AR11 address must be unused, e.g. 77Ø42Ø in system with one AR11, 77Ø46Ø in system with three AR11's. Otherwise, patch location ARADD with the address of the first AR11 and location ARVCT with the vector of the first AR11. If an unused address is not left after the last AR11, inhibit testing of more than one AR11 by patching 5ØØ3 into the 3\$ location after location RBEG. When running the wraparound program, each AR11 in the system must have a G5036 wraparound module installed. <u>*Important Note:</u> The BC08-R cable should be connected "upside-down" at the G5036 end, i.e. A to VV rather than A to A. 4.4 DEC/X11 Module MAINDEC-11-DXARA-A The DEC/X11 module operates with or without the G5036 wrap-around module installed. The program tests for the presence or absence of the G5036 and selects the proper routine accordingly. If the G5036 module is available, it should be installed. In this case, the AR11 DEC/X11 exerciser uses wraparound techniques to measure (and compare to spec limits) rms and peak noise levels on A/D and both D/A's. All A/D conversions are started on clock overflow after a random number has been loaded into the clock pre-set register. Since the system is being exercised in the background					
SIZE A		CODE SP	NUMBER AR11-Ø-6	REV	

ENGINEERING SPECIFICATION				CONTINUATION SHEET	
TITLE		AR11 Troubleshooting Procedure			
at the time of A/D conversion, true worst case noise levels are measured, under conditions of full system interaction. If an error is detected (any of the noise levels exceeds its spec limit), the program measures average value and peak-to-peak spread on the +5 VHQ and <u>+14</u> V power supplies, and reports these along with the error message. If the exerciser senses that the G5036 module is not present, it executes a routine which takes conversions on each of the 16 channels, and displays them on the screen of the scope driven by the AR11. Each channel is displayed in turn for about three seconds.					
5.0 AR11 TEST POINTS					
The following test points are available on the AR11 module for troubleshooting purposes:					
TPC: "Clock" - a 1 MHz TTL square wave output from the clock oscillator circuit. If this point is wrong, all bets are off, so that this is a good "quick look" first check for any AR11 problem.					
TPG: "Logic Ground" - use for scope ground when checking AR11 logic signals. Scope should be floating to avoid ground loops.					
TPHQ: "High Quality Ground" - use for scope ground when looking at AR11 analog signals. Scope should be floating to avoid ground loops.					
TP+: "+14 VHQ" - positive analog supply.					
TP-: "-14 VHQ" - negative analog supply. If TP+ and TP- are less					
		SIZE	CODE	NUMBER	REV
		A	SP	AR11-Ø-6	

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than <u>+13</u> Volts, analog problems may occur. The <u>+14</u> V level s should be checked first when verifying an analog problem.					
TPPD: "Power Driver"- the power square-wave drive used in the dc-to-dc converter. This point is a good "quick look" first check for any <u>+14V</u> power supply problem.					
TPØ, TPL: Used for "all Ø's" and "all 1's" jumpers. See section 6.4 below.					
TPSH: Sample-and-Hold output - tracks the selected analog input signal +.8 Volts (unipolar) and +3.3 Volts (bipolar).					
TPA: "A/D Approximation" - tracks the selected analog input signal during "sample", and zeroes in on ground in a series of decreasing plus and minus 2-microsecond steps during "hold".					
TPE: "Enable A/D" - useful for external scope trigger to synchronize scope presentation to A/D conversion when looking at TPA.					
6.0 TROUBLESHOOTING					
6.1 Troubleshooting Flow					
It will be useful to follow the flow of figure 1 below in troubleshooting an AR11. All troubleshooting of logic and dc-to-dc converter power supply should be done with reference to the AR11 schematics and AR11 Circuit Descriptions. Test points which are useful at the various points in the flow chart are indicated on the flow chart.					
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		A	SP	AR11-Ø-6	

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ARL1 Troubleshooting Procedure

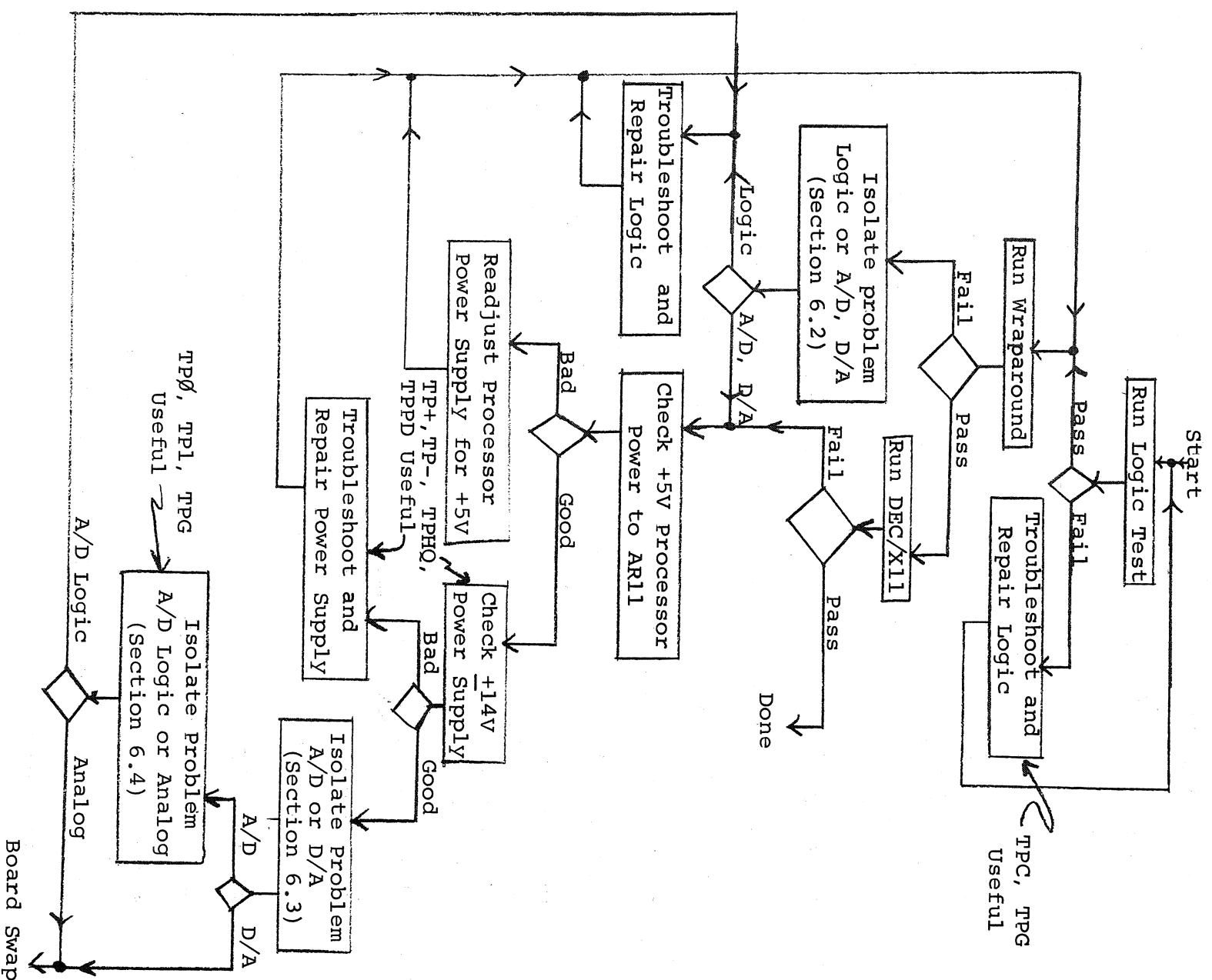


Figure 1: AR11 Troubleshooting Flow

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AR11 Troubleshooting Procedure

6.2 Wraparound Problem - Logic on A/D , D/A ?

Most problems uncovered by the wraparound program are in the

A/D and D/A sections. The following logic problems, which can be fixed in FA & T or in the field, may be uncovered by the wraparound program:

6.2.2.1 "External A/D Start Failed" - The problem is with either

the external A/D start logic or the scope intensify output pulse.

6.2.2.2 "VC Status Register in Error" - The problem is with

either the erase flip-flop, erase return circuitry, or the CHANNEL Ø2 L output signal.

6.2.2.3 "VC Logic Signal High Output Too Low" and "VC Logic

Signal Low Output Too High" - The problem is with the logic level of one of the four scope control logic outputs.

6.3 A/D or D/A?

In most cases, it will be obvious from the error message, error PC, and diagnostic listing comment field exactly where a given problem is - A/D, X D/A or Y D/A. For example the error message may identify a problem as "D/A differential linearity" or A/D inter-channel settling". In other cases, the error message may not identify the culprit, e.g. "Noise level exceeded limit" and it is necessary to refer to the comment field at the location in the error PC to identify the problem, e.g. "A/D bipolar im

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A	SP	AR11-Ø-6	

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TITLE ARL1 Troubleshooting Procedure			
noise" or "X D/A peak noise". The problem arises when a functional failure occurs in either the A/D or one of the D/A's (as opposed to some analog characteristic slightly exceeding its spec limit). In this case, multiple errors are printed out and it's not obvious whether the problem is in the A/D or one of the D/A's. The following table should aid in determining whether the failed device is A/D, X D/A, or Y D/A. Each of the wraparound tests uses some combination of A/D and D/A's. Those devices with an "X" are used in the indicated test.			
TEST	A/D	X D/A	Y D/A
1			
2			
3	X		
4	X		
5	X		
6	X		
7	X		
10	X		
11	X		
12	X		
13	X		
14	X		
15	X		
16	X		
17	X		
20	X		
21	X		
22	X		
23	X		
24	X		
25	X	X	
26	X	X	
27	X	X	
30	X	X	
31	X	X	
32	X	X	
33	X		

SIZE	CODE	NUMBER	REV
A	SP	AR11-0-6	

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TITLE ARL1 Troubleshooting Procedure			
34	X		X
35	X	X	X
36	X	X	X
37	X	X	X
40	X	X	X
41	X		X
42	X		X
43	X		X
44	X		X
45	X	X	X
46	X	X	X
47	X	X	X
50	X		X
51	X		X
52	X	X	X
53	X	X	X

In those cases, where it is impossible to determine from the above table whether it is the A/D or one of the D/A's which has failed, the individual Test II analog diagnostics should be run.

If the ARL1 is interfaced to a scope, Test II (B) will display a series of "pictures" which verify X and Y D/A operation.

If the "pictures" are good, the A/D can be assumed bad by process of elimination. This can be verified using Test II (C), the calibration test, and observing the output on the scope screen.

If the ARL1 is not interfaced to a scope, it is necessary to run Test II (C), the calibration test, and set front console SW10 = 1 to force printout of the converted value.

6.4 A/D Logic or Analog?

Once it has been determined that the A/D converter is non-functional, it is necessary to know whether the problem is in the

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AR11 Troubleshooting Procedure

A/D successive approximation logic (which may be repaired) or in the A/D analog circuitry (which necessitates board swapping). This can be done with the "all 0's" and "all 1's" jumpers. Jumpering TP0 to TPG bypasses the analog circuitry and simulates that output from the analog circuitry which results in a 0000 conversion. Jumpering TP1 to TPG bypasses the analog circuitry and results in a 1777 conversion. These numbers should be monitored using Test II (C), the calibration test. If 0000 and 1777 conversions do not result, the problem is in the A/D successive approximation logic. If 0000 and 1777 conversions do result, the problem is in the A/D analog circuitry.

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ENGINEERING SPECIFICATION

DATE 8/21/72

TITLE MULTILAYER REWORK STANDARD

REV	DESCRIPTION	REVISIONS				
		CHG NO	ORIG	DATE	APPD BY	DATE

1.0 SCOPE

This standard is to apply to rework of any multilayer module manufactured or purchased by Digital Equipment Corporation which is sold or otherwise delivered to a customer.

2.0 GENERAL

The purpose of this standard is to supplement the Module Rework Standard (SP 7605845-0-0, Rev. A) in establishing acceptable methods for modifications to multilayer modules, both in-house and in the field.

Figure 1 shows a cross section of a multilayer board. It is a four-layer board, having etch lines on Side #1 and Side #2 with a ground plane and a power plane between.

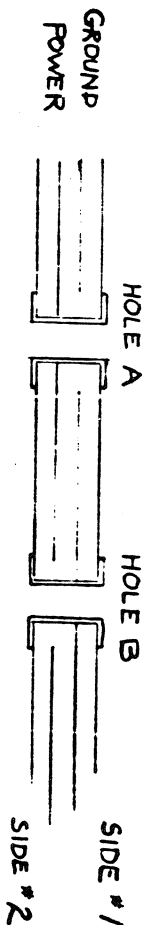


FIGURE 1

In this figure, the ground plane is connected to the Hole B and the power plane to Hole A. If you were looking at this board you would see a clearance hole in the ground plane around Hole A and a clearance hole around Hole B in the power plane. The drilled holes A and B are plated-thru holes that make contact to the proper planes. It is the presence of these inner planes and the connection of plated-thru hole to inner layer that necessitates many of the changes to standard rework practices. The plated-thru hole can be destroyed by excessive heat or mechanical force. Because the inner layer acts as a good dissipator of heat, it is very difficult to remove a component that is in a hole connected to an inner layer.

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3.0 CUTTING LINES

3.1 Etch lines are allowed to be cut in troubleshooting due to the inability to remove a component without destroying it. The cut shall be made as narrow as possible. To repair the cut etch, a piece of uninsulated #30 gauge wire 1/4" to 1/2" in length is to be soldered across the cut, with at least 1/8" of the wire soldered to the etch on each side of the cut.

4.0 ADDING LINES

4.1 #30 gauge white Kynar insulated wire is to be used for all repairs which are not associated with an ECO. White wire is not to be used for ECO's.

4.2 Wires may be added to the #2 side (non-component side) when necessary for repairs under the following restrictions:

4.2.1 The wires must be added after wave solder.

4.2.2 The length of the wire on Side #2 is limited to 1/2".

4.2.3 The wire must lay flat against the board to reduce the possibility of snagging during module removal or insertion. Cementing of the wire to the board is required.

4.3 Wires may be soldered directly to leads of components in multiple pin packages (transistors, IC's). Wire is to be wrapped one full wrap around the lead of the component before soldering, insuring that there is no possibility of contact to an adjacent lead or etch.

4.4 Connection to component leads prior to wave solder shall be by placing the wire in the component hole along with the component.

4.5. It may be necessary to run wires from side 1 to side 2. The following techniques are to be followed:

4.5.1 The preferred method is to utilize an existing hole that has no component. Clean the hole of solder (7.1.3) and run the wire through, insuring that no uninsulated portion of the wire is in the hole.

4.5.2 The alternate method is to drill a hole. (See 6.2)

5.0 TACK SOLDERING

5.1 Tack soldering to gold fingers is allowed on both side 1 and side 2 under the following restrictions:

5.1.1 The wire or solder may not extend into the critical contact area (Wire #305040-0-0).

5.1.2 A wire on side 2 shall be as short as possible and will not ex-

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- for holes which connect to the power or ground planes. The minimum amount of heat should be used, but do not try to pull the lead from the hole until the solder has melted or the hole will be removed with the lead. Do not hold the lead with the pliers while heating, since the pliers will act as a heat sink. If the leads were cut too close to the board to grip with the pliers, push the lead up from side #2 with the soldering iron until enough lead exists on side #1 to grip. The leads must be withdrawn from the #1 side, since the cut end of the lead could damage the hole if it was pulled out from side #2. Clip axial leads close to side #2 before removing.
- 7.1.3 Cleaning of the hole may be accomplished by use of a solder removal tool or by heating the solder and pushing it out with a #20 (.032 diam.) stainless steel wire. When using the solder removal tool, solder may have to be added to the hole first. Minimize heating.
- 7.1.4 Insert the new component, bending the leads slightly to retain the component.
- 7.1.5 Clip the leads of the component, insuring that they do not extend greater than 1/16" from the surface of the boards.
- 7.1.6 Solder all leads on side #2.
- 7.1.7 Clean flux from both sides of the board with trichloroethylene, freon, or equivalent.
- 7.2 If a hole is "pulled" during repairs, the following procedures apply:
- 7.2.1 If the hole was a freethrough, wires must be soldered to the component lead and then soldered to the etch lines to regain connection.
- 7.2.2 If the hole connected to a plane, #30 gauge white wire is to be used to connect the affected lead to the nearest hole connecting to the same plane.

8.0 REMOVING INTERNAL SHORTS

Figure 2a shows a hole with an internal short. This condition may be caused by improper etching of the clearance hole when the board is made. It is possible to salvage the board by removing the short and using wires to regain the necessary connections between component and etch lines.

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- ceed 1/2" in length. (See 4.5 for routing wires from side 2 to side 1.
- 5.2 Tack soldering to gold fingers is to be done only in the following manner:
- 5.2.1 The stripped length of the wire to be added is not to exceed 1/8 of an inch from end of insulation to end of bare wire.
- 5.2.2 The tack soldering of the wire onto the extended and unextended gold finger is to be done neatly to prevent putting too much solder on finger or causing the solder to flow down the finger for more than 1/8 of an inch, maximum, making the board non-acceptable.
- 6.0 DRILLING HOLES
- 6.1 Drilling of new holes in multilayer boards is to be considered a last resort.
- 6.2 All new holes shall be drilled with a #58 drill through a clearance hole in the layers, insuring that the hole is not drilled into the inner layers. Should this happen, inspect the hole for any copper smears between the layers, test the board for power to ground short, fill the hole with epoxy, then try another hole (stycast 1266 or equivalent epoxy).
- 6.3 A #54 drill shall be used for removing internal shorts (See 8.0). Holes drilled to remove internal shorts prior to wave solder shall be filled with epoxy after testing the board for power to ground shorts. If the hole is not epoxied, solder could fill the hole during wave solder and regain the internal short.
- 6.5 Holes drilled for component addition or to provide passage for insulated wires from side to side may only be drilled through clearance holes.
- 7.0 COMPONENT REMOVAL/REPLACEMENT
- 7.1 The following technique is to be used when removing components:
- 7.1.1 Clip the leads close to the connection to the component and remove the body of the component. This is necessary since the crimped portion of the leads will damage the hole if the component is removed in one piece. Modified cutters (Utica 46C-4 Mod) are required to perform this on multiple lead components. Care should be exercised not to damage the etch during the cutting.
- 7.1.2 Apply heat to individual leads from side #1 and remove leads carefully from side #1 using a pair of needle nose pliers. The weller "hot tip" (PT-P8) is the recommended soldering iron

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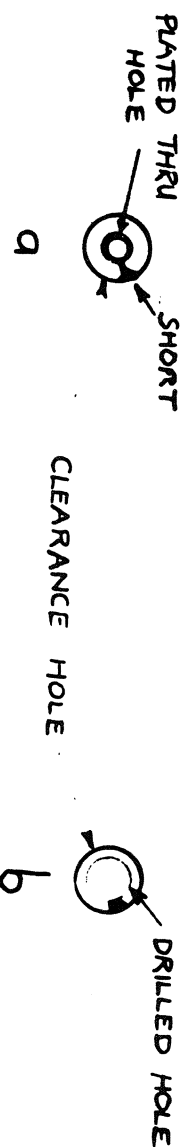
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FIGURE II



- 8.1 If there is a component lead in the hole, remove the component. (7.0)
- 8.2 Drill out the plated-thru hole with a #54 drill. (6.2)
- 8.3 Inspect that the walls of the plated-thru hole have been removed by the drilling.
- 8.4 Check for removal of the short with an ohmmeter.
- 8.5 If the short still exists or copper smears are visible in the hole, clean the hole with a .058 in. reamer.

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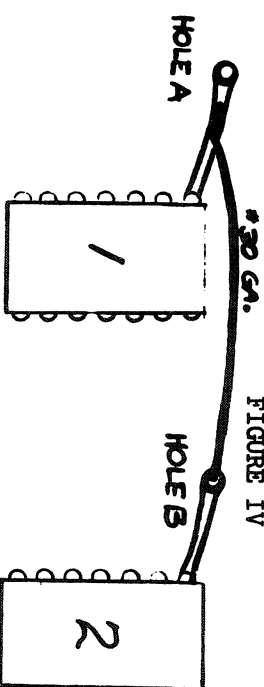
- 8.6 Since the end of the copper trace that was causing the short is still present at the side of the drilled hole (Figure 2b), no uninsulated wire or component lead may be inserted in the hole.
- 8.7 Before inserting the new component (the old one was destroyed in removal), cut the lead off at the seating plane that corresponds to the drilled hole (Figure 3).

FIGURE III



- 8.8 Insert the new component (7.1.4).
- 8.9 Attach a white #30 gauge insulated wire to the cut lead (4.3).
- 8.10 Tack solder the other end of the wire to the necessary etch. If on side #2, run the wire through the drilled hole and attach (4.2).
- 8.11 If a short was removed in a hole that was intentionally connected to one of the planes, the connection may be regained by tack-soldering a white #30 gauge insulated wire to the etch and running the wire to a hole that connects to the same plane. Solder the wire into the hole.

FIGURE IV



Hole A and Hole B are power plane connections. If Hole A also had a short to the ground plane, it would be drilled out to remove the short and a wire run from the etch to Hole B. This would regain the power connection to IC #1.