

CHAPTER 4

11-FAMILY PROGRAMMING INFORMATION

4.1 GENERAL DESCRIPTION

This chapter describes the RL11, RL V11, and RL V12 controllers and points out the differences among them.

4.1.1 RL11 Controller Description

The RL11 controller consists of a single hex-height M7762 module. It can be installed in any hex-height small peripheral controller (SPC) slot. This controller provides a programmable interface between the PDP-11 UNIBUS and the RL01/RL02 disk drive(s). The controller has four addressable registers that are detailed in Paragraph 4.2. The controller can respond to one of seven commands from the software. These controller commands are explained in detail in Paragraph 4.3.

The RL11 buffers the data flow between drive and memory with a 16- x 16-bit IC buffer. This buffer has the designation of SILO as it is a first-in, first-out device.

4.1.2 RL V11 Controller Description

The RL V11 controller consists of 2 quad-height modules designated M8013 and M8014. This controller provides a programmable interface between the LSI-11 Q-Bus and the drive(s). Like the RL11, the RL V11 has four addressable registers that are explained in detail in Paragraph 4.2. The RL V11 can respond to one of eight commands from the software. These commands are explained in Paragraph 4.3.

The RL V11 buffers the data flow between drive and memory with a 256- x 16-bit RAM. This RAM has the designation of FIFO (first-in, first-out).

4.1.3 RL V12 Controller Description

The RL V12 controller consists of one quad-height module designated M8061. This is a fine-line etch, multi-layered module with an extremely high IC chip density. The controller may be used on the standard LSI-11 Q-Bus or the Q-22 Bus. The use of 22-bit addressing (Q-22 Bus) is selected via a jumper. This controller functionally replaces the RL V11 as the programmable interface between the drive(s) and the LSI-11 Q-Bus. The program accessible registers are explained in detail in Paragraph 4.2. Like the RL V11, the RL V12 has a maintenance command that the RL11 does not have. All eight commands are described in Paragraph 4.3. The RL V12 also has a 256- x 16-bit RAM used as a FIFO buffer.

4.2 ADDRESSABLE REGISTERS

There are four addressable registers in the RL11 and RL V11 controllers that are used to control and monitor the operation within the controller itself and within the disk drive unit(s). These are described briefly in Table 4-1 and described in detail in the following text. The RL V12 controller contains these four plus an additional register to hold the balance of the 22-bit memory address.

Table 4-1 Controller Addressable Registers

Address (Octal)	Description
774400	Control Status (CS) – Indicates drive ready condition; decodes drive commands and provides overall control functions and error indications. Bus Address (BA) – Contains the memory location involved in a data transfer during a normal read or write operation. Disk Address (DA) – Stores information for: (1) seeking to desired track; or (2) selecting sectors to be transferred during read/write operations; or (3) used when requesting a drive status message. Multipurpose (MP) – (1) Functions as word counter when transferring read/write data between UNIBUS and drives; or (2) acts as storage buffer when reading drive status; or (3) stores header information from controller silo when executing a read header command. Bus Address Extension (BAE) – Contains the upper six bits of 22-bit memory addressing. This register is used only with the RL V12 controller and then only when 22-bit addressing mode is enabled.
774402	
774404	
774406	
17774410	

4.2.1 Control Status Register

The Control Status (CS) register (Figure 4-1) is a 16-bit register with a base address of 774400. Bits 1 through 9 can be read or written; the other bits can only be read. Table 4-2 describes the bit format of the Control Status register.

When the controller is initialized, bits 1-6 and 8-13 are cleared and bit 7 is set. Bit 0 is set whenever the selected drive is in the ready condition; otherwise, the bit is cleared. Bit 14 is set whenever there is a drive error; it is cleared when the drive error is corrected or the drive error is cleared by a Get Status command. Bit 15 is set when there is a drive or controller error (indicated in bits 10-14).

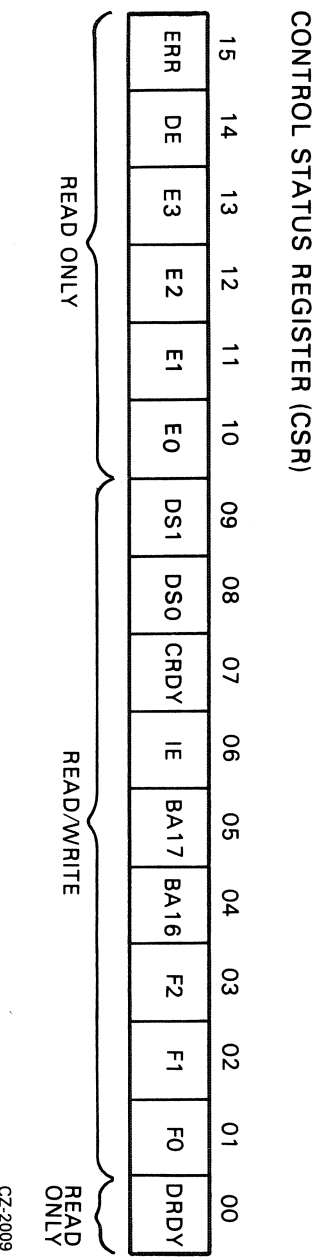


Figure 4-1 CS Register

Table 4-2 Control Status Register Bit Description

Bit(s)	Description																		
0	Drive Ready (DRDY) – When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a seek or head select operation is initiated and set when the operation is completed.																		
1-3	Function Code – These bits are set by software to indicate the command to be executed. <table> <tr> <td>Command</td><td>F2-F0</td></tr> <tr> <td>No Op (RL11) or Maintenance Mode (RLV11/RLV12)</td><td>000</td></tr> <tr> <td>Write Check</td><td>001</td></tr> <tr> <td>Get Status</td><td>010</td></tr> <tr> <td>Seek</td><td>011</td></tr> <tr> <td>Read Header</td><td>100</td></tr> <tr> <td>Write Data</td><td>101</td></tr> <tr> <td>Read Data</td><td>110</td></tr> <tr> <td>Read Data without Header Check</td><td>111</td></tr> </table>	Command	F2-F0	No Op (RL11) or Maintenance Mode (RLV11/RLV12)	000	Write Check	001	Get Status	010	Seek	011	Read Header	100	Write Data	101	Read Data	110	Read Data without Header Check	111
Command	F2-F0																		
No Op (RL11) or Maintenance Mode (RLV11/RLV12)	000																		
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Get Status	010																		
Seek	011																		
Read Header	100																		
Write Data	101																		
Read Data	110																		
Read Data without Header Check	111																		
4-5	Bus Address Extension Bits (BA16, BA17) – These are the two most significant bus address bits when operating in 18-bit addressing modes. They are read and written as data bits 4 and 5 of the cs register but considered as address bits 16 and 17 of the bus address register (see Paragraph 4.2.2).																		
6	Interrupt Enable (IE) – When this bit is set by software, the controller is allowed to interrupt the processor at the normal command or error termination.																		
7	Controller Ready (CRDY) – When cleared by software, this bit indicates that the command code in bits 1-3 is to be executed (negative G0 bit). The hardware sets this bit to indicate the controller is ready to accept another command.																		

Table 4-2 Control Status Register Bit Description (Cont)

Bit(s)	Description																
8-9	Drive Select (DS0, DS1) – These bits determine which drive will communicate with the controller via the drive bus.																
10-13	Error Code <table> <tr> <td>Error Name</td><td>E3-E0</td></tr> <tr> <td>Operation Incomplete (OPi)</td><td>0001</td></tr> <tr> <td>Read Data CRC (DCRC or Write Check Error (WCE)</td><td>0010</td></tr> <tr> <td>Header CRC (HCRC)</td><td>0011</td></tr> <tr> <td>Data Late (DLT)</td><td>0100</td></tr> <tr> <td>Header Not Found (HNF)</td><td>0101</td></tr> <tr> <td>Non-Existant Memory (NXM)</td><td>1000</td></tr> <tr> <td>Memory Parity Error (MPE) RLV12 only</td><td>1001</td></tr> </table>	Error Name	E3-E0	Operation Incomplete (OPi)	0001	Read Data CRC (DCRC or Write Check Error (WCE)	0010	Header CRC (HCRC)	0011	Data Late (DLT)	0100	Header Not Found (HNF)	0101	Non-Existant Memory (NXM)	1000	Memory Parity Error (MPE) RLV12 only	1001
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14	Drive Error (DE) – This bit is tied directly to the DE interface line. When set, it indicates that the selected drive has flagged an error. (The source of the error can be determined by executing a Get Status command and then executing an MPR read.) DE can be cleared by executing a Get Status command with bit 3 of the DA register set.																
15	Composite Error (ERR) – When set, this bit indicates that one or more of the error bits (bits 10-14) is set. If the IE bit (bit 6 of CS) is set and an error occurs (which sets bit 7), an interrupt will be initiated.																

4.2.2 Bus Address Register

The Bus Address (BA) register (Figure 4-2) is a 16-bit register with an address of 774402. Bits 1 through 15 can be read or written; bit 0 is always zero. Bus address bits 16 and 17 are contained in bits 4 and 5 of the CS register.

The BA register indicates the memory location involved in the data transfer during a normal read or write operation. The contents of the BA register are automatically incremented by two as each word is transferred between the bus and the I/O buffer. This register overflows bits BA16 and BA71 into CS register bits 4 and 5. If the controller is an RL V12 and if 22-bit addressing mode is enabled, then bits BA16 through BA21 are found in the BAE register.

The BA register is cleared by initializing the drive or by loading the register with zeros.

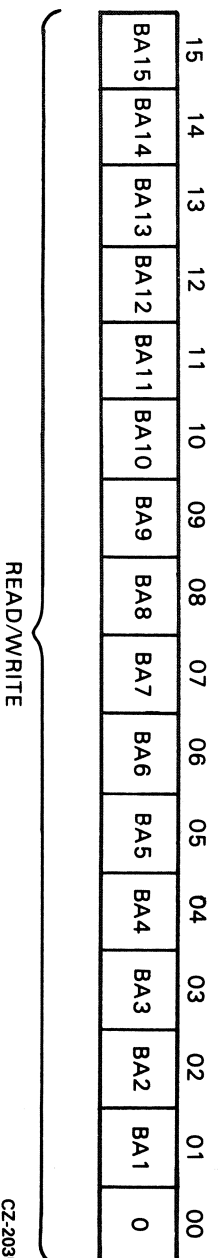


Figure 4-2 BA Register

4.2.3 Disk Address Register

The Disk Address (DA) register is a 16-bit register with an address of 774404. Its contents can have one of three meanings depending on the function being performed. This register is cleared by initializing the device or loading the register with zeros. All 16 bits can be read or written by the processor. The following three paragraphs describe the uses of the Disk Address register.

4.2.3.1 DA Register During a Seek Command – To perform a Seek function, it is necessary to provide cylinder address difference, head-select, and head-directional information to the selected drive. Figure 4-3 shows the bit layout of the Disk Address register during seek commands, while Table 4-3 describes the bit format.

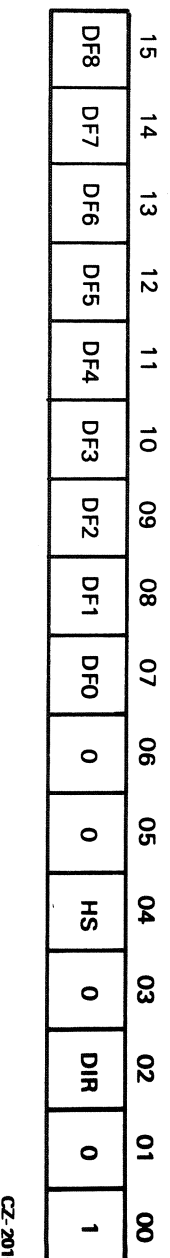
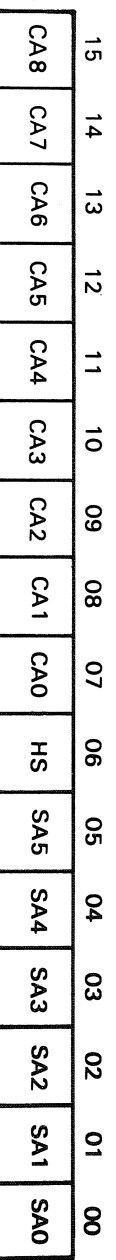


Figure 4-3 DAR Contents to Execute
a Seek Command

**Table 4-3 Disk Address Register Bit
Description for Seek Commands**

Bit(s)	Description
0	Marker Bit – Must be a one.
1	Seek – Must be a zero, indicating to the drive that a seek is being requested. With this bit cleared, the drive uses the remaining contents of the register as seek parameters.
2	Direction (DIR) – This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 7-15).
3	Must be a zero.
4	Head Select (HS) – Indicates which head (disk surface) is to be selected. A one selects the lower head; a zero, the upper head.
5-6	Reserved.
7-15	Cylinder Address Difference DF 08:00 – Indicates the number of cylinders the heads are to move on a seek.

4.2.3.2 DA Register During Read or Write Data Command – For a read or write operation, the DA register is loaded with the address of the first sector to be transferred. As each successive sector is transferred, the DA register is automatically incremented. The contents of this register are used by the header comparison logic to locate the desired sector. The header read from the disk is compared against the contents of this register. Figure 4-4 shows the bit format of the Disk Address register during data transfer commands, while Table 4-4 describes the bit format.



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**Figure 4-4 DA Register Contents During a
Read/Write Data Command**

Table 4-4 Disk Address Register Bit Description for Data Transfer Commands

Bit(s)	Description
0-5	Sector Address SA 05:00 – Desired address of one of the 40 sectors on a track as supplied by the software (range is 0 through 47, octal).
6	Head Select (HS) – Desired head address of one of the two drive heads. A one indicates the lower head; a zero, the upper head.
7-15	Cylinder Address CA 08:00 – Desired address of one of the cylinders on the disk (range is 0 through 777, octal). The RL01 has 256 cylinders and the RL V12 has 512 cylinders.

4.2.3.3 DA Register During a Get Status Command – For a Get Status command, the DA register bits must be programmed as shown by Figure 4-5 and described in Table 4-5.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

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Figure 4-5 DAR Contents to Execute a Get Status Command

Table 4-5 Disk Address Register Bit Description for Get Status Commands

Bit(s)	Description
0	Marker Bit – Must be a one.
1	Get Status (GS) – Must be a one, indicating to the drive that the status word is being requested. At the completion of the Get Status command, the drive status word is read into the controller Multipurpose (MP) register. With this bit set, the drive ignores bits 8-15.
2	Must be a zero.
3	Reset (RST) – When this bit is set, the drive clears its error register (resets all drive faults) before sending the status word to the controller.

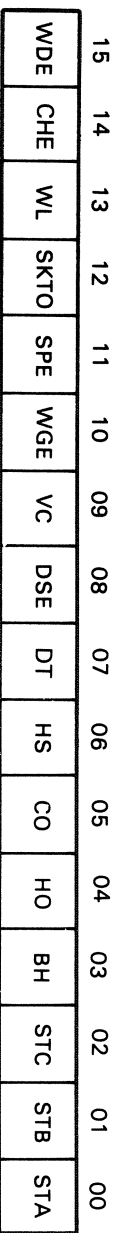
Table 4-5 Disk Address Register Bit Description for Get Status Commands (Cont)

Bit(s)	Description
4-7	Must be a zero.
8-15	Not used during a Get Status.

4.2.4 Multipurpose Register

The Multipurpose (MP) register is a 16-bit register with an address of 774406. This register can have one of three meanings, depending on the function being performed. The following three paragraphs describe the uses of the Multipurpose register.

4.2.4.1 MP Register After a Get Status Command – When a Get Status command is executed, the status word is returned to the controller and transferred to the MP register. Figure 4-6 shows the bit layout, while Table 4-6 describes the bit format.



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Figure 4-6 MPR – Following a Get Status Command

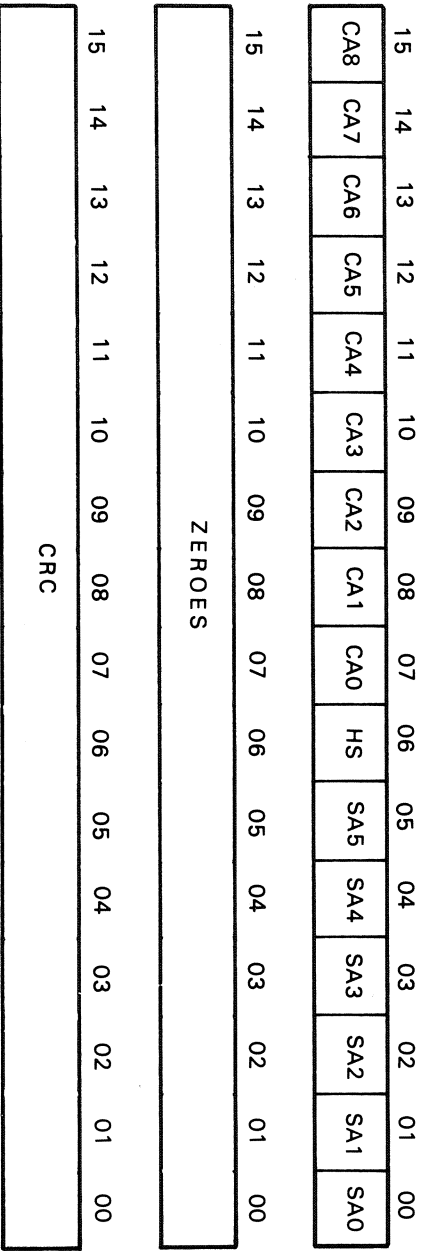
Table 4-6 MP Register Bit Description for Get Status Commands

Bit(s)	Description
0-2	Major State Code (ST C:A) – These bits define the state of the drive.
	STC STB STA
	0 0 0 Load cartridge
	0 0 1 Spin-up
	0 1 0 Brush cycle
	0 1 1 Load heads
	1 0 0 Seek
	1 0 1 Lock on
	1 1 0 Unload heads
	1 1 1 Spin-down

**Table 4-6 MP Register Bit Description
for Get Status Commands (Cont)**

Bit(s)	Description
3	Brush Home (BH) – Set when the brushes are home.
4	Heads Out (HO) – Set when the heads are over the disk.
5	Cover Open (CO) – Set when the drive access cover is open or the dust cover is not in place.
6	Head Select (HS) – Indicates the currently selected head. A zero indicates the upper head; a one, the lower head.
7	Drive Type (DT) – A zero indicates an RL01; a one, an RL02.
8	Drive-Select Error (DSE) – Set when a multiple drive selection is detected.
9	Volume Check (VC) – Set during transition from a head load state to a head-on-track state. Cleared by execution of a Get Status command with Bit 3 asserted.
10	Write Gate Error (WGE) – Sets when Write Gate is asserted and one or more of the following conditions exist. • Drive is not “ready to read/write” • Drive is write-protected • Sector pulse is occurring • Drive has another error
11	Spin Error (SPE) – Set when spindle has not reached speed in the required time during spin-up or when spindle speed is too high.
12	Seek Time Out (SKTO) – Set when the heads do not come on-track in the required time during a Seek command or when “ready to read/write” is lost while the drive is in position (lock-on) mode.
13	Write Lock (WL) – Set when the drive is write protected.
14	Current Head Error (CHE) – Set if write current is detected in the heads when Write Gate is not asserted (reading).
15	Write Data Error (WDE) – Set if Write Gate is asserted but no transitions are being detected on the Write Data line.

4.2.4.2 MP Register After a Read Header Command – When a Read Header command is executed, the next header is read and its three words are transferred to the MP register. The first word contains sector address, head-select, and cylinder address information. The second word contains zeros. The third word contains header CRC information. All three words can be read sequentially by the program by reading the contents of the MPR. Figure 4-7 shows the bit layout of the MP register for Read Header commands, while Table 4-7 describes the bit format.



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Figure 4-7 MPR – Following a Read Header Command

Table 4-7 MP Register Bit Description for Read Header Commands

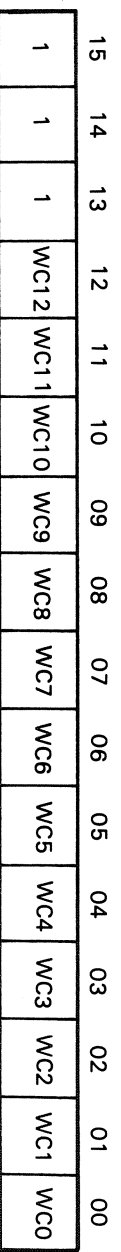
Bit(s)	Description
0-5	SA 0:5 – Sector Address
6	HS – Head Select
7-15	CA 0:8 – Cylinder Address

4.2.4.3 MP Register During Read/Write Data Commands – Before the reading or writing data, the program loads the word count into the MP register in two's complement form. The counter is incremented as each word is transferred. Usually, the reading or writing operation is terminated when the word counter reaches zero (overflows). The word counter can keep track of from one to the full 40-sector count of 5120 data words (decimal). Figure 4-8 shows the bit format of the MP register for data transfer commands, while Table 4-8 describes the bit format.

NOTE

The RL01/RL02 disk drive will not do spiral read/writes. If data is to be transferred past the end of the last sector of a track, it is necessary to break up the operation into the following steps.

1. Program the data transfer to terminate at the end of the last sector of the track.
2. Program a seek to the next track. This can be either a head switch to the other surface but same cylinder or a head switch and move to the next cylinder.
3. Program the data transfer to continue at the start of the first sector at the next track.



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Figure 4-8 MPR – Used as a Word Counter

Table 4-8 MP Register Bit Description for Data Transfer Commands

Bit(s)	Description
0-12	Word Count WC 12:00 – Contains the two's complement of total number of words to be transferred.
13-15	Must be ones.

4.2.4.4 Bus Address Extension Register – The Bus Address Extension (BAE) register (Figure 4-9) is a six-bit register with an address of 17774410. It is used only with the RLV12 controller, and then only when the 22-bit addressing mode is enabled. Bits 0 through 5 can be read or written. Bits 0 and 1 contain the same information found in the CSR bits 4 and 5.

NOTE

If 22-bit addressing is to be used, the software must correctly load the CSR bits 4 and 5 with the contents of BA17 and 16. Upon command initiation, these two bits are loaded into BAE bits 0 and 1. Figure 4-9 shows the bit format of the Bus Address Extension register.

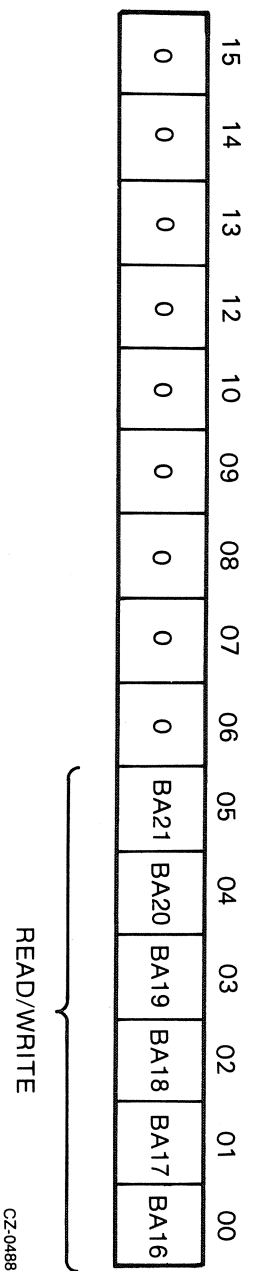


Figure 4-9 BAE Register

4.2.5 Register Summary

Figure 4-10 is a bit and function summary of the CS, BA, BAE, DA, and MP registers.

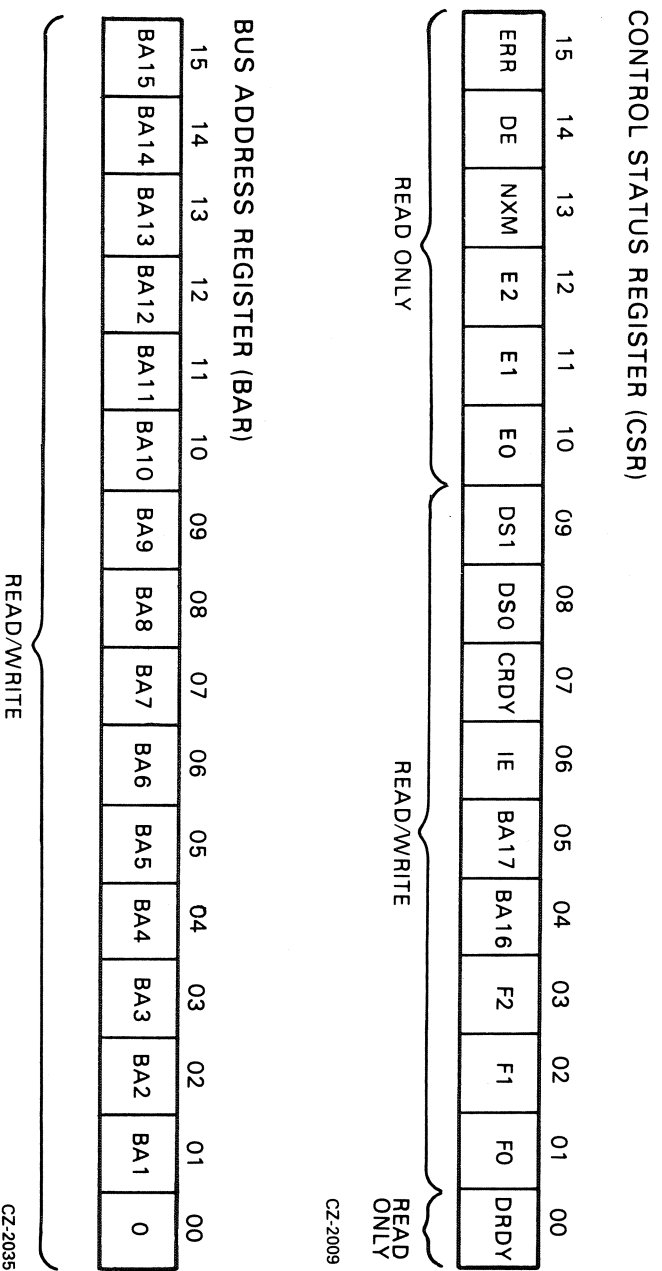


Figure 4-10 Register Summary (Sheet 1 of 3)

15	14	13	12	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	BA21	BA20	BA19	BA18	BA17	BA16

READ/WRITE

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DAR DURING READING OR WRITING DATA COMMANDS

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CAB	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

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DAR DURING GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	X	X	X	X	X	X	X	0	0	0	0	RST	0	1	1

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MPR AFTER GET STATUS COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WDE	CHE	WL	SKTO	SPE	WGE	VC	DSE	DT	HS	CO	HO	BH	STC	STB	STA

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MPR AFTER READ HEADER COMMAND

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CAB	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	HS	SA5	SA4	SA3	SA2	SA1	SA0

ZEROES

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC															

Figure 4-10 Register Summary (Sheet 2 of 3)

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MPR DURING READ/WRITE COMMANDS FOR WORD COUNT

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	WC12	WC11	WC10	WC9	WC8	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

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Figure 4-10 Register Summary (Sheet 3 of 3)

4.3 CONTROLLER COMMANDS

The RL11 controller responds to one of seven commands from the software, while the RLV11/RLV12 can respond to one of eight commands. Table 4-9 lists the commands. Each command is explained in the following paragraphs.

Table 4-9 RL11/RLV11/RLV12 Controller Commands

Function Code	Command
0	No Op (RL11) or Maint. (RLV11/RLV12)
1	Write Check
2	Get Status
3	Seek
4	Read Header
5	Write Data
6	Read Data
7	Read Data Without Header Check

4.3.1 No-Op (RL11) or Maintenance (RLV11) – Function Code 0

The RL11 performs no operation aside from clearing errors (all except DE), setting CRDY and interrupting if IE is set.

The RLV11/RLV12 maintenance command is used during a diskless diagnostic routine to detect controller malfunctions or to establish a level of confidence in controller operation. Prior to issuing the maintenance command, a buffer area in memory must be set aside for writing and reading of test patterns. The controller registers must be loaded by program with the following information.

- BAR with address of first memory buffer location
- WC register with a count of 511 (177001 octal)
- DAR with test word
- CSR with a function code 0, reset bit 7

When the maintenance command is issued (MAINT) and the CRDY bit is cleared, the OPI timer starts. The microsequencer decodes the command and starts a maintenance routine. Two internal tests are performed and the DAR is incremented after each. DMA transfers take place between memory and the controller FIFO, transferring 256 words from the memory write test buffer into the FIFO. Once the FIFO is full, 255 words are transferred into the memory read test buffer previously prepared. The DAR is now incremented a third time. Throughout MAINT, error checks are made; if an error occurs, the function sets ERR. The DAR is incremented as the test proceeds. This incrementing serves as a trace to determine the failing internal test.

Next, the test word +3 that was initially loaded into the DAR is channeled through the data multiplexer and into the CRC circuit. A CRC word is generated from this test word and sent through the data multiplexer again. This CRC of the test word then passes through the write precompensation circuit and the data separator circuit to eventually end up in the FIFO.

The contents of the DAR are then incremented and become test word +4. This new test word follows the same path as the preceding test word and ends up as the second word in the FIFO. At this point, the FIFO holds:

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of test word +4

The contents of the DAR are now incremented once again and become test word +5.

Next, the second word in the FIFO (CRC of test word +4) is removed from the FIFO and serialized. It is sent through the data multiplexer the CRC, and data multiplexer again, and so on. It follows the same data path as the two previous words and ends up back in the FIFO as the new second FIFO word. At this point, the FIFO holds the following.

WORD	FIFO
1st	CRC of test word +3
2nd	CRC of CRC of test word +4

The contents of the DAR is then incremented for the sixth time to become test word +6. The controller ready bit is then set and the CPU receives an interrupt request. This completes the maintenance command operation.

As a result of this maintenance test, the following circuits are tested: the FIFO, the registers, the data multiplexer, the CRC circuit, the match circuit, the write precompensation circuit, the data separator circuit and the FIFO input and output serializer. Also, many of the microsequencer functions are exercised.

4.3.2 Write Check – Function Code 1

The write check command is used to verify that data was written on the disk correctly. It is used after writing a block of data onto the disk by the write command function. The write check command reads this same block of data from the disk and compares it with the contents of its source data buffer area in main memory. Because this comparison is performed in the controller, this source data must be transferred out of memory and into the controller buffer.

Prior to issuing this command, the BA register must be loaded with the address of the first location of the data block in the main memory. The word counter register must be loaded with the data block length. The DA register is then loaded with the starting disk address location. At this point, the write check command can be loaded into the CS register.

Once the header is found, and the header CRC validates the match, 128 words of data are read from the disk. The disk data is then compared serially with the serial data coming out of the silo (SER DATA OUT). Either a compare error or a data CRC error will set bit 11 in the CS register.

4.3.3 Get Status – Function Code 2

The Get Status command causes the status word from a drive to be transferred to the controller where the software can access it through the MPR. The software should first verify that the controller is ready to perform an operation (the drive does not have to be ready). Then, the software should load the DAR with ones in bits 01 and 00, and zeros in the other locations. Next, the software should load the CSR with drive-select bits, a negative GO bit, IE bit (if desired) and a code of 2 in the function bits. The controller will then command the selected drive to transfer its status word to the MPR in the controller. If the “reset” bit (03) in the DAR is also set, the drive resets its status register before transferring it to the controller. This is the manner in which Volume Check is cleared or to check for hard errors.

4.3.4 Seek – Function Code 3

The Seek operation causes the positioner to move (either forward or reverse) some number of cylinders. The software should first verify that the drive is ready to accept a command, then load the DAR with the difference word (difference between the present position and desired position). This word contains the number of cylinders to move (bits 15 through 07), the head-select bit (04) and the direction bit (bit 02, 1=forward, 0=reverse). Bits 06, 05 and 01 must be reset and bit 00 must be set. After the DAR is loaded, the software should load the CSR with the command word. This word should contain the drive-select bits, the negative GO bit, the IE bit (if desired), and a code of 3 in the function bits. The controller sends the Seek command to the selected drive, causing the drive to start its Seek operation. At this time, the controller becomes ready and interrupts if IE is set. The controller is now ready to accept another command to perform another operation on another drive while the Seek is occurring.

If the difference word is large enough that the heads attempt to move past the innermost or outermost limits, the head will stop at the guard band and retreat to the first even-numbered data track.

4.3.5 Read Header – Function Code 4

When a Read Header function is decoded, the controller will read the first header encountered on the selected drive and place the three header words in the buffer. They pass through the buffer and stop with the first word in the MP register. The software can then access the first word to determine the current sector, head, and cylinder address. When the software extracts the first word from the MP register, the second word automatically moves into the MP register. If the software extracts the second word, the third word automatically moves into the MP. This is the CRC word. The software can now access it for checking purposes.

4.3.6 Write Data – Function Code 5

When this function is decoded with CRDY cleared, the controller reads successive header words and compares them to the DA register. When a match is found, the header CRC is checked and, if correct, that sector is written with the words from memory designated by the BA and/or BAE register(s). The BA and MP registers are incremented for each word that is transferred. For partial sector writes, the remaining sector area is filled with zeros. At the end of the sector, the sector portion of the DA register is incremented. The next sector is written if all the words have not been written. At the end of the transfer, CRDY is set and an interrupt made if IE is set.

4.3.7 Read Data – Function Code 6

When this function is decoded, the controller reads successive header words and compares them to the contents of the DA register. When a match is found, the header CRC is checked and, if correct, that sector is read and the words are placed in the memory location designated by the BA and/or BAE register(s). Both the BA and MP registers are incremented for each word that is transferred. This operation continues until the contents of the MP register are all zeros. Data CRC is checked and the DA register is incremented at the end of each sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

4.3.8 Read Data Without Header Check – Function Code 7

When this function is decoded, the data portion of the sector following the next sector pulse is read and the words requested are placed in the memory locations designated by the BA register. The BA and MP registers (word count in two's complement form) are incremented for each word transferred. The header is neither compared nor checked for CRC errors. Data CRC is checked at the end of a sector. If the word count has not overflowed, the next sector is read. Otherwise, CRDY is set and an interrupt is made if IE is set.

NOTE

The DA register is not incremented during multi-sector transfer.

4.4 CSR ERROR CODE DEFINITIONS

4.4.1 Operation Incomplete (OPI)

This error is flagged by the setting of bit 10 of the CSR. When bit 10 is set and 11 through 13 are clear, the indication is that the current command being executed did not complete within the OPI timer period. For an RL11, this timer period is 200 ms. For the RL V11 controller, the period is 490 ms. The RL V12 controller timer is set for 550 ms.

4.4.2 Data CRC (DCRC) or Write Check (WCE)

This error is flagged by the setting of bit 11 of the CSR. When bit 11 is set and bit 10 is clear, the indication is either that a CRC error has occurred when reading data or that a write check error has occurred. If the function currently being executed is a write check command, then the probabilities are that the error is a WCE. If the function being executed is a read data command, then the error is a DCRC. A write data command cannot flag either of these errors.

4.4.3 Header CRC (HCRC)

This error is flagged by the setting of bit 11 of the CSR. When bit 11 is set and bit 10 is also set, the indication is that a CRC error has occurred when reading a header. This error can set during write data or read data commands.

4.4.4 Data Late (DLT)

This error is flagged by the setting of bit 12 of the CSR. When bit 12 is set and bit 10 is clear, the indication depends upon the command being executed.

- Write Data Command – The silo or FIFO buffer in the controller emptied before the word counter overflowed. This means that the command is not finished but the buffer contains no more words to write. When this happens the DMA cycles are too slow.
- Read Data Command – The silo or FIFO buffer in the controller is full and there are more words to read from the disk. When this happens, the DMA cycles are too slow causing data being read to be lost.

4.4.5 Header Not Found (HNF)

This error is flagged by the setting of bit 12 of the CSR. When bit 12 is set and bit 10 is also set, the indication is that the desired header address could not be found before the OPI timer expired.

4.4.6 Non-Existant Memory (NXM)

This error is flagged by the setting of bit 13 of the CSR. When bit 13 is set and bit 10 is clear, the indication is that the addressed memory did not respond to the DMA cycle request within 10 to 20 microseconds.

4.4.7 Memory Parity Error (MPE)

This error is flagged by the setting of bit 13 of the CSR. When bit 13 is set and bit 10 is also set, the indication is that a data parity error was detected on a DMA cycle to the controller. This error applies to RLV12 controllers only.

4.5 OPERATIONAL CONSIDERATIONS

4.5.1 Interrupt

The controller will request an interrupt if the IE bit and the CRDY bit are both set in the CS register. The IE bit is set or reset by the software and reset with the initialize condition. The CRDY bit is set by the hardware upon completion of a function or upon the setting of an error flag. It is also set by the initialize condition. It is reset by the software to cause the controller to start a function (negative GO bit). The interrupt vector address is 160. The normal priority level for the RL11 is BUS REQUEST 5. The RLV11 and RLV12 controllers use the one priority level provided by the LSI-11 processor.

4.5.2 Seek Operation

The following sequence is an example of performing a seek function.

1. Issue read header function to drive and wait for interrupt or wait for CRDY.
2. Check error flag.
3. Read the header word from the MP register.
4. Calculate difference and direction for the seek.
5. Move difference word to the DA register.
6. Issue seek function to drive and wait for seek to be completed as indicated by drive ready bit.
7. Check error flag.

A software system that optimizes positional latency (see Paragraph 1.4) would keep current cylinder and head-select information in core so that Steps 1, 2, and 3 would be unnecessary. Also, note that reading the header gives rotational position as well so that some rotational optimization is possible.

4.5.3 Overlapped Seeks

Since the controller comes ready and interrupts as soon as a seek is issued, it is possible to issue seeks to additional drives while the first is seeking. However, no interrupt occurs when the seeks are completed, so the transfer command should be issued to the drive requiring the shortest seek as soon as all seeks are issued. In this way, the drive completing its seek first will immediately perform its transfer and interrupt when finished.

4.5.4 Data Transfer

Data transfer is via DMA facility. Sixteen words of silo buffering are provided for data by the RL11. The RL V11 and RL V12 controllers provide 256 words of FIFO (RAM) buffering and will not start transferring a sector unless the FIFO has enough space to hold the entire sector.

To do a data transfer, steps of the seek operation would be followed by:

- Load BA and BAE registers with address of first memory location to be transferred,
- Load DA register with address of first disk location to be transferred,
- Load WC register with two's complement of number of words to be transferred,
- Issue read data or write data and wait for interrupt or test for ready,
- Check error flag.

Other drives could do seeks or data transfers between the issuing of seek and the issuing of the data transfers.

4.5.5 Recovery of Data with Bad Headers

Function 7, read data without header check, is provided to allow the recovery of data should headers become unreadable. If constant HNF of HCRC errors are encountered on a particular sector so that the data is not recoverable by the standard read command, proceed as follows. Perform successive read header commands until the sector preceding the bad sector is found. Then, within 300 microseconds, issue the read data without header check command. The data portion of the next sector will be read without either a header compare or a check of the header CRC. Data CRC errors will be reported.

4.5.6 Non-Interchangeability of RL01K/RL02K Disk Cartridges

These two types of cartridges are not functionally interchangeable but a cartridge will physically fit into the "wrong" type of drive. If a cartridge is loaded into the wrong drive, no damage will occur to the drive, media, or data, but the software will not run normally. If such symptoms are exhibited, the operator should check for the proper cartridge type.

4.6 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them can be considered recoverable in the sense that if the operation is retried it is possible that the error will not recur and successful use of the subsystem can continue. Some of the errors are considered fatal because retries could damage the data, media, or equipment. The errors are listed with the recommended reaction in Table 4-10.

The nature of these errors should be considered when determining how many times to retry the operation before declaring that retrying has reached a practical limit. For instance, a DLT error could be caused by a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability for a short duration. In this latter case, it is likely that the operation would be successful on the first retry. The rate of occurrences is a good indicator of overall system performance and an error logging routine should count that. A general increase in the rate of DLT errors could indicate hardware system failures or it could indicate that the usage of the system is approaching its throughput capacity in its present configuration.

Table 4-10 Errors

Controller Error	Bit in C.S.	Recommended Reaction
OPI	10	Retry some practical number of times.
DCRC/HCRC/WCE	11	Retry some practical number of times. Be sure to record contents of the DA register.
DLT/HNF	12	Retry. If HNF, perform a read header, and verify cylinder.
NXM	13	Retry once. Be sure to record the contents of the BA register.
DRIVE ERROR	14	Perform a Get Status and check bits listed below.
Drive Error	Bit in Status Word	Recommended Reaction
DSE	8	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	10	Retry.
SPE	11	Retry.
SKTO	12	Retry. Wait for 1.5 sec after Reset.
CHE	14	Fatal. Do not retry.
WDE	15	Fatal. Do not retry.

Another example of applying practical reaction to an error is the handling of an HNF error. It should be retried once; if it recurs, then possibly the head is not positioned over the correct track. If a read header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If it is not, then possibly there is a bad spot on the media and another area should be tried. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the original sector.

As an additional example, consider an NXM error. It indicates that a memory unit is not responding to a DMA request for data transfer to/from that memory unit. It is unlikely that the media or disk unit is failing and only slightly more likely that the controller is failing (hardware problem). It is possible that the program is trying to access a non-existent memory unit (software problem). A retry may be worthwhile for one time but more than likely it will recur. The most important piece of information needed for diagnosis is the contents of the BA register.

Each of the errors should be given the same type of practical thought when programming error recovery routines. Whenever an error occurs, the program should log it (along with the symptoms such as the contents of the registers), the status of the unit, and whether or not a retry was successful. The more complete the error log, the more quickly and accurately the cause can be diagnosed.

4.7 DIFFERENCE SUMMARY (RK05 AND RL01/RL02)

This section may be helpful to users who have formerly used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming an RK05 subsystem and programming an RL01/RL02 subsystem.

In general, the RK05 subsystem has a lot of its functionality built into the hardware while the RL01/RL02 subsystem requires the software to provide some of the functionality. The major differences are explained below.

4.7.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end-of-track condition. The hardware will then cause a mid-transfer seek to the next track and restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface of the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DAR advances to 50 (octal), which is illegal, and the OPI error flag is set. It is necessary for the software to: 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation, or, 2) detect that it has occurred. The software must initiate a separate seek function as well as a continuance of the read/write function. Note that a head switch from upper to lower surface without a positioner movement to the next cylinder is considered a seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

4.7.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit seek is a software-directed seek operation. An implicit seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired cylinder address or head address does not coincide with the present position. The RL01/RL02 subsystem hardware does not have this capability. The software must ensure that the positioner is over the desired cylinder and that the desired head is selected before starting a read/write operation.

4.7.3 Recalibrate

The RK05 subsystem has a return-to-zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder 0 must be performed. If the current cylinder address is not known then the drive is commanded to seek into the outer guard band. The guard band will be detected and the head will retreat to cylinder 0.

4.7.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 disk cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

4.7.5 Reformating

The RK05 cartridge can be reformatted in the field while the RL01K/RL02K cartridges cannot. The embedded servo information and Bad Sector File greatly reduce the need to reformat the cartridge in the field.

4.7.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.