NEW NUMBER = DZDHD

DH11 Speed Selection Logic Test

ABSTRACT

The DH11 speed selection logic test verifies that the speed selection functions of the line parameter register operate properly for each transmitter and receiver line. Transmitter timing is checked first, and then receiver timing is tested. The program uses a relative timing comparison to determine if line speed selection is correct.

NOTE:
The external clock functions (speed codes 16 and 17) are not tested.

REQUIREMENTS

PDP-11 family standard computer with 4KW of memory
ASR-33 teletype or equivalent
DH11 asynchronous multiplexer
DM11 maintenance card installed

STORAGE = program loads into 4KW of memory

LOADING = Absolute Loader

EXECUTION TIME = Less than 30 minutes per device

STARTING PROCEDURE = start at 200
restart at 2000

PRINTOUTS = Yes

SWITCH REGISTER OPTIONS = Yes

SW15 = HALT ON ERROR
SW14 = LOOP ON CURRENT TEST
SW13 = SUPPRESS ERROR TYPEOUT
SW11 = INHIBIT ITERATIONS
SW10 = ESCAPE TO NEXT TEST ON ERROR
SW09 = FREEZE VARIABLE PARAMETER IN CURRENT TEST
SW01 = START PROGRAM AT SELECTED TEST
SW00 = CHANGE PARAMETERS AT PROGRAM RESTART