

Rmφ3

digital

Digital Equipment GmbH

E 751

Supplement

**Schulungs-
Zentrum
München**



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RM02/03 TRAINING SUPPLEMENT

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CHAPTER 5 Installation and PM

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MBA Integrated Backplane Control

5.1

Logic Chassis Control

5.2

Massbus Cable Connection

5.3

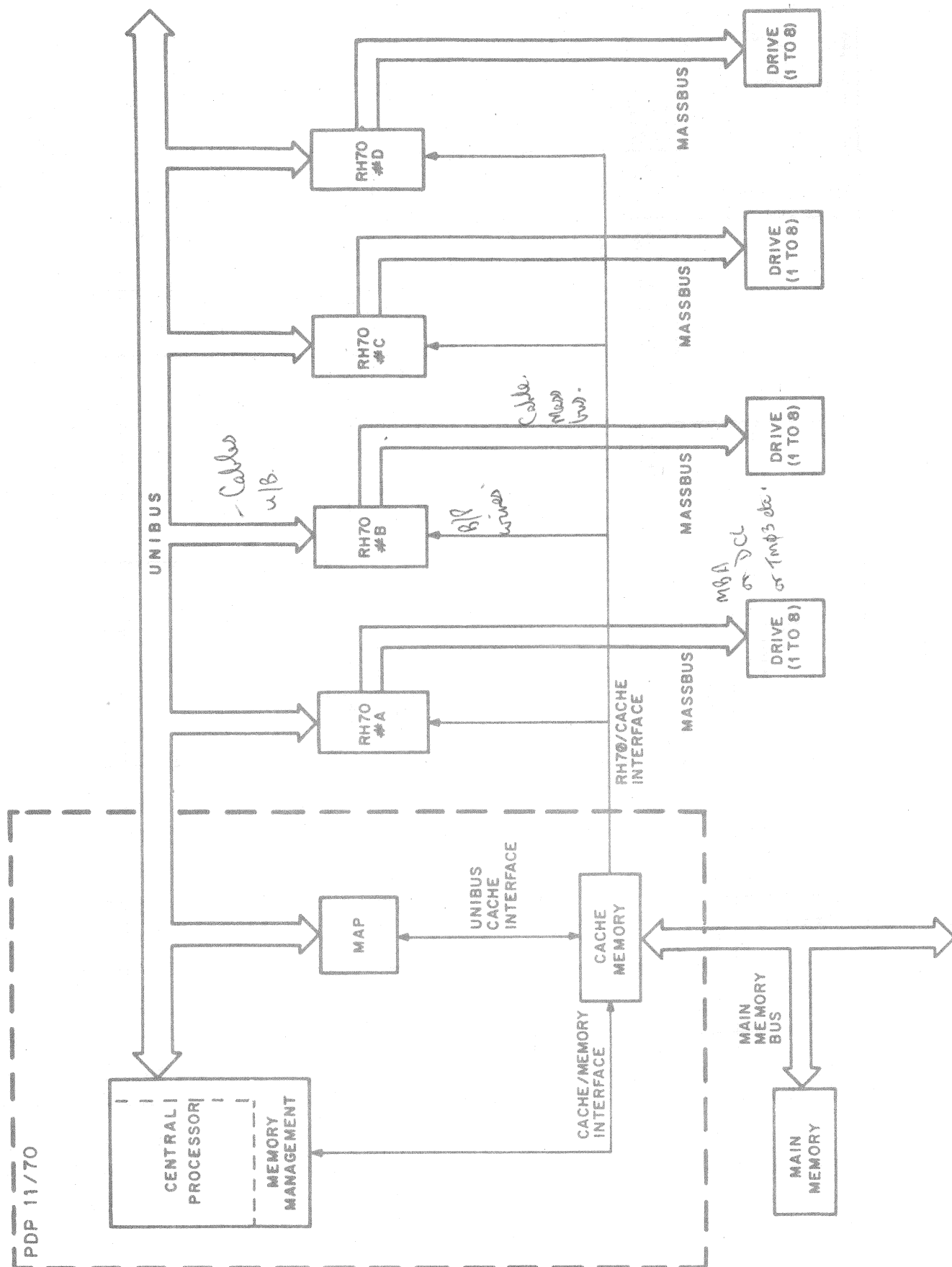
Daisy-Chain Power Sequence

5.4

Comparison Chart of PDP-11 DECdisk Specifications

5 NB. figures for
RM03
CABLES
BK5--
BK8--

MANUFACTURER (MODEL #)	RS 64 RC 11	RS 08-11 RS 09 RS 11 RF 11	RS 03 RH 11	RS 04 RH 11	RX 01 (FLOPPY)	RK 05-11 RK 11	RK 05-F RK 11	R2 02 R2P 11C R2P 11C	REPLS RP 11	RM 01 DCL RH 11	MEMOREX (677-51)	RP 05 DCL RH 11	RP 06 DCL RH 11	RK 06 RKC 11	RM 03 MBA RH	RL 01 RL 11
TYPE OF DISK	DEC FIXED HEAD	DEC FIXED HEAD	DEC FIXED HEAD	DEC FIXED HEAD	CAL COMP (CENTURY-DATA) MOVING HEAD	DEC FIXED HEAD	DEC FIXED HEAD	MEMOREX (660-L)	I.S.S. (714 DEC)	I.S.S. (715 DEC)	I.S.S. (733 DEC)	MEMOREX (677-51)	MEMOREX (677-01)	DEC DISK PACK, REMOVABLE	CONTROL DATA (BK5B5610)	DEC
MEDIA	10" NI-CO PLATED, NON-REMOVABLE	16" NI-CO PLATED, NON-REMOVABLE	16" NI-CO PLATED, NON-REMOVABLE	16" NI-CO PLATED, NON-REMOVABLE	IBM "DISKETTE" CARTRIDGE, REMOVABLE	IBM 2315 CARTRIDGE, REMOVABLE	IBM 2315 CARTRIDGE, NON-REM.	IBM 2316 DISK PACK, REMOVABLE								DEC 5440 MODIFIED CARTRIDGE, REMOVABLE
CAPACITY (ONE DISK)	65 KW	262 KW	262 KW	524 KW	128 KW	1.2 MW	2.4 MW (2 LOGICAL UNITS)	10 MW					88 MW	6.9 MW	40 MW	2.5 MW
MAX # DISKS/CONTROL	4	8	8		2	8	3 PHYSICAL UNITS; 6 LOGICAL	8								4
# WORDS PER SECTOR	32	1	64	128	64	256										128
# SECTORS PER TRACK	64	2048	64	64	26	12									32	40
# TRACKS PER SURFACE	32	128	64	64	77	203	406	203					815	411	823	256
# DATA SURFACES	1			2	1	2		20						3	5	2
BIT CELL TIME	835 ns	720 ns	203 ns	164 ns (EFFECTIVE)	4 us	690 ns	690 ns	400 ns	400 ns	155 ns				232 ns	103 ns	244 ns
WORD XFER RATE	14 us	16 us	8 us	2 us FOR SHORT XFERS (4 us OK)	36 us	11 us	11 us	7.4 us	7.4 us	2.5 us				3.7 us	1.65 us	3.9 us
MAX. ACCESS TIME	13 ms	33 ms	17 ms	17 ms	1000 ms	85	85 ms	60 ms	55 ms	52 ms		53 ms	53 ms	67 ms	52 ms	100 ms
MAX. BIT DENSITY	1000 BP1	1500 BP1	2200 BP1	2200 BP1	3200 BP1	2200 BP1	2200 BP1	2200 BP1	2200 BP1	4040 BP1					6000 BP1	3725 BP1
RECORDING METHOD	NRZI	NRZI	NRZI	NRZI	FM	FM	FM	FM	FM	FM						
TIMING OR SERVO TRACKS	CLOCK (A) MARK (B) ADDR (C) DELIMIT (C)	CLOCK (A) MARK (B) ADDR (C) DELIMIT (C)	CLOCK TRACK	CLOCK TRACK	SOFT SECTOR	NONE	NONE	NONE	NONE	TRACK FOLLOWING SERVO						SERVO IN-DATA TRACK FOLLOWING
MOTOR SPEED	1000 R.P.M.	1000 R.P.M.	3500 R.P.M.	3500 R.P.M.	360 R.P.M.	1500 R.P.M.	1500 R.P.M.	2400 R.P.M.	2400 R.P.M.	3600 R.P.M.				2400 R.P.M.	3600 R.P.M.	2400 R.P.M.
POSITIONING SYSTEM	NONE				STEPPING MOTOR, NO. DETENT	LINEAR MOTOR, ELECTRONIC DETENT		LINEAR MOTOR, MECHANICAL DETENT								DC MOTOR ELECTRONIC DETENT

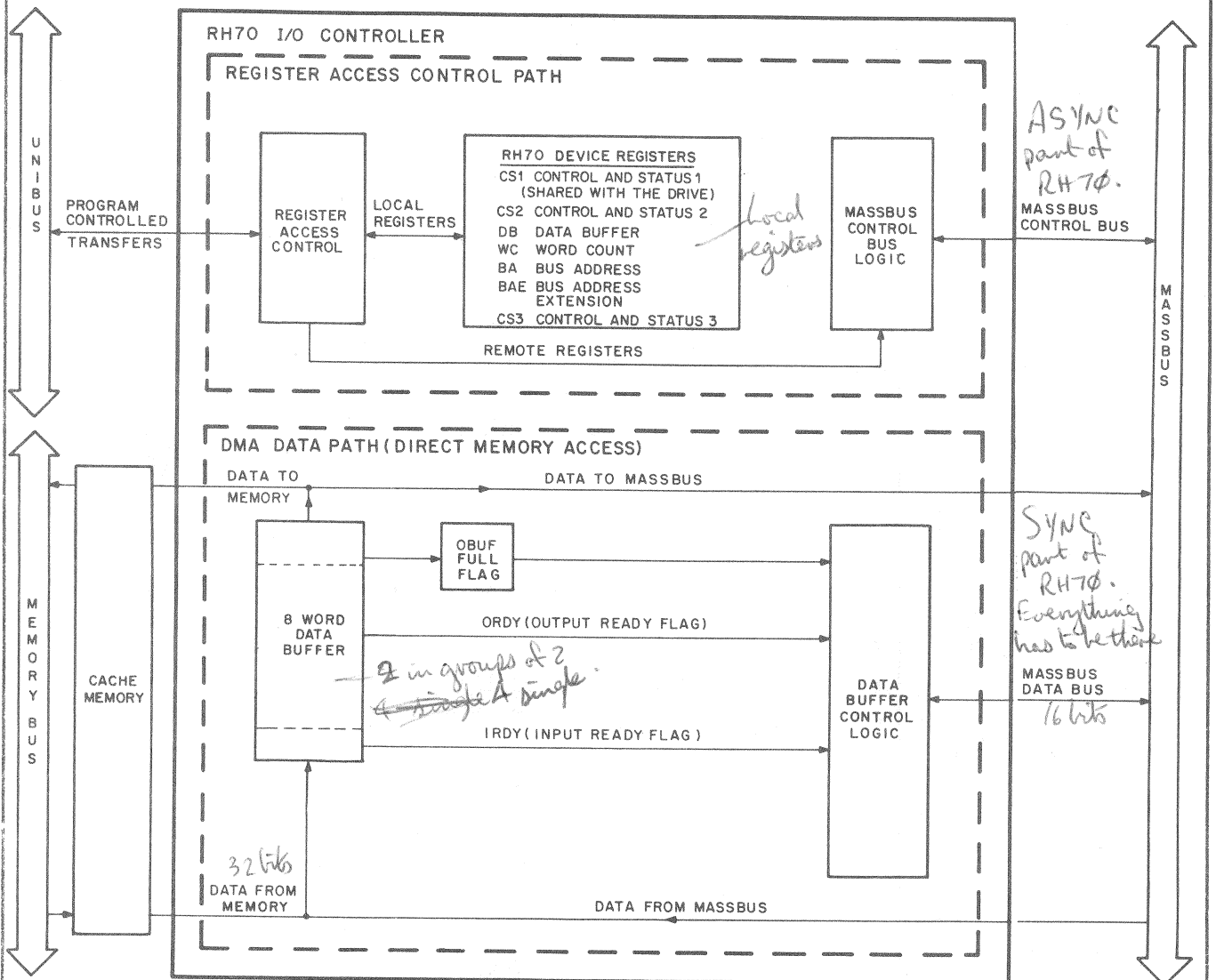


Up to 4 R47d.
Previous BP.

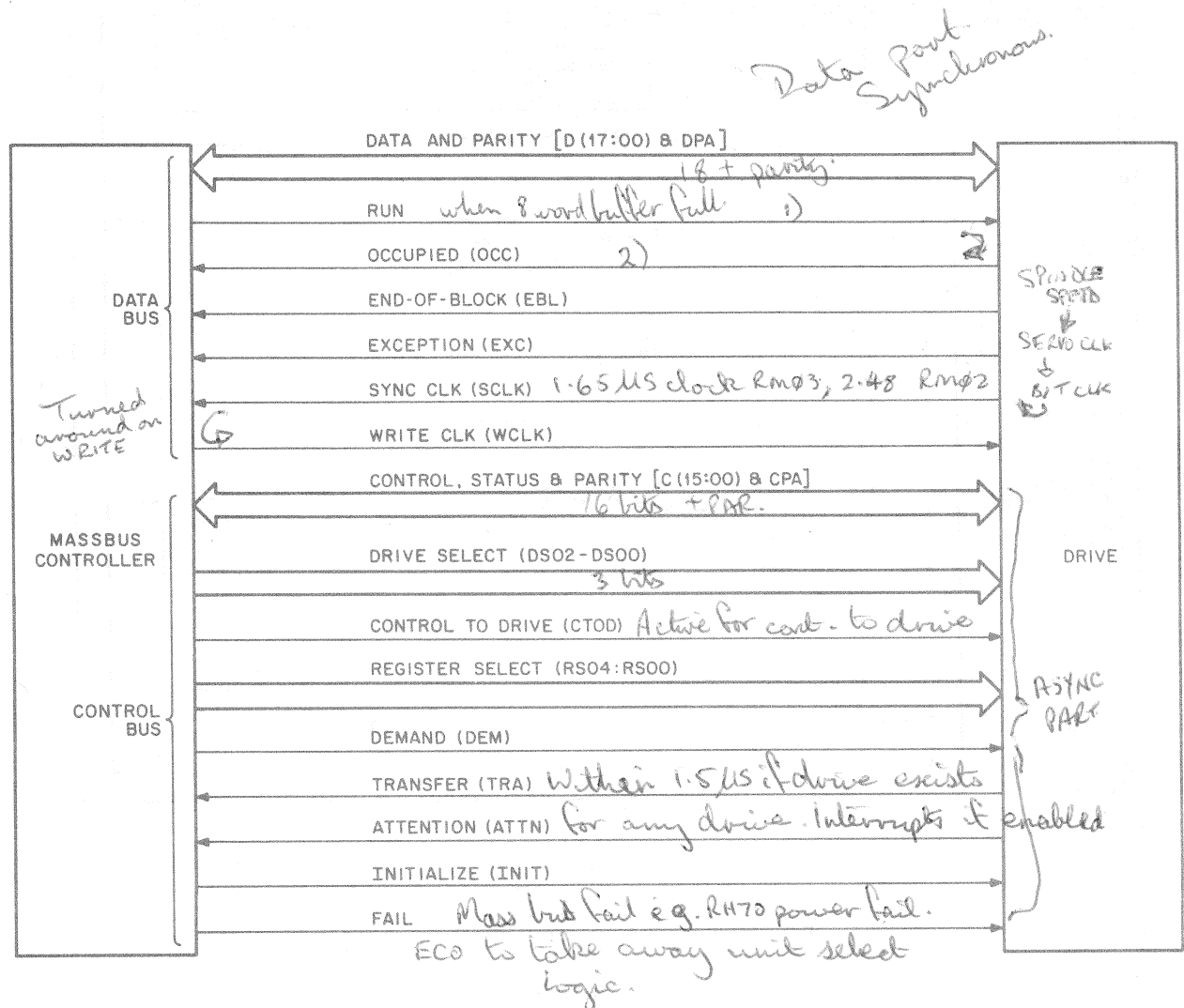
u/b control
moderate -
CSR &
Vector set up
Grant card if non-existent.

Logic Print	Functions
BCTA	Register Selection
BCTB	SSYN and Demand Logic
BCTC	Unibus Interrupt Logic
BCTD	Unibus Data Transceivers
AWRA	Bus Address Reg (11:01)
AWRB	Bus Address and Extension (21:12) and Control Parity Out
AWRC	BUSI MUX (BA and BAE Registers) and Address Drivers
AWRD	Word Count Register (07:00)
AWRE	Word Count Register (15:08) and WC OFLO
AWRF	BUSI MUX (WC and Remote Registers) and MCPE
MDPA	Memory Register Control
MDPB	Even Word Memory Data Registers and Mixer
MDPC	Odd Word Memory Data Registers and Memory Parity Generator/Checkers
MDPD	Data Registers Control
MDPE	Write-Check Logic, Clock RE and Data Parity
MDPF	Data Buffer Registers
MDPH	IMX and Data Drivers
MDPJ	Data Path Block Diagram
CSTA	CS1, CS2, and CS3 Control and Status, Function Select
CSTB	Errors, IE, Intr. Req. and Massbus Control
CSTC	PE, NEM, and Memory Cycle Control
CSTD	BUSI MUX (CS1 and CS2 Registers) and Clear Logic
CSTE	BUSI MUX (DB and CS3 Register) and START Logic
MBSA	Massbus Transceiver (Massbus Cable A)
MBSB	Massbus Transceiver (Massbus Cable B)
MBSC	Massbus Transceiver (Massbus Cable C)

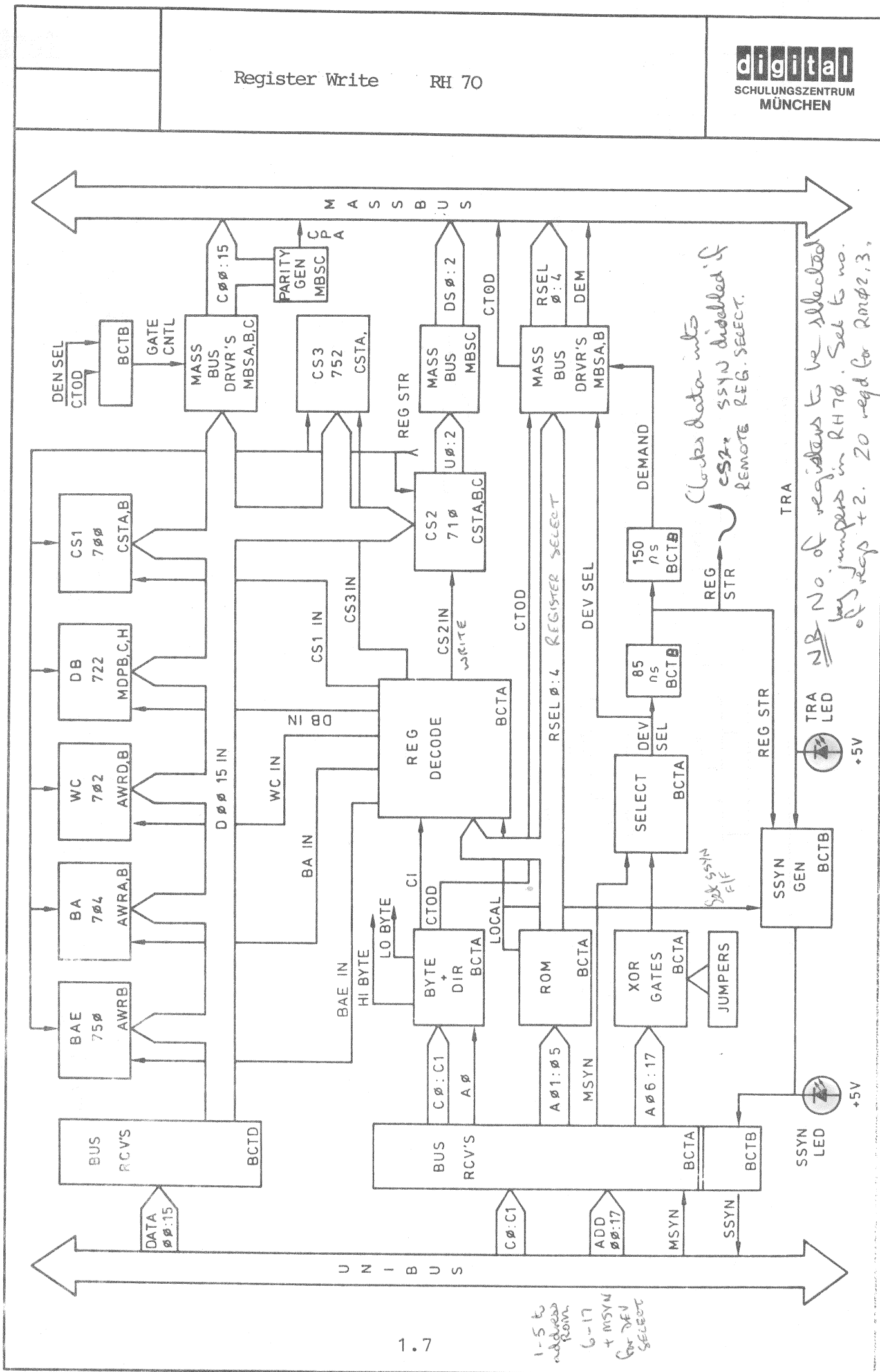
RH70 SIMPLIFIED DATA PATH DIAGRAM



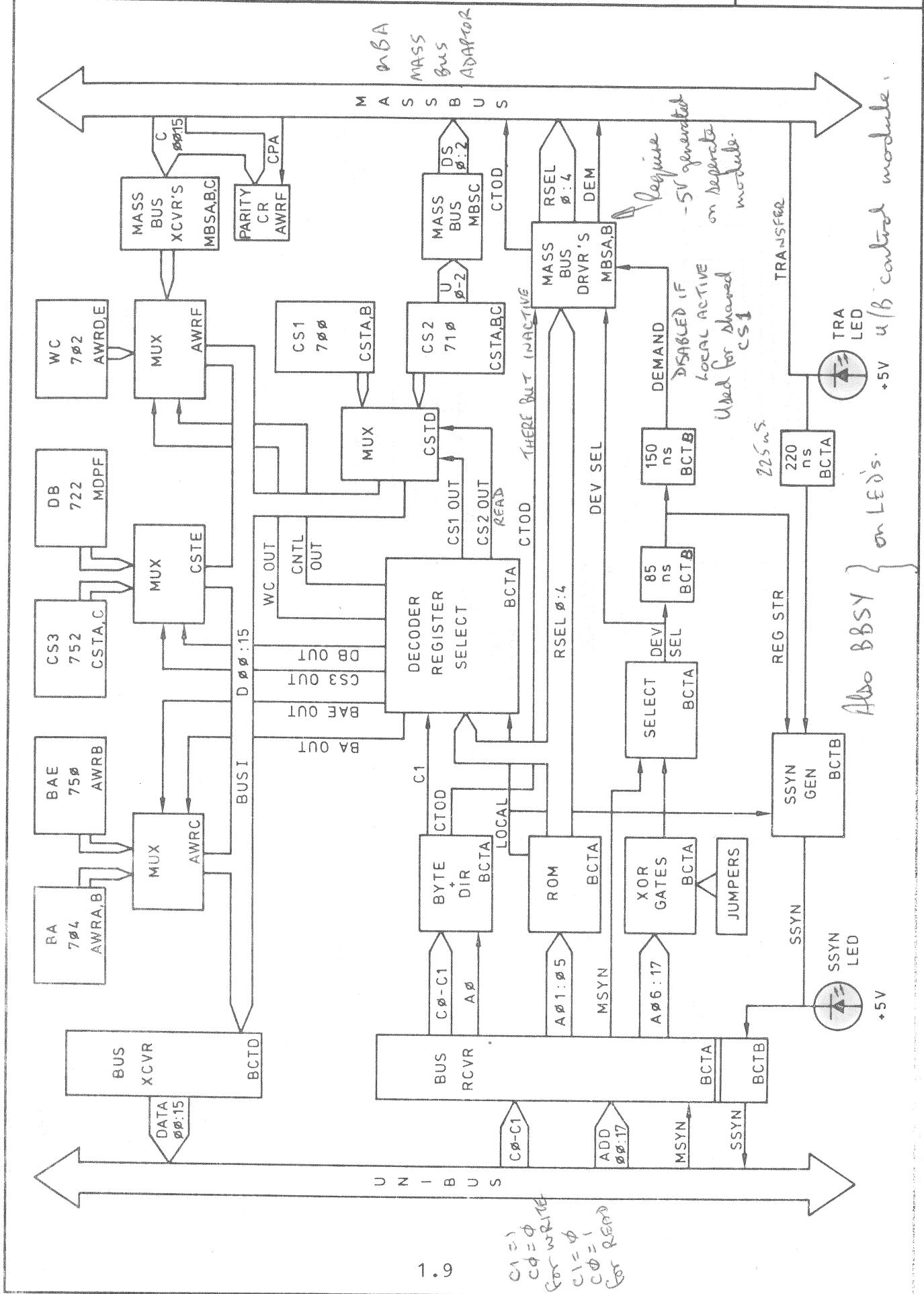
CS1 776700 VECT 254
RMCS2 776710
RMDC 776734

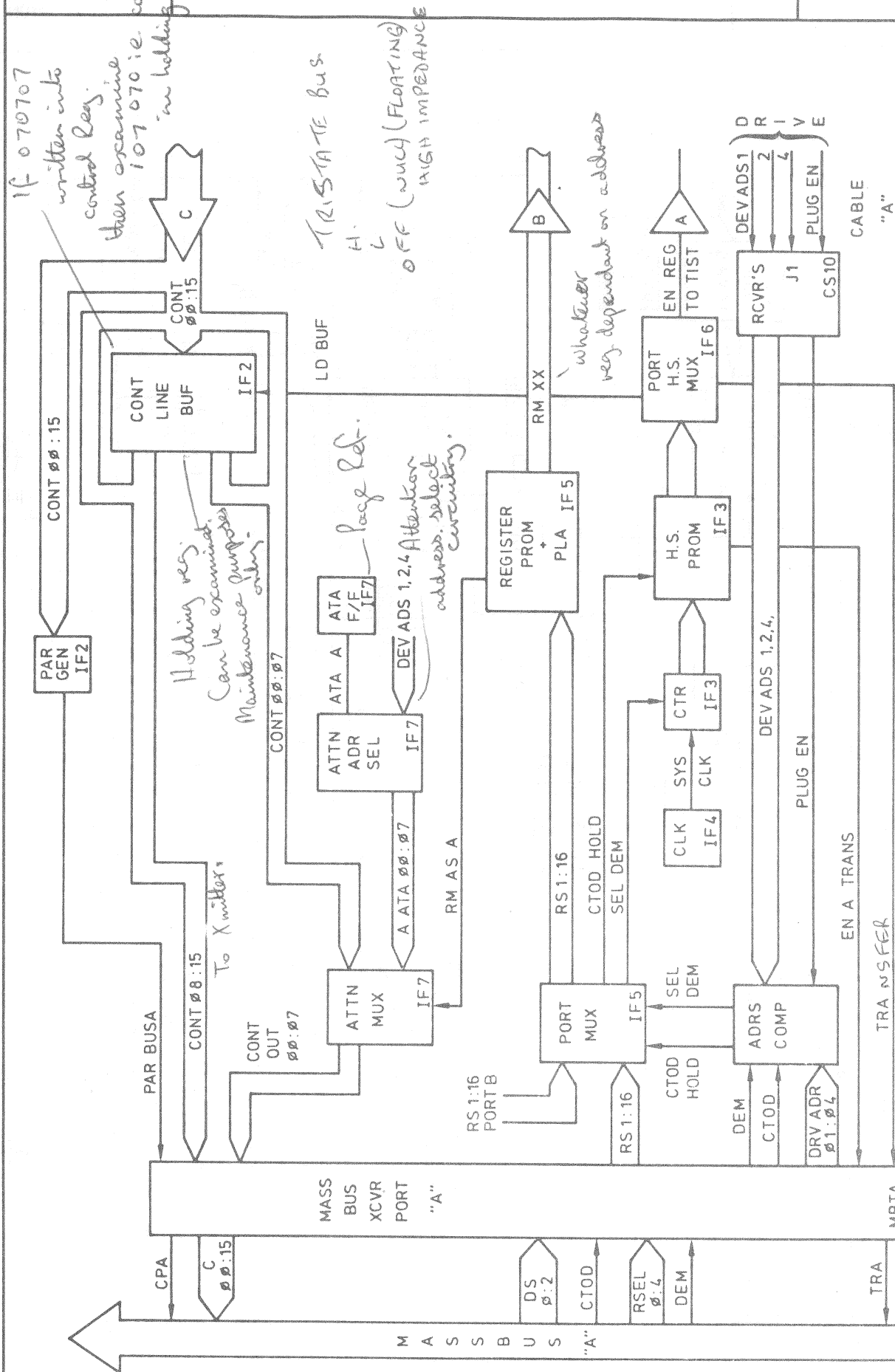


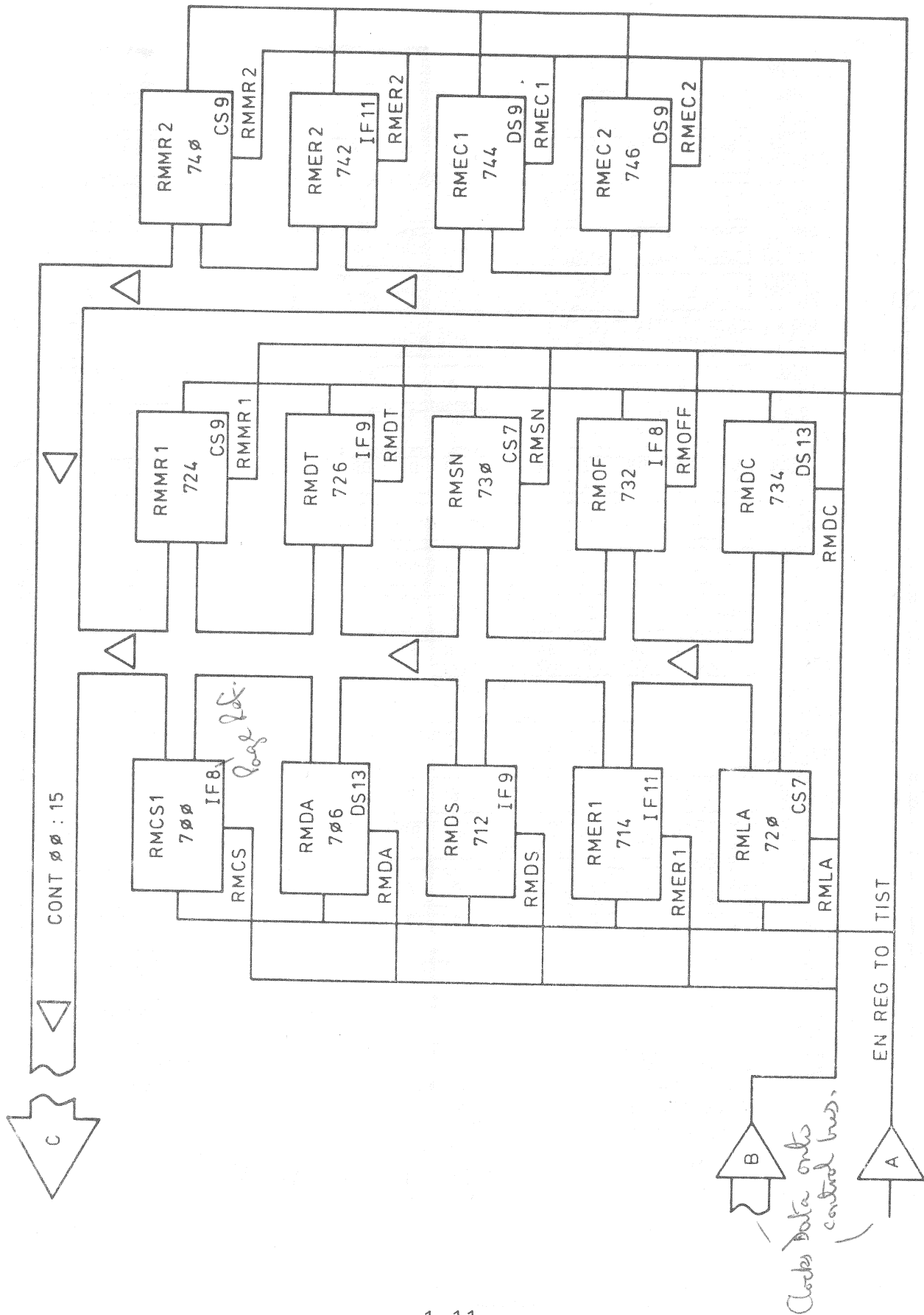
↑
EBL.
if a error then
exception signal











RWM 03 REGISTERS

digital
SCHULUNGSZENTRUM
MÜNCHEN

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																		
* RMCS1 776700	SC	TRE	MCPE	DVA	0	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO	R/W		
* RMWC 776702	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC 0	R/W	
* RMBA 776704	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 9	BA 8	BA 7	BA 6	BA 5	BA 4	BA 3	BA 2	BA 1	BA 0	R/W	
RMDA 776706	0	0	0	FAT EXPANS.	TA 4	TA 2	TA 1	0	0	0	SA 16	SA 8	SA 4	SA 2	SA 1	SA 0	R/W	
* RMCS2 776710	DLT LATE	WCE	PE	NE	DR	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0	UNIT SELECT
RMDS 776712	ATA	ERR	PIP	MED	MOL	WRL	LBT	PGM	DPR	DRY	VOL	0	0	0	0	0	OM	OFFSET MODE
RMER1 776714	DCA	UNS	OPI	DTE	WLE	ILL	IAE	AOE	HCR	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF	RESET TO CENTER LINE
RMAS 776716	0	0	0	0	0	0	0	0	ATA	ATA	ATA	ATA	ATA	ATA	ATA	ATA	ATA	R/W
RMLA 776720	0	0	0	0	0	SC 16	SC 8	SC 4	SC 2	SC 1	0	0	0	0	0	0	0	R
* RMDB 776722	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0	DB 0	R/W
RMRR1 776724	OCC	R/G	EBL	REX	ESR	PLF	SEC	RCD	PDA	PHA	CONT	PS	EECC	WD	LS	LST	DMD	R or RHD SILE
RMRR1 776724	DC	DCE	DEBL	STD	MC	MRD	MUR	MOC	MSE	MDF	MSP	SPR	MWP	MI	MSC	DMD	DMD	W
RMDT 776726	NBA	TAP	NOH	0	DRQ	0	0	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT 0	DT 0	R
RMSN 776730	SN 8XXX	SN 4XXX	SN 2XXX	SN 1XXX	SN 8XX	SN 4XX	SN 2XX	SN 1XX	SN 8X	SN 4X	SN 2X	SN 1X	SN 8	SN 4	SN 2	SN 1	SN 0	R
RMOF 776732	0	0	0	FMT	ECI	HCI	0	0	OFD	0	0	0	0	0	0	0	0	R/W
RMDC 776734	0	0	0	0	0	0	DC 512	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1	DC 0	R/W
RMHR 776736	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W
RMRR2 776740	REQ A	REQ B	TAG	TST BIT	CTL CYL	CTL HD	BB 9	BB 8	BB 7	BB 6	BB 5	BB 4	BB 3	BB 2	BB 1	BB 0	BB 0	DEPENDANT R ON TAG1 TAG2 TAG3
RMER2 776742	BSE	SKI	OPE	INV	LSC	LBC	0	0	DVC	0	0	0	0	DPE	0	0	0	R/W
RMEC1 776744	0	0	0	P 4096	P 2048	P 1024	P 512	P 256	P 128	P 64	P 32	P 16	P 8	P 4	P 2	P 1	P 0	R
RMEC2 776746	0	0	0	0	0	PAT 11	PAT 10	PAT 9	PAT 8	PAT 7	PAT 6	PAT 5	PAT 4	PAT 3	PAT 2	PAT 1	PAT 0	R
* RMBAE 776750	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16	A15	R/W
* RMCS3 776752	APE	DPE OW	DPE EW	WCE OW	WCE EW	DBL	0	0	0	IE	0	0	IPCK 3	IPCK 2	IPCK 1	IPCK 0	IPCK 0	R/W

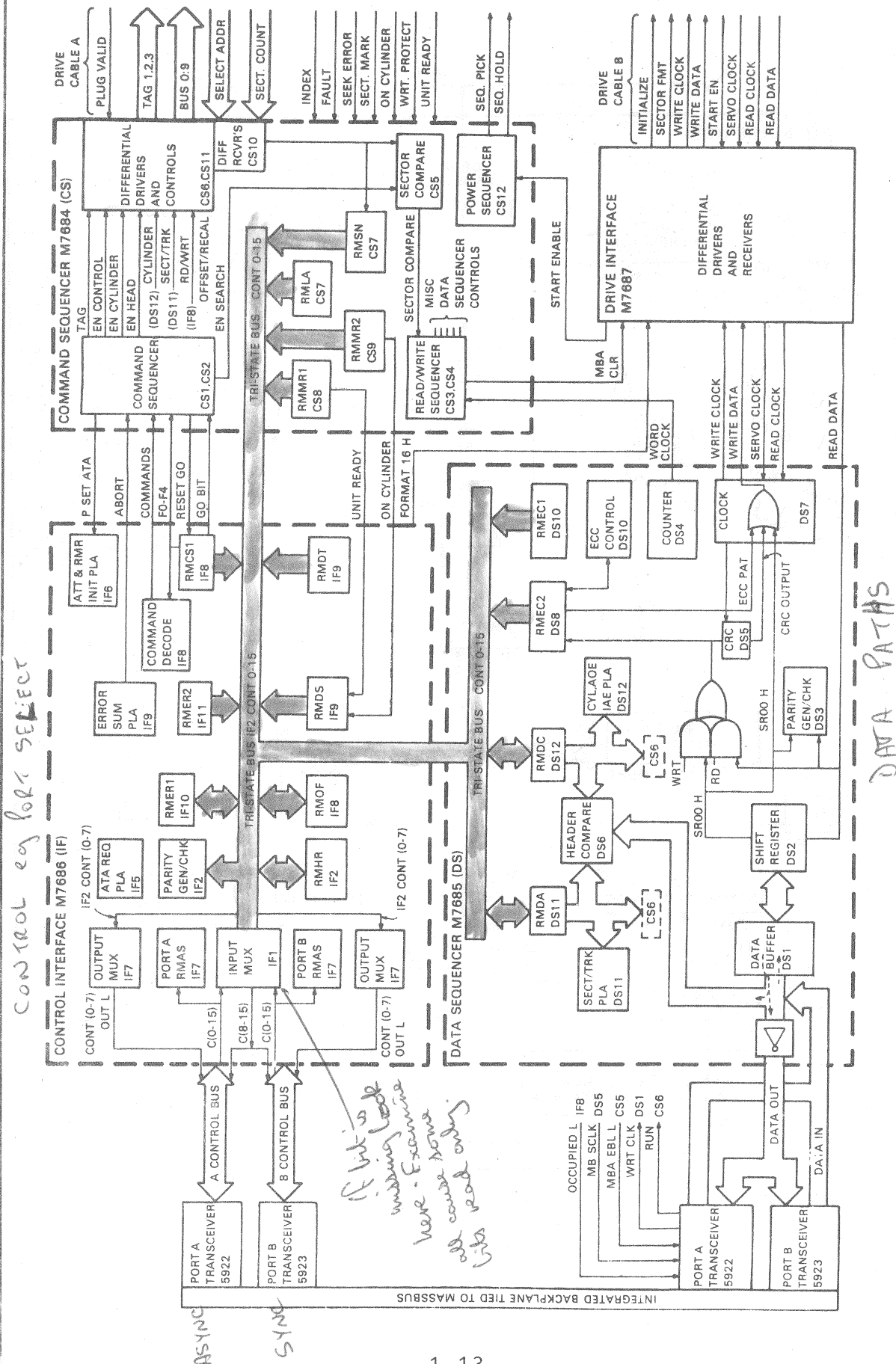
* = LOCATED IN THE RH70
i.e. LOCAL REG.
EVEN WORD
ODD WORD
SINGLE WORDS XFER WHEN ODD THEN DOUBLE NEXT. When WC = -1 or Bus Address Inopen inhibited

Special condition
13# 15 all Rem. Parity Error
Device Avail. Remote
PSEL
address bits (16)17
Remote Function
Data STR. Late
Data STR. Early
in Future
DISK STATUS
Maintenance
20020 Rm#3
20025 Rm#2
240xx Dual Port
Holding Register
Maintenance
NB care with A16 & A17
Ecc reg.
RH70 not RH11

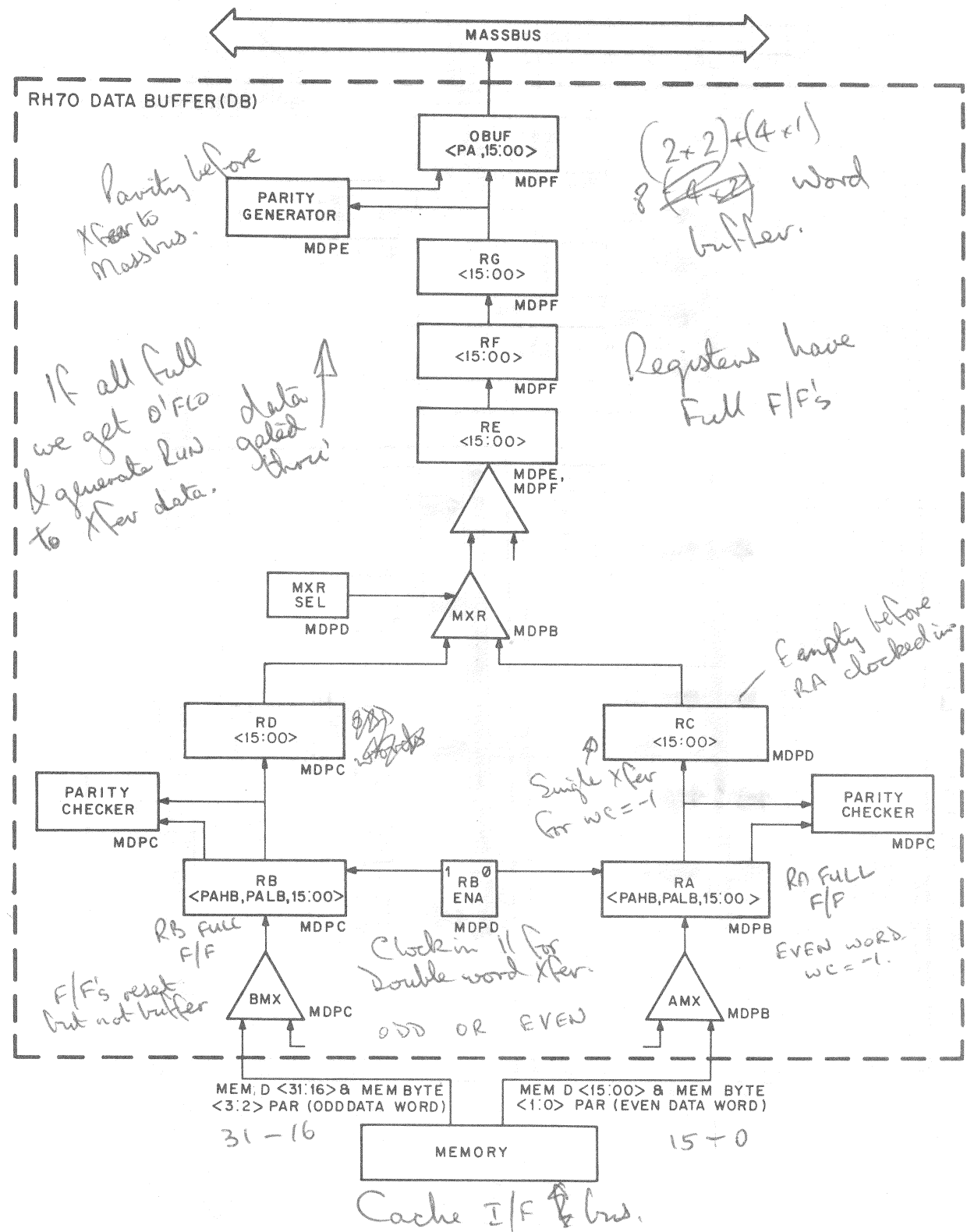
TAG	HD	CYL	TAG
TAG1	0	1	1
TAG2	1	0	1
TAG3	1	1	1

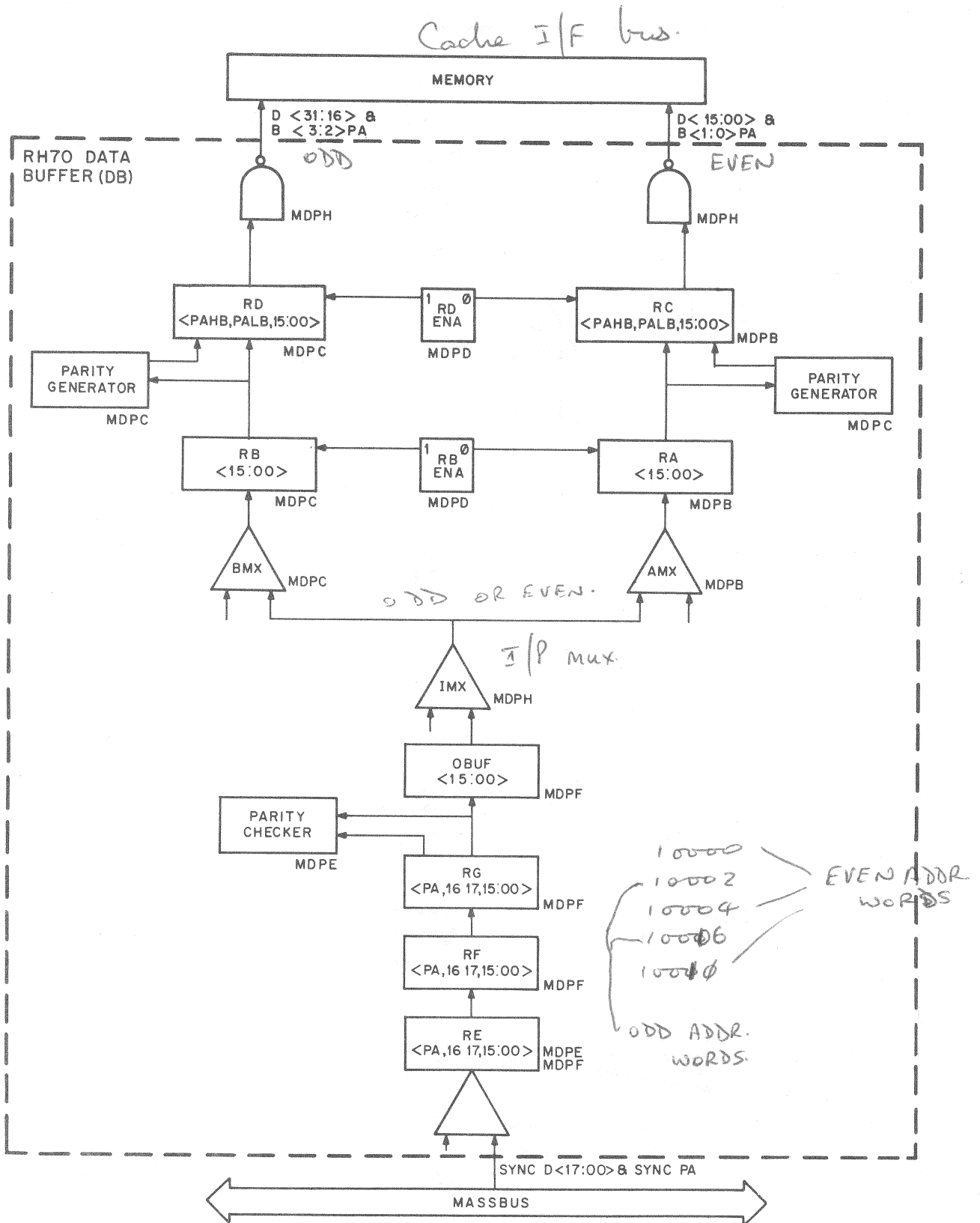
See page 4:19 User Manual

MBA Block Diagram



WRITE COMMAND DATA PATH

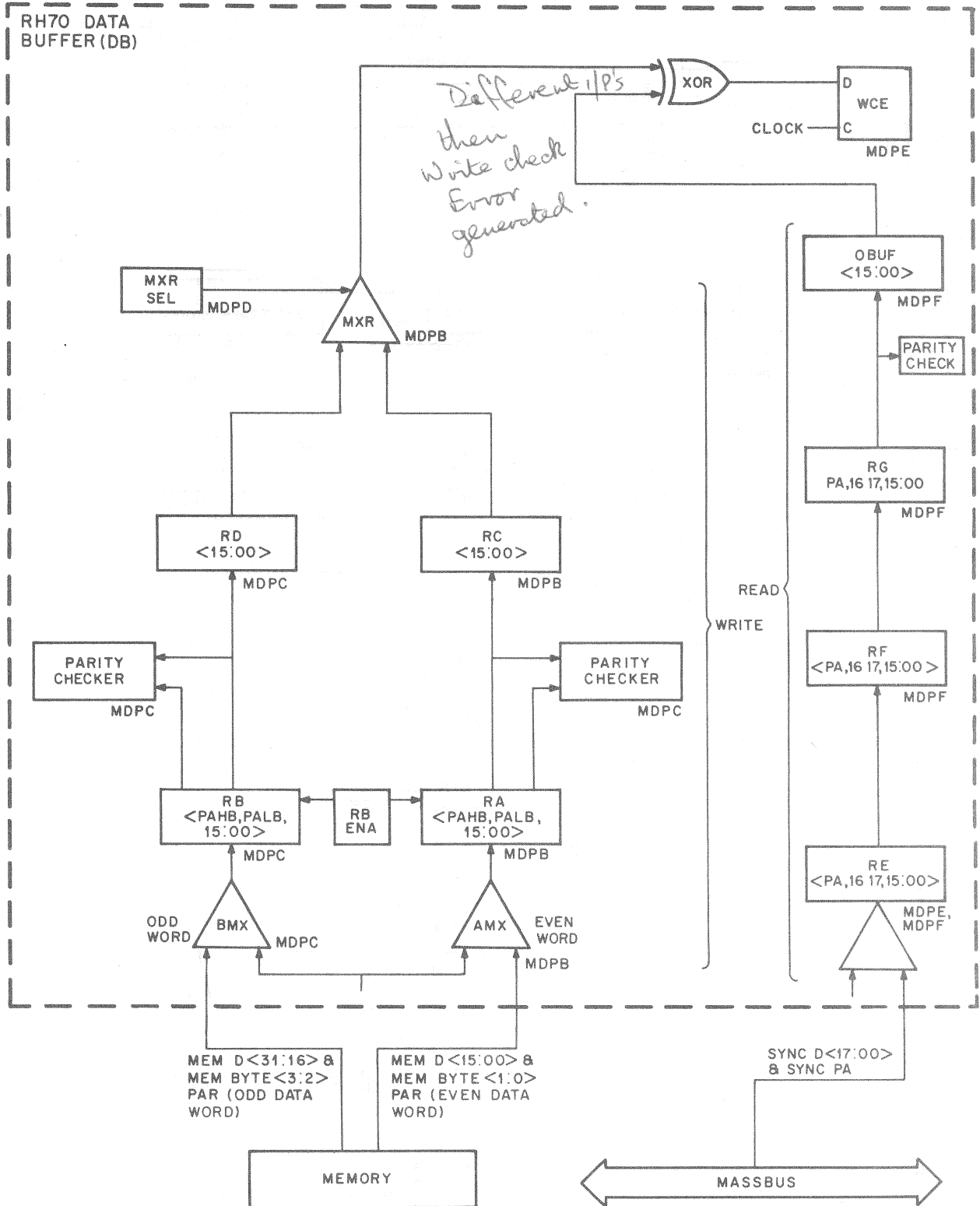


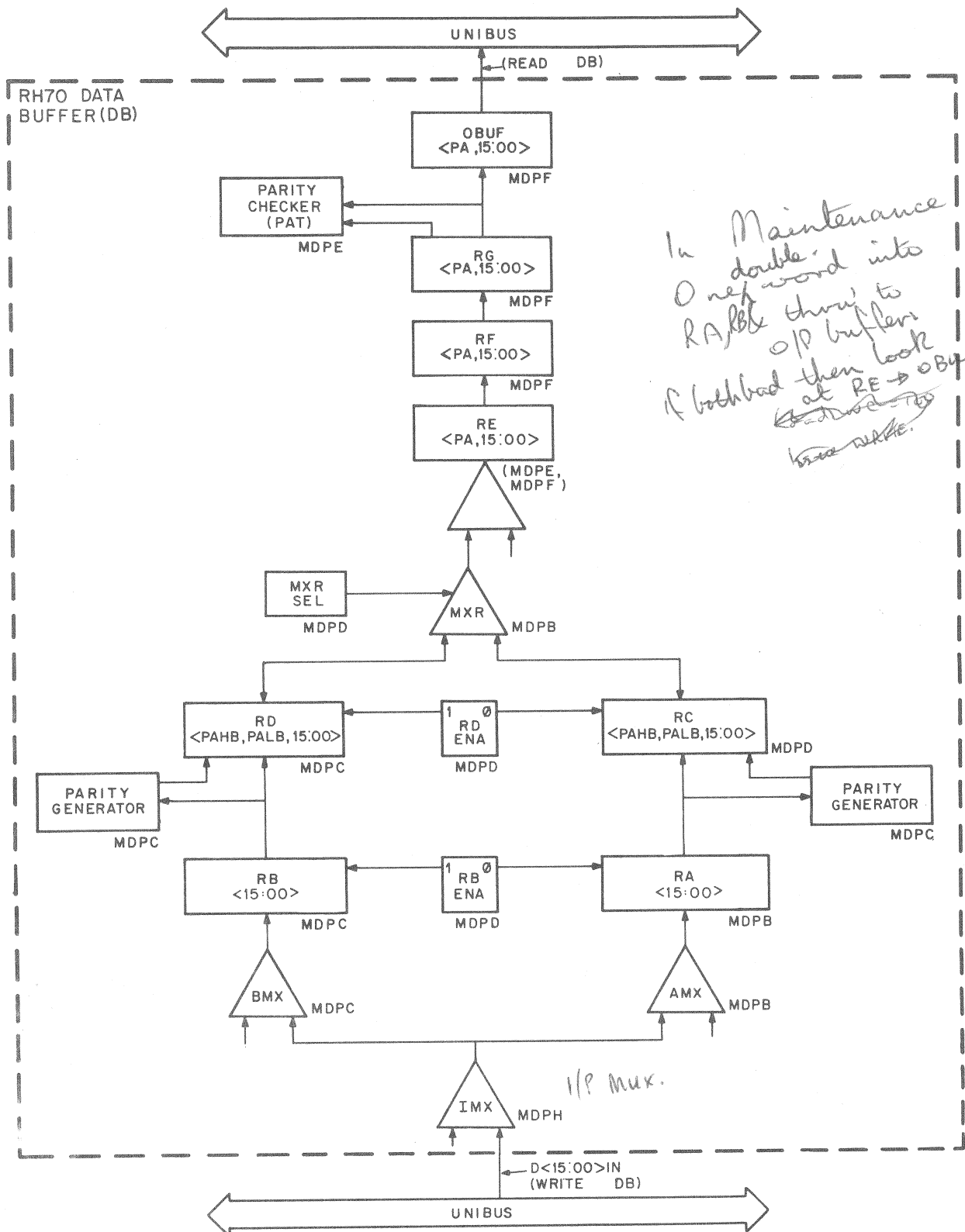


WRITE-CHECK COMMAND DATA PATH

Read from disk pack & memory.

Can remove jumpers to eliminate WCE's

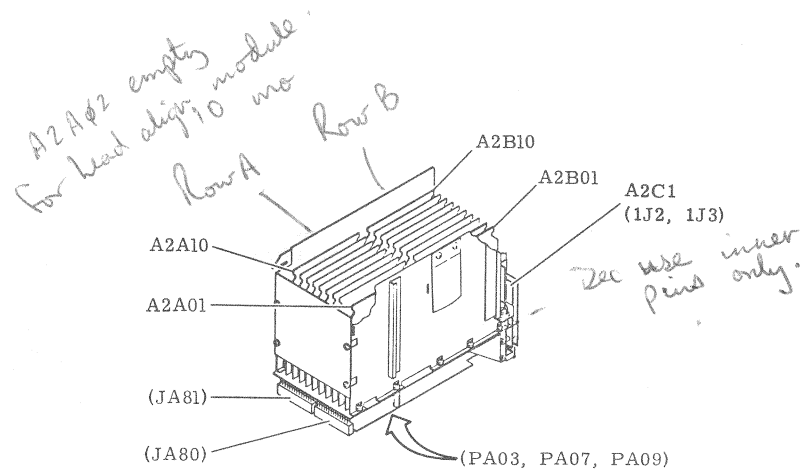




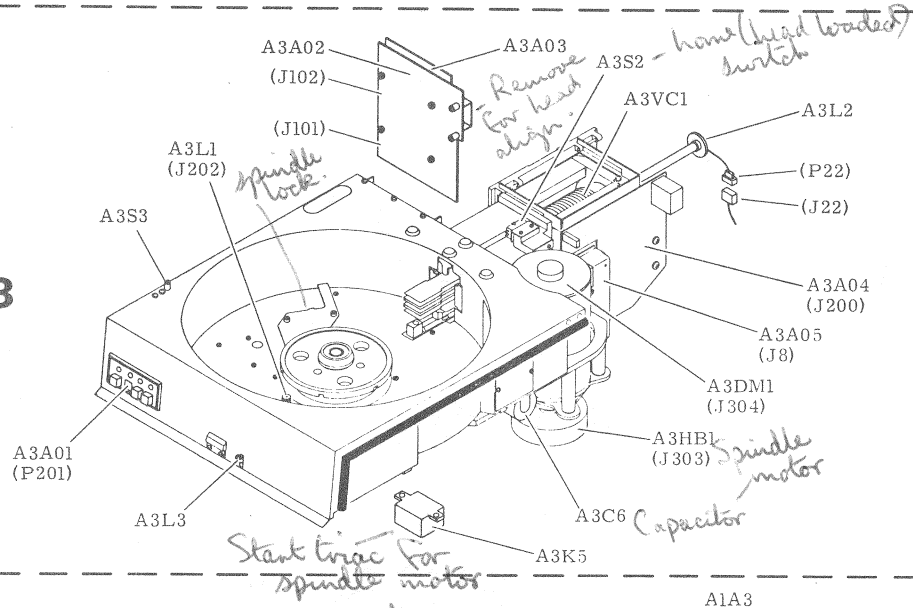
000000
000000
000000

—

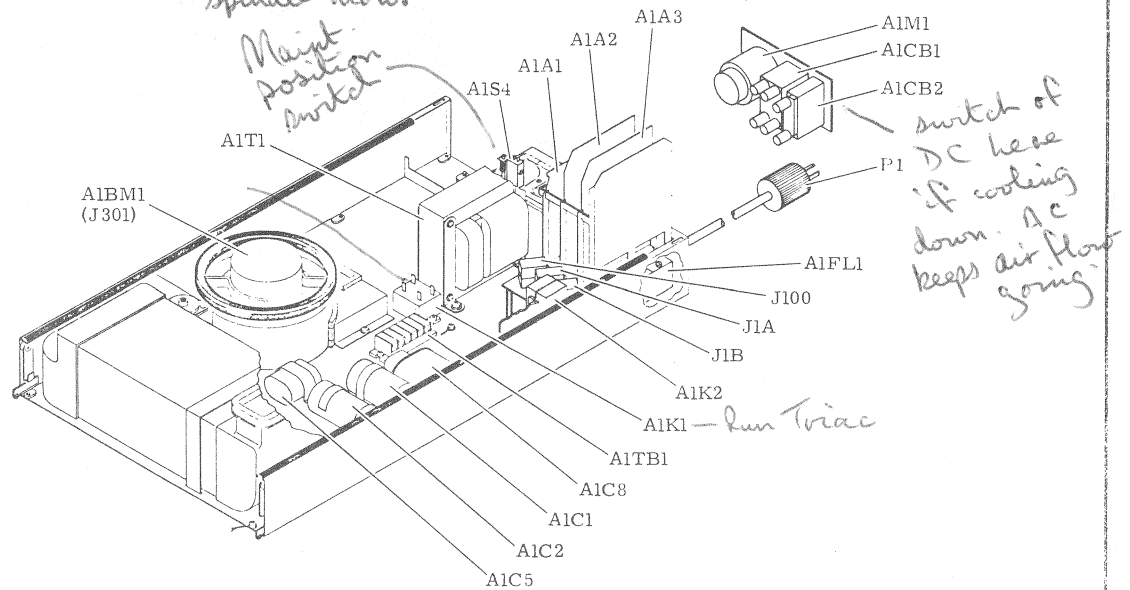
A2

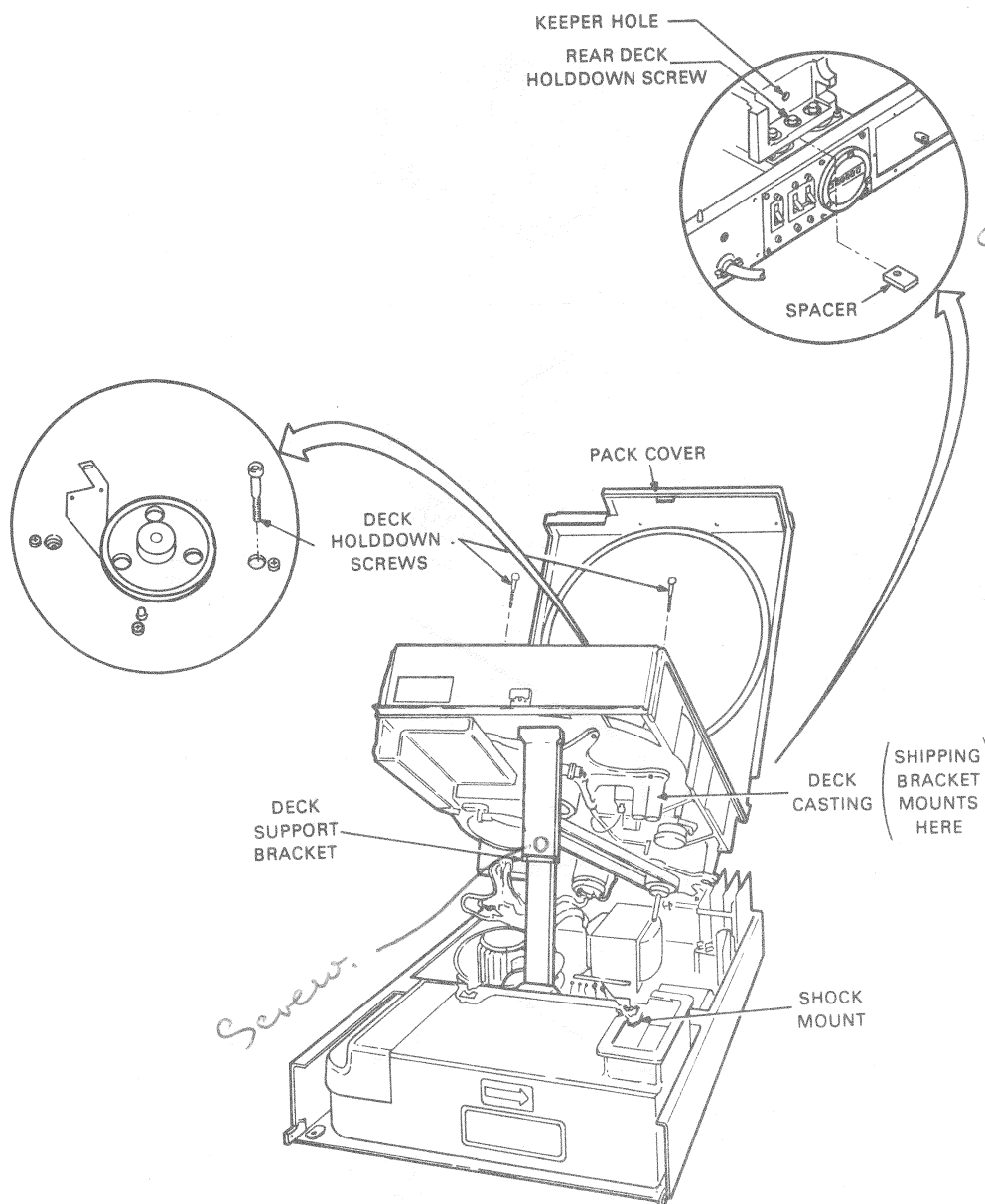


A3



A1





$\overline{OC} \bullet (W+R)$
A04CR5

R•W
A04CR4

HD SEL
A04CR3

WRITE
A04CR2

VOLTAGE
A04CR1
 $\pm 12V$
 $\pm 5V$ $\pm 42V$

A10S1
LOCAL/REMOTE
← LOCAL → REMOTE

A04S1
MAINT FAULT
CLEAR
← CLEAR → NORM

*not oncyt. & work.
at same time*

*Sometimes gives
unwanted voltage
faults.*

*Fault detect
module*

*{PWR SEQ PICK
PWR SEQ HOLD
Can start
drive in
local. 2 signals
from MBA req'd
to start in
remote*

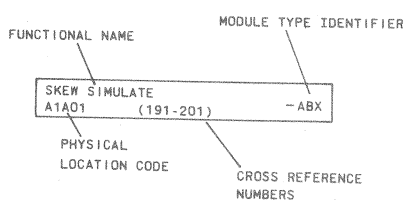
*Velocity
adjust
for linear
motor speed.
Only one
in drive*

Module AΦ3
Sheets 1-5.

* 031-035

Φ3 = AΦ3

IF 131 13 = BΦ3



±5 V POWER SUPPLY	-SHV
A1A03 (331-333)	
±12 V AND ±20 V	-SKV
A1A02 (321-322)	
±42 V PWR SUPPLY & EMERGENCY RETRACT	-SJV
A1A01 (311-312)	

TRACK SERVO PREAMP	-ZQN
A3A05 (291-292)	
POWER AMPLIFIER	-VTN
A3A04 (281-282)	

LINEAR MOTOR

FOR

Rev

module name.
names on chassis

TRANSMITTERS	-TVV	WRITE CLOCK 806 KHz	-LSV
A2B01 (111-113)		A2A01 (011-013)	
RECEIVERS	-RVV	FTU/HEAD ALIGNMENT CARD SLOT	
A2B02 (121-124)		A2A02 (021-022)	
①		FINE SERVO DECODER	-FRV
①		A2A03 (031-035)	
①		FAULT CARD	-KPV
		A2A04 (041-045)	
DIFF GEN AND CONTROL	-LWV	DATA LATCH	-LRV
A2B06 (161-165)		A2A05 (051-053)	
NRZ TO COMPENSATED MFM	-LVV	READ PLO	-LVZ
A2B07 (171-173)		A2A06 (061-065)	
ACCESS CONTROL & INDEX/SEE DECODE	-LTV	D/A FUNCTION GENERATOR	-LQV
A2B08 (181-184)		A2A07 (071-073)	
ACCESS CONTROL NO. 1	-LVV	ACCESS CONTROL NO. 2	-LUV
A2B09 (191-194)		A2A08 (081-085)	
①		SWITCHING MODE CONTROL	-LPV
		A2A09 (091-093)	
		INTERLOCKS & SPEED DETECTOR	-SGV
		A2A10 (101-104)	

HEAD SELECT & READ AMPLIFIER	-ZJN
A3A02 (261-263)	
WRITER	-ZKN
A3A03 (271-274)	

OPERATOR CONTROL PANEL	-ZYN
A3A01 (251-252)	

FRONT

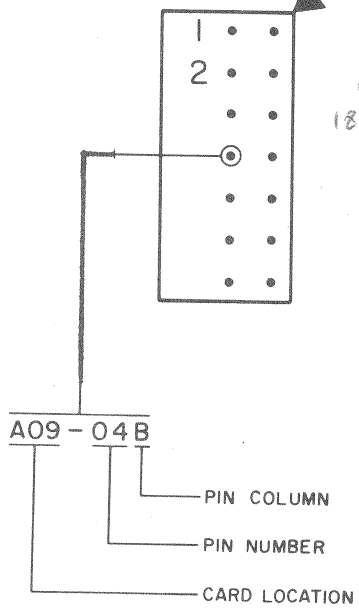
NOTE:
① NOT USED

Revision important

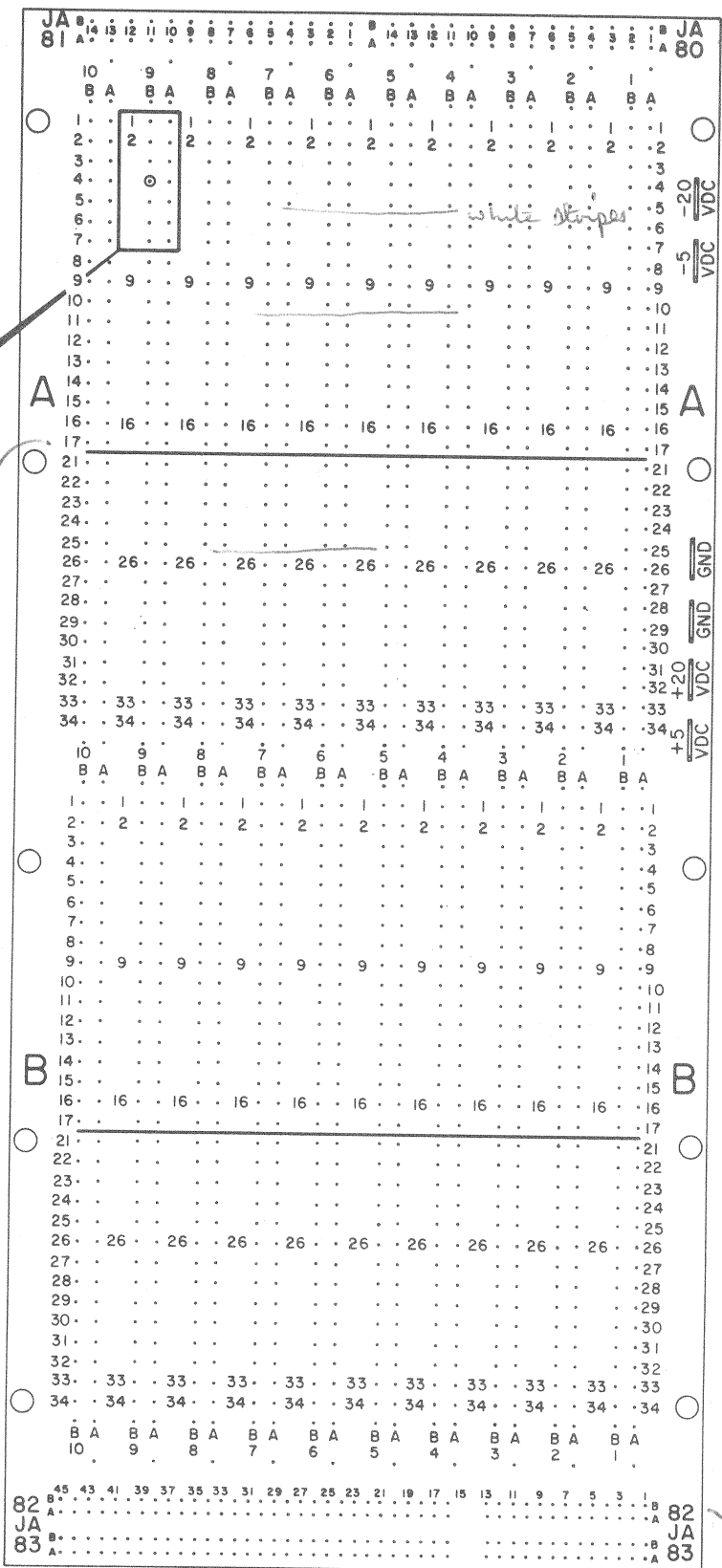
BACKPANEL LAYOUT

JA 80, 81. One to 9F/P other to R/W board.

Right
When sat on linear motor, which it must be for BIP access



NB
18, 19, 20

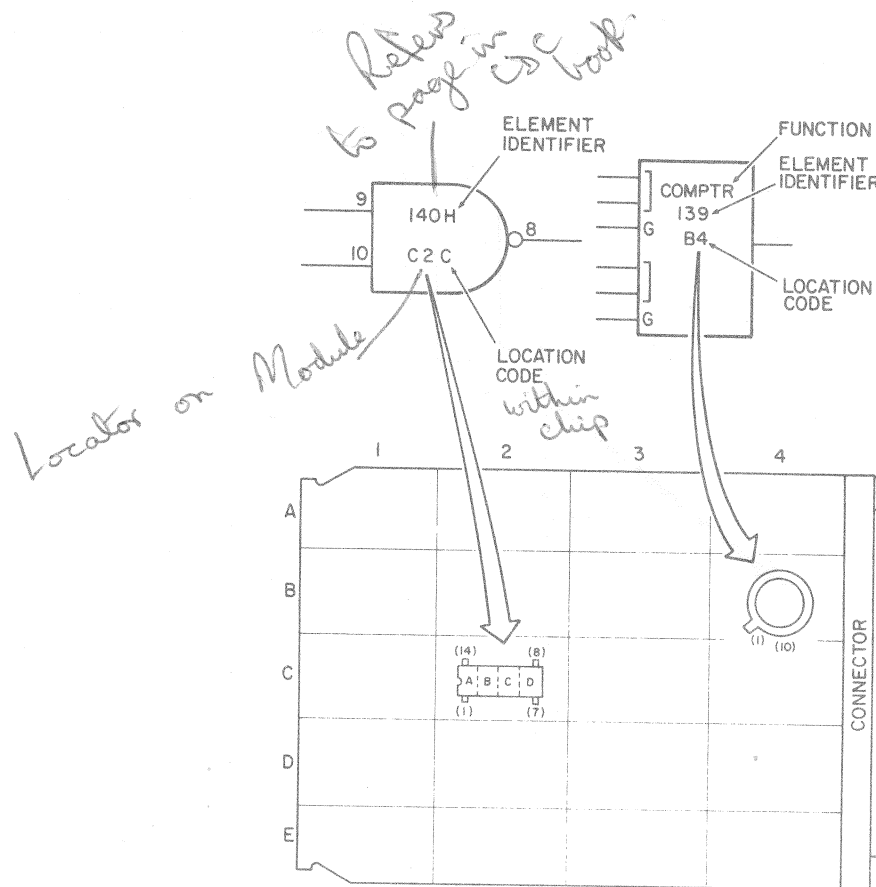


Left

A cable

B cable

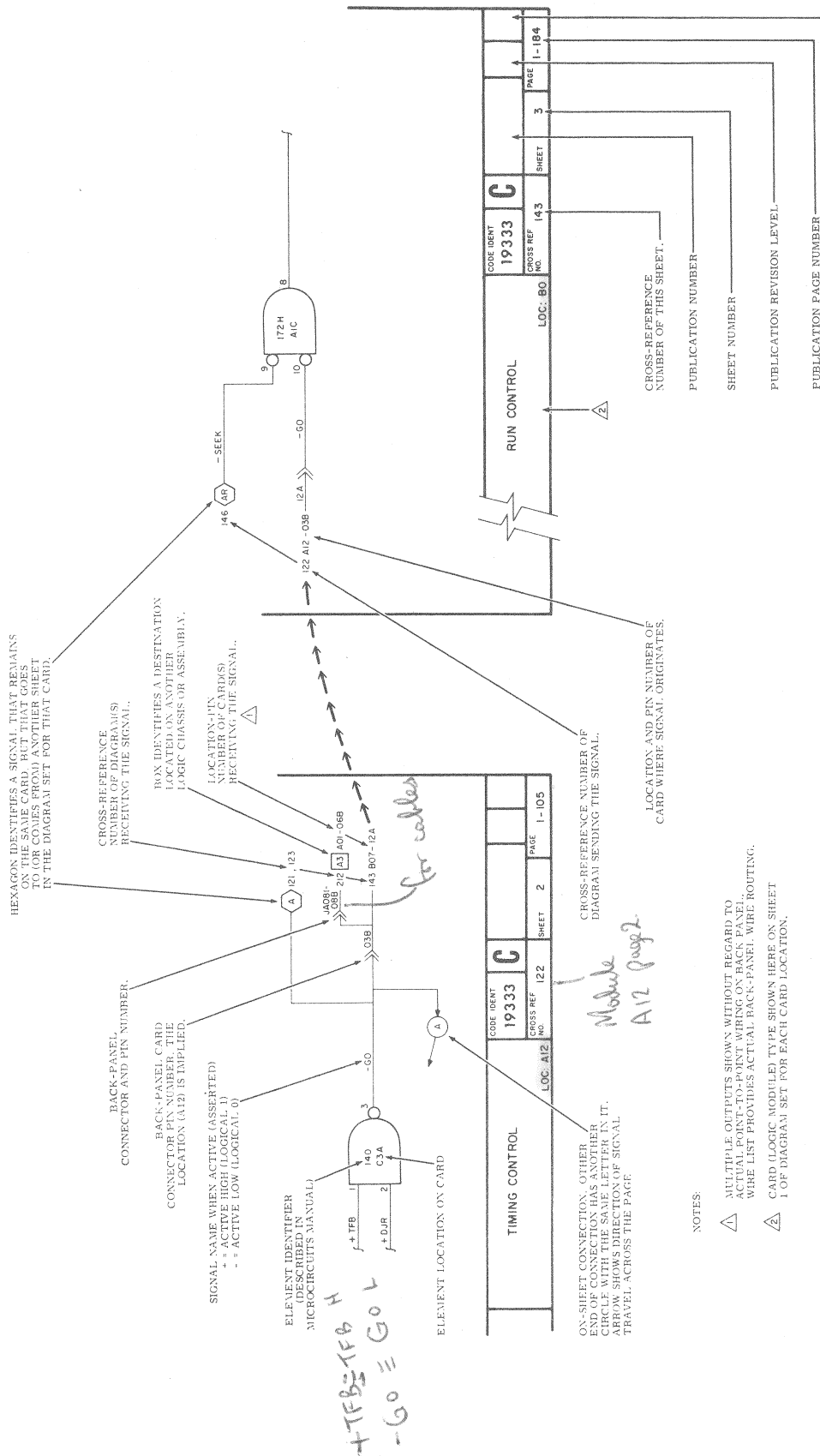
JA 83
not used



Logical State	Nominal Voltage	Typical Range
TTL "1"	+3 V	+2.5 V to +4.0 V *
TTL "0"	0 V	0 V to +0.9 V
ECL "1"	-0.9 V	-0.61 V to -0.97 V
ECL "0"	-1.8 V	-1.52 V to -2.38 V

* Measuring a TTL open collector voltage may result in a reading that is close to the actual power supply voltage.

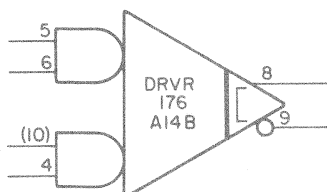
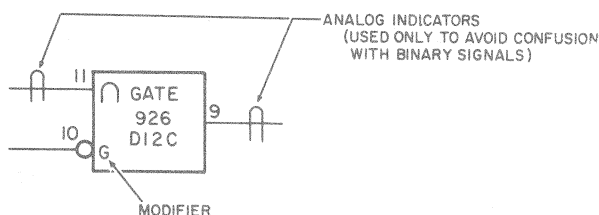
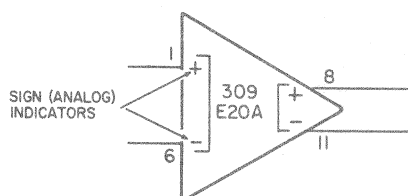
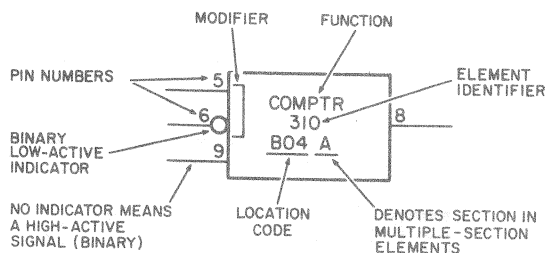
Only 500 mV between MDA 1's & 0's



REVISION LEVEL OF DIAGRAM SHEET.
THIS SHEET IS THE FIRST REVISION
WITH THAT SHOWN IN "REVISION STATUS
OF SHEETS" LISTING ON SHEET 1 OF THE
DIAGRAM SET FOR EACH CARD LOCATION.

*Loc A12
Loc B07
Loc B07-12A
Loc B07-12A*

INDICATORS



If enable then () indicates enables more parts of I.C.

MODIFIERS

G An enable signal. A viable output from the microcircuit depends upon the presence (active state) of the G modifier. Hence, G is often referred to as a dependency modifier.

], [A differential input, or a differential output, respectively. The microcircuit derives the differential by comparing the input signals appearing at the two pins spanned by the bracket, or by applying the generated differential signal to the two bracketed output pins.

| The heavy vertical bar is a mnemonic device to aid in distinguishing line drivers and receivers from other microcircuits using the same distinctive-shape (amplifier) symbol. The bar always appears within the symbol (as do all modifiers). It is near the input (left) side of the symbol for receivers and near the output side (right) for drivers.

INDICATORS

/ Non-standard logic level: The slash on an input or output line identifies a binary level that differs from that considered standard. (Refer to standard levels for TTL, ECL, CMOS as given in section 1.)

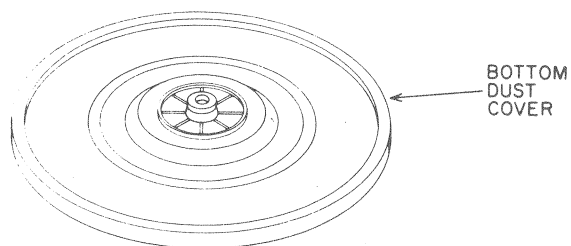
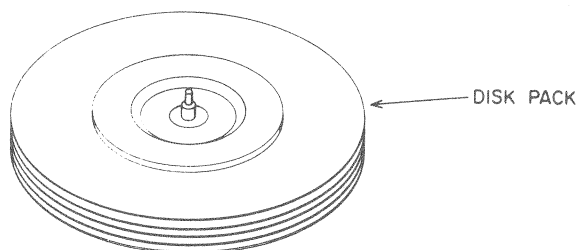
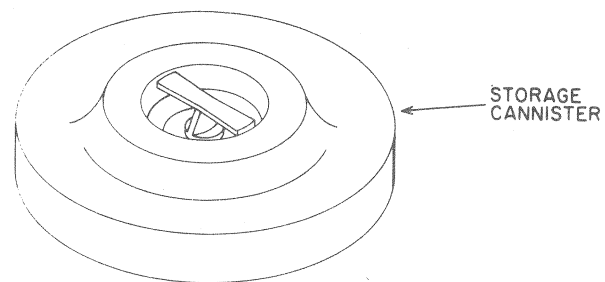
+ , - Analog sign indicators: The plus sign indicates the normal (non-inverting) analog input or output; the minus sign identifies the inverting input or output. Analog signals most frequently appear in pairs. When they do not, only the inverting signal (-) is identified; the lack of a + indicator, then, implies a non-inverting input or output.

⌋ Analog signal: The inverted "U" (input or output) on a signal line is used only if confusion between analog and digital signals might otherwise arise. It is not used, for example, in conjunction with the + and - modifiers that in themselves define a signal as analog.

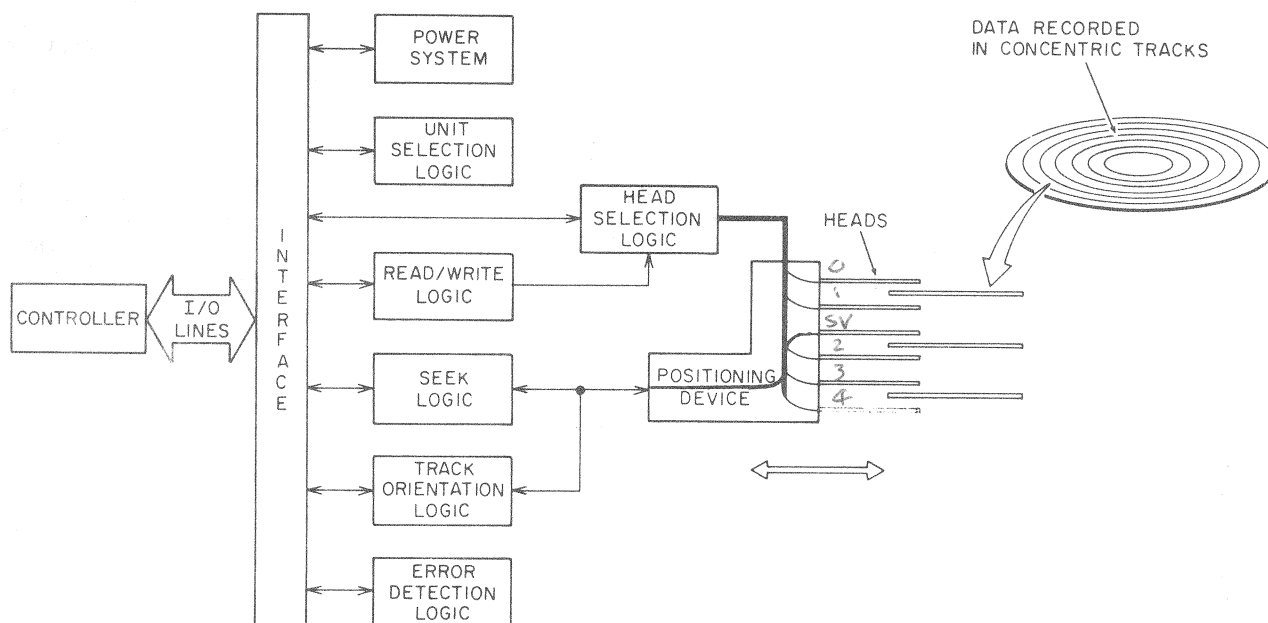
Binary (digital) logic: This symbol differentiates binary from analog signals (input or output). It is used only if confusion might otherwise arise.

◇ Open-collector output: If the open-collector output line is continued on another diagram sheet, the diamond may be repeated just to the left of the off-sheet indication. This serves as a reminder that the pull-up resistor is shown elsewhere.

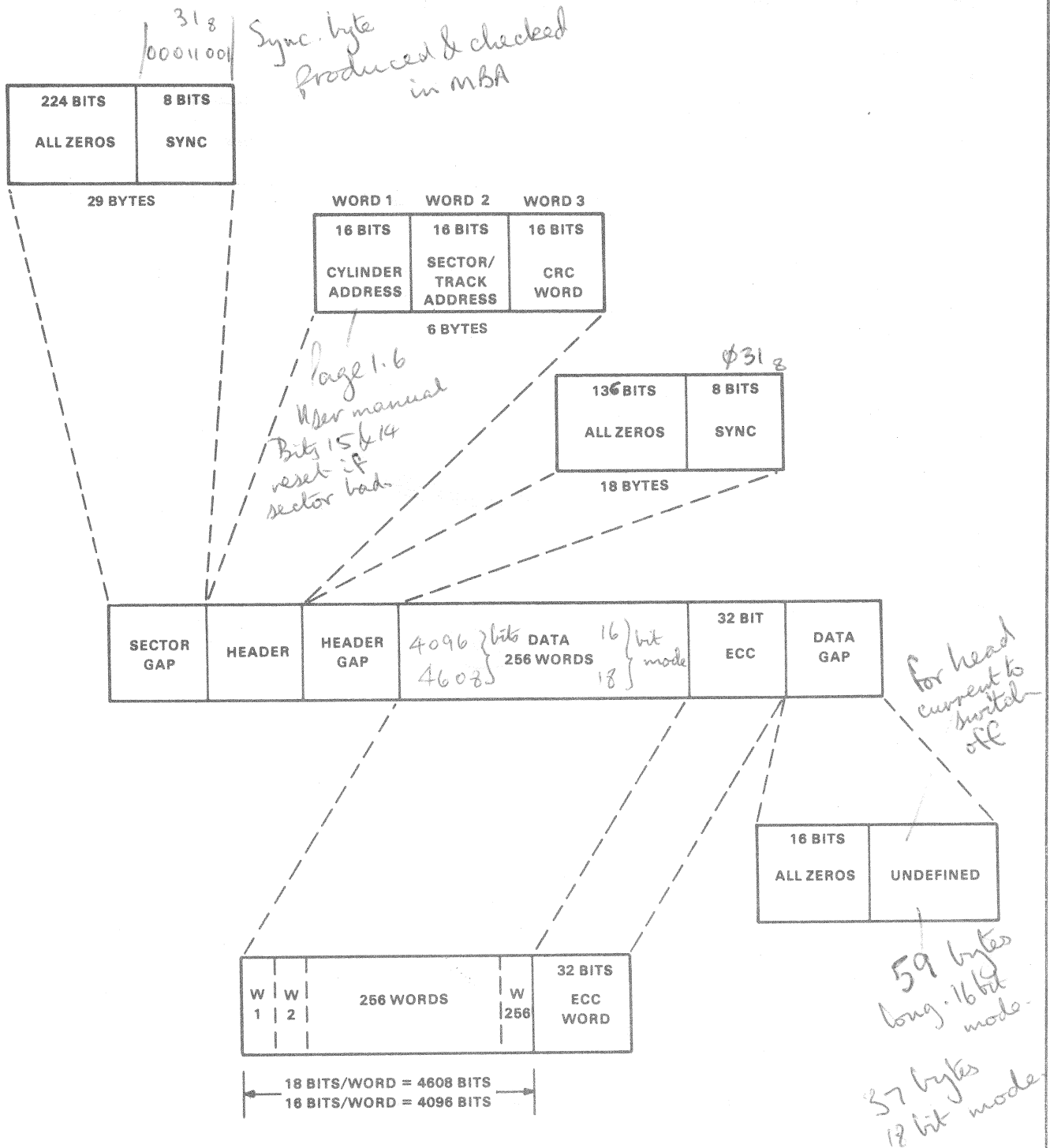
DISC PACK DRIVE FUNCTIONAL BLOCK DIAGRAM



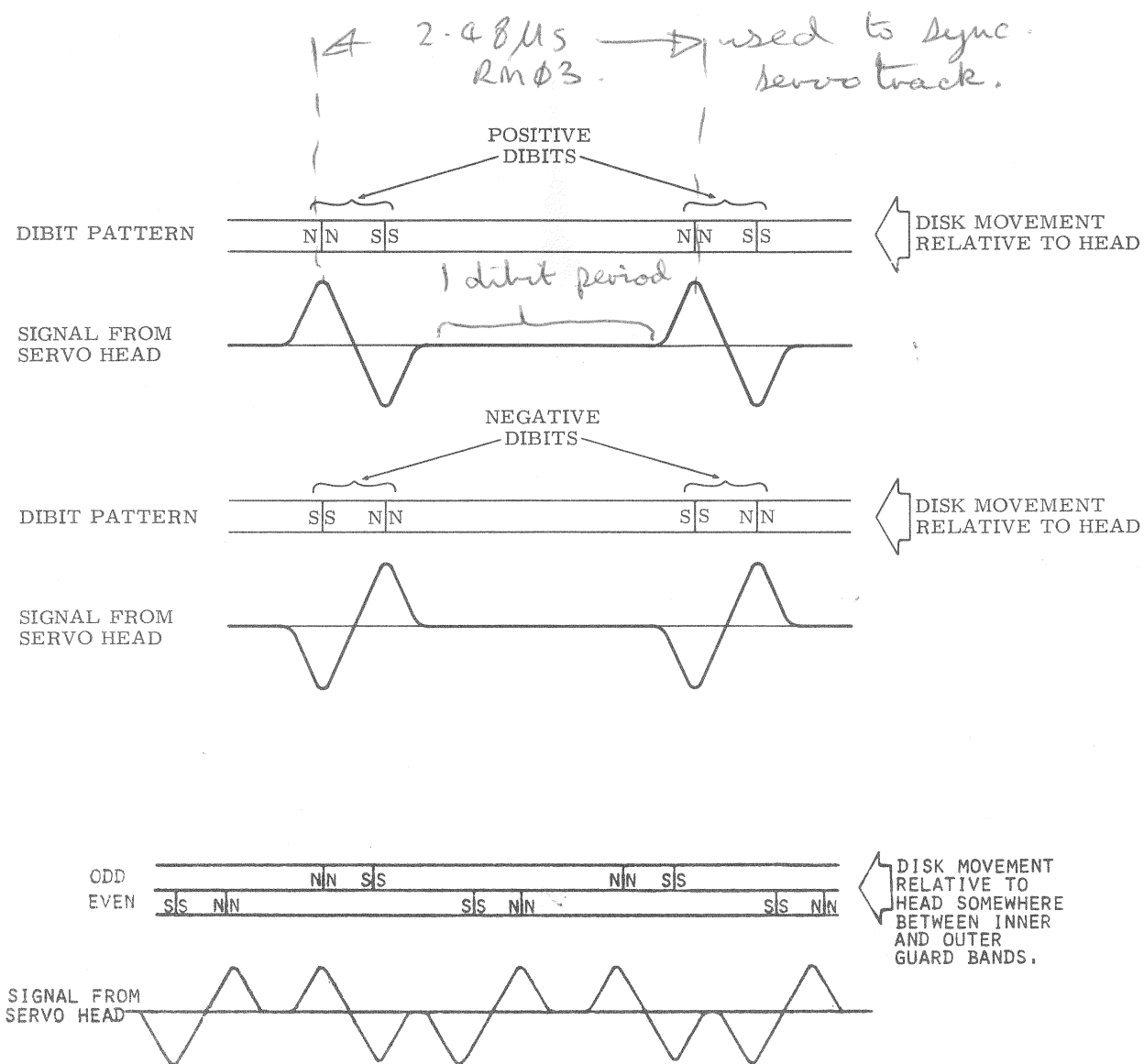
Disk Pack

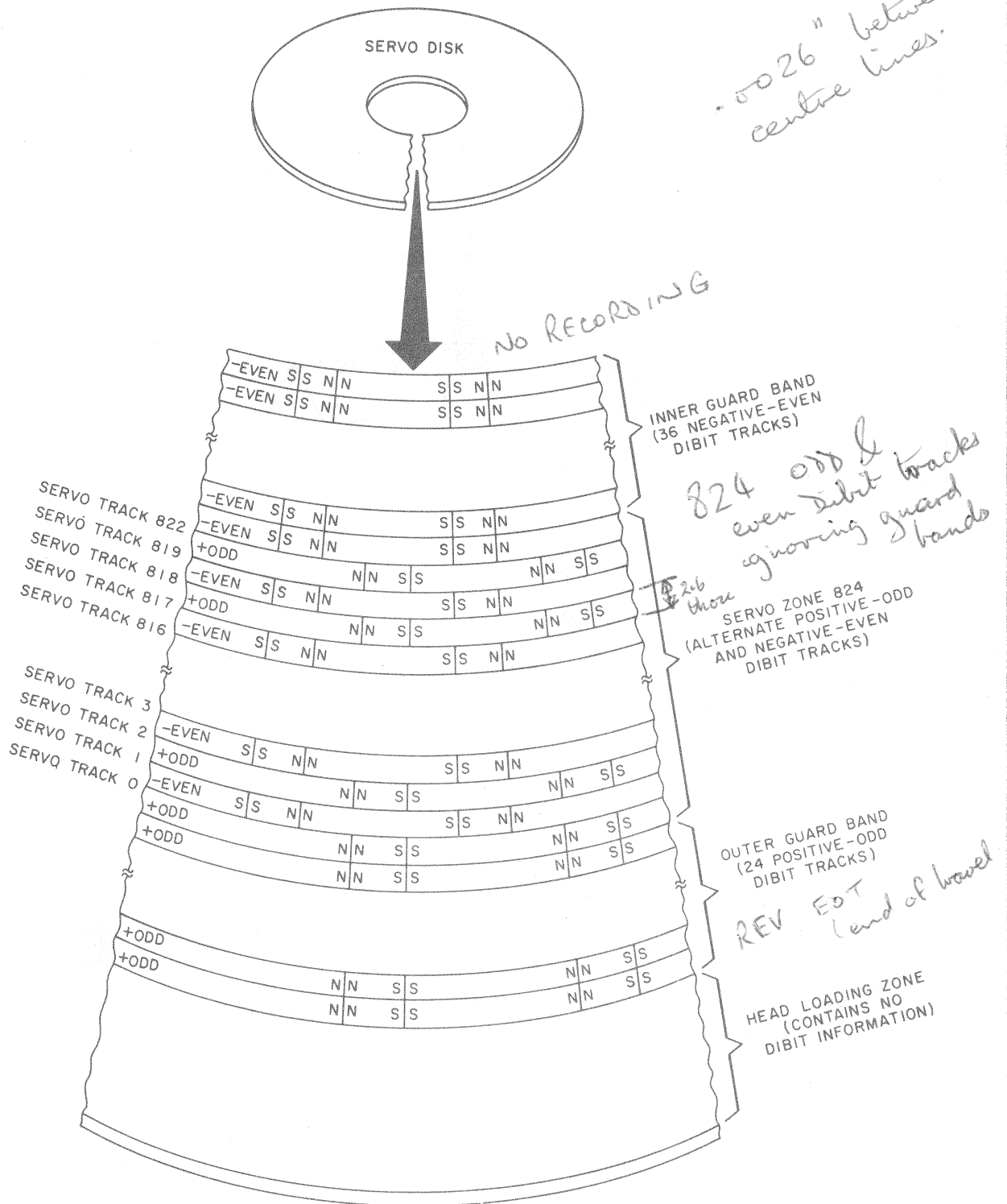


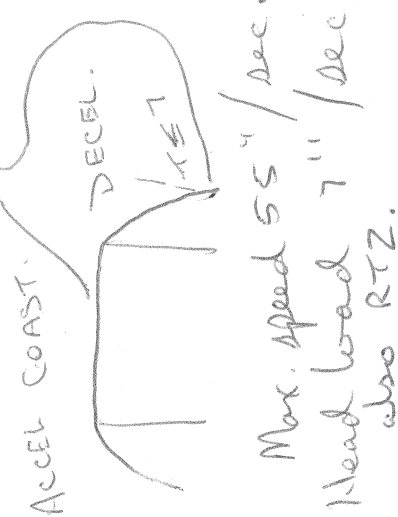
SECTOR FORMAT

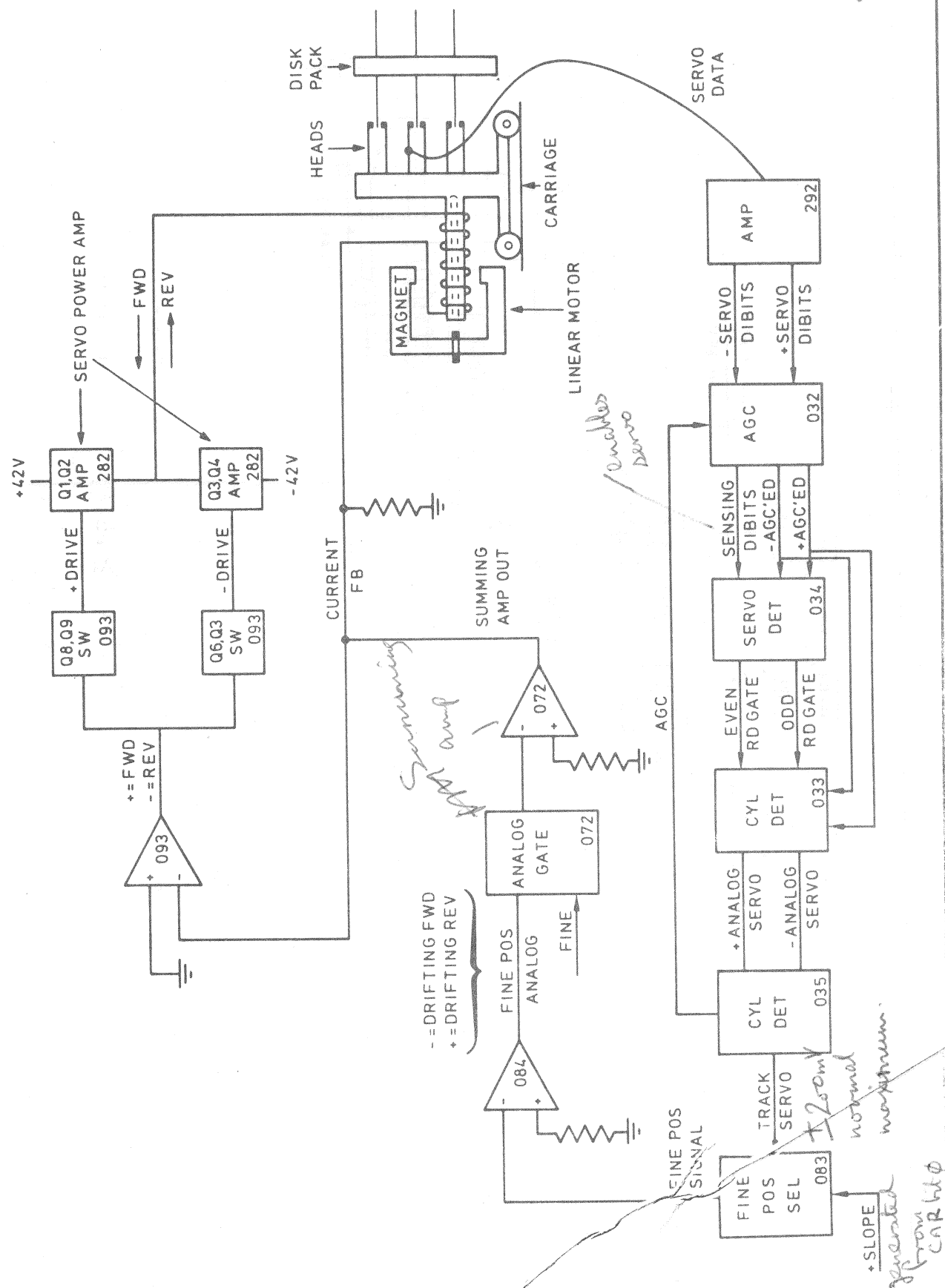


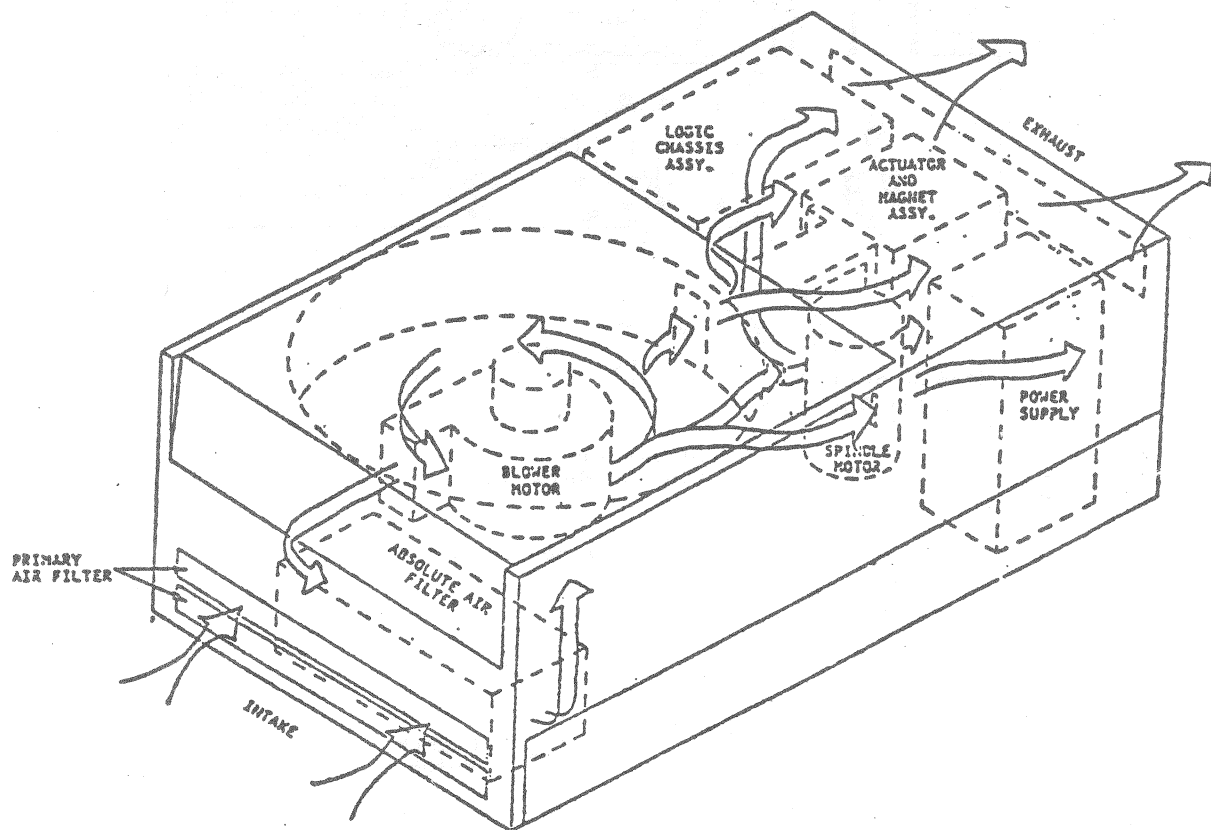
When Writing. we rewrite
pre-header Sync byte
& Header gap.



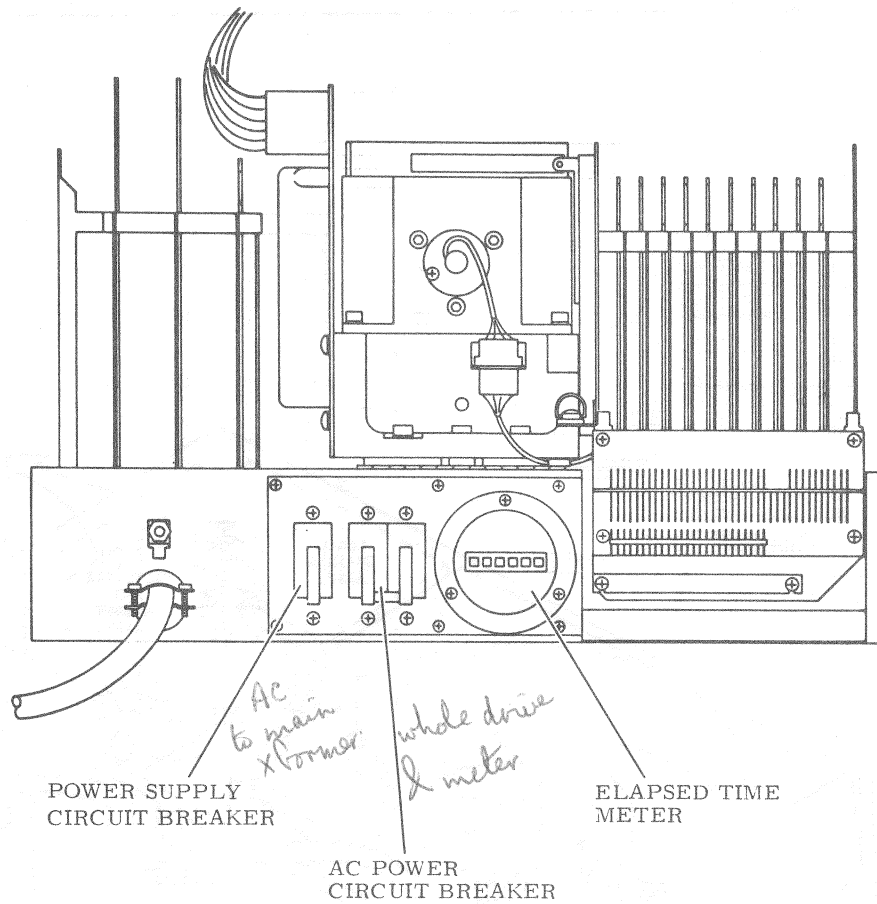




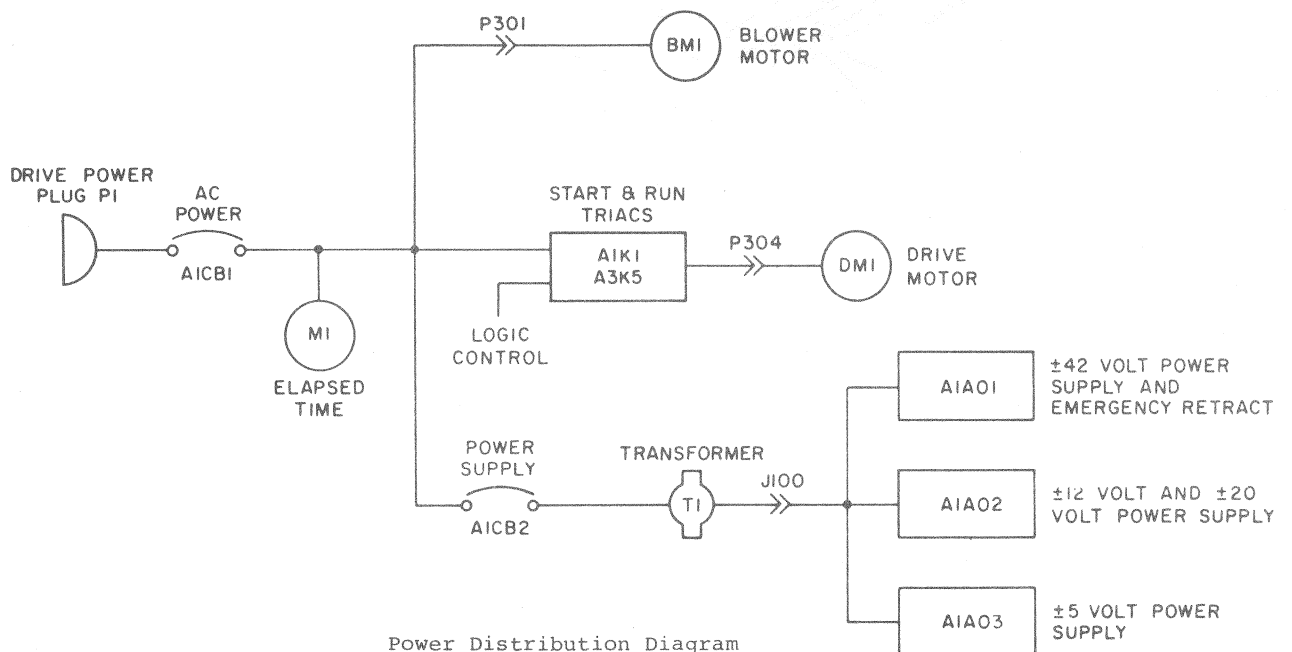




POWER CONTROL PANEL AND DISTRIBUTION DIAGRAM

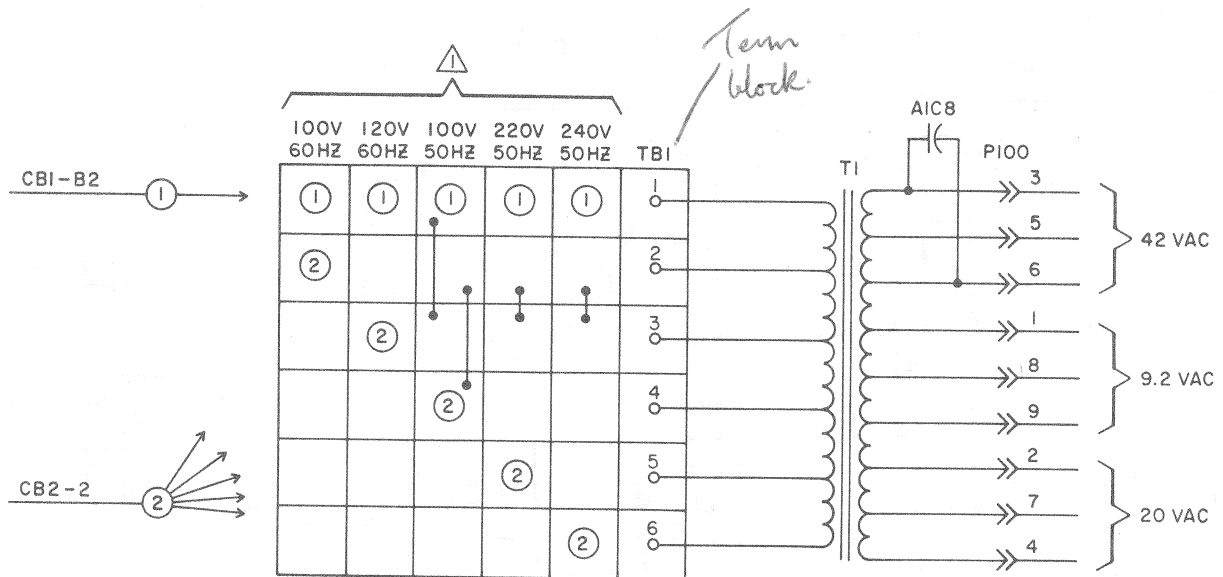


Power Control Panel Switches and Indicators



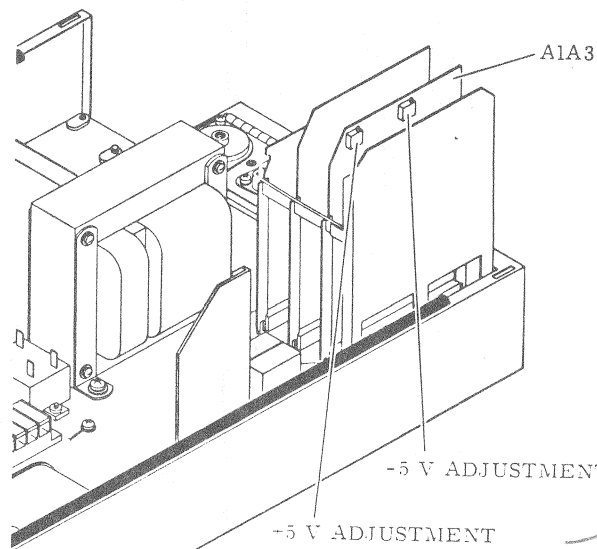
Power Distribution Diagram

AC POWER WIRING POWER SUPPLY ADJUSTMENT LOCATIONS



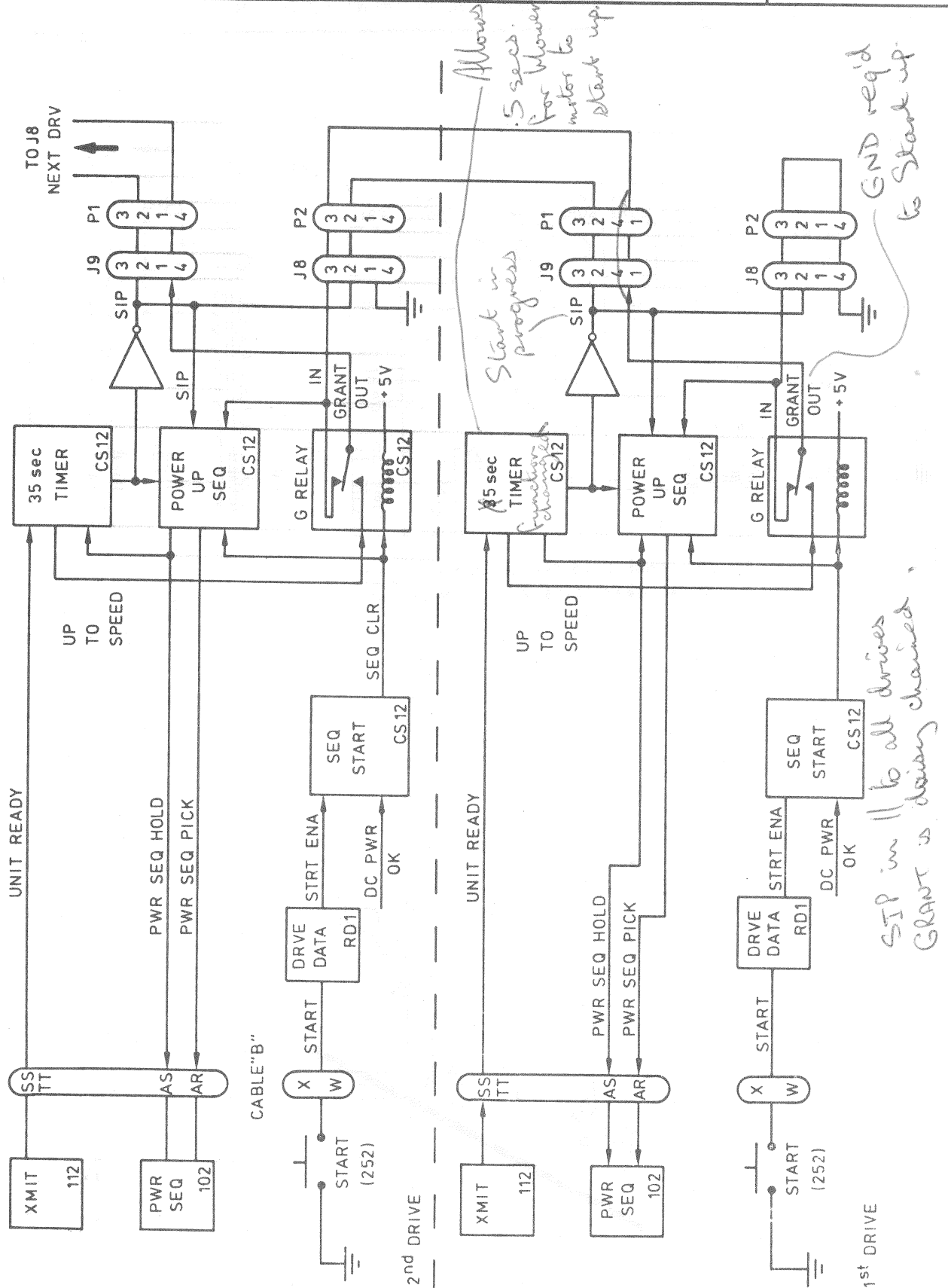
NOTES: CONNECTIONS DEPEND ON SITE POWER.
2 INDICATES 16 AWG JUMPER WIRE.

eg. jumper 2-3 for 240V 50Hz
CBI-B2 always to 1
CB2-2 to TBI-6



Must be measured on B/P with DVM.
±5.1 V with 32 cyl. seek.
±5.15 V without seeks.
Check voltages before head alignment.

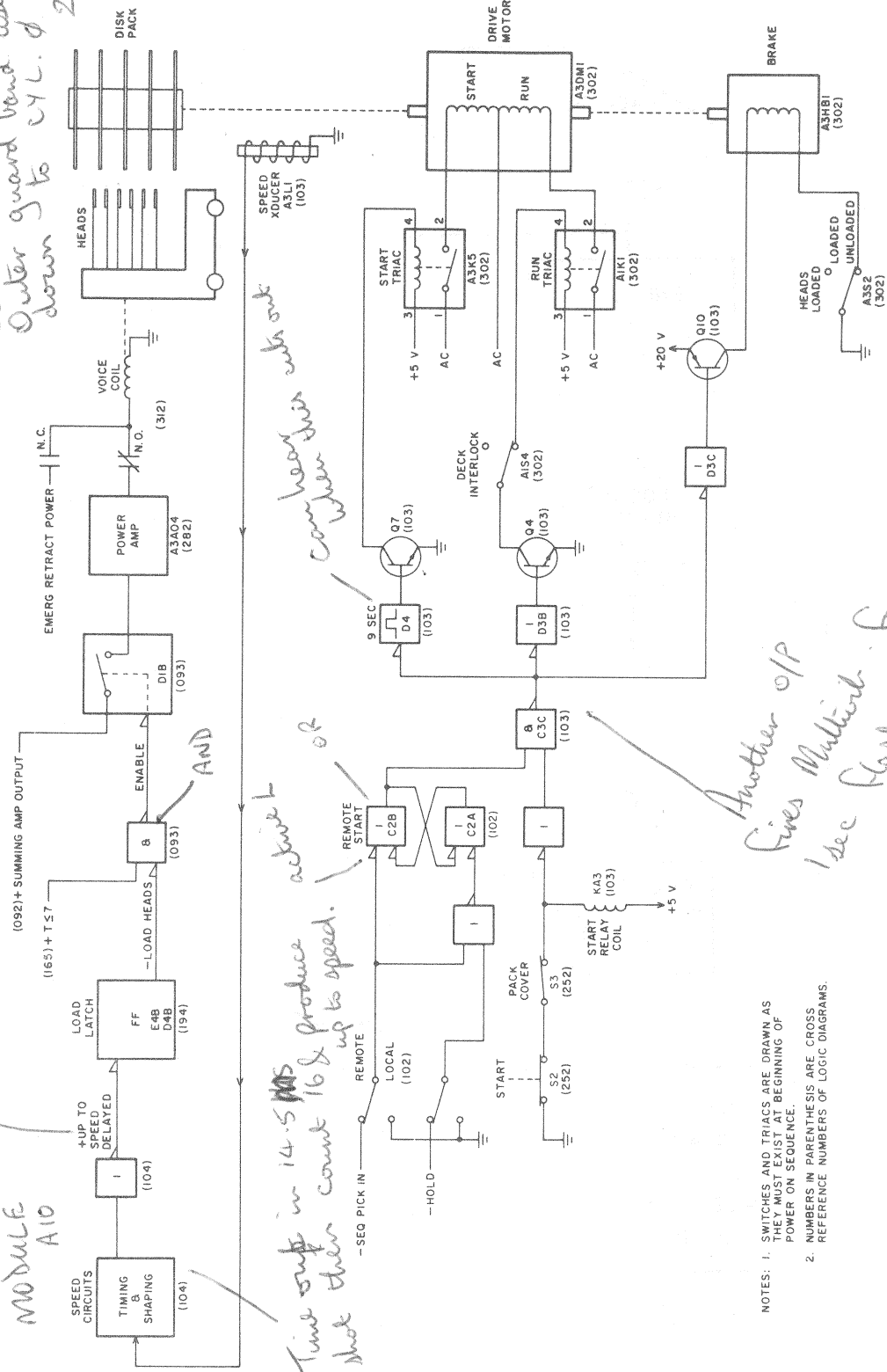
Power Sequence Blockdiagramm



On load heads start 350ms
time out which gives fault
condition if no digits sent.
Outer guard band used to slow
down to 24 tracks of
odd digits
before last
EVEN digits

slow
up to speed.

MODULE
A10

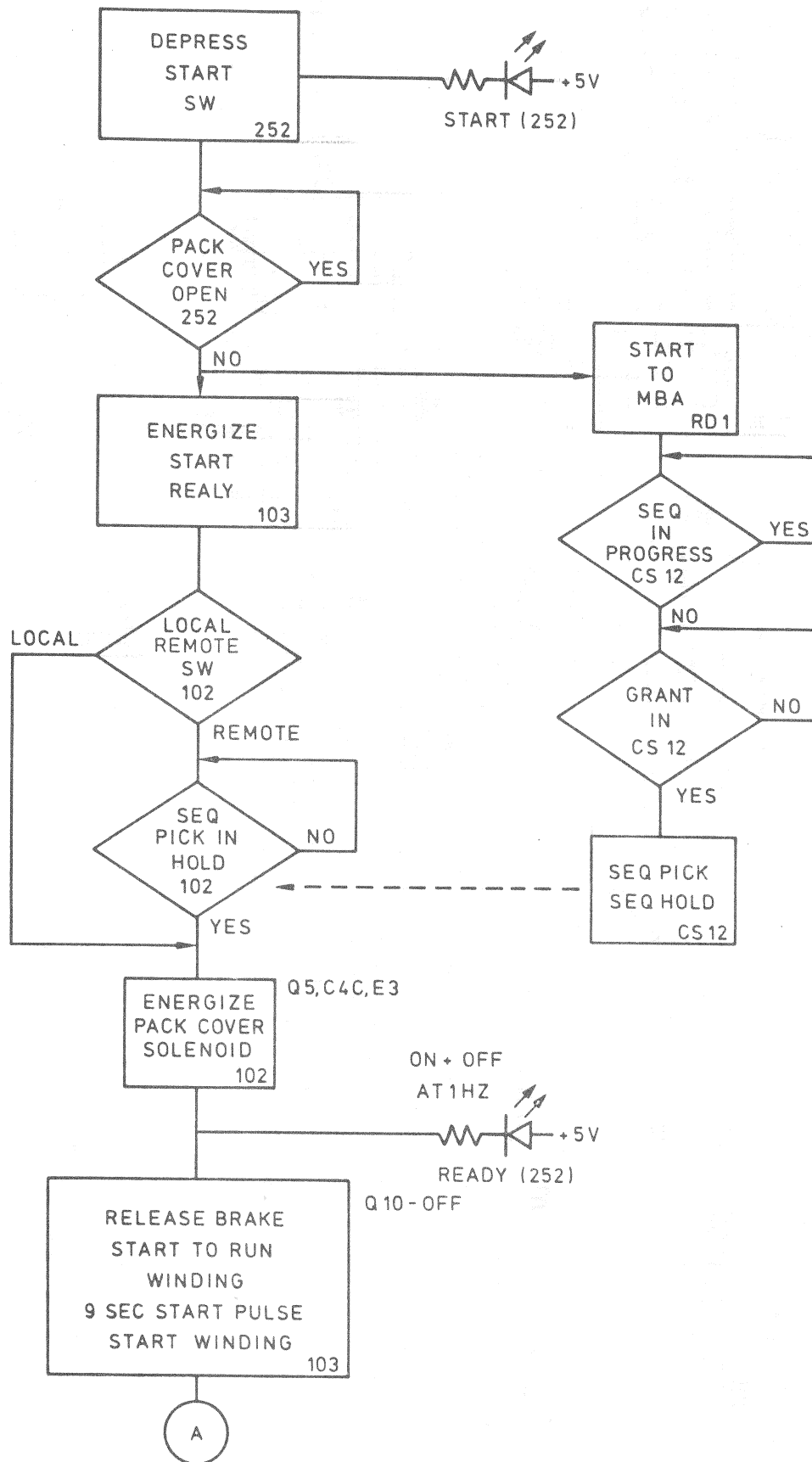


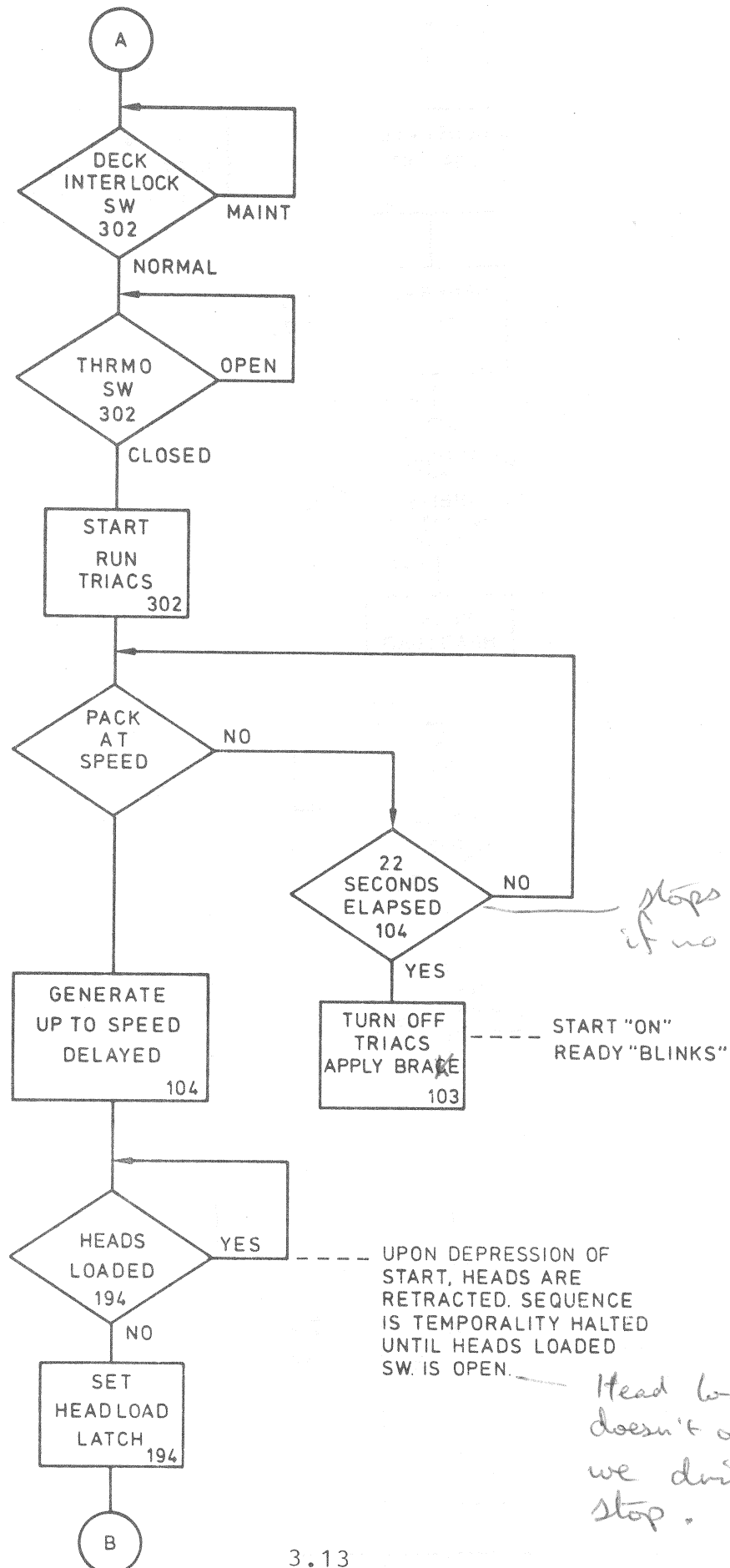
converging into one

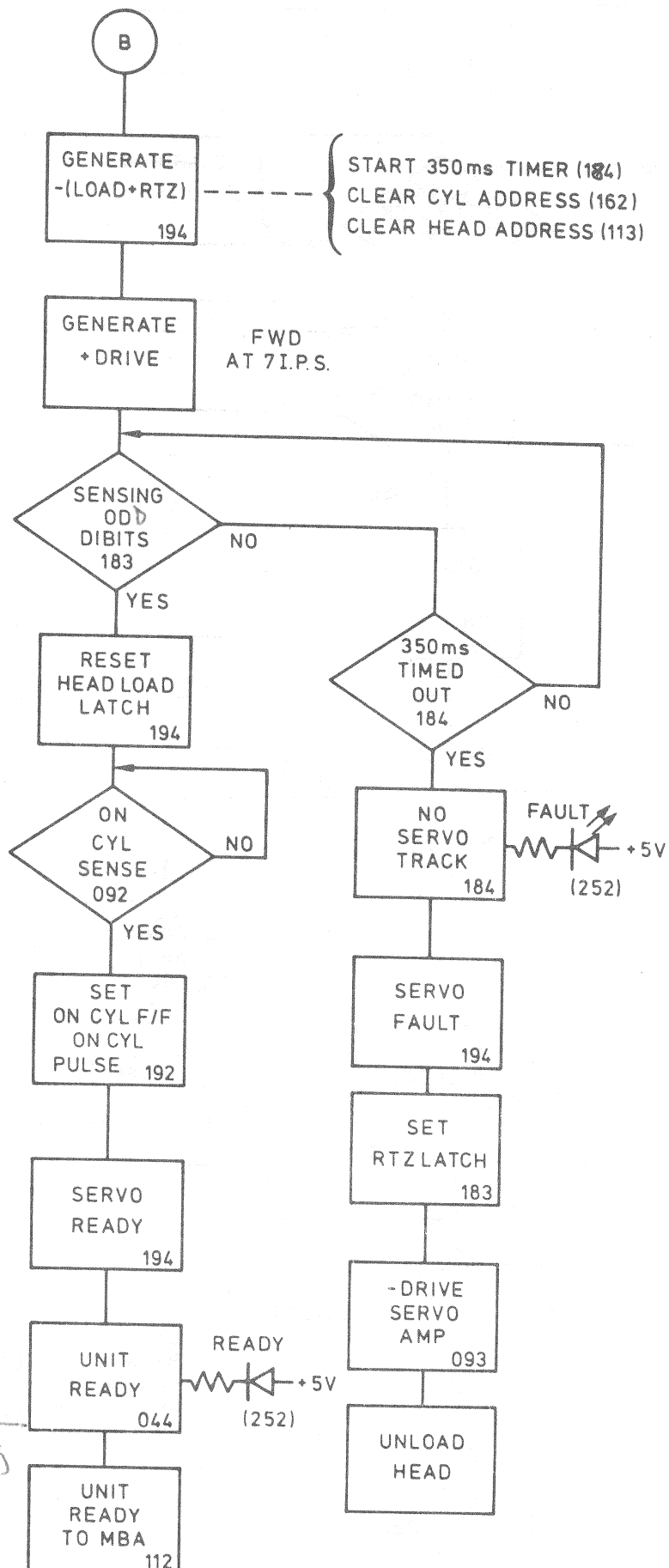
No Time out in 14.5 ms
then count 16 & produce
up to speed.

Another O/P
Gives Multibit for
1 sec flash on ready light

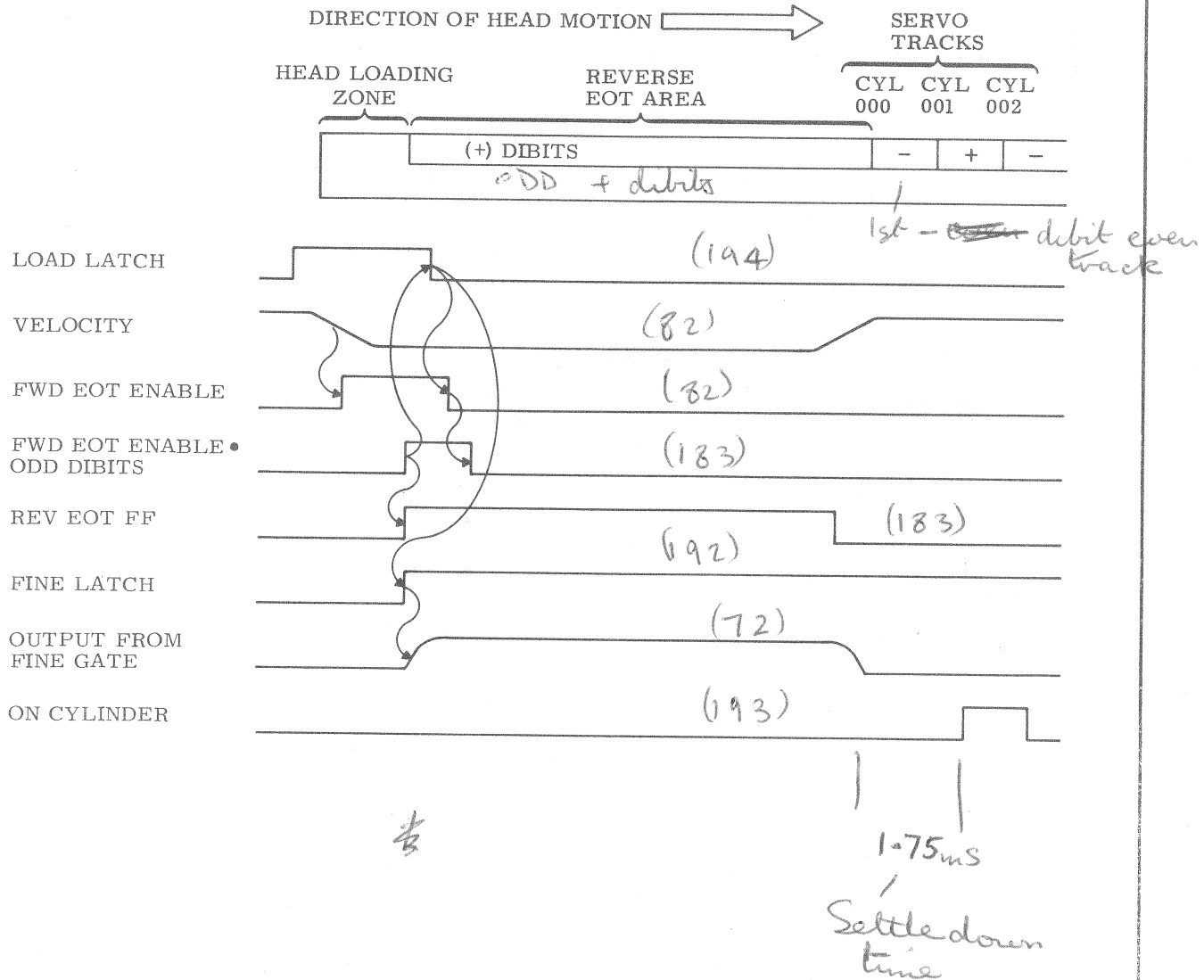
- NOTES:
1. SWITCHES AND TRIACS ARE DRAWN AS THEY MUST EXIST AT BEGINNING OF POWER ON SEQUENCE.
 2. NUMBERS IN PARENTHESES ARE CROSS REFERENCE NUMBERS OF LOGIC DIAGRAMS.



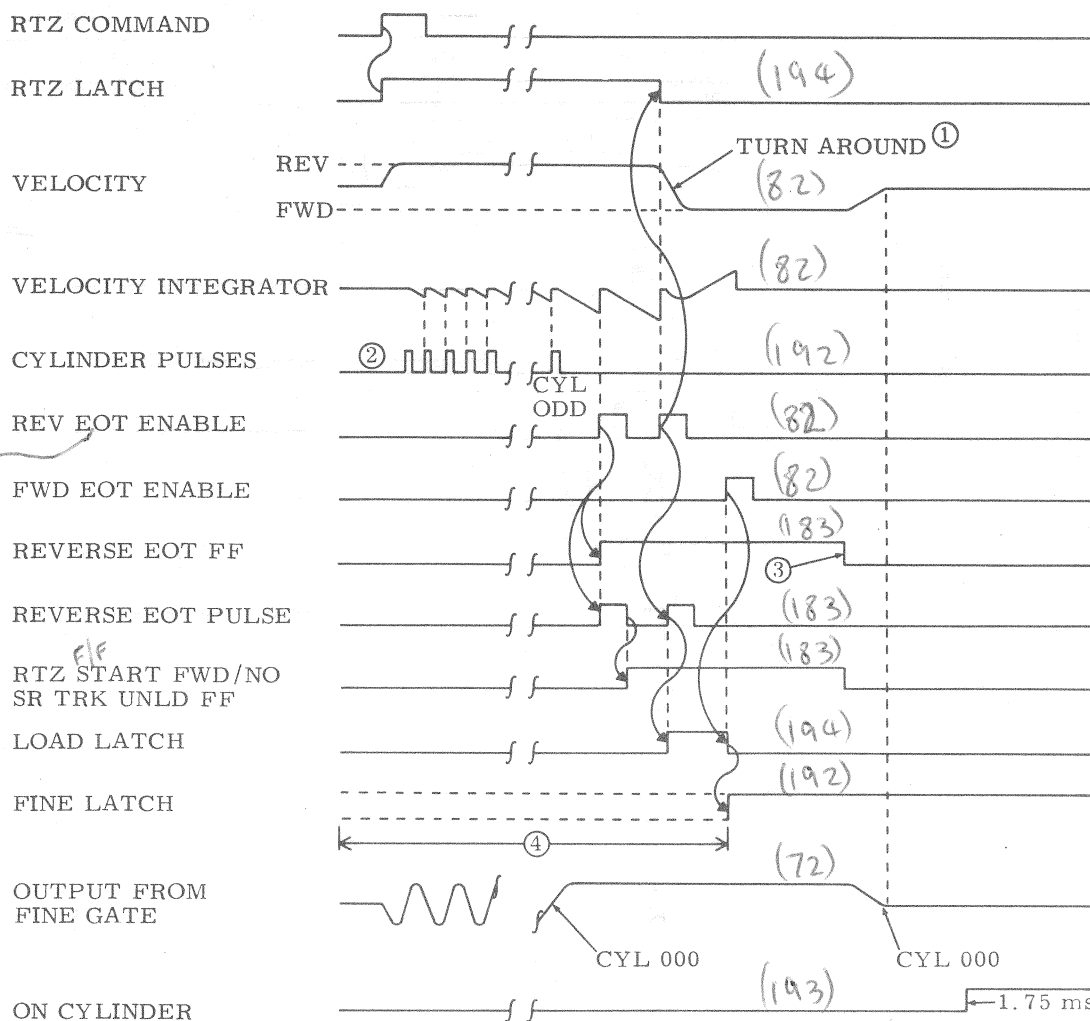




HEAD LOAD SEEK TIMING



RETURN TO ZERO SEEK TIMING

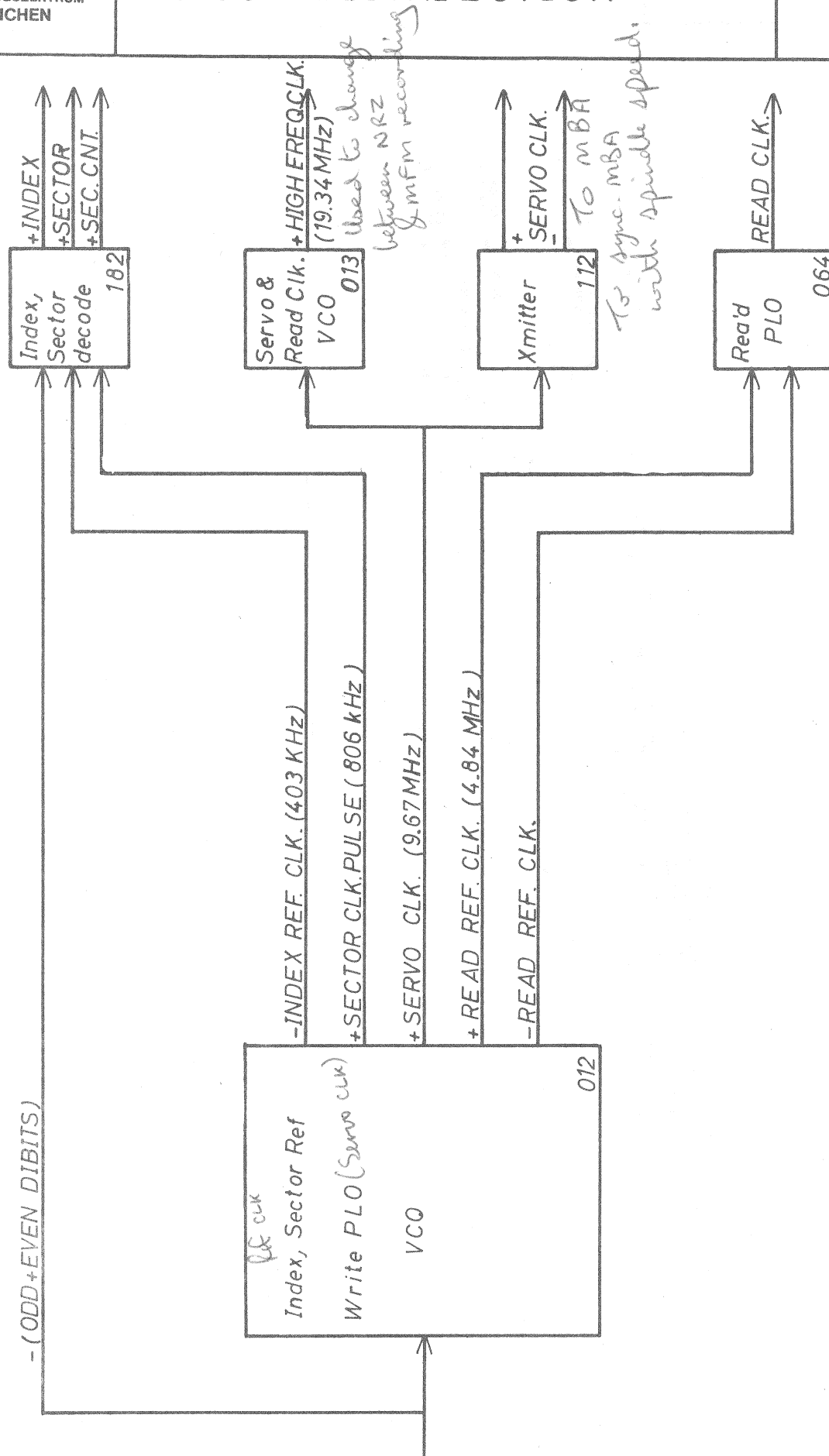


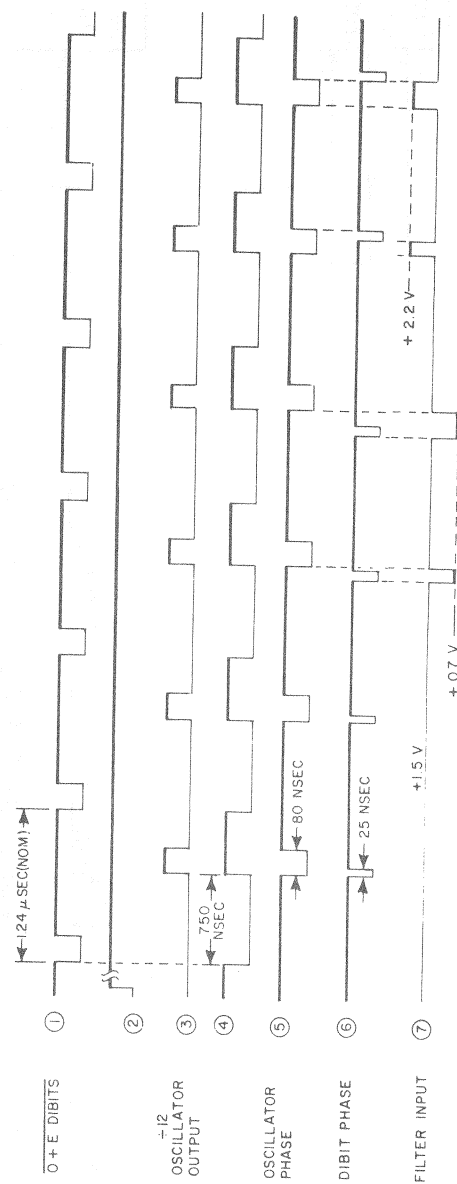
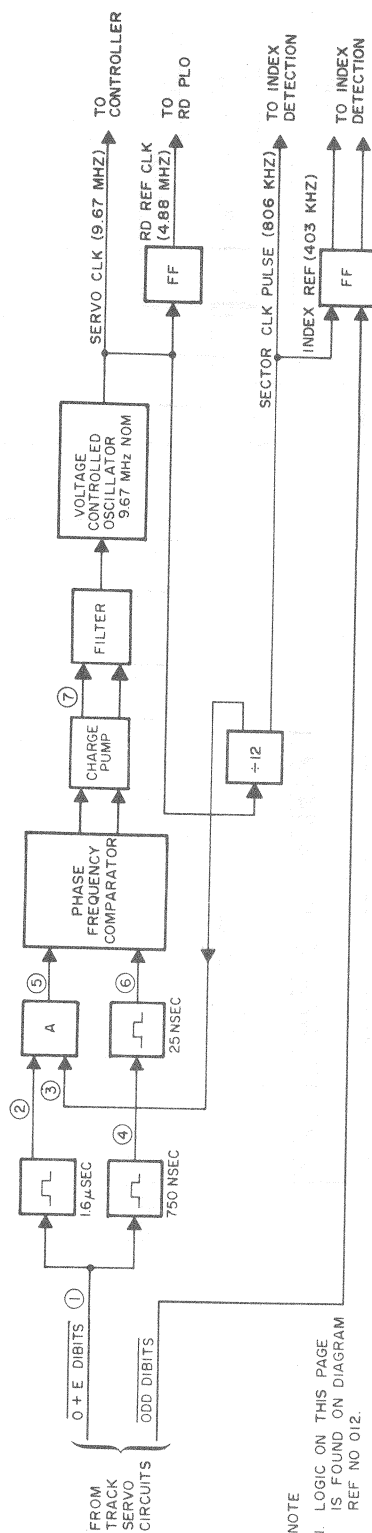
NOTES:

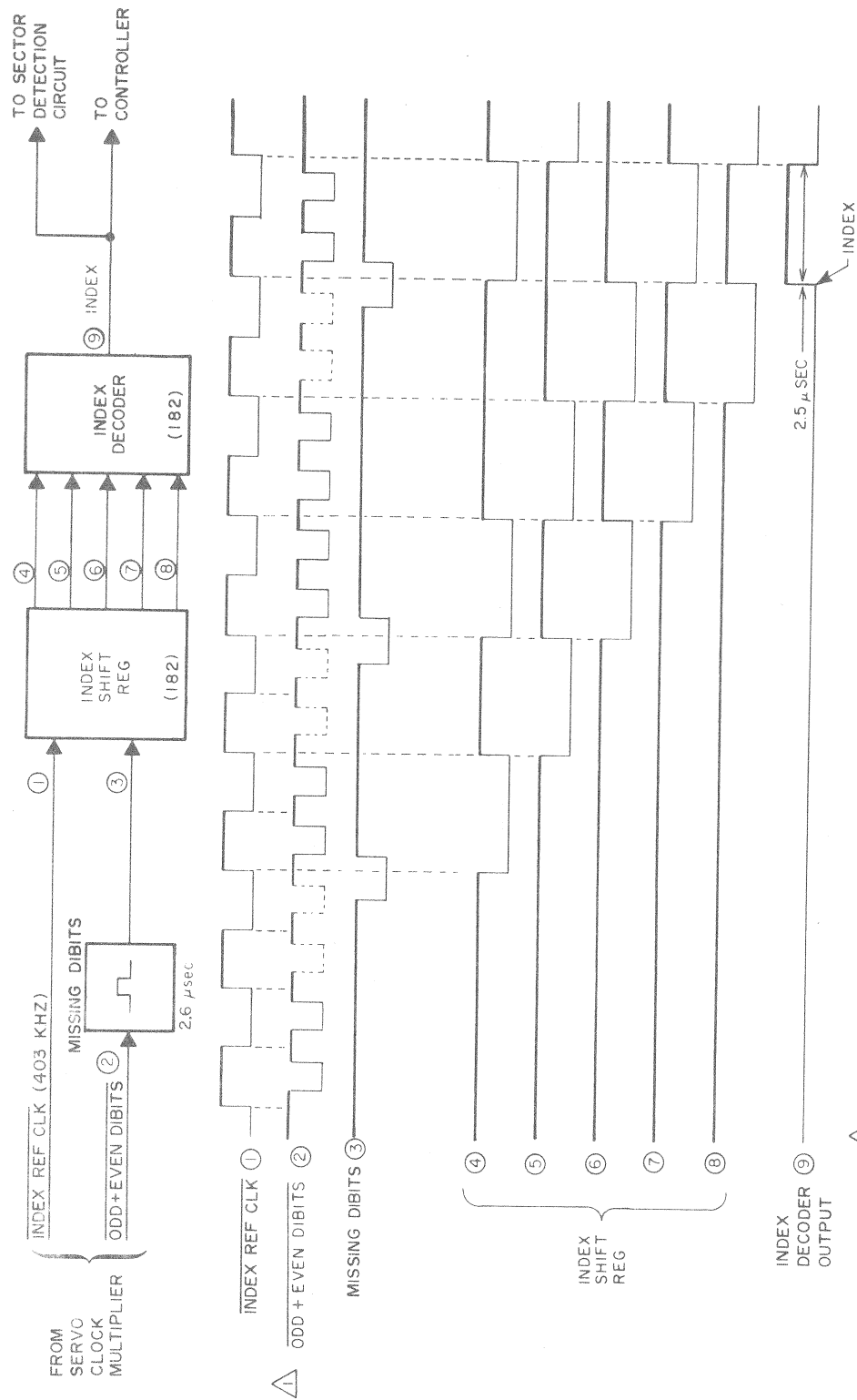
- ① CLEARING RTZ AND SETTING LOAD LATCH CAUSES CARRIAGE TO REVERSE DIRECTION AND MOVE FWD.
- ② CYLINDER PULSES RESET VELOCITY INTEGRATOR.
- ③ REV EOT FF CLEARED WHEN NEGATIVE-EVEN DIBITS ARE DETECTED AS HEADS APPROACH 000.
- ④ FINE LATCH IS JAMMED (BOTH INPUTS HIGH) THUS DISABLING BOTH COARSE AND FINE GATES AS LONG AS EITHER LOAD OR RTZ LATCH IS SET.

Settle down time as on CYL allows WR & WR CHK.

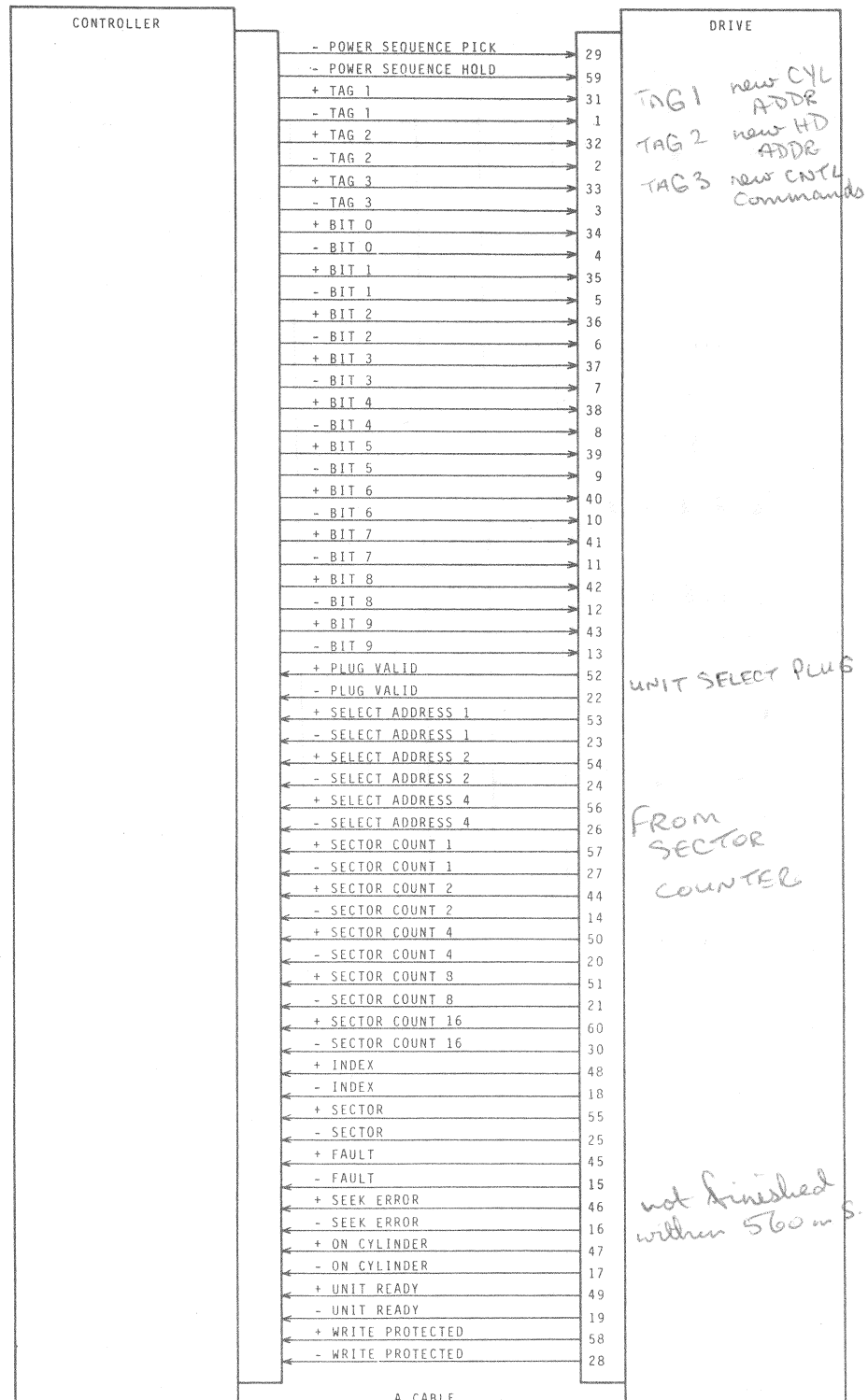
CLOCK DISTRIBUTION





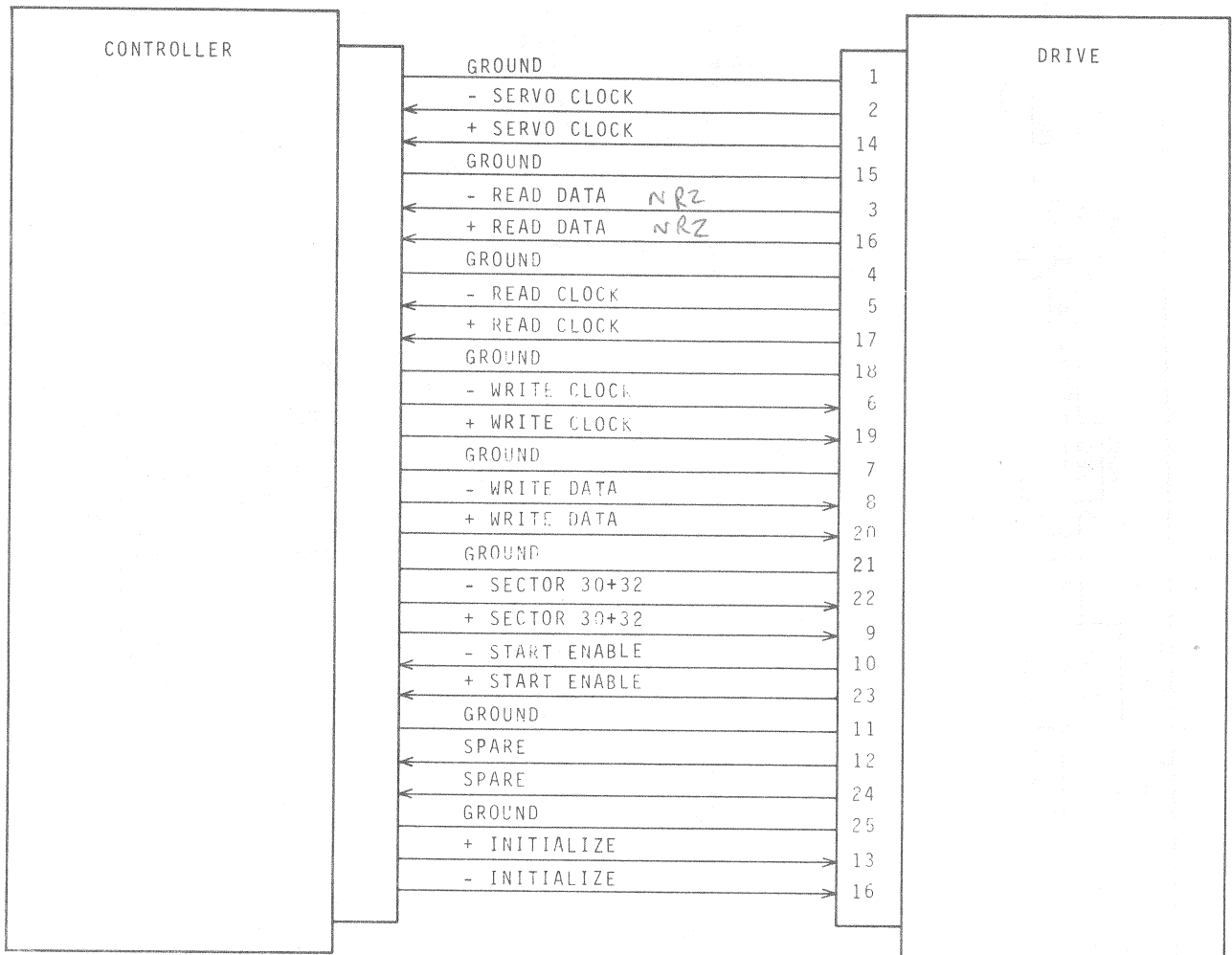


NOTES; Δ MISSING DIBITS SHOWN BY DASHED LINES.
NOMINAL FREQUENCY OF ODD+EVEN DIBITS
SIGNAL IS 806 KHZ.



A CABLE

60 wire
LF signals.

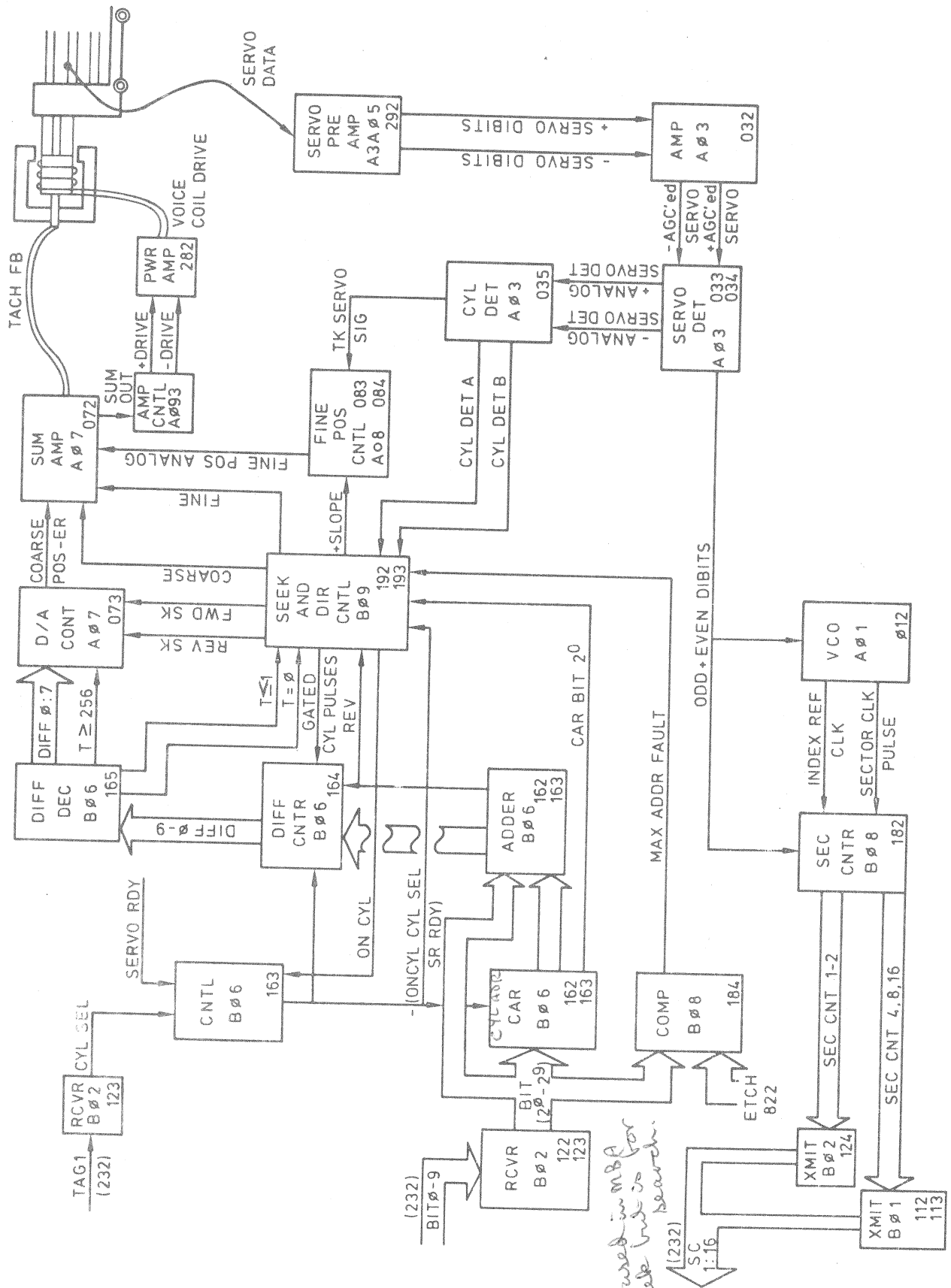


B CABLE

26 wires HF signals



Servo System Blockdiagramm



bit seq.



Indicates peak shifts → on pack. Hence to precompensate when writing, 6uS precomp. used.

DATA TO BE WRITTEN	1	0	1	1	1	1	0	0	0	0	0	0	1	0
RECORDING METHOD	RZ	NRZ	NRZI	F.M. (MODIFIED NRZI; FREQUENCY MODULATION)	P.E. (PHASE ENCODING; MANCHESTER METHOD)	M.F.M. (MODIFIED FREQUENCY MODULATION; MILLER ENCODING)								

ONE OF ORIGINAL RECORDING TECHNIQUES, NOW OBSOLETE

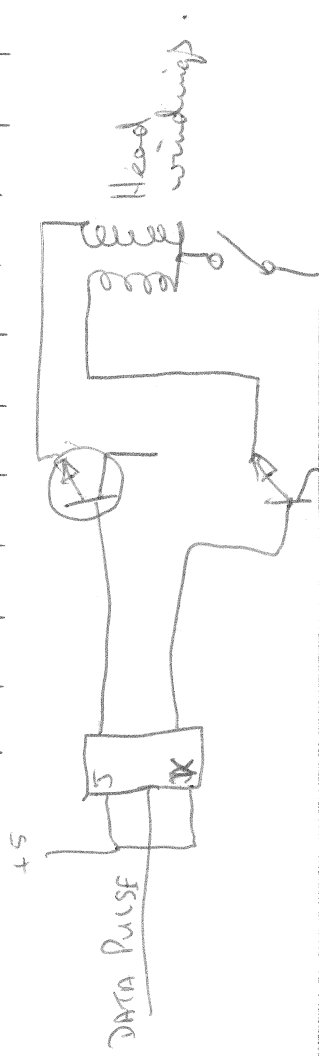
1ST MODIFICATION; USED ON MAGNETIC DEVICES BUILT IN 1950'S

USED ON MOST TAPE DRIVES (UP TO 800 BPI) INCLUDING DEC'S TU10, PLUS DF-32, RS04, AND RS08 DECDISKS

USED ON MOST MOVING HEAD DISK DRIVES DURING 1960'S (INCLUDING RK05 AND RP03)

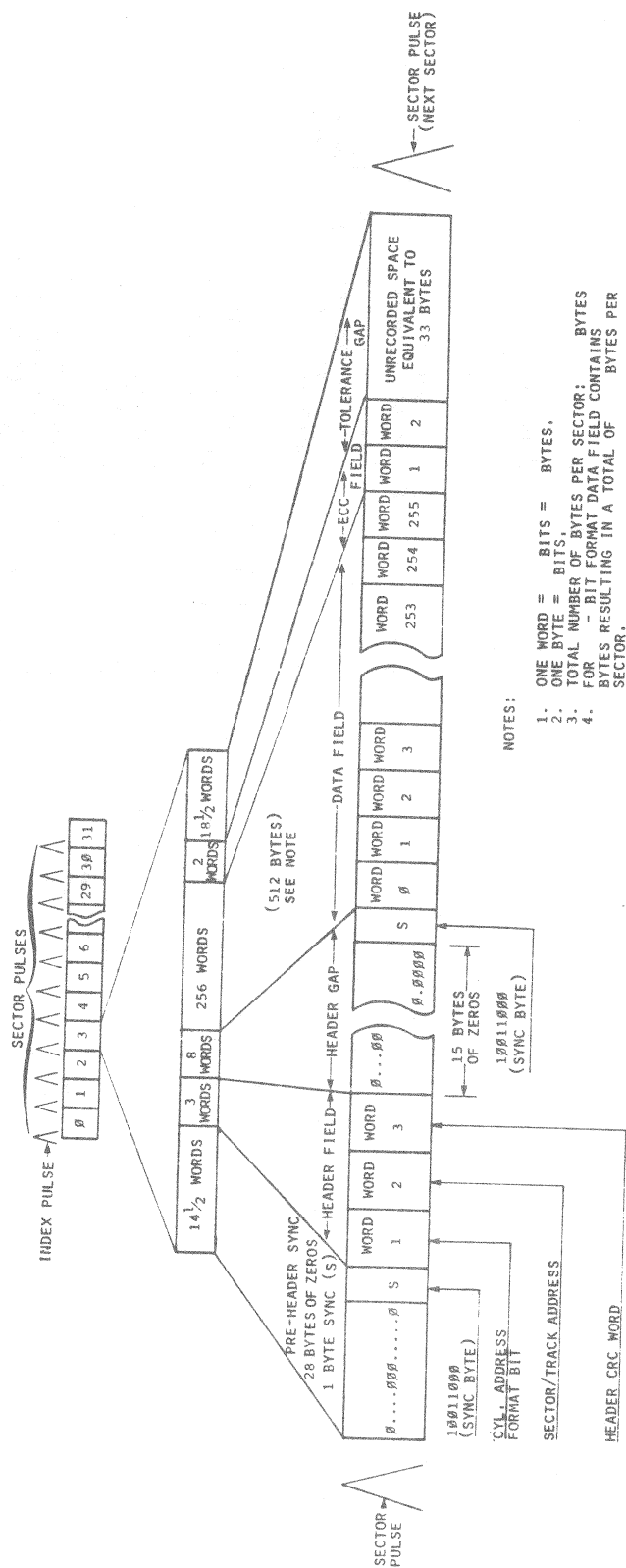
USED WITH NEWER TAPE DRIVES (1600 BPI) AND SOME HI-DENSITY DISK PACKS (PLUS DECTAPE)

NEWER METHOD ALLOWS EXTREMELY HI-DENSITY COUPLED WITH VERY RELIABLE READ-BACK, USED ON VERY HIGH-DENSITY TAPES AND DISKS SUCH AS THE FIXED-HEAD RS04, THE MOVING-HEAD RP04/5/6 LINE, THE RK06 AND THE NEW RL AND RM PRODUCT LINES.



Comparison of Various Recording Methods and Equipment

Sector Format (16 Bit Mode) Diagram



PROM OUTPUTS

This tells us where we are, (What signals are active at sector word count)

WRITE HEADER AND DATA

WORD COUNT

FUNCTION

000→131

P EN CRC / ECC

001

PRE CLEAR CRC / ECC

001→419

P WRITE GATE

014

P EN SYNC, P EN LOAD SR To
P DATA EN SCLK, BRANCH (128)

128

P EN LOAD SR, P DATA EN SCLK

129

P HEADER AREA

130

P EN LOAD SR, P HEADER AREA

139

P EN CRC OUT, BR RD TO WRT

161→415

P EN SYNC, P EN LOAD SR To
P DATA EN SCLK, BRANCH (161)

416

P DATA EN SCLK, P EN LOAD SR

417→418

P EN LOAD SR

419

P EN ECC OUT

P EN EBL End of block. (Stop writing must occur before next index pulse.)

WRITE DATA

WORD COUNT

FUNCTION

000→131

P EN CRC / ECC

001

PRE CLEAR CRC / ECC

004→129

P READ GATE To

011

P LFS, BRANCH (128)

128

P HEADER AREA (FMT + CYL COMPARE)

129

P HEADER AREA (TRACK + SECTOR COMPARE)

130

P EN CRC OUT, BR RD TO WRT

131→419

P WRITE GATE

139

P EN SYNC, P EN LOAD SR To
P DATA EN SCLK, BRANCH (161)

161→415

P DATA EN SCLK, P EN LOAD SR

416

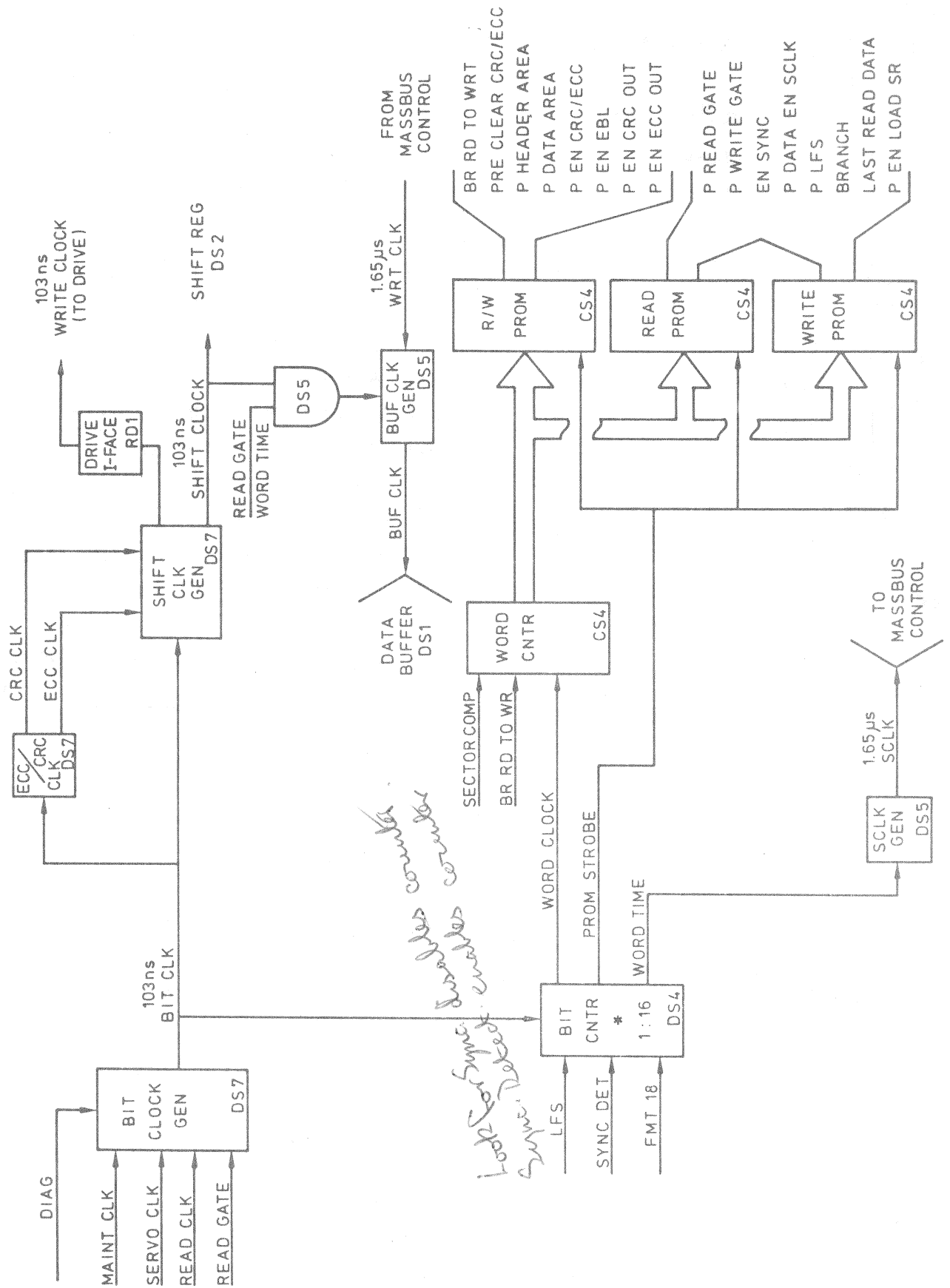
P EN LOAD SR

417→418

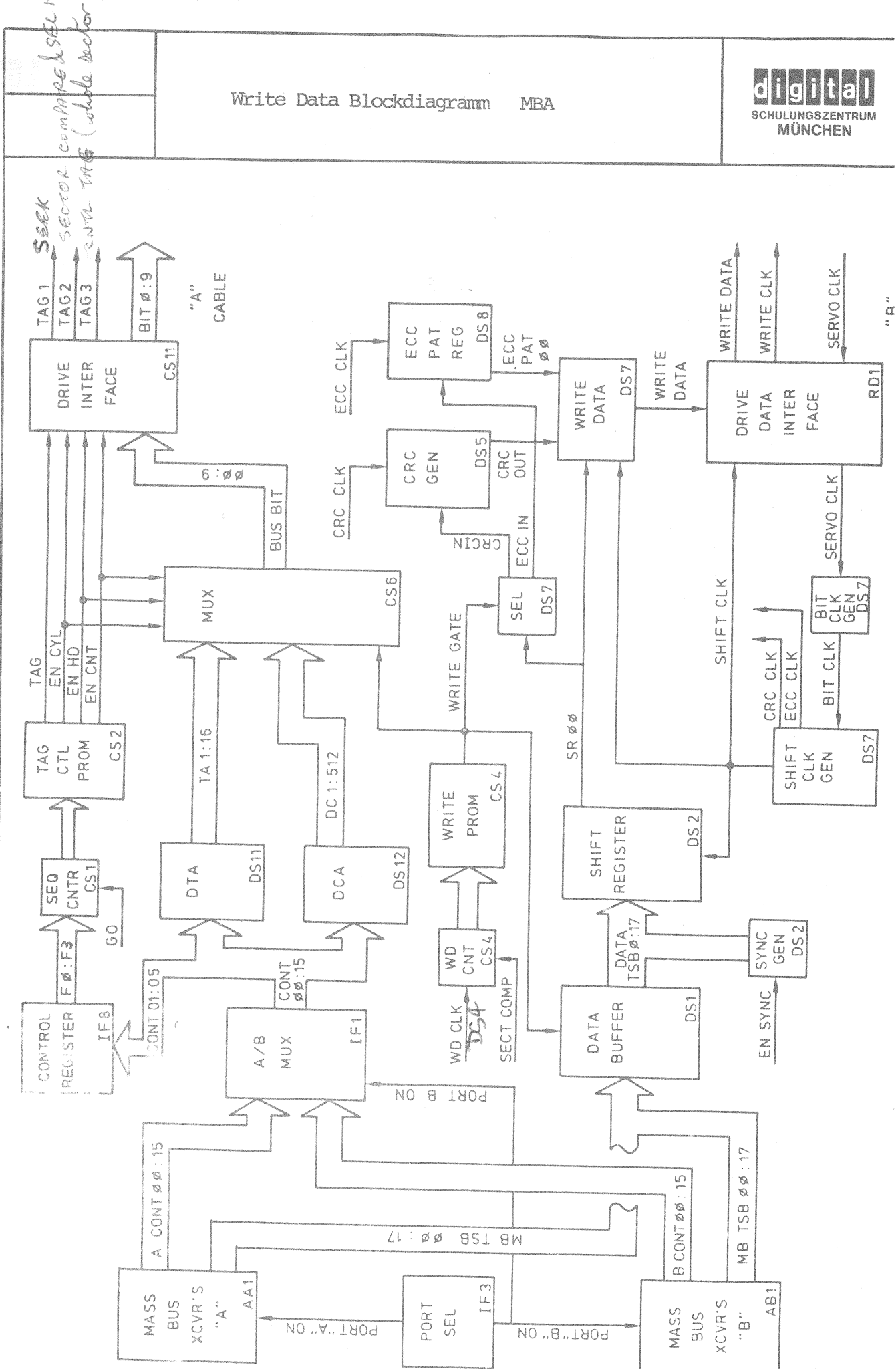
P EN ECC OUT

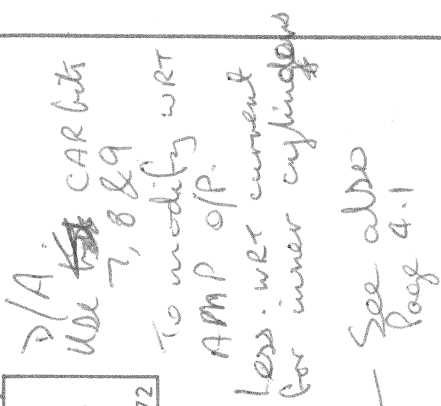
419

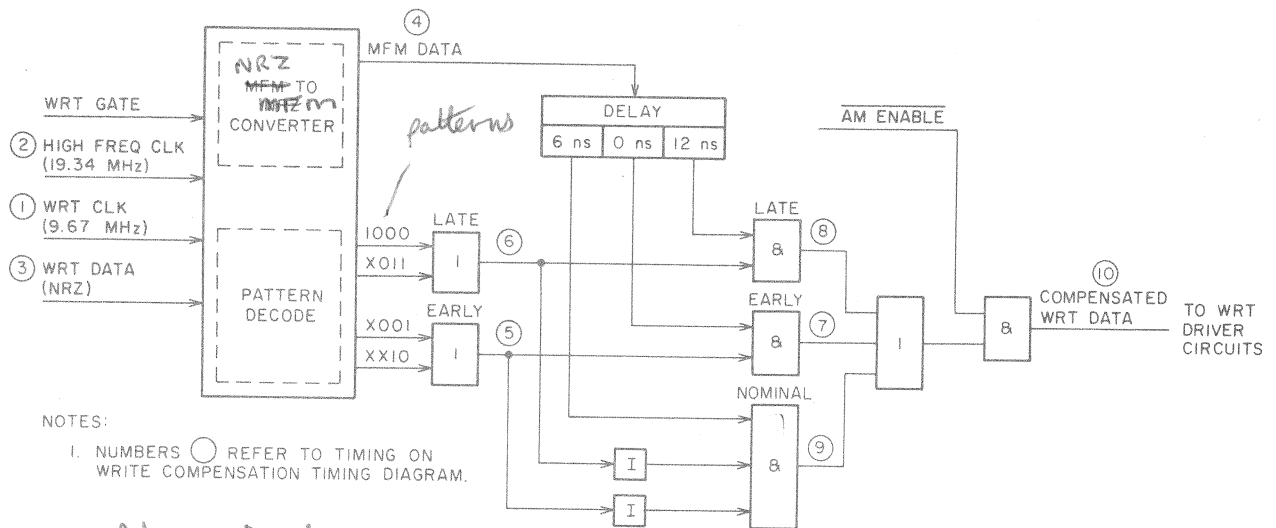
P EN EBL



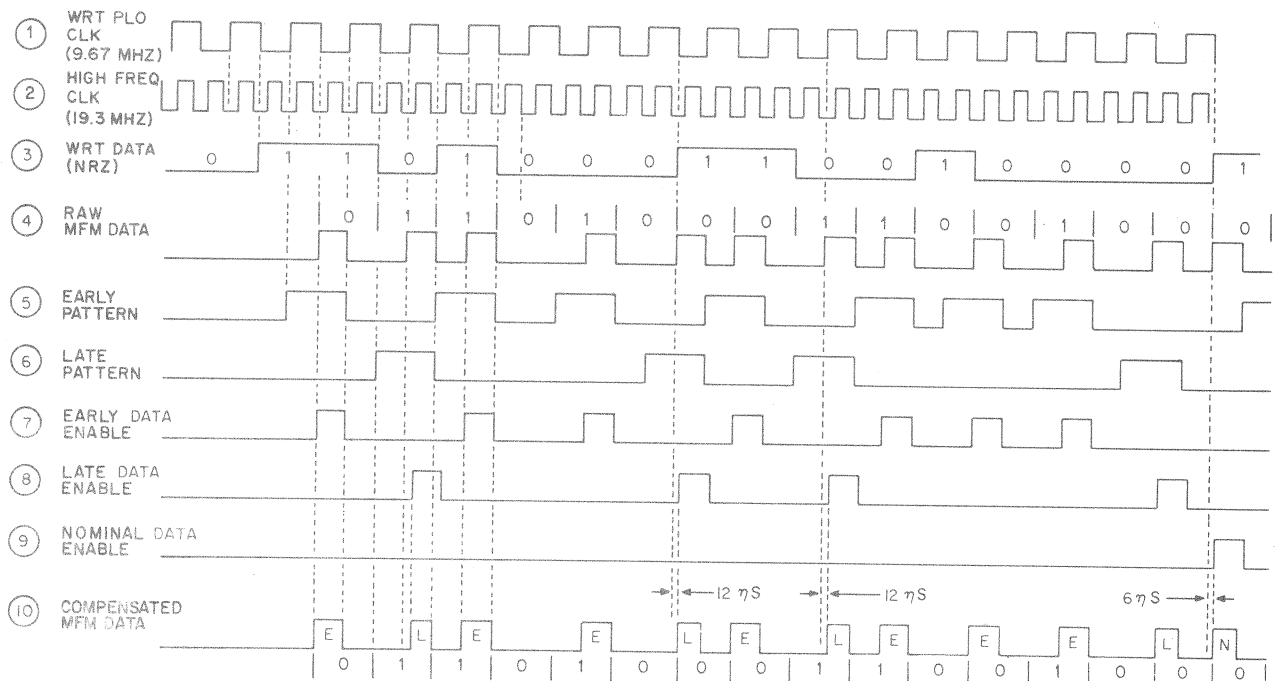
Write Data Blockdiagramm MBA





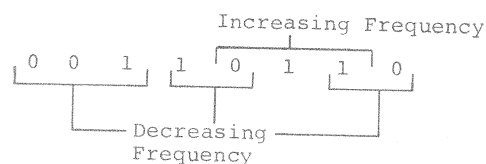


Normal is already 6ns late.
Hence ϕ is ~~now~~ 6ns is nominal 12ns is late (Rms)
Early is ϕ
NRZ to MFM Converter/Write Compensation Circuit
8ns 16ns or Rms



NOTE:

NUMBERS ○ REFER TO LOGIC FOR WRT COMPENSATION/NRZ TO MFM CONVERTER CIRCUITS.



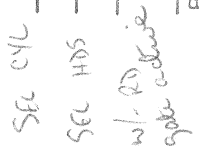
PROM OUTPUTS

READ HEADER AND DATA

<u>WORD COUNT</u>	<u>FUNCTION</u>
000→131	P EN / CRC / ECC
001	P PRECLEAR CRC / ECC
004→129	P READ GATE To <i>when sync byte found.</i>
011	P LFS, BRANCH (128)
128	P HEADER AREA (FMT and CYL) Gen SCLK <i>SYS clock</i>
129	P HEADER AREA (TRACK and SECTOR) Gen SCLK
130	P EN CRC OUT, BR RD TO WRT
132→417	P READ GATE To
136	P LFS, BRANCH (161)
161→416	P DATA EN SCLK
416	LAST READ DATA
417→418	P EN ECC OUT
419	P EN EBL

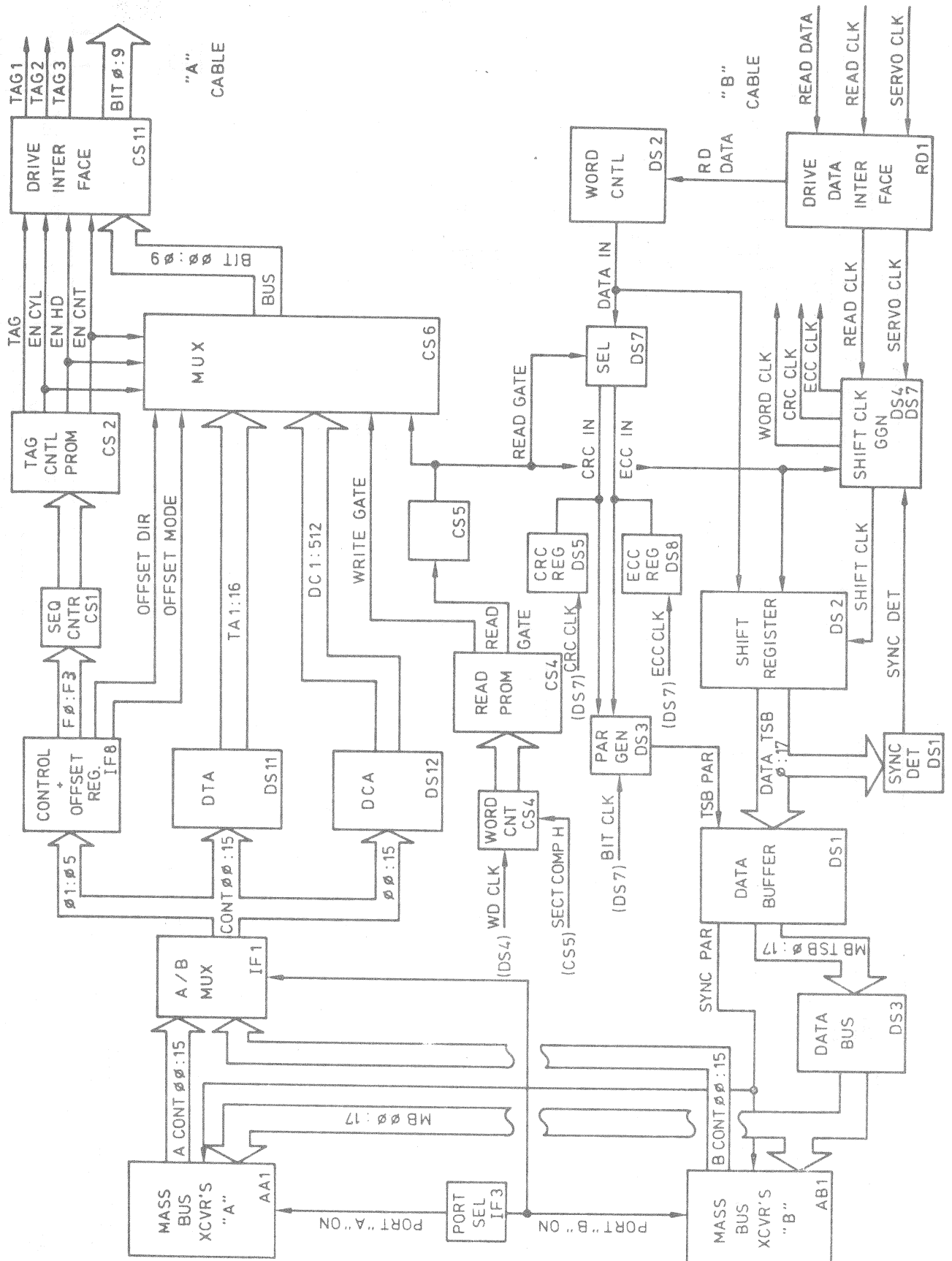
READ DATA

Same as READ HEADER AND DATA except there is no SCLK generated at word counts 128 and 129. *Header read & compared but not sent to RH70.*



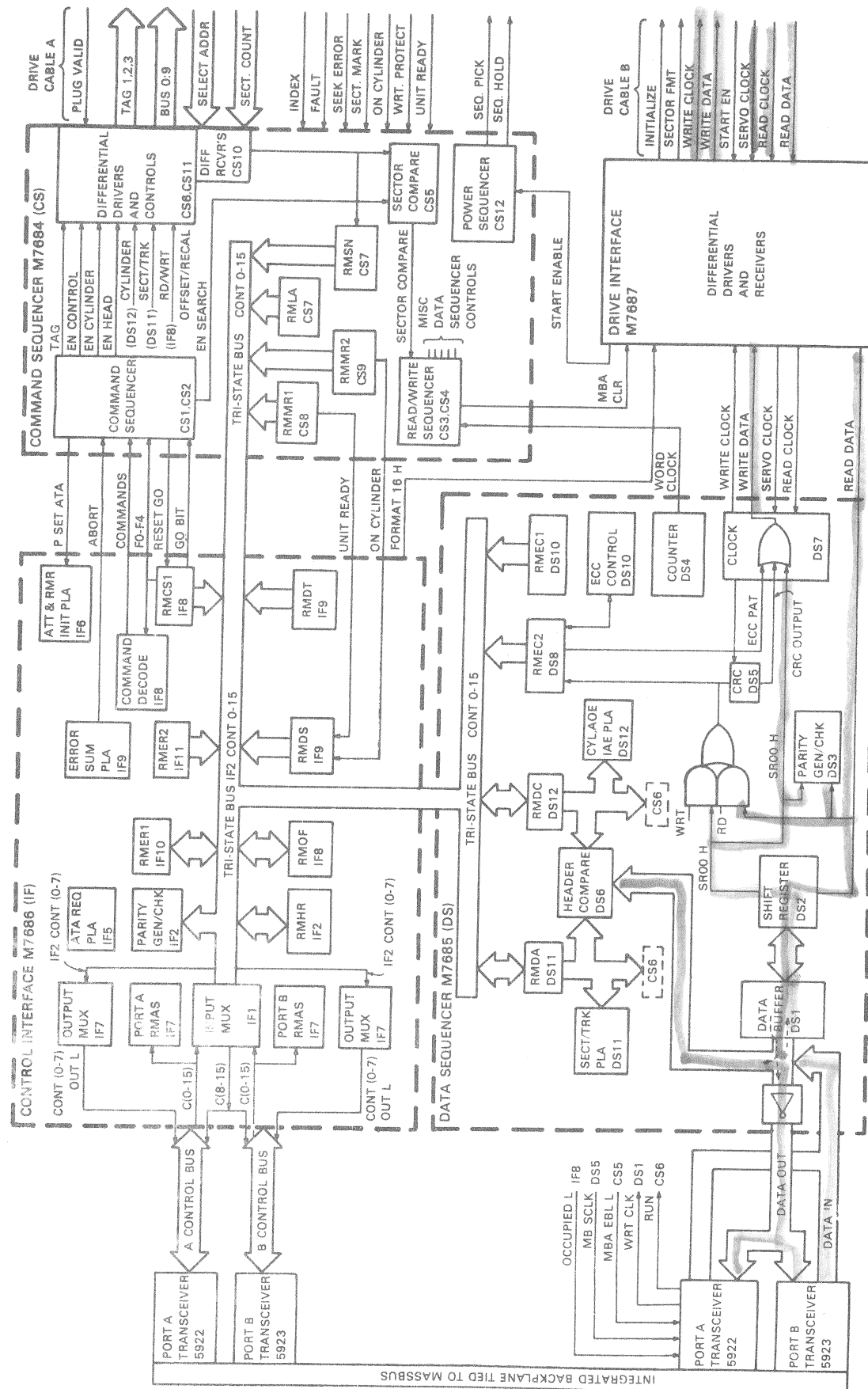
Read Data Blockdiagramm MBA

digital
SCHULUNGSZENTRUM
MÜNCHEN

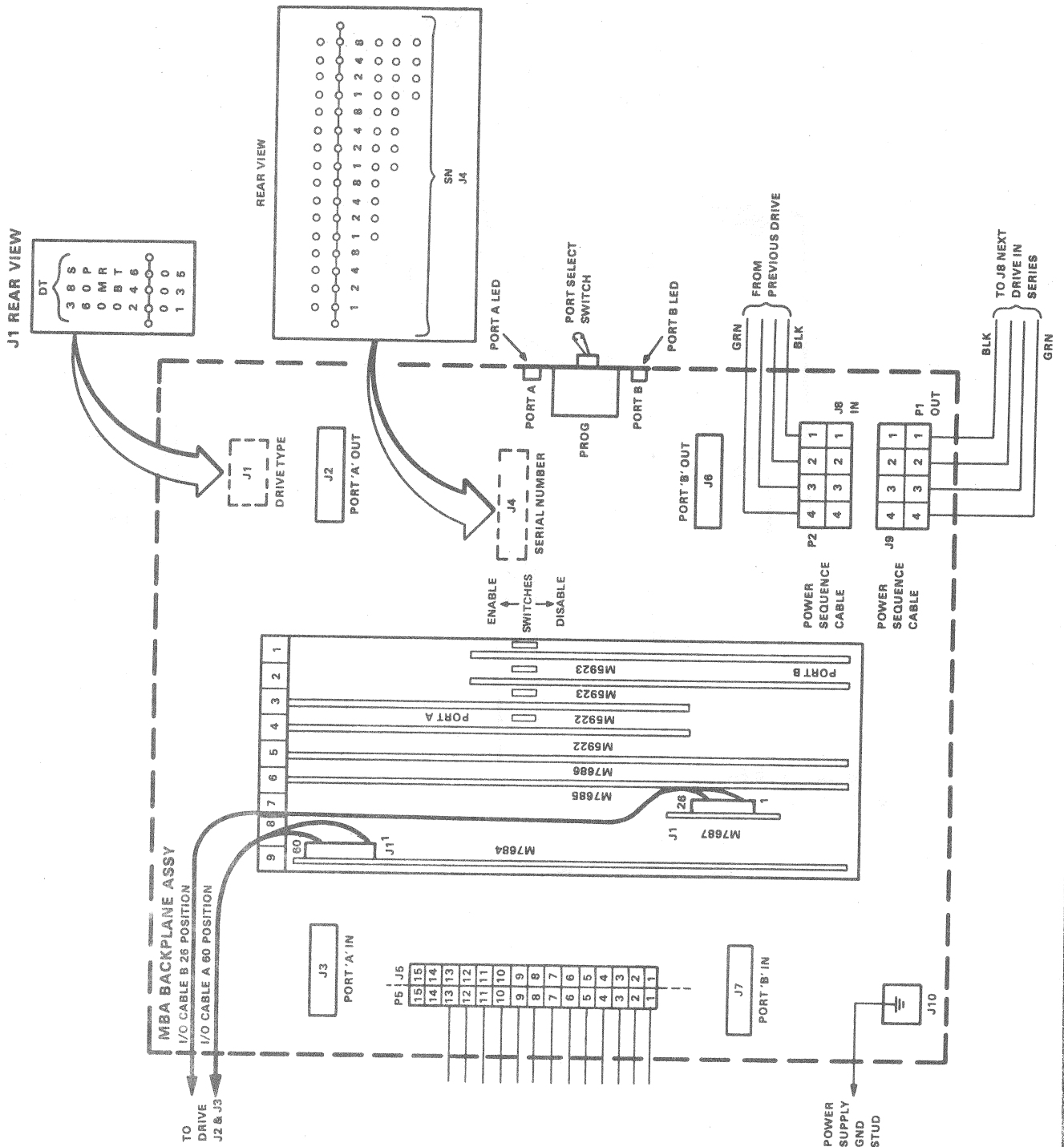


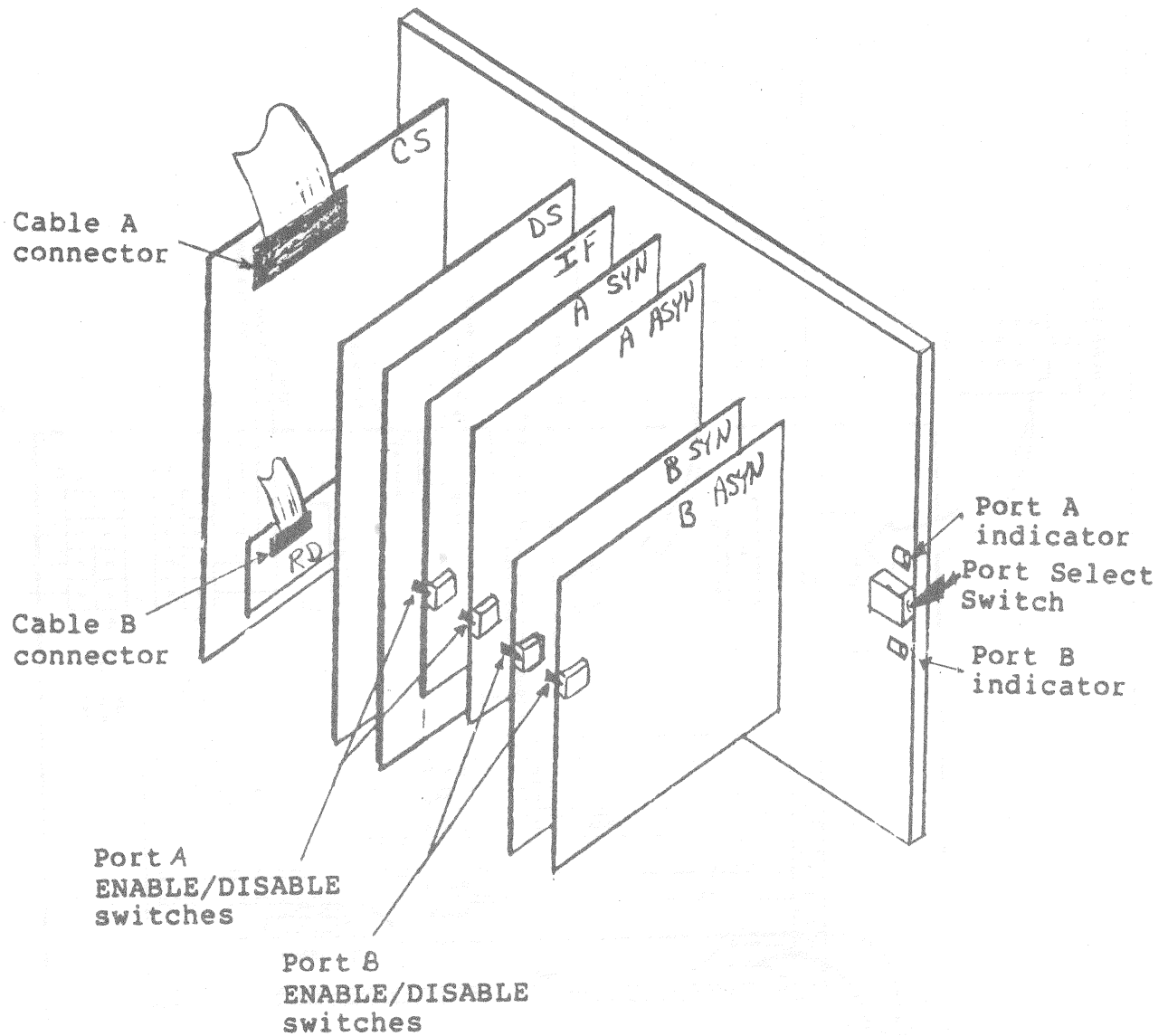
MBA Block Diagram

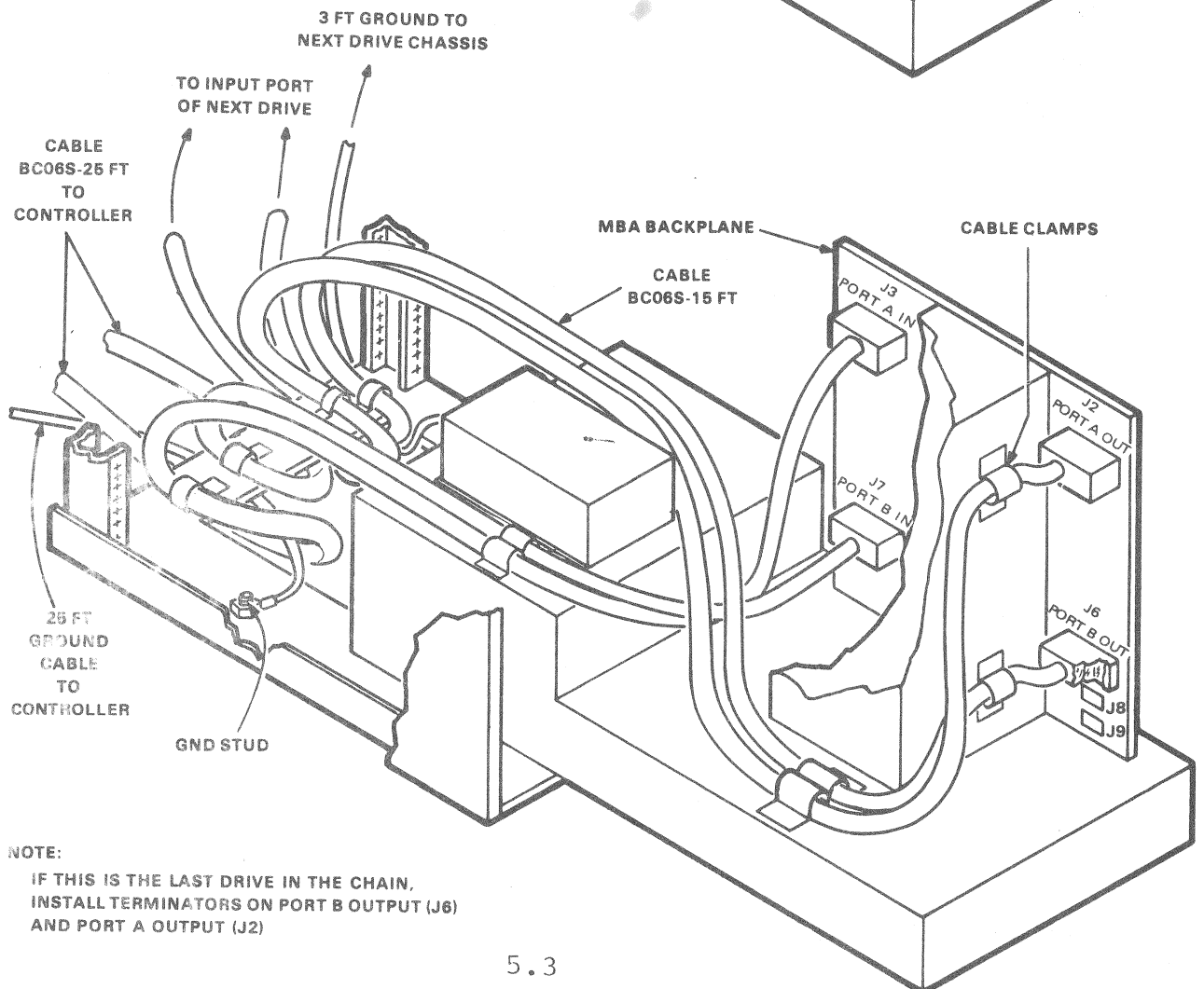
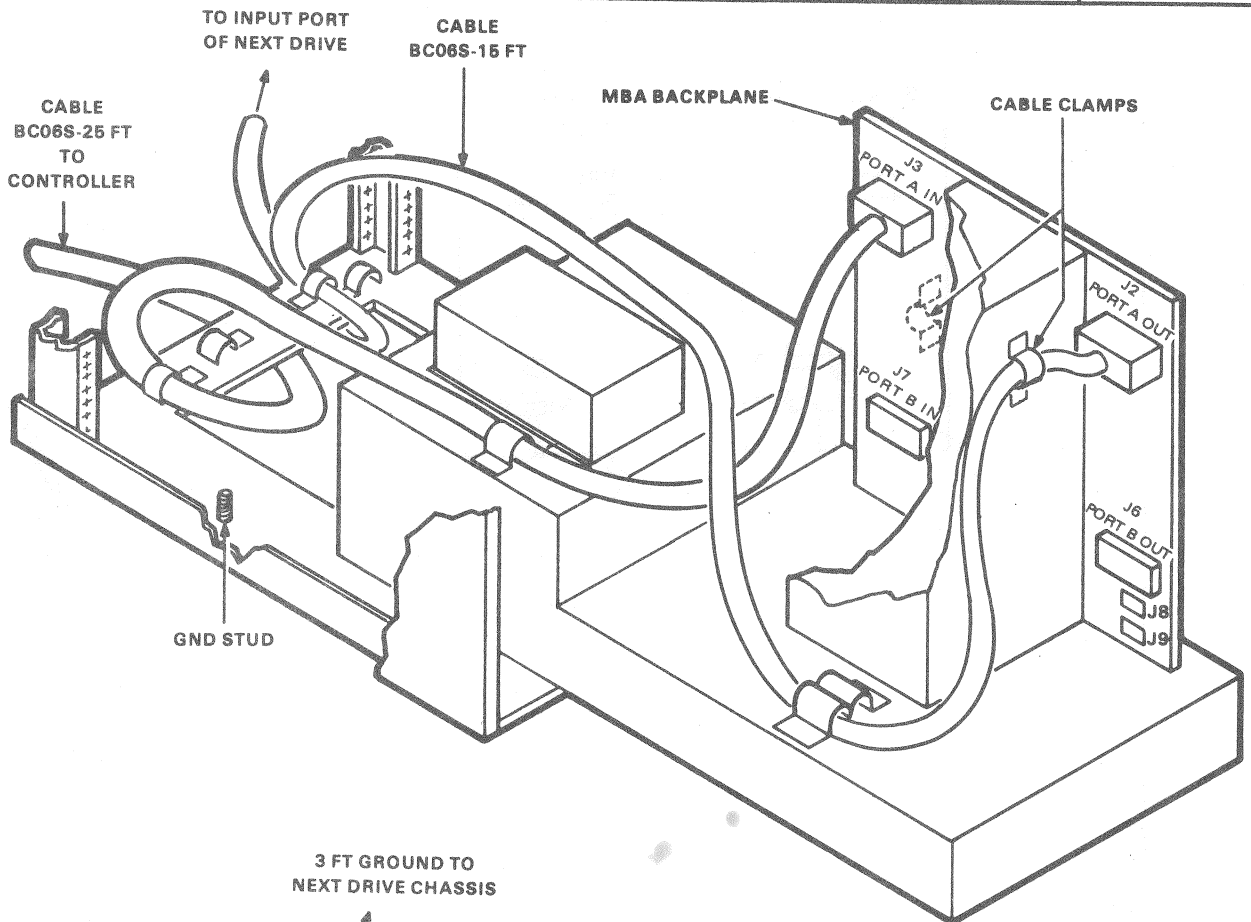
FOR R&W.

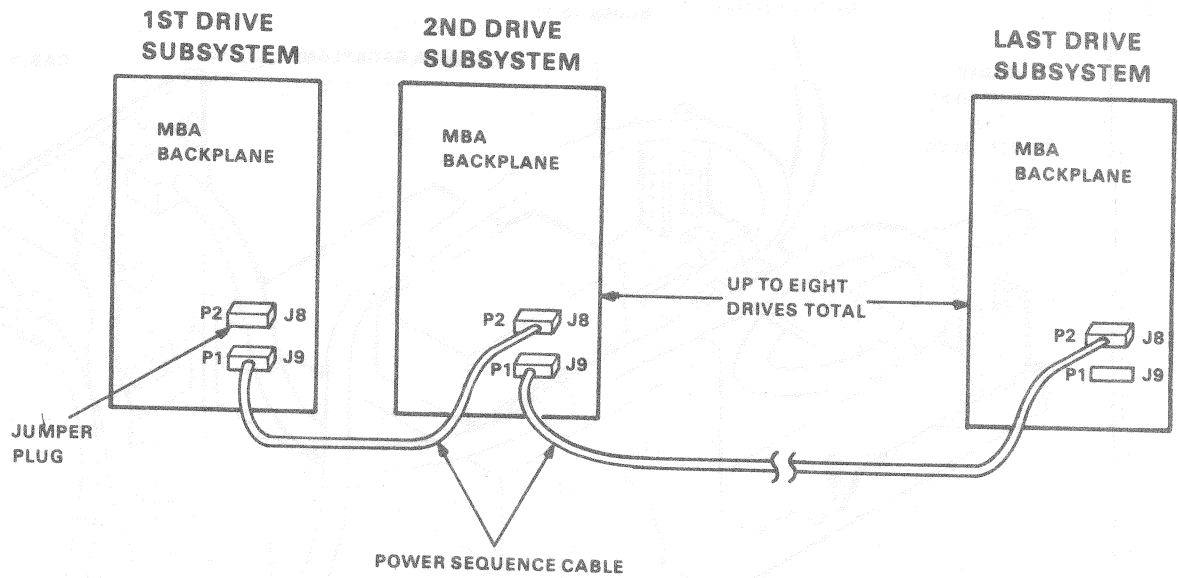


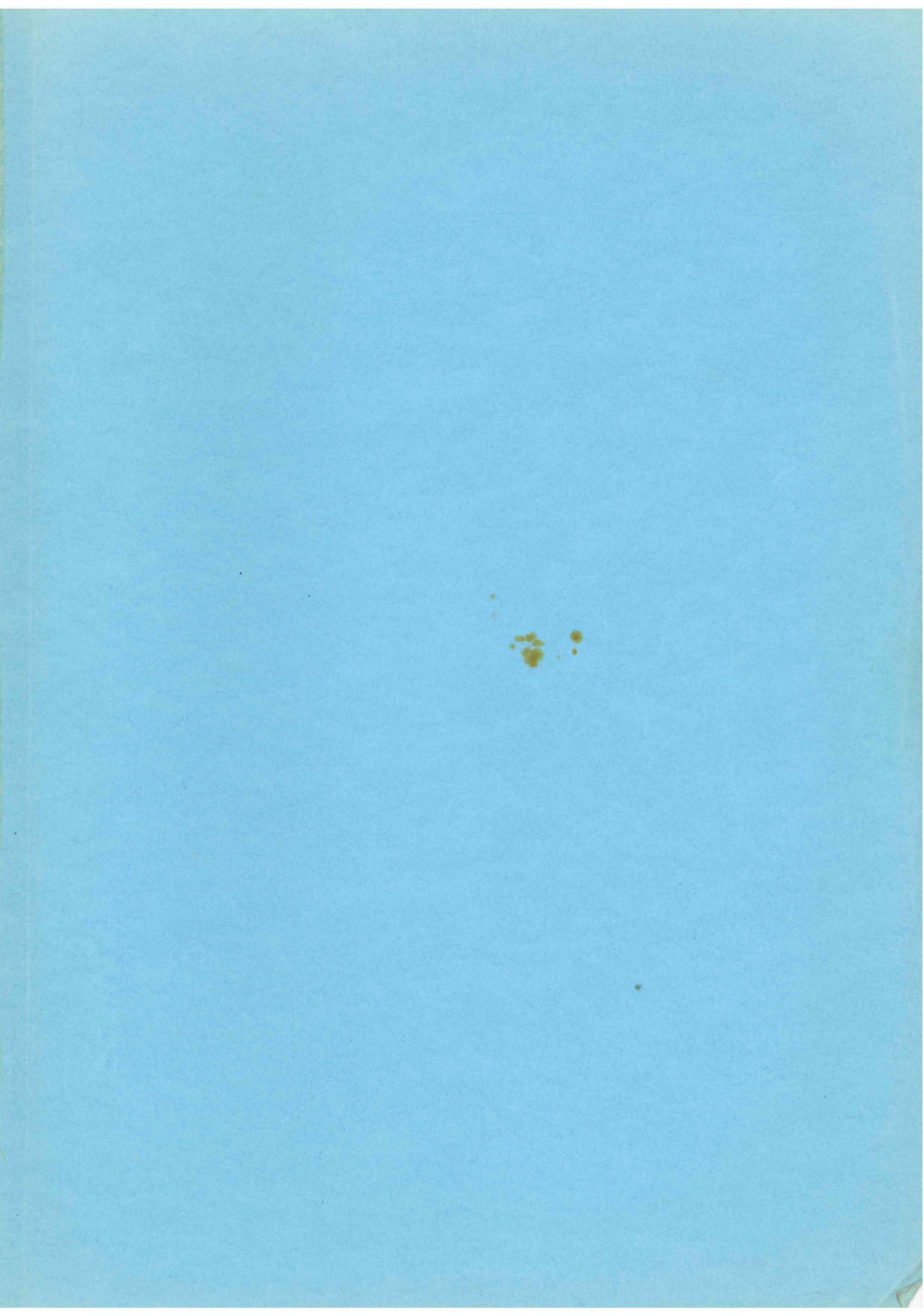
— READ —
— WRITE —











digital

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