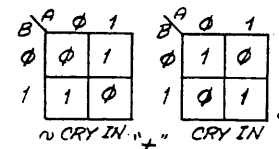
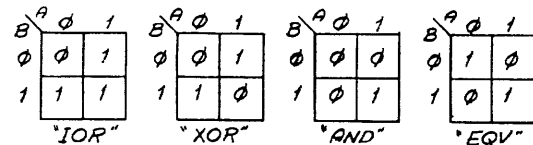


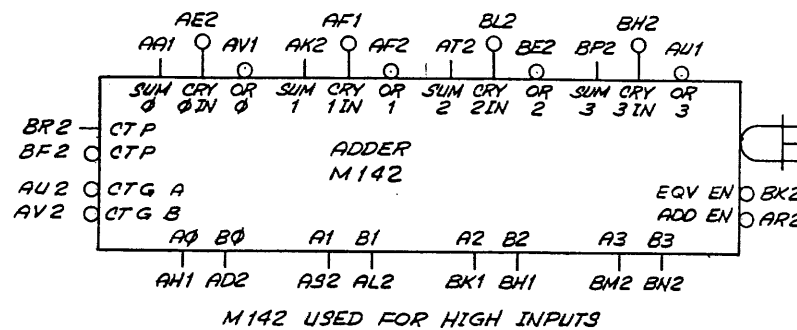
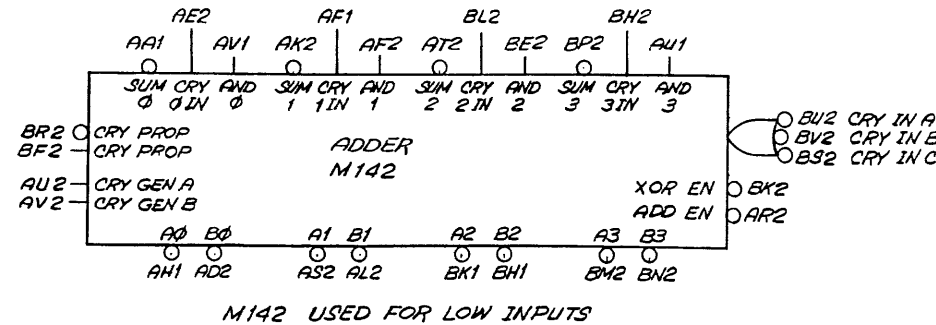
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GENERAL INFORMATION



$$\begin{aligned} A_n + B_n &= A_n \vee B_n \vee \text{CRY}_n \text{ IN} \\ &= (A_n \wedge \sim B_n \wedge \sim \text{CRY}_n \text{ IN}) \vee \\ &\quad (\sim A_n \wedge B_n \wedge \sim \text{CRY}_n \text{ IN}) \vee \\ &\quad (\sim A_n \wedge \sim B_n \wedge \text{CRY}_n \text{ IN}) \vee \\ &\quad (A_n \wedge B_n \wedge \text{CRY}_n \text{ IN}) \end{aligned}$$

UNLESS OTHERWISE INDICATED:
IC'S ARE DEC1074H -- N AS NOTED
CAPACITORS ARE .01μF 100V
RESISTORS ARE 1/4 W



THE SUM OUTPUTS REPRESENT VARIOUS FUNCTIONS DEPENDING ON THE ENABLES

~XOR EN	XOR EN
SUM = A XOR B	SUM = A XOR B
~ADD EN	ADD EN
SUM = NON-STANDARD FUNCTION	SUM = A + B

THE NON-STANDARD FUNCTION DEPENDS UPON CARRIES AND IS DIFFERENT FOR DIFFERENT BITS.

THE SUM OUTPUTS REPRESENT VARIOUS FUNCTIONS DEPENDING ON THE ENABLES

~EQV EN	EQV EN
SUM = A AND B	SUM = A EQV B
~ADD EN	ADD EN
SUM = NON-STANDARD FUNCTION	SUM = A + B

THE NON-STANDARD FUNCTION DEPENDS UPON CARRIES AND IS DIFFERENT FOR DIFFERENT BITS.

THE AND OUTPUTS REPRESENT THE "AND" OF THE INPUTS

THE CRY_n IN OUTPUTS REPRESENT THE PROPER CARRY IN TO THE PARTICULAR BIT FOR ADDITION. CRY 1 IN IS THE PROPER CARRY TERM ONLY WHEN ADD EN AND XOR EN ARE ASSERTED. CRY 1 IN IS NOT ASSERTED IF XOR EN IS NOT ASSERTED. CRY 1 IN IS NOT ASSERTED IF XOR EN IS ASSERTED BUT ADD EN IS NOT ASSERTED. THE OTHER CRY_n IN OUTPUTS ARE ALWAYS THE PROPER CARRY INTO THE PARTICULAR BITS.

THE OR OUTPUTS REPRESENT THE "OR" OF THE INPUTS

THE CRY_n IN OUTPUTS REPRESENT THE PROPER CARRY IN TO THE PARTICULAR BIT FOR ADDITION. CRY 2 IN IS THE PROPER CARRY TERM ONLY WHEN ADD EN AND EQV EN ARE ASSERTED. CRY 1 IN IS NOT ASSERTED IF EQV EN IS NOT ASSERTED. CRY 1 IN IS NOT ASSERTED IF EQV EN IS ASSERTED BUT ADD EN IS NOT ASSERTED. THE OTHER CRY_n IN OUTPUTS ARE ALWAYS THE PROPER CARRY INTO THE PARTICULAR BITS.

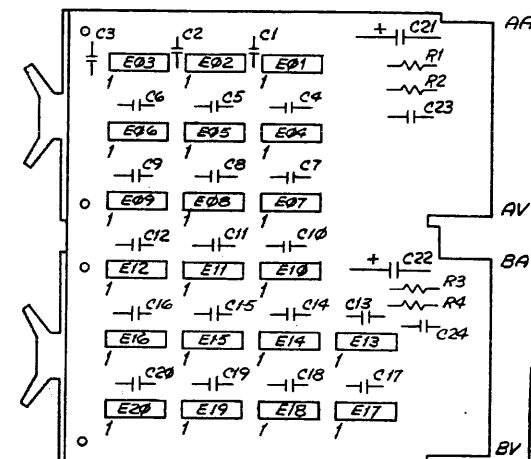
FOR LOW INPUTS

$$\begin{aligned} \text{CRY 3 IN} &= \text{CRY 1 IN} \vee \text{CRY 2 IN} \vee \text{CRY 3 IN} \\ \text{CRY 2 IN} &= (\text{CRY 3 IN} \wedge \text{A3}) \vee (\text{CRY 3 IN} \wedge \text{B3}) \vee (\text{A3} \wedge \text{B3}) \\ \text{CRY 1 IN} &= (\text{CRY 2 IN} \wedge \text{A2}) \vee (\text{CRY 2 IN} \wedge \text{B2}) \vee (\text{A2} \wedge \text{B2}) \\ \text{CRY 1 IN} &= (\text{CRY 1 IN} \wedge \text{A1}) \vee (\text{CRY 1 IN} \wedge \text{B1}) \vee (\text{A1} \wedge \text{B1}) \\ \text{CRY PROP} &= (\text{A3} \vee \text{B3}) \wedge (\text{A2} \vee \text{B2}) \wedge (\text{A1} \vee \text{B1}) \wedge (\text{A0} \vee \text{B0}) \\ \text{CRY GEN} &= (\text{A0} \wedge \text{B0}) \vee (\text{A1} \wedge \text{B1}) \wedge (\text{A0} \vee \text{B0}) \vee (\text{A2} \wedge \text{B2}) \wedge (\text{A1} \vee \text{B1}) \wedge (\text{A0} \vee \text{B0}) \vee (\text{A3} \wedge \text{B3}) \wedge (\text{A2} \vee \text{B2}) \wedge (\text{A1} \vee \text{B1}) \wedge (\text{A0} \vee \text{B0}) \end{aligned}$$

FOR HIGH INPUTS

$$\begin{aligned} \text{CRY 3 IN} &= \text{CRY 1 IN} \wedge \text{CRY 2 IN} \wedge \text{CRY 3 IN} \\ \text{CRY 2 IN} &= (\text{CRY 3 IN} \wedge \text{A3}) \vee (\text{CRY 3 IN} \wedge \text{B3}) \vee (\text{A3} \wedge \text{B3}) \\ \text{CRY 1 IN} &= (\text{CRY 2 IN} \wedge \text{A2}) \vee (\text{CRY 2 IN} \wedge \text{B2}) \vee (\text{A2} \wedge \text{B2}) \\ \text{CRY 1 IN} &= (\text{CRY 1 IN} \wedge \text{EQV EN}) \vee (\sim \text{ADD EN} \wedge \text{EQV EN}) \\ \text{CRY 0 IN} &= (\text{CRY 1 IN} \wedge \text{A1}) \vee (\text{CRY 1 IN} \wedge \text{B1}) \vee (\text{A1} \wedge \text{B1}) \\ \text{CTP} &= (\text{A3} \wedge \text{B3}) \vee (\text{A2} \wedge \text{B2}) \vee (\text{A1} \wedge \text{B1}) \vee (\text{A0} \wedge \text{B0}) \\ \text{CTG} &= (\text{A0} \wedge \text{B0}) \vee (\text{A1} \wedge \text{B1}) \wedge (\text{A0} \vee \text{B0}) \vee (\text{A2} \wedge \text{B2}) \wedge (\text{A1} \vee \text{B1}) \wedge (\text{A0} \vee \text{B0}) \vee (\text{A3} \wedge \text{B3}) \wedge (\text{A2} \vee \text{B2}) \wedge (\text{A1} \vee \text{B1}) \wedge (\text{A0} \vee \text{B0}) \end{aligned}$$

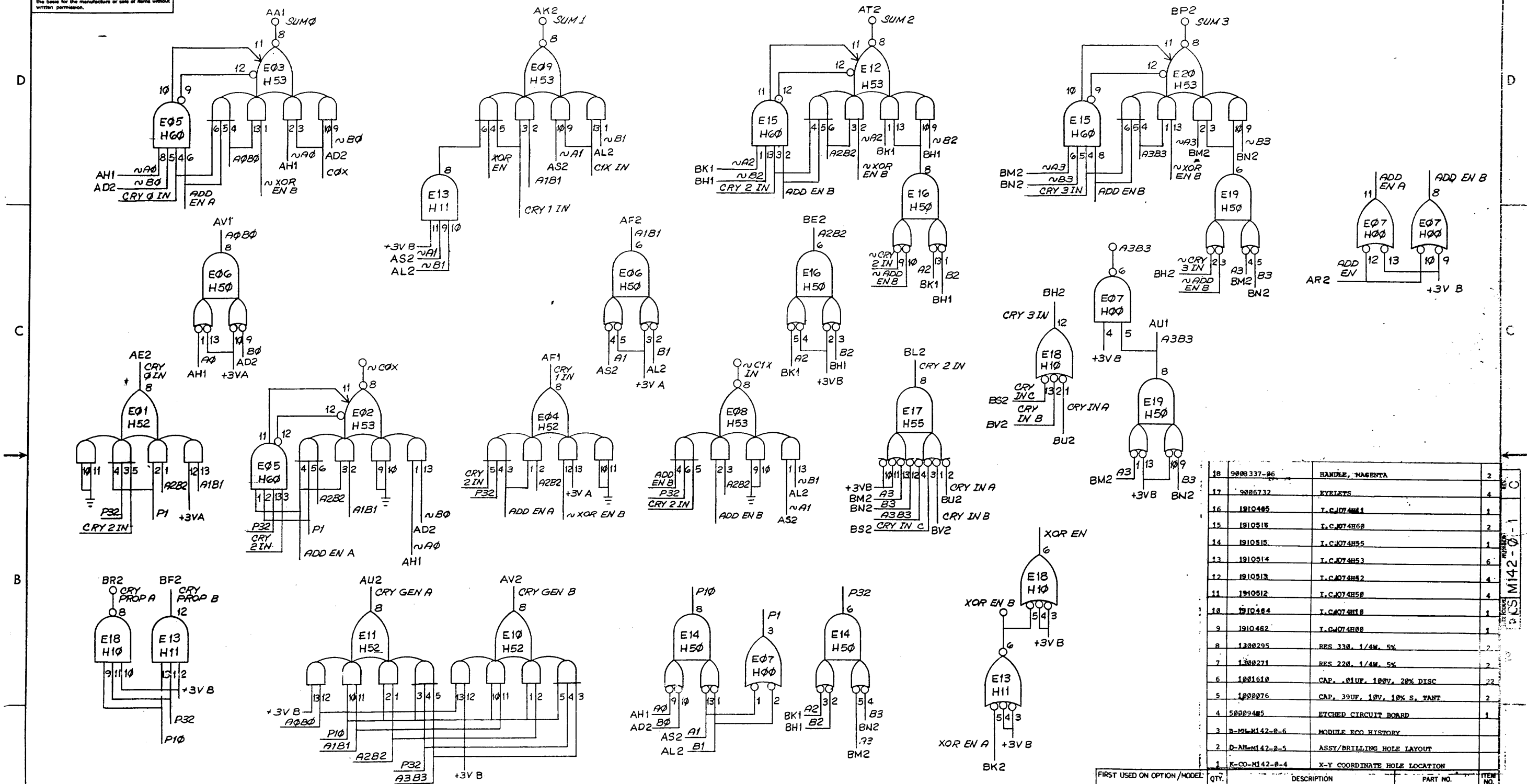
NOTE SUBTLE DIFFERENCE FROM CRY GEN ABOVE



NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

ETCHREVA		QTY.		DESCRIPTION		PART NO.		ITEM NO.	
FIRST USED ON OPTION/MODEL		DATE		DATE		DATE		DATE	
UNLESS OTHERWISE SPECIFIED		CHK'D.		DATE		DATE		DATE	
UNLESS OTHERWISE SPECIFIED		DATE		DATE		DATE		DATE	
TOLERANCES		DIMENSION IN INCHES		TOLERANCES		DIMENSION IN INCHES		TOLERANCES	
DECIMALS		FRACTIONS		ANGLES		DECIMALS		FRACTIONS	
± .005		± 1/64		± 0°30'		± .005		± 1/64	
FINAL SURFACE QUALITY		REMOVE BURRS AND BREAK SHARP CORNERS		FINAL SURFACE QUALITY		REMOVE BURRS AND BREAK SHARP CORNERS		FINAL SURFACE QUALITY	
MATERIAL		NEXT HIGHER ASSY		MATERIAL		NEXT HIGHER ASSY		MATERIAL	
FINISH		SCALE		SHEET		1 OF 2		REV. C	
TITLE		M142		4 BIT		ADDER		REV. C	
SIZE CODE		NUMBER		DCS		M142-0-1		REV. C	
DIST.		1		2		3		4	

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NOTE
ALL SIGNAL NAMES ON THIS SHEET CONNECTED TO LOW ASSERTION
DESIGNATION CIRCLES "O" ARE AS IF SUFFIXED WITH "L". ALL SIGNAL
NAMES ON THIS SHEET NOT CONNECTED TO LOW ASSERTION
DESIGNATION CIRCLES ARE AS IF SUFFIXED WITH "H".

18	9808 337-26	HANDLE, MAGENTA	2
17	9805732	EYRIETS	4
16	1910485	I.C.4074H41	1
15	1910516	I.C.4074H50	2
14	1910515	I.C.4074H55	1
13	1910514	I.C.4074H53	6
12	1910513	I.C.4074H52	4
11	1910512	I.C.4074H50	4
10	1910484	I.C.4074H10	1
9	1910482	I.C.4074H00	1
8	1380295	RES 330. 1/4W. 5%	2
7	1380271	RES 220. 1/4W. 5%	2
6	1001610	CAP. .01UF. 100V. 20% DISC	22
5	1000076	CAP. 39UF. 10V. 10% S. TANT	2
4	50009405	ETCHED CIRCUIT BOARD	1
3	B-M4-M142-B-6	MODIFY ECO HISTORY	
2	D-AR-M142-B-5	ASSY/DRILLING HOLE LAYOUT	
1	K-CO-M142-B-4	X-Y COORDINATE HOLE LOCATION	
QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DRN. <i>27</i>	DATE <i>3/28/70</i>	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
CHDK. <i>27</i>	DATE <i>3-3-71</i>		
ENG. <i>27</i>	DATE <i>3-5-71</i>		
PROJ. ENG. <i>27</i>	DATE <i>3-5-71</i>		
PROD. <i>27</i>	DATE <i>3-5-71</i>		
FIRST USED ON		TITLE M142 4 BIT ADDER	
SCALE			
SHEET <i>2</i> OF <i>2</i>			
SIZE CODE		NUMBER	REV.
DCS		M142 - 0 - 1	C
DIST.			