DIGITAL EQUIPMENT CORPORATION
Maynard, Massachusetts
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Non-Catalog
$265.00

4709

7 BIT TRANSMITTER

The 4709 Transmitter is a parallel to serial converter, self contained on a double length DEC System Module board. This unit includes all of the parallel to serial conversion, buffering, gating and synchronizing necessary to transfer information between a parallel digital device and an outgoing serial asynchronous data line. A 7-bit character consisting of 9.0, 9.5, or 10.0 units is transmitted in serial form. The 7-bit data character is disassembled in the shift register. Start and Stop elements are added to each character transmitted. The bit immediately following the Start bit is the least significant bit.

A jumperable Stop Element Counter is provided to count out the stop time. By selective jumpering, 1.0, 1.5, or 2.0 units of stop time may be obtained.

An external device reads a 7-bit character into the shift register. If the Enable level is present at read-in time the module will be placed in the Active state when the Stop Element Counter has timed out for the preceding character. The Start Element of the character is placed on the line when the module goes into the Active state. The 7 bits of the character follow the start bit at one unit intervals. At the completion of the sending of the last data bit, the module is placed in the inactive state, the Stop element is placed on the line, the Stop Element Counter is activated, and the Flag is turned on.

The Flag indicates to an external device that a character has been transmitted and that the next character can be read into the shift register.

The time in which the next character must be loaded in order to insure maximum transmission rates varies with the length of the Stop element and the speed. The following formula may be used to determine the time:

$$T \quad \text{(seconds)} = \frac{\text{Stop Element (units)}}{\text{baud (bits per second)}}$$

Note that when the character has been transmitted, the shift register is zero. The next character is read in by transferring ones. The only way this register can be cleared is by transmitting a character.

A level input (wait) is provided to prevent the Stop Element Counter from timing out. When the level is removed the Stop Element Counter will time out for the jumpered stop unit time minus 1/2 to 1 unit (variation is due to clock synchronism). By connecting the Receiver Active to this input the "turn around" condition is satisfied during half duplex operation.

The Clock input should be two times the baud or bit frequency. The maximum Clock input is 25 kc, which will permit the baud rates up to 12.5 kc.

The transmitter may be connected to devices other than DURA MACH 10 i.e., interface between two computer systems, displays, etc. There are two data output terminals. An inverter and a power inverter (similar to one section of a Type 4689) provide dual complementary outputs. The output of the line flip-flop is jumperable to the inverter input (which in turn drives an output power inverter) to provide output signal flexibility.

An indicator light mounted on the handle provides a means of observing the state of the Flag. A switch mounted on the handle opens (floats) the Flag output circuit.

Bits may be present in the shift register when power is initially supplied to the module. It is recommended that a character of all "ones" be transmitted as the first character following resumption of power. Otherwise the first character transmitted may be incorrect.

INPUTS: Clock: DEC Standard 0.4 microsecond negative pulses or equivalent. Loading is one unit of Pulse Load. Clock frequency should be twice element or baud frequency, and no greater than 25 kc.

Read In: DEC Standard 0.4 microsecond negative pulses or equivalent. Loading is one unit of Pulse Load. When jumper F is in the load is two units of Pulse Load.

Bits 1, 2, 3, 4, 5, 6, 7, and Enable: DEC Standard Levels or equivalent. The gate is enabled by a ground, present at least one microsecond before the Read-In terminal is pulsed, and disabled by a negative level, which must be present for at least two microseconds before the gate is pulsed. There is no DC load; the transient load is 2 units of Base Load, or 1/4 unit of Emitter Load, depending on the direction of the level change. Time constant is 0.5 μsec.

Clear Flag: DEC Standard Levels or Standard 0.4 microsecond negative pulse or equivalent. Input must be at ground while transmitting data. Loading is one unit of Pulse Load (1/8 unit of DC Emitter Load if level is used).

Wait: DEC Standard Levels. This input is enabled by negative levels. Loading is 1 unit of base load. Restrictions exist on use of this input at the time Active is cleared. See Chart below:

STOP CODE JUMPERS	STOP CODE UNITS	TO AVOID SHORT STOP ELEMENT			
		WAIT MUST EXTEND		IF IT HAS BEEN NEGATIVE LESS THAN	
C	1	0	elements after Active is cleared.	-	elements before Active is cleared.
A, C	1 1/2	1/2		1/2	
A, B	2	1/2		1	

OUTPUTS: Data Output Pin W: DEC Standard Level capable of driving 4 units of Base Load, 0.5 units of DC Emitter Load, and any number of Pulsed Emitter Loads provided not more than one is pulsed at a time.

Data Output Pin V: Output is capable of driving currents up to 100 ma from negative voltages which are no greater than -15 volts. The output is clamped so it can be no more negative than -15 volts.

Active: Resistor coupled output capable of driving 2 units of Base Load. The Active flip-flop cannot be cleared by grounding this output.

Flag: DEC Standard Level capable of driving 6 units of Base Load, 0.5 units of DC Emitter Load, and any number of Pulsed Emitter Loads provided not more than one is pulsed at a time. Output line may be opened (floated) by a series switch. Hence it is suggested that this output drive Base Loads.

Indicator Lamp: Provides visual indication of the Flag flip-flop. Light on indicates Flag Flip-flop set.

POWER REQUIREMENTS: -15 volts/ 225 ma (not including any loads on Pin V);
+10 volts (A)/ 9 ma.

DEC CONVENTION FOR DESIGNATING INTERNAL JUMPERS:

(1) Line Flip-flop Output: 1 = -3 v, 0 = ground during Mark state.

(2) Jumpers A, B, C,: C 1 unit Stop code
AC 1 1/2 unit Stop code
AB 2 unit Stop code

(3) Jumper F: Flag is cleared on Read-in if other leg of AND circuit is negative or floating.

Jumpering code following the above sequence:

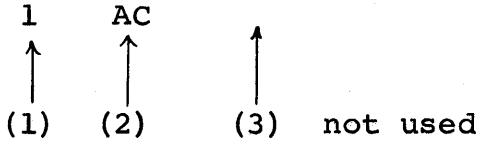
Example I

(1) Line Flip-flop = 1

(2) Jumper AC in

(3) Jumper F out

becomes 1AC



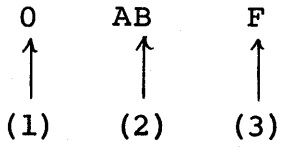
Example II

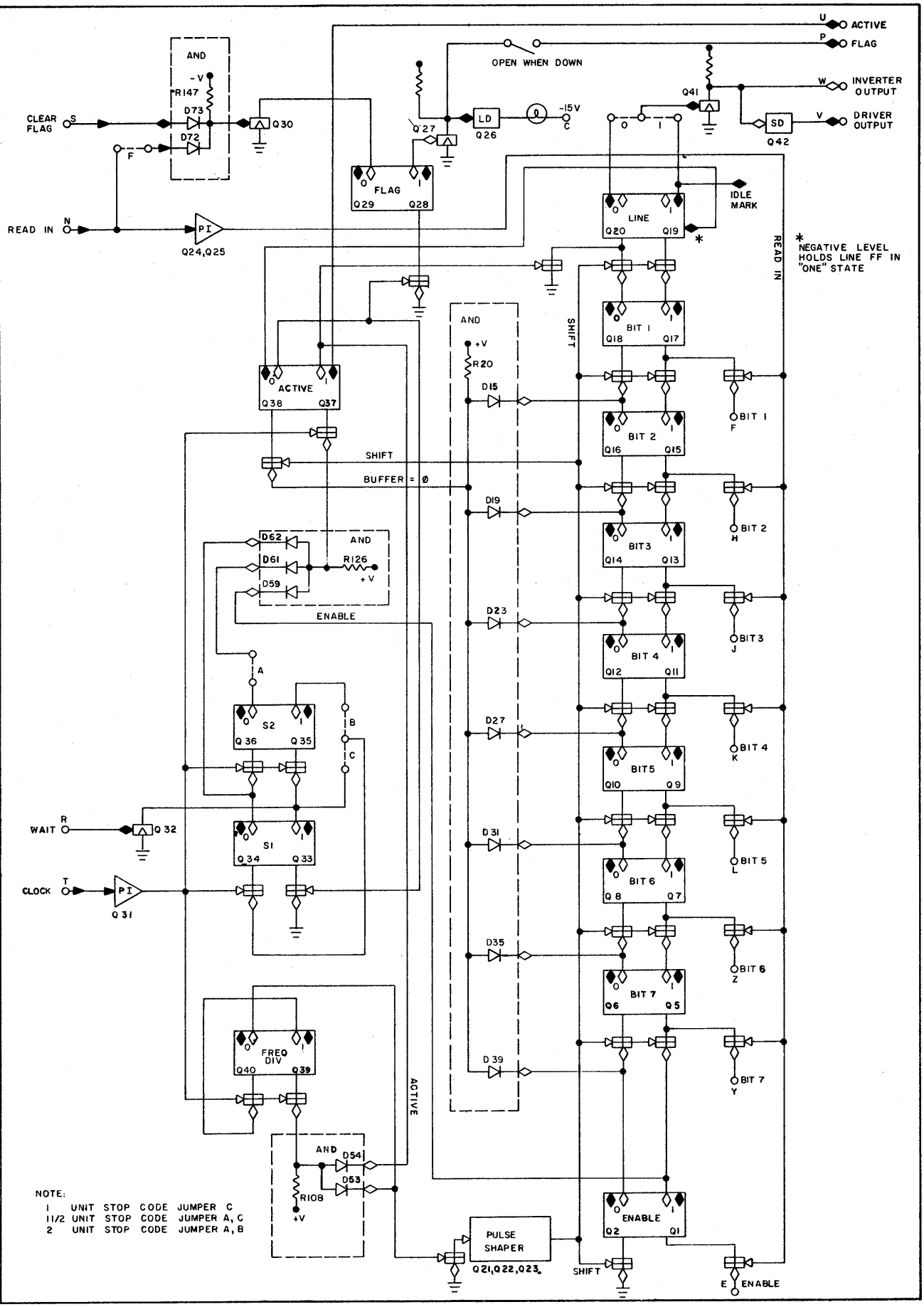
(1) Line Flip-flop = 0

(2) Jumper AB in

(3) Jumper F in

becomes 0ABF





NOTE:
1 UNIT STOP CODE JUMPER C
1 1/2 UNIT STOP CODE JUMPER A, C
2 UNIT STOP CODE JUMPER A, B

ECO NO.	ENG.	REVISIONS

DRAFTSMAN I. HAHN DATE 6-30-65
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PRODUCTION DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 7 BIT TRANSMITTER 4709

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