

Skip on Data Ready (VSDR)

Octal Code: 6561

Execution Time: 2.6 μ s

Operation: Set a data ready flag when the scanning voltmeter has selected a channel and digitized the analog signal. This instruction is used to test for the data ready flag.

Read Data and Clear Flag (VRD)

Octal Code: 6562

Execution Time: 2.6 μ s

Operation: Transfers the content of the selected byte of the IDVM output word to the accumulator and clears the data ready flag. The first data available after the flag is set is always byte 1. Subsequent bytes are program-selected using the Byte Advance command (see Figure 7-26).

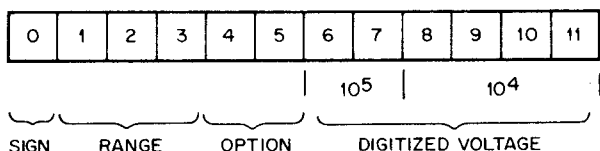


Figure 7-26 Data Word (to Computer)

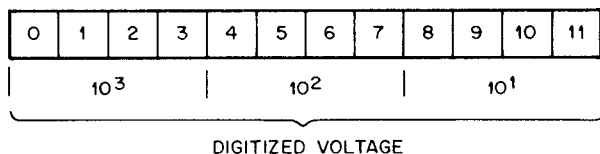


Figure 7-27 Data Word (to Computer)

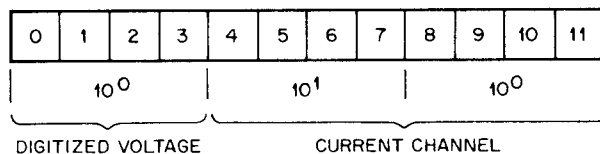


Figure 7-28 Data Word (to Computer)

All address and digitized data is in 8-4-2-1 BCD format.

Byte Advance (VBA)

Octal Code: 6564

Execution Time: 2.6 μ s

Operation: The total data word from the AF04A is 36 bits long. The first data word after the flag is set is always the 12 most significant bits. The BYTE ADVANCE command requests the next 12 most significant bits. When the data is available, the data ready flag is set again. To select the 12 least significant bits, a second BYTE ADVANCE command is required. When the data is available, the data ready flag is set again.

Sample Current Channel (VSCC)

Octal Code: 6571

Execution Time: 2.6 μ s

Operation: Digitizes the analog signal on the current channel. This command is not required except when multiple samples are required on any channel. (Using this command on a preselected channel saves up to 10 ms per sample.)

Frequency and Period Measurement Options for AF04A

A separate input permits the IDVM to be used as a frequency counter capable of counting to 2 MHz with selectable gate times of 1, 10, and 100 ms, providing measurement resolution of 10 Hz. Increased accuracy at low frequencies (to 10 kHz with automatic 250% overranging) is accomplished with the period-measurement mode. This mode counts an internal frequency source for 1, 10 or 100 periods of the frequency being measured, thereby providing increased full-scale accuracy. Period readout is in milliseconds. Frequently and voltage measurements may be made within one scanning cycle by grouping all frequency inputs in one master or slave scanner and all voltage inputs in another master or slave scanner. The output of one scanner may then be connected to the frequency-input connector of the IDVM, and the output of the other scanner to the voltage input. One of the optional control word bits is used to program the IDMV for frequency or period measurements.

Specifications (See Figure 7-29)

Frequency Measurements

Range: 10 Hz to 2 MHz

Sensitivity: 100 mV rms or -1V pulses, at least 0.3 μ s wide at 50% points. 100V rms maximum working voltage.

Input Impedance: 22K shunted by less than 1000 pF, including internal cabling.

Time Base: 100 kHz crystal oscillator with initial accuracy of + or - 0.0005%, long-term stability + or - 0.001%/wk; temp. coefficient + or - 0.0002%/degrees C.

Period Measurements

Range: 1, 10, and 100 period average. Input frequency from 10 Hz to 25 kHz sine wave or 0.1 pps to 25,000 pps.

Sensitivity: 100 mV rms or - IV pulses, at least $0.3\mu\text{s}$ wide at 50% points. 100V rms maximum working voltage.

Input Impedance: 22K shunted by less than 1000 pF, including internal cabling.

Accuracy: ± 1 count + time base accuracy + trigger error. Trigger error $< \pm 0.03\%$ for 100 mV rms sine wave with 40 dB signal-to-noise ratio.

Time Base: 100 kHz crystal oscillator with initial accuracy of $\pm 0.0005\%$, long-term stability $\pm 0.0001\text{T/wk}$; temp. coefficient $\pm 0.0002\%/^\circ\text{C}$.

Selected Resolution

Selected Resolution	0.001%		0.01%		0.1%	
	Maximum Reading	Resolution	Maximum Reading	Resolution	Maximum Reading	Resolution
Frequency	2000.00kHz	10Hz	02000.0kHz	100Hz	002000kHz	1kHz
Period	99.9999msec	$0.1\mu\text{s}$	999.999msec	$1.0\mu\text{s}$	9999.99msec	$10\mu\text{s}$

Figure 7-29

Additional AF04-A Options

A type AF04-X expansion Mounting Panel is available which provides an additional 200 channels. For each 10 channels implemented, the Type AF04-S 10-Channel Guarded Reed Relay Multiplexer Switch is required.

Thermocouple reference junctions

Extended scanner for more than 1000 channels

AA50-A Digital-To-Analog Conversion Subsystem

The AA50-A DAC is a general-purpose, program-controlled DAC subsystem that converts 12-bit (11 bits plus sign) words into analog outputs having a continuously adjustable full-scale range of 0 to $\pm 10V$ at 10 mA.

The AA50-A is housed in a H911 type mounting panel and is furnished complete with power supply, I/O cables, control and interface logic, and up to six DAC modules, each providing one analog output. The unit interfaces with the external bus of the PDP-8/E. All operations are controlled by IOT instructions, including the selection of the DAC module to receive the 12-bit output word. Each DAC module contains a buffer register and a scaling amplifier with reference mounted on the same module.

For an output function, the computer issues an IOT instruction that specifies the DAC module to receive the 12-bit word. The control logic of the AA50-A decodes the IOT, performs input gating for the 12-bit word from ACO-11, and loads the words into output buffer of the designated DAC module. The word remains in the output buffer until the buffer is updated by another input; thus, the resulting analog output is available until updating occurs.

Specifications

Digital Input	Parallel, 11 bits plus sign in two's complement form
Coding	3777 (octal) = + 10V 0000 (octal) = 0V 4000 (octal) = - 10V
Standard Analog Output	0 to $\pm 10V@$ 10 ma (adjustable)
Settling Time	$20\mu s$ to $\frac{1}{2}$ LSB (measured at output connector with no capacitive loading)
Accuracy	0.05% of full scale
Linearity	$\pm \frac{1}{2}$ LSB ($\pm 2.44mV$ for $\pm 10V$ DAC output)
Capacitive Loading	0.1 μf at output connector will not cause instability

Programming

The following instructions are associated with AA50-A operation:

Select DAC 0 (DACS0)

Octal Code: 6551

Execution Time: 2.6 μ s

Operation: Transfers content of AC to DAC module 1 and converts it to analog output.

Select DAC 1 (DACS1)

Octal Code: 6552

Execution Time: 2.6 μ s

Operation: Transfers content of AC to DAC module 2 and converts it to analog output.

Select DAC 2 (DACS2)

Octal Code: 6553

Execution Time: 3.6 μ s

Operation: Transfers content of AC to DAC module 3 and converts it to analog output.

Select DAC 3 (DACS3)

Octal Code: 6554

Execution Time: 2.6 μ s

Operation: Transfers content of AC to DAC module 4 and converts it to analog output.

Select DAC 4 (DACS4)

Octal Code: 6555

Execution Time: 3.6 μ s

Operation: Transfers content of AC to DAC module 5 and converts it to analog output.

Select DAC 5 (DACS5)

Octal Code: 6556

Execution Time: 3.6 μ s

Operation: Transfers content of AC to DAC module 6 and converts it to analog output.

Device codes 56 and 57 are used when additional (up to three total) AA50's are required.

AA05-A/AA07 Digital-to-Analog Converter and Control

The AA05 Digital-to-Analog Converter (DAC) provides housing power and control for up to 24 10-bit DAC modules. The AA07 Expansion Unit extends the capacity of the system to 64 channels of DAC.

Each conversion channel may use any of four printed circuit card DAC modules. These modules include two single-buffered units, Types A608 and A609, and two double-buffered units, Types A610 and A611. A608 is a single-buffered, 10-bit DAC, with unipolar output (0V to + 10V). Type A609 is a single-buffered, 10-bit DAC with bipolar output and variable offset. A610 and A611 are similar to A608 and A609, respectively, except that the former are double-buffered units.