EK-0TU77-PS-002

TU77 Subsystem

Pocket Service Guide

digital

EK-CTU77-PS-002

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Pocket Service Guide

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CONTENTS

FIGURES

TABLES

1 INTRODUCTION

1.1 OVERVIEW

The TU77 is a magnetic tape transport that records and reads data in 9-track, non-return to zero (NRZI) or phase-encoded (PE) format. Bit density is 800 bits/in for the NRZI format and 1600 bits/in for the PE format. The transport can read data in either forward or reverse direction. The read/write tape speed for both directions is 125 in/s. The nominal rewind time for a 731.5 m (2400 ft) reel is 65 s.

The TU77 interfaces with the system processor via the MASSBUS, a MASSBUS controller, and a TM03 tape formatter. Up to four TU77s can be driven from one TM03. Figure 1-1 shows the basic system configuration for a TU77. The TM03 and its power supply (H7420DA) are housed in the TU77 cabinet (H9602-KA corporate cabinet). A TU77 containing a TM03 is a *master unit*. A TU77 without the TM03 is a *slave unit*.

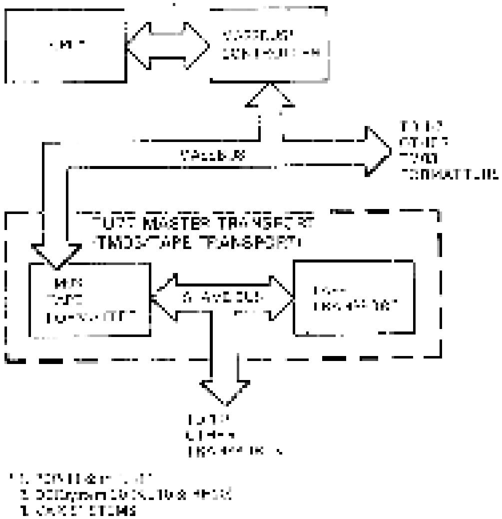

Figure 1-1 Basic System Configuration

1.2 CONTROLS AND INDICATORS

Two groups of controls and indicators are in the TU77 cabinet. One group is the operator control panel, the other is the TU77 maintenance controls and indicators.

1.2.1 Operator Control Panel

All operator controls and indicators on the TU77 control panel are shown in Figure 1-2. Table 1-1 lists each control and its function. Table 1-2 lists each indicator and its function.

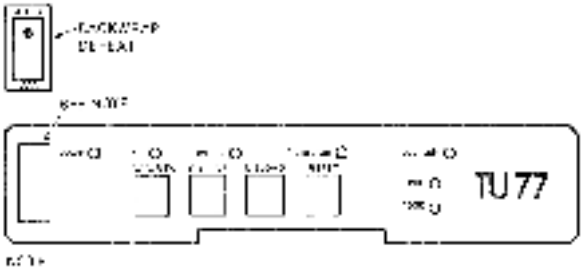

Figure 1-2 TU77 Control Panel

Table 1-1 TU77 Operator Panel Controls

Control	Function
Slave select switch (unlabeled)	Selects address (slave 0 to [illegible]) of tape transport. Each slave displays a unique number.
LOAD/REW	Pressing and releasing LOAD/REW initiates one of three sequences. 1. With no tape in path, it starts a load sequence. 2. With tape in path but not tensioned, it starts a midway load sequence. Upon completing load sequence, tape loads and runs reverse to beginning-of-tape (BOT). 3. With tape in path and tensioned and the transport off-line, tape rewinds to BOT. If tape is already at BOT or the transport is on-line, there is no effect.
ON LINE	Pressing and releasing ON-LINE switches transport from off-line to on-line. Pressing and releasing it again changes transport from on-line to off-line.
UNLOAD	If TU77 is off-line, pressing and releasing UNLOAD causes tape to rewind and unload. If tape is already at BOT, it will unload. If TU77 is on-line, UNLOAD has no effect.
RESET	Pressing and releasing RESET terminates all off-line functions or clears a load fault.
BACKWRAP DEFEAT	AUTO (automatic) position allows a backwrap and retry for 10-1/2 in reel, with or without a cartridge. MAN (manual) position inhibits a backwrap and retry for 10-1/2 in reel, without a cartridge and small reels.

Table 1-2 TU77 Operator Panel Indicators

Indicator	Function
power	Indicates presence of dc and secondary ac power.
bot	Indicates tape is at BOT.
on-line	Indicates TU77 is on-line. Transport reverts to off-line mode if any of the following events occur. 1. ON-LINE button is pressed. 2. An external rewind unload command is received. 3. Vacuum column interlock is broken. 4. AC power is lost. 5. RESET button is pressed.
file protect	Indicates that a reel of tape without a write-enable ring has been loaded onto the transport.
load fault	Indicator flashes when a load fault occurs. For example, it happens 1. when an autoload sequence fails to load a tape from a 267 mm (10-1/2 in) reel after two attempts 2. when an load sequence fails to load tape from a 216 or 178 mm (8-1/2 or 7 in) reel after only one attempt. 3. when a load sequence fails to load tape from a 267 mm (10-1/2 in) reel upon manual load after only one attempt.
800	Indicates transport is set to read or write at 800 bits/in (NRZI mode).
1600	Indicates transport is set to read or write at 1600 bits/in (PE mode).

1.2.2 Maintenance Switch and Indicator Functions

Three printed circuit board assemblies (PCBAs) in the card cage behind the base assembly contain manual switches and indicators for maintenance. Figure 1-3 shows where these switches and indicators (light emitting diodes or LEDs) are located. Table 1-3 lists each indicator function on the M8940 MTA PCBA. Table 1-4 lists each switch function on the M8940 MTA PCBA. Table 1-5 lists the functions of both S1 switches, S1/S2 on the control PCBA and S1 on the reel servo PCBA.

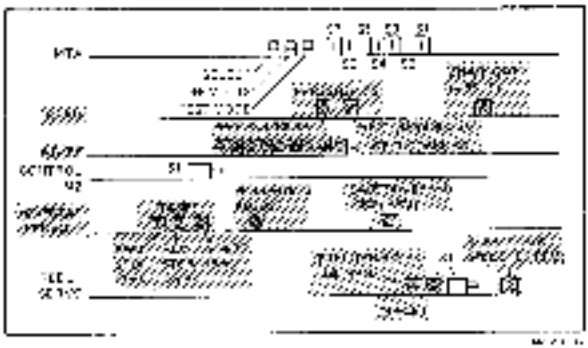

Figure 1-4 Maintenance Controls and Indicators

Table 1-3 M8940 MTA Indicators

ID Number	Function
DS1	Load/Ready
DS2	+5 V on
DS3	Unit select

Table 1-4 M8940 MTA Switches

Switch	Function Left	Right
S1	1600 BPI*	3200 BPI*
S2	Start/stop	Run continuous
S3	NRZI	PE
S4	Normal	Test
S5	Forward	Reverse
S6	R/W	Skip
S7	Write	Read

* Phase-encoded—write only.
† NRZI, all tapes.

Table 1-5 Center and Rear Seven Switches

Switch	Function Front	Center	Rear
Center SEVEN	Forward	Stop	Reverse
Rear Seven	Servo enable		Servo enable

1.3 RELATED DOCUMENTS

Table 1-6 lists and describes documentation related to the TU77 subsystem.

Table 1-1 Related Documents

Title	Document Number	Contents
TU77 Magnetic Tape Transport User Guide*	EK-OTU77-UG	Description, installation and operating procedures for the TU77.
TU77 Magnetic Tape Transport Technical Manual, Volume 1	EK-TU77-TM	Schematics and logic prints of the TU77.
TU77 Magnetic Tape Transport Technical Manual, Volume 2	EK-OTU77-TM	Description, installation, operation theory, and maintenance of the TU77.
TU77 Illustrated Parts Breakdown	EK-OTU77-IP	Exploded views and parts lists of the TU77.
TU77 Field Maintenance Print Set	MP00644	Engineering drawings and schematics of the TU77 cabinet, M8940, and the 8E power controller.
TMH3 Magnetic Tape Formatter User Guide*	EK-OTM03-UG	Description, installation, and programming of the TM03.
TM03 Tape Formatter Technical Manual	EK-OTM03-TM	Description, installation, theory of operation, and maintenance of the TM03.
TM03 Maintenance Print Set	MP00349	Engineering drawings, schematics, and logic prints of the TM03.
RH20 MASSBUS Controller Unit	EK-RH20-UG-001	Description of RH20 MASSBUS controller.
RH780 MASSBUS Adapter Technical Description	EK-RH78A-TD-001	Programming and theory of RH780 MASSBUS adapter.
RH750 MASSBUS Adapter Technical Description	EK-RH750-TD-001	Description of RH750 MASSBUS adapter (MBA) for VAX-11/750

* This document is shipped with TU77.

2 TROUBLESHOOTING

2.1 GENERAL

This chapter provides the following information for troubleshooting the TM03/TU77:

- TM03/TU77 diagnostic table listing tests for all relevant or applicable computer systems
- TM03/TU77 diagnostic procedures
- Illustration of M8940 MTA PCBA showing status indicators, switches, and test points
- Annotated timing diagram
- Tape failure diagrams
- Pneumatic system troubleshooting flow diagram

2.2 TM03/TU77 DIAGNOSTICS

Install a write-enable ring on a 2400 foot (10-1/2 in) reel of tape. Mount the reel onto the supply hub. Close the transport front door. Press the LOAD/REW button to load the tape. Press the ON LINE button and make sure the on-line indicator is on.

Table 2-1 lists the TM03/TU77 diagnostics for PDP-11, DECSYSTEM-20, and VAX-11/780 systems. Run the following diagnostics that apply to the system. Use the instructions in the diagnostics documentation and check for the results specified in Paragraphs 2.2.1 through 2.2.5.

2.2.1 Control Logic Test 1

Run control logic test 1 twice. No errors are allowed.

2.2.2 Control Logic Test 2

Run control logic test 2 twice. No errors are allowed.

2.2.3 Basic Function Test

Run the PDP-11 basic function test twice. No errors are allowed. Run DECSYSTEM-20 basic function tests B1 and B2 once. No errors are allowed.

Table 2-1   TM03/TU77 Diagnostics

Title	PDP-11	DECSYSTEM 10/20	VAX-11/780	Description
Control logic test 1	MAINDEC 11-DZTBA*	N/A	ZZ-EVMAC	Tests TM03 logic. Includes control logic maintenance modes.
Control logic test 2	MAINDEC 11-DZTBB*	N/A	ZZ-EVMAC	Tests TM03 logic. Includes control and data logic in maintenance mode.
Basic function test	MAINDEC 11-DZTBC*	MAINDEC 10-DFTUE†	N/A	Tests the subsystem command functions (read, write, space).
Drive function timer	MAINDEC 11-DZTBE*	N/A	ZZ-EVMAB	Tests for correct tape motion timing (speed, acceleration, deceleration) and data transfer rate.
Data reliability	MAINDEC 11-DZTBD*	MAINDEC 10-DFTUK*	ZZ-EVMAA	Tests TM03 and TU77 reliability by writing and reading user-determined or predetermined data patterns and recording media. Provides error information to the user via the console.

* Revision B or higher.
† Revision F or higher (2020) sub-forms DSTUA for DFTUE.

2.2.4 Drive Function Timer

Run the PDP-11 or VAX-11/780 drive function timer diagnostics twice. No soft or hard errors are allowed.

2.2.5 Data Reliability

2.2.5.1 PDP-11 System Using TU-DZ11-ELP*

1. Run the data reliability test once in NRZI mode with the following parameters.

   Density = 3
   Parity = 0
   Format = 14
   Record count = 1
   Character count = 20
   Pattern number = 1
   Tape mark = .
   Interchange read = 0
   Single pass = 1
   CRC correction = 0
   Stats
    Read = 1
    Write = 1
    Turnaround = 1

   Before typing the last carriage return (CR), set the console switches to 000020. Then type a carriage return to run the test. The following errors are allowed.

   0 hard errors (read or write)
   2 soft write errors
   2 soft read errors

*Revision D or higher.

2. Run the data reliability test once in PE mode with the following parameters.

   Density = 4
   Parity = 0
   Format = 14
   Record count = 1
   Character count = 20
   Pattern number = 1
   Tape mark = 1
   Interchange read = 0
   Single pass = 1
   Stalls
    Read = 1
    Write = 1
    Turnaround = 1

   Before typing the last carriage return, set the console switches to 000020. Then type a carriage return to run the test. The following errors are allowed.

   0 hard errors (read and write)
   4 soft write errors
   2 soft read errors

2.2.5.2 DECSYSTEM-20 Using 10-DFTUK*

1. Run NRZI test R8 once. The following errors are allowed.

   0 hard errors (read and write)
   3 soft write errors
   1 soft read errors

2. Run PE test R1 once. The following errors are allowed.

   0 hard errors (read and write)
   1 soft write errors
   1 soft read error

---

*Revision B or higher

3. Set left switches to 100010. Run the NRZI IW test once with the following parameters.

   Delay = 800
   Close skew window = <CR>
   Data compare mask = <CR>
   SYSERR recording = N
   Fast mode Y or N = Y
   Verify tapes = N

   The following errors are allowed.

   0 hard write errors
   1 soft write error

   Run the NRZI IR test once. The following errors are allowed.

   0 read errors (hard or soft)

4. With the left switches still set to 400010, run the PE IW test once with the following parameters.

   Density = <CR> or 1600
   Close skew window = <CR>
   Data compare mask = <CR>
   SYSERR recording = N
   Fast mode Y or N = Y
   Verify tapes = N

   The following errors are allowed.

   0 hard write errors
   1 soft write error

   Run the PE IR test once. The following errors are allowed.

   0 read errors (hard or soft)

2.2.6.3 VAX-11/780 System Using ZZ-FSMAA

1. Run the data reliability test exec in NRZI mode. Supply the requested information. The following errors are allowed.

   0 hard errors (read and write)
   2 soft write errors
   2 soft read errors

2. Run the data reliability test exec in PE mode. Supply the requested information. The following errors are allowed.

   0 hard errors (read and write)
   4 soft write errors
   2 soft read errors

2.3 MS940 MTA STATUS INDICATORS

Figure 2-1 shows the indicators, switches, and test points used for troubleshooting the MTA PCBA. Tables 2-2, 2-3, and 2-4 list their functions.

NOTES

1. Switches shown in Figure 2-1 are set to the right.

2. In test write mode, a tape must have a write-enable ring or else the write/erase heads disable.

3. All the MTA switches are dynamic. That is, the user can change densities, write frequency, start/stop, etc., whether or not tape is moving.

4. When creating a tape in test mode, return switch 7 to the read (right) position at end-of-tape (EOT). If you do not, a reverse/rewind to BOT overwrites the tape.

5. Set switch 4 to the normal (left) position before returning the transport to operating system on-line use.

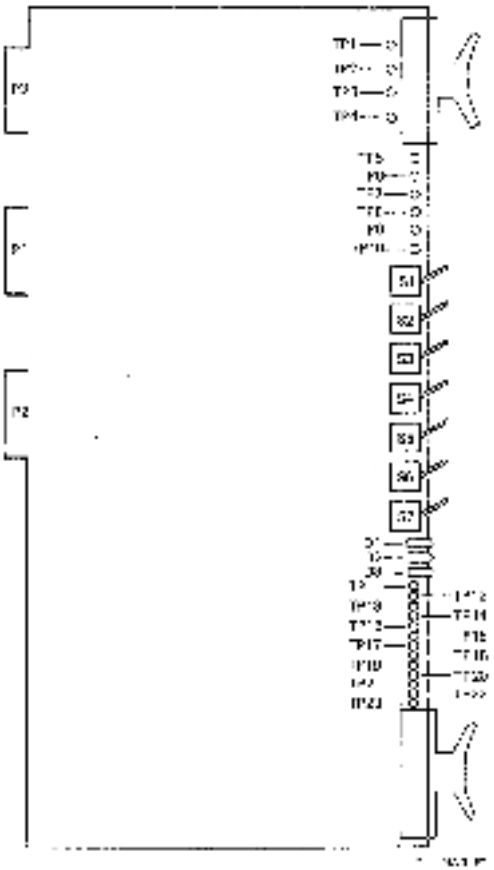

Figure 2-1 M8540 MTA Switches and Test Points

Table 2-2 M8940 MTA Test Points (Figure 2-1)

TP	Signal	TP	Signal
1	IRD0-H	13	IWD5
2	IRD1-H	14	IWD4
3	IRD2-H	15	IWD3
4	IRD3-H	16	IWD2
5	IRD4-H	17	IWD1
6	IRD5-H	18	IWD0
7	IRD6-H	19	IWDP-L
8	IRD7-H	20	IEPT-L
9	IRDP-H	21	IRWD L
10	IRDS-H	22	ILDP L
11	IWD7	23	TONL
12	IWD6		

Table 2-3 M8940 MTA Indicators (Figure 2-1)

D Number	Function
D1	Test mode
D2	+5 V on
D3	Unit select

Table 2-4 M8940 MTA Switches (Figure 2-1)

Switch	Function Left	Right
S1	1600 BPI*	3200 BPI
S2	Single step	Run continuous
S3	NRZI	PE
S4	Normal	Test
S5	Forward	Reverse
S6	Run	Stop
S7	Write	Read

* Phase-encoded write only.

2.4 LOAD FAULTS

When a load fault occurs, the load fault indicator on the control panel flashes. The fault can be in one of several possible areas. To determine the fault area and correct the problem, scope the test points on the control M2 PCBA. Table 2-5 lists the load fault numbers and test points. During a normal 'load' cycle the signal level at the test points remains high. Any test point that pulses low or goes low during the cycle indicates a load fault. Paragraph 2.5 has load fault flow diagrams.

Table 2-5 Load Fault Areas

Load Fault	Control M2 PCBA Test Point	Areas
0	TP24	No tachometer signal during cycle from take-up reel
1	TP27	Cartridge fault (one or several) is being closed or open
2	TP32	Cartridge fault (one or several) is being open
3	TP35	Air flow at capstan is [illegible] CFM
4	TP12	Two attempts (one to each reel) to load tape were not successful
5	TP11	Tape leader reject
6	TP39	Set loops fault

2.5 LOAD FAULT FLOW DIAGRAMS

Figures 2-2 through 2-5 show load faults 0 through 6.

NOTE:
Refer to Chapter 3 for test point (TP) locations.

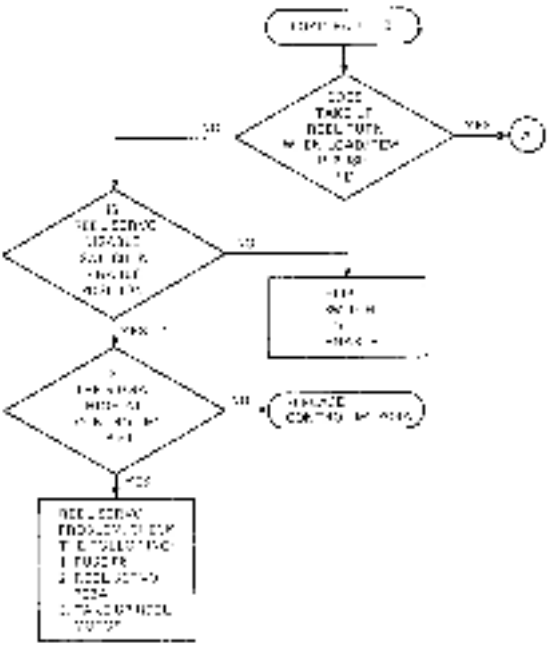

Figure 2-2 Load Fault Flow Diagram (1 of 2)

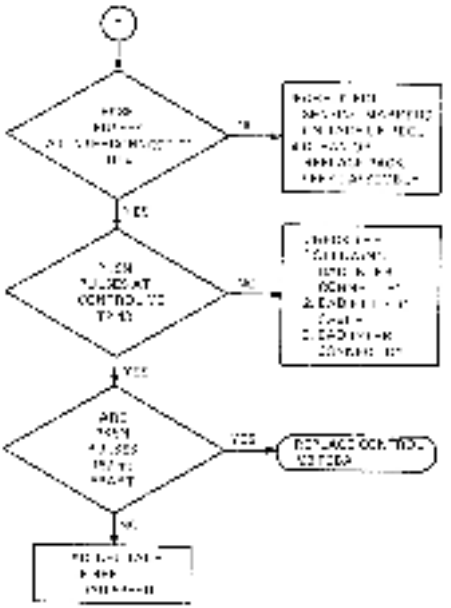

Figure 2-6 Lead Fault 0 Flow Diagram (2 of 2)

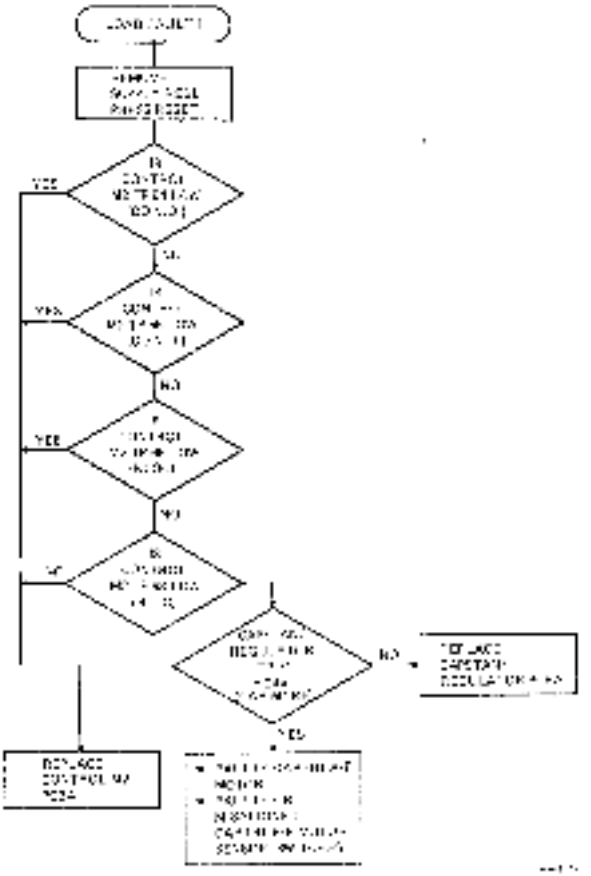

Fig. 3-4 Error Fault Flow Diagram

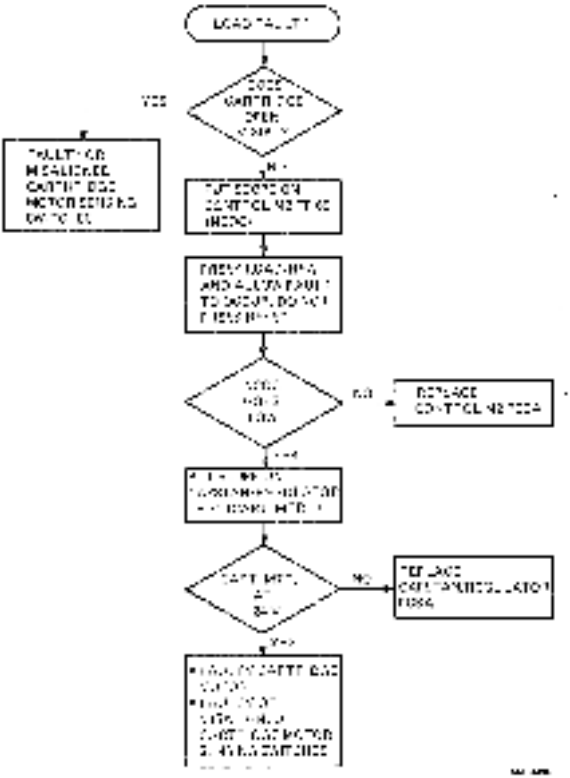

Fig. 2-4 Loss Fault Flow Diagram

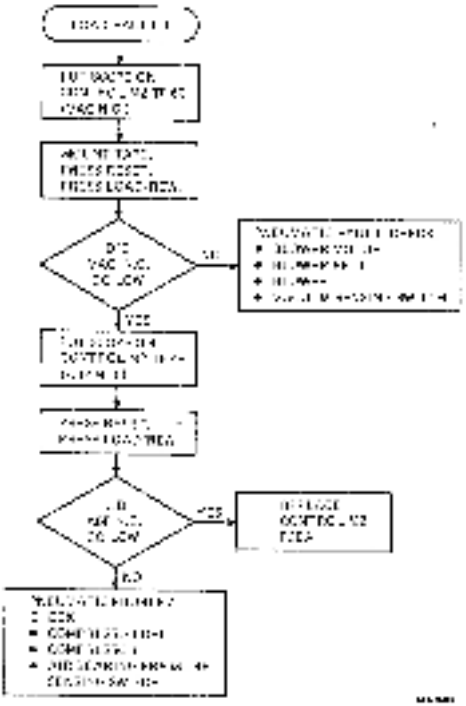

Figure 3-3 Load Fail 3 Flow Diagram

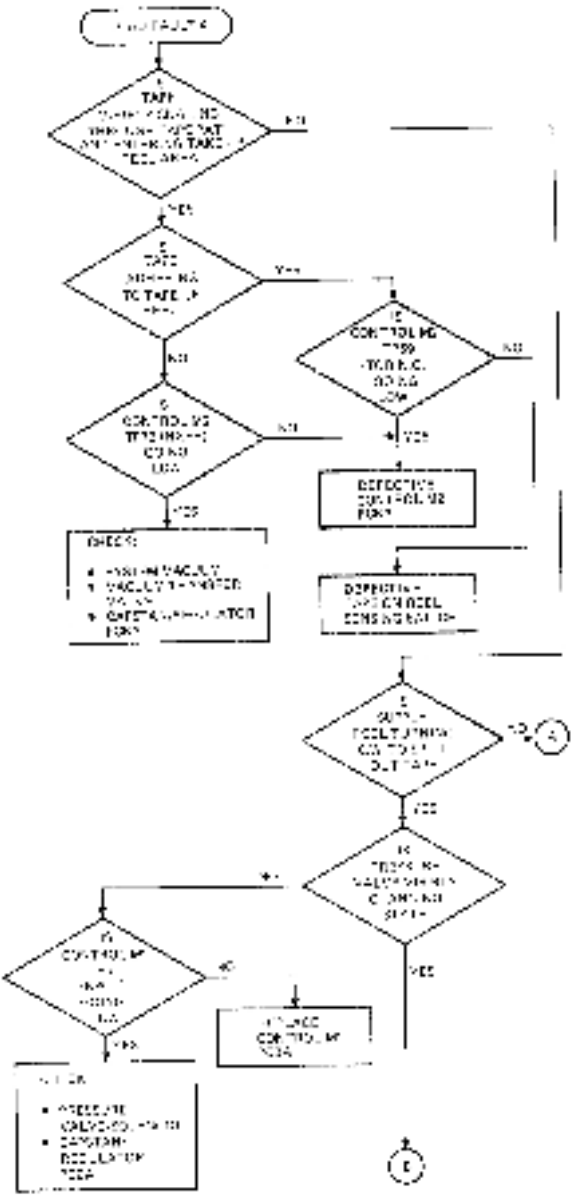

Figure 2-6 Error Fault 4 Flow Diagram (1 of 2)

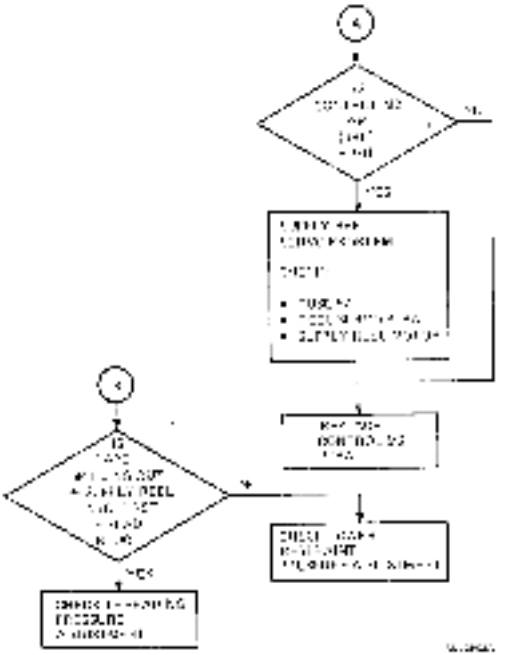

Fig. 2-7. Load Push-1 Flow Diagram 2 of 21

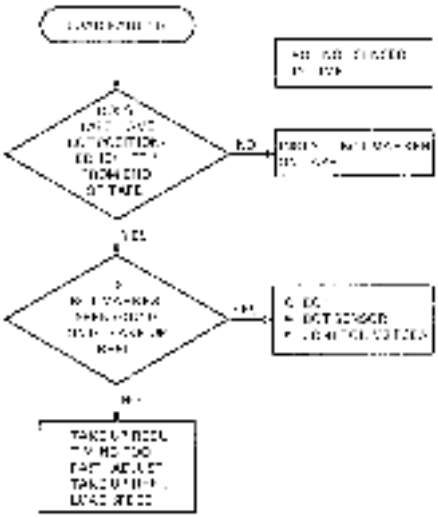

Figure 2-7 Copy Fault Flow Diagram

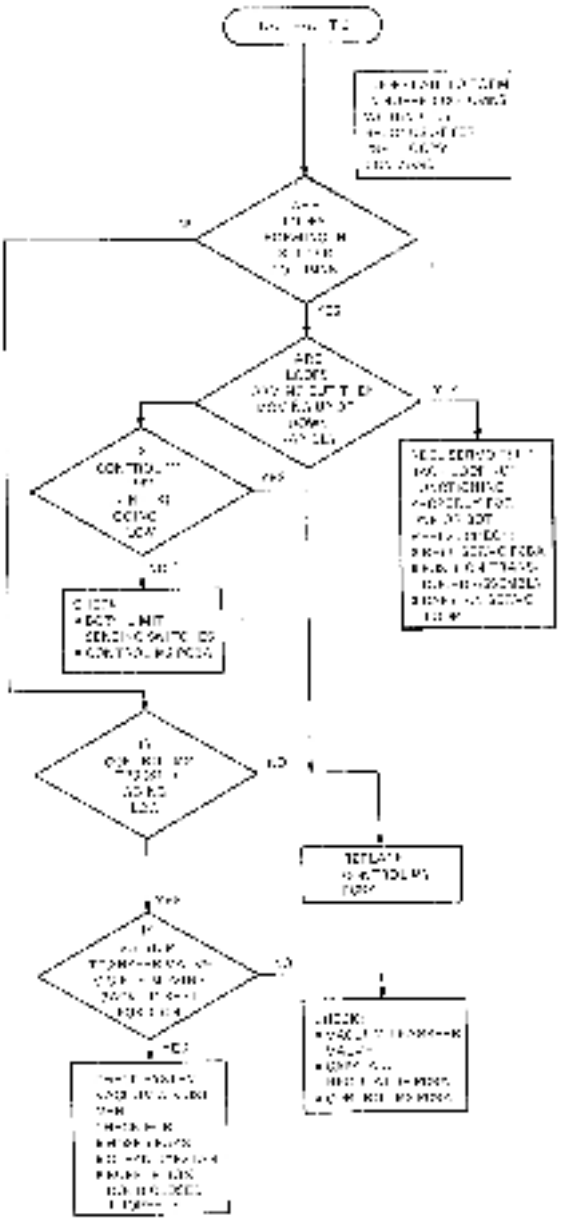

Figure 3-9 Error Fault 6 Flow Diagram

2.6 PNEUMATIC SYSTEM TROUBLESHOOTING

Figure 2-9 is a troubleshooting flow diagram of the pneumatic system.

NOTE
Refer to Chapter 3 for test point locations.

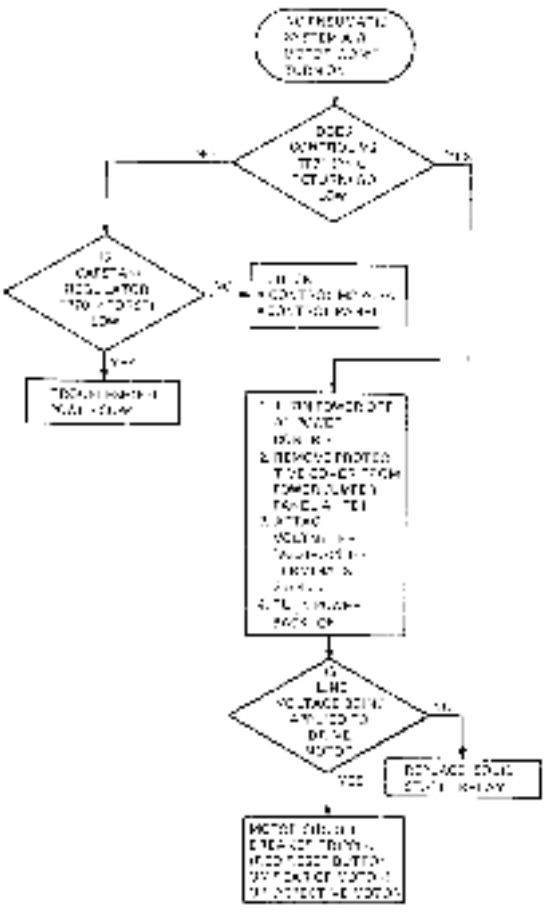

Figure 2-9 Pneumatic Troubleshooting Flow Diagram

3 CHECKS AND ADJUSTMENTS

3.1 GENERAL

This chapter provides adjustment and alignment procedures. They are grouped by function and include illustrations.

3.2 POWER DISTRIBUTION

Table 3-1 gives the power supply voltages for all the power in the IU77. Voltages can be measured at the appropriate fuses.

WARNING
Dangerous voltages are in the power supply.

Table 3-1 IU77 Power Supply Voltage Readings*

Fuse	Type	Circuit Function	Measured Voltage (dc) Minimum	Nominal	Maximum
F1	10 A FB	12 V	−13	13.5	13.5
F2	5 A FB	24 V	−23	24	126
F3	5 A FB	24 V	−23	24	−26
F4	20 A FD	36 V (3)	−45	37.5	+40
F5	20 A FD	36 V (3)	−45	37.5	−40
F6	20 A FD	36 V (7)	−45	40	+42
F7	20 A FD	−36 V (8)	−45	40	+42

* All measurements taken at power supply fuse block.

With a digital voltmeter (DVM), check all the regulated voltages at TP11, TP15, and TP18 with respect to TP1 (DC COM-2) on the capstan/regulator PCBA. Figure 3-1 shows locations of the test points and adjustments.

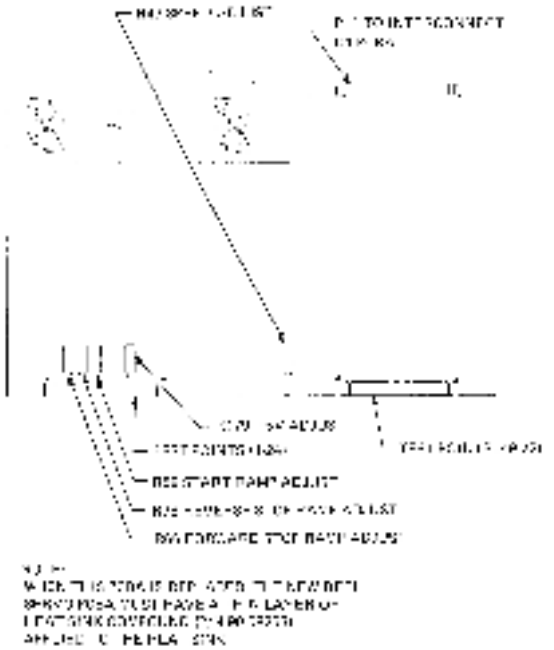

Fig. 3-1 Capstan/Regulator PCBA Adjustments and Test Points

TP11

−5 Vdc minimum −5.15 Vdc nominal −5.3 Vdc maximum	Adjust R1 (5.1 Vdc). Early TDD2 models do not have this potentiometer. Replace the capstan/regulator PCBA if the voltage is out of tolerance.

TP15

+14 Vdc minimum +15 Vdc nominal +16 Vdc maximum	The +5 Vdc is not adjustable. If voltage is out of tolerance, change the capstan/regulator PCBA.

TP18

−4 Vdc minimum −5 Vdc nominal −6 Vdc maximum	The −12 Vdc is not adjustable. If voltage is out of tolerance, change the capstan/regulator PCBA.

NOTE
When replacing the capstan/regulator PCBA, apply a thin layer of heat sink compound (PN 90-08268) to the heat sink mating surface.

3.3 BASE ASSEMBLY INTERCONNECT ADJUSTMENTS

Figure 3-2 shows the D base assembly interconnect PCBA. Figure 3-3 shows the three D variations of the base assembly interconnect PCBAs. An interconnect D PCBA can be replaced by an interconnect D1 PCBA with no modifications. After replacing a PCBA, make the following adjustments.

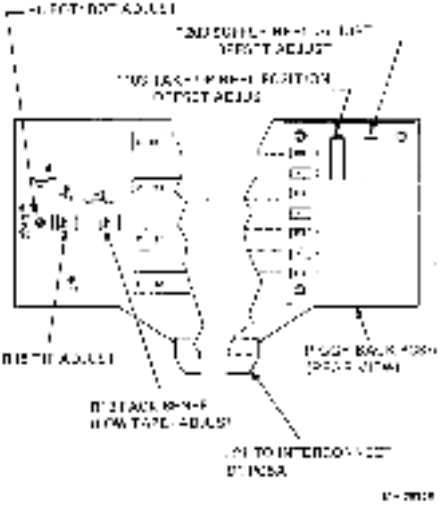

Figure 3-2 Interconnect P PCBA Adjustments and Test Points

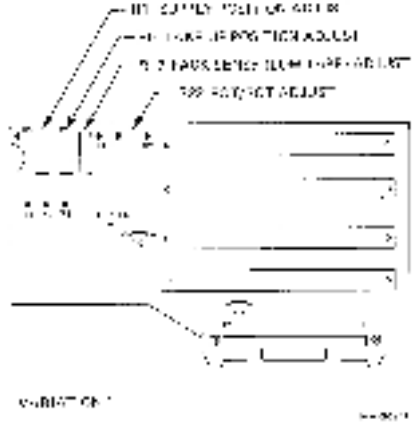

Figure 3-3 Interconnect P1 PCBA Adjustments and Test Points (1 of 2)

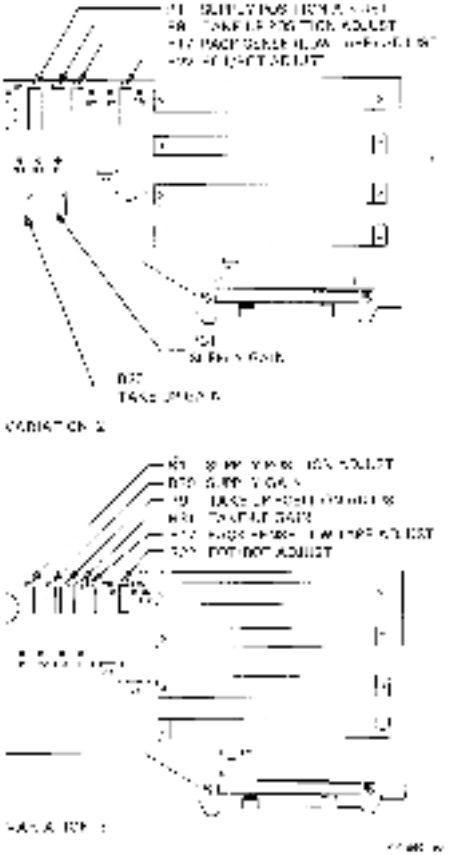

Figure 3-3 Interconnect PCB/A Adjustments and Test Points (2 of 2)

3.3.1 EOT/BOT Adjustment

Test equipment	DVM	
Test point	Interconnect T	(+) lead to TP6 (−) lead to TP5
	Interconnect T	(+) lead to TP1 (−) lead to TP3
Adjustment	R22 (interconnect T1) R5 (interconnect T)	
Criterion	0 V ± 0.1 V with tape in path but no BOT or EOT marker in front of sensor	

NOTE
The following measurement is taken with BOT and EOT markers under sensor.

− 2 V minimum at BOT
+ 2 V minimum at EOT

3.3.2 Tape-In-Path (TIP) Sensor (Interconnect F Only) Adjustment

NOTE
TIP is not adjustable on interconnect T1 PCBA.

Test equipment	DVM	
Test point	(+) lead to TP2 (−) lead to TP3	
Adjustment	R15 (interconnect T only)	
Criterion	≥ − 4 V with no tape in path ≤ − 0.5 V with tape in path	

3.3.3 Pack Sense Assembly (Low Tape Sensor) Adjustment

Test equipment	DVM	
Test point	Interconnect T	(–) lead to TP4 (+) lead to TP3
	Interconnect F	(+) lead to TP4 (–) lead to TP5
Adjustment	R17 (interconnect T) R15 (interconnect F)	
Criterion	≥ +0.3 V (reflective tab opposite sensor) ≤ −0.3 V (reflective tab away from sensor)	

NOTE
These levels should pulse twice for each revolution of take-up reel.

3.4 VACUUM AND AIR PRESSURE ADJUSTMENTS

3.4.1 System Vacuum Adjustment

Test equipment	0–40 in. water differential air gauge (low input) (PN 29-11650)
Test point	Crimp'd reel measure point (see Figure 3-4)
Setup	Load 10 1/2 in. tape to BOT. Set ST or control M2 PCBA to FWD (Figure 3-2)
Criterion	28 in. ± 1 in. water
Adjustment	1. Loosen butterfly valve lockout on vacuum valve (Figure 3-6, Item 1).
	2. Adjust screw (Item 2) if necessary.

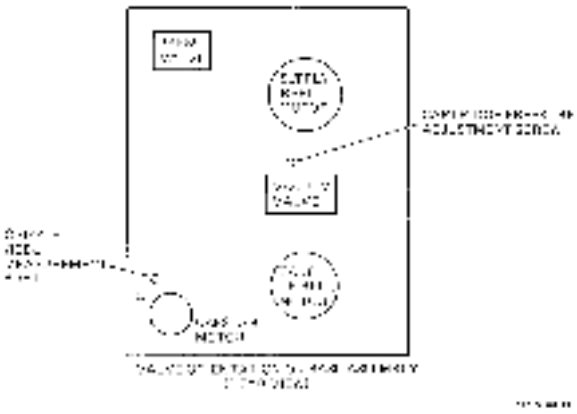

Figure 3-4 Valve Orientation on Base Assembly (Rear View)

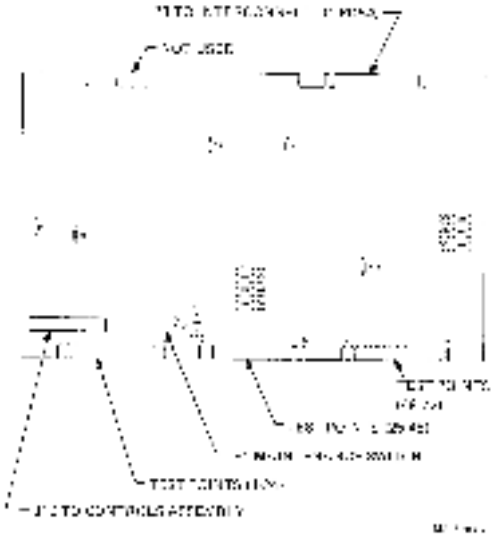

Figure 3-5 Control M2 PCBA Adjustments and Test Points

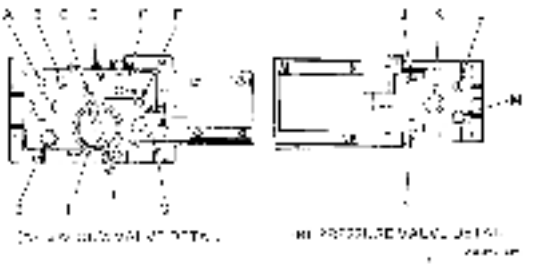

Figure 3-6 Vacuum Valve and Pressure Valve

3.4.2 Take-up Reel Vacuum Adjustment

Test equipment	0–40 in. water differential air gauge (low input) (PN 29-11652)
Test point	Take-up reel vacuum port on vacuum valve (Figure 3-6, item C)
Set up	1. Make sure there is no tape on supply reel. 2. Set reel servo disable switch (S1) on reel servo PCBA to rear (Figure 3-7). 3. Press and release LOAD/REW on control panel. 4. Rotate take-up reel three (3) turns only to deactivate load error 3 function.
Adjustment	Adjustment screw and sliding plate (Figure 3-6, Item D)
Criterion	10 in. = 1 in. water

NOTE
Do not leave pneumatic power on more than 3 minutes or vacuum transfer solenoid will overheat. Allow 9 minutes for cooling after performing this test.

If adjustment was performed, recheck system vacuum.

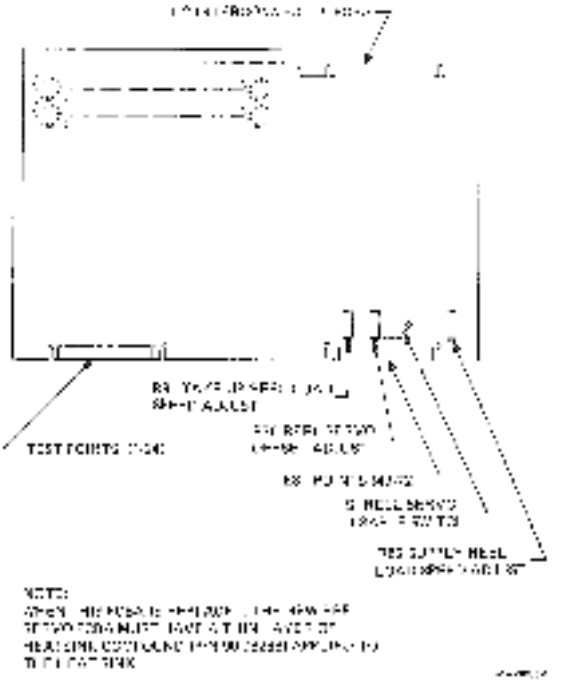

Figure 3-7 Read Servo PCBA Adjustments and Test Points

3.4.3 Air Bearing Pressure Adjustment

Test equipment	0 – 5 psi differential air gauge (high impar) (PN 39- 1636)
Test point	Air bearing pressure port (Figure 3-6, item N)
Setup	1. Load a 10- 12 in. mpc to SOL.
	2. Set S1 on control MI PCBA to FWD (Figure 3-5)

Adjustment — Loosen locknut and adjust screw (Figure 3-6, item J).

CAUTION
Threads on air bearing pressure adjust screw strip easily.

Criterion — 1.25 mil = 0.25 psi

3.4.4 Thread Block and Cartridge Pressure Adjustment

NOTE
The two thread block and cartridge pressure adjustments interact with each other.

3.4.4.1 Thread Block Pressure Adjustment

Test equipment — 0 – 40 in. water differential air gauge with input (PN 29-11650)

Test point — Thread block pressure port (Figure 3-6, item M)

Setup

1. Make sure there is no tape on supply reel.
2. Set reel servo disable sw. (S11) on reel servo PCBA toward rear (Figure 3-7).
3. Press and release LOAD/REW on control panel.
4. Rotate take-up reel to fully open and disable reel fault 10 and cause pressure solenoid to energize.

CAUTION
Do not allow solenoid to remain energized for more than 3 minutes. Allow 9 minutes to cool.

Adjustment	Thread block pressure adjust screw (Figure 3-6, item F)
Criterion	24 in. ± 2 in. water

NOTE
If an adjustment was made in the thread block pressure, check the cartridge pressure criterion below and readjust as necessary.

3.4-4.2 Cartridge Pressure Adjustment

Test equipment	0 – 40 in. water differential pressure gauge (low input)

NOTE
Use 0 – 5 in. gauge, if available.

Test point	Connect the differential pressure gauge to tube fitting as follows. On the front panel, remove socket head screw from cartridge pressure port in lower restraint and install tube fitting (PN 80-25228).
Setup	Use test setup as thread block setup (Paragraph 3.4-4.1).
Adjustment	Cartridge pressure adjustment screw (Figure 3-6)
Criterion	2.5 in. – 0.5 in. water without cartridge (approximately 5 – 15 in. water with cartridge)

NOTES
There may be air leaks in system if less than 9 in. pressure is observed on the gauge with a cartridge installed.

If an adjustment was made in the cartridge pressure, check thread block pressure criterion and readjust as necessary.

3.5 CAPSTAN SERVO ADJUSTMENTS

3.5.1 Capstan Speed Adjustment

Test equipment	Hand-held tachometer or scope
Test point	TP2 on connector M2 PCBA (CACH PULSE) (Figure 3-5) Work tape method or hand-held tachometer dial reading
Setup	1. Load work tape to BOT. Set FWD/REV/NORM switch (S1) on control M2 PCBA to FWD. 2. Place tip of tachometer cone into small dimple at rear of capstan (tachometer dial 1).
Adjustment	R47 on capstan regulator PCBA (Figure 3-6). Turn clockwise to increase speed, counterclockwise to decrease speed
Criteria	Period equals 80 μs ± 0.8 μs on scope or Tachometer reads 1500 rpm ± 24 rpm when held against dimple on rear of capstan motor shaft

3.5.2 Start/Stop Ramps (Forward) Adjustment

Test equipment	Scope
Test point	1. Place scope probe to TP501 on data L PCBA (Figure 3-8) 2. Set sync at external (+) on TP21 on control M2 PCBA (Figure 3-5) for forward start adjust. 3. Set sync at external (−) on TP21 for forward stop adjust
Setup	Load a NRZI GCR tape to BOT. Configure MTA switches to read forward in start/stop (Figure 3-11)

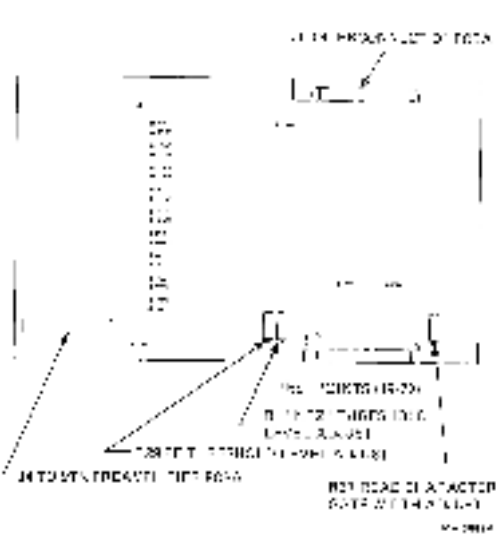

Figure 4-9 Data L PCBA Adjustments and Test Points

Adjustment

1. R59 on capstan/regulator PCBA for start ramp (Figure 4-10)
2. R66 on capstan/regulator PCBA for stop ramp

NOTE
Turn counterclockwise for decreasing time, clockwise for increasing.

Criterion

1. 3 ms ± 0.15 ms (start PWD) (Figure 4-9)
2. 3 ms ± 0.15 ms (stop PWD) (Figures 4-10 and 4-11)
3. Adjust for no overshoot on stop ramp (Figure 4-11).

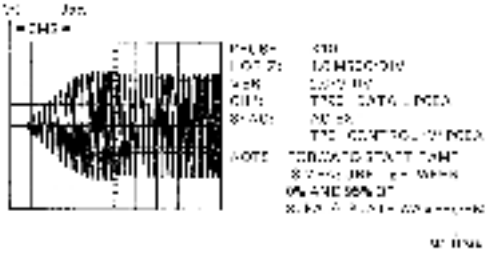

Figure 3-5 Forward Start Ramp

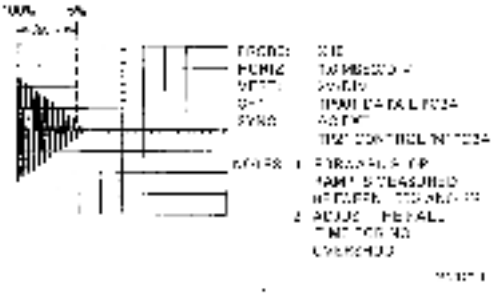

Figure 3-6 Forward Stop Ramp (Correct Waveform)

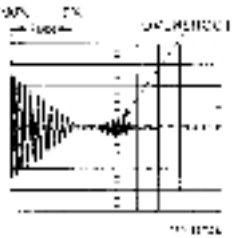

Figure 3-7 Forward Stop Ramp (Incorrect Waveform Showing Overshoot)

3.5.2.1 Stop Ramp (Reverse) Adjustment

Test point	Same as Paragraph 3.5.1
Setup	Same as Paragraph 3.5.1 except MTA configured for read reverse start/stop
Adjustment	R78 on capstan regulator PCBA (Figure 2-11)
Criterion	3 ms ± 0.15 ms Adjust for as specified (Figure 2-11). See Figure 3-10 for correct waveform.

NOTE
Reverse stop ramp should be slightly shorter than forward stop ramp (Figures 3-10 and 3-12).

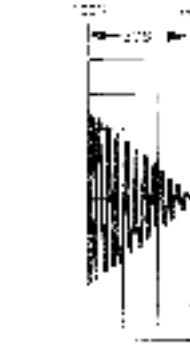

Figure 3-12 Reverse Stop Ramp

3.6 REEL SERVO ADJUSTMENTS

3.6.1 Reel Servo Offset Adjustment

Test equipment: None

Test point: None

Setup:

1. Turn power off.
2. Make sure there is no tape on supply reel.
3. Disconnect take-up reel motor leads at motor.
4. Turn power on.
5. Press LOAD/REW on front panel.
6. Turn take-up reel three (3) turns by hand to defeat load fault.

Adjustment: R76 on reel servo PCBA (Figure 3-[illegible])

Criterion: Adjust for no motion in the supply reel motor hub.

3.6.2 Supply Reel Load Speed Adjustment

Test equipment: Hand held tachometer (PN 29 [illegible] 1635) and two jumpers

NOTE
If a tachometer is not available, use the alternate method at end of test.

Test point: None

Setup:

1. Place tip of tachometer probe into small dimple at the end of supply reel motor shaft.
2. Use jumpers to connect reel servo TP62 (NAL) and TP69 (NSREL) to TP15 (GND) (Figure 3-[illegible]).

3. Make sure there is no tape on supply reel.

4. Supply reel hub should be turning counterclockwise.

Adjustment: R52 on reel servo PCBA (Figure 2-7)

Criteria: 95 rpm ± 5 rpm on tachometer

Alternate method: Use this method if tachometer is not available.

Mount a 10 1/2 in. tape and follow previous setup.

2. Mark reel with masking tape.

3. Measure time for 10 revolutions.

4. Time should be 10 to 12 s. Adjust R52 if necessary.

3.6.3 Take-up Reel Load Speed Adjustment

Test equipment: Hand-held tachometer (HP 29-01695) and two jumpers

NOTE
If a tachometer is not available, use the alternate method at end of test.

Test point	Notes
Servo	1. Place tip of tachometer cone into small triangle at rear of take-up reel servo motor shaft.
	2. Use jumpers to connect reel servo PCBA TP60 (XA15) and TP57 (NTRB) to TP59 (GND) (Figure 3-7).
	3. Take-up reel should be turning clockwise.
Adjustment	R51 on reel servo PCBA (Figure 3-7)

Criterion	150 rpm ± 15 rpm on tachometer
Alternate method	Use this method if tachometer is not available.
Test equipment	Scope and two jumpers
Test point	TP43 (low tape sensor) on control M2 PCBA (Figure 3-5)
Scope	Same as above
Adjustment	R41 on reel servo PCBA (Figure 3-7)
Criterion	167 ms ± 16.7 ms between leading edges of two consecutive pulses

3.6.4 Tape Loop Position Adjustment

NOTES
Check, and adjust if necessary, all vacuum and pressure readings outlined in Paragraph 3.5 before attempting to adjust the loop positions.

If the loop positions are so far out of adjustment that interlock (fail safe) is broken, proceed to step 1 and do the entire procedure. Otherwise, proceed to step 23.

1. Turn tape unit power off.
2. Set control M2 PCBA maintenance switch S1 to the center position (Figure 3-5).
3. Set reel servo disable switch S1 on the reel servo PCBA (Figure 3-7) toward the rear (disable).
4. Connect control M2 PCBA TP52 (NINTLK) and TP71 (PNL return) to TP25 (ground).
5. Disconnect one capstan motor lead.
6. Mount a DT 19-132 reel of tape without cartridge on the supply hub. Open the buffer box door and hand thread the leader through the tape path. Wind approximately 30 ft of tape on the take-up reel. Close the buffer box door.
7. Turn transport power back on. Vacuum and pressure comes on.

8. Manually rotate the supply reel clockwise to put tape into the supply buffer column. Rotate the reel so the tape forms a loop and the end of the loop is at the middle of the park zone. The park zone is the series of 13 small holes in the center of the buffer column (Figure 3-15). Hold the reel and apply masking tape to the outer flange and the transport to prevent the loop from being pulled down the buffer column by the vacuum.

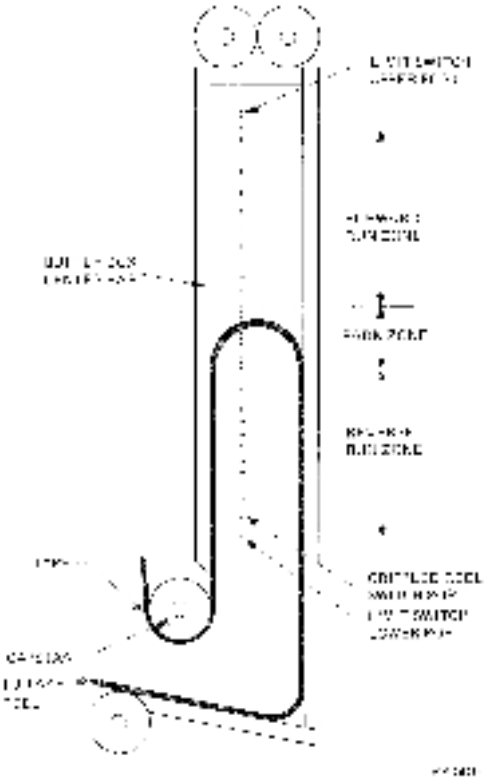

Figure 3-15. Buffer Column Park Zone
(Take-up Column Shown)

9. Hold the tape against an bearing 4 (Figure 3-14) with your finger and manually rotate the take-up reel counterclockwise to form a loop in the take-up buffer arm. Continue rotating the take-up reel until the loop is in the middle of the park zone and then tape the reel as in step 3. Release the tape at air bearing 4.

10. Check that both loops are in the middle of the park zone.

11. Press RESET on the control panel.

12. Connect a DVM to the test servo PCBA with the positive lead to TP53 (TP053) and negative lead to TP49 (ground).

13. Observe the DVM. The voltage displayed should be between +0.2 Vdc minimum and -0.2 Vdc maximum.

14. If the voltage is out of tolerance, adjust potentiometer R9 on the interconnect PCBA (Figure 3-2) or R103 on the interconnect PCBA (Figure 3-2).

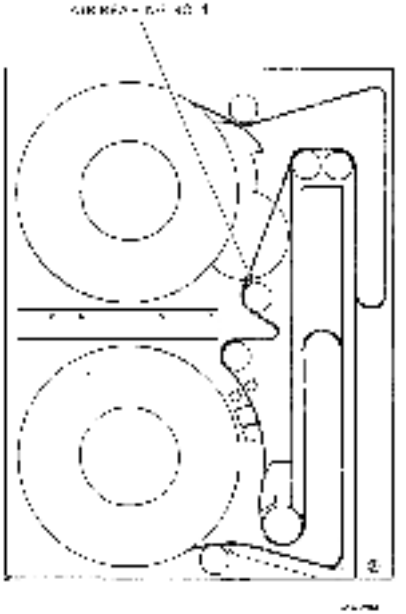

Figure 3-14 Base Assembly, Front Components

15. Connect the DVM positive lead to reel servo PCBA TP50 (SPOS).

16. Observe the DVM. The voltage displayed should be between +0.2 Vdc (minimum) and +0.7 Vdc (maximum).

17. If the voltage is out of tolerance, adjust potentiometer R1 on the interconnect P1 PCBA or R103 on the interconnect P PCBA for 0 Vdc.

NOTE

These voltages are produced on the base assembly by the respective pressure transducers. Therefore, during steps 12 through 17, the air measurements must be within specification and the loops must be in the middle of the park zones. (Refer to note under Paragraph 4.6.4.)

18. Put transport power off.

19. Remove ground wires from TP02 and TP71 on the control M2 PCBA.

20. Rotate the reel servo by setting reel servo PCBA switch S1 toward the front. Disable the front door interlock switch.

21. Reconnect the capstan motor lead.

22. Remove the masking tape from both reels and rotate one of the reels to take up slack.

23. Put transport power on and load a full 10 1/2 in. reel of tape. If the tape fails to load, refer to the reel servo troubleshooting procedures in Chapter 2.

24. Set gain potentiometers R30 and R21 on interconnect P1 PCBA (Figure 3-3, variations 2 and 3 only) fully clockwise. (The potentiometers have a range of approximately 28 turns.)

25. Adjust position potentiometers R1 and R9 on interconnect P1 PCBA and R203 and R105 on interconnect P PCBA so that both tape loops are within the park zones.

26. Move the tape approximately 30 ft from BOT by placing control M2 PCBA switch S7 toward the front of the transport for 3 s.

27. Ground control M2 PCBA TP21 to TP25 to initiate a forward/reverse shuttle.

28. Adjust the take-up position potentiometer R9 on the interconnect P1 PCBA or R103 on the P PCBA so the loop travel is equal above and below the take-up arm mark zone.

29. Remove the ground from control M2 PCBA TP31.

30. Record the new position of the tape loop in the take up column. You need this record in step 32.

31. Adjust take up gain potentiometer R31 on the interconnect P1 PCBA (variations 2 and 3 only) approximately 10 turns counterclockwise.

32. Adjust the take up position potentiometer R9 (interconnect P1) or R103 (interconnect P1 PCBA) so the take up loop park position is identical to that recorded in step 30.

33. Ground control M2 PCBA TP31 again to get a forward/reverse shuttle.

34. Fine tune the take up R9 and gain R31 (on interconnect P1 variations 2 and 3) potentiometers so the take-up loop matches the boundaries shown in Figure 3-17. The position potentiometer moves the loop excursion up and down in the window.

CAUTION
The gain potentiometer increases and decreases the length of the excursion. Rotating the gain potentiometer counterclockwise decreases the servo loop gain and allows a longer loop excursion. Rotating it clockwise increases the gain and allows a shorter loop excursion. Do not allow the take-up loop excursion to extend beyond 9-1/2 in.

NOTE
The gain and position potentiometers are interactive, so alternate adjustments in the fine tuning process.

35. Remove the ground from TP31 on the control M2 PCBA.

36. Set control M2 PCBA switch S1 toward the front of the transport and allow the tape to move to EOT. At EOT, set S1 to the rear for 3 s and allow the tape to move 30 ft from EOT.

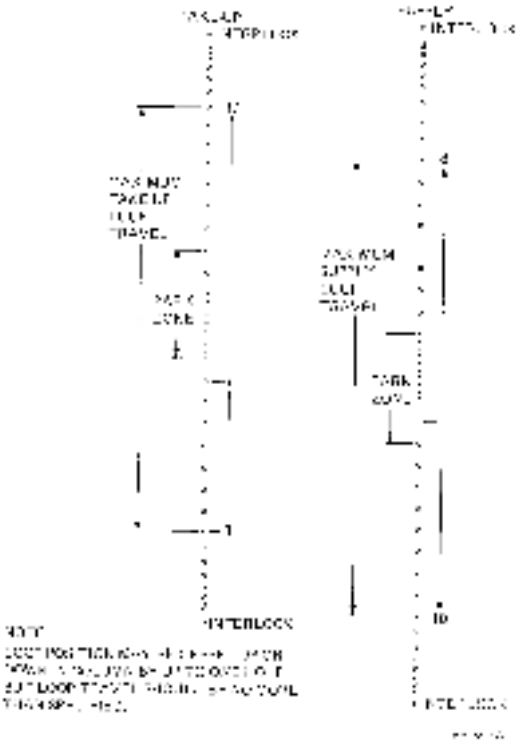

Figure 3-15 Loop Travel Limits

37. Repeat steps 27 through 35 for the supply reel servo loop position. Use position potentiometer R1 and gain potentiometer R30 on the interconnect PCBA (variations 2 and 3). Do not allow the supply loop excursion to extend beyond 10 in. in step 34.

38. When finished with the supply reel loop position, rewind the tape to BOT. Move the tape to EOT and rewind to BOT two more times. If interlock is broken, readjust the position and gain potentiometers until an optimum point is reached.

5.7 READ AND WRITE ADJUSTMENTS

NOTE:
Make sure tape path is clean.

5.7.1 NRZI Threshold Adjustment

Test equipment: DVM

Test point: (+) lead to data L PCBA TP67 (NRZP)
(−) lead to TP13 (GND) (Figure 5-8)

Setup:

Configure M8940 MTA PCBA switches as follows (Figure 2-1).

S3 left NRZI
S4 right test
S6 right stop
S7 right read

2. Mount and load a work tape to BOT. Place the transport on line.

Criterion: 1020 mV maximum
780 mV minimum

NOTE
If voltage is out of tolerance, adjust data L PCBA potentiometer R11 for a 900 mV reading.

5.7.2 NRZI Gain Adjustment

Test equipment: Scope

Test point: TP101 (channel P to TP901 (channel T) on data L PCBA (Figure 5-8)

Setup:

1. Write a 1's (NRZI) on a master output tape from BOT to EOT.

2. Rewind to BOT.

3. Set M8940 MTA PCBA switches for NRZI test (forward/continuous read (Figure 2-1, Table 2-4).

Adjustment R107 through R329 on the 9TK preamplifier PCBA (Figure 3-16 and Table 3-2)

Criterion 12 V p-p ± 1 V

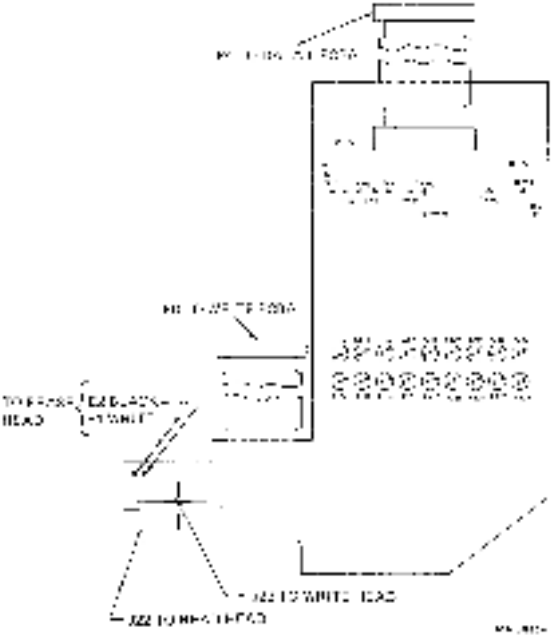

Figure 3-16 9TK Preamplifier PCBA Adjustments and Test Points

Table 3-3 NRZI Channel Test Points and Adjustments

Channel	Data I Test Point (Figure 2-81)	9TK Preamplifier Adjustment (Figure 3-17)	Nominal
P	TP10	R107	12 V p-p ± 1 V
0	TP20	R118	12 V p-p ± 1 V
1	TP30	R129	12 V p-p ± 1 V
2	TP40	R207	12 V p-p ± 1 V
3	TP50	R218	12 V p-p ± 1 V
4	TP60	R229	12 V p-p ± 1 V
5	TP70	R307	12 V p-p ± 1 V
6	TP80	R318	12 V p-p ± 1 V
7	TP90	R329	12 V p-p ± 1 V

3.7.3 NRZI Read/Write Skew Adjustments

3.7.3.1 NRZI Read Skew Adjustment

Test equipment	Scope
Test point	TP53 (packet pulse) data 1 PCBA (Figure 3-8)
Setup	1. Load a write-enabled master skew tape (PN 20-10234) to ROU. 2. Set M8040 MLA PCBA switches for NRZI test/read/forward/enable/disable as (Figure 2-, Table 2-4)
Adjustment	Adjusting screw accessible by removing small plug at buffer box door. Use a 1/8 in. allen wrench (Figure 3-17)
Criterion	Adjust for minimum packet pulse width of 1.2 µs minimum including jitter.
Setup	Set M8040 MLA PCBA switches for NRZI/Read/Forward/Disable/Disable.
Criterion	1.2 µs pulse

NOTE
If pulse width exceeds 1.2 µs, the capstan tracking may have to be fine tuned.

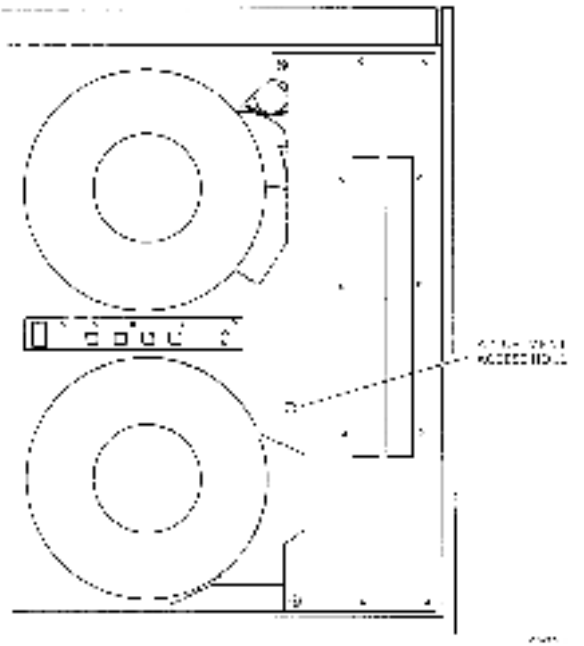

Figure 3-19 Location of NRZI Read Skew Assembly Adjustment

3.7.3.2 NRZI Character Gate Adjustment

Test equipment	Scope
Test point	1. Ch1 to data L TP51 (ANY-H) (Figure 2-8) 2. Ch2 to data L TP96 (TRIS) sync — on Ch1: DC
Setup	1. Load a write-protected master skew tape (PN 29-19234) to BOT 2. Set M89-0 MLA PBCA switches for forward/read/continuous/NRZI/test (Figure 2-1, Table 2-4)
Adjustment	R37 on data L PCBA
Criterion	Delay between leading edge of TP51 and positive going edge of TP96 is 4.85 µs ± 0.15 µs (Figure 3-18).

Figure 3-18 IRDS Delay Character Gate

3.7.3.3 NRZI Write Skew Adjustment

Test equipment Scope

Test point Data L TP53 (L SKEW) (Figure 3-9)

Setup
1. Load a master output tape (PN 29-11691) to BOT.
2. Set M8940 MTA PBCA switches for NRZI write/forward/continuous streaming

Adjustment While observing scope, adjust R801 through R801 on write PCBA (Figure 3-19). Turn clockwise until pulse width display increases. Then back off until it is the same as before. Adjust R901 for minimum pulse width.

Criteria 1.8 µs maximum

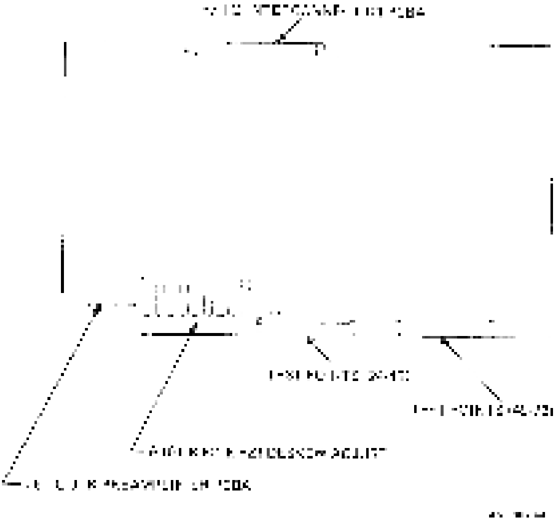

Figure 3-19 Write/Deskew PCBA Adjustments and Test P...

3.7.4 PE Read Threshold (Low) Adjustment

Test equipment: DVM

Test point: (+) lead to data L TP71 (Figure 3-8)
(−) lead to data L TP49 (GND)

Setup:
1. Load a master output tape (PN 29-116911) to BOT.
2. Set M889-0 MLA PCBA switches (Figure 2-1) for PE threshold/cold and place transport on-line.

Adjustment: R46 on data L PCBA

Criterion: 920 mV ± 60 mV

3.7.4.1 PE Data Adjustment

Test equipment: Scope

Test point: TP 01 through TP902, data L PCBA (Figure 3-8 and Table 3-3)

Table 3-3 PE Channel Test Points and Adjustments

Channel	Data L Test Point (Figure 3-8)	9TK Preamplifier Adjustment (Figure 3-17)	Nominal
P	TP102	R105	12 V p-p ± 1 V
0	TP202	R123	12 V p-p ± 1 V
1	TP302	R123	12 V p-p ± 1 V
2	TP402	R206	12 V p-p ± 1 V
3	TP502	R223	12 V p-p ± 1 V
4	TP602	R306	12 V p-p ± 1 V
5	TP702	R306	12 V p-p ± 1 V
6	TP802	R317	12 V p-p ± 1 V
7	TP902	R323	12 V p-p ± 1 V

Setup	1. Load master output tape (PN 20-12901) to BOT. 2. Set M8040 MTA PCBA switches for PE/active/forward/run/continuous/3200 FCI.
Adjustment	R106 through R129 on DTK preamplifier PCBA (Figure 3-16 and Table 3-2)
Criterion	12 V p-p ± 1 V

3.8 INTERCONNECT DT PCBA

The Interconnect DT PCBA (Figure 3-20) is the vertical board that interconnects the various logic boards in the card cage.

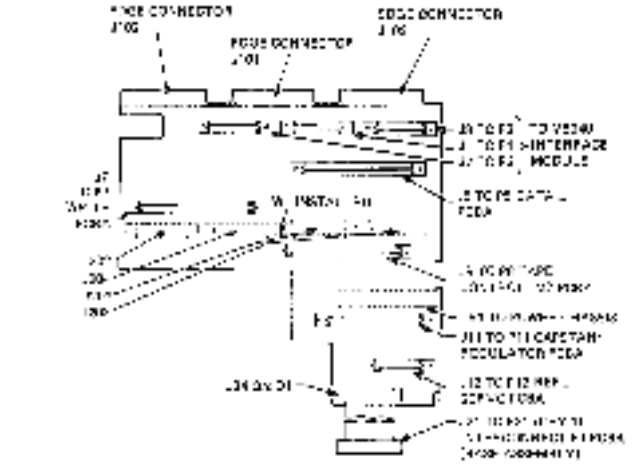

Figure 3-20 Interconnect DT PCBA (Front View)

4 TM03 REGISTERS

4.1 GENERAL

This chapter is divided into two sections. The first section is a quick reference with a figure and table of the TM03 registers. The second section is a detailed description of each register described in the first section.

4.2 QUICK REFERENCE

Figure 4-1 shows the TM03 register's format and bit functions. Table 4-1 summarizes descriptions of the registers listed in Figure 4-1. Table 4-2 also references the octal offset and UNIBUS address codes for the registers.

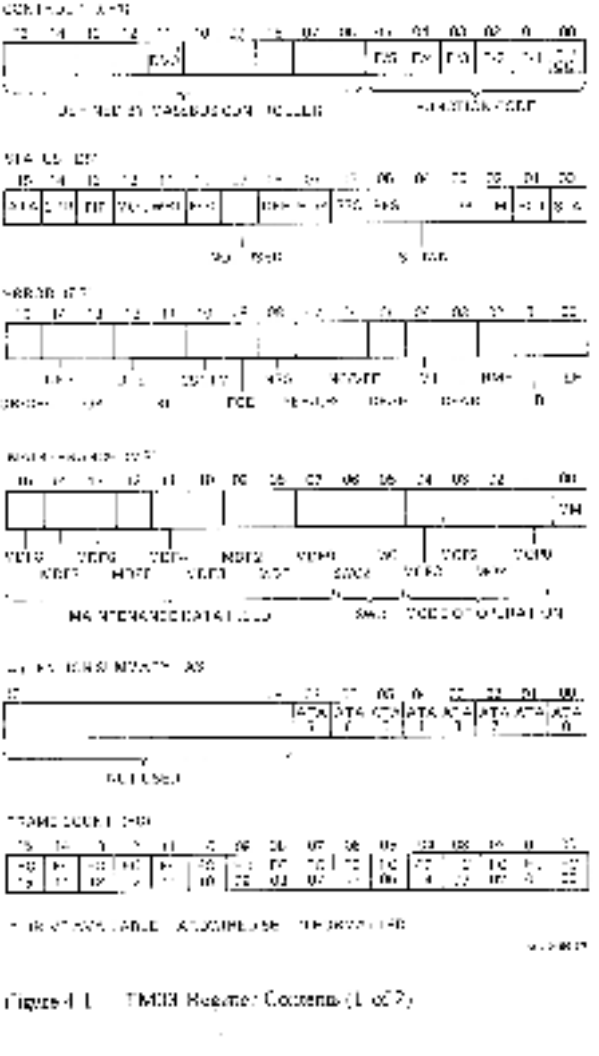

Figure 5-1 TMS3 Register Contents (1 of 2)

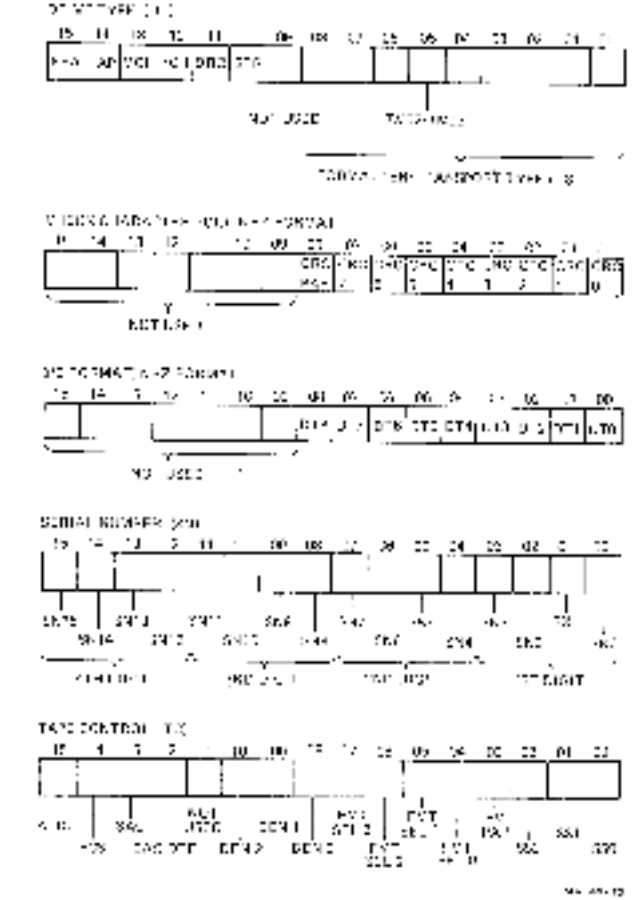

Figure 7-1. TMOD Register (Timer/Counter 0 and 1)

Table 4-1 TM03 Registers (Figure 4-1)

Address Codes				
Octal	VAX Offset	UNIBUS	Name	Description
00	0	772440	Control (CS1)	Read/write — Controls functions to be performed (GO bit)
01	4	772442	Status (DS)	Read only — Contains drive status information (6 bits are summary bits)
02	8	772444	Error (ER)	Read only — Contains error indicators
03	C	772446	Maintenance (MR)	Read/write — Controls diagnostic functions
04	10	772450	Attention summary (AS)	Read/write — Indicates attention active status of each TM03 formatter bit per TM03.
05	14	772452	Frame count (FC)	Read/write — For a write data transfer operation, contains 2's complement of number of frame characters to be transferred. For a space operation, contains 2's complement of number of records to be spaced. For a read data transfer operation, contains 2's complement of number of frame characters read.

Table 4-1 TM03 Registers (Cont)

Address Octal	Address VAX Offset	UNIBUS	Name	Description
06	18	772466	Drive type (DT)	Read only—Indicates type of formatter and type and status of transport (including formatter and transport with power applied).
07	1C	772450	Check character (CK)	Read only—For a NRZI operation, contains CRC error character. For a PE operation, contains dead track indications.
10	20	772470	Serial number (SN)	Read only—Contains last four digits of transport serial number.
11	24	772472	Tape control (TC)	Read/write—Controls transport selection and configuration modes.

4.3 DETAILED DESCRIPTION

This section contains the detailed description of each register in the TM03 formatter. Refer to Figure 4-1 for the register formats and Table 4-1 for register address codes.

4.3.1 Control Register (CS1)

The control register is a read/write register. It receives operational commands from the MASSBUS controller via the control bus. This register operates in conjunction with the drive control register to control the operation of the selected transport.

The control register is shared with the MASSBUS controller. Bits 00 through 05 are set by the TM03. The remaining nine bits are by the controller.

The TM03 transport responds to the 11 function codes listed in Table 4-2. If CS1 is loaded with a function code (with GO bit set) that does not agree with those listed in the table, an 'Illegal function error' (UFE) is generated.

Table 4-2 Control Register Command Functions

Code (bits 00 – 05) (octal)	Operation	Description
00	No operation	Performs no operation. Clears GO bit in control register.
03	Rewind off line*	1. Initiates a rewind command on selected transport (all phase transports if PS).
		2. Clears GO bit in control register.
		3. Sets drive ready (DRY), slave status change (SSC), and attention active (ATA) bits in status register.
07	Rewind	1. Initiates a rewind to BOT tape on selected transport and clears GO bit.
		2. Sets DRY, PIP, and ATA bits in status register during rewind.
		3. When BOT is sensed, sets SSC and clears PIP in status register.
11	Drive clear	Resets all TM03 and selected transport logic to power up initialize. Does not affect unselected transports.

* Requires manual intervention to return TU77 to on-line operation.

Table 4-2 Control Register Command Functions (Cont)

Code F(0 – 5) (octal)	Operation	Description
21	Read [illegible]	Presets tape control register (TCR) to select slave 0, odd parity, PDP-11 core dump format, and 800 bits/in NRZI. Can cause a write-protect error.
25	Erase	Erases approximately 3.0 in (3 in) of tape. Clears GO bit and sets ATA bit in status register.
27	Write tape mark	Writes a special tape record on selected transport. Clears GO and sets ATA bit. Termination in status register.
31	Space forward	Moves tape forward (toward EOT) on selected transport over number of records specified by frame count register. Aborts space operation if Tape mark (TM) or EOT is encountered before specified frame count. Clears GO bit and sets ATA bit in control register.
33	Space reverse	Moves tape in reverse (toward BOT) direction on selected transport over number of records specified by frame count register. Aborts space operation if TM or BOT is encountered before specified frame count. Clears GO bit and sets ATA bit in control register.
51	Write check (forward)	Same as read (forward)
55	Write check reverse	Same as read (reverse)
61	Write forward	Writes forward one tape record on selected transport. Record length is determined by frame count register. Clears GO bit on command termination.
71	Read forward	Reads forward one tape record on selected transport. Clears GO bit on command termination.
75	Read reverse	Reads reverse one tape record on selected transport. Clears GO bit on command termination.

4.3.2 Status Register (TMS)

The status register is a 16-bit, read-only register that stores the tape system status information. Table 4-3 defines each bit position. Although the status register multiplexer is in the TM03, inputs to this multiplexer can be generated either by a selected transport, or the TM03 logic itself. Therefore, each bit position in Table 4-3 is identified by one or more of the following designations. They indicate the origin of the input signal.

(SS) — selected transport
(S) — any transport
(M) — TM03 logic

Table 4-3 Status Register Bit Positions

Bit Position	Name	Description
00 (SS)	Slave attention (SLA)	Indicates that a selected transport has come on-line.
01 (SS)	Beginning of tape (BOT)	Indicates that a selected transport has detected BOT marker.
02 (M)	Tape mark (TM)	Indicates that a tape mark has been detected. Remains asserted until next tape motion is initiated.
03 (M)	Identification burst (IDB)	Indicates that a PE identification burst has been detected. Asserted until a subsequent tape motion command is initiated.
04 (SS)	Settle down (SDWN)	Indicates that tape motion on selected transport is stopping.
05 (SS)	Phase encoded status (PES)	Indicates that selected transport is configured for PE operation. Negated during NRZI operation.
06 (S)	Slave status change (SSC)	Indicates that any transport has just gone on-line or off-line, or has completed a rewind operation.
07 (M)	Drive ready (DRY)	Indicates that both TM03 and selected transport are ready to accept a command.
08 (M)	Drive present (DPR)	Hardwired set.
09	Not used	N/A

Table 4-3 Status Register Bit Positions (Cont)

Bit Position	Name	Description
10 (SS)	End of tape (EOT)	Indicates to the selected transport that a recorded EOT marker during forward tape motion. Is negated when EOT has been detected during reverse tape motion.
11 (SS)	Write lock (WRL)	Indicates that selected transport is write protected.
12 (SS)	Medium on line (MOL)	Indicates that selected transport has tape loaded and is on line.
13 (M/SS)	Positioning in progress (PIP)	Indicates that selected transport is performing a tape motion operation. This bit is asserted by TM03 (M) during a rewind operation and by the selected transport (SS) during a rewind.
14 (M)	Composite error (ERR)	Indicates that an error condition has occurred. Is asserted whenever any bit in error register is set.
15 (M)	Attention active (ERR)	Is asserted whenever ATTN interrupt signal is generated. Indicates one of the following conditions:
		1. TM03 and selected transport require servicing.
		2. TM03 and selected transport have become ready after a non-data transfer operation.
		3. A drive status change (SSC) has occurred.

4.3.3 Error Register (ER)

Sixteen different error conditions can be detected in the TM03/transport system (Table 4-4). The error register is a 16 bit, read only register that stores all of the tape system error indications.

TM03/transport errors are categorized as class A and class B. Class B errors terminate an in progress data transfer, but class A errors do not. The MASSBUS controller is notified of any errors during a data transfer by the immediate assertion of the exception (EXC) signal on the MASSBUS. If the TM03/transport is not performing an operation when an error occurs, or is performing a rewind (the GO bit is clear), the controller is immediately notified of an error condition by the assertion of ATTN on the MASSBUS.

Table 4-4 Error Register Bit Indicators

Bit Position	Name	Description	Error Class
00	Illegal function (ILF)	Indicates that an illegal function code has been transmitted.	D
01	Illegal register (ILR)	Indicates that a read or write from a nonexistent register was attempted.	A
02	Register modification refused (RMR)	Indicates that, during a transfer operation (GO = 1), a write into one of the registers was attempted.*	A
03	Control bus parity (CPAR)	Indicates that an incorrect control bus parity was detected.	A
04	Format (FMT)	Indicates that a transfer with an incorrect frame count is attempted. When MS/TS is fiddler stick, a FMT error can also indicate one of the following conditions:	B
		1. Microcode parity error	
		2. MS/TS data parity error	
		3. Illegal microcode instruction	

* This does not apply to write commands or functions [illegible]

Table 4-4 Error Register Bit Indicators (Cont)

Bit Position	Name	Description	Error Class
05	Data bus parity error (DPAR)	Indicates that an incorrect MASSBUS data bus parity error was detected	A
04	Inconsistent (bit) error or vertical parity error (INCA/VRE)	During a PE read operation, indicates that one of the following conditions 1. Multiple (two or more) dead tracks 2. Dead tracks without parity errors 3. Parity errors without dead tracks 4. Skew overflow 5. Parity error in bit locator During an NRZI read operation, indicates that a vertical parity error has occurred or that data has occurred after skew delay is over.	A
03	PE frame error or LRC error (PEF/LRC)	During a PE read operation, indicates that an incorrect preamble or postamble was detected During an NRZI write operation, indicates that LRCC read from the tape does not match LRCC constructed by the TM03 from the characters	A
02	Nonstandard gap (NSG)	Indicates that something was detected in the first half of each frame's gap while a write operation was in progress. Never sets during a read operation	A
01	Frame count error (FCE)	Indicates that a read operation has ended and frame counter is not clear. Also asserted when MASSBUS controller fails to negate RUN when TM03 asserts SPE.	A

Table 6-4 Error Register Bit Indications (Cont)

Bit Position	Name	Description	Error Class
10	Corrective Skew or Illegal Tape Mark (CS/ITM)	In Input Phase Configuration, indicates that excessive skew was detected. This condition is only a warning and does not indicate a data error. During an NRZI read operation, indicates that characters not legally a tape mark were read and recognized as a tape mark (but as record less than 18 characters minimum).	A
11	Nonexecutable function (NEF)	Indicates one of the following conditions: 1. A write operation was attempted with a write protected tape (WLK = 1). 2. A space reverse, read reverse, or write check reverse was attempted with tape at BOT. 3. The ID burst bit in tape unit status register does not agree with PES status bit in status register during a write operation. 4. A space or write operation was attempted when TCS = 0 in control register. 5. A write operation was attempted with DEN2 = 0 in tape control register (NRZI mode) and 2's complement of a number less than 18 is in frame count register. 6. The type of transport (tape unit TM8901 OR YC or YD) cannot agree with type of transport specified by drive type register. This indicates that TM03 and transport are not operating at same tape speed.	B

Table 4-4 Error Register Bit Indicators (Cont)

Bit Position	Name	Description	Error Class
12	Drive timing error (DTE)	Indicates one of the following conditions: 1. During a write operation, WCLK was not received from MASSBUS controller in time to present a valid tape character. 2. A data transfer (read/write) was attempted when MASSBUS data was not already accepted.	B
13	Operation incomplete (OPI)	Indicates that the end of record has not been detected within 7 s from command initiation during a read forward or space operation. Also set if BOT is detected during a read reverse or a space reverse.	B
14	Unsafe (UNS)	Indicates one of the following conditions: 1. A program controlled operation was attempted on a selected transport that is not on-line. 2. An imminent power failure was detected (AC LO).	D
15	Correctable data error or CRC (COR/CRC)	During a PE read operation, indicates that a single data track has occurred. During an NRZI operation, indicates that CRCC read off the tape does not match CRCC computed from the characters read off the tape	A

4.3.4 Maintenance Register (MR)

The maintenance register (M8025-YB) is a 16-bit, read/write register. This register allows user-level diagnostic testing of the TM03 data paths and error detection circuitry. The maintenance register can configure the data paths into five wraparound loops, each loop testing certain TM03 circuits. The maintenance register data field is part of these loops and is used to read or write test data into the TM03. Table 4-5 briefly describes each bit in the maintenance register.

Table 4-5 Maintenance Register Bit Positions

Bit Position	Name	Description
00	Maintenance mode (MM)	When set, configures TM03 to maintenance mode operation.
01 – 04	Maintenance operation code (MOP0 – 3)	Controls command execution during maintenance mode. MM and MOP function together to alter normal command execution during maintenance mode.
05	Maintenance clock (MC)	Controls data sequencing through TM03 data path in maintenance mode.
06	Tape speed clock (SWCK)	A clock signal generated by selected slave. Frequency depends on tape speed of selected slave. Used to monitor maintenance mode read operations.
07 – 15	Maintenance data bus (MD15 – 8)	8 Tape data generated during write/read operations. A serial/parallel NRZI transfers contains LRC of the record.

4.3.5 Attention Summary Register (AS)

The attention summary register (MSSUS:YAS) is a read/write pseudo register that consists of one to eight bits, depending on the number of drives (TM03s) on the MASSBUS. The term *pseudo register* refers to the fact that only one register bit position is physically in each TM03. This bit position reflects the state of the attention active (ATA) status bit for that TM03. Therefore, bit position 0 of the attention summary register is generated by the ATA bit of TM03 number 0; bit position 1 is generated by the ATA bit of TM03 number 1; and so on to bit 7. Bits 8 through 15 are unused.

Unlike the other TM03 registers, the attention summary register is directly selected by the controller without first addressing a particular TM03. Therefore, for a single attention summary register read operation, every TM03 in the system responds by placing the state of its ATA bit in the appropriate bit position on the control bus and disabling its remaining 15 control bus transmitters. This control bus configuration appears as a single register output that collectively informs the controller of all TM03s that require attention (ATA = 1). The controller can then selectively examine the error or status registers of each of the affected TM03s to determine the cause of the individual attention conditions.

The controller can also write into the attention summary register; however, the significance of the bits being written is unusual. Writing a 1 into a bit position resets the ATA bit in the TM03 assigned to that bit position; however, writing a 0 has no effect. This unique writing scheme allows the controller to reset, after interaction, all summary bits that were set, without accidentally resetting those bits that may have become set in the meantime. Table 4-6 shows the effects of writing into an attention summary bit position.

Table 4-5 Effects of Writing into Attention Summary Bit Position

ATA Bit Before	Summary Bit Written	ATA Bit After
0	0	0
1	0	1
0	1	0
1	1	0

4.3.6 Frame Count Register (FC)

The frame count register (MS709 XA) is a 16-bit, read/write register that counts tape frames. During a data transfer operation, this register is incremented each time a tape character is transferred to or from the tape. However, during a space operation, this register is incremented each time a record is detected. The register output may be read by the controller at any time, but the controller can only write into this register when the transport is not performing a space operation or data transfer (DRY negated). The three conditions are as follows:

4.3.6.1 **Write Operation** – For a write operation, the frame count register is loaded (before write GO is set) with the 2's complement of the number of tape characters to be written. During the writing process, the frame count register is incremented each time a tape character is received. Normal write data transfer terminates when the frame count register overflows to 0.

4.3.6.2 **Space Operation** – For a space operation, the frame count register functions similarly to a write operation except it is loaded with the 2's complement of the number of records to be spaced. The register is incremented each time a record is detected. The space operation terminates when the register overflows to 0 or a tape mark is sensed.

4.3.6.3 **Read Operation** – For a read operation, this register is automatically reset before read initiation. The register is then incremented each time a tape character is read. At the end of the read operation, the frame count register contains a count of the number of characters read.

4.3.7 Drive Type Register (DT)

The drive type register (MS793 only) is a 16-bit, read-only register. The register contents identifies the type of formatter, transport, plug, etc. When a read from this register is performed, the register contents is applied to the appropriate multiplexer bit positions. Bits 0 through 6 (DU – DT) of this register identify the type and status of the selected formatter and transport. If a nonexistent transport is selected or if the selected transport is not powered up, bits 0 through 6 will contain 0's. If no selected transport is powered up, the drive type code will be 08X, where X represents bits DPU, 2T1, and DT2 and indicates the type of slave. Bits DPU through DT8 are coded as shown in Table 4-7 for the TM03. Neither INIT nor drive clear can affect bits DPU through 2T8.

Table 4-8 describes each bit of the drive type register.

Table 4-7 Type and Status of Selected Formatter and Transport

Drive Type (DT) 8	7	6	5*	4	3	2	1	0	Selection
0	0	0	1	0	1	0	0	0	Unselected slave
0	0	0	1	0	1	0	0	1	114.3 cm per s (45 in/s), slave selected
0	0	0	1	0	1	0	1	0	190.5 cm per s (75 in/s), slave selected
0	0	0	1	0	1	1	0	0	317.5 cm per s (125 in/s), slave selected

* DT5 indicates the type of formatter being used.
DT5 = 0 = TM02
DT5 = 1 = TM03
(142054_8 = TM03/TU77 selected)

Table 4-8 Drive Type Register Bit Positions

Bit Position	Name	Description
00 – 08	Drive type (DT0 – 8)	Specifies type of formatter and transport.
09	N/A	Not used
10	Slave present (SPR)	Asserted when a transport is powered up and has been assigned selection code as specified in tape control register.
11	Drive request required (DRQ)	Always negated to indicate that device is a single port unit.
12	7-channel (7CH)	Always negated. The TM03 does not interface with 7-channel transports.
13	Moving head (MOH)	Always negated to indicate that the device is not a moving head unit.
14	Tape drive (TAP)	Always asserted to indicate that the device is a tape transport.
15	Not sector addressed (NSA)	Always asserted to indicate that the device is not sector addressable.

4.3.8 Check Character Register (CK)

The check character register (MBA03 Y01) is a 9-bit, read-only register that permits the programmer to check the validity of a data transfer. At the end of an NRZI read operation, this register contains the CRCC for that operation. Therefore, the programmer can determine if the CRCC generator logic is functioning correctly. At the end of a PE read operation, this register contains a dead track indicator (DT = 1) if any track that may have dropped one or more bits during the operation.

4.3.9 Serial Number Register (SN)

The serial number register is a 16-bit, read-only register. It contains a binary coded decimal (BCD) that represents the four least significant digits of the transport serial number.

4.3.10 Tape Control Register (TC)

The tape control register (MBA03 Y01) is a 16-bit read/write register that selects an existing transport and configures it for a particular operational mode.

Table 4-9 briefly describes each bit position.

Table 4-9 Tape Control Register Bit Descriptions

Bit Position	Name	Description
00 – 02	Slave control (SSU – 2)	Specifies unit number of transport to be used
03	Even parity (DEV PAR)	When set for NRZI operation, even parity is written or read from tape. Ignored during PE operation. (PE operations are always odd parity.)
04 – 07	Format select (FMT SEL0 – 3)	Specifies MASSBUS to tape character formatting during a write operation or tape character to MASSBUS formatting during a read operation. Format codes are as follows.* Refer to Chapter 5 for detailed explanations of data formats. 0000 PDP 10 format 10 core dump 0001 PDP 15 format 15 core dump 0011 PDP 10 format 10 extensible 1100 PDP 11 format 11 normal 1101 PDP 11 format 11 core dump 1110 PDP 15 format 15 normal 1111 PDP 11 format reserved

Table 4-9 Tape Control Register Bit Positions (Cont)

Bit Position	Name	Description
08–10	Density select (DEN0 – 2)[b]	Specifies tape character density during read or write operations as follows:
		DEN2 / DEN1 / DEN0 / Density (bits/in.):
		0 / 1 / 1 / 800 NRZI
		1 / 0 / 0 / 1600 PE
		1 / 0 / 1 / Reserved
		1 / 1 / 0 / Reserved
		1 / 1 / 1 / Reserved
11	Not used	N/A
12	Enable abort on data transfer errors (EABO DTE)	When set, immediately aborts a write or a read operation on one of the following errors:
		COR/CRC – error register bit 15
		PEF/LRC – error register bit 7
		INC/VPE – error register bit 6
		DPAR – error register bit 5
13	Slave address change (SACH)	Asserted whenever slave select bits of tape control register are changed. Negated on next drive set pulse.
14	Frame count status (FCS)	Is normally set at end of a write into frame count register. However, if FCS = 0, and a space or write command with GO = 1 is loaded, a nonexecutable function (NEF) error is generated and the command is not executed. Is reset when frame count register overflows.
15	Acceleration (ACCL)	This read only bit is asserted when transport is not actively reading or writing data.

[a] Codes 0000 and 0011 select an MS815 data formatting module. This is used by 36-bit processors.

Codes 1100 and 1101 select an MS8505 data formatting module. This is used by PDP-11 and VAX processors.

All other format codes are invalid. An invalid code causes a format error (FMT = error register bit 4) when a data transfer command with GO = 1 is loaded.

[b] DEN2 bit selects 800 and 1600 bits/in. DEN1 and DEN0 bits are not used. DEN codes 5[illegible], 6[illegible], and 7[illegible] are reserved for future use.

5 DATA FORMATS

5.1 GENERAL

This chapter illustrates how the TM03 maps MASSBUS transfers onto tape during write operations and how tape characters are mapped onto the MASSBUS data lines during read operations. It defines PDP-10 and PDP-11 processor bits and shows bit locations during a MASSBUS transfer. This chapter also shows the packing/unpack format of the processor words into tape frames for the various formatting modes.

5.2 MASSBUS/TM03 TRANSFERS

Consider a single record that is read from or written on tape. Assume four MASSBUS transfers occur during the writing (reading) of this record and that the contents of the first transfer is 11111_8, the contents of the second transfer is 22222_8, the third 33333_8, and the fourth 44444_8. If the write (or read) is in a forward direction, the four MASSBUS/TM03 transfers are as follows.

11111_8 – first transfer
22222_8 – second transfer
33333_8 – third transfer
44444_8 – fourth transfer

If the read is in a reverse direction, the four MASSBUS/TM03 transfers are as follows.

44444_8 – first transfer
33333_8 – second transfer
22222_8 – third transfer
11111_8 – fourth transfer

Words transferred between memory and the TM03 are formatted on the MASSBUS according to the processor used. Two transfers are required to transmit a 36-bit PDP-10 word while only a single transfer is required for a 16-bit PDP-11 word. The word formats on the MASSBUS for the PDP-10 and PDP-11 are shown in Tables 5-1 and 5-2. The 18 data lines on the MASSBUS are designated D0 through D17.

Table 5-1 PDP-10 MASSBUS Word Format

D17 – D0	MASSBUS Data Lines
B0 (MSB) – B17	First MASSBUS transfer*
B18 – B35 (LSB)	Second MASSBUS transfer*

* In read reverse, the order of MASSBUS transfers are reversed; that is, B18 through B35 is sent first and B0 through B17 is sent second.

Table 5-2 PDP-11 MASSBUS Word Format

D15 – D00*	MASSBUS Data Lines
B15 (MSB) – B0 (LSB)	MASSBUS transfer

* D17 and D16 are not used.

5.3 TM03/TAPE FRAME PACKING AND UNPACKING

5.3.1 Frame Packing

In a write operation, the processor data stored in the TM03 is disassembled and packed onto tape in a number of tape characters or frames. The number of frames depends on the processor used and the mode of operation.

5.3.2 Frame Unpacking

In a read operation, the tape frames are read off tape (unpacked) and assembled into a data word for MASSBUS transfer.

5.3.3 Packing/Unpacking Formats

Tables 5-3 through 5-6 show the packing/unpacking formats for the PDP-10 and PDP-11 processors in various format modes. During a read reverse operation, the frames are read off tape in reverse order.

NOTE
To any given transfer, the frame count register must contain the 2's complement of the number of frames required to transfer complete processor words to or from tape. For example, in the PDP-10 core dump mode (Table 5-4), it takes five tape frames to read or write a word on tape. The frame count register must be loaded with the 2's complement of 5 times the number of words read or written.

25-word transfer: $25 \times 5 = 125$ frames
26-word transfer: $26 \times 5 = 130$ frames
27-word transfer: $27 \times 5 = 135$ frames

Table 5-3 PDP-10 Compatibility Mode – Format Code 0011

Tape Frames	Tape Track Positions								
	TP	T7*	T6	T5	T4	T3	T2	T1	T0†
1	P	B0	B1	B2	B3	B4	B5	B6	B7
2	P	B8	B9	B10	B11	B12	B13	B14	B15
3	P	B16	B17	B18	B19	B20	B21	B22	B23
4	P	B24	B25	B26	B27	B28	B29	B30	B31

* MSB
† LSB

Table 5-4 PDP-10 Core Dump Mode – Format Code 0000

Tape Frames	Tape Track Positions								
	TP	T7*	T6	T5	T4	T3	T2	T1	T0†
1	P	B0	B1	B2	B3	B4	B5	B6	B7
2	P	B8	B9	B10	B11	B12	B13	B14	B15
3	P	B16	B17	B18	B19	B20	B21	B22	B23
4	P	B24	B25	B26	B27	B28	B29	B30	B31
5	P	0	0	0	0	B32	B33	B34	B35

* MSB
† LSB

Table 5-5 PDP-11 Normal Mode – Format Code 1100

Tape Frames	Tape Track Positions TP	T7*	T6	T5	T4	T3	T2	T1	T0†
1	P	R7	R6	R5	R4	R3	R2	R1	R0
2	P	R15	R14	R13	R12	R11	R10	R9	R8

* MSB
† LSB

Table 5-6 PDP-11 Core Dump Mode – Format Code 1101

Tape Frames	Tape Track Positions TP	T7	T6	T5	T4	T3*	T2	T1	T0†
1	P	–				R7	R6	R5	R4
2	P					R3	R2	R1	R0
3	P					R11	R10	R9	R8
4	P					R15	R14	R13	R12

* MSB
† LSB

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