

MODEL F1B and MODEL F4

PDP-10 COMPATIBLE SYSTEMS

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PHYLOGENY OF THE PDP10

at DEC

PDP-6
DISCRETE COMPONENTS
.25 MIPS

↓
KA10
DISCRETE COMPONENTS
.5 MIPS

↓
KI10
TTL IC'S
.8 MIPS

↓
KS10
800 TTL IC'S
.4 MIPS

↓
KL10 (A.K.A. 2060, 1060, ETC.)
4,000 ECL IC'S
1.5 MIPS
.5 MFLOPS

↓
DOLPHIN
BORN DEAD

↓
JUPITER
BORN DEAD

THE S1 IS NOT PDP10
COMPATIBLE, ALTHOUGH
ITS ARCHITECTURE
SHOWS MUCH PDP10
INFLUENCE.

↓
S1, MARK I (1980)
8,000 ECL IC'S
6 MIPS

↓
S1, MARK IIA (1984)
27,000 ECL IC'S
10 MIPS
20 MFLOPS

↓
• IMPROVED CONSTRUCTION METHODS
• IMPROVED SUDS ("SCALD")

↓
F1B
6,000 ECL IC'S
6 MIPS
2.5 MFLOPS

at STANFORD

SUPERFOONLY (DESIGNED 1968-71)
10,000 TTL IC'S
3 MIPS
"SUDS" CAD/CAM System

at FOONLY, INC.

↓
F1 (1978)
5,000 ECL IC'S
3.5 MIPS
.7 MFLOPS

↓
F2/3 (1979)
1,200 TTL IC'S
.5 MIPS

↓
F4 (1981)
2,000 TTL IC'S
1 MIPS

THE F1B IS NOT
A NEW DESIGN,
BUT A MODIFI-
CATION OF THE F1A.

at XEROX

MAXC
MAXC II

• "MBOX" DESIGN
• CONSULTATION
• SUDS

the LIVERMORE
CONNECTION

• CONSTRUCTION METHODS
• CONSULTATION
• SUDS

Characteristics of Foonly Models F1B and F4 Systems

Compatibility

Digital Equipment's TOPS20 and TOPS10 operating systems both supported, with complete Digital model KL10 instruction set.

Performance

Model F1B: About four times that of the KL10. See "Comparison of Characteristics of KL10, F4, and F1B" for details. Cycle time is 80ns; one cycle is needed for MOVEI or ADD A,B; two cycles for ADD A, MEM and for jumps, including PUSHJ; three cycles for ILDB or POPJ. A dedicated floating-point unit performs double precision floating multiply in 5 cycles.

Model F4: About 2/3 performance of KL.

Physical Size

Model F1b: 30" x 90" x 72" high

Model F4: 24" x 30" x 72" high

Power Needed

Model F1b: 5 KW

Model F4: 1.5 KW

Design Features

Model F1B: Cache size is 8k words, and the pager Translation Buffer is also 8k. The cache operates in one cycle; only 3 additional cycles are needed for misses. Main memory size is up to 32MW. The unique debugging features include several 1k History Memories, extensive Console Computer access to the logic, and various Hardware Breakpoints. Total I/O bandwidth is 5MW per second. Logic is 6000 ECL 10K packages.

Model F4: No cache; 4k Translation Buffer; main memory to 4MW. Console Computer, history memories, hardware breakpoints. Logic is 2000 TTL series packages.

I/O

All Foonly systems perform input/output via our standard FBUS. Foonly currently manufactures an extensive standard line of FBUS i/o controllers. Custom interfaces can be provided.

- DISK -- 300MB removable media, 450MB fixed media (SMD interface)
- TAPE -- 6250BPI, 40 - 120 IPS ("Pertec" standard OEM interface is used, but we do NOT use Pertec drives).
- SERIAL LINES -- programmable, 300 - 19,000 bd
- LINE PRINTERS -- ("Data Products" standard OEM interface)
- ELECTROSTATIC PLOTTERS -- Varian/Versatec
- ETHERNET (10MB)
- ARPANET
- TYMNET (actually a PDP-11 interface (DR-11C))
- COLOR BIT-MAP DISPLAY (Foovision)

Maintenance

Foonly's remote maintenance system allows all bugs and problems, in both hardware and system software, to be dealt with by top level wizards at the factory (see "Instant Expert Service", below). This is possible only because of the unique capabilities of our maintenance support hardware.

The Console Computer (CC) is the central element of the maintenance hardware. It is a 68000-based system (6502-based on F4) which uses a display terminal to present in dynamically updated information.

- CC controls power, senses voltages and temperatures, and can adjust clock speed and skew delays.
- CC can load and examine registers, memories, and data paths.

- CC can test for cables being plugged in correctly. One wire in each signal cable is devoted to this function.
- CC controls the logic analyzer. In conjunction with the CCTALK program on the support system (see description under "Maintenance"), this greatly improves the utility and ease of operation of this excellent tool. Condition setups can be stored and edited, and displays of data are more flexible, have symbolic labels, and can be stored.
- History Memories record the last 1k machine cycles. Items recorded included macro and micro PCs, MBOX addresses, and dozens of signals indicating the type of operation performed and the result (eg, Instruction Fetch with Cache Hit) by each of the functional units of the machine.
- Hardware Breakpoints are available for macro and micro addresses.
- The system can be single stepped; functional units can be separately disabled, and certain major functions can be disabled to simplify machine operation. For example, the cache can be turned off. Also, the overall pipelining can be inhibited, so that only one functional unit at a time is operating; this not only helps isolate bugs in the (rather complex) pipeline control logic, but also often allows the machine to keep running in the presence of bugs.

Comparison of Characteristics of KL10, F4, and F1B

Below is a summary comparison of the main factors determining the performance of three software compatible processors: the Digital Equipment Corp. model KL10/20, the Foonly model F4, and the Foonly model F1B. The instruction timings shown are among the most important for general applications.

Our estimate, based on the facts given below, is that the model F4 performs at about 2/3 the level of the KL (but less on Floating Point), and the model F1B at about 4 times the level of the KL (more on Floating Point).

	KL	F4	F1B
Virtual Address Size	23 bit	30 bit	30 bit
Maximum Physical Memory	4MW	8MW	32MW
Cache:			
Size	2K	NONE	8K
Access Time	.133	--	.08
Nominal Miss Rate	10%	0	5%
Time Lost on Miss	.8	--	.24
Address Translation Buffer:			
Size	512	4K	8K
Average Refill Time	7usec	20usec	7usec
Translation Overhead Coefficient (= (Refill-Time/SQRT(Buffer-size)))			
	0.3	0.3	0.06
Power Requirement (CPU)	8 KW	1.5 KW	5 KW
Floor Space Needed (CPU)		6 sq. ft.	24 sq. ft.

INSTRUCTION TIMINGS

The column headed "KL (NO MISSES)" comes from DEC's standard instruction timing program (running in Section 0 on a 2060). Corrections for cache misses, calculated from parameters given on the preceding page for each machine's cache performance, have been included in all other timings.

	KL (NO MISSES)	KL (WITH MISSES)	F4	F4/KL	F1B (WITH MISSES)	F1B/KL
ILDB	1.405	1.645	2.5	66%	.316	521%
IDPB	1.707	1.947	2.8	69%	.316	616%
MOVE	.401	.561	.650	86%	.184	305%
MOVEI	.266	.346	.375	92%	.092	376%
MOVEM	.567	.727	.550	132%	.144	505%
JRST	.300	.380	.375	101%	.114	333%
PUSHJ	.703	.863	1.425	61%	.212	407%
PUSH	.735	.975	1.100	89%	.224	435%
POP	.869	1.109	1.250	89%	.224	495%
POPJ	.637	.797	1.125	71%	.264	302%
AOBJN	.432	.512	.375	137%	.168	305%
JUMPE	.401	.481	.563	86%	.128	376%
ADD	.434	.594	.650	91%	.184	323%
ADDI	.301	.381	.375	102%	.092	414%
IMUL	2.171	2.251	8.25	30%	.416	541%
FMPR	2.808	2.888	13.125	21%	.416	694%
DFMP	4.547	4.627	50	8%	.576	803%

Instant Expert Service

A new level of responsiveness and effectiveness is now possible in dealing with interruptions of system availability, whether caused by hardware failure or system software problems. The improvement over traditional methods results from our Instant Expert Service (IES); it works as follows.

Upon detection of any abnormality in system operation, the customer notifies the Support Center (SC) (by telephone or network). SC personnel immediately connect to the customer's system via the dedicated modem in the Console Computer of the F1. An expert in the diagnosing of malfunctioning systems then determines the general nature of the problem (operator error, user confusion, system software, probable hardware failure). This expert is a specialist in this task, knows how to use Exec DDT and basic hardware debugging aids. Further, he has available an extensive database (online in the SC computer system) containing up-to-date information on the exact configurations, version levels, and problem history of the customer's system, as well as sources and core images for the system software being used at that site. No time will be lost, therefore, before the SC has an accurate idea of the difficulty.

Experience shows that 90% of all problems can be solved (or at least system operation restored) at this stage by expert intervention. Operator errors and user confusions can be cleared up; known system problems can be corrected by immediate patches or special intervention; and software distribution problems can often be fixed by transmission of updates via the maintenance connection. Most interruptions of service can thus be remedied with little delay.

If the Diagnostic Expert concludes that a hardware problem is likely, a Support Engineer takes over the investigation. This engineer's qualifications are very much higher than that of a field service representative, and furthermore he begins his examination with the benefit of a detailed report on the observed symptoms, obtained from the Diagnostic Expert. Using the unprecedented maintenance aids of the F1 and its Console Computer, as well as the SC database (which includes on line all hardware documents), the Support Engineer localizes the failure. If, as sometimes happens, he would like to do experiments with the help of an operating system expert, one is near at hand. Meanwhile a field service representative can be en route to the customer's site with spare parts and test equipment. By the time he arrives, the engineer will probably have a good understanding of the failure, and replacement of failed parts proceeds under the engineer's careful supervision, which nearly eliminates the common problem of secondary trouble induced by inexperienced field service.

This scenario is admittedly idealized, but it illustrates the crucial feature that makes the IES system so effective in the real, sub-ideal world: every stage of the response to each problem is conducted by an expert. The advantages of this are clear, but they can be realized fully only by a carefully integrated system of exceptional debugging aids, precisely controlled databases and procedures, and (most important) the commitment of personnel with sufficient expertise. We believe that our system can achieve these goals more fully than ever before.