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FIELD MAINTENANCE PRINT SET

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D-CS-M3514-0-CHA5	CACHE DIR PWR, GND, CAP
D-CS-M3514-0-RES	CACHE DIR TERMINATORS

UNIT VARIATIONS COVERED BY THIS PRINT SET

MCA20

MCA20

Field Maintenance
Print Set

Digital Equipment
Corporation

PRINT SET REORDER NO.:
MP00267

REVISIONS	REV.		USED ON OPTION/MODEL	DRN.	DATE	TITLE:	digital		
	CHG. NO.		MCA20	CHK'D	DATE				
	DATE			PROJ. ENG.	DATE				
				FIELD SERV.	DATE				
SHEET 1 OF 1			DATE		SIZE		CODE	NUMBER	REV.
					B		TC	MCA20-0-1	
					DIST.				

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—SEE NOTES 1 & 2

	F	D	C	B	A
1	(00000)		00000	(00000)	00000
2	(00000)		00000	(00000)	00000
3	(00000)		00000	(00000)	00000
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53			00000	(00000)	00000
54			00000	(00000)	00000

REF. PIN SIDE
* SEE MODULE VARIATION TABLE

VARIATION / MODULE LOCATION CHART			
SLOT	MODULE / VARIATION		
	CACHE NO CHANNEL	CHANNEL NO	CACHE & CHANNEL
9	M8549-YA	M8533	M8533
10	NCNE	M8533	M8533
11	M8534-YD	M8538	M8538
12	M8549-YS	M8534	M8534
17	M8521	M8549-YH	M8521
18	NCNE	NCNE	NCNE
19	M8521	M8549-YH	M8521
24	M8521	M8549-YH	M8521
25	M8521	M8549-YH	M8521
27	M8514	M8549-YE	M8514
28	M8515	M8549-YF	M8515
	KLID AA, AB REF	KLID CA, CB REF	KLID BA, BB, BC, BD REF

NOTES:

1. SLOT 2 & 3 (SBUS) BC22C CABLES FROM INTERNAL MEMORY, OR DINA20 OR EMPTY
2. SLOT 1 (E AND CBUS) BC11A & BC22C CABLES FROM DTE

		DESCRIPTION		DWG./PART NO.		ITEM NO.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES							
ANGLES 30°		CLASS OF ACCURACY (CHECK ONE)		APPROXIMATE DIMENSION RANGE INCHES			
SURFACE QUALITY		IN		OVER 1.0 TO 3.0	OVER 3.0 TO 6.0	OVER 6.0 TO 12.0	OVER 12.0 TO 40.0
MEDIUM		☐		1.004	1.008	+0.012	+0.016
PREFERRED		☒		+0.012	+0.018	+0.024	+0.030
MICROFINISH		☐					

THIRD ANGLE PROJECTION		FIRST USED ON	
		KL10 diligit	
REMOVE BURRS AND BREAK SHARP CORNERS		TITLE	
DO NOT SCALE DWG		MODULE UTILIZATION (CPU)	
NEXT HIGHER ASSY.		SIZE CODE	
MATERIAL		NUMBER	
SCALE		REV	
FINISH		D INCH KL10-2-CPU	
SHEET		OF 1	
DRAWN		DATE	

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE

CACHE UPGRADE PROCEDURE

The following are the procedural steps in upgrading a non-cache 20 system to a cached 20 system. It is necessary to follow these steps in order.

Test equipment required:

- 1) Digital Voltmeter accuracy $\pm 0.05\%$ or better DC voltages.
- 2) Oscilloscope (Teletronic type 465, 475, 7000 series, or equivalent).
- 3) 3 Probes of equal length.

1) Run all system diagnostics at CR0, CS0 (25 MHz) and CR0, CS1 (28 MHz). Follow Appendix A. If any failures occur in this step, problems must be resolved before continuing the upgrade procedure.

2) Power system down and remove the following modules:

M8549YH	Slot 17
M8549YH	Slot 19
M8549YH	Slot 24
M8549YH	Slot 25
M8549YV	Slot 27
M8549YF	Slot 28

3) Install the following modules:

M8521	Slot 17
M8521	Slot 19
M8521	Slot 24
M8521	Slot 25
M8514	Slot 27
M8515	Slot 28

Reference documentation for Steps 2 and 3.

KL10 - C/VOL. 2
Print KL10-0-CPU
Module Utilization (CPU)

4) Add C backpanel wire from 4E43A1 to 4D44E1 (cache available).

5) Power up system and check all DC power in entire system at this point with digital voltmeter.

DC (TTL) voltage tolerance	± 5.0 + or - 0.025 volts	$\pm 5\%$
(Measured at module power)	-5.0 + or - 0.025 volts	
(pins.)	-15.0 + or - 0.075 volts	
	$+20.0$ + or - 0.100 volts	
DC (ECL) Voltage tolerance	-5.2 + or - 0.050 volts	$\pm 1\%$
(Measure at sense tabs on CPU Backplane.)	-2.0 + or - 0.050 volts	

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE

CACHE UPGRADE PROCEDURE

6) Check timing following the MA20/MB20/RH20 adjustment procedure accompanying this document: Appendix B.
If any timing is not within ± 1.0 Nsec of 50% points on the waveform, readjust to within ± 1.0 Nsec before continuing with upgrade procedure.

7) Rerun all CPU, memory and system diagnostics as listed in Appendix A.

8) Run DFKPB (instruction timing test) at CR0, CS0 (25 MHz) and compare the output with the accompanying document Appendix C. The times should differ only in the least significant digit.

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE

CACHE UPGRADE PROCEDURE

Appendix A

CPU Tests

1) DGKAA	-	E BOX test #1
2) DGKAB	-	E BOX test #2
3) DGKAB	-	M BOX test #1
4) DGKBD	-	Memory Control Test
5) DGABC	-	Paging Logic Test
6) DGMCA	-	Cache Option Test
7) DGMCB	-	Ram Banger test
8) DGMCD	-	Channel Logic test
9) DGMCE	-	Channel Loopback test
10) DGKCA	-	Meter Board Test
11) DFKM3	-	Cache Reliability
12) DFKAA	-	Basic Instruction test #1
13) DFKAB	-	Basic Instruction test #2
14) DFKAC	-	Basic Instruction test #3
15) DFKBA	-	Basic Instruction Reliability
16) DFKCA	-	Advanced Instructions
17) DFKDA	-	CPU/PI/Memory Reliability
18) DFKEA	-	Paging Hardware
19) DFKEB	-	MUOU and User Mode Test
20) DFKAD	-	Basic Instruction test #4

20 Tests

1) DGDTE	-	Basic DTE test
2) DFDTE	-	DTE Reliability test

DMA20/MA20/MB20 Tests

1) DDMMD	-	Memory Exerciser
2) DDMNE	-	BLT test
3) DDMNF	-	Floating Ones & Zeros test
4) DDMNG	-	Memory Exerciser (Over 256K)
5) MARGN.CMD	-	Auto Memory Margins

LP20 Test

1) DZLPL	-	LP20 Logic & Printer Test
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RH20 Tests

1) DFRHB	-	Tests RH20's - does not use any mass bus devices.
2) DFSXA	-	System 20 exerciser - tests RH20's with or without mass bus devices.

TU45/TN02 Tests

1) DFRHP	-	RH20 Fault Isolator
2) DFTUE	-	TU45 Device test
3) DFTUF	-	TU45 Multi-Device test

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

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ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE

CACHE UPGRADE PROCEDURE

Appendix A (Continued)

RP04/RP05/RP06 Tests

1) DFRPH	-	RP04 Device Test
2) DFRPJ	-	RP05 Device Test
3) DFRPK	-	RP06 Device Test
4) DDRPI	-	RP04/RP05/RP06 Reliability Test

SIZE	CODE	NUMBER	REV
A	SP	MCA20-0-2	

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ENGINEERING SPECIFICATION

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CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

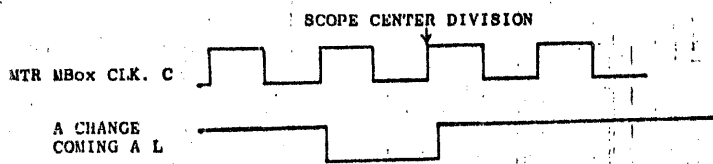
APPENDIX B

MA20 DESKEW PROCEDURE

- Notes:
1. Use equal length probes with short ground clips.
 2. Select CS0, CR0, (25MHz) on KL10.
 3. The M8562 delay lines are arranged so that (A) clock is the top pot and (B) clock is the bottom pot.
 4. A 7000 series or equivalent scope should be used when deskewing the MA20.
 5. The scope sweep rate should be 5ns or less per CM.

MA20 DESKEW PROCEDURE (ON LINE)

1. Attach Channel A probe to Pin 4D33P1. The signal name is: MTR MBox Clk. C.
2. Attach Channel B to 4E22F2. The signal name is: A Change Coming A L.
3. Observe on the scope the relationship of the MTR MBox Clk. C to A Change Coming A L.
4. See the figure below. Set the signal position accordingly.
5. Now move Channel B probe to Pin 5D26A1. Adjust the top delay on the M8562 in EF07 of the MA20 so that the leading edge 50 percent point crosses the previously set center division on the scope screen.
6. Now move Channel B probe to 5D29A1. Adjust the delay line on the M8562 in slot EF54 as in Step 5.
7. Next, move Channel A probe to Pin 5D26K1. Adjust the lower M8562 delay line in EF01 so that the leading edge aligns with the third MTR MBox Clk. C from which the clocks were previously aligned. Center the clock on a scope division line. Now align leading edges.
8. Now move Channel B Probe to 5D29K1. Adjust Clocks as in Step 7 for the M8562 in Slot EF54.

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CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

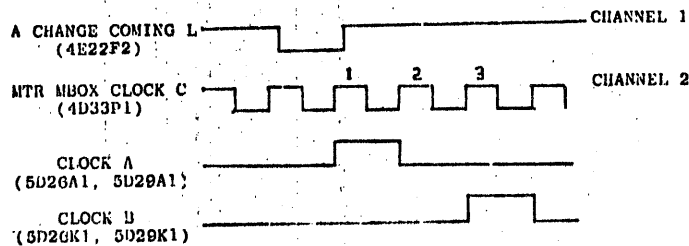
APPENDIX B

MU20 DESKEW PROCEDURE

- Notes:
1. Use equal length probes with short ground clips.
 2. Select clock rate 0 on KL10 (for on line deskew procedure).
 3. The M8565 delay lines are arranged so that (A) clock is the top pot and (B) clock is the bottom pot.
 4. A 7000 series or equivalent scope should be used when deskewing the MU20.
 5. The scope sweep rate should be 5ns or less per CM.

MU20 DESKEW PROCEDURE (ON LINE)

1. Set clock rate to "CR0", clock "source" to "CS0", Type "FX1" to turn the clock on.
2. Place channel 1 probe on Pin 4E22F2 "A Change Coming A L", sync on channel 1.
3. Place channel 2 probe on Pin 4D33P1 "MTR MBox clock C".
4. Align the rising edge of the pulse designated as 1, so that the 50% point crosses the second vertical division of the scope screen. Note this position.
5. Place channel 2 probe on Pin 5D26A1. Adjust the top delay on the M8565, slot 5EF01 so that the leading edge 50% point crosses the second vertical division of the scope screen.
6. Place channel 2 probe on Pin 5D29A1. Adjust the top delay on the M8565, slot 5EF01 so that the leading edge 50% point crosses the second vertical division of the scope screen.
7. Replace channel 2 probe on Pin 4D33P1 "MTR MBox Clock C".
8. Align the leading edge of the pulse designated as 3, so that the 50% point crosses the nearest vertical division mark of the scope screen. Note this position.
9. Place Channel 2 probe on Pin 5D26K1. Adjust the bottom delay on the M8565. Slot 5EF01 so that the leading edge 50% point crosses the vertical division. Mark note in Step 8.
10. Place Channel 2 probe on Pin 5D29K1. Adjust the bottom delay on the M8565, Slot 5EF54 so that the leading edge 50% point crosses the vertical division. Mark Note in Step 8.

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A SP MCA20-0-2DEC FORM NO EN-01022-16-N370-1381
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CONTINUATION SHEET

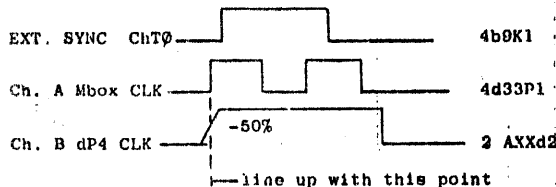
TITLE CACHE UPGRADE PROCEDURE

APPENDIX B

RH20 DESKEW PROCEDURE

Use a 475 or a 4 trace scope.
All the RH20's are deskewed to MBOX CLK that produces CHT0 in the channel. Recheck skew whenever the CBUS cable or M8566 board is replaced. The pots to be adjusted are on the M8569 board. The top pot is for RH20 #0, second pot for RH20 #1 etc.

- 1) Load Micro Code. Set CS0-CR0, FX1.
- 2) Sync Positive - External sync on 4B0K1 --- Ch T0 H -- (Ch C1).
- 3) Ch A on 4D33P1 - MBOX CLK H - (MTR 2).
- 4) Ch B on 2 AXXD2 - DP1 CLK H - (DP4).
- 5) Align 1 AXXD2 with the 50% point of the MBOX CLK that happens approximately 10 ns before the CHT0 CLK.



RH20	PIN #
0	2 A36D2
1	2 A33D2
2	2 A30D2
3	2 A27D2
4	2 A24D2
5	2 A21D2
6	2 A18D2
7	2 A15D2

SIZE CODE NUMBER REV
A SP MCA20-0-2DEC FORM NO EN-01022-16-N370-1381
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ENGINEERING SPECIFICATION

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CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

APPENDIX C

Appendix C
PDP-10 KL10 INSTRUCTION TIMING TEST (DFKFR)
VERSION 0.1, SV=0.11, CPU#0, MCV=126, MCO=0, MO=30, 60HZ
SWITCHES = 000000 000000
CLK SOURCE = NORMAL, CLK RATE + FULL, AC BLK 0, CACHE: 0 1 2 3

- 1 - BASIC CLOCK CYCLE IS 40 NSEC.
- 2 - INDEXING TAKES 40 NSEC.
- 3 - INDIRECT TAKES 280 NSEC.
- 4 - INDEXING AND INDIRECT TAKES 320 NSEC.
- 5 - MOVE1 TAKES 320 NSEC.
- 6 - MOVE FROM AC TAKES 440 NSEC.
- 7 - MOVE FROM MEMORY TAKES 480 NSEC.
- 8 - HRR FROM MEMORY TAKES 520 NSEC.
- 9 - SETOM 0 TAKES 560 NSEC.
- 10 - JHST TAKES 360 NSEC.
- 11 - JSR TAKES 680 NSEC.
- 12 - PUSHJ TAKES 840 NSEC.
- 13 - ADD FROM MEMORY TAKES 520 NSEC.
- 14 - MUL (8 ADD/SUB - 18 SHIFTS) TAKES 2.52 USEC.
- 15 - DIV TAKES 5.58 USEC.
- 16 - FIX A FLOATING POINT ONE TAKES 1.04 USEC.
- 17 - FLTR AN INTERGER ONE TAKES 1.84 USEC.
- 18 - FAD (1 RIGHT SHIFT) TAKES 1.88 USEC.
- 19 - FAD (8 SHIFT RIGHT - 3 LEFT) TAKES 2.16 USEC.
- 20 - FMP (7 ADD/SUB - 14 SHIFTS) TAKES 2.40 USEC.
- 21 - FMP TAKES 5.72 USEC.
- 22 - DMOVE FROM MEMORY TAKES 880 NSEC.
- 23 - DFAD (1 RIGHT SHIFT) TAKES 2.44 USEC.
- 24 - DFAD (8 SHIFT RIGHT - 1 LEFT) TAKES 2.44 USEC.
- 25 - DFMP (7 ADD/SUB - 32 SHIFTS) TAKES 4.92 USEC.
- 26 - DFMP TAKES 10.32 USEC.
- 27 - CONO PI TAKES 1.92 USEC.
- 28 - CONI PI TAKES 3.36 USEC.
- 29 - DATAO APR TAKES 1.56 USEC.
- 30 - DATAI APR TAKES 1.76 USEC.
- 31 - MOVE TO MEMORY TAKES 680 NSEC.
- 32 - LOGICAL SHIFT (35 PLACES LEFT) TAKES 640 NSEC.
- 33 - LOGICAL SHIFT (35 PLACES RIGHT) TAKES 760 NSEC.
- 34 - LOGICAL SHIFT COMBINED (71 PLACES LEFT) TAKES 1.12 USEC.
- 35 - LOGICAL SHIFT COMBINED (71 PLACES RIGHT) TAKES 1.16 USEC.
- 36 - INCREMENT BYTE POINTER TAKES 1.00 USEC.
- 37 - INCREMENT AND LOAD BYTE TAKES 1.44 USEC.
- 38 - INCREMENT AND DEPOSIT BYTE TAKES 1.80 USEC.
- 39 - JFCL TAKES 880 NSEC.
- 40 - CAI TAKES 480 NSEC.
- 41 - JUMP TAKES 480 NSEC.
- 42 - CAM TAKES 600 NSEC.
- 43 - EQV AC TO AC TAKES 480 NSEC.
- 44 - EQV MEMORY TO AC TAKES 520 NSEC.
- 45 - SETOM TAKES 680 NSEC.
- 46 - AOS TO MEMORY TAKES 840 NSEC.

SIZE CODE NUMBER REV
A SP MCA20-0-2DEC FORM NO EN-01022-16-N370-1381
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ENGINEERING SPECIFICATION

digital

CONTINUATION SHEET

TITLE CACHE UPGRADE PROCEDURE

APPENDIX C (Continued)

- 47 - EXCHANGE AN AC WITH AN AC TAKES 640 NSEC.
- 48 - EXCHANGE AN AC WITH MEMORY TAKES 840 NSEC.
- 49 - EXECUTE TAKES 640 NSEC.
- 50 - BLT MEMORY TO MEMORY TAKES 1.92 USEC.
- 51 - BLT AC TO MEMORY TAKES 1.88 USEC.
- 52 - DATAI TAKES 10.00 USEC.
- 53 - DATAO TAKES 10.00 USEC.

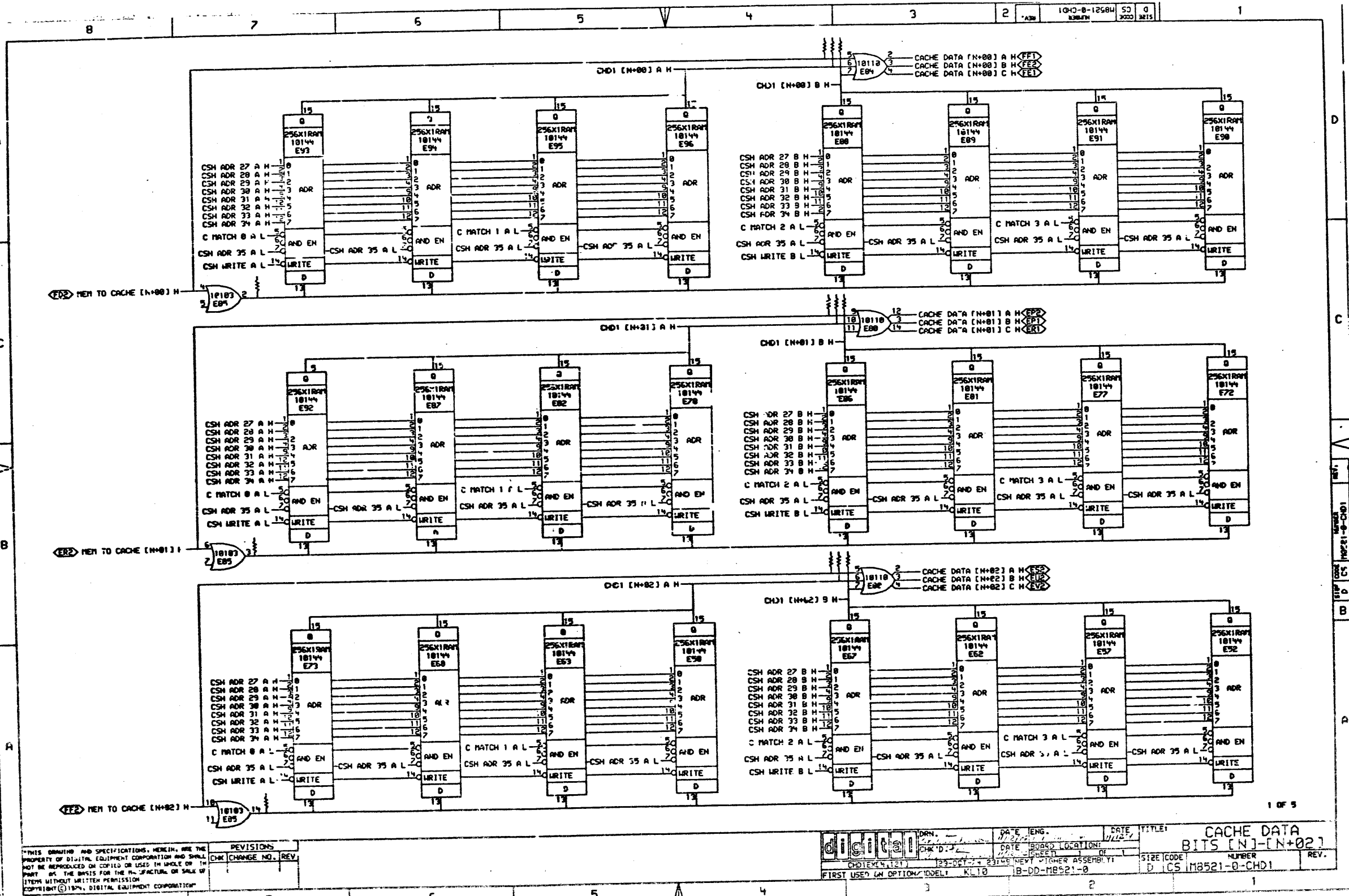
TEST COMPLETED

SIZE
A

CODE
SF

NUMBER
MCA20-0-2

REV



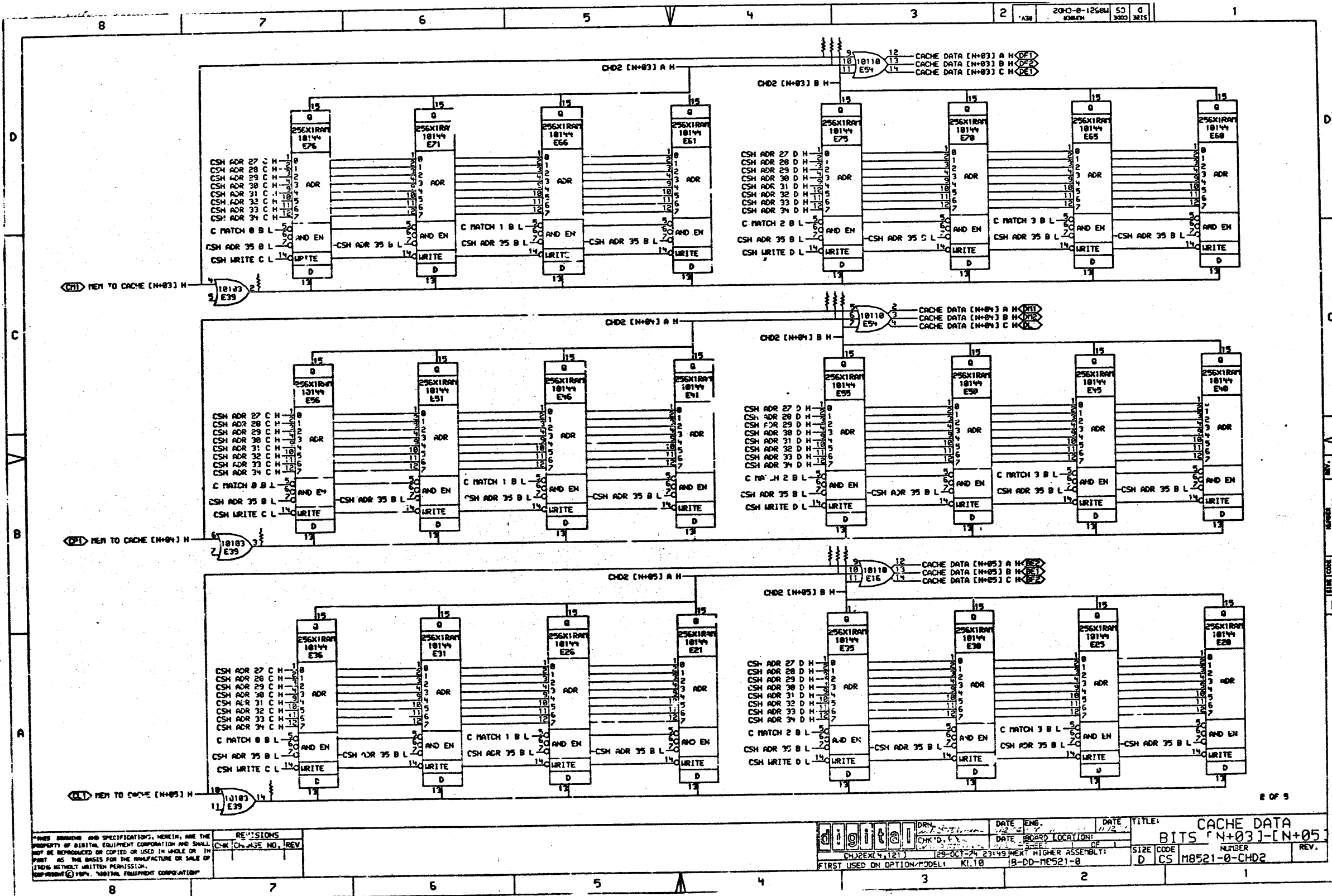
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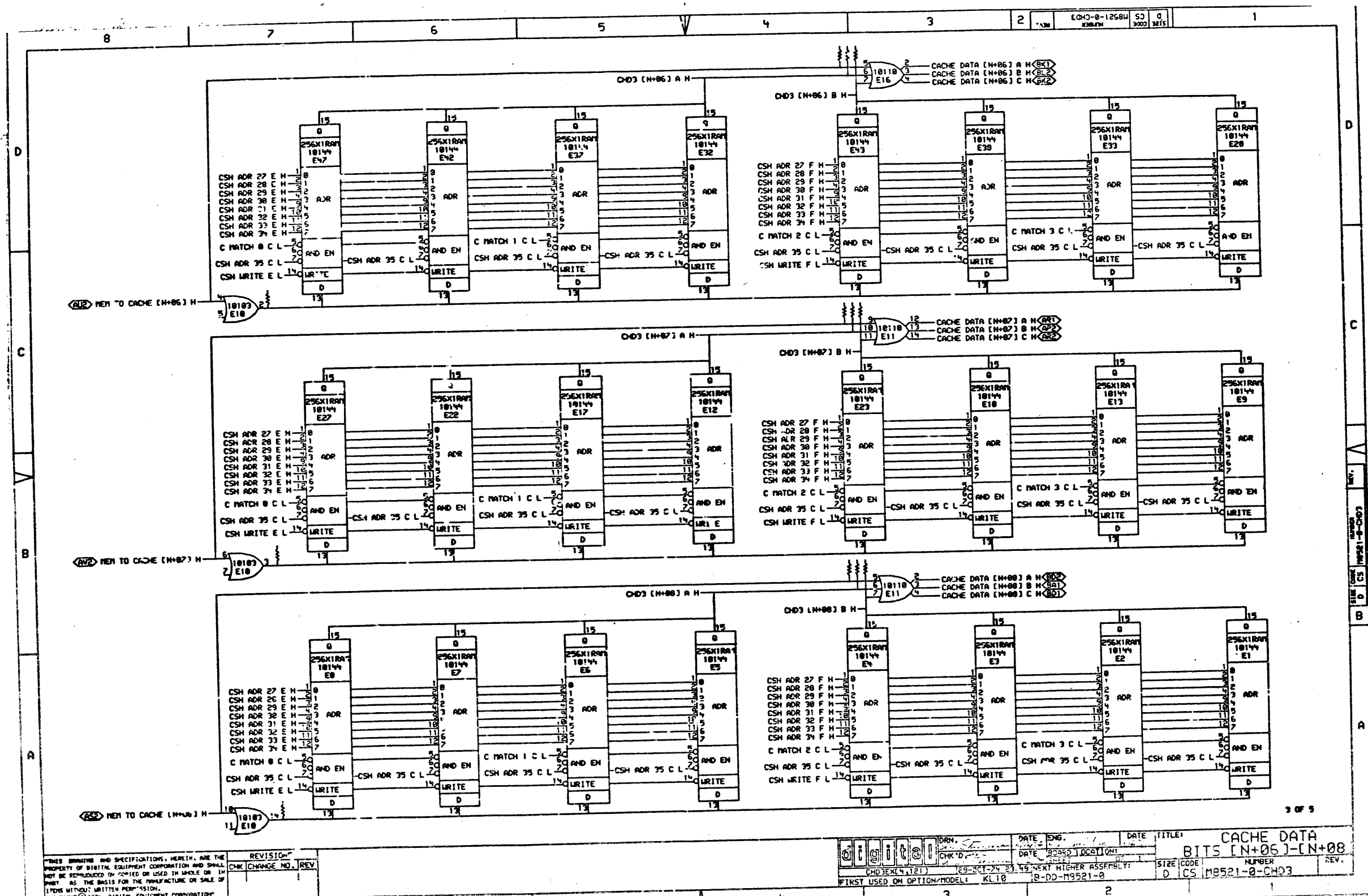
REVISIONS		
REV	CHANGE NO.	REV
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DATE	ENG.	DATE	ENG.	DATE	ENG.
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11/12/71	KL10	11/12/71	KL10	11/12/71	KL10
11/12/71	KL10	11/12/71	KL10	11/12/71	KL10

CACHE DATA BITS [N]-[N+02]

DATE	ENG.	DATE	ENG.	DATE	ENG.
11/12/71	KL10	11/12/71	KL10	11/12/71	KL10
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11/12/71	KL10	11/12/71	KL10	11/12/71	KL10



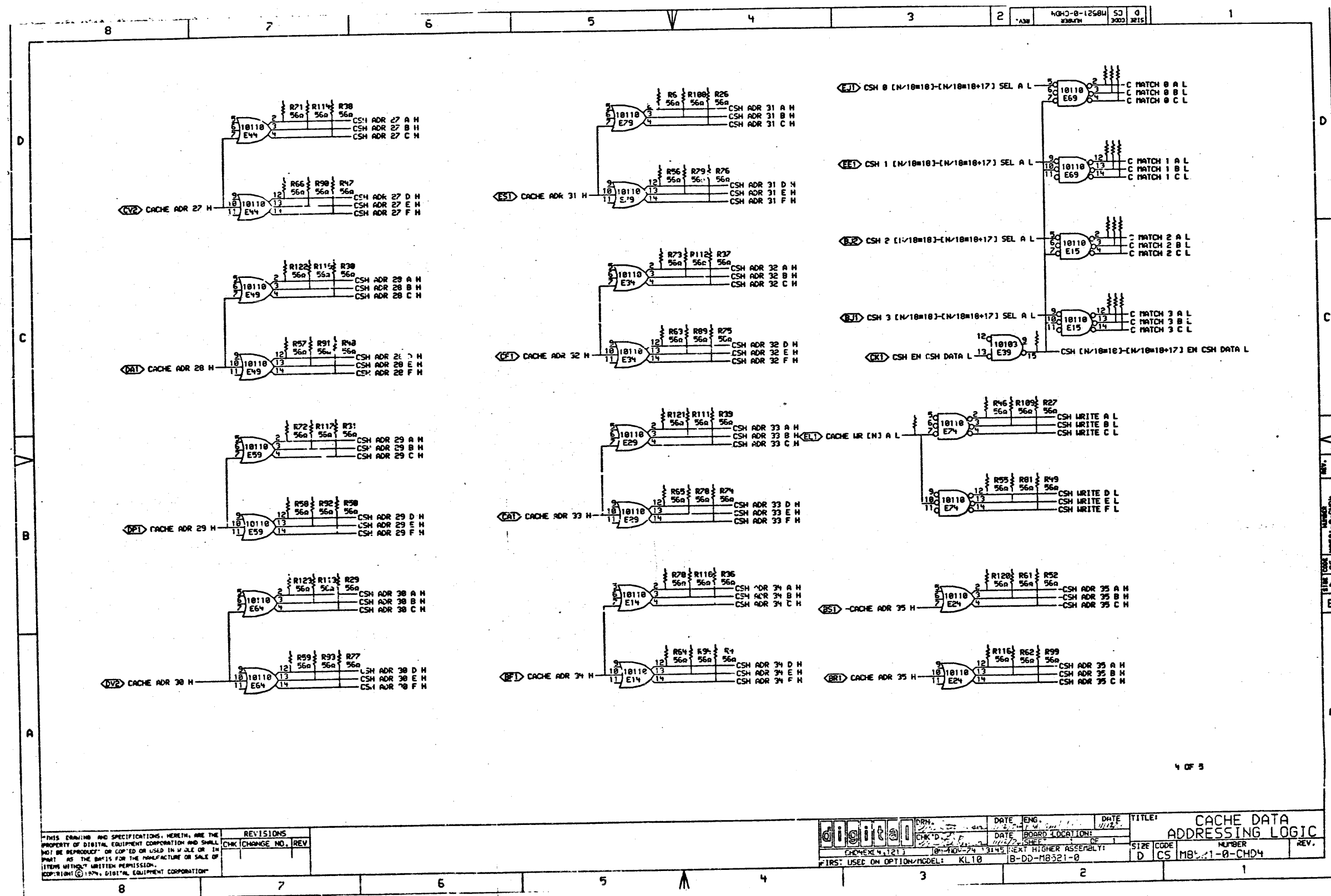


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REVISION
CHK CHANGE NO. REV

DATE	ENG.	DATE	TITLE
CHK'D		DATE	LOCATED
CHD3EX14,121			
FIRST USED ON OPTION/MODEL: KL10			
DATE: 08-00-1974			
NEXT HIGHER ASSEMBLY: 8-DD-M9521-8			
SIZE CODE: D		NUMBER: CS M9521-8-CHD3	
REV.			

CACHE DATA
BITS [N+06]-[N+08]

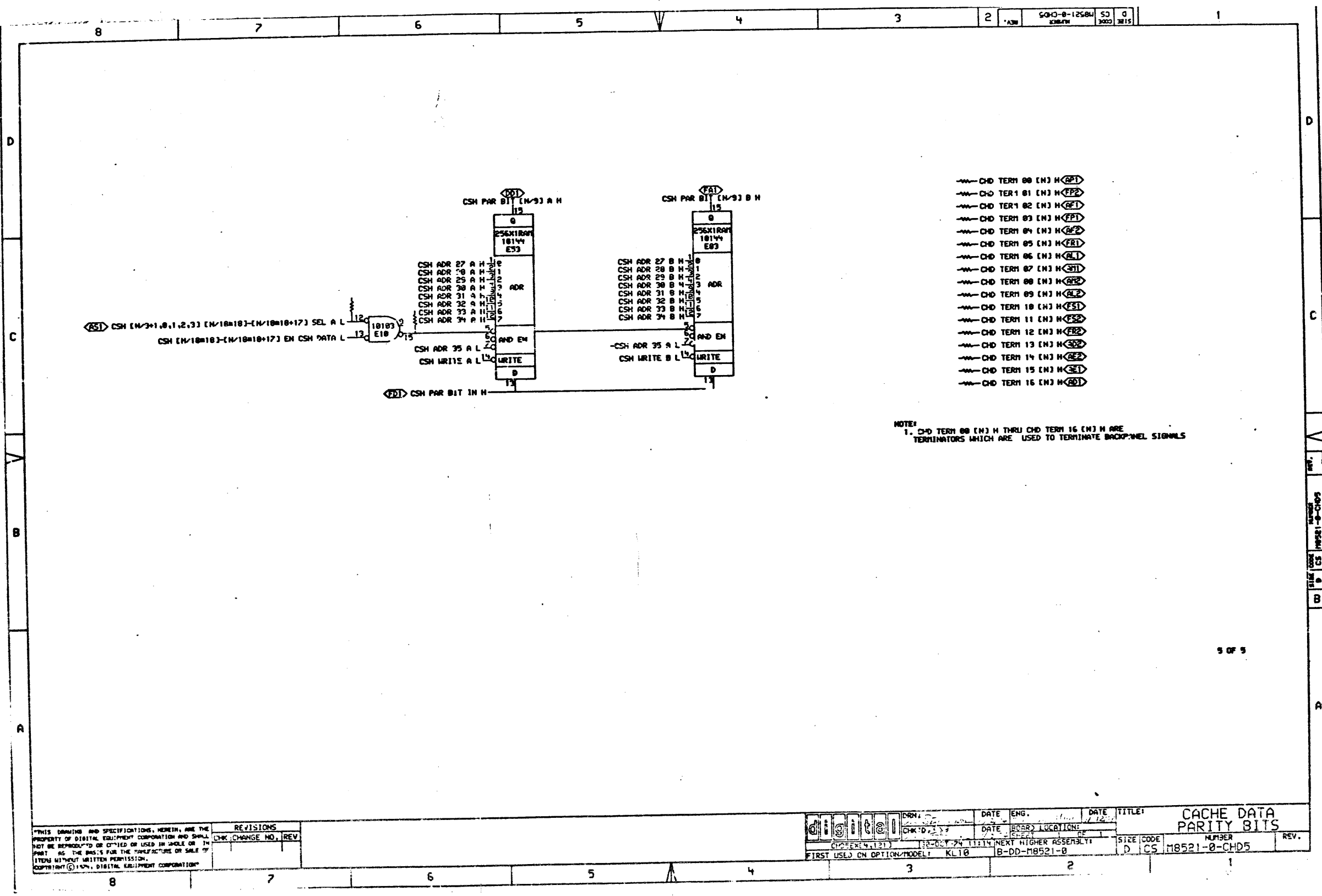


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REVISIONS		
CHK	CHANGE NO.	REV

digital	DATE	ENG.	DATE	TITLE
	CHK'D	DATE	BOARD LOCATION	SHEET
CHECKED BY: 1213		101-AD-24 3145		NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: KL10		B-DD-M8321-0		SIZE CODE
				NUMBER
				REV.

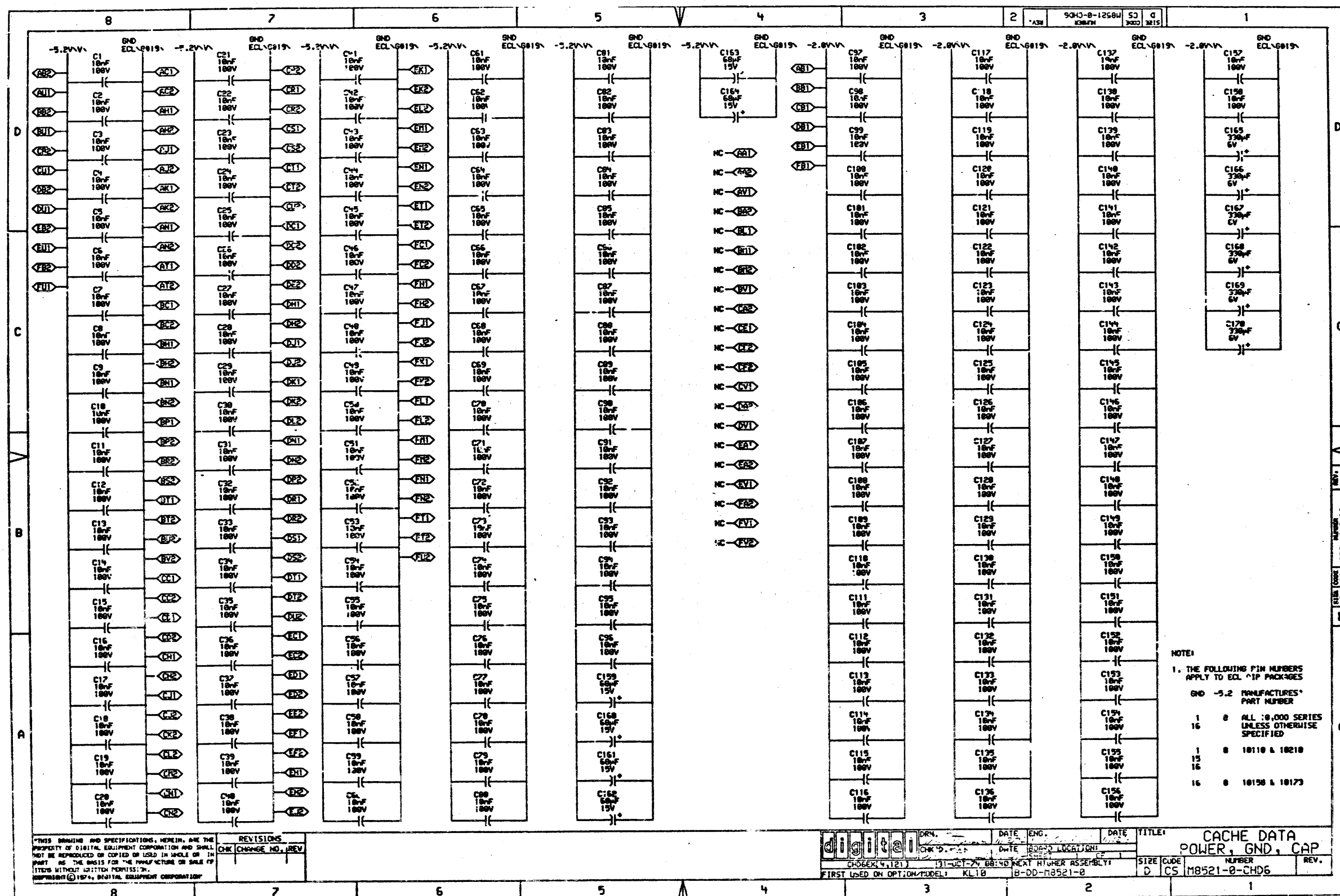
CACHE DATA ADDRESSING LOGIC
D CS M8321-0-CHD4

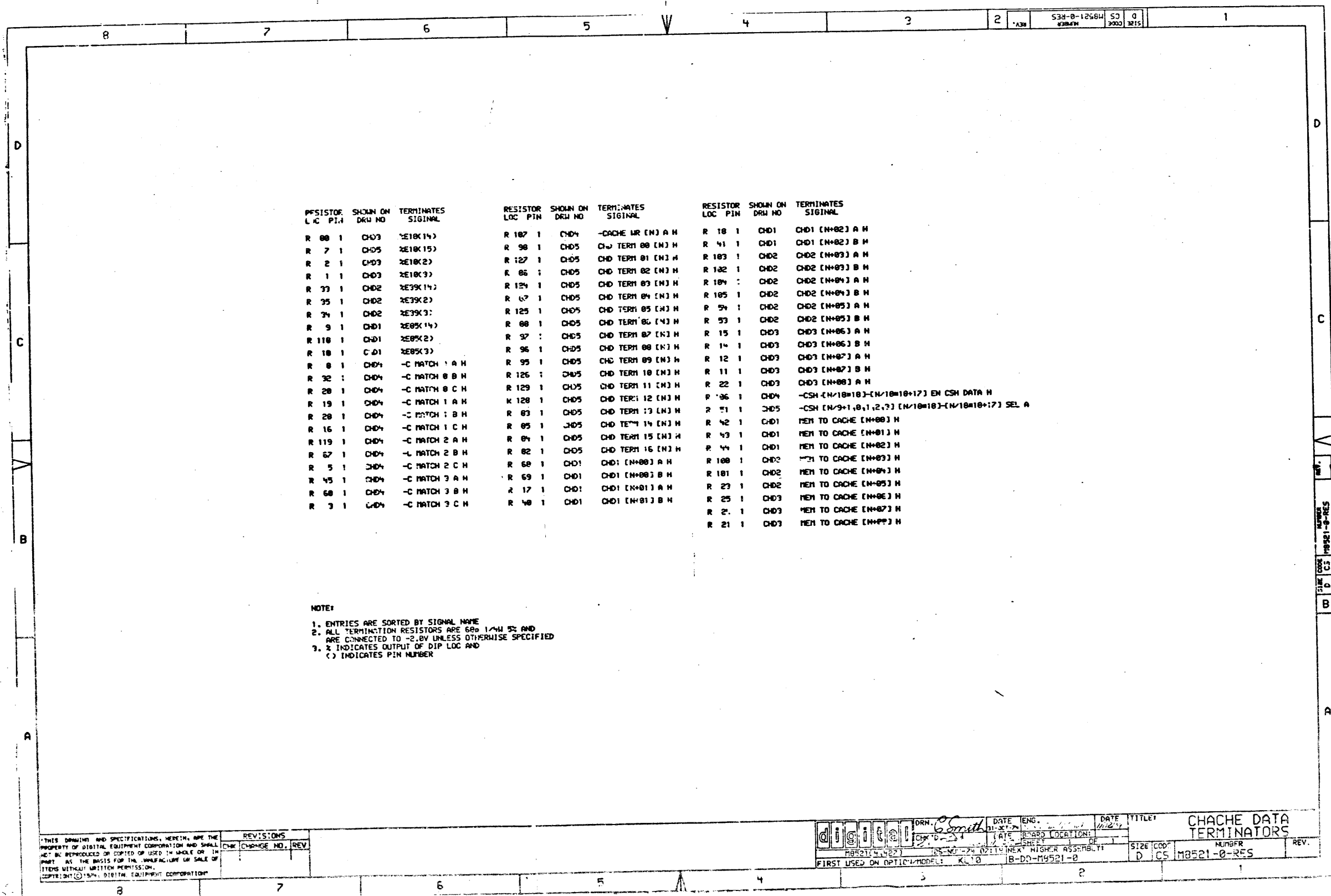


NOTE:
1. CHD TERM 00 (N) H THRU CHD TERM 16 (N) H ARE TERMINATORS WHICH ARE USED TO TERMINATE BACKWEL SIGNALS

5 OF 5

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FIRST USED ON OPTION/MODEL KL10		SIZE CODE NUMBER D CS M8521-0-CHD5		REV.			

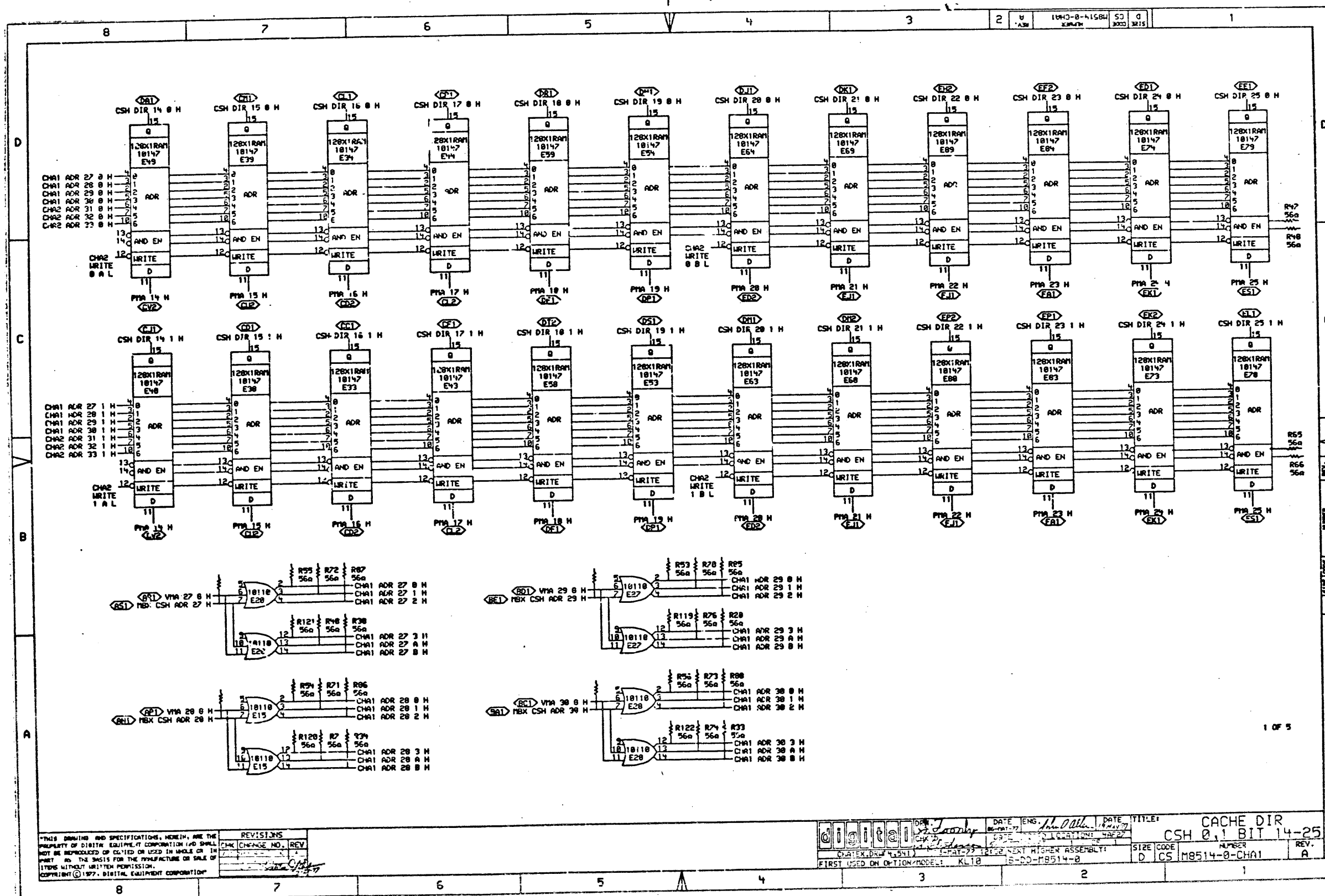


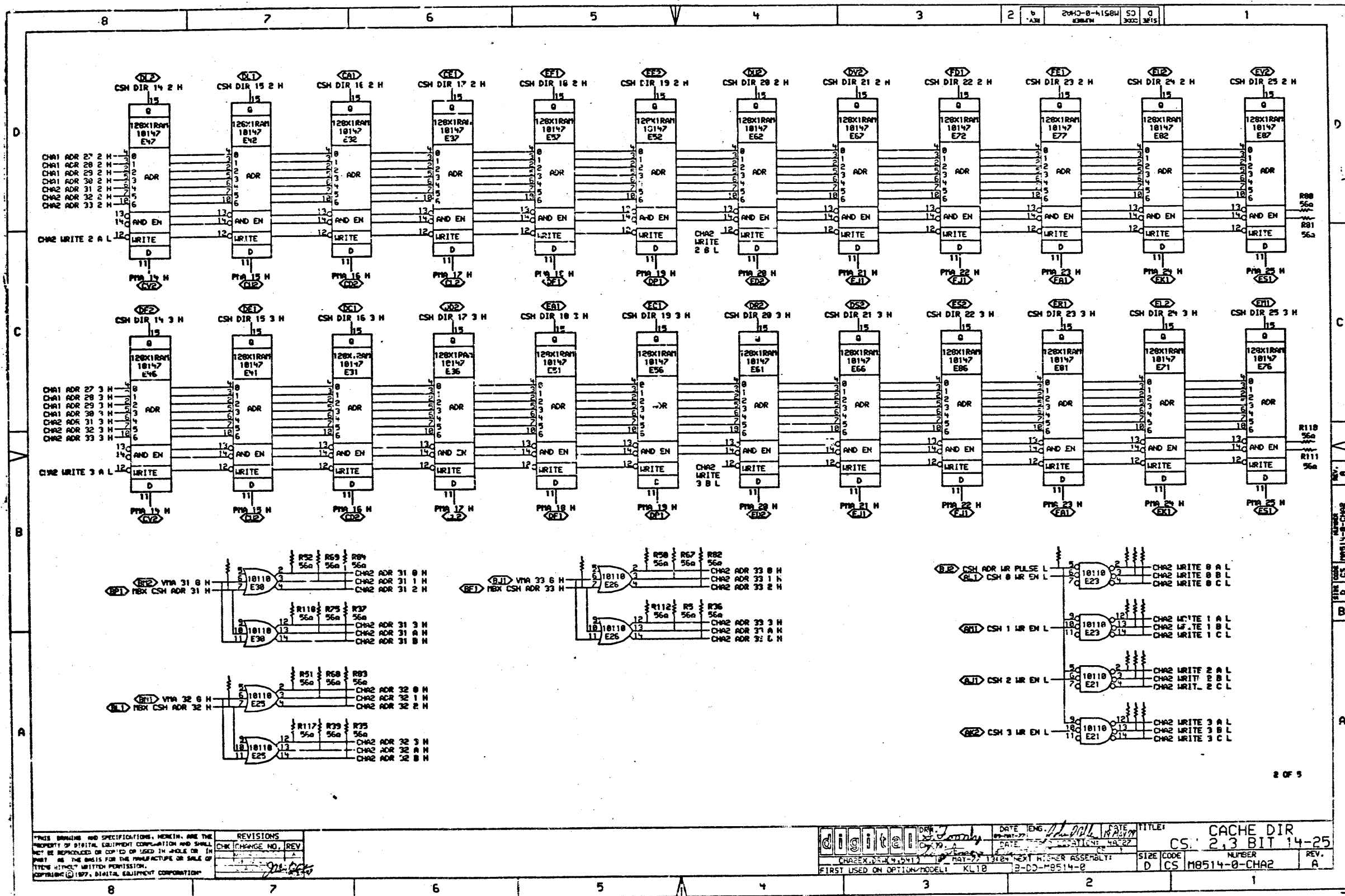


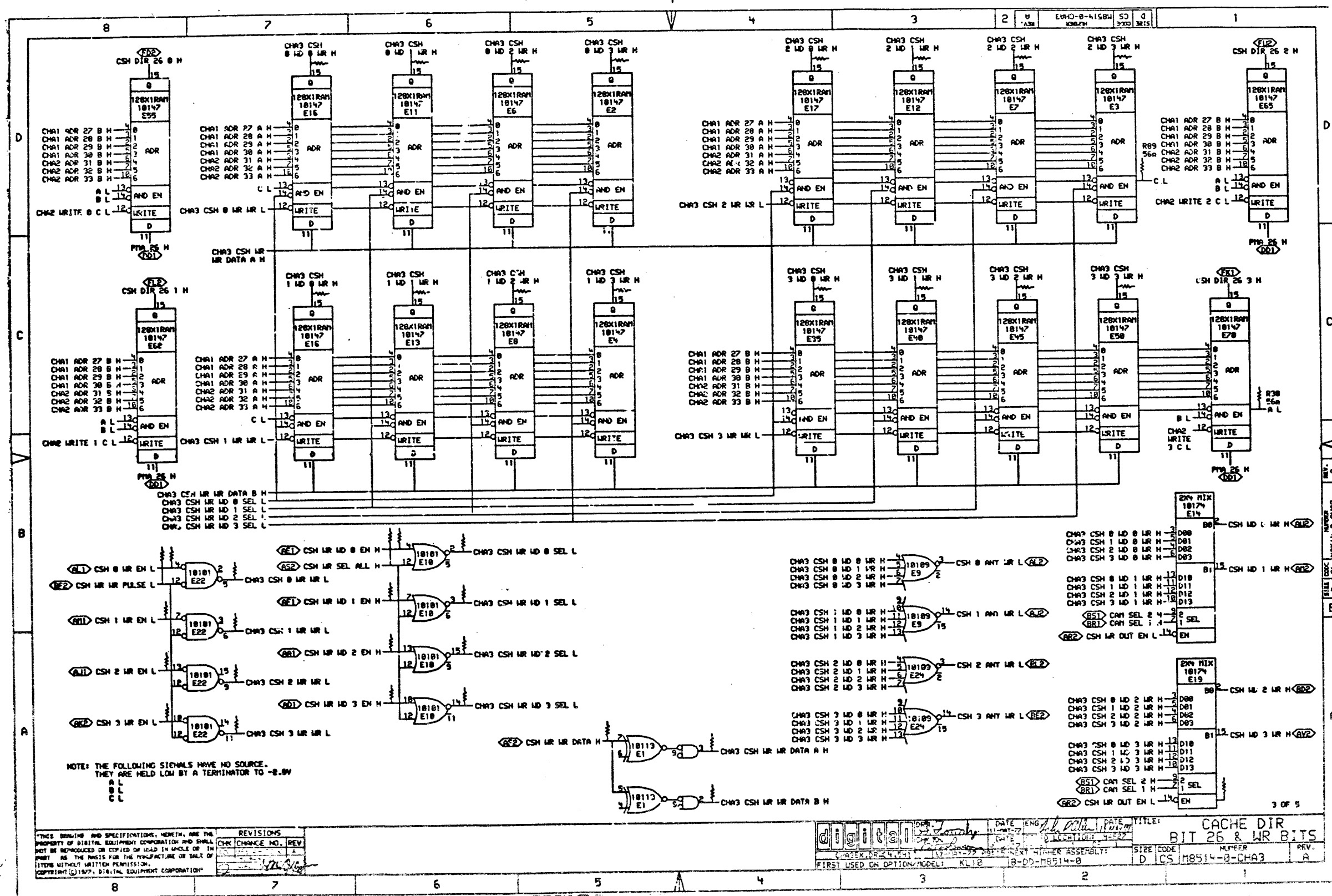
RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL	RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL	RESISTOR LOC PIN	SHOWN ON DRW NO	TERMINATES SIGNAL
R 88 1	CH03	2E10K14	R 107 1	CH04	-CACHE LR (N) A H	R 18 1	CH01	CH01 (N+02) A H
R 7 1	CH05	2E10K15	R 98 1	CH05	CH0 TERM 00 (N) H	R 41 1	CH01	CH01 (N+02) B H
R 2 1	CH03	2E10K2	R 127 1	CH05	CH0 TERM 01 (N) H	R 103 1	CH02	CH02 (N+03) A H
R 1 1	CH03	2E10K3	R 85 1	CH05	CH0 TERM 02 (N) H	R 102 1	CH02	CH02 (N+03) B H
R 33 1	CH02	2E39K14	R 124 1	CH05	CH0 TERM 03 (N) H	R 104 1	CH02	CH02 (N+04) A H
R 35 1	CH02	2E39K2	R 67 1	CH05	CH0 TERM 04 (N) H	R 105 1	CH02	CH02 (N+04) B H
R 24 1	CH02	2E39K3	R 125 1	CH05	CH0 TERM 05 (N) H	R 54 1	CH02	CH02 (N+05) A H
R 9 1	CH01	2E85K14	R 88 1	CH05	CH0 TERM 06 (N) H	R 53 1	CH02	CH02 (N+05) B H
R 110 1	CH01	2E85K2	R 37 1	CH05	CH0 TERM 07 (N) H	R 15 1	CH03	CH03 (N+06) A H
R 10 1	CH01	2E85K3	R 96 1	CH05	CH0 TERM 08 (N) H	R 14 1	CH03	CH03 (N+06) B H
R 8 1	CH04	-C MATCH 1 A H	R 95 1	CH05	CH0 TERM 09 (N) H	R 12 1	CH03	CH03 (N+07) A H
R 32 1	CH04	-C MATCH 0 B H	R 126 1	CH05	CH0 TERM 10 (N) H	R 11 1	CH03	CH03 (N+07) B H
R 20 1	CH04	-C MATCH 0 C H	R 129 1	CH05	CH0 TERM 11 (N) H	R 22 1	CH03	CH03 (N+08) A H
R 19 1	CH04	-C MATCH 1 A H	R 128 1	CH05	CH0 TERM 12 (N) H	R 36 1	CH04	-CSH (N/10+10)-(N/10+17) EN CSH DATA H
R 20 1	CH04	-C MATCH 1 B H	R 83 1	CH05	CH0 TERM 13 (N) H	R 51 1	CH05	-CSH (N/9+1,0,1,2,3) (N/10+10)-(N/10+17) SEL A
R 16 1	CH04	-C MATCH 1 C H	R 85 1	CH05	CH0 TERM 14 (N) H	R 42 1	CH01	MEM TO CACHE (N+00) H
R 119 1	CH04	-C MATCH 2 A H	R 84 1	CH05	CH0 TERM 15 (N) H	R 43 1	CH01	MEM TO CACHE (N+01) H
R 67 1	CH04	-L MATCH 2 B H	R 82 1	CH05	CH0 TERM 16 (N) H	R 44 1	CH01	MEM TO CACHE (N+02) H
R 5 1	CH04	-C MATCH 2 C H	R 68 1	CH01	CH01 (N+00) A H	R 100 1	CH02	MEM TO CACHE (N+03) H
R 45 1	CH04	-C MATCH 3 A H	R 69 1	CH01	CH01 (N+00) B H	R 101 1	CH02	MEM TO CACHE (N+04) H
R 60 1	CH04	-C MATCH 3 B H	R 17 1	CH01	CH01 (N+01) A H	R 23 1	CH02	MEM TO CACHE (N+05) H
R 3 1	CH04	-C MATCH 3 C H	R 40 1	CH01	CH01 (N+01) B H	R 25 1	CH03	MEM TO CACHE (N+06) H
						R 21 1	CH03	MEM TO CACHE (N+07) H

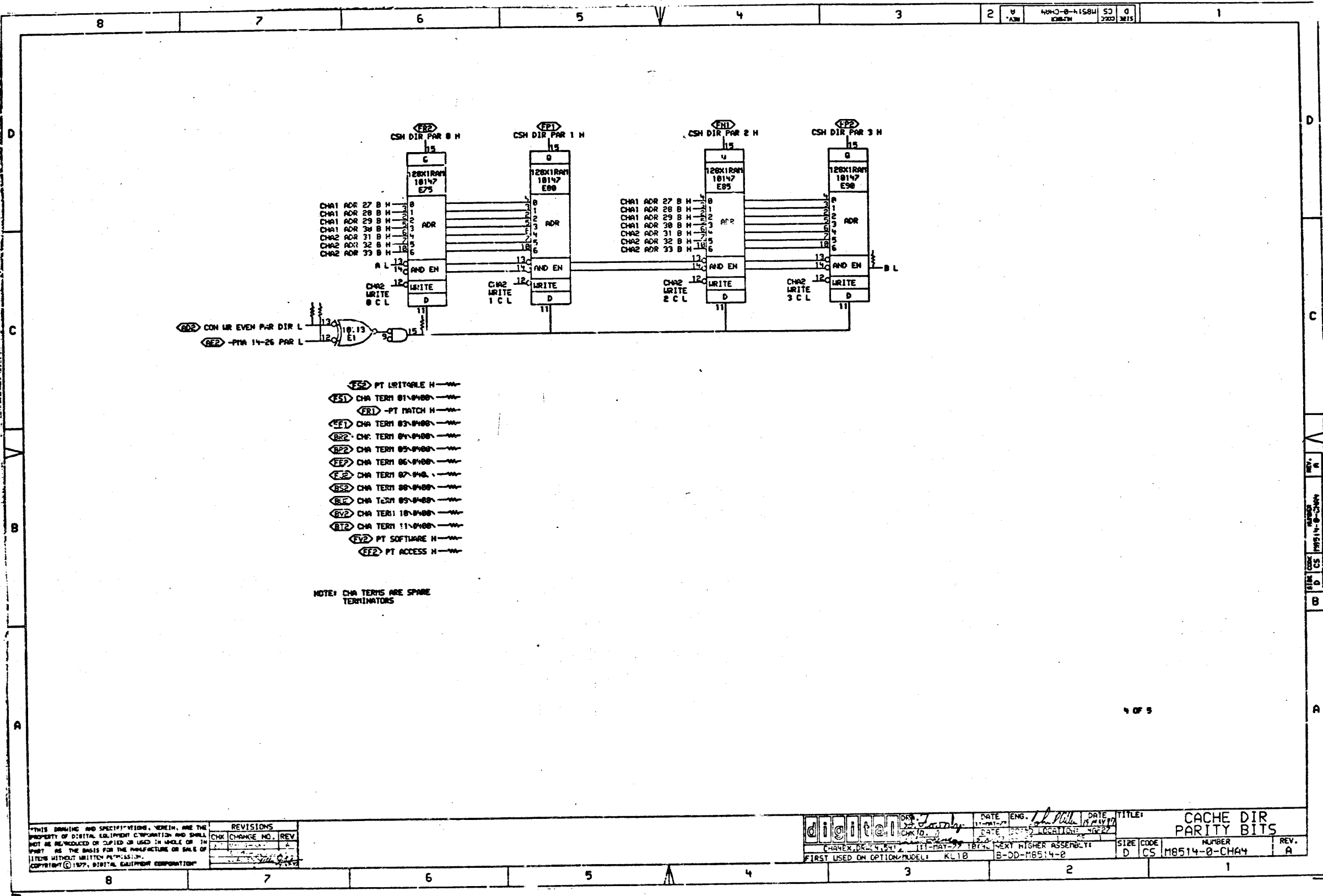
NOTES:
1. ENTRIES ARE SORTED BY SIGNAL NAME
2. ALL TERMINATION RESISTORS ARE 600 1/4W 5% AND
ARE CONNECTED TO -2.0V UNLESS OTHERWISE SPECIFIED
3. X INDICATES OUTPUT OF DIP LOC AND
() INDICATES PIN NUMBER

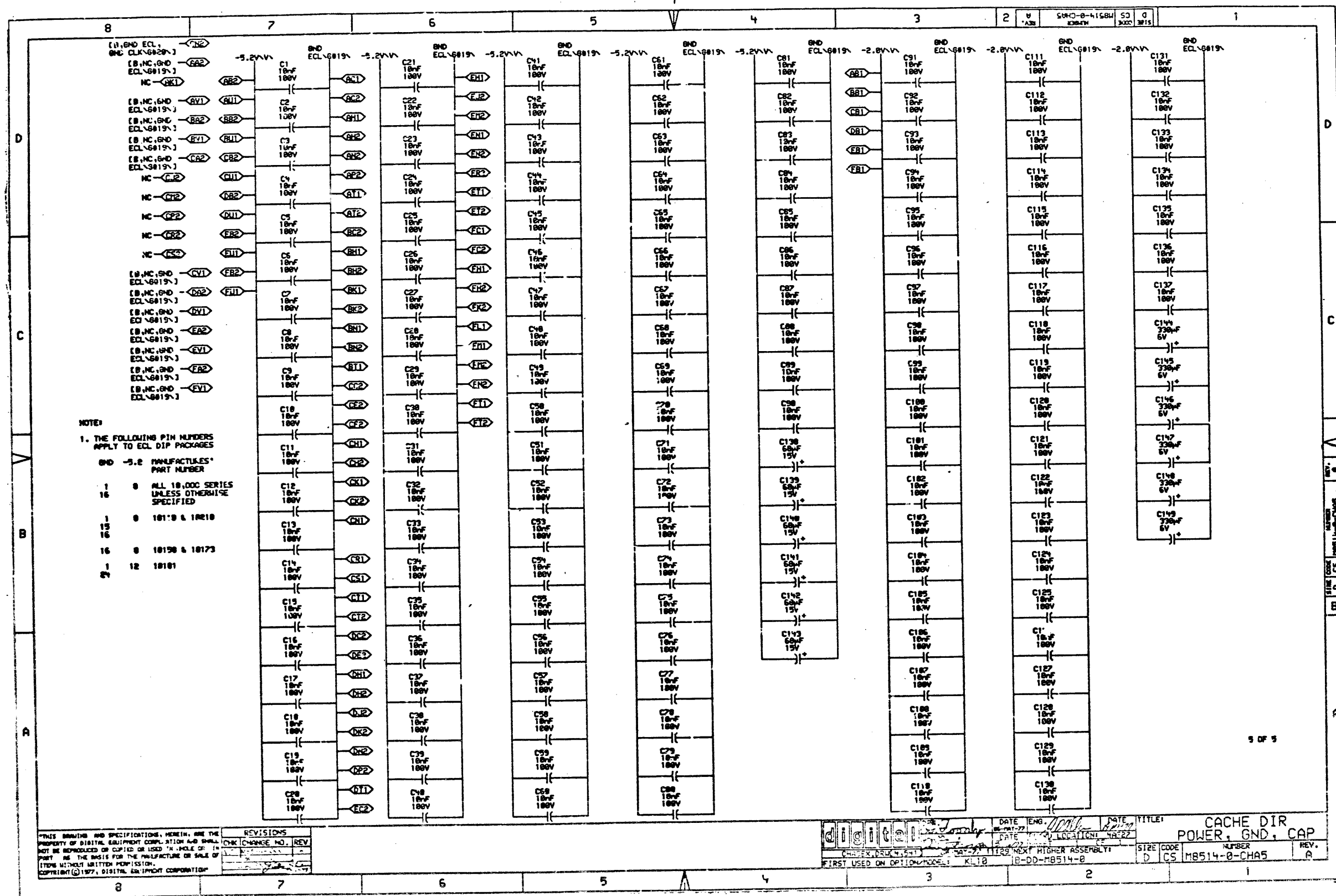
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				DATE BOARD LOCATION: <i>11/24/74</i>		SIZE CODE NUMBER REV.	
				FIRST USED ON OPTIC-MODEL: <i>KL10</i>		D CS M8521-0-RES	

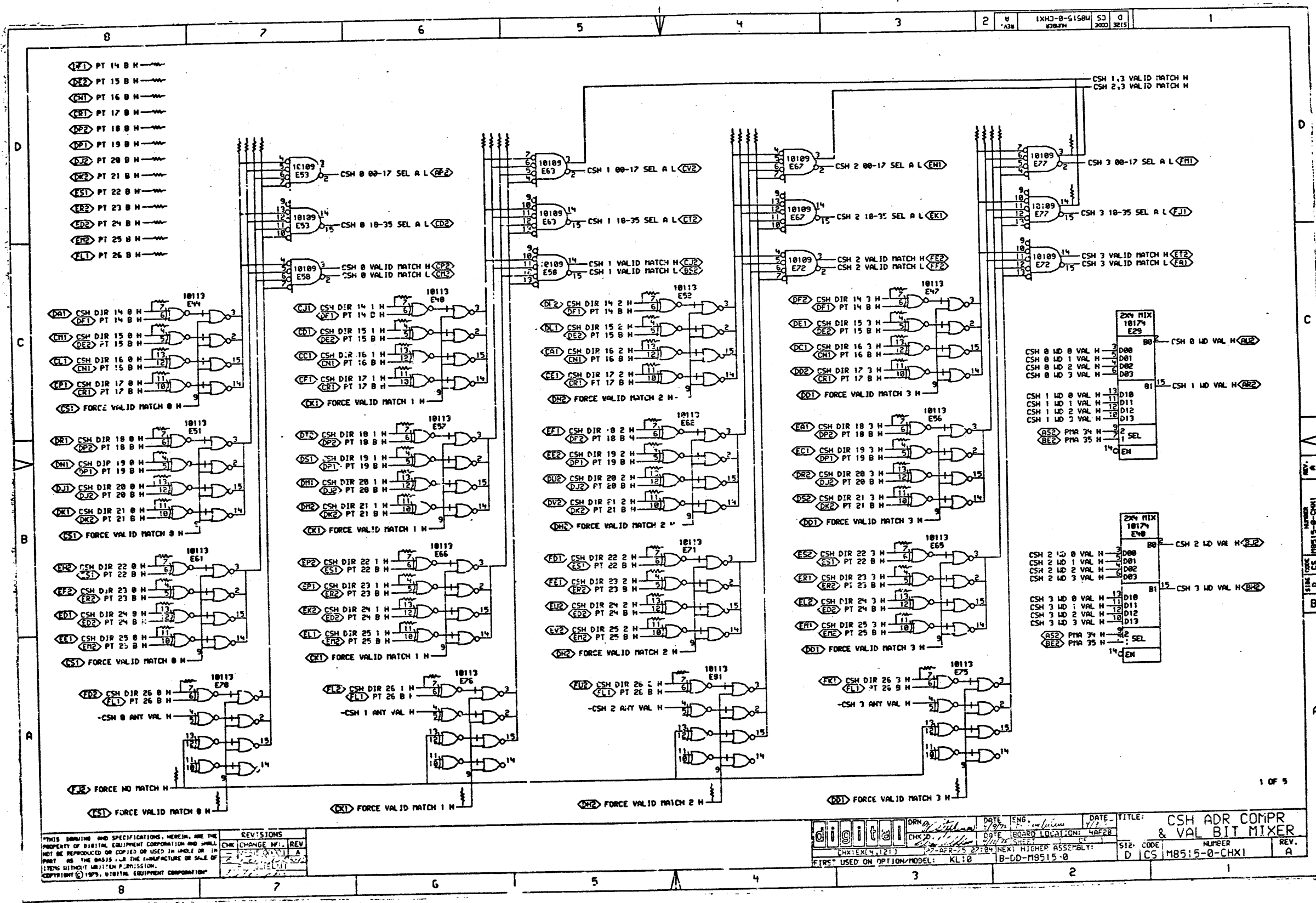


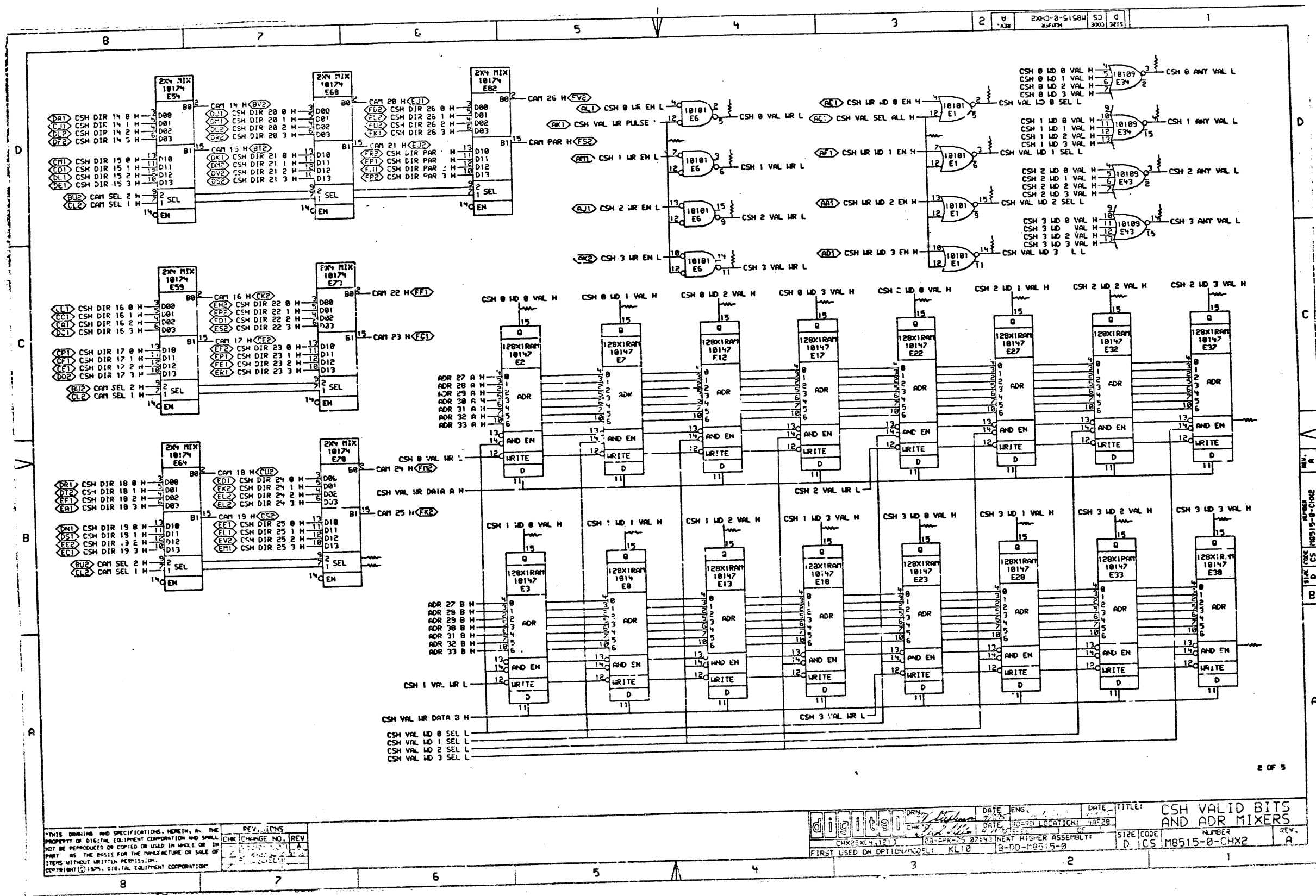


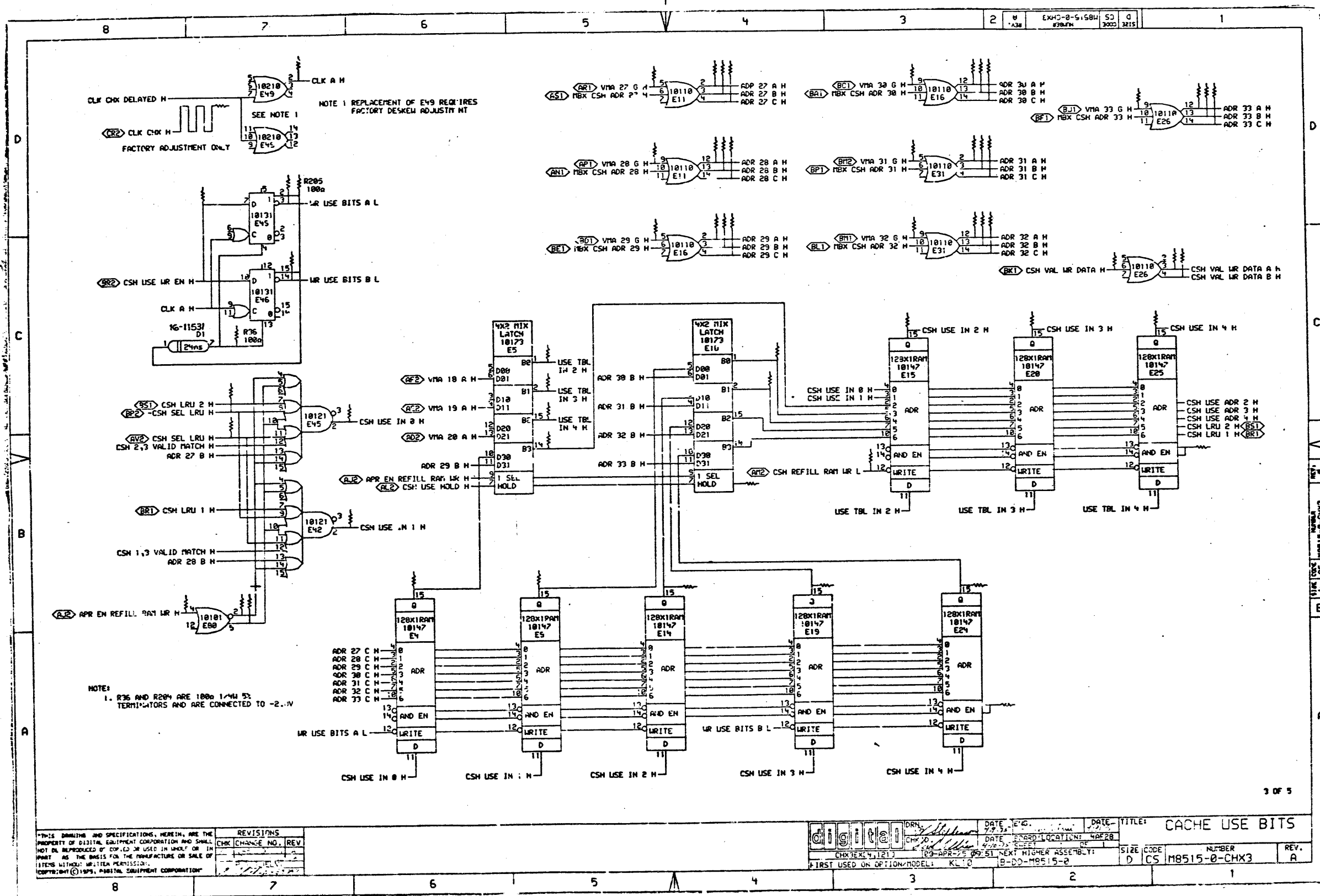


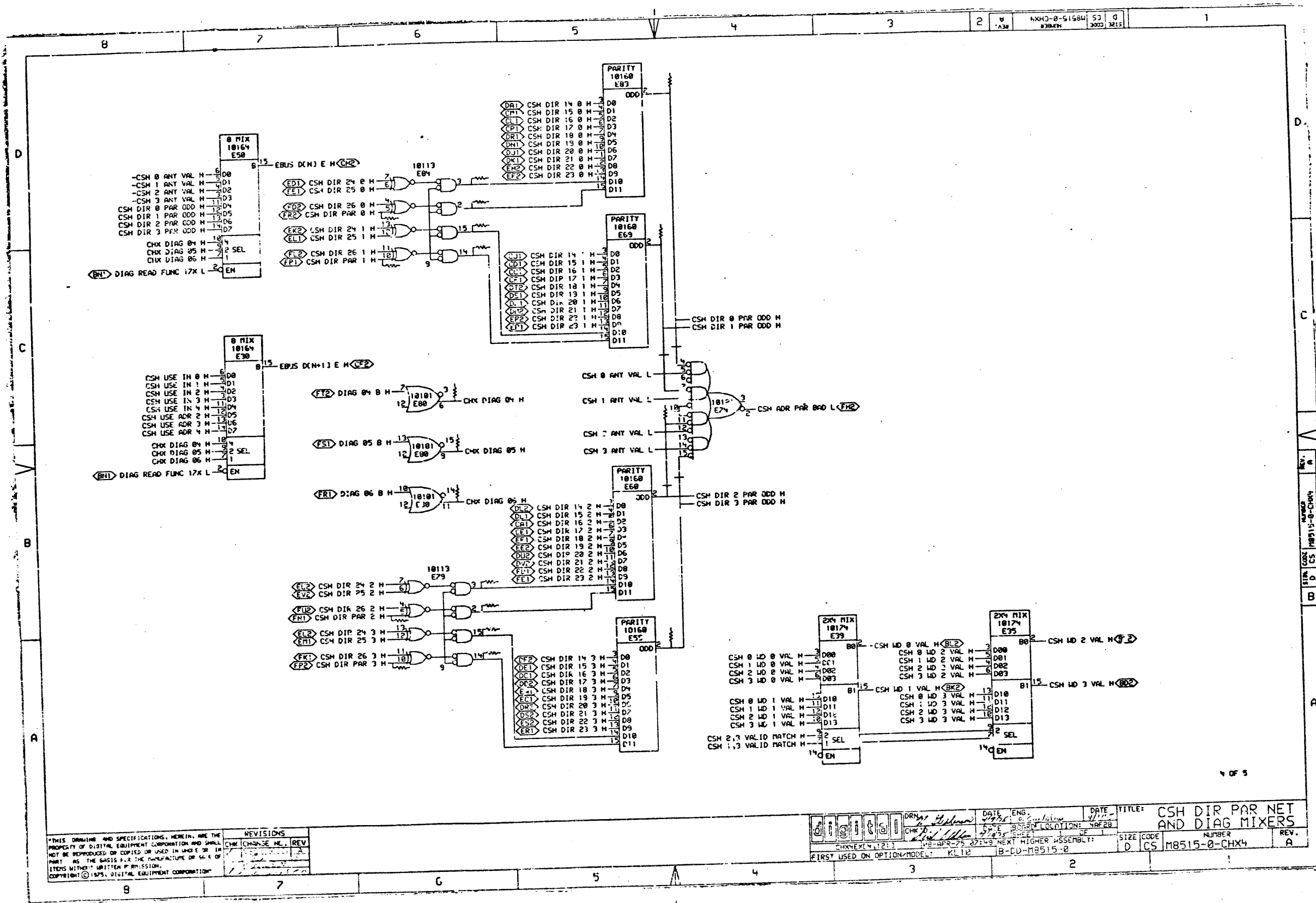


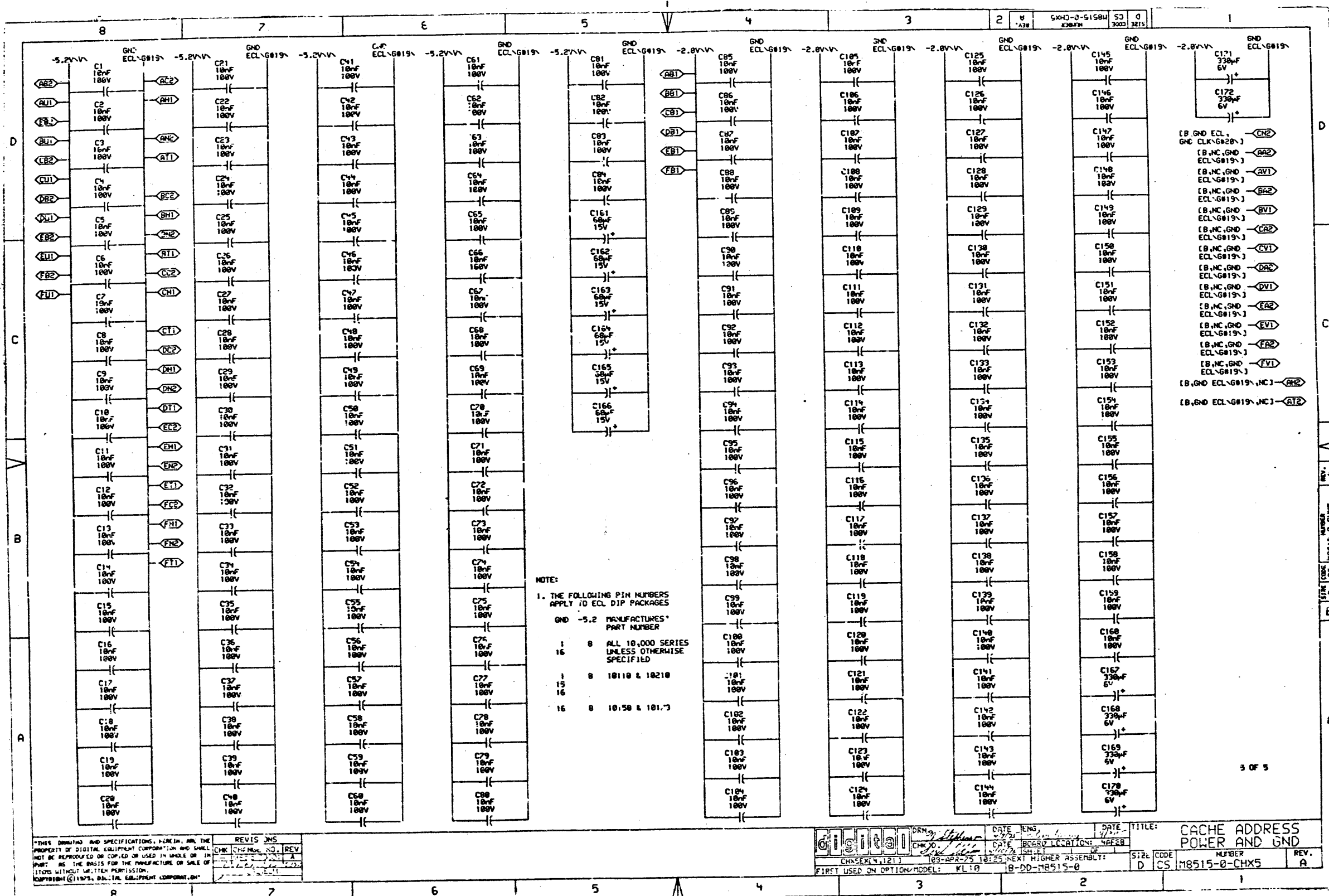












RESISTOR LOC(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R9K(1)	CHK3EX B4	68a	2E1K(15)
R3K(1)	CHK3EX B4	68a	2E1K(15)
R166(1)	CHK2EX B1	68a	2E2K(13)
R57(1)	CHK3EX A2	68a	2E2K(15)
R8K(1)	CHK3EX B3	68a	2E2K(15)
R14K(1)	CHK3EX B1	68a	2E2K(13)
R133(1)	CHK2EX A1	68a	2E30K(13)
R2K(1)	CHK3EX B6	68a	2E4K(15)
R14K(1)	CHK1EX D7	68a	2E4K(14)
R36(1)	CHK3EX C7	100a	2E4K(13)
R205(1)	CHK3EX D7	100a	2E4K(15)
R153(1)	CHK1EX D2	68a	2E4K(14)
R145(1)	CHK1EX D6	68a	2E4K(14)
R140(1)	CHK1EX D7	68a	2E31(13)
R140(1)	CHK1EX D4	68a	2E32(14)
R15K(1)	CHK1EX D2	68a	2E36(14)
R14K(1)	CHK1EX D6	68a	2E37(13)
R130(1)	CHK1EX D7	68a	2E31(13)
R146(1)	CHK1EX D4	68a	2E62(14)
R152(1)	CHK1EX D2	68a	2E65(14)
R145(1)	CHK1EX D5	68a	2E66(13)
R139(1)	CHK1EX D7	68a	2E7K(15)
R150(1)	CHK1EX D4	68a	2E7K(14)
R147(1)	CHK1EX D2	68a	2E7K(15)
R142(1)	CHK1EX D5	68a	2E7K(13)
R4K(1)	CHK4EX A6	68a	2E7K(14)
R4K(1)	CHK4EX A6	68a	2E7K(15)
R51(1)	CHK4EX B6	68a	2E7K(2)
R53(1)	CHK4EX B6	68a	2E7K(3)
R109(1)	CHK3EX B7	68a	2E80K(5)
R112(1)	CHK3EX B7	68a	2E80K(5)
R149(1)	CHK1EX D4	68a	2E81(15)
R62(1)	CHK4EX C6	68a	2E8K(14)
R51(1)	CHK4EX D6	68a	2E8K(15)
R123(1)	CHK4EX D6	68a	2E8K(2)
R127(1)	CHK4EX D6	68a	2E8K(3)
R10K(1)	CHK3EX B5	68a	2E9K(15)
R163(1)	CHK3EX D4	68a	ADR 27 A H
R113(1)	CHK3EX D4	68a	ADR 27 B H
R101(1)	CHK3EX D4	68a	ADR 27 C H

NOTE:
1. ALL TERMINATORS HAVE PIN TWO CONNECTED TO -2.0V AND ARE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED
2. ENTRIES ARE SORTED BY SIGNAL NAME
3. 2 INDICATES OUTPUT OF DIP LOC AND
(1) INDICATES PIN NUMBER

RESISTOR LOC(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R160(1)	CHK3EX D4	68a	ADR 28 A H
R111(1)	CHK3EX D4	68a	ADR 28 B H
R140(1)	CHK3EX D4	68a	ADR 28 C H
R167(1)	CHK3EX C4	68a	ADR 29 A H
R1K(1)	CHK3EX C4	68a	ADR 29 B H
R102(1)	CHK3EX C4	68a	ADR 29 C H
R170(1)	CHK3EX D3	68a	ADR 30 A H
R11(1)	CHK3EX D2	68a	ADR 30 B H
R95(1)	CHK3EX D2	68a	ADR 30 C H
R150(1)	CHK3EX D3	68a	ADR 31 A H
R5K(1)	CHK3EX D2	68a	ADR 31 B H
R91(1)	CHK3EX D2	68a	ADR 31 C H
R159(1)	CHK3EX C3	68a	ADR 32 A H
R6K(1)	CHK3EX C2	68a	ADR 32 B H
R93(1)	CHK3EX C2	68a	ADR 32 C H
R161(1)	CHK3EX D1	68a	ADR 33 A H
R4K(1)	CHK3EX D1	68a	ADR 33 B H
R9K(1)	CHK3EX D1	68a	ADR 33 C H
R202(1)	CHK3EX B7	68a	APR EN REFILL RAM LR H
R157(1)	CHK3EX B6	68a	CAN SEL 1 H
R155(1)	CHK2EX B6	68a	CAN SEL 2 H
R20K(1)	CHK4EX C6	68a	CHK DIAB 04 H
R99(1)	CHK4EX B6	68a	CHK DIAB 05 H
R23(1)	CHK4EX B5	68a	CHK DIAB 06 H
R35(1)	CHK3EX D7	68a	CLK A H
R137(1)	CHK3EX D7	68a	CLK CLK H
R203(1)	CHK2EX D1	68a	-CSH 0 ANY VAL H
R162(1)	CHK2EX D4	68a	-CSH 0 VAL LR H
R110(1)	CHK2EX C5	68a	CSH 0 LD 0 VAL H
R105(1)	CHK2EX C5	68a	CSH 0 LD 1 VAL H
R26(1)	CHK2EX C4	68a	CSH 0 LD 2 VAL H
R106(1)	CHK2EX C4	68a	CSH 0 LD 3 VAL H
R103(1)	CHK2EX D1	68a	-CSH 1 ANY VAL H
R132(1)	CHK2EX D4	68a	-CSH 1 VAL LR H
R100(1)	CHK2EX B5	68a	CSH 1 LD 0 VAL H
R107(1)	CHK2EX B5	68a	CSH 1 LD 1 VAL H
R22(1)	CHK2EX B4	68a	CSH 1 LD 2 VAL H
R10K(1)	CHK2EX B4	68a	CSH 1 LD 3 VAL H
R27(1)	CHK1EX D2	68a	CSH 1,3 VALID MATCH H
R108(1)	CHK2EX D1	68a	-CSH 2 ANY VAL H

RESISTOR LOC(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R165(1)	CHK2EX D4	68a	-CSH 2 VAL LR H
R33(1)	CHK2EX C3	68a	CSH 2 LD 0 VAL H
R3K(1)	CHK2EX C2	68a	CSH 2 LD 1 VAL H
R31(1)	CHK2EX C2	68a	CSH 2 LD 2 VAL H
R21(1)	CHK2EX C1	68a	CSH 2 LD 3 VAL H
R20(1)	CHK1EX D2	68a	CSH 2,3 VALID MATCH H
R203(1)	CHK2EX C1	68a	-CSH 3 ANY VAL H
R135(1)	CHK2EX C4	68a	-CSH 3 VAL LR H
R25(1)	CHK2EX B3	68a	CSH 3 LD 0 VAL H
R32(1)	CHK2EX B2	68a	CSH 3 LD 1 VAL H
R29(1)	CHK2EX B2	68a	CSH 3 LD 2 VAL H
R30(1)	CHK2EX B1	68a	CSH 3 LD 3 VAL H
R40(1)	CHK4EX D4	68a	CSH DIR 0 PAR ODD H
R37(1)	CHK4EX C4	68a	CSH DIR 1 PAR ODD H
R122(1)	CHK1EX C8	68a	CSH DIR 14 0 H
R67(1)	CHK1EX C6	68a	CSH DIR 14 1 H
R52(1)	CHK1EX C5	68a	CSH DIR 14 2 H
R4K(1)	CHK1EX C3	68a	CSH DIR 14 3 H
R130(1)	CHK1EX C8	68a	CSH DIR 15 0 H
R60(1)	CHK1EX C6	68a	CSH DIR 15 1 H
R53(1)	CHK1EX C5	68a	CSH DIR 15 2 H
R46(1)	CHK1EX C3	68a	CSH DIR 15 3 H
R120(1)	CHK1EX C8	68a	CSH DIR 16 0 H
R69(1)	CHK1EX C6	68a	CSH DIR 16 1 H
R5K(1)	CHK1EX C5	68a	CSH DIR 16 2 H
R47(1)	CHK1EX C3	68a	CSH DIR 16 3 H
R156(1)	CHK1EX C8	68a	CSH DIR 17 0 H
R71(1)	CHK1EX C6	68a	CSH DIR 17 1 H
R56(1)	CHK1EX C5	68a	CSH DIR 17 2 H
R50(1)	CHK1EX C3	68a	CSH DIR 17 3 H
R129(1)	CHK1EX C8	68a	CSH DIR 18 0 H
R70(1)	CHK1EX C6	68a	CSH DIR 18 1 H
R55(1)	CHK1EX C5	68a	CSH DIR 18 2 H
R40(1)	CHK1EX C3	68a	CSH DIR 18 3 H
R151(1)	CHK1EX B8	68a	CSH DIR 19 0 H
R65(1)	CHK1EX B6	68a	CSH DIR 19 1 H
R58(1)	CHK1EX B5	68a	CSH DIR 19 2 H
R116(1)	CHK1EX B3	68a	CSH DIR 19 3 H
R30(1)	CHK4EX C4	68a	CSH DIR 2 PAR ODD H
R126(1)	CHK1EX B8	68a	CSH DIR 20 0 H

RESISTOR LOC(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R66(1)	CHK1EX B6	68a	CSH DIR 20 1 H
R110(1)	CHK1EX B5	68a	CSH DIR 20 2 H
R119(1)	CHK1EX B3	68a	CSH DIR 20 3 H
R125(1)	CHK1EX B8	68a	CSH DIR 21 0 H
R6K(1)	CHK1EX B6	68a	CSH DIR 21 1 H
R57(1)	CHK1EX B5	68a	CSH DIR 21 2 H
R120(1)	CHK1EX B3	68a	CSH DIR 21 3 H
R12K(1)	CHK1EX B8	68a	CSH DIR 22 0 H
R59(1)	CHK1EX B6	68a	CSH DIR 22 1 H
R45(1)	CHK1EX B5	68a	CSH DIR 22 2 H
R41(1)	CHK1EX B3	68a	CSH DIR 22 3 H
R121(1)	CHK1EX B8	68a	CSH DIR 23 0 H
R60(1)	CHK1EX B6	68a	CSH DIR 23 1 H
R117(1)	CHK1EX B5	68a	CSH DIR 23 2 H
R4K(1)	CHK1EX B3	68a	CSH DIR 23 3 H
R87(1)	CHK1EX B8	68a	CSH DIR 24 0 H
R81(1)	CHK1EX B6	68a	CSH DIR 24 1 H
R82(1)	CHK1EX B5	68a	CSH DIR 24 2 H
R7K(1)	CHK1EX B3	68a	CSH DIR 24 3 H
R80(1)	CHK1EX B8	68a	CSH DIR 25 0 H
R79(1)	CHK1EX B6	68a	CSH DIR 25 1 H
R77(1)	CHK1EX B5	68a	CSH DIR 25 2 H
R73(1)	CHK1EX B3	68a	CSH DIR 25 3 H
R85(1)	CHK1EX A8	68a	CSH DIR 26 0 H
R8K(1)	CHK1EX A6	68a	CSH DIR 26 1 H
R75(1)	CHK1EX A4	68a	CSH DIR 26 2 H
R76(1)	CHK1EX A3	68a	CSH DIR 26 3 H
R72(1)	CHK4EX A4	68a	CSH DIR 3 PAR ODD H
R66(1)	CHK4EX D6	68a	CSH DIR PAR 0 H
R8K(1)	CHK4EX C6	68a	CSH DIR PAR 1 H
R80(1)	CHK4EX B6	68a	CSH DIR PAR 2 H
R7K(1)	CHK4EX A6	68a	CSH DIR PAR 3 H
R11(1)	CHK3EX B3	68a	-CSH REFILL RAM LR H
R114(1)	CHK3EX B7	68a	CSH SEL LRU H
R115(1)	CHK3EX C7	68a	-CSH SEL LRU H
R17(1)	CHK3EX B5	68a	CSH USE ADR 2 H
R10(1)	CHK3EX C4	68a	CSH USE ADR 3 H
R19(1)	CHK3EX C4	68a	CSH USE ADR 4 H
R7(1)	CHK3EX B4	68a	CSH USE HOLD H
R92(1)	CHK3EX C6	68a	CSH USE IN 0 H

REVISIONS		
CHK	CHANGE NO.	REV
	1	1

digital
DATE: 10-1-75
ENG: J. Smith
CHK: J. Smith
DATE: 10-1-75
LOC: 4888
TITLE: CACHE EXTENSION TERMINATORS
SIZE: D
CODE: CS
NUMBER: M8515-0-RES
REV: A
FIRST USED ON OPTION/MODEL: KL10
NEXT HIGHER ASSEMBLY: 18-DD-M8515-0

RESISTOR LOCK(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R09K(1)	CHKDEX B6	68a	CSH USE IN 1 H
R10K(1)	CHKDEX C3	68a	CSH USE IN 2 H
R24K(1)	CHKDEX C2	68a	CSH USE IN 3 H
R58K(1)	CHKDEX C1	68a	CSH USE IN 4 H
R79K(1)	CHKDEX D7	68a	CSH USE MR EN H
R109K(1)	CHKDEX D3	68a	CSH VAL SEL ALL H
R163K(1)	CHKDEX D2	68a	-CSH VAL MD 0 SEL H
R174K(1)	CHKDEX D2	68a	-CSH VAL ME 1 SEL H
R164K(1)	CHKDEX C2	68a	-CSH VAL MD 2 SEL H
R136K(1)	CHKDEX C2	68a	-CSH VAL MD 3 SEL H
R195K(1)	CHKDEX C2	68a	CSH VAL MR DATA H
R168K(1)	CHKDEX C1	1.8a	CSH VAL MR DATA A H
R191K(1)	CHKDEX C1	68a	CSH VAL MR DATA B H
R198K(1)	CHKDEX D4	68a	-CSH VAL MR PULSE H
R106K(1)	CHKDEX A3	68a	FORCE NO MATCH H
R159K(1)	CHKDEX A7	68a	FORCE VALID MATCH 0 H
R184K(1)	CHKDEX A6	68a	FORCE VALID MATCH 1 H
R185K(1)	CHKDEX A4	68a	FORCE VALID MATCH 2 H
R241K(1)	CHKDEX A3	68a	FORCE VALID MATCH 3 H
R173K(1)	CHKDEX D8	68a	PT 14 B H
R172K(1)	CHKDEX D8	68a	PT 15 B H
R171K(1)	CHKDEX D8	68a	PT 16 B H
R174K(1)	CHKDEX D8	68a	PT 17 B H
R177K(1)	CHKDEX D8	68a	PT 18 B H
R176K(1)	CHKDEX D8	68a	PT 19 B H
R175K(1)	CHKDEX D8	68a	PT 20 B H
R178K(1)	CHKDEX D8	68a	PT 21 B H
R181K(1)	CHKDEX D8	68a	PT 22 B H
R180K(1)	CHKDEX D8	68a	PT 23 B H
R179K(1)	CHKDEX D8	68a	PT 24 B H
R182K(1)	CHKDEX C8	68a	PT 25 B H
R187K(1)	CHKDEX C8	68a	PT 26 B H
R12K(1)	CHKDEX C5	68a	USE TBL IN 2 H
R13K(1)	CHKDEX C5	68a	USE TBL IN 3 H
R16K(1)	CHKDEX C5	68a	USE TBL IN 4 H
R191K(1)	CHKDEX D5	68a	VMA 27 B H
R192K(1)	CHKDEX D5	68a	VMA 28 B H
R193K(1)	CHKDEX C5	68a	VMA 29 B H
R194K(1)	CHKDEX D3	68a	VMA 30 B H
R197K(1)	CHKDEX D3	68a	VMA 31 B H

RESISTOR LOCK(PIN)	SHOWN ON DRAW REF	VALUE	TERMINATES SIGNAL
R198K(1)	CHKDEX C3	68a	VMA 32 B H
R196K(1)	CHKDEX D2	68a	VMA 33 B H
R98K(1)	CHKDEX D7	68a	-MR USE BITS A H
R96K(1)	CHKDEX C7	62a	-MR USE BITS B H

NOTE:

1. TERMINATORS HAVE PIN TWO CONNECTED TO -2.0V AND ARE 5% 1/4WATT UNLESS OTHERWISE SPECIFIED
2. ENTRIES ARE SORTED BY SIGNAL NAME
3. 2 INDICATES OUTPUT OF DIP LOC AND
- (1) INDICATES PIN NUMBER

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REVISIONS
CHG CHANGE NO. REV

digital DRN. <i>C Smith</i> DATE <i>10-2-75</i> TITLE: CACHE EXTENSION TERMINATORS	DATE <i>10-2-75</i> LOCATION: <i>44E23</i>
REVISED: <i>10-2-75</i> DATE: <i>10-2-75</i> SIZE: <i>D</i> CODE: <i>CS</i> NUMBER: <i>M8515-0-RES</i> REV: <i>A</i>	
FIRST USED ON OPTION/MODEL: <i>KL10</i> B-DD-M8515-0	