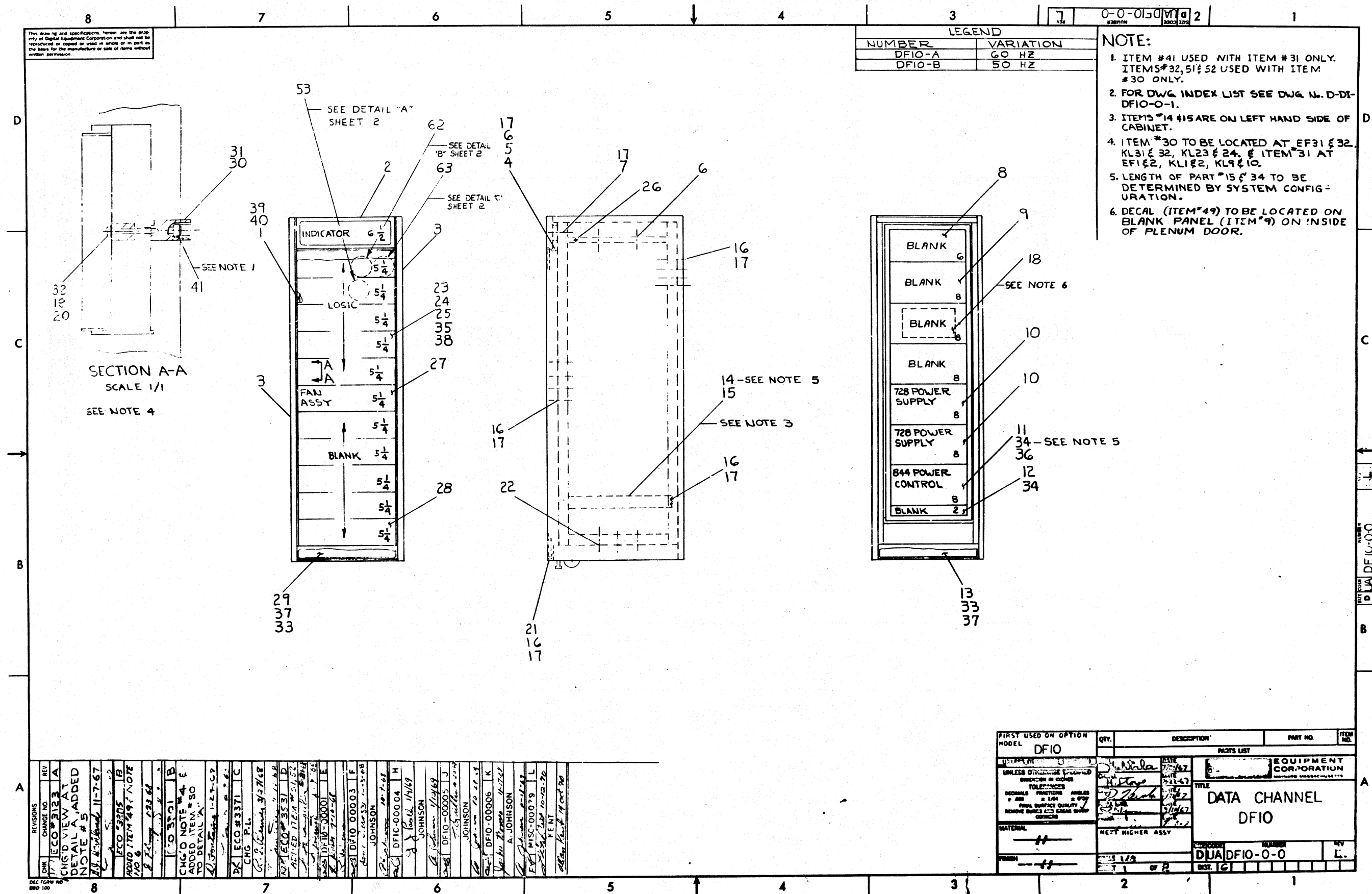


MASTER DRAWING LIST

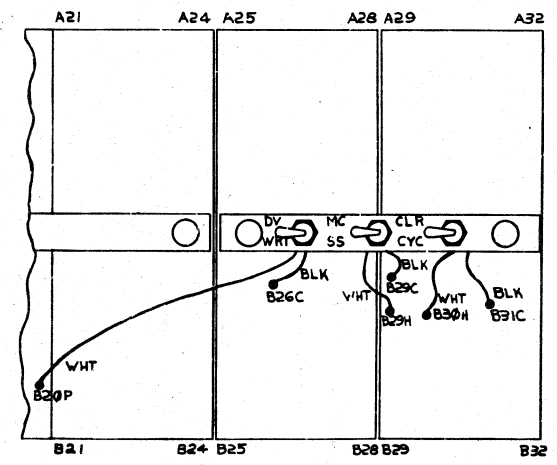
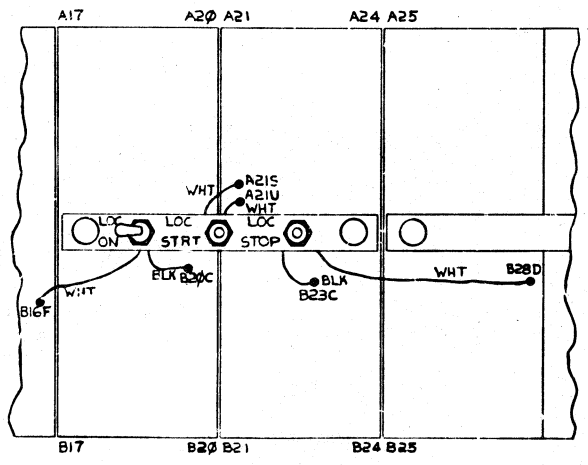
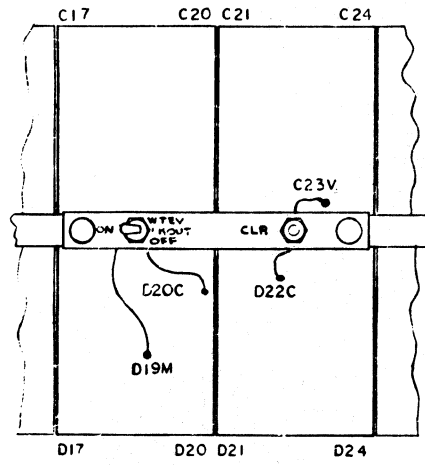
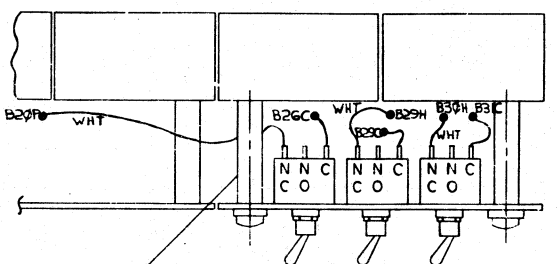
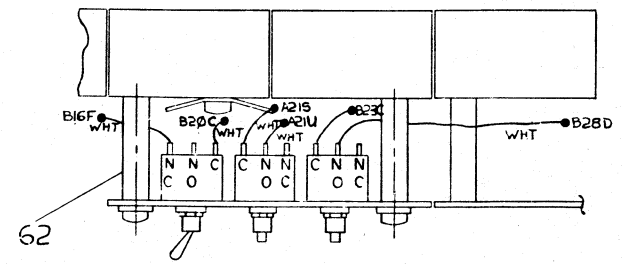
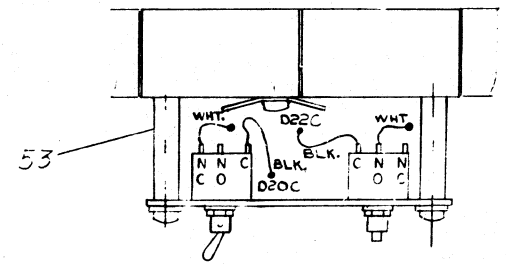
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MASTER DRAWING LIST			
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-DF10-0-0	L	2	DATA CHANNEL DF10 (60 HZ)
A-PL-DF10-0-0	L	4	DATA CHANNEL DF10 (60 HZ)
D-MU-DF10-0-3		3	MODULE UTILIZATION
A-PL-DF10-0-3		2	MODULE UTILIZATION
C-AD-7006140-0-0		1	CABLE SET DF10
D-DI-DF10-0-1	H	2	DRAWING INDEX LIST DF10
D-ES-DF10-0-CAD	A	2	ADDRESS DRIVERS CAD
D-IC-DF10-0-CBC	A	1	CHANNEL BUS CONN'S & TERMS
D-BS-DF10-0-CBL		1	DATA DISPLAY CONNECTORS
D-BS-DF10-0-CCA	A	1	DATA CHANNEL CONTROL A
D-BS-DF10-0-CCB	C	1	DATA CHANNEL CONTROL B
D-BS-DF10-0-CCC		2	DATA CHANNEL CONTROL C
D-BS-DF10-0-CCW	A	1	CONTROL WORD ADDRESS REGISTER (CCW)
D-BS-DF10-0-CDA		1	DATA ADDRESS REGISTER
D-BS-DF10-0-CIA	A	1	INITIAL ADDRESS REGISTER
D-BS-DF10-0-CPG	A	1	DATA CHAN PAR GEN
D-BS-DF10-0-MBL	A	2	MEMORY BUFFER 0-17
D-BS-DF10-0-MBR	B	2	MEMORY BUFFER 18-35
D-BS-DF10-0-WCR	A	1	WORD COUNT REGISTER
D-BS-DF10-0-TERM	A	1	SIGNAL TERMINATIONS
D-FE-DF10-0-00A	C	1	FLOW CHART A
D-FD-DF10-0-00B	C	1	FLOW CHART B MEMORY CYCLE
D-FD-DF10-0-00C	B	1	FLOW CHART C
A-WL-DF10-0-5	A	3	DF-10 CHANNEL TWISTED PAIR
A-CP-DF10-0-6	B	2	DF-10 CHANNEL
K-WL-DF10-0-2		1	WIRE LIST
A-SP-DF10-0-7		6	CHANNEL MANUFACTURING TEST PLAN OUTLINE
A-SP-DF10-0-8		4	RECOMMENDED SPARE PARTS LIST
D-IC-DF10-0-4		1	WIRING POWER DC & AC
A-SP-DF10-0-9		3	CHANNEL MFG. TEST PLAN OUTLINE (ON LINE)
D-AD-7005561-0-0			WIRED ASSY
A-PL-7005561-0-0			WIRED ASSY
REVISIONS			
REV.	DATE	CHG. NO.	APP'D.
A	2/22/68	4	A.J.
B	2/26/68	6	A.J.
C	3/68	16	A.J.
D	5/68	33	A.J.
E	7/9/68	00001	A.J.
F	7/68	00002	R.W.
H	10/68	00003	A.J.
J	1/7/69	00004	A.J.
K	10/7/69	00005	A.J.
L	10/69	00006	A.J.
M	10/70	Misc 79	A.K.
DRN. HUHTALA DATE 8/23/67			
CHK'D. DATE 4/67			
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DETAIL "A"

DETAIL "B"

DETAIL "C"

REV	CHANGE NO.	DATE
1	1	1/1/67

QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	DATA CHANNEL	DFIO	1
1	DATA CHANNEL	DFIO	2
1	DATA CHANNEL	DFIO	3
1	DATA CHANNEL	DFIO	4
1	DATA CHANNEL	DFIO	5
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1	DATA CHANNEL	DFIO	100

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY		REVISIONS		
PARTS LIST					CHANGE NO.	DATE	ENG.
ITEM NO.	DWG. NO.	DESCRIPTION	DF10-0	DF10-A			
28	B-5100	PANEL, BLANK (7402016)	5	5			
29	D-AD-7005361-2-0	DOOR FRONT (ASSY)	1	1			
30	C-MD-7408446-2-0	BLOCK, RET, UNIVERSAL, REWORK	3	3			
31	C-MD-7408446-1-0	BLOCK, RET, UNIVERSAL, REWORK	3	3			
32	9006029-1	SCR PHL HD PAN #6-32 x 1 1/2 SST	3	3			
33	9006633	WASH, INT TOOTH #6	4	4			
34		CORD, 25' #1202980 OR 9' #1201265	1	1			
35	D-IA-7005459-12-0	CABLE W012-W250	1	1			
36	C-AD-7005427-0-0	CABLE TWIST LOCK 25'	1	1			
37	90-06020-1	SCR PHL HD PAN #6-32 x 1/2 SST	4	4			
38	90-06507	POP RIVET 1/8D #AD44ABS USMC	20	20			
39		CLAMP NYLON #CPC1953-16B (1" DIA)	A/RA/R				
40		CLAMP NYLON #CPC1953-6B (3/8" DIA)	A/RA/R				
41	9007799	SCR PHL FILL HD 8-32 x 1-1/2 LG	3	3			
MADE BY A. HUHTALA		DATE 7/31/67	TITLE DATA CHANNEL DF10		DRWG. NO. A-PL- DF10-0-0		REV. LTR.
CHECKED H. Stowe		DATE 8-30-67	FOR DF10-0 (60 HZ) DF10-A (50 HZ)		ASSY NO D-UA-DF10-0-0		SHEET 3 OF 5
ENG D. Plumb		DATE 9/1/67					L

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY		REVISIONS		
PARTS LIST					CHANGE NO.	DATE	ENG.
ITEM NO.	DWG. NO.	DESCRIPTION	DF10-0	DF10-A			
1	E-IA-7406273-0-0	CAB. FRAME (REWORK)	1	1			
2	D-AD-7005535-0-0	PANEL INDICATOR ASSY	1	1			
3	E-IA-7405092-0-0	END PANEL ASSY	2	2			
4	A-MD-7405860-0-0	SPACER	1	1			
5	B-MD-7405861-0-0	BRACKET (DOOR PIVOT)	1	1			
6	90-06350	SCR, SOC HD CAP #10-32 x 1" SST	6	6			
7	90-06083-1	SCR, PHL PAN #10-32 x 2 1/2 SST	2	2			
8	B-5111	PANEL, BLANK #7402035	1	1			
9	B-5111	PANEL, BLANK #7402036	3	3			
10	D-MA-728A-0-1	POWER SUPPLY #728A		2			
10	D-MA-728-0-1	POWER SUPPLY #728		2			
11	D-UA-844-0-0	POWER CONTROL #844	1	1			
12	B-5111	PANEL, BLANK #7402033	1	1			
13	D-AD-7005358-2-0	DOOR, FULL ASSY	1	1			
MADE BY A. HUHTALA		DATE 7/31/67	TITLE DATA CHANNEL DF10		DRWG. NO. A-PL- DF10-0-0		REV. LTR.
CHECKED H. Stowe		DATE 8-30-67	FOR DF10-0 (60 HZ) DF10-A (50 HZ)		ASSY NO D-UA-DF10-0-0		SHEET 1 OF 5
ENG D. Plumb		DATE 9/1/67					L

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY		REVISIONS		
PARTS LIST					CHANGE NO.	DATE	ENG.
ITEM NO.	DWG. NO.	DESCRIPTION	DF10-0	DF10-A			
14	D-AD-7005467-0-0	BRACKET, POWER CONN (ASSY)	1	1			
15	C-UA-BC10B-0-0	MC, CABLE/REMOTE CONT.	1	1			
16	90-06073-3	SCR PHL HD TRUSS #10-32 x 1/2 SST	106	106			
17	90-06635	WASH, EXT TOOTH #10 SST	110	110			
18	B-DC-7406500-0-0	DECAL - DF10	1	1			
19	9006659	WASH, FLAT #6	3	3			
20	9007801	WASH, SPLIT LOCK #6	3	3			
21	D-MD-7405862-0-0	TRIM STRIP BOTTOM	1	1			
22	90-06346	SCR, SOC HD CAP #10-32 x 1/2	4	4			
23	D-AD-7005561-0-0	WIRED ASSEMBLY	1	1			
24	C-MD-5302486-0-0	PLATE, RIGHT END (5302486)	5	5			
25	C-IA-5402526-0-0	PANEL MARGINAL CHECK	5	5			
26	90-07073	CLAMP, CAB-L-TITE #2C1-150 DAKOTA	A/RA/R				
27	E-AD-7005474-0-0	HOUSING PAN ASSY	1	1			
MADE BY A. HUHTALA		DATE 7/31/67	TITLE DATA CHANNEL DF10		DRWG. NO. A-PL- DF10-0-0		REV. LTR.
CHECKED H. Stowe		DATE 8-30-67	FOR DF10-0 (60 HZ) DF10-A (50 HZ)		ASSY NO D-UA-DF10-0-0		SHEET 2 OF 5
ENG D. Plumb		DATE 9/1/67					L

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				PARTS LIST				QUANTITY				REVISIONS		
ITEM NO.	DWG. NO.	DESCRIPTION	DF10-0	DF10-A								CHANGE NO.	DATE	ENG.
42	90-60534	WAGON INT. TYPING #0	2	2										
43		SWITCH #0011-12 MICRO #12-1103	1	1										
44		SWITCH #0013-0701 MICRO #12-1037	1	1										
45	91-19-7006025-0-0	WIRE SWITCH MAINTENANCE	1	1										
46		SPACER #0-02-1/2 X 1/4 X 1-1/2-1/16	2	2										
47	90-60535-1	BUK TUBE #100-0-32 X 1-1/2-1/16	2	2										
48	90-60534-0-0	SCREWSCREWS-DF10	1	1										
49	90-60534-0-0	SCREW-DF10	1	1										
50	90-60700	WAGON 1/8-0-18 X 1/4 X 1-1/2-1/16-1/16	2	2										
51	90-60534	WAGON, 1/16 X 1/4	3	3										
52	90-60534	WAGON, 1/16 X 1/4	3	3										
53	C-AD-7005899-0-0	MAINT. SWITCH ASS'Y #1	1	1										
54	D-IA-7005459-11-0	CABLE W012-W250	1	1										
55	D-IA-7005459-6-0	" " "	2	2										
MADE BY A. HUTHALA			DATE 7/31/67			TITLE DATA CHANNEL DF10			DRWG. NO. A-PL-DF10-0-0			REV. LTR.		
CHECKED			DATE 9/12/67			FOR DF10-0 (60 HZ) DF10-A (50 HZ)			ASSY NO D-UA-DF10-0-0			SHEET 4 OF 5		
ENG			DATE 9/12/67									L		

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				PARTS LIST				QUANTITY				REVISIONS		
ITEM NO.	DWG. NO.	DESCRIPTION	DF10-0	DF10-A								CHANGE NO.	DATE	ENG.
56	D-IA-7005459-9-0	CABLE W012 - W250	1	1										
57	D-IA-7005459-5-0	" " "	2	2										
58	D-IA-7005459-10-0	" " "	1	1										
59	D-IA-7005459-8-0	" " "	1	1										
60	D-IA-7005459-4-0	" " "	1	1										
61	D-IA-7005459-7-0	" " "	1	1										
62	C-AD-7006560-0-0	MAINT. SWITCH ASS'Y #2	1	1										
63	C-AD-7006561-0-0	MAINT. SWITCH ASS'Y #3	1	1										
REF	C-AD-7006140-0-0	CABLE SET DF10	-	-										
MADE BY S. Pardo			DATE 1/9/69			TITLE DATA CHANNEL DF10			DRWG. NO. A-PL-DF10-0-0			REV. LTR.		
CHECKED			DATE			FOR DF10-0 (60 HZ) DF10-A (50 HZ)			ASSY NO D-UA-DF10-0-0			SHEET 5 OF 5		
ENG			DATE									L		

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PARTS LIST			DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE ENG.			
		3	DIODE NETWORK	R001	A-16	3-28-67			
		9	DC CARRY CHAIN	R181	B-33	5-20-68			
		27	FLIP FLOP (QUAD)	S202	C-DF10-00006	11-11-67			
		3	PULSE AMPLIFIER	R613					
		5	INTE. GRATING ONE SHOT	R303					
		22	PULSE BUS TRANSCEIVER	W102					
		1	DELAY LINE	W301					
		3	DIODE GATE	B137					
		11	DIODE GATE	B135					
		11	TAPPED DELAY LINE	B311					
		12	PULSE AMPLIFIER	B611					
		14	INVERTER	B165					
		23	DIODE GATE	B133					
		15	FLIP FLOP	B214					
		5	DUAL R S FLIP FLOP	B212					
		2	DIODE GATE	B134					
MADE BY EUTALIA		DATE 8/2/67	TITLE		SIZE CODE	NUMBER	REV.		
		DATE 10-9-67	MODULE LIST		A PL	DF10-0-3	C		
		DATE 11/5/68	FOR		ASSY. NO.	D-MU-DF10-0-3	SHEET 1 OF 2		

PARTS LIST			DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS				REVISIONS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.	CHANGE NO.	DATE ENG.			
		22	DIODE GATE	B163					
		18	3-BIT PARITY CIRCUIT	B130					
		11	BUS DRIVER	B683					
		3	DIODE GATE DRIVER	B685					
		14	2 MA LEVEL TERMINATOR	G704					
		1	PULSE AMPLIFIER	S603					
		1	BLANK MODULE	W990					
		1	SCHMITT TRIGGER	W501					
		6	CABLE TERMINATOR	G700					
MADE BY EUTALIA		DATE 8/2/67	TITLE		SIZE CODE	NUMBER	REV.		
		DATE 11-8-67	MODULE LIST		A PL	DF10-0-3	SC		
		DATE 11/5/68	FOR		ASSY. NO.	D-MU-DF10-0-3	SHEET 2 OF 2		

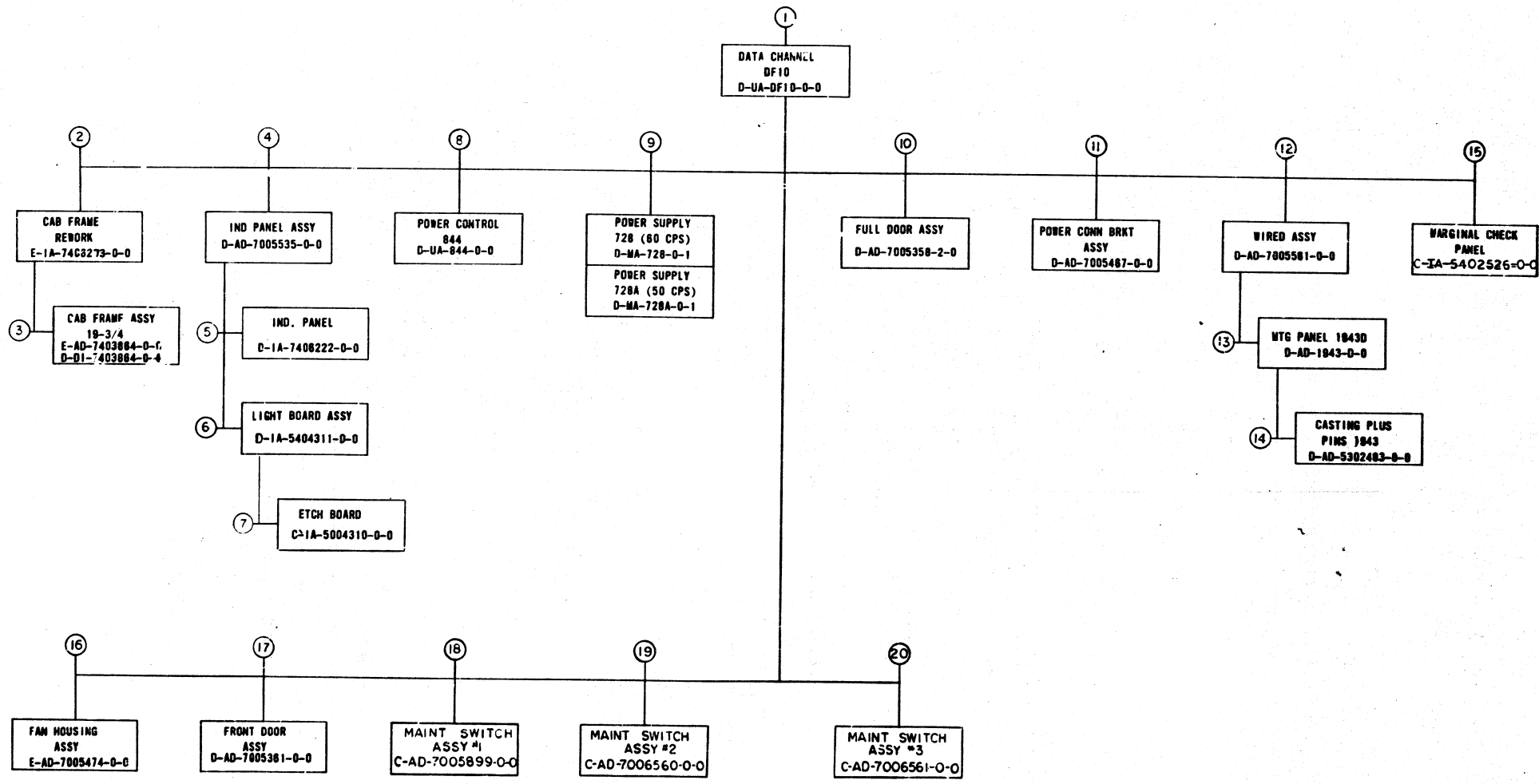
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PARTS LIST ITEM NO.	MARK END	CONN TYPE	TO	CONN TYPE	MARK END	LENGTH	PART NO./DWG NO.
35	Z30	W250	—	W012	F5	56-1/2	7005459-12
54	Z31	↑	—	↑	H3	52-1/2	11
55	Z32	↑	—	↑	C2	39-1/2	6
57	Z33	↑	—	↑	D1	37	5
58	Z20	↑	—	↑	F4	49-1/2	10
59	Z21	↑	—	↑	H2	44-1/2	8
57	Z22	↑	—	↑	C1	37	5
56	Z10	↑	—	↑	F3	47-1/2	9
55	Z11	↑	—	↑	H1	39-1/2	6
60	Z12	↓	—	↓	C29	34	4
61	Z13	W250	—	W012	D32	42-1/2	7005459-7

REVISIONS		REV.
CHK	CHANGE NO.	
—	CRIG. DFIO-00004	—
—	DFIO-00005	A
—	7-23-69	
—	JOHNSON	
—	10-28-61	

FIRST USED ON OPT/MOD. DFIO		QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED		PARTS LIST			
UNLESS OTHERWISE SPECIFIED		EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			
DIMENSION IN INCHES		TITLE CABLE SET DFIO			
TOLERANCES		CODE 7006140-0-0			
DECIMALS FRACTIONS ANGLES		REV. A			
± .005 ± 1/64 ± 0°30'		C			
FINAL SURFACE QUALITY		D-U-A-DFIO-0-0			
REMOVE BURRS AND BREAK SHARP		SCALE —H—			
CORNERS		CUT 1 OF 1			
MATERIAL		D-U-A-DFIO-0-0			
FINISH		CUT 1 OF 1			

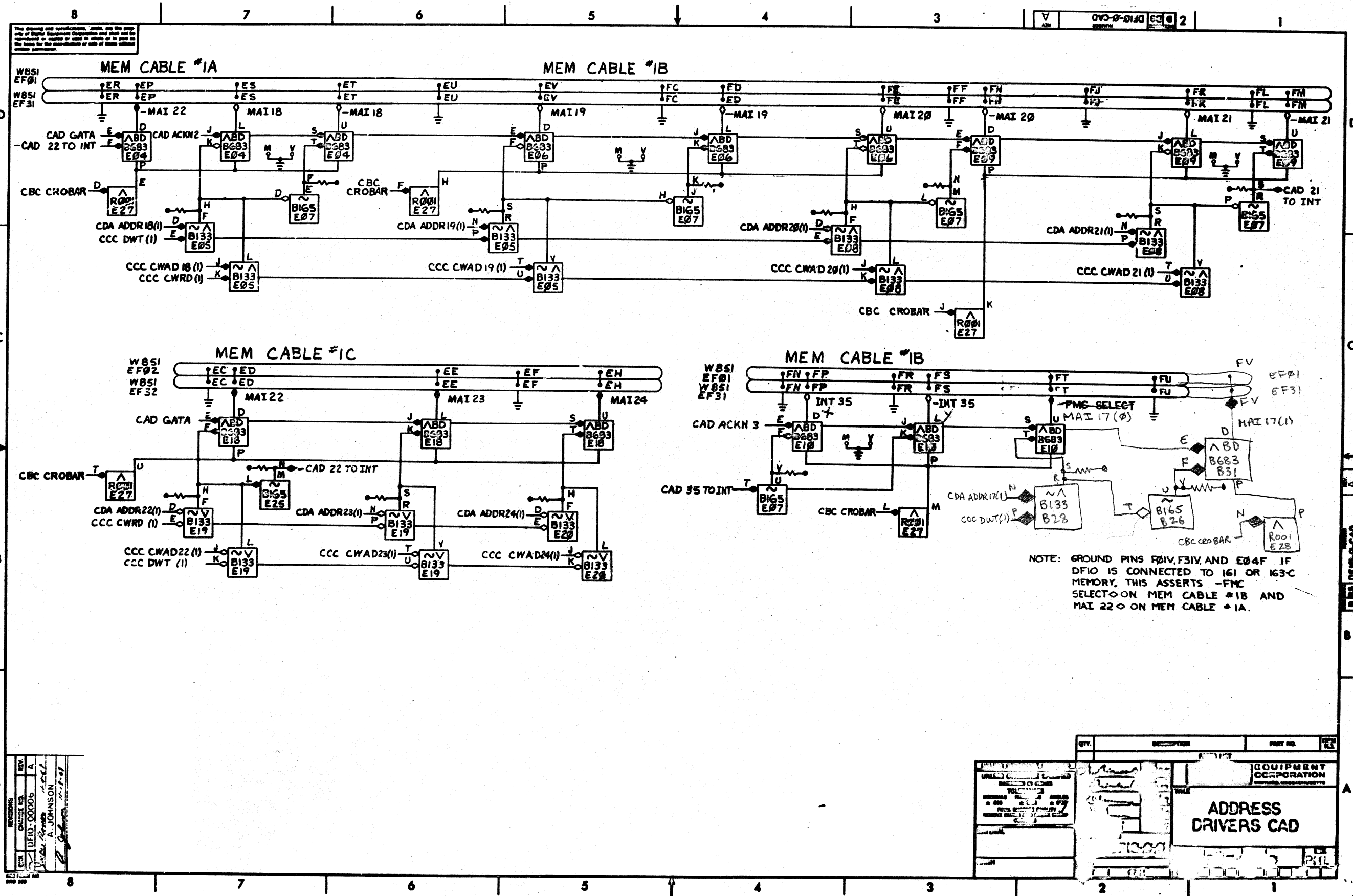
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REV	DATE	BY	CHKD	APPD	DESCRIPTION
1	11-7-67	W. J. ...			...
2	11-8-67	...			...
3	11-16-67	...			...
4	11-16-67	...			...
5	11-16-67	...			...
6	11-16-67	...			...
7	11-16-67	...			...
8	11-16-67	...			...
9	11-16-67	...			...
10	11-16-67	...			...
11	11-16-67	...			...
12	11-16-67	...			...
13	11-16-67	...			...
14	11-16-67	...			...
15	11-16-67	...			...
16	11-16-67	...			...
17	11-16-67	...			...
18	11-16-67	...			...
19	11-16-67	...			...
20	11-16-67	...			...

ASSEMBLY DWG NO. D-UA-DF10-0-0

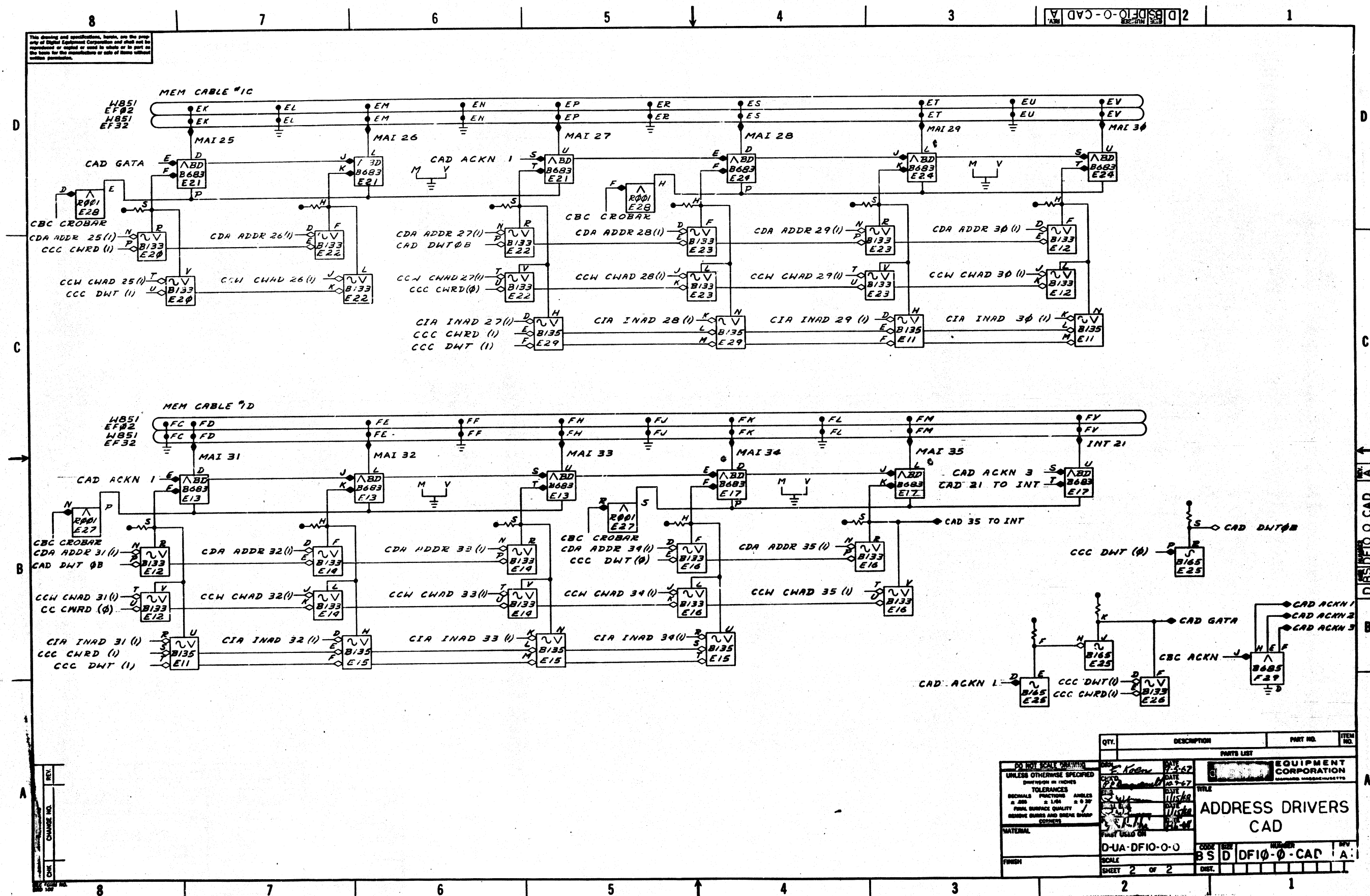
FIRST USED ON OPTION/ MODEL DF10		QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES HOLE POSITIONAL TOLERANCE HOLE POSITIONAL TOLERANCE		DATE 11-16-67 BY W. J. ... CHKD ...		EQUIPMENT CORPORATION DRAWING INDEX LIST DF10	
DRAWN BY W. J. ... CHECKED BY ...		DATE 11-16-67 BY W. J. ... CHKD ...		REV D DI DF10-0-1 M.C.	



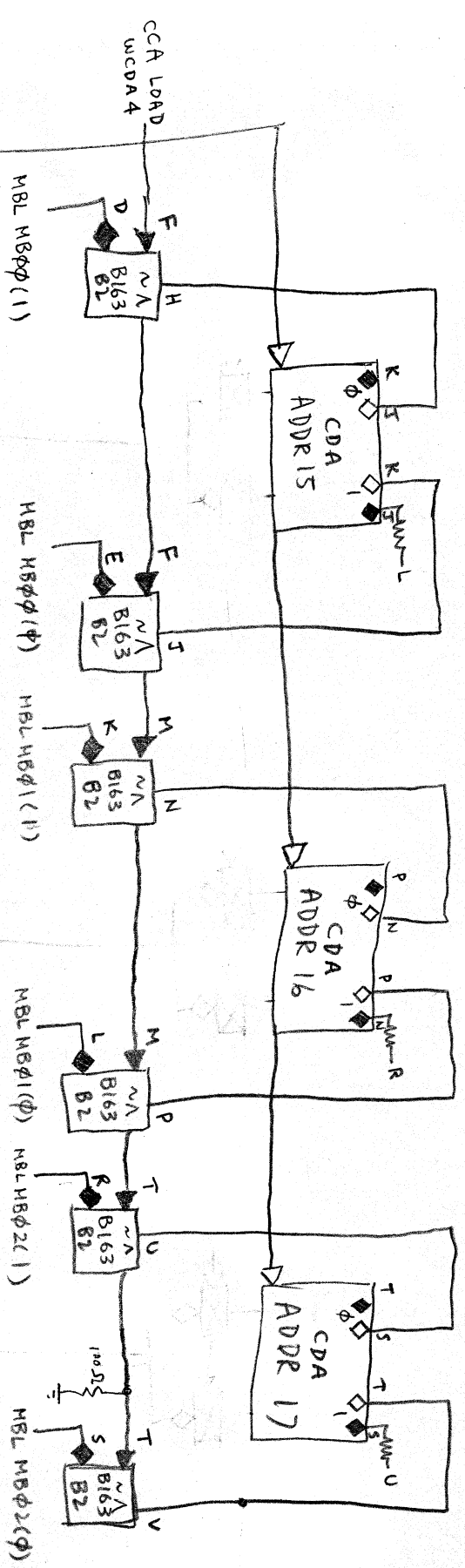
REV	DATE	BY	CHKD
1	10-1-68	A. JOHNSON	
2	10-1-68	A. JOHNSON	

QTY	DESCRIPTION	PART NO.	REV
1	ADDRESS DRIVERS CAD		

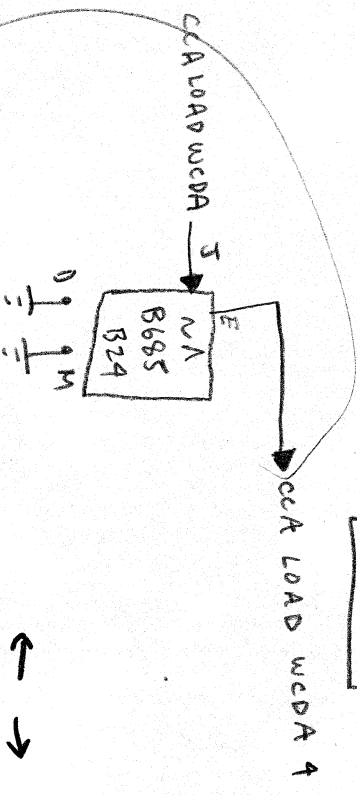
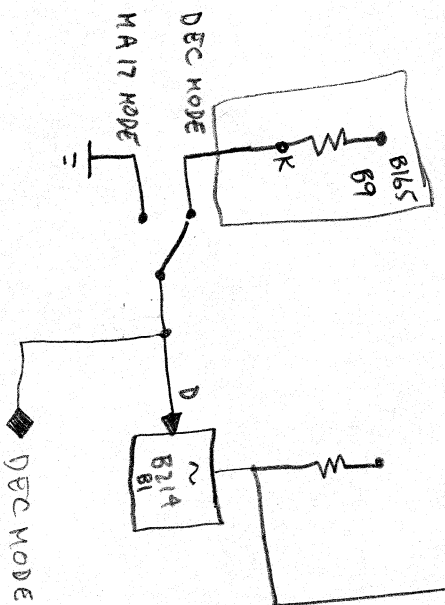
EQUIPMENT CORPORATION
CHICAGO, ILLINOIS 60606



B214 B1

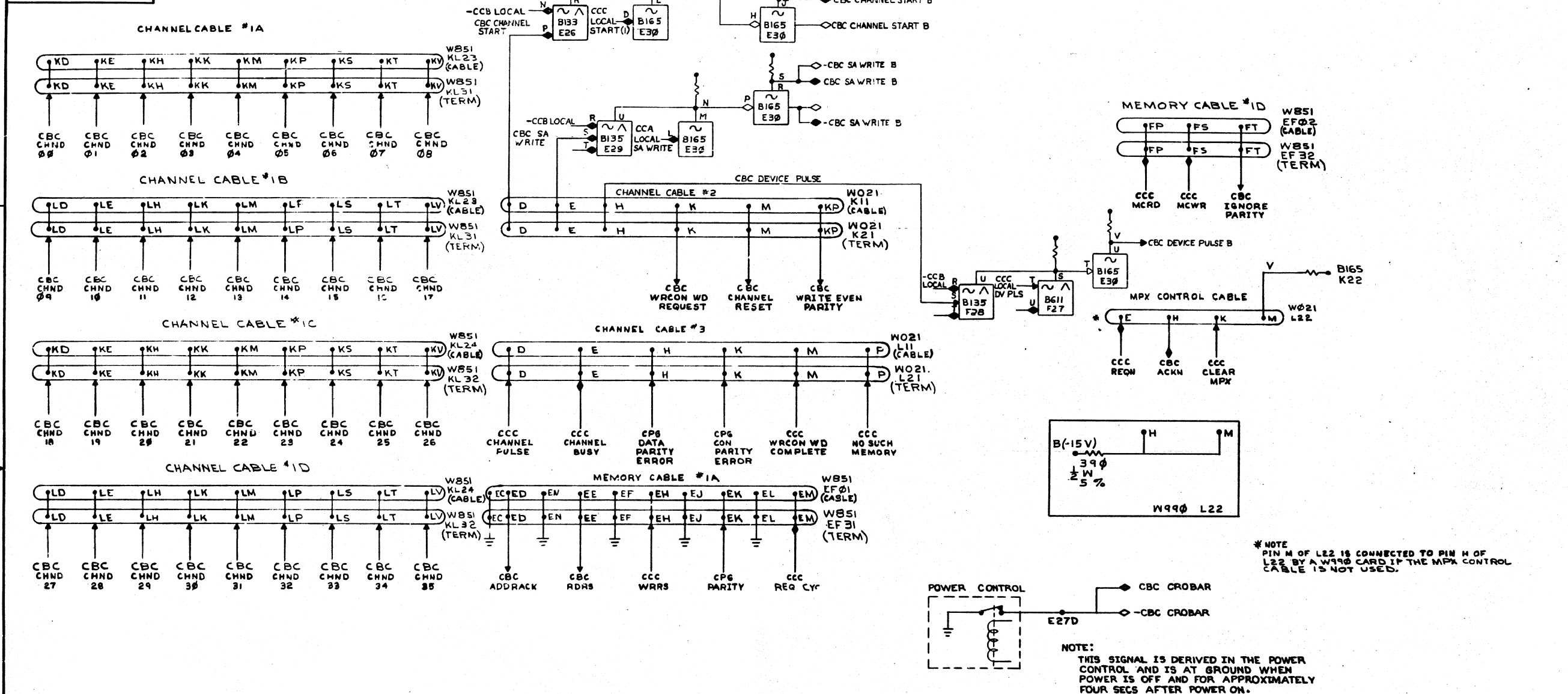


delete ground on F01V - F31V BUS



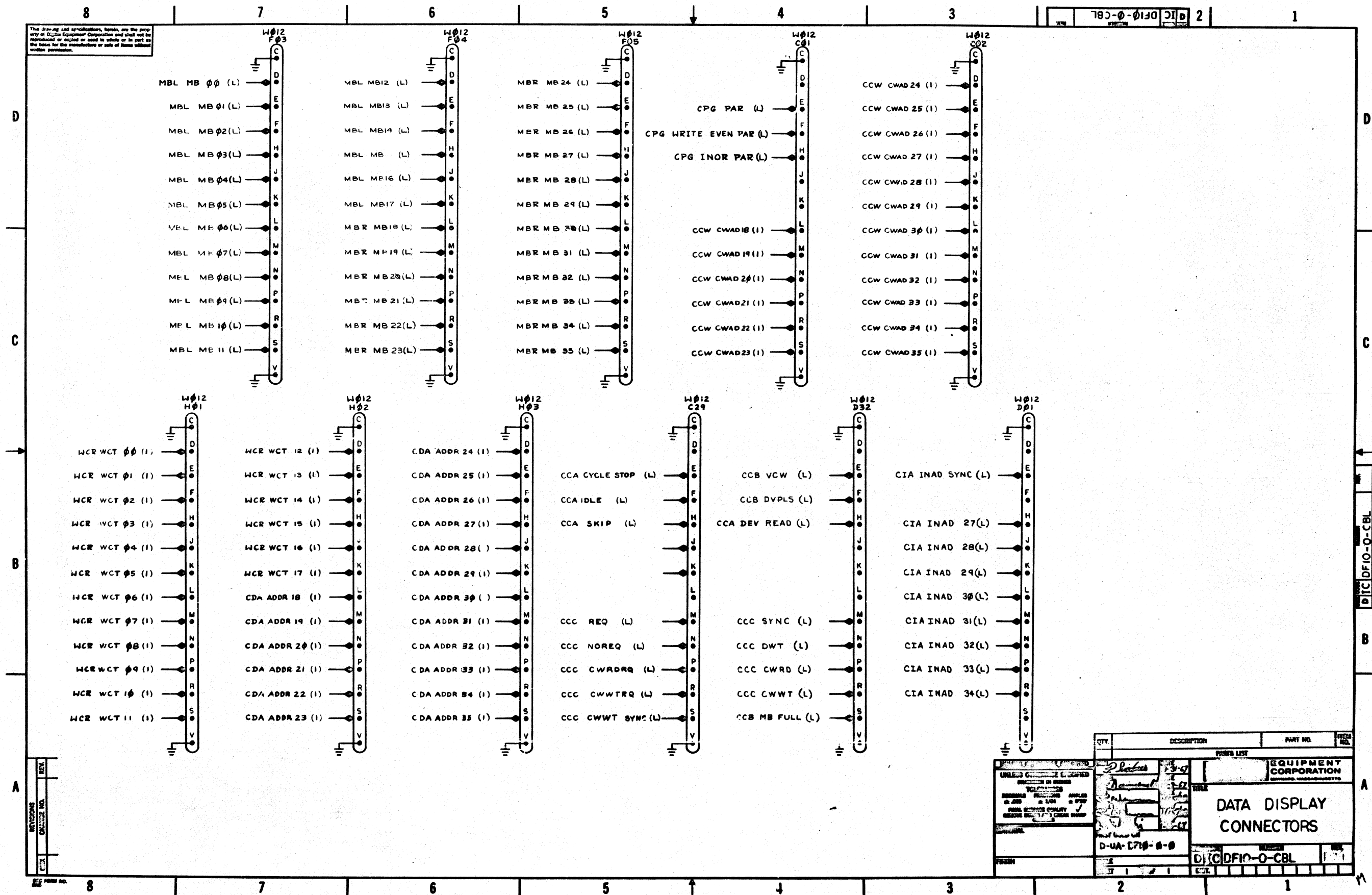
← MAIN
→ DEC

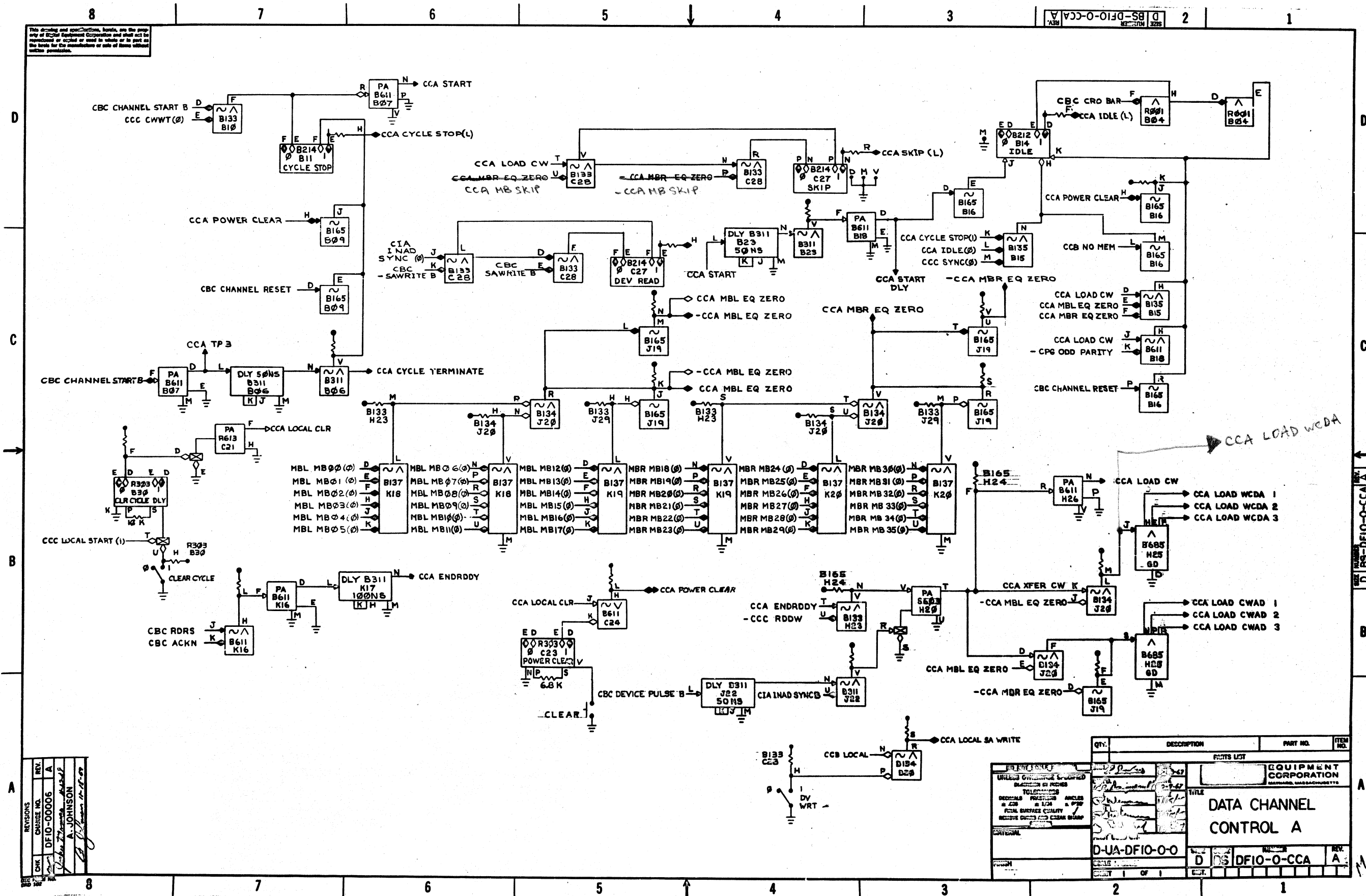
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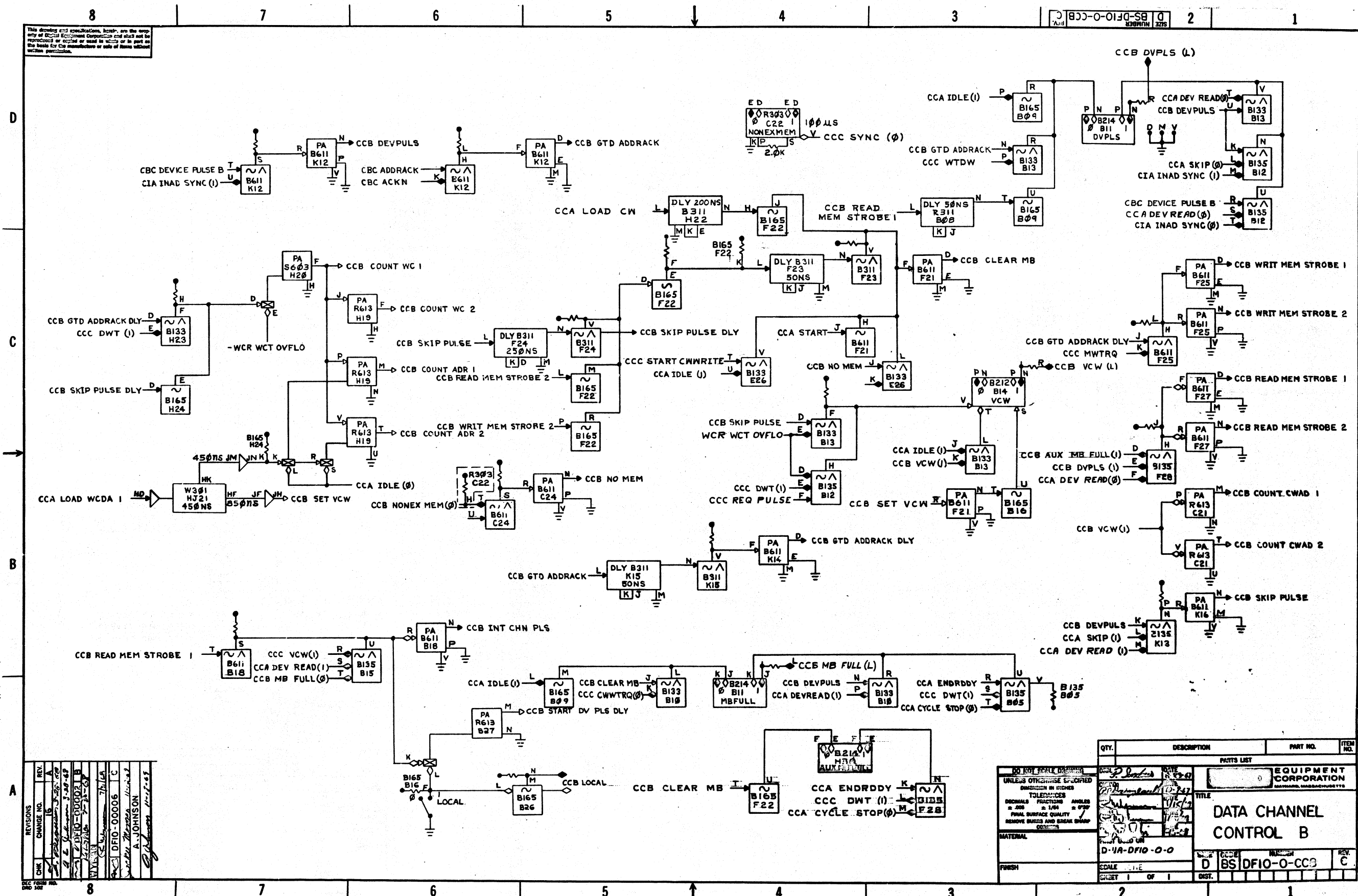


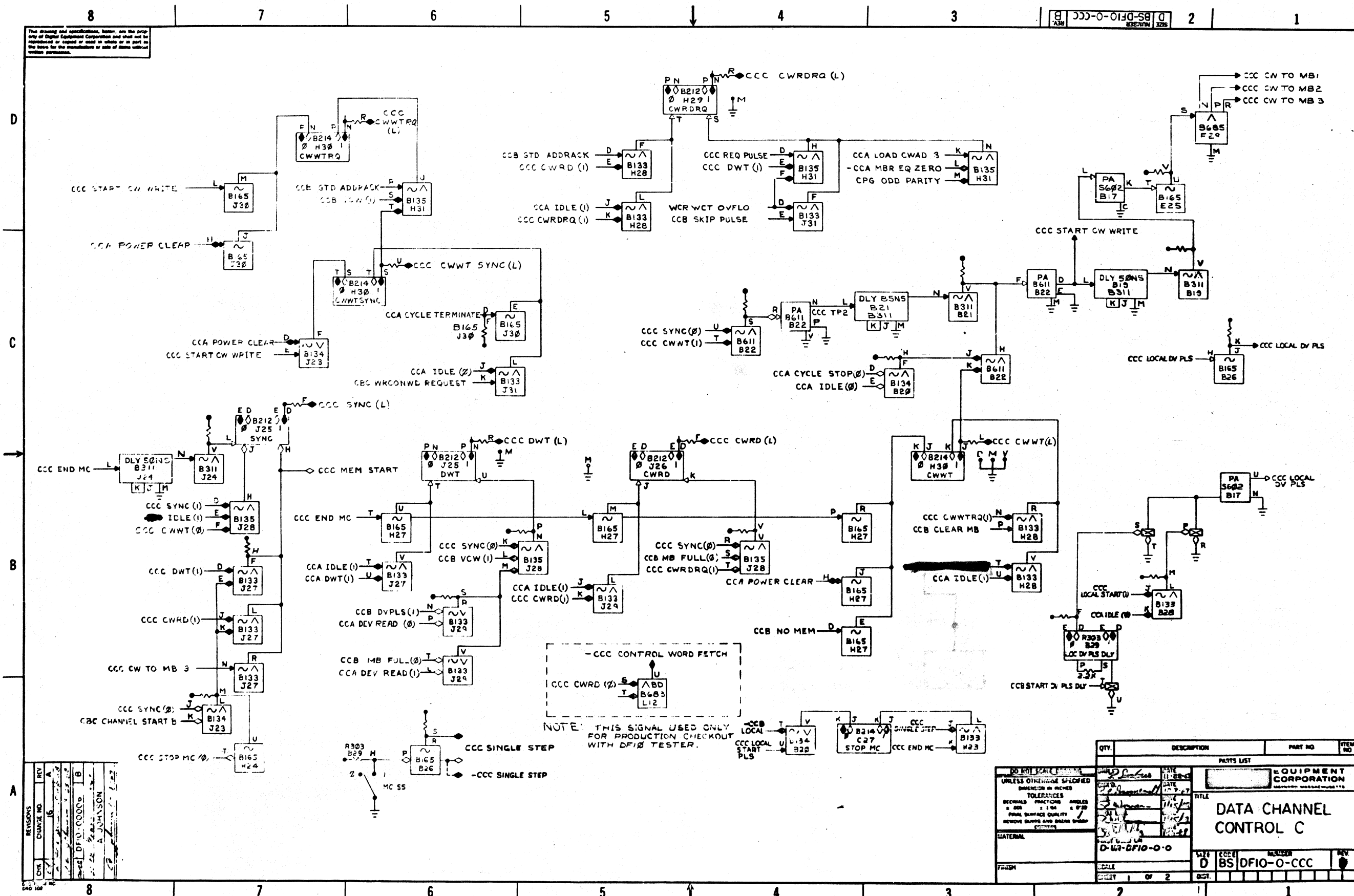
REV.	CHG.	NO.	DATE	BY	CHK.
1	1	1	11/15/68	A. JOHNSON	
2	2	2	11/15/68	A. JOHNSON	

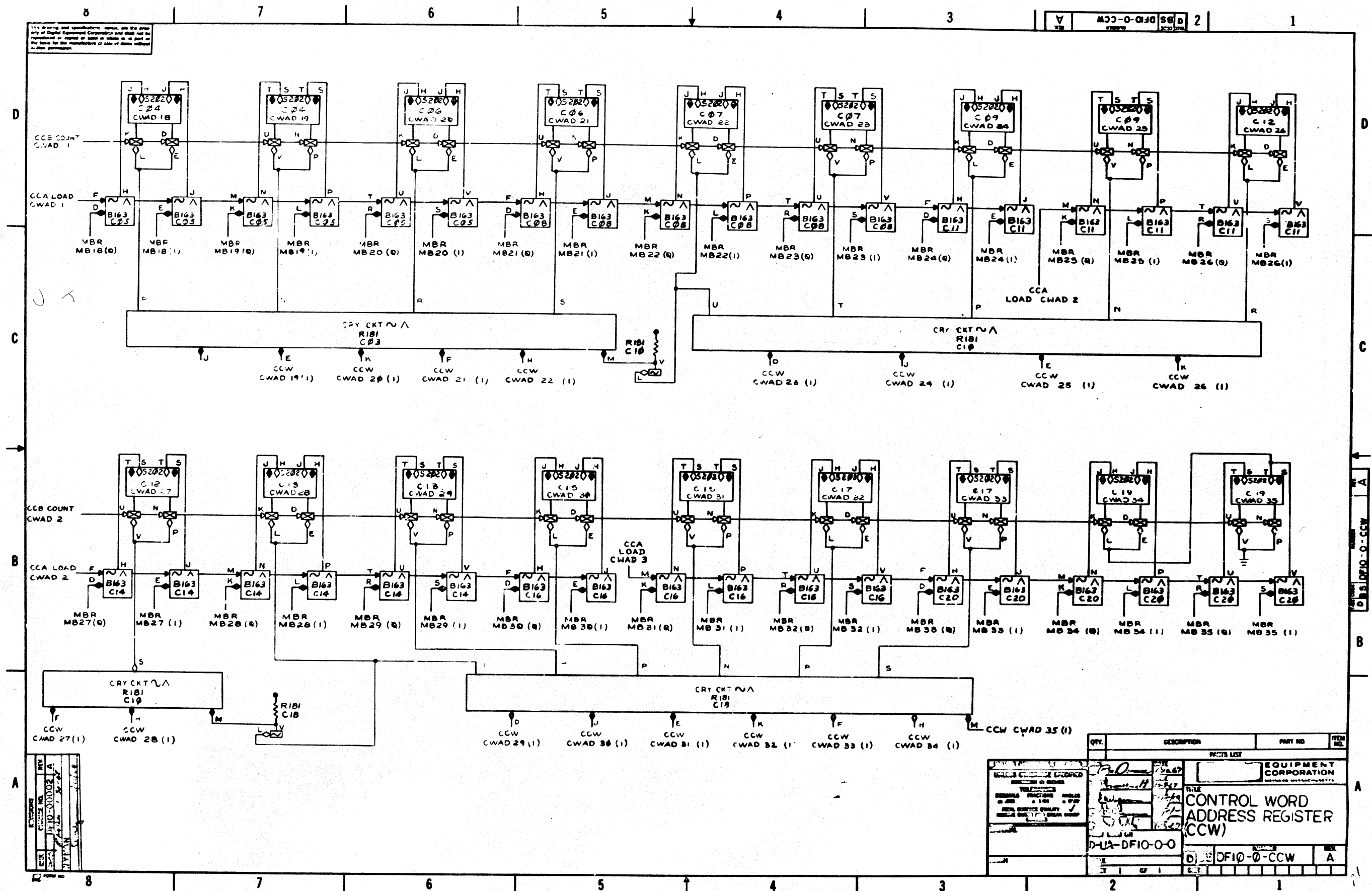
QTY.	DESCRIPTION	PART NO.	ITEM NO.
1	CHANNEL BUS CONN'S & TERM'S	D-IG-DFI0-0-CBC	A
1	CHANNEL BUS CONN'S & TERM'S	D-IG-DFI0-0-CBC	A

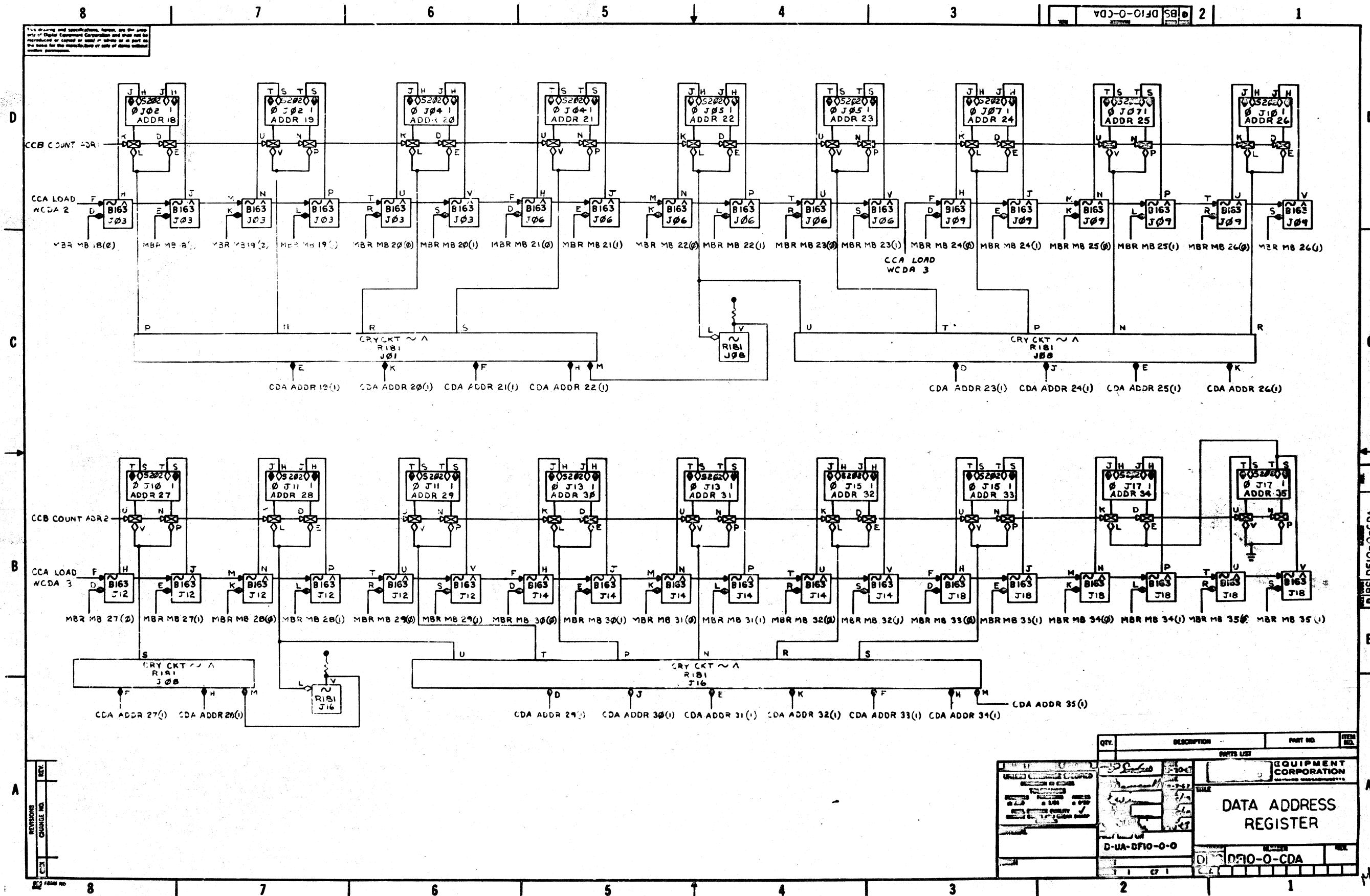


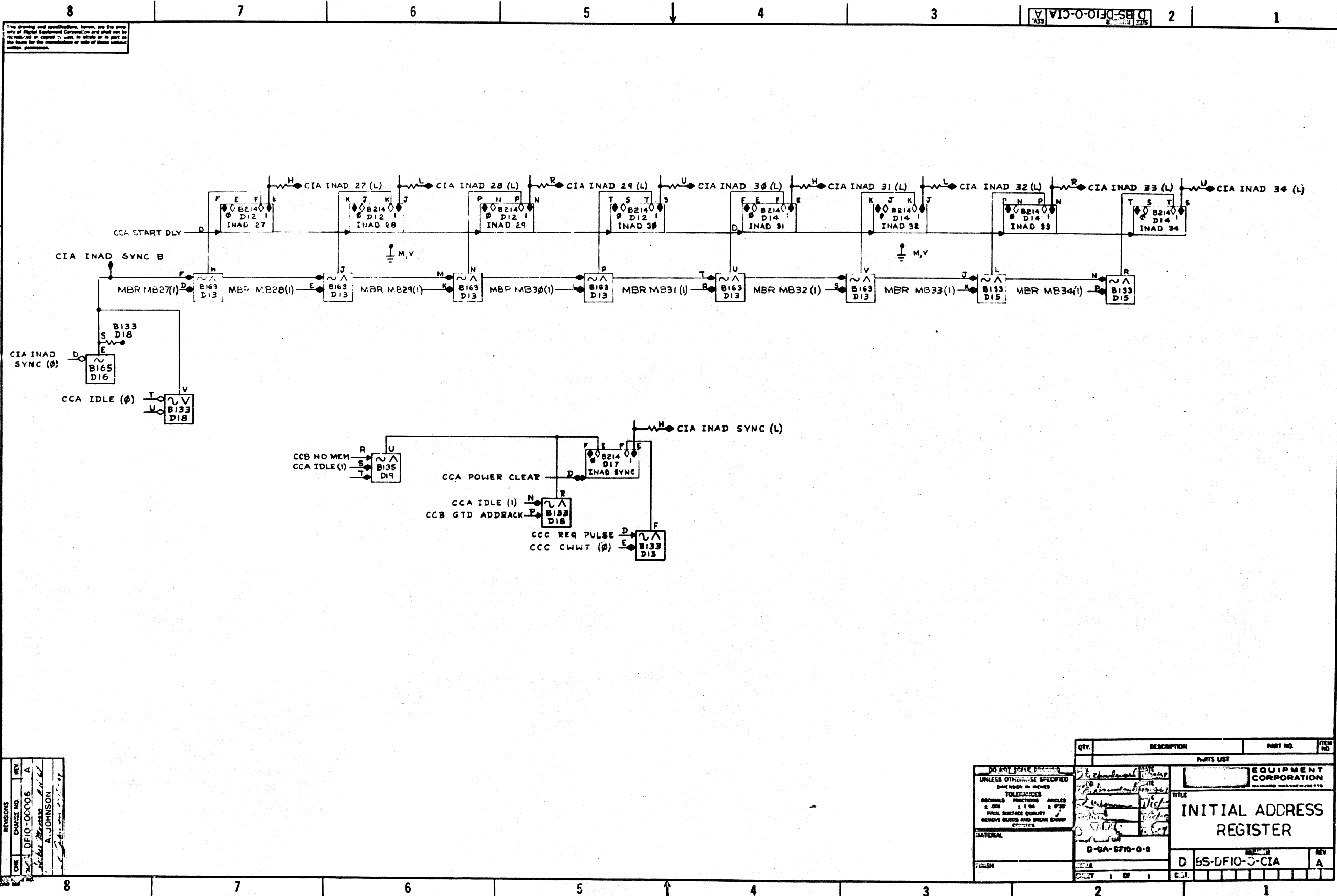










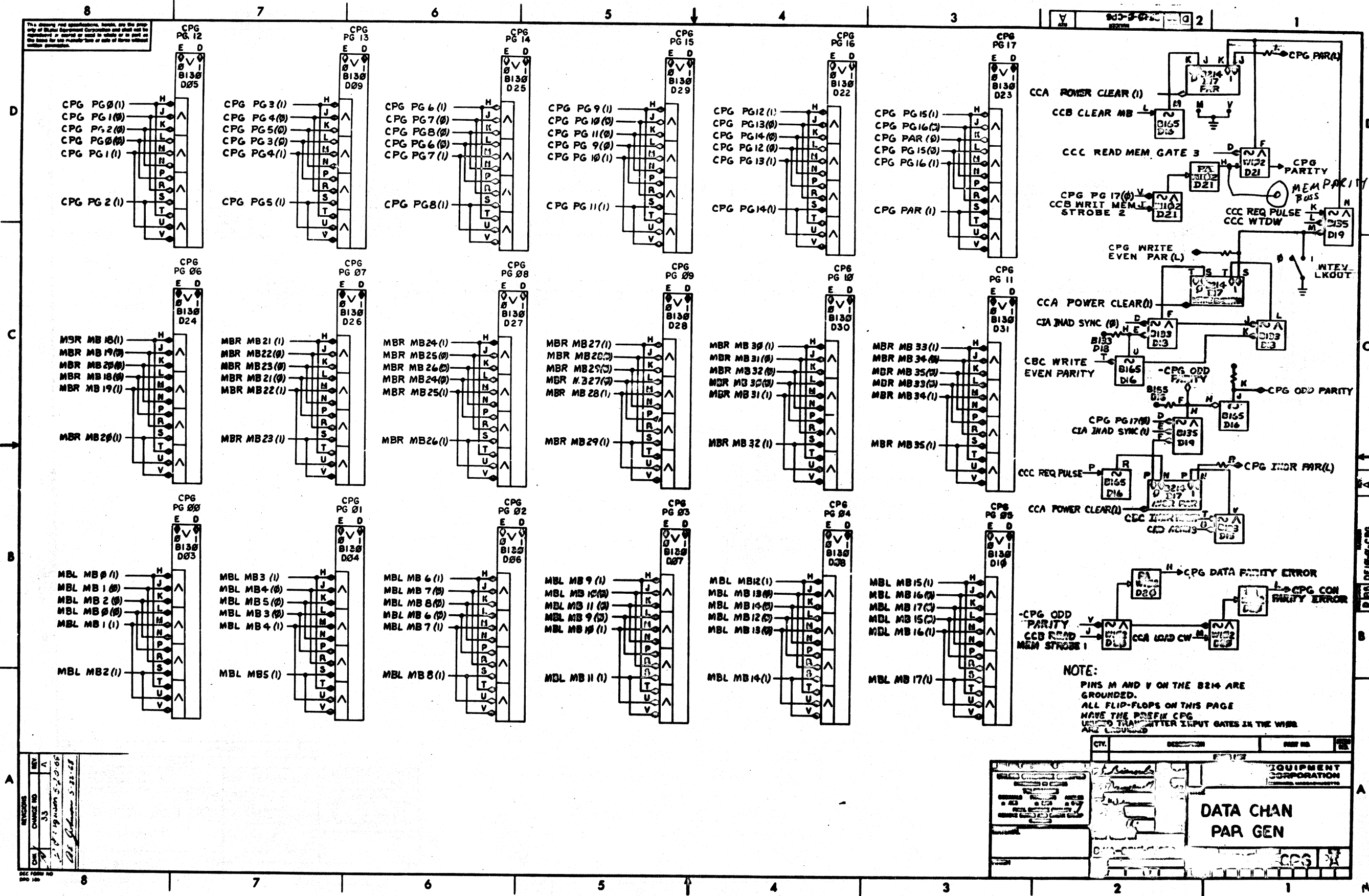


D-BS-DFIO-0-CIA

A

REVISIONS	DATE	BY	REV
1	10-1-66	A. JOHNSON	A

QTY.		DESCRIPTION	PART NO.	ITEM NO.
EQUIPMENT CORPORATION				
TITLE				
INITIAL ADDRESS REGISTER				
D-BS-DFIO-0-CIA				
REV A				

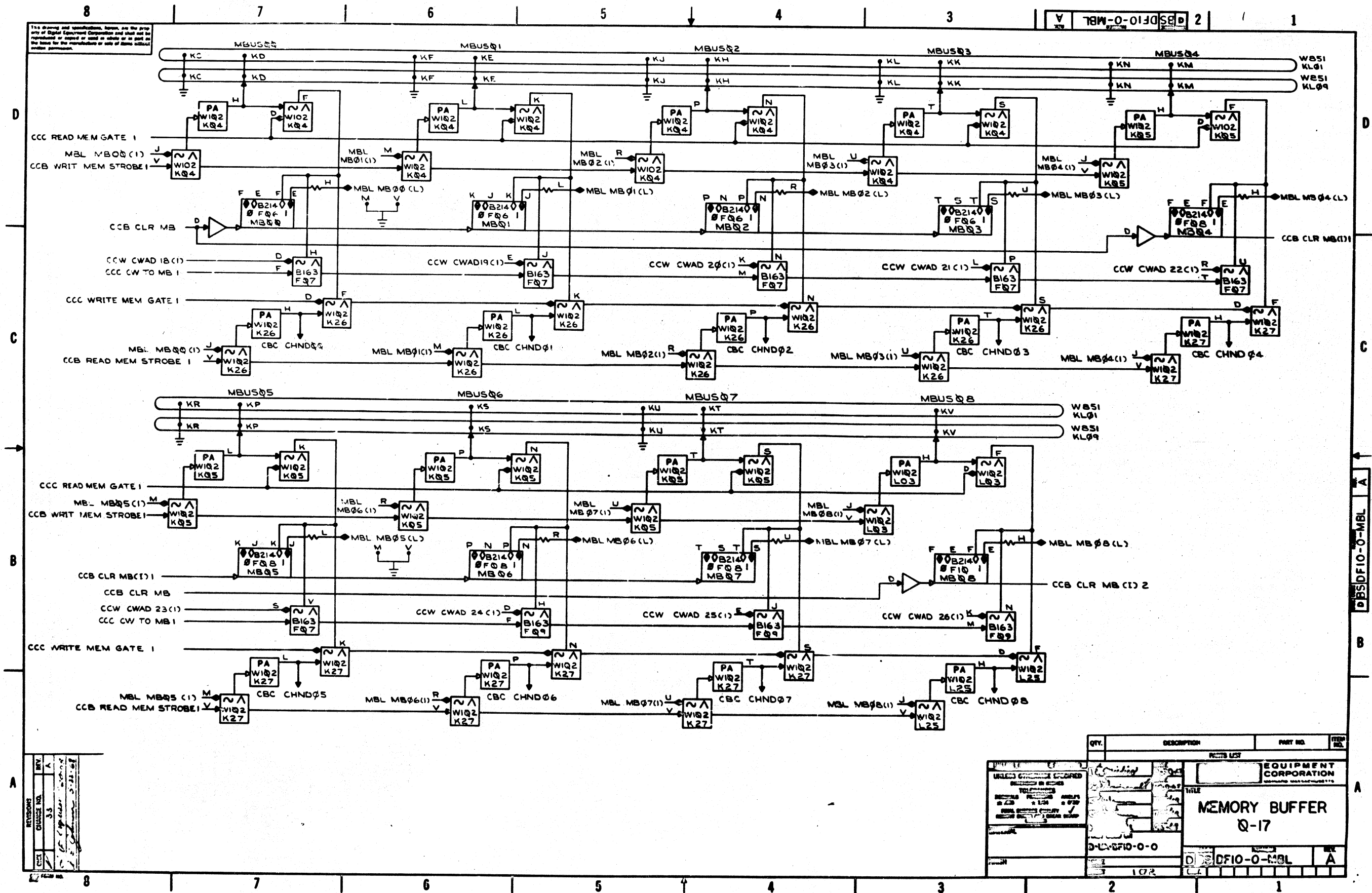


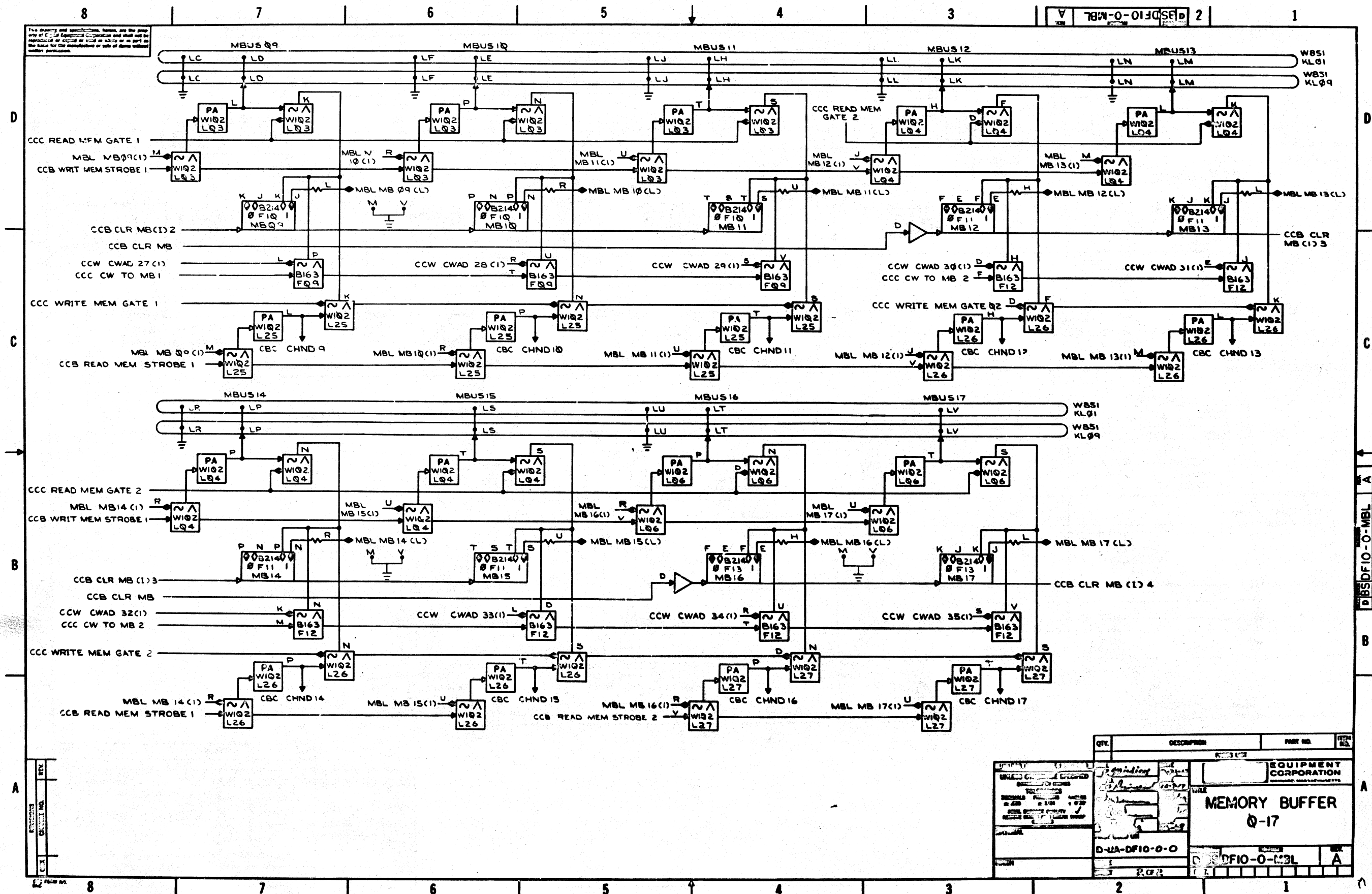
REV	DATE	BY	CHK
1	5-22-68	...	...
2	5-22-68	...	...
3	5-22-68	...	...

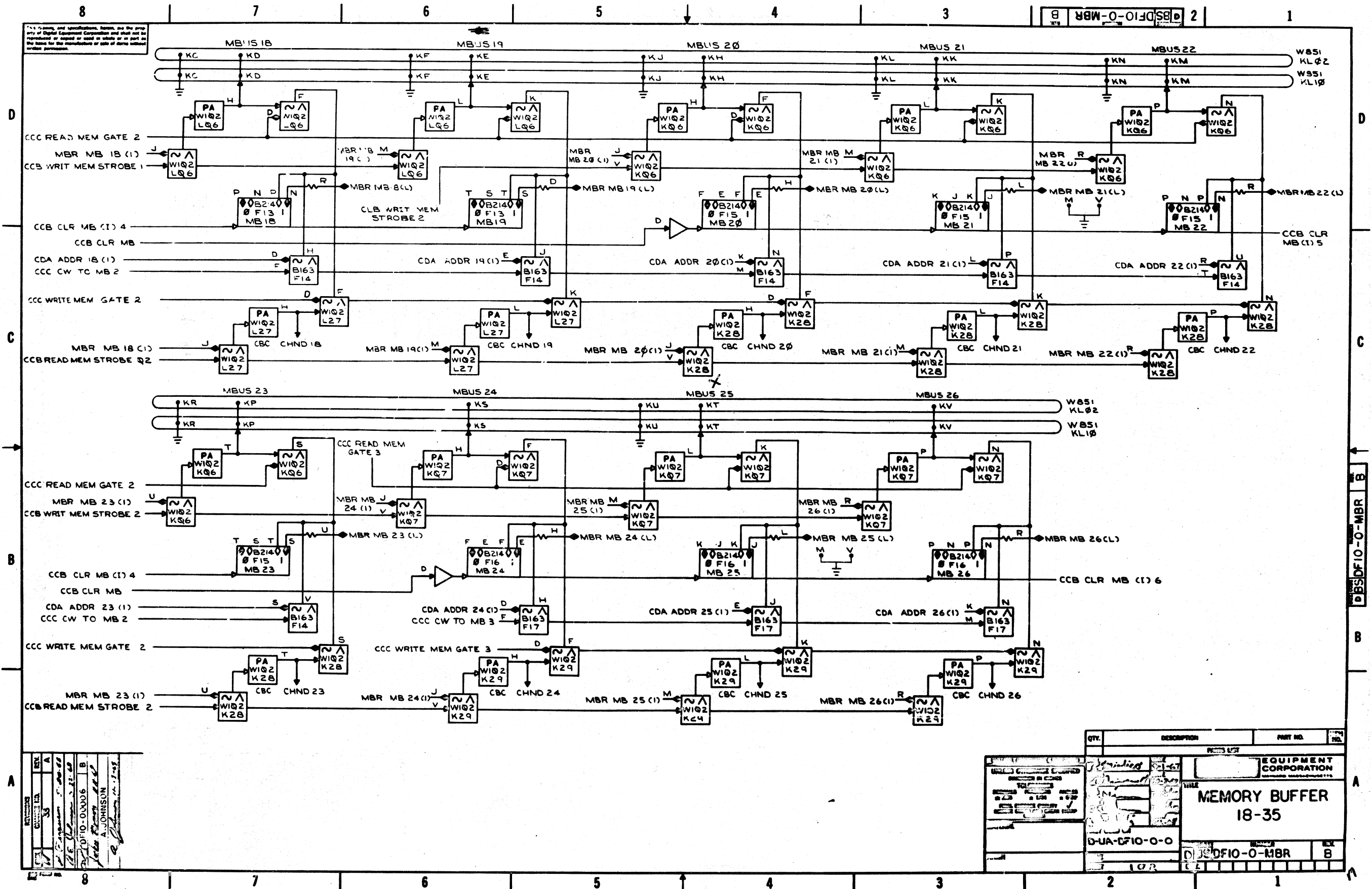
DEC FORM 100
100-100

DATA CHAN
PAR GEN

EQUIPMENT
CORPORATION

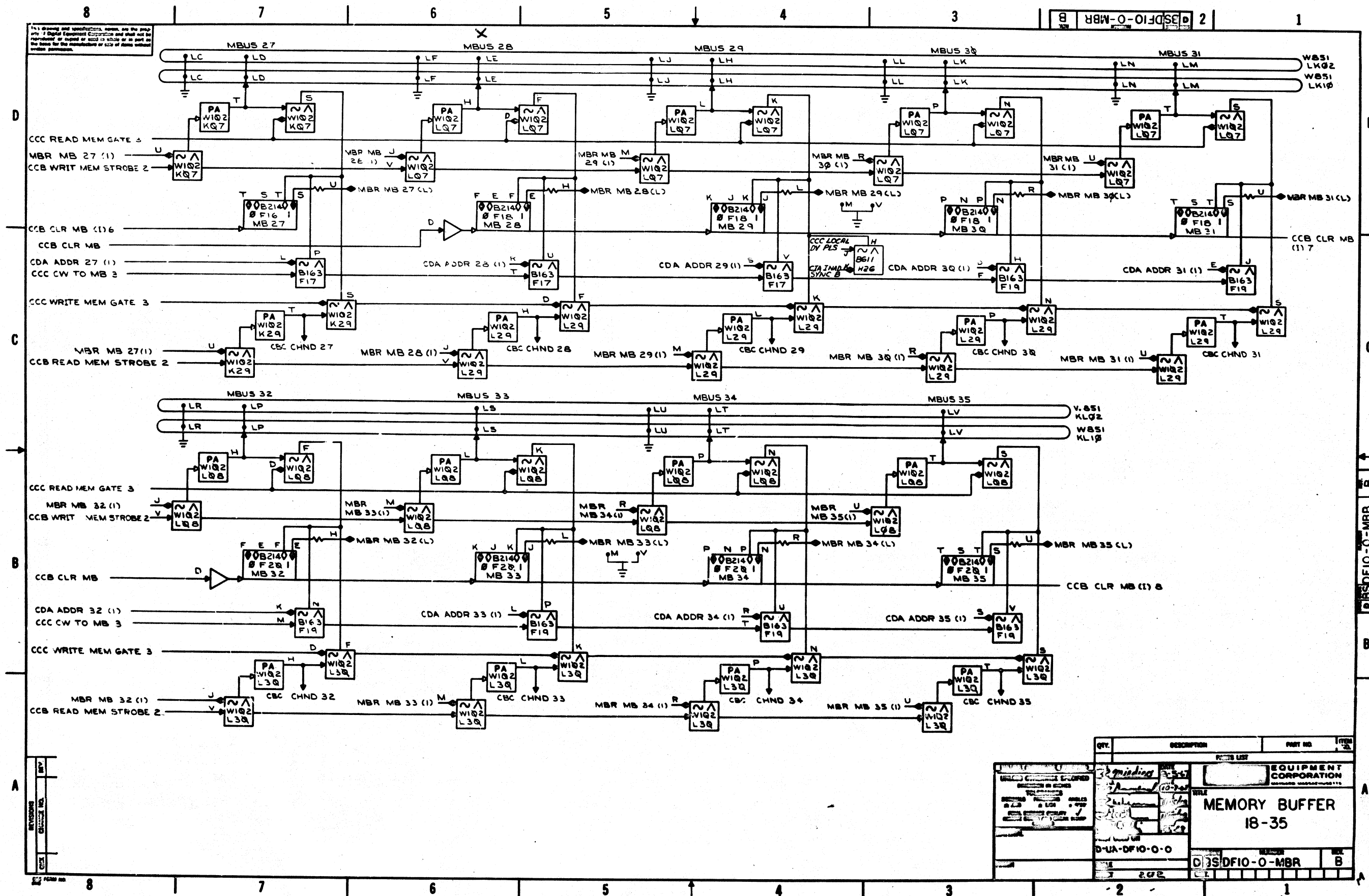


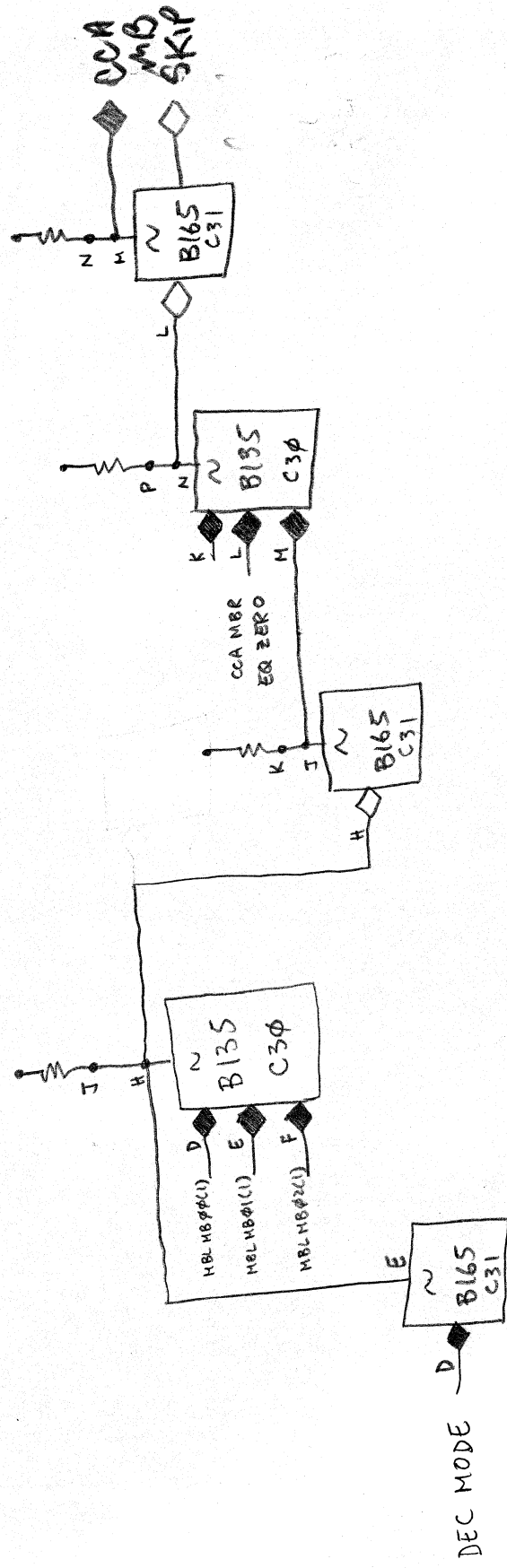


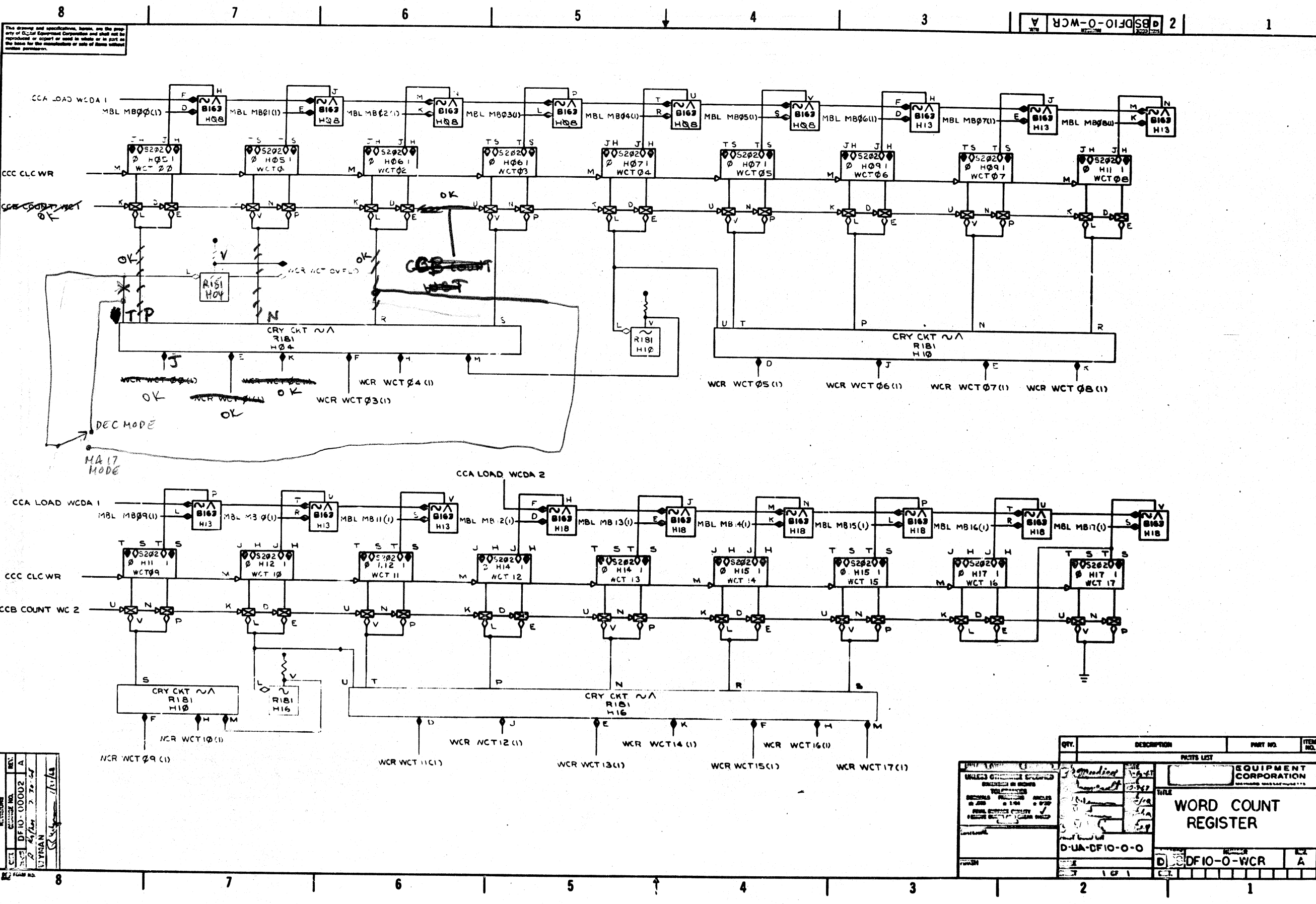


QTY.	DESCRIPTION	PART NO.	REV.
1	Memory Buffer 18-35	D-UB-CF10-O-MBR	B

UNITED STATES GOVERNMENT OFFICE OF THE SECRETARY OF DEFENSE WASHINGTON, D.C. 20301	RECEIVED 10-10-66 10-10-66	EQUIPMENT CORPORATION MEMORY BUFFER 18-35 D-UB-CF10-O-MBR
---	---	--







D-UB-DFIO-O-WCR

A

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	WORD COUNT REGISTER	D-UB-DFIO-O-WCR	A

REVISIONS

REV.	DATE	BY	CHKD.
1	10/1/54	UTMAN	

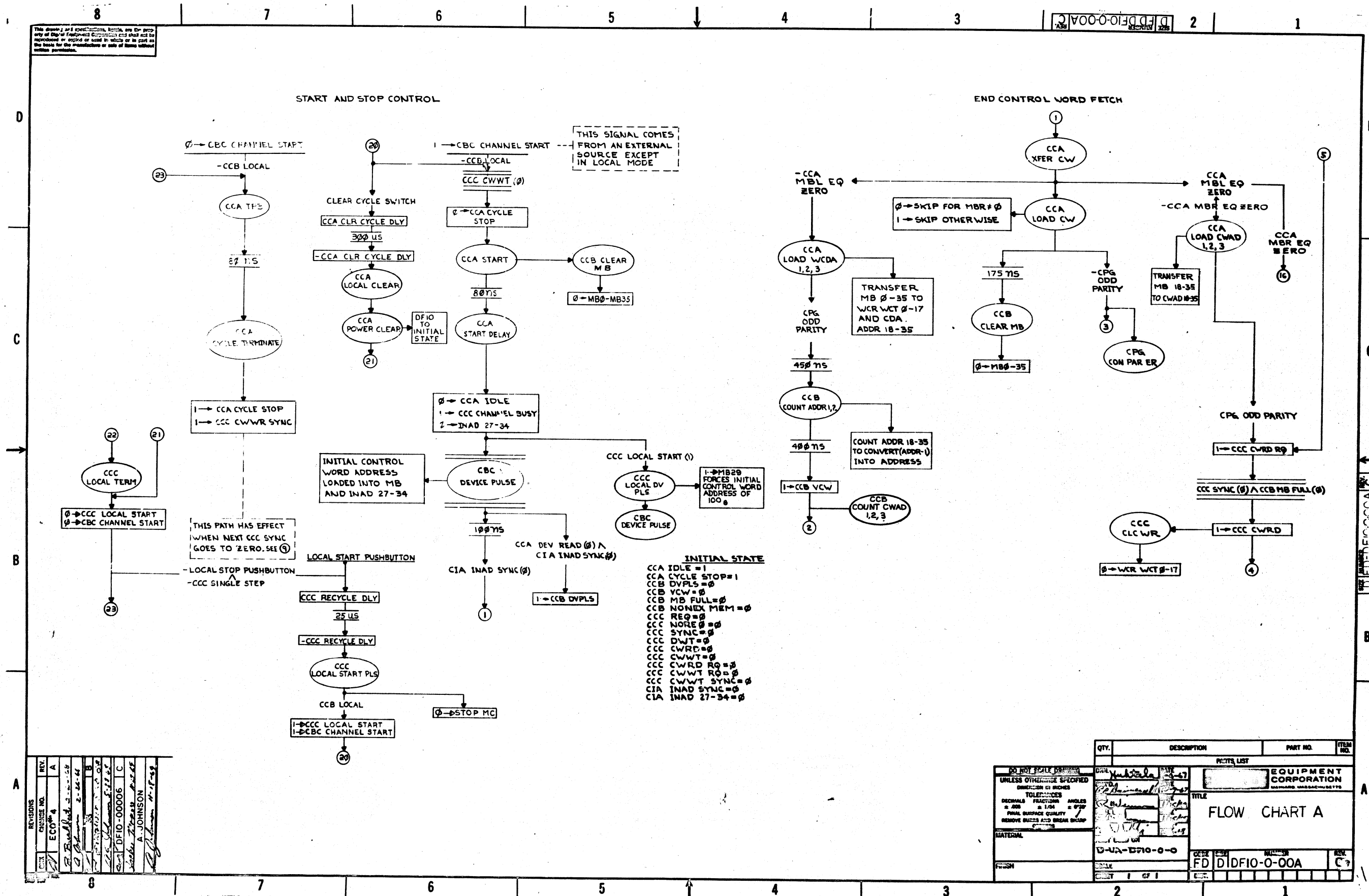
10/1/54

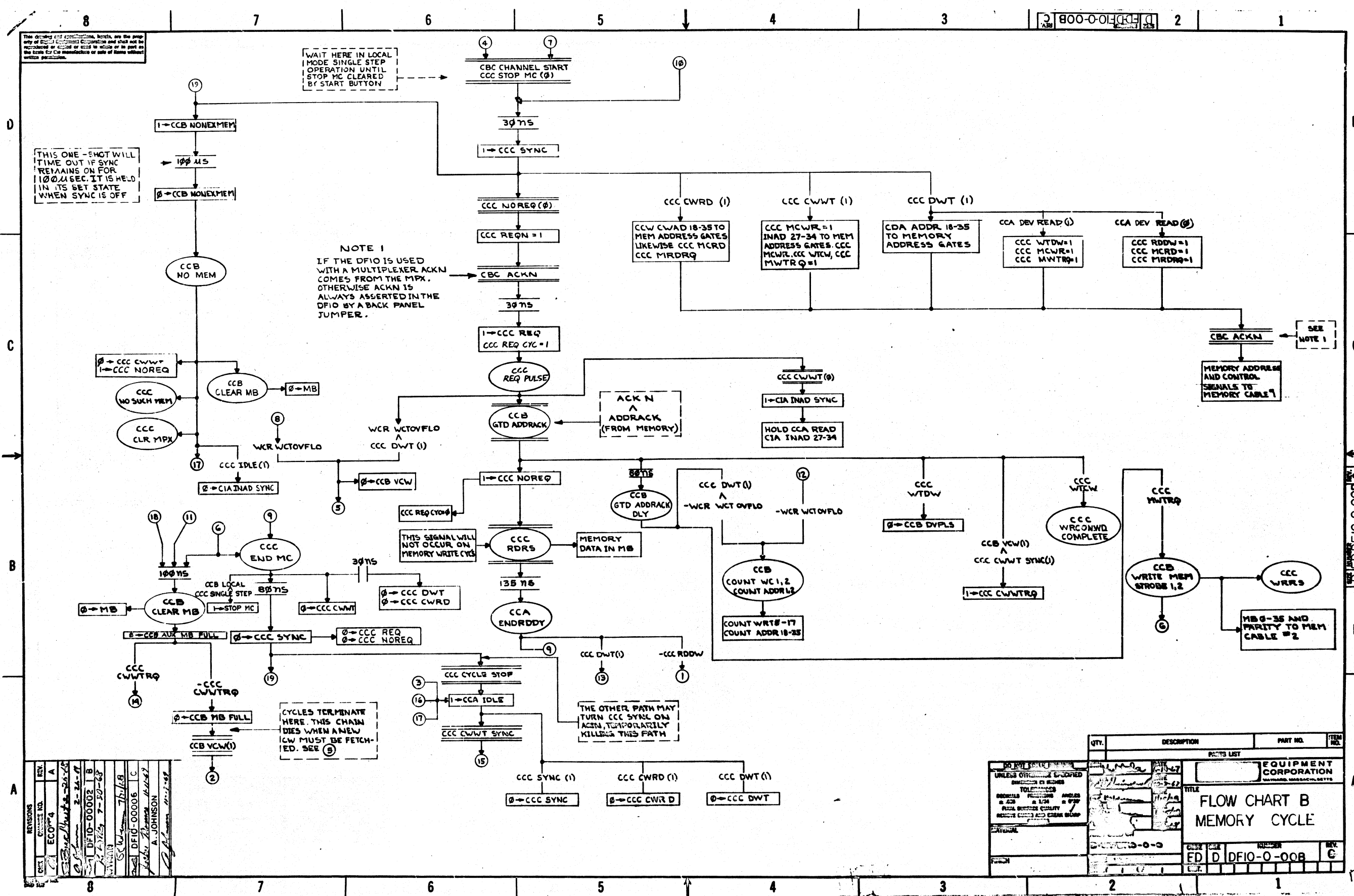
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8		7		6		5		4		3		2		1	
D		E		F		H		J		K		L		M	
A10	MBL MB 24 (2)	CBC DEVICE PULSE B	WCR WCT CW FLO	CCC WTDW	CCC SYNC (0)	CCC DWT (1)	CCC CWWTRQ (0)	CCC CWWT (1)	CCC CWWT (0)	CCA DEV READ (1)	CCB SET VCW	CCA DEV READ (2)	CCB COUNT CHWD2	CCA MBL EQ (0)	GND
B3	MBL MB 24 (1)	MBL MB 24 (1)	CCA LOAD CHWD1	MBL M 23 (1)	MBL MB 23 (0)	CCA ENDRDDY	MBL MB 22 (1)	MBL MB 22 (0)	MBL MB 21 (1)	MBL MB 21 (0)	MBL MB 20 (1)	MBL MB 20 (0)	CCA LOAD CHWD3	CCA MBL EQ 0	
C26	CCC MEM START	CCC SYNC (1)	CCA MBL EQ 0												
D22	MBL MB 25 (0)	MBL MB 25 (1)	MBL MB 26 (0)	MBL MB 26 (1)	MBL MB 27 (1)	MBL MB 27 (0)	MBL MB 28 (1)	MBL MB 28 (0)	MBL MB 29 (1)	MBL MB 29 (0)	MBL MB 30 (1)	MBL MB 30 (0)	CCA MBL EQ 0	CCA MBL EQ (0)	
D11	MBL MB 12 (1)	MBL MB 13 (0)	MBL MB 12 (0)	MBL MB 13 (1)											
E3	CAD GATA	CCC CW TO MBI	CCC CW TO MB2	CCC CW TO MB3	CAD ACKN 2	CAD ACKN 3	CCC CWRD (0)	CCC CWRD (1)	CCC CWRD (0)	CCC CWRD (1)	CCC CLCHR	CAD ACKN 1	CCB COUNT WC2	CCB COUNT WC1	
J32	CCA XFER CW	CCA CYCLE TERMINATE	CCA POWER CLEAR	CCB DVPLS (1)	CCA CYCLE STOP	CCB VCW (1)	CCC LOCAL DV PLS	CCB MB FULL (1)	CCB MB FULL (0)	CCB MB FULL (1)	CCB DVPLS (0)	CCA ACKN 1	CCB COUNT WC2	CCB COUNT WC1	
K3	CCA LOAD WCD A1	CCA LOAD WCD A2	CCA LOAD WCD A3	CCB COUNT ADR1	MBR MB 35 (1)	MBR MB 35 (0)	MBR MB 34 (1)	MBR MB 34 (0)	MBR MB 33 (1)	MBR MB 33 (0)	MBR MB 32 (1)	MBR MB 32 (0)	MBR MB 31 (1)	MBR MB 31 (0)	
K8	CCB COUNT ADR2	MBR MB 21 (1)	MBR MB 24 (1)	MBR MB 26 (1)	MBR MB 22 (1)	MBR MB 23 (0)	MBR MB 33 (1)	MBR MB 33 (0)	MBR MB 32 (1)	MBR MB 32 (0)	MBR MB 31 (1)	MBR MB 31 (0)	MBR MB 30 (1)	MBR MB 30 (0)	
K25	MBL MB 22 (0)	MBL MB 21 (1)	MBL MB 22 (0)	MBL MB 26 (0)	MBR MB 26 (0)	MBR MB 32 (0)	CCC READ MEM	MBR MB 27 (0)	MBR MB 28 (0)	MBR MB 24 (0)	MBL MB 13 (0)	CCA DEV READ (1)	CCA DEV READ (0)	CCA DEV READ (0)	
K30	MBR MB 20 (1)	MBR MB 21 (0)	MBR MB 22 (0)	MBR MB 26 (0)	MBR MB 32 (0)	CCC READ MEM	MBR MB 27 (0)	MBR MB 28 (0)	MBR MB 24 (0)	MBL MB 13 (0)	CCA DEV READ (1)	CCA DEV READ (0)	CCA DEV READ (0)	CCA DEV READ (0)	
L5	MBL MB 28 (1)	MBL MB 12 (1)	MBL MB 12 (1)	MBL MB 12 (1)	MBL MB 29 (1)	READ MEM GATE 1	CCC READ MEM	MBL MB 12 (0)	MBL MB 11 (0)	MBR MB 8 (0)	MBR MB 18 (1)	MBL MB 14 (0)	MBR MB 30 (1)	MBR MB 30 (0)	
L14	CCA SKIP (1)	CIA INAD SYNC (1)	MBR MB 19 (1)	CCC DWT (1)	CCA IDLE (0)	CCA IDLE (1)	CCC WRITE MEM	MBL MB 12 (0)	MBL MB 11 (0)	MBR MB 8 (0)	MBR MB 18 (1)	MBL MB 14 (0)	MBR MB 30 (1)	MBR MB 30 (0)	
L28	MBR MB 19 (0)	MBR MB 31 (1)	MBR MB 31 (0)	MBL MB 29 (0)	CCC WRITE MEM	CCC WRITE MEM	CCC WRITE MEM	MBL MB 12 (0)	MBL MB 11 (0)	MBR MB 8 (0)	MBR MB 18 (1)	MBL MB 14 (0)	MBR MB 30 (1)	MBR MB 30 (0)	GND

NAME	POINT	COMPONENT	POINT
CBC ACKN	F29J	100Ω	F30C
CCA LOAD CW	C28T	100Ω	D29C
CCA START	F21J	100Ω	F21M
CCB CLEAR MB	B10J	100Ω	B11M
CCB DEVPLS	B10N	100Ω	B11C
CCB GTD ADDRACK	B13N	100Ω	B13C
CCB INT CHN PLS	L20M	100Ω	L21R
CCB NO MEM	L20U	100Ω	L21U
CCB READ MEM STROBE 1	B18T	100Ω	B18V
CCB READ MEM STROBE 1	L25V	100Ω	L28V
CCB SKIP PULSE	B13D	100Ω	B15C
CCA WRIT MEM STROBE 1	K05V	100Ω	L06C
CCB WRIT MEM STROBE 2	L08V	100Ω	L09R
CCA START DLY	D12D	100Ω	D12M
CCC REQ PULSE	B12F	100Ω	B19C
CCC START CW WRITE	J23E	100Ω	J24C
CCB READ MEM STROBE 2	L27V	100Ω	L31U
CCC END MC	J24L	100Ω	J28C
F21N	B16T	100Ω	C17C
CCC TP 2	B21L	100Ω	B21M
CCA TP 3	B06L	100Ω	B07P
CCB GTD ADDRACK DLY	F25J	100Ω	F26M
K16D	K17L	100Ω	K18M
RES	C23S	100Ω	C23P
RES	C22S	100Ω	C22P
CCC CONTROL	L12U	100Ω	L12M
CBC CROBAR	E27F	100Ω	E27C
CBC CROBAR	E27J	100Ω	E28C
RES	B22P	100Ω	B22S
RES	B29P	100Ω	B29S
RES	A20P	100Ω	A20S
RES	B28U	100Ω	C20C

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
EQUIPMENT CORPORATION			
SIGNAL TERMINATIONS			
D-UA-DF10-0-0			
1 OF 1			





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THIS ONE - FIGHT WILL TIME OUT IF SYNC REMAINS ON FOR 100 μSEC. IT IS HELD IN ITS SET STATE WHEN SYNC IS OFF

WAIT HERE IN LOCAL MODE SINGLE STEP OPERATION UNTIL STOP MC CLEARED BY START BUTTON

NOTE 1
IF THE DFIO IS USED WITH A MULTIPLEXER ACKN COMES FROM THE MPX. OTHERWISE ACKN IS ALWAYS ASSERTED IN THE DFIO BY A BACK PANEL JUMPER.

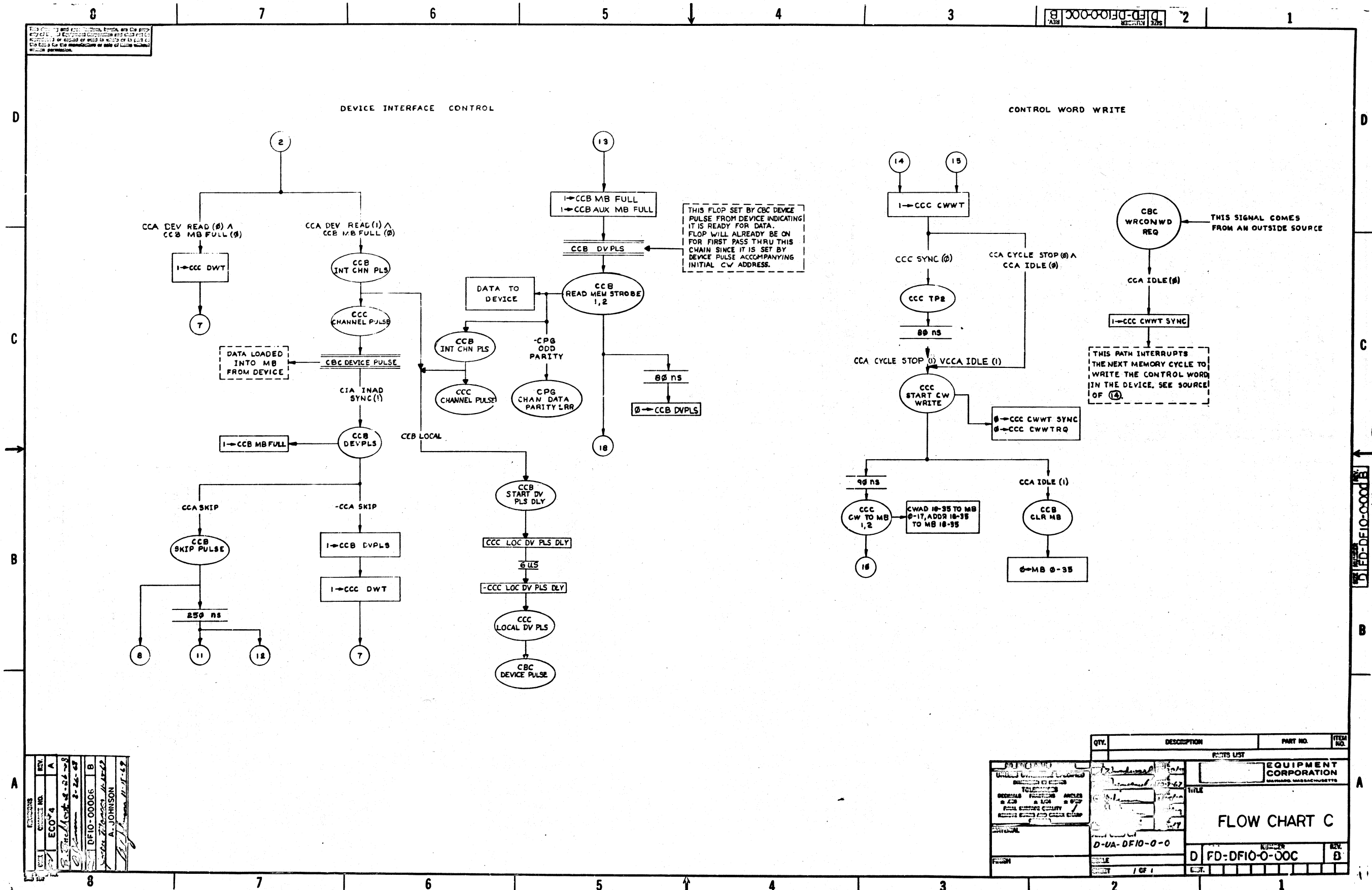
ACK N
ADDRESS
(FROM MEMORY)

SEE NOTE 1
MEMORY ADDRESS AND CONTROL SIGNALS TO MEMORY CABLE 1

CYCLES TERMINATE HERE. THIS CHAIN DIES WHEN A NEW CW MUST BE FETCHED. SEE ⑤

THE OTHER PATH MAY TURN CCC SYNC ON AGAIN, TEMPORARILY KILLING THIS PATH

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
EQUIPMENT CORPORATION			
TITLE			
FLOW CHART B			
MEMORY CYCLE			
ED	D	DFIO-0-00B	C



FORM NO. 106

DEC FORM NO
DRA 106

DRWG NO K-WL-DFIO-O-2		REVLTR B													
<table border="1" style="width: 100%; border-collapse: collapse; margin-top: 20px;"> <tr> <th style="width: 10%;">REV LTR</th> <th style="width: 10%;">ECO NO</th> <th style="width: 10%;">DATE</th> <th style="width: 10%;">ENG</th> </tr> <tr> <td style="text-align: center;">A</td> <td style="text-align: center;">16</td> <td style="text-align: center;">3-28-68</td> <td style="text-align: center;">[Signature]</td> </tr> <tr> <td style="text-align: center;">B</td> <td style="text-align: center;">DFIO-00006</td> <td style="text-align: center;">11/11/69</td> <td style="text-align: center;">[Signature]</td> </tr> </table>				REV LTR	ECO NO	DATE	ENG	A	16	3-28-68	[Signature]	B	DFIO-00006	11/11/69	[Signature]
REV LTR	ECO NO	DATE	ENG												
A	16	3-28-68	[Signature]												
B	DFIO-00006	11/11/69	[Signature]												
DRAWN <i>J. F. Lemay</i>		DATE 9-11-67		 EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		TITLE DATA CHANNEL DFIO									
CHECKED <i>P. J. [Signature]</i>		DATE 1-12-68				FOR TAPE* FILE*									
ENG <i>[Signature]</i>		DATE 1/15/68													
PROJ ENG <i>[Signature]</i>		DATE 1/15/68				SIZE CODE K WL DFIO-O-2		REV LTR B							
PROD <i>[Signature]</i>		DATE 1-16-68													
ASSY NO		SCALE		SHEET OF		DIST.									

DIGITAL EQUIPMENT CORPORATION									
HAYWARD, MASSACHUSETTS									
DATE 2/16/68									
ENGINEERING SPECIFICATION									
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)									
REVISIONS									
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE			
1	ORIGINATED	6	R. Wyman	2/21/68					
ENG	Robert Wyman	APPD	SIZE	CODE	NUMBER	REV			
			A	SP	DF10-0-7	6			
SHEET 1 OF 6									

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)							
Verify the CCB GTD ADDRACK delay. (CCB GTD ADDRACK to CCB GTD ADDRACK DLY 85 $\pm$ 6 ns.) Verify the CCC SYNC turn-off delay (CCC END MC to CCC SYNC off 85 $\pm$ 6 ns).							
3. Verify the operation of each bit in the control word address register by turning the control word switches 18 - 35 on one at a time. Do not have more than two nor less than one switch on at any one time.							
4. Turn on the parity bit and bit 35 of the control word switches. Turn off the Ignore Memory Parity Switch. The channel should now terminate upon fetching the first control word and send the Control Word Parity Error pulse. The tester should then generate RECYCLE and reinitiate the operation. Repeat this test with parity bit off, 35, 34 on; 35 off, 34, 33 on; etc. through bits 18, 19 on, all others off. Verify the time from CBC DEVICE PULSE to CCA XFER CW (100 $\pm$ 20 ns). Verify the time from CCA DTP3 to CCA CYCLE TERMINATE (66 $\pm$ 3 ns).							
5. Verify that each termination in 4 above causes the contents of CWAD and ADDR to be transmitted to memory. (ADDR, the data address, should be 0.) Verify the time from CCC TP2 to CCC START CW WRITE (85 $\pm$ 6 ns) and CCC START CW WRITE to CCC CW TO MB1 (95 $\pm$ 6 ns).							
B. Verify that the control word register loads and counts properly.							
1. Set the following tester conditions:							
Control Word 1 000001 000001							
Memory Data 0 000000 000001							
Channel Data 000000 000001							
Terminate Clock 0							
Memory Cycle Terminate 0							
Write 0							
Continue 1							
Write Control Word 0							
Even Parity 0							
SIZE				CODE		NUMBER	
A				SP		DF10-0-7	
REV				6			
DEC FORM NO DRA 108							
SHEET 3 OF 6							

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)							
Setup							
Connect a twisted pair from the Channel to the tester according to the table below:							
		Signal	Channel	Tester			
		Ground	L12U	B21L			
			L12M	B21C			
Then check voltages at several points in all mounting panels of the Channel.							
Control Test							
A. Verify that the channel can successfully load control word addresses.							
1. Set the following tester conditions:							
Control Word 0 000000 000001							
Memory Data 1 000000 000000							
Channel Data 000000 000001							
Terminate Clock 0							
Memory Cycle Terminate 0							
Write 0							
Continue 1							
Write Control Word 0							
Even Parity 0							
Ignore Memory Parity 1							
Recycle Delay 100							
Terminate Delay 100							
2. When the start pushbutton on the tester is pushed, the channel should continuously fetch the value set in the control word switches and load it in the control word address register (CWAD). Verify the CCA END RDDY delay time. (CCC RD25 to CCA ENDRDDY 135 $\pm$ 6 ns). Verify the CCB CLEAR MB delay. (CCA LOAD CW to CCB CLEAR MB 220 $\pm$ 6 ns)							
SIZE				CODE		NUMBER	
A				SP		DF10-0-7	
REV				6			
DEC FORM NO DRA 108							
SHEET 2 OF 6							

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)							
Ignore Memory Parity 1							
Recycle Delay 100							
Terminate Delay 100							
2. When the Start pushbutton is pushed, the channel should load the contents of the Control Word switches into the Control Word register (WC and ADDR) and count WC up until it overflows. Check each WC bit position one at a time to verify that it is properly loaded. (Be sure WC $\neq$ 0 when loaded.) Do the same for ADDR. (Be sure ADDR $\neq$ 0 when loaded.) To speed the testing, set the Terminate Clock switch to 1. Then when the Terminate Delay times out, the channel will be forced idle. Verify the time relationship between CCA LOAD WCDA 1, CCB COUNT ADR 1 and CCB SET VCW. (CCA LOAD WCDA 1 to CCB COUNT ADR 1 500 $\pm$ 50 ns. CCA LOAD WCDA 1 to CCB SET VCW 850 ns $\pm$ 50 ns.)							
3. Turn off the Terminate Clock. Set the Word Count portion of the Control Word switches to 777777, Address portion to anything, parity odd, and turn the Ignore Memory Parity switch off. Start the operation and verify that CWAD counts properly.							
Data Test							
A. Verify that data is transferred properly through the channel.							
1. Set the following tester conditions:							
Control Word 1 000001 000001							
Memory Data 0 000000 000001							
Channel Data 000000 000001							
Terminate Clock 0							
Memory Cycle Terminate 0							
Write 0							
Continue 1							
Write Control Word 0							
Even Parity 0							
SIZE				CODE		NUMBER	
A				SP		DF10-0-7	
REV				6			
DEC FORM NO DRA 108							
SHEET 4 OF 6							

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)			
	Ignore Memory Parity	0	
	Recycle Delay	100	
	Terminate Delay	100	
2.	Start the operation, and using the Channel Data switches verify the operation of the data path (including the parity network) for floating ones. Verify that total cycle time for a data transfer is $740 \text{ ns} \pm 50 \text{ ns} + 2$ channel cable delays + 2 memory cable delays (1.5 ns per foot of cable). Turn on Even Parity and verify that even parity is transmitted to memory for floating ones.		
3.	Set the Address portion of the Control Word switches to zero (with proper parity) and verify that the skip operation is properly performed, i.e. no data transferred to memory. Verify the delay from CCB SKIP PULSE to CCB SKIP PULSE DLY ($266 \pm 10 \text{ ns}$). Verify that total cycle time is $600 \pm 50 \text{ ns} + 2$ memory cable delays + 2 channel cable delays (1.5 ns per foot).		
4.	Set Write = 1. Using the Memory Data switches verify the operation of the data path (including the parity network) for floating ones. Verify the timing from CCB READ MEM STROBE 1 to CCB DVPLS going off ($75 \pm 6 \text{ ns}$). Verify that total cycle time is $570 \pm 50 \text{ ns} + 2$ memory cable delays (1.5 ns per foot). (Channel cable delays do not enter into this time.)		
5.	Turn on Write Control Word and verify that CWAD and ADDR are transmitted to memory. Set the Word Count portion of the control word to 777777, Address portion anything, parity odd. Verify that no control word write cycle is taken even though Write Control Word is on.		
Termination Tests			
A.	Verify that termination of the channel by the device causes no malfunction.		
1.	Set the following tester conditions:		
	SIZE	CODE	NUMBER
	A	SP	DF10-0-7
			REV

BEC FORM NO
DRA 108

SHEET 5 OF 6

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (OFFLINE)			
	Control Word	1 000001 000001	
	Memory Data	1 000000 000000	
	Channel Data	000000 000001	
	Terminate Clock	1	
	Memory Cycle Terminate	0	
	Write	0	
	Continue	1	
	Write Control Word	0	
	Even Parity	0	
	Ignore Memory Parity	0	
	Recycle Delay	100	
	Terminate Delay	100	
2.	Start the operation, and using the low order nine bits of the Channel Data switches, verify the operation of the INAD register.		
3.	Verify that the channel terminates properly after each operation.		
4.	Turn on the Memory Cycle Terminate switch and verify that the channel terminates properly.		
5.	Turn off Memory Cycle Terminate and Terminate Clock. Set Recycle Delay to 100. Turn on No Memory Switch and start the operation. The normal start-up cycle should now ensue, but the first control word will never be fetched. Instead, the CCB NONEXMEM single shot should time out generating the NO SUCH MEM pulse on the Channel Bus and terminating the cycle. Verify proper operation.		
	SIZE	CODE	NUMBER
	A	SP	DF10-0-7
			REV

BEC FORM NO
DRA 108

SHEET 6 OF 6

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS									
ENGINEERING SPECIFICATION									
TITLE DF 10 RECOMMENDED SPARE PARTS LIST									
DATE May 14, 1968									
REVISIONS									
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE	NUMBER	SIZE	REV
--	ORIGINATOR	33	--	--	--	--	--	--	--

ENG	Fertig	APPD	RE Johnson	CODE	SP	SIZE	A	DF10-0-8	NUMBER	REV
SHEET 1 OF 4										

ENGINEERING SPECIFICATION									
TITLE DF 10 RECOMMENDED SPARE PARTS LIST									
CONTINUATION SHEET									
TRANSISTORS									
Type	Part No.	Quantity							
DEC SDA-86718-1	15-02105	2							
2894	15-03097	2							
2N3605	15-02151	2							
2N4258	15-05321	6							
DEC 3009B-S	15-03100	2							
2N2904	15-01742	2							
DEC 3639-D	15-02762-02	8							
DEC 2894-38-S	15-03099	2							
DEC 3009A-S	15-01999	2							
DEC 2894-2S	15-03098	2							
DEC 6534	15-03409	2							

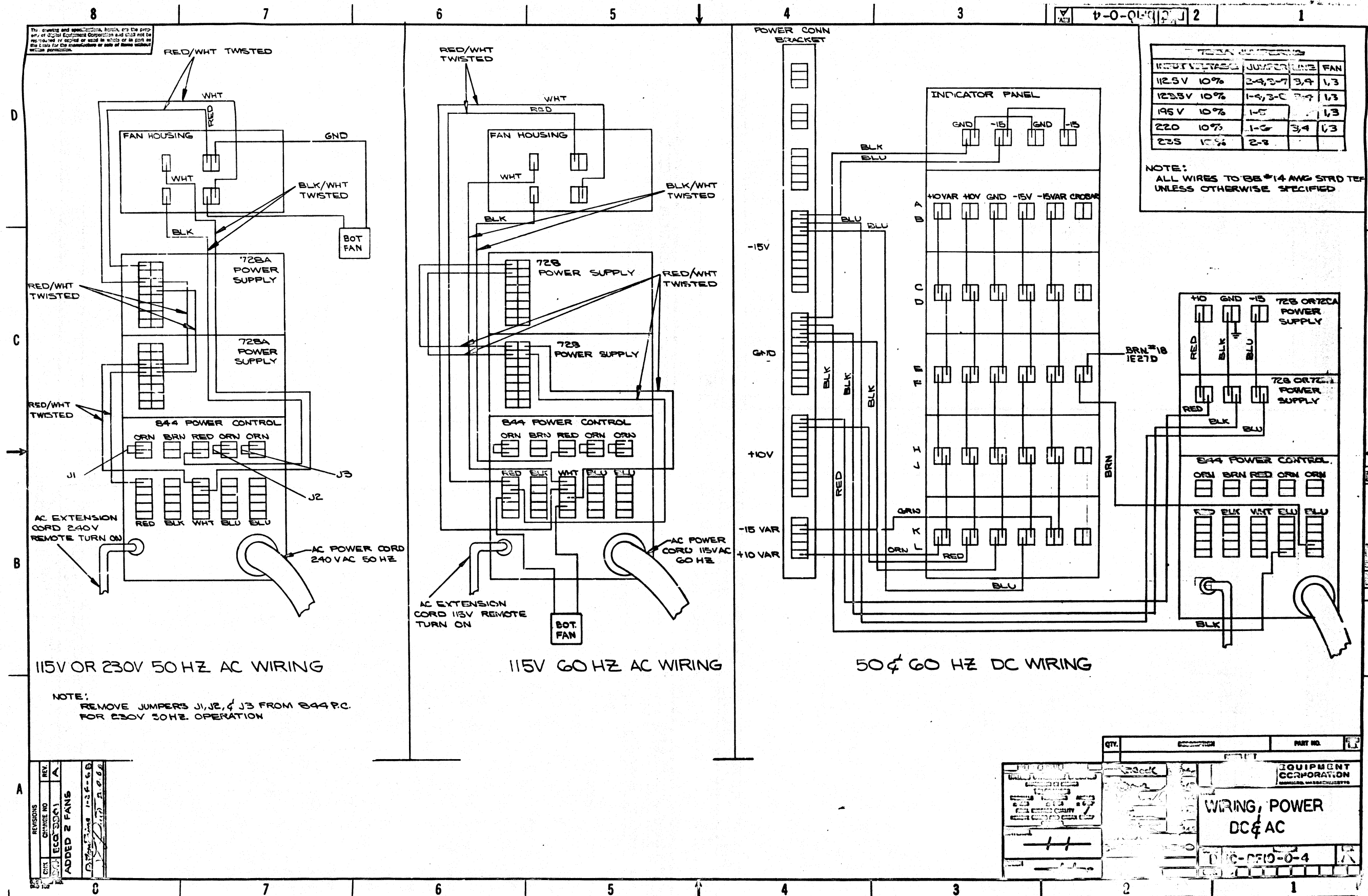
DEC FORM NO	SIZE	CODE	NUMBER	REV
DRA 108	A	SP	DF10-0-8	4
SHEET 3 OF 4				

ENGINEERING SPECIFICATION									
TITLE DF 10 RECOMMENDED SPARE PARTS LIST									
CONTINUATION SHEET									
MODULES									
Type	Amount								
B130	2								
B133	1 2								
B134	1								
B135	1								
B137	1								
B163	2								
B165	1								
B212	1								
B214	1								
B311	1								
B611	1								
B683	1								
B685	1								
G704	1								
R001	1								
R303	1								
R613	1								
S181	1								
S603	1								
W012	1								
W102	2								
W250	1								
W301	1								

CODE	SIZE	NUMBER	REV
SP	A	DF10-0-8	4
SHEET 2 OF 4			

ENGINEERING SPECIFICATION									
TITLE DF 10 RECOMMENDED SPARE PARTS LIST									
CONTINUATION SHEET									
ADDITIONAL									
Description	Part No.	Quantity							
D662	11-00113	10							
D664	11-00114	10							
D668	11-02161	6							
INDICATOR LIGHTS	12-555	10							
TRIMPOT	A-13-S395	1							

CODE	SIZE	NUMBER	REV
SP	A	DF10-0-8	4
SHEET 4 OF 4			



DIGITAL EQUIPMENT CORPORATION									
MAYNARD, MASSACHUSETTS									
ENGINEERING SPECIFICATION									
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (ONLINE)									
DATE 10/7/69									
REVISIONS									
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE			
ENG Arthur Johnson									
APPD <i>Arthur Johnson</i>									
SIZE CODE SP A									
NUMBER DF10-0-9									
REV									
SHEET 1 OF 3									
DEC FORM NO DRA 107									

ENGINEERING SPECIFICATION									
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (ONLINE)									
6. Display 4000 _g to verify that zeroes are written in this location.									
7. Display location 101 _g to verify that the correct control word is being written into memory.									
101 _g = 001001 004001									
8. Stop the DF10 by pressing LOCAL STOP. Set MEM CYCLE SINGLE STEP = 1 and press LOCAL START. The DF10 should stop after doing the first memory cycle. When LOCAL START is pressed, a second memory cycle should take place. Continue to single step by pressing LOCAL START button and verify correct operation.									
9. Clear the DF10 by pressing CLEAR button and enter "ones" in location 4000 _g . Set DEVICE WRITE = 1 and press LOCAL START. Verify that "8's" are read from memory into the DF10 memory buffer during the data word transfer.									
(NOTE: This may be verified visually in the MB lights by increasing the word count of the control word in location 1000 _g and entering "ones" in the appropriate number of locations starting at location 4000 _g .)									
10. Set CLEAR CYCLE = 1 and press LOCAL START. Verify OCA CLR CYCLE DLY (300 us ± 20%). Verify that OCA LOCAL START is cleared when OCA CLR CYCLE DLY times out.									
SIZE CODE SP A									
NUMBER DF10-0-9									
REV									
SHEET 3 OF 3									
DEC FORM NO DRA 108									

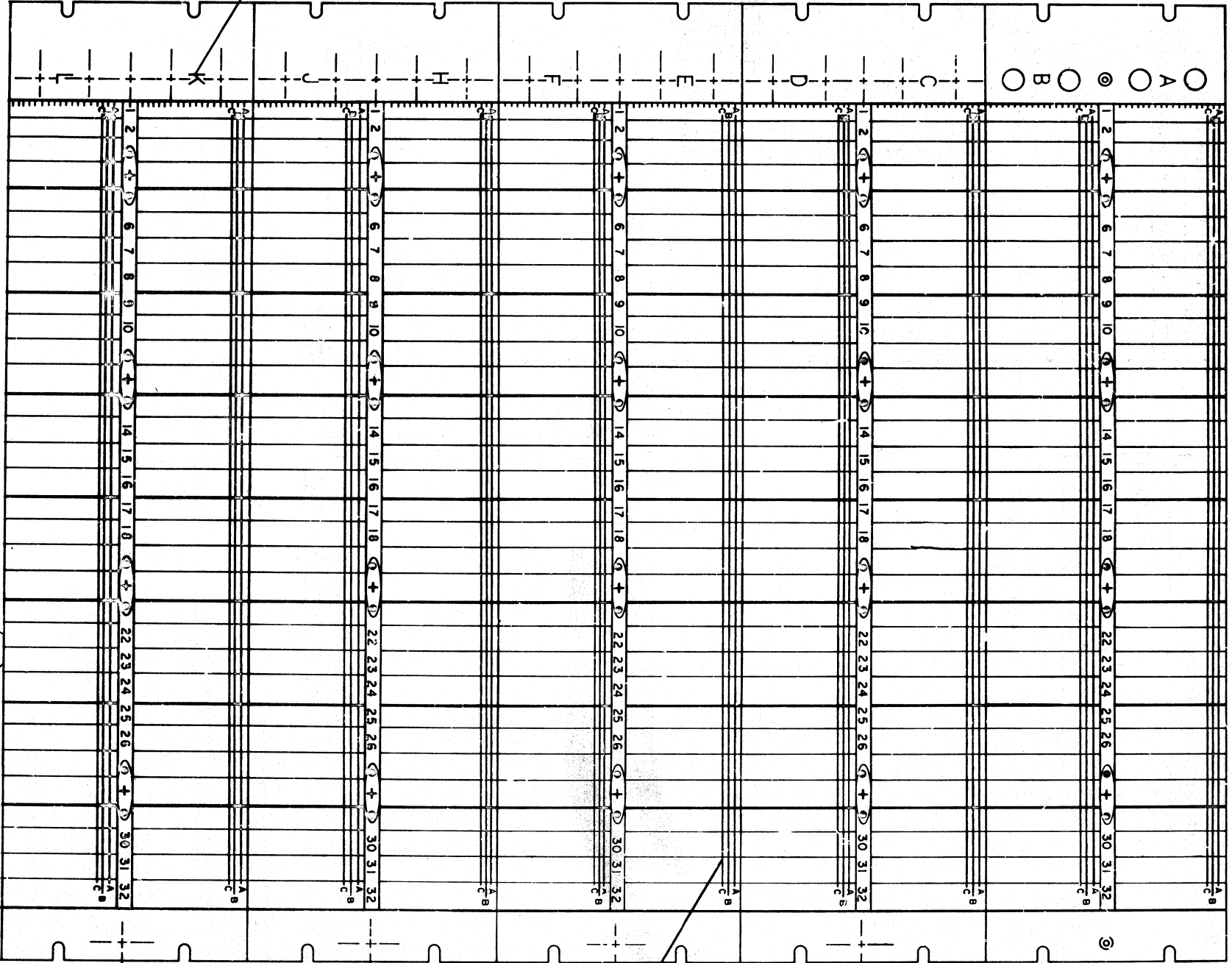
ENGINEERING SPECIFICATION									
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (ONLINE)									
General This procedure tests the LOCAL mode feature of the DF10. For additional on-line tests, see test procedure for devices using channel bus.									
Set Up DF10 connected to MA10 or MB10 via memory bus.									
Procedure									
1. Set the following DF10 conditions:									
LOCAL 1									
Device Write 0									
MEM Cycle Single Step 0									
Clear Cycle 0									
At the MA10 console, load a control word into 100 _g as follows:									
LOC 100 = 000000 000000									
2. Press the LOCAL START pushbutton. The DF10 should start, fetch the zero control word, terminate, and then recycle, the operation repeating until the LOCAL STOP pushbutton is pressed. Verify the length of RECYCLE DLY (25 us ± 20%).									
3. Display OCA LOCAL START (1) on the scope. Hold down LOCAL STOP pushbutton and press LOCAL START. Verify the channel cycles only once.									
4. Load the following location at the MA10 console.									
LOC 100 = 0—0 001000									
1000 = 777777 003777									
1001 = 000000 000000									
4000 = 777777 777777									
5. When the LOCAL START pushbutton is pressed, the DF10 should fetch the control words, do a one word data transfer (across to memory), and then terminate. The operation should repeat until LOCAL STOP is pressed. Verify OCA LOC DV PLS DLY (6 us ± 20%).									
SIZE CODE SP A									
NUMBER DF10-0-9									
REV									
SHEET 2 OF 3									
DEC FORM NO DRA 108									

ENGINEERING SPECIFICATION									
TITLE CHANNEL MANUFACTURING TEST PLAN OUTLINE (ONLINE)									
DEC FORM NO DRA 108									

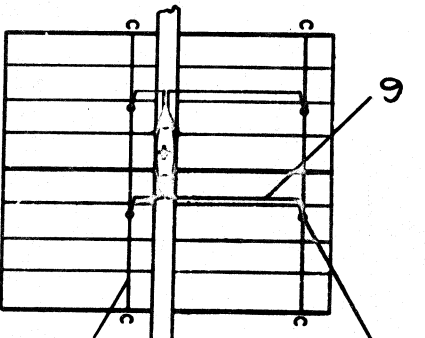
REV.	DESCRIPTION	DATE
1	REVISIONS	
2	REVISIONS	
3	REVISIONS	
4	REVISIONS	
5	REVISIONS	
6	REVISIONS	
7	REVISIONS	
8	REVISIONS	

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 8. REVISIONS

THIS DRAWING AND SPECIFICATIONS, PRINTS, AND THE PRO-
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 the basis for the manufacture or sale of items, shall be



SEE NOTE 1
 SEE NOTE 2
 SEE DETAIL A
 SEE DETAIL B



DETAIL A
 20 PLACES
 SEE NOTE 3

NOTES:
 1. CONNECTIONS ON ITEMS #3 & #6 TO BE
 SOLDERED AND LOCATED AT MINIMUM
 PRACTICAL HEIGHT ABOVE BLOCK.
 2. USE YELLOW WIRE (ITEM #5) FOR
 MACHINE WRAPPED & BLUE WIRE
 (ITEM #7) FOR HAND WRAPPED
 WIRING.
 3. ALL CONN BLOCKS TO BE GROUNDED
 TO GND LUGS AS SHOWN.

REV.	DESCRIPTION	DATE
1	REVISIONS	
2	REVISIONS	
3	REVISIONS	
4	REVISIONS	
5	REVISIONS	
6	REVISIONS	
7	REVISIONS	
8	REVISIONS	

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