

**XVM system
reference manual**

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FOREWORD

XVM systems offer comprehensive solutions to data processing needs. They combine new design concepts with a wide array of traditional features that have evolved from DIGITAL's years of leadership in the medium scale scientific computer field. Both elements share the common purpose of simplifying the application of XVM computer systems to accommodate demanding environments.

XVM systems excel in applications where hardware and software components are matched to meet the requirements of the user. These matches of hardware and software components can be viewed at two levels. First, XVM systems come with a complete assortment of support software tools to allow complete programming. These tools, such as monitors, compilers, and system utility components, are the base on which all XVM systems are built. Second, for certain specific turn-key applications, XVM systems come ready to perform applications work with no further programming. At both levels, hardware components allow for modular additions and field upgrades without penalty.

DIGITAL offers a variety of configurations as hardware building blocks to total system capability. These systems differ in their hardware options and peripherals that are required to support various operational software.

The hardware systems are designed with several functional objectives in mind. Among these are the complete autonomy between central processor, input/output processor, and memory, so that processing and I/O operations can occur concurrently in overlapping cycles: A PDP-11 programmable peripheral processor, so that slow speed devices can be spooled to a high performance disk; TTL integrated-circuit construction for high reliability; fast internal speeds, to meet the demands of real-time data processing; core memory expansions to 131,072 words for future growth; floating point hardware for demanding scientific applications; and a sophisticated memory protect system for multi-user integrity in multiprogramming environments. Peripheral device handling and interfacing to instruments are easily accomplished and system growth potential is virtually unlimited with the modular structure of the XVM hardware and software systems.

INTRODUCTION

The XVM 18-bit computer has unique capabilities attractively suited to high-speed data acquisition and processing. Expandable core memory (to 131,072 words) and a full complement of processor options and peripherals enable the XVM to handle virtually any medium scale computing requirement.

This manual supplies background information to familiarize the reader with present and potential capabilities of the system.

THE XVM SYSTEM

The basic XVM System is organized into three autonomous subsystems: central processor, memory, and I/O processor, each with independent timing and control logic. Communication between these subsystems occurs through use of an effective asynchronous request scheme. Subsystem autonomy facilitates wide scale expansion of the system, increased throughput, high capacity, reliability, and maintainability. Four other major subsystems of the XVM are: the floating point processor, the peripheral processor, the XVM I/O bus peripherals, and the Unibus peripherals..

CENTRAL PROCESSOR (CPU)

The CPU controls and executes the system's stored programs. By virtue of its control autonomy, the CPU coordinates its operation with that of other subsystems, thus providing supervisory control over the XVM.

As the main unit in this integrated control, the central processor contains arithmetic and control logic hardware for a wide range of operations, including high-speed, fixed point arithmetic and hardware multiply and divide option, extensive test and branch operations implemented with special hardware registers, high-speed input/output instructions, and other arithmetic and control operations.

The basic processor includes a number of major registers for processor-memory communications; it also includes a program counter, an accumulator, an Index register, and a Limit register. Two 18-bit registers provide memory buffer functions. This allows for processor overlap with memory cycle time and affects faster instruction execution times.

MEMORY

Memory is the primary storage area for computer instructions and system data. Independent read/write control and buffer logic in each memory segment establishes complete autonomy for the memory, i.e., different memories can be accessed simultaneously by different processors. The primary XVM memory systems are the ME15 and MF15 memory units that permit installation and utilization of up to 131,072 words of core memory in 8K or 32K increments.

MEMORY PROCESSOR

The XM15 Memory Processor, located between the memory and the CPU, I/O, and peripheral processors, contains the Memory Management logic, the Instruction Pre-fetch unit, the Automatic Priority Interrupt unit, and the Memory Ports which arbitrate the different memory requests. The XM15 has dual input ports, and may have two output ports to memory. The device will operate with either ME15 (8K) or MF15 memories on one or both of its output ports. Memory interleaving is possible with similar memory types and it is also possible to interleave the two output ports.

I/O PROCESSOR

The I/O processor satisfies the peripheral data transfer needs. A diverse line of system peripherals available to the XVM require this processor to interface three modes of input/output:

1. Single cycle block data transfer; blocks of data transfer at rates of up to 1 million words per second.
2. Multicycle block data transfer; blocks of data transfer at rates up to 250,000 per second for input and 180,000 per second for output.
3. Program control data transfers; single word transfers to/from the accumulator in the central processor unit.

The I/O processor provides timing, control, and data lines for information transfers between memory or the central processor and the peripheral devices. It also provides for such features as the automatic priority interrupt system and the real-time clock.

FP15 Floating Point Processor

The FP15 enables the XVM to perform arithmetic and logic operations using floating point arithmetic. The prime advantage is increased speed over complex floating point software routines. The FP15 has single precision and extended integer capability, as well as single and double precision floating point.

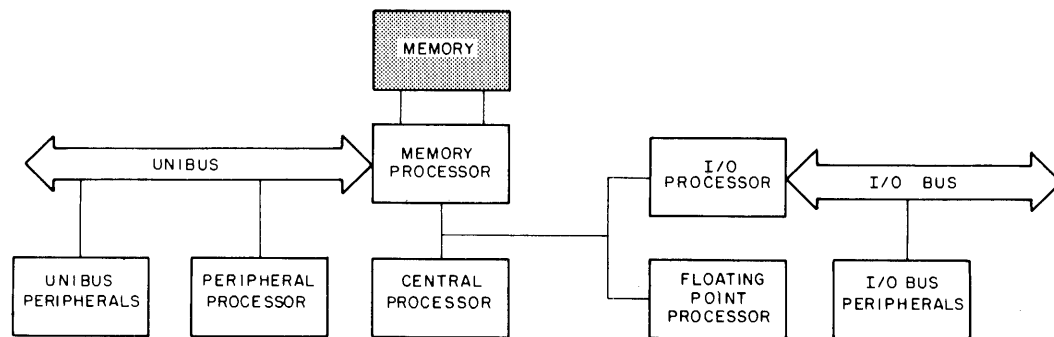
The FP15 is an expansion of the central processing unit and increases the XVM instruction set by over 120 instructions. Floating point instructions intermix with XVM instructions. This In-line mode of operation greatly simplifies programming and ensures fast execution.

Peripheral Processor

The Unichannel 15 (UC15) is a peripheral processor for XVM that uses a PDP-11 minicomputer. It provides the XVM with a second general purpose processor and a second high-speed I/O bus: The Unibus is an 18-bit pathway permitting transfer of 18-bit words, 16-bit PDP-11 words, or two 8-bit bytes.

CHAPTER 1

XVM PROCESSOR



15-0982

1.1 CENTRAL PROCESSOR DESCRIPTION

The central processor (CPU) controls and executes stored programs. By coordinating its operation with that of other subsystems, it provides supervisory control over the XVM system.

The CPU contains arithmetic and control logic for a wide range of operations. These include high-speed, fixed point arithmetic with hardware multiply and divide, extensive test and branch operations implemented with special hardware registers, high-speed input/output instructions, and other arithmetic and control operations.

The XVM CPU contains several major registers for processor-memory communications, – a Program Counter, an Instruction register, an accumulator, an Index register, and a Limit register.

SUMMARY OF CHARACTERISTICS

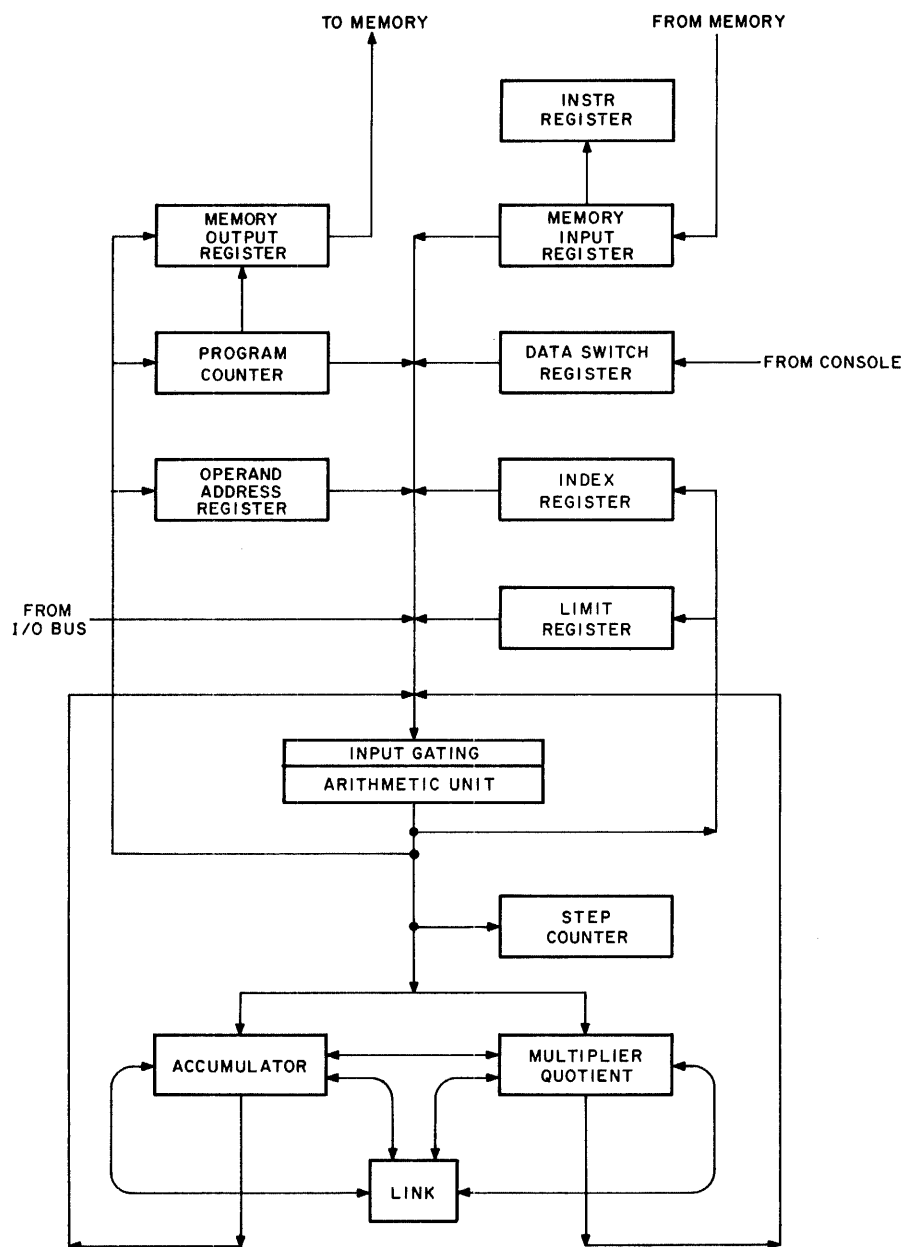
Description – 18-bit parallel operation, asynchronous operation, fixed point signed and unsigned arithmetic (1's and 2's complement)

Instruction Types

- Memory Reference
- Operates
- Register Transfer and Control
- Extended Arithmetic Element
- Input/Output Transfer

Indexing – 1 Index register, 1 Limit register, 8 auto-increment locations

The CPU performs calculations and data processing in a parallel binary mode through step-by-step execution of individual instructions. Both the instructions and the data on which the instructions operate are stored in the core memory of the XVM. The arithmetic and logical operations necessary for executing instructions are performed by the arithmetic unit operating with central processor registers. Figure 1-1 shows a simplified block diagram of the CPU.



15-0002

Figure 1-1 Central Processor, Simplified Block Diagram

Arithmetic Unit (AU)

The XVM Arithmetic Unit (AU) handles all Boolean functions and contains an 18-bit, 85 ns adder. The AU acts as the transfer path for inter-register transfers and shift operations.

Instruction Register (IR)

This register accepts the six most significant bits of each instruction word fetched from memory. Of these bits, the four most significant constitute the operation code, the fifth signals when the fetched instruction indicates indirect addressing, and the sixth indicates indexing.

Accumulator (AC)

This 18-bit register retains the result of most arithmetic/logical operations.

For all program-controlled input/output transfers, information is transferred between core memory and an external device through the AC. The AC can be cleared and complemented. Its contents can be rotated right or left with the Link. The contents of the memory, buffered through the Memory Input register, can be added to the contents of the AC with the result left in the AC. The contents of both registers can be combined by the logical operations AND and exclusive-OR, the result remaining in the AC. The inclusive-OR can be performed between the AC and the data switches on the operator's console (through the Data Switch register) and the result left in the AC.

Data Switch Register

The Data Switch register receives and stores an 18-bit word through the console bus from data switches on the console. This allows programs to accept switch data from the operator's console.

Link (L)

This 1-bit register is used to extend the arithmetic capability of the accumulator. In 1's complement arithmetic, the Link is an overflow indicator; in 2's complement arithmetic, it logically extends the accumulator to 19 bits and functions as a Carry register. The program can check overflow into the Link to simplify and speed up single- and multi-precision arithmetic routines.

The Link can be cleared and complemented and its state sensed independent of the accumulator. It is included with the accumulator in rotate operations and in logical shifts.

Program Counter (PC)

The PC determines the program sequence (the order in which instructions are performed). This 17-bit register contains the address of the next instruction.

Operand Address Register (OA)

The Operand Address register is an internal register that contains the address of the location where data is currently being fetched.

Memory Input and Output Buffer Register (MI and MO)

Information is read from a memory cell into the Memory Input register and is interpreted as either an instruction or a data word. Information is read from the CPU into memory through the Memory Output register, and is interpreted as either an address or a data word. The use of two internal 18-bit registers for memory buffer functions allows processor overlap with memory cycle time to decrease execution time and to allow autonomous operation of the CPU and memory. They also allow the I/O processor to gain access to memory between cycles of multicycle instructions. By not having to wait for completion of an instruction, I/O device latency is vastly improved.

Index Register (XR)

The 18-bit Index register is used to perform indexing operations with no increase in instruction time. An indexed operation adds the contents of the Index register to the address field of the instruction operand, producing an effective address for the data fetch cycle. Index value can be positive or negative in 2's complement form (+131,072). The Index register can be used with the Limit register, described in the following paragraph.

Limit Register (LR)

The 18-bit Limit register enables a program to detect loop completion. The base address of a data array is loaded into the Index register and the ending address is loaded into the Limit register. Within an indexing loop, add to index and skip (AXS) instruction adds a signed value ($-256_{10} \leq Y \leq +255_{10}$) to the Index register and compares the sum in the index to the contents of the Limit register. If the contents of the Index register are equal to or greater than those of the Limit register, the next instruction is skipped.

XVM Control Console

The XVM system console contains the controls, switches, and lights required for operator initiation, control, and monitoring of the system. Up to twenty-four 18-bit registers can be displayed to provide the user with visual indication of major registers and buses.

Some of the features of the console are:

- A READ-IN switch to initiate the hardware reading of the bootstrap devices.
- REGISTER indicators and REGISTER DISPLAY switches to allow continual monitoring of key points in the system such as the accumulator, Index register, Limit register, Multiplier-Quotient register, Program Counter, memory address, interrupt status, input/output bus, input/output address, and I/O status.
- Separate ADDRESS and DATA switches to establish an 18-bit data or instruction word to be read into a memory location by the DEPOSIT switch, to be entered into the accumulator by a program instruction, or to be executed by the EXECUTE switch.
- EXAMINE switch to allow the manual examination of the contents of any memory location placed in the ADDRESS switches.

KE15 EXTENDED ARITHMETIC ELEMENT (EAE)

The KE15 Extended Arithmetic Element (EAE) is a standard XVM feature which facilitates high-speed arithmetic operations and register manipulations. The EAE uses an 18-bit Multiplier-Quotient register (MQ) as well as a 6-bit Step Counter register (SC). EAE instructions can be microcoded so that several operations are performed by one instruction to simplify arithmetic programming and reduce execution time.

Multiplier-Quotient Register (MQ)

The Multiplier-Quotient register and accumulator perform as a 36-bit register during shifting, normalizing, multiplication, and division operations. The contents of the Multiplier-Quotient register are displayed by the REGISTER indicators on the operator's console when the REGISTER DISPLAY control is in the MQ position.

During the multiply instruction, the MQ receives the 18 least significant bits of the double word product formed in the AC and MQ. During the divide instruction, the MQ is the least significant 18 bits of the double word DIVIDEND formed by the AC and MQ.

Step Counter (SC)

The Step Counter is used to count the number of steps in an EAE instruction. The step counter is preloaded, except during normalize operations, with the numbers of steps specified by an instruction and is counted down as the instruction is executed. When the SC reaches zero, the EAE operation is terminated.

PROCESSOR EXPANSION

KF15 Power Failure Protection

The basic XVM is not affected by power interruptions of less than 10 ms duration. Active registers in the processor may lose their contents when interrupts of longer duration occur, but memory is not disturbed. The KF15 Power Failure feature, standard on all XVM systems, allows the preservation of the active register contents in the event of longer power interrupts and the automatic restart of the system when power is restored. When the line power failure occurs, the system must be operating with the program interrupt facility or the automatic priority interrupt system enabled in order to sense the KF15's initiation of a program interrupt in time to save the register contents. When power is restored, the processor automatically restarts and the instruction in location 0 is executed.

1.2 ADDRESSING

The following paragraphs explain XVM addressing modes and formats.

Words in Memory

Words stored in magnetic core memory are simply strings of 18 bits. There is no method of distinguishing between an instruction word and a data word. The Central Processor Unit (CPU), which decodes and operates an instruction word, can differentiate between instruction and data words because of the sequence in which they appear at the CPU, from memory.

To keep track of the sequence, the processor is provided with a Program Counter which normally holds the address of the next location in sequence in the memory. The word thus located, may point to another location that is the address of a data word or instruction.

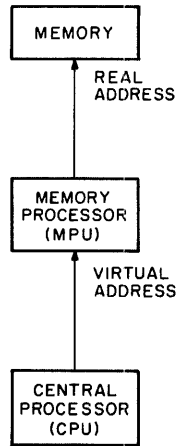
There are three main types of instructions:

1. Instructions that reference memory indicating in the operand address field the (virtual) location of the data necessary to complete the instruction. For example, ADD the contents of location 000100 to the accumulator.
2. Instructions that deal with control, and do not require a memory access. For example, RAL: Rotate the accumulator and link one place to the left.
3. Instructions that reference peripheral equipment, and cause information transfers to or from the devices, termed IOT's. For example, TLS: Load console terminal print buffer from AC10-17, and start printing.

Addresses

There are two types of addresses: real and virtual. The XVM system uses both types in a variety of ways to facilitate as many operations as possible (Figure 1-2).

Virtual addresses are those calculated by the CPU and sent to the Memory Processor Unit (MPU). Virtual addressing makes it possible for many users to obey the same rules, use the same addresses, and yet all can use the XVM system at the same time. The virtual addresses are accepted by the MPU and modified if necessary, depending upon which manner of addressing is currently set up within the MPU. The resulting address is then sent to memory as a real address. A real address corresponds to the required location in memory, as shown in Figure 1-3.



15-0822

Figure 1-2 Real and Virtual Addresses

	LOCATION	PAGE	BANK	BLOCK	
0	0	PAGE 0	BANK 0	BLOCK 0	
4K	7777 10000	PAGE 1			
8K	17777 20000	PAGE 2	BANK 1		
	27777 30000	PAGE 3			
16K	37777 40000	PAGE 4	BANK 2		
	47777 50000	PAGE 5			
24K	57777 60000	PAGE 6	BANK 3		
	67777 70000	PAGE 7			
32K	77777 100000				
					BLOCK 1
64K	177777 200000				BLOCK 2
	277777 300000				BLOCK 3
128K	377777				

MEMORY ADDRESSING
PAGE = 4K LOCATIONS
BANK = 8K LOCATIONS
BLOCK = 32K LOCATIONS

MEMORY ADDRESSING
 PAGE = 4K LOCATIONS
 BANK = 8K LOCATIONS
 BLOCK = 32K LOCATIONS

15-0184

Figure 1-3 Memory Addressing

1.2.1 XVM CPU Addressing Modes

The XVM Central Processor produces an address in a variety of ways which are described briefly in the following paragraphs to assist the reader in understanding the whole addressing picture. Detailed programming examples are provided in paragraph 1.2.3.

To start with, assume that virtual addresses are un-modified by the MPU.

Direct Addressing: Type I

A direct address (Figure 1-4) is the most basic type of address. The address field is either 13 or 12 bits long, depending upon whether the XVM CPU is in Bank or Page mode respectively. This type address is usually termed an operand address, because an instruction normally occupies bits 00 to 03.

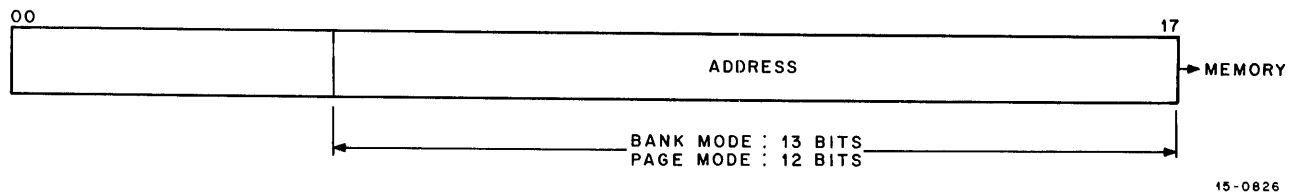


Figure 1-4 Direct Addressing: Type I

Indirect Addressing: Type II

An indirect address (Figure 1-5) is more complex than the direct address. The operand address (in the upper box) contains the address of a location, which in turn contains an address of a data word. The width of the address that is passed to memory depends upon the conditions prevailing in the MPU at that time. Normally, either 15- or 17*-bit addressing is selected by the monitor's software.

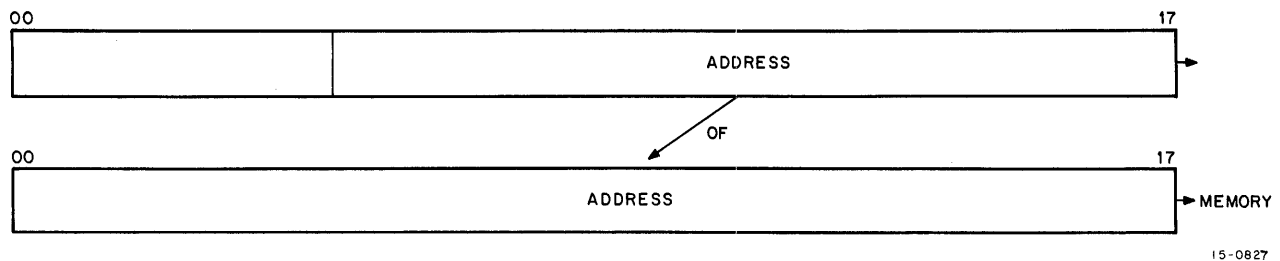


Figure 1-5 Indirect Addressing: Type II

Auto-Increment Addressing: Type III

The auto-increment address (Figure 1-6) is a special type of indirect addressing. If any one of the addresses 00010 to 00017 should be addressed indirectly, the contents of this "auto-increment" location will be extracted, incremented, and restored. This value is then used as the address of the required data word. When these auto-increment addresses are accessed in any other way, they function as other locations. This feature facilitates the processing of sequential strings of data.

Note that the actual core memory locations affected by the auto-increment process are determined by the current settings of the MPU.

*16- and 18-bit addressing is permitted, but it is not used by current DEC software.

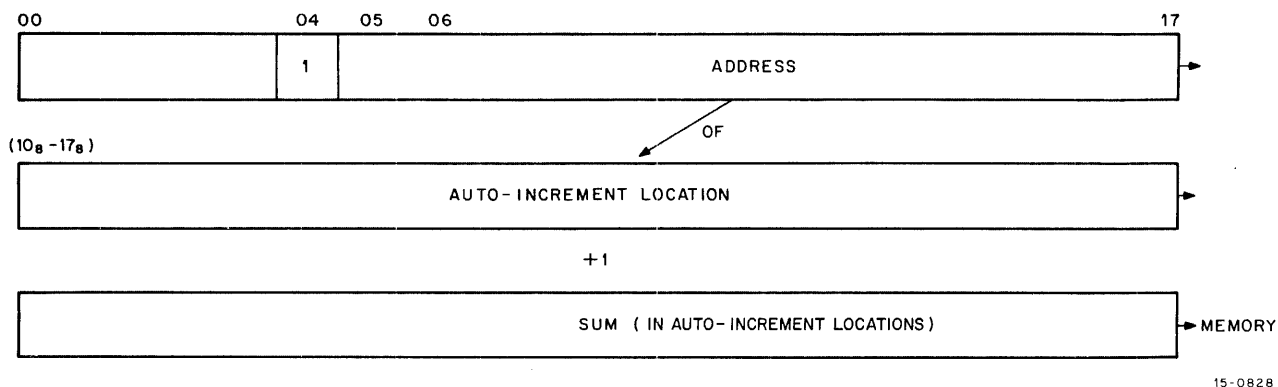


Figure 1-6 Auto-Increment Addressing: Type III

Indexed Addressing: Type IV

Indexed addressing (Figure 1-7) makes use of the Index register to address up to 131072 locations. Bit 05 is used to indicate that an indexed reference is being made. It follows that the XVM CPU must be running in Page mode to enable this mode of addressing. The operand address is concatenated with PC01-PC05, from the Program Counter (PC). The result is added to the contents of the Index register (XR) and the sum is used as the memory address. Note that the contents of the Index register may be negative.

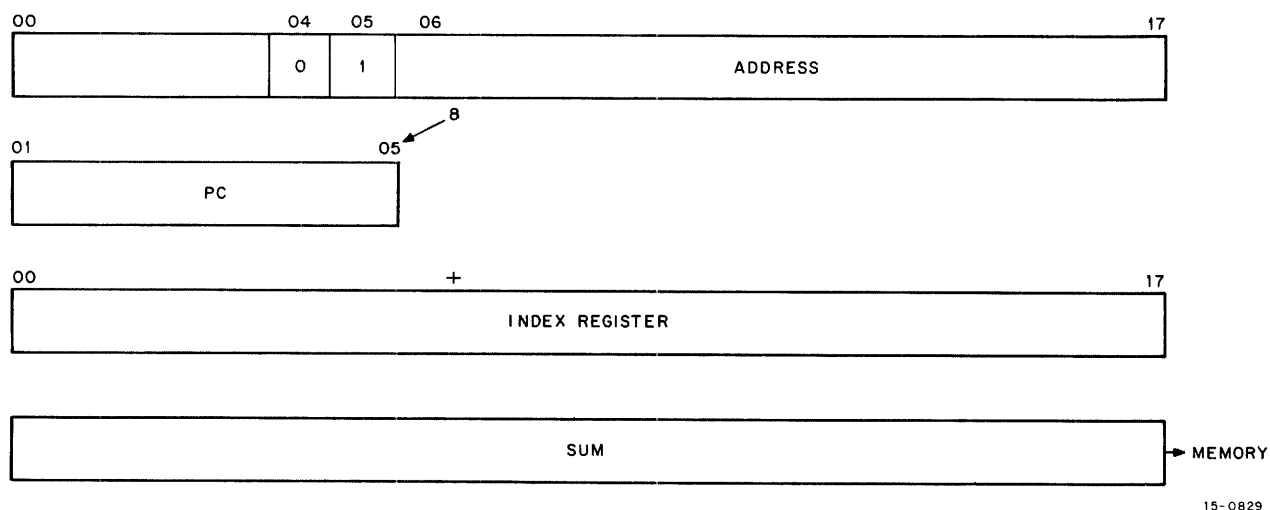


Figure 1-7 Indexed Addressing: Type IV

Indirect-Indexed Addressing: Type V

Indirect-indexed addressing (Figure 1-8) is the first of the composite types of addressing. The 12 bits of operand address point to (i.e., contain the address of) a location that holds an address. This second address may be 15 or 18 bits wide, depending on the internal settings of the MPU. This address has the contents of the Index register (18 bits) added to it, and the result is sent to the MPU. This will again affect the address such that either 16, 17, or 18 bits of address will be presented to the memory.

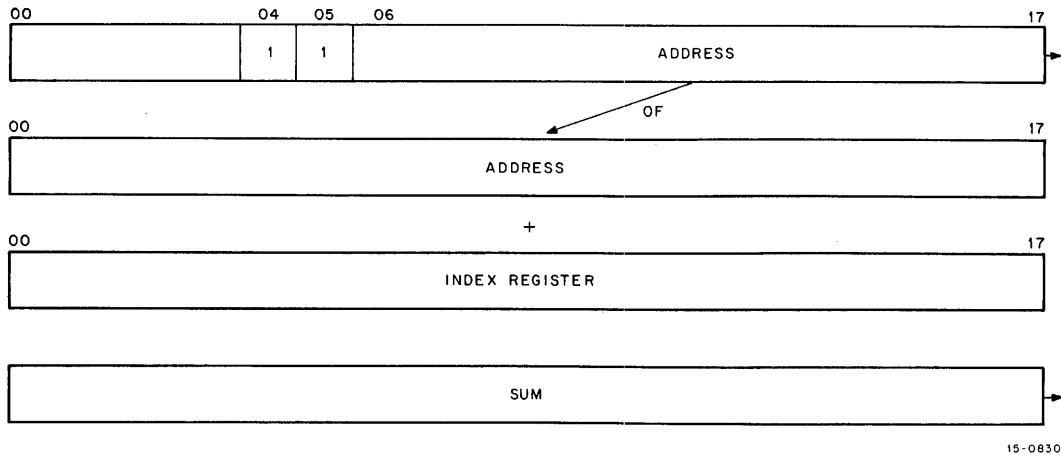


Figure 1-8 Indirect-Indexed Addressing: Type V

Auto-Increment, Indexed Addressing: Type VI

This is the most complex type of XVM CPU address formation (Figure 1-9). The operand address (between 10_8 and 17_8), when referenced indirectly, becomes the pointer to an auto-increment location, the contents of which are incremented by one, and used as an address. The contents of this location has the current value of the Index register added to it, and the sum is used as the final address to be sent to the memory via the MPU.

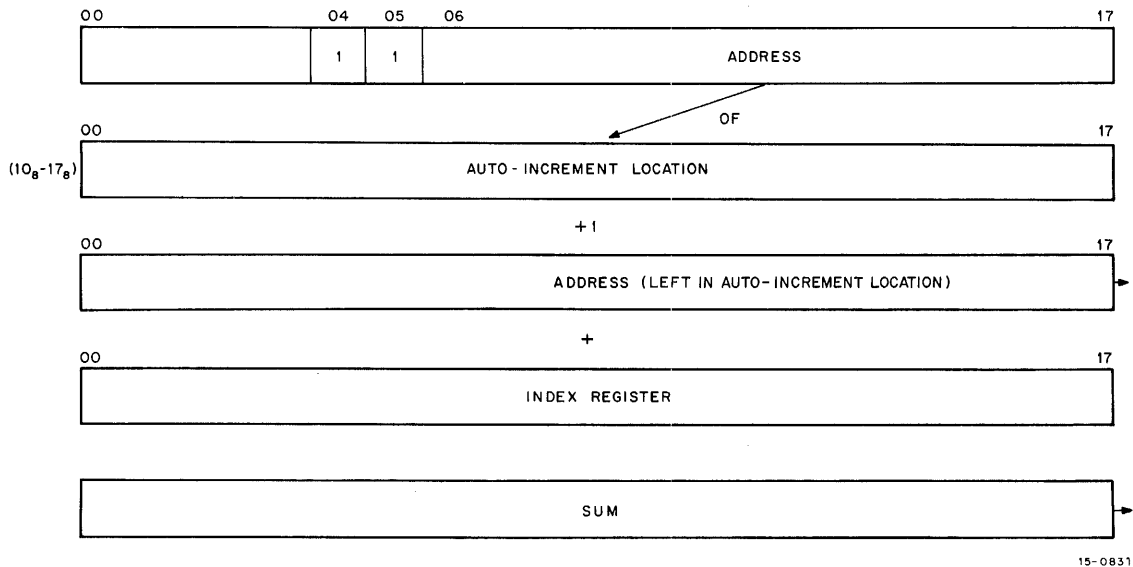
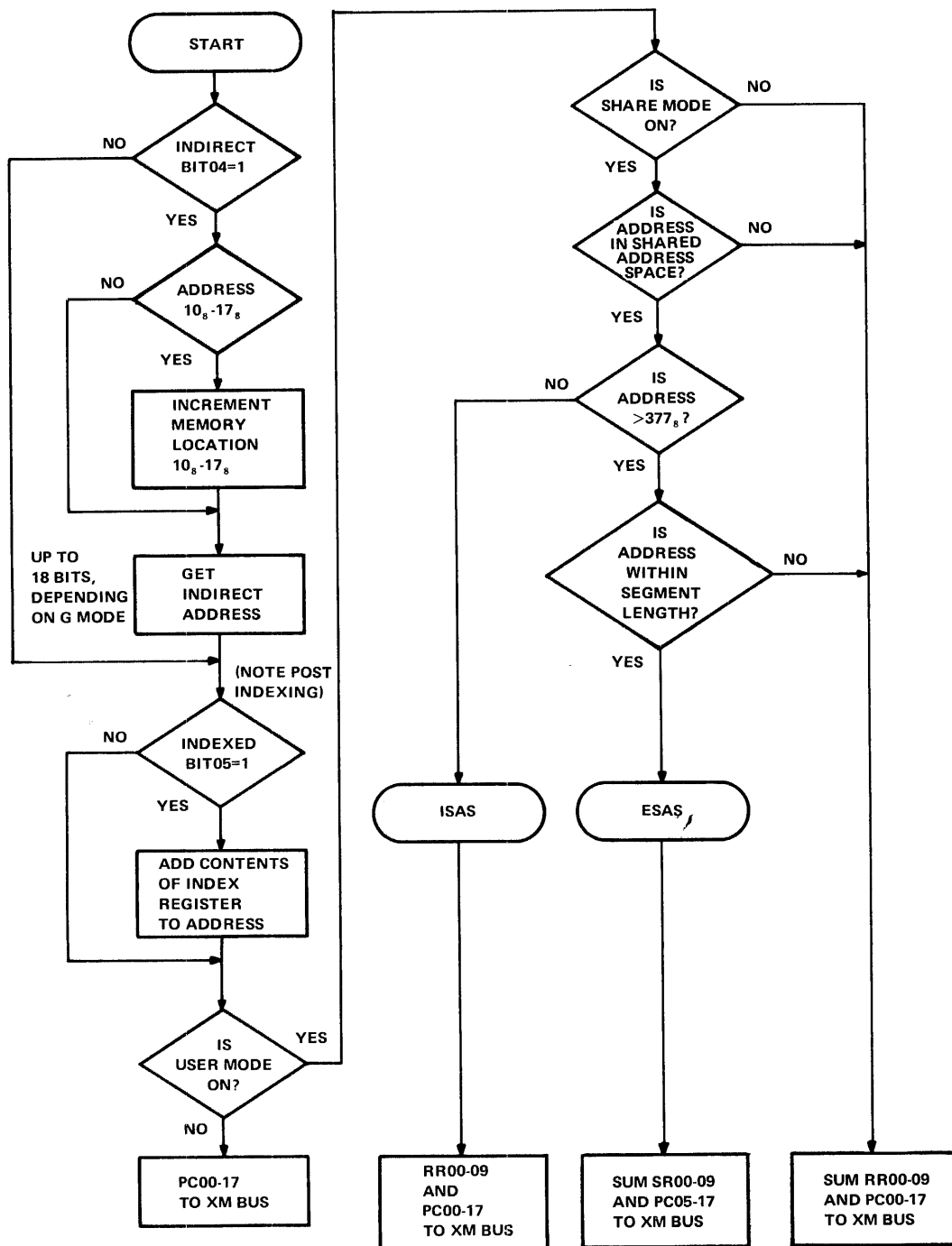


Figure 1-9 Auto-Increment, Indexed Addressing: Type VI

In summary, there are six XVM CPU addressing modes. These are designated Type I through Type VI, in order of their complexity. Figure 1-10 is a flow chart of the address modification sequence.



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Figure 1-10 Address Modification Flowchart

1.2.2 XVM MPU Address Mapping

The following paragraphs briefly describe the four ways that the XVM MPU changes virtual addresses to real addresses before sending the addresses to core memory. The MPU performs a wide variety of functions. However, the majority of these functions are only operative when the system is in User mode (for a full description of User mode, see Chapter 2, Section 1).

There are four ways that the virtual address presented by the CPU can be converted to a real address:

Direct Mapping (DMAP)

Refer to Figure 1-11. In this mode, the CPU-generated address is passed through the MPU and no modification takes place. This form of addressing is in effect whenever the system is in either of the two following states; first, when the system is in the Executive mode of operation, which means that none of the memory management functions are being used; second, when the system is in User mode, but the Relocate Disable (RDIS) function is operative.

Relocated Mapping (RMAP)

Refer to Figure 1-12. The system, to be in this category of addressing, must be in User mode, and relocation must be enabled (RDIS is false). The addresses presented by the XVM CPU have the contents of another register added to them, so that the correct partition* is accessed. The Relocation register (RR00-RR09) holds the equivalent of an “offset,” which is used to map the virtual address to the user’s area of core.

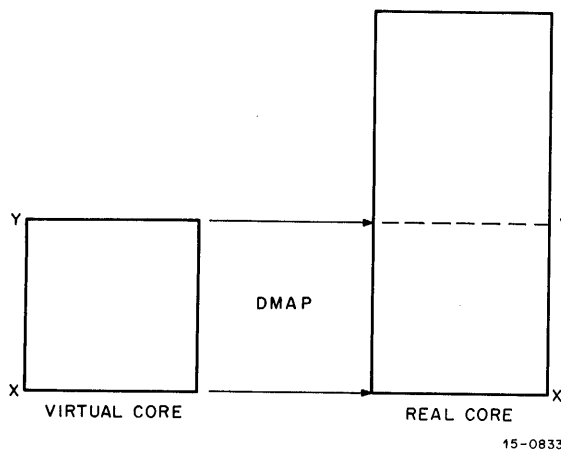


Figure 1-11 Direct Mapping (DMAP)

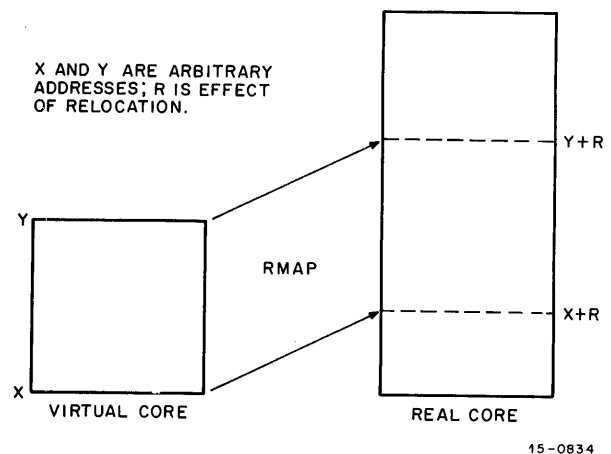
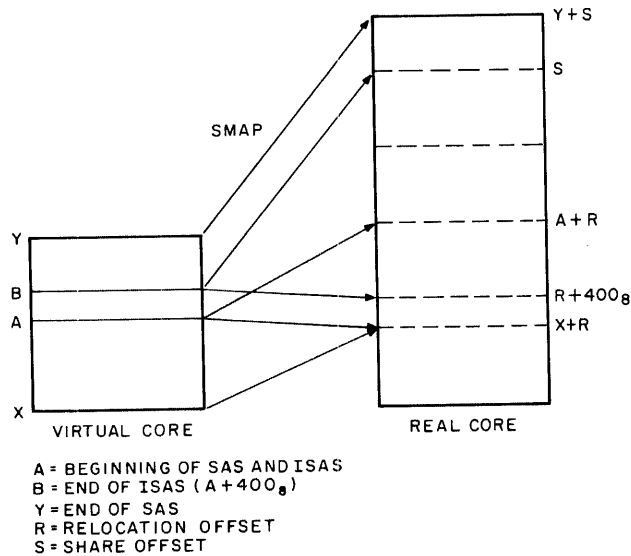


Figure 1-12 Relocated Mapping (RMAP)

Shared Mapping (SMAP)

Refer to Figure 1-13. This particular form of address manipulation is the most complex of the XVM addressing schemes. When the system is in User mode and Share mode, the virtual addresses issued by the XVM CPU are examined by the MPU to determine if they lie within the Shared Address Space (SAS). The SAS is defined by two limits; the starting address of the SAS is a function of the G-Mode bits, and the length of the SAS is held by the Segment Length register (SLR). If the CPU address is within the SAS, and furthermore if it is within the first 400₈ locations, then the CPU is referencing the Internal Shared Address Space (ISAS). The address (bits 10-17) is combined with the contents of the Relocation register (RR00-09) and the result is sent to the memory. The location accessed will be within the first 400₈ locations of the user’s partition.

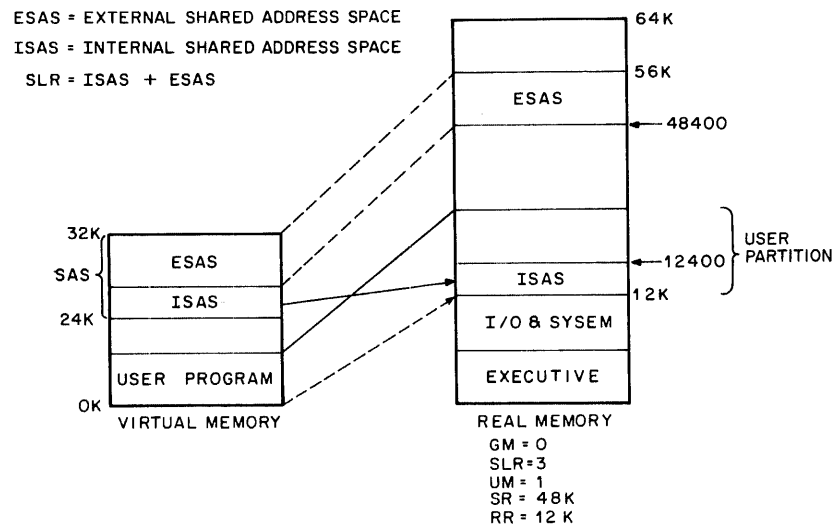
*“Partition” refers to the area of real memory that has been assigned to that particular program.



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Figure 1-13 Shared Mapping (SMAP)

Refer to Figure 1-14. If the XVM CPU address happens to be within the limits of the SAS, but not within the first 400₈ locations thereof, then the CPU is said to be accessing ESAS (the External Shared Address Space); to reach this area, the CPU address (bits 05-17) is added to the contents of the Share register (SR00-09), which holds another “offset” similar to the Relocation register. The sum of these is then sent to memory.



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Figure 1-14 External Shared Address Space (ESAS) Example

Boundary Mapping (BMAP)

Refer to Figure 1-15. To use the facilities of this separate, special type of mapping, the XVM CPU and MPU must be configured as a “P-Mode” system. The previous two methods of address modification, RMAP and SMAP operate only while the system is configured as an “R-Mode” system.

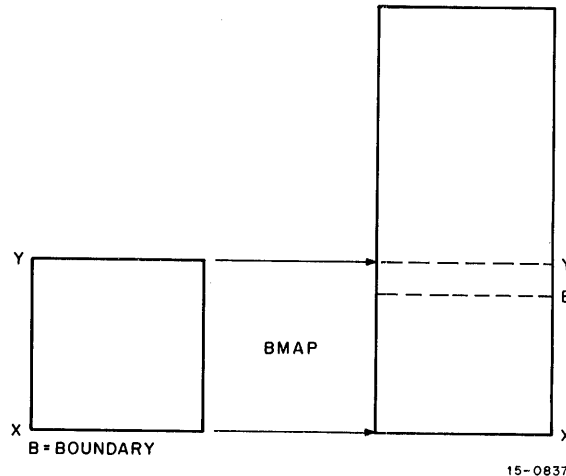


Figure 1-15 Boundary Mapping (BMAP)

The XVM system, when in BMAP, establishes a boundary in real core below which access is prohibited. This type of mapping is normally used in specialized applications.

There is another register that is used by the RMAP, BMAP, and SMAP categories, called the Boundary register (BR00-09). It specifies the virtual address that is considered to be the upper limit of the user's partition or the lower limit of the user's allowable memory area in BMAP operation. If an attempt is made to map a virtual address to a real address beyond the zone established by the Boundary value, the XVM CPU will TRAP, because of the boundary violation. The TRAP is an alarm condition which informs the CPU that a violation of some kind exists and must be rectified.

1.2.3 Addressing Examples

Programming examples for each type of addressing (Type I through Type VI) are provided in the following paragraphs. In these examples, it is assumed that the MPU does not modify the address received from the XVM CPU.

Short program examples are also provided to illustrate the effects of the MPU in different address mapping modes.

Direct Addressing, Type I – Bank or Page Mode

The XVM uses bits 5 through 17 in Bank mode, or bits 6 through 17 in Page mode, as the effective address (EFA) for direct addressing.

The following example illustrates direct addressing:

PC	Instruction	
000100	202222	(LAC 02222)

In the example, the instruction fetched from location 000100 specifies “load the AC with the contents of location 2222.” Direct addressing is indicated, and the EFA is 002222.

Indirect Addressing, Type II – Bank or Page Mode

Indirect addressing is specified when bit 4 of a memory reference instruction is set. Some of the frequent uses of indirect addressing include building or retrieving blocks of data in core memory and referencing memory locations outside of the page or bank containing the program.

The following examples illustrate indirect addressing (* Specifies indirect addressing):

PC	Instruction	
000200	221111	(LAC* 01111)

The instruction fetched from location 000200 specifies “load the AC with the contents of the memory location specified by the contents of 01111 (located in page 0 of bank 0).” If location 01111 contained 000300, the EFA would be 000300, and the contents of 000300 would be loaded into the accumulator.

Indirect addressing enables the user to reference any memory locations in core, depending on the setting of the MPU. In the above example, memory location 300 can be referenced in any memory page by specifying the page in address bits 3,4, and 5:

PC	Instruction	
000200	221111	(LAC*01111)

If location 01111 contains 070300, the contents of location 300 in page 1 of bank 3 are loaded into the accumulator.

Auto-Increment Addressing, Type III – Bank or Page Mode

Whenever addresses 000010 through 000017 are indirectly referenced by an instruction, the content of the location is incremented by one before it is used as the operand. The auto-increment feature is performed only when the location is referenced indirectly. The locations act as any other memory location when referenced directly.

An auto-increment operation can be initiated from any page, bank, or block of memory. The XVM auto-increments whenever a memory reference instruction specifies indirect addressing, and the address points to any location from 000010 through 000017.

NOTE

The Auto-increment register is incremented before the content is used as the operand address.

Programming examples:

Auto-increment from page 0, bank 0, block 0, and read the data word stored in location 001000 into the accumulator.

Step 1	Set the Auto-increment register to the operand address value -1. In this case, 000777.
Step 2	Reference the Auto-increment register with indirect addressing specified.
Step 3	The Auto-increment register increments by one, and the EFA is now the new value (001000) in the register.

Steps 1, 2 and 3 are represented in assembly language form as:

Step 1	{ LAC	K777	/Auto-increment register 10
	{ DAC	10	/C(001000) loaded into AC
	LAC*	10	
	.		
	.		
	K777	000777	/Constant for initialization

When operating from a memory bank other than bank 0, the initial contents of the Auto-increment register must be set up using indirect addressing. If direct addressing is used, locations 10 through 17 of the bank containing the program are referenced. For example, if operating in bank 2, Step 1 in the previous example must be modified as:

Step 1	LAC	K777	
	DAC*	K10	/Deposit in location 10 of 1
			/page 0, bank 0
Step 2, 3	LAC*	10	/C(001000) loaded into AC
	.		
	.		
	K777	000777	/These constants are located
	K10	000010	/in the same memory bank as
			/the main program

Indexed Addressing, Type IV – Page Mode Only

The XVM Central Processor has an 18-bit Index register (17 bits + sign) and an 18-bit Program Counter with appropriate data paths and adder circuitry to compute 17-bit effective addresses.

Indexed addressing can only be used in Page mode operation and is indicated when bit 5 of a memory reference instruction is set. With this type of addressing, the user gains access to 131,071 memory locations (000000 through 377777 octal) without adding an additional memory cycle to compute the effective address (as does indirect addressing).

The following example illustrates indexed addressing:

PC=003000	LAC	100,X	/(210100 octal)
XR=000100			

The instruction fetched from location 3000 specifies “load the AC with the content of the effective address calculated by adding PC01-05 (00), the XR (100) and the address field of the instruction (100).” This results in an effective address of 000200 because:

000100	(XR)
<u>+000100</u>	(PC ₁₋₅) + (ADDR)
000200	(EFA)

If operating in an extended memory bank or block, indexed addressing can be used to reference other pages, banks, or blocks above or below the operating area.

Programming example:

The program is operating in block 2, bank 0, page 1 and must reference location 1000 in block 3, bank 3, page 1 (location 371000):

PC=213000 LAC 1000,X /(211000 octal)
 XR=160000

The EFA is calculated in the following manner:

$$\begin{array}{rcl}
 160000 & & (\text{XR}) \\
 +211000 & & (\text{PC}_{1-5}) + (\text{ADDR}) \\
 \hline
 \text{EFA}=371000 & & (\text{block 3, bank 3, page 1, location 1000})
 \end{array}$$

The program is operating in block 2, bank 0, page 1, and must reference location 1000 in block 0, bank 0, page 0 (location 001000):

PC=213000 LAC 1000,X /(213000 octal)
 XR=570000 (negative value)

The EFA is calculated by:

$$\begin{array}{rcl}
 570000 & & (\text{XR}) \\
 +211000 & & (\text{PC}_{1-5}) + (\text{ADDR}) \\
 \hline
 \text{EFA}=001000 & & (\text{block 0, bank 0, page 0, location 1000})
 \end{array}$$

NOTE

The XR contains a negative value. In this case, it is the 2's complement value of the current block, bank, and page. All 18 bits (17 bits + sign) of the XR are involved when using indexed addressing. The EFA of the last example can also be calculated in the following manner:

$$\begin{array}{rcl}
 \text{PC}=213000 & \text{LAC} & 200,X & /(210200 \text{ octal}) \\
 \text{XR}=570600 & & & \\
 \\
 570600 & & (\text{XR}) & \\
 +210200 & & (\text{PC}_{1-5}) + (\text{ADDR}) & \\
 \hline
 001000 & & \text{EFA} &
 \end{array}$$

Indirect Indexed Addressing, Type V – Page Mode Only

Indirect indexed addressing is implemented only in Page mode and is indicated when both the indirect addressing indicator (bit 4) and the indexed address indicator (bit 5) of a memory reference instruction are set.

When indirect indexed addressing is indicated, the XVM CPU first calculates the address indirectly referenced. This calculation is done in exactly the same manner as described in the Indirect Addressing paragraph. The XVM carries the address calculation one step further, when indirect indexing is specified. The contents of the Index register are added to the data word which was retrieved indirectly.

The addition (2's complement) of the XR is always the last step to occur (post indexing).

The following example illustrates indirect indexed addressing:

PC=203000 DAC* 100,X /(070100 octal)
XR=000100

location 200100=007000

The EFA is calculated as:

007000	(contents of location 200100)
 +000100	 (XR)
007100	EFA

The instruction fetched from memory location 203000 specifies "deposit the contents of the accumulator into the memory location calculated by retrieving the contents of memory location 200100 (location 100 of the current block, bank, and page) and add the contents of the Index register to the contents of memory location 200100."

The indirect address pointer is calculated by appending bits 1 through 5 of the PC to the 12-bit address (6 through 17) of the instruction word resulting in a 200100 address pointer. An additional memory cycle is required to retrieve the contents (007000) of memory location 200100. The contents of the XR are then added, resulting in a final EFA of 007100.

Auto-Increment Indexed Addressing, Type VI – Page Mode Only

Auto-increment indexed addressing can be implemented only when operating in Page mode. This type of addressing is specified when the indirect address indicator (bit 4) and the indexed address indicator (bit 5) of the memory reference instruction are both set and address bits 6 through 17 equal a value of 10 through 17 octal.

When this type of addressing is specified, the XVM CPU performs the following steps to calculate the EFA:

1. The contents of the Auto-increment register are retrieved, incremented by one, and then restored in the register.
2. The new contents of the Auto-increment register are used as an address pointer.

3. The contents of the XR bits 0 through 17 are added (2's complement) to the address pointer.
4. The sum is used as the final, or effective address (EFA).

The following example illustrates this type of addressing:

PC=170245 DAC* 15,X /(070015 octal)
 000015=000777

 XR=001000

Following the procedure given above, the EFA is calculated as:

000777	contents of location 15	} Step 1
+ 1	increment	
001000	new contents of location 15	
	used as address pointer	
 +001000	contents of XR	Step 3
002000	EFA	Step 4

All of the foregoing assumes that the MPU does not modify the address received from the XVM CPU. A small program is used to illustrate the effects of the MPU in different address mapping modes.

500	BEGIN	LAC	FADD	Relocation Register = 000000
.		DAC	ILOC	Boundary Register = 000000
.		LAC	K	Share Register = 000000
.		DAC*	ILOC	
.		ISZ	ILOC	User Mode* Share Mode*
.		JMP	.-2	G-Mode = 0
.		HLT		
.	FADD	000600		
.	ILOC	000000		
511	K	252525		

Direct Mapping (DMAP)

In DMAP, the constant K is deposited first in location 600₈, and then every succeeding location until the system runs out of memory. When the program attempts to access the last location +1, the system will TRAP to location 20₈ absolute, or 0₈ if Program Interrupt Enable is on. A pointer, in one or both of these locations, should point to a service routine to handle the "alarm" type conditions.

Relocated Mapping (RMAP)

Relocation Register = 007400
 Boundary Register = 020400
 Share Register = 000000
 User Mode = 1 RDIS = 0
 Share Mode = 0
 G-Mode = 0

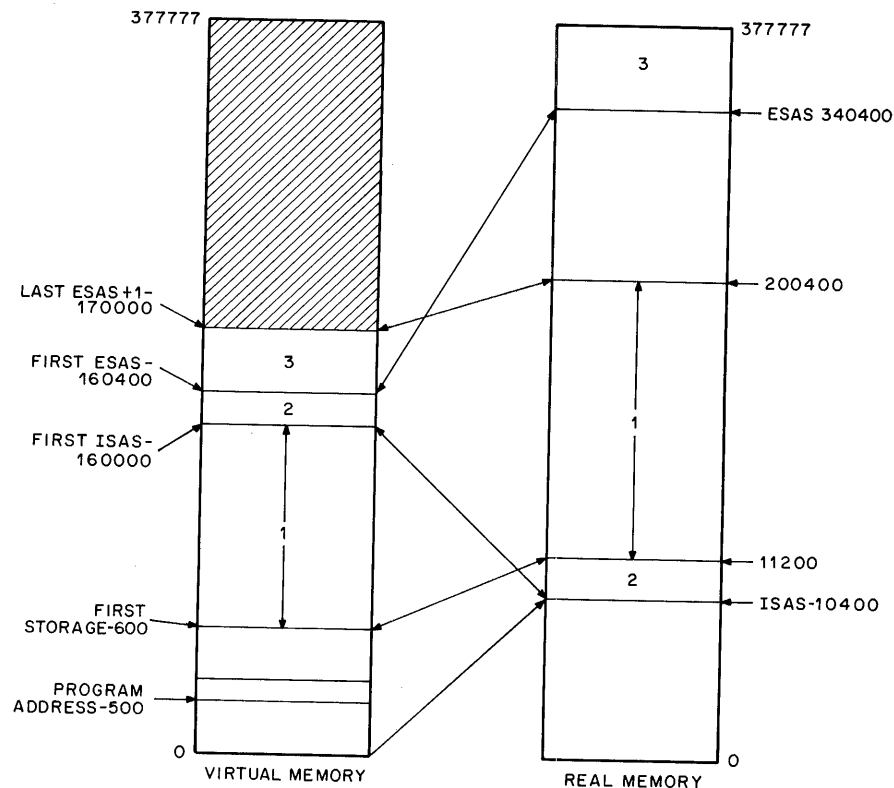
In RMAP, the first real address to have the constant deposited in it would be 010200 (FADD + RR). The system will then continue depositing the constant in sequential locations until it attempts to access location 020400 (virtual), at which point the system will be interrupted by the Boundary Violation which causes a TRAP to 0 or 20₈.

Shared Mapping (SMAP)

Relocation Register = 010400
 Boundary Register = 0170400
 Share Register = 340000
 G-Mode = 3

User Mode = 1
 Share Mode = 1
 RDIS = 0
 SLR = 2

In SMAP, the first address to be accessed would be 011200 (Figure 1-16). The system will then continue to deposit until the virtual address 160000 is produced. This will be changed to 010400 and the constant will be stored in the subsequent 377₈ locations. The address was changed because the address 160000 corresponds to the first address of the ISAS. The next significant address will be 160400 which is the first address in ESAS. The address will be modified from 760400 to 340400. This will continue until the end of ESAS is reached by address 167777 (virtual) which is 347777 (real). The next location (170000 virtual) will be relocated to 200400 (real) which will cause a trap because it is above the Boundary register.

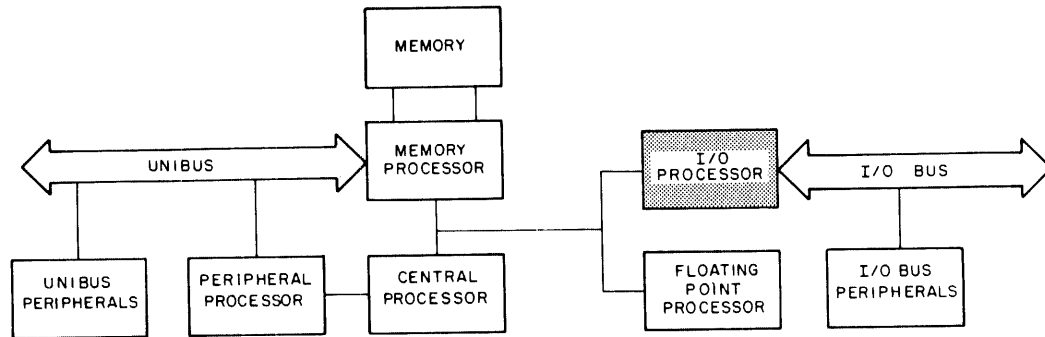


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Figure 1-16 Shared Mapping Example

Boundary Mapping (BMAP)

The BMAP case is less complex than RMAP or SMAP. The program runs as it would normally in DMAP except all virtual addresses are checked to ensure that they are greater than the contents of the Boundary register. Therefore, if the Boundary register was set at 001400, then the contents of location FADD (000600) must be changed to 001400 or greater before the system will execute the program without trapping.



15-0983

1.3 INPUT/OUTPUT PROCESSOR

SUMMARY OF CHARACTERISTICS

The I/O processor contains two subunits, the data channel controller and the addressable I/O bus.

Data Channel Controller

Data Transfer Modes – Single and multicycle block transfer, memory-increment, add-to-memory
Real-Time Clock – KW15

Addressable I/O Bus

Features – Two-cycle skip line, program interrupt, console terminal interface
Data Transfer Modes – Program-controlled data transfers
Device Ports – A maximum of 50 physical ports shared between the data channels and the addressable I/O bus
API – Eight levels of automatic priority interrupts – Four hardware levels and four software levels

I/O PROCESSOR

The I/O processor contains the control logic and registers necessary to transfer up to 18 bits of parallel data on a common bidirectional I/O bus. Data may be transferred directly between the I/O processor and memory, or between the I/O processor and the accumulator (AC) of the CPU. All transfers are made on a request/grant basis, providing complete autonomy of processors and memory. The I/O processor operates with a 1 μ s nominal cycle time.

While transfers are being made between memory and the I/O processor, the CPU is free to operate independently. Requests from the I/O processor for memory access are, however, given priority over CPU requests by the memory bus switch; this can cause the CPU an occasional “cycle-stealing” delay. The structure of the I/O processor provides the following benefits to the user:

- Simultaneous data transfers and CPU computing permits high speed processing to meet the demands of real-time applications.

- User-designed or special-purpose equipment can be easily and inexpensively interfaced to the system.
- Synchronous and asynchronous devices can be handled with equal ease.
- Direct memory access devices that would otherwise require additional interface logic require only one interface with the XVM single cycle data channel.

Modes of Data Transfer

Peripheral devices may transfer data in any one of three modes: single cycle block transfers, multicycle block transfers, and program-controlled transfers.

Block Transfer Controller

The block transfer controller implements the first two modes of data transfers, and in addition, has an add-to-memory mode and an increment memory mode. The real-time clock is also implemented in this section.

Multicycle Block Transfers

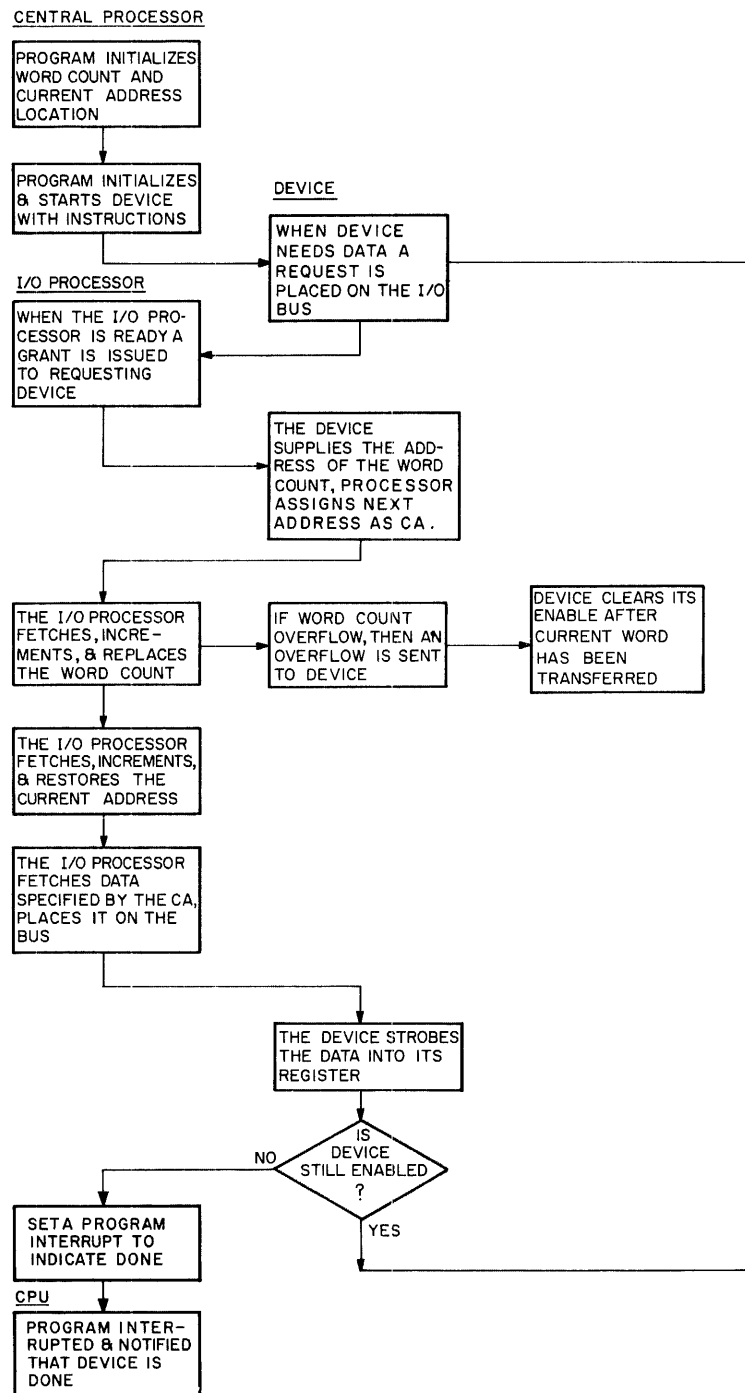
A 2-word packet in core memory is reserved for each of these channels: locations 22 and 23 for the first, 24 and 25 for the second, 26 and 27 for the third, and 30 and 31 for the fourth and so on in standard software systems. The two words in the packet are used to store the "word count" (WC) (number of words to be transferred in the block), and the "current address" (CA) (where the data is to be transferred). The I/O processor contains the control logic and an adder to automatically fetch, increment, and replace the contents of the two locations.

Data is read into memory and out from memory in three I/O processor cycles. Maximum input rate is 170,000 words/second and maximum output rate is 130,000 words/second.

Prior to initiating a multicycle block transfer (flowcharted in Figures 1-17 and 1-18), the program stores the 2's complement of the word count and the current address minus one in the two appropriate memory locations. The transfer is then initiated by an IOT instruction. During the first cycle, the contents of the Word Count location are incremented by one and restored. During the second cycle, the current address is incremented by one and restored, in addition to being transferred to the memory. During the third cycle, the actual data transfer occurs.

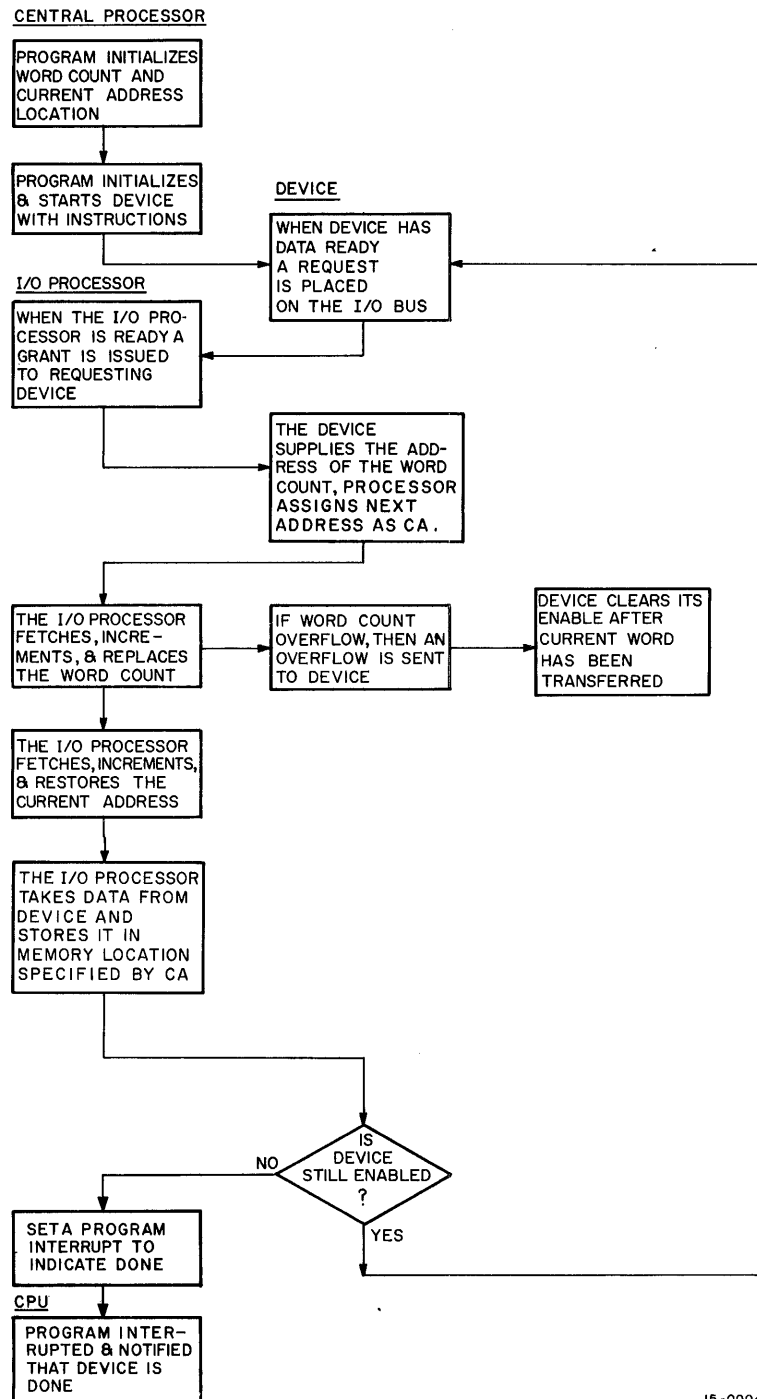
The I/O processor continues to transfer data sequentially until the Word Count register reaches 0, at which time an interrupt is generated to notify the monitor that the block transfer is complete. Because these multicycle block transfers are completely automatic and do not require any CPU attention except for I/O transfer initialization, the CPU is free to compute while they are taking place. The only limitation on simultaneity lies in the sharing of memory. The I/O processor has first priority on memory requests and effectively "locks out" the CPU for three cycles. As data transfer rates approach maximum, the CPU can be completely locked out.

Figure 1-19 illustrates how the data channel controller registers implement the multicycle transfers.



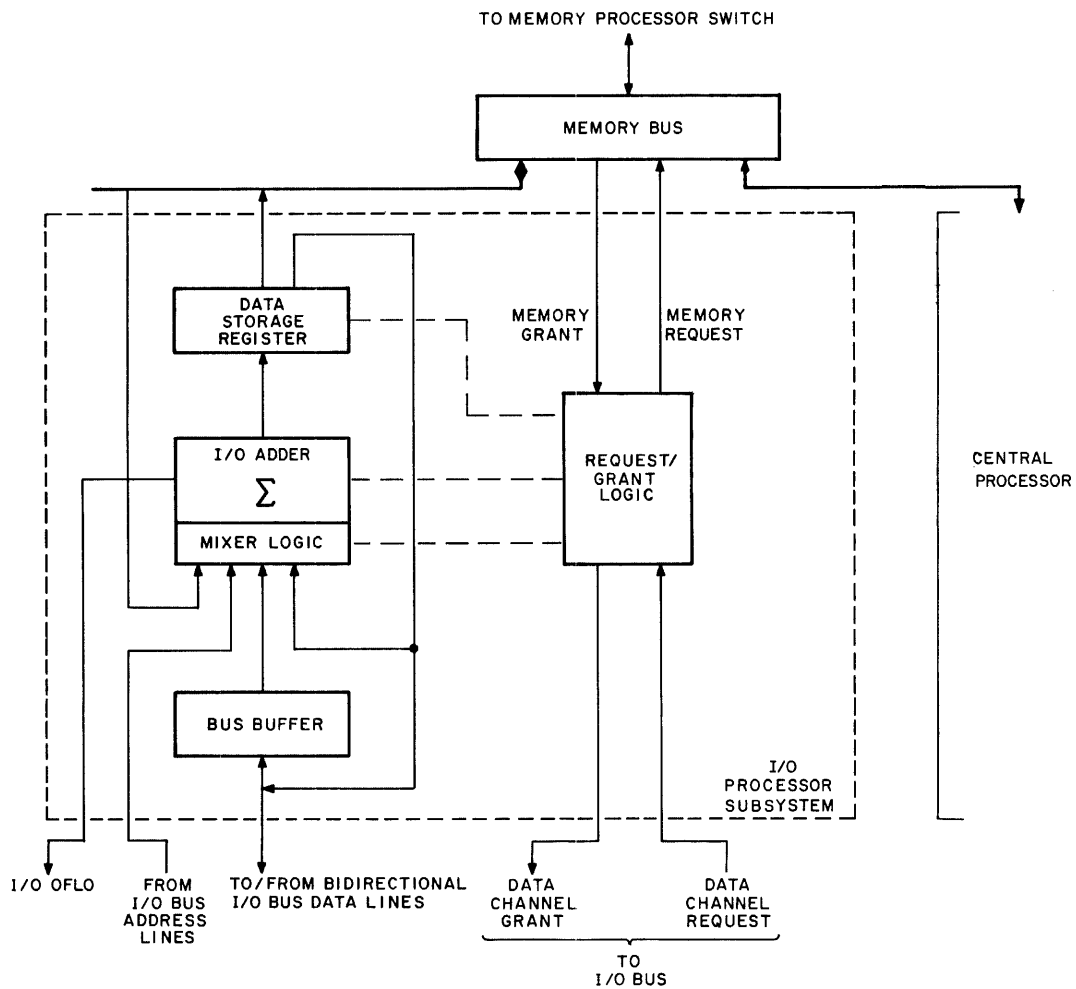
15-0859

Figure 1-17 Multicycle Out Block Transfer Flowchart



15-0004

Figure 1-18 Multicycle Transfer Implementaion



15-0005

Figure 1-19 Multicycle Transfer Implementation

Assume the 2-word core memory packets assigned to a given multicycle data channel have been loaded by the respective I/O service routine. For the case of data input to memory, the following occurs:

1. An instruction from the service routine enables the device controller. This allows the controller to request a data transfer from the I/O processor.
2. When the device controller's data buffer registers are full, it issues a "data channel request."
3. The I/O processor, if not busy, acknowledges the request by returning a "data channel grant."
4. The device controller then generates a fixed code pointing to its packet address in core memory. This is transmitted over the common I/O bus address lines and is stored in the Data Storage register of the data channel controller through the I/O adder. The adder is inhibited during this operation.
5. The I/O processor then generates a "memory cycle request."
6. The address data on the I/O bus address lines points to the word count, the first word of the packet. This data is brought out of memory and into the data channel controller's adder. The word count data word is incremented by one and stored back into memory. If, during this incrementing, the adder overflows (indicating that the current address is the last), then an I/O overflow pulse is transmitted back to the device to disable future data channel requests from the line and also to post an interrupt to the monitor, when the DCH transfer is completed.

This "word count" operation occurs in one I/O processor cycle, using one memory cycle.

During the second I/O processor cycle, the fixed address from the device controller is gated through the adder and is incremented by 1. It points to the second word in the packet, the "current address," which is then transmitted back to the adder, incremented by 1, and strobed back to memory.

During the third I/O processor cycle, the contents of the "current address" location is strobed to the memory to point to the data array word where the I/O data will be transferred. The data is then gated from the device controller, through the adder (which is inhibited during this cycle), and into memory.

Data output follows the same sequence (Figure 1-19) with the exception that one additional I/O processor cycle is required to allow the bus to settle after data is strobed out of memory and into the device.

Single Cycle Block Transfers

Single cycle block transfers, flowcharted in Figure 1-20, are used by high-speed peripherals that normally transfer complete records (blocks) of information, such as disks and video devices. A single cycle of the I/O processor takes approximately 1 μ s, allowing a maximum transfer rate of up to one million 18-bit words per second.

High-speed hardware registers, designed into the device controllers of the high-speed peripherals, store the "current address" (the memory cell where data is currently being transferred), and the "word count" (the number of words remaining to be transferred in a block). These registers are loaded by input/output transfer (IOT) instructions issued by the CPU. Device testing and initialization are handled by the CPU via IOTs to provide supervisory control. A subsequent IOT initiates the data transfer. The I/O processor uses the current address information to address core memory, then strobes the data between memory and the device controller. Logic within the device controller then increments the Current Address register and the Word Count register to provide sequential block transfer.

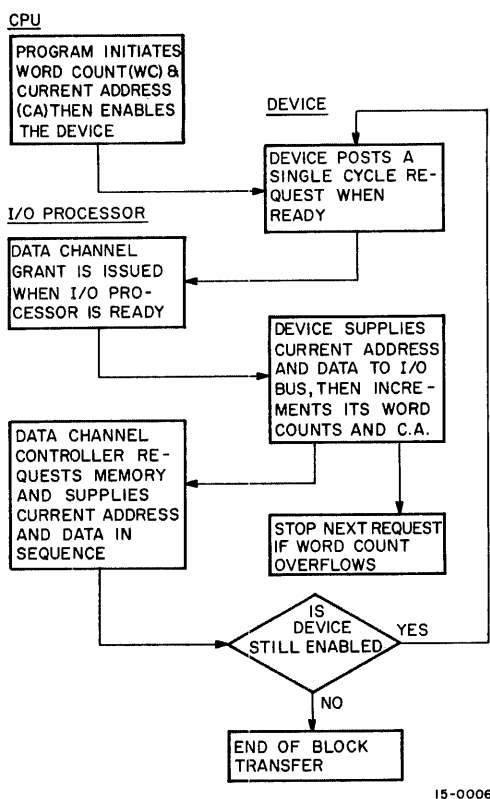


Figure 1-20 Single Cycle Block Transfer Flowchart

When the Word Count register overflows at the end of a block transfer, an interrupt is generated to allow the monitor system to take further action. Typically, this action will include deselecting the device from the I/O bus or reloading the device controller registers for another block transfer. The maximum number of words that may be transferred in a single block is determined by memory size and device capacity.

Figure 1-20 illustrates how the data channel controller registers handle single cycle transfers.

Assuming that the program has initiated the word count and current address of the device controller, and has then enabled it, the following occurs:

1. The device controller sends a single cycle data channel request to the I/O processor.
2. The I/O processor, as soon as it becomes available, acknowledges the request by returning a "data channel grant" signal.
3. The device then strobes both its current address and its data onto the I/O bus to the I/O processor.
4. The data channel controller feeds the current address through its adder (which is inhibited throughout the single cycles) to the Data Storage register. A memory cycle is requested, and this address is strobed into a memory bank's address buffer. The data is then strobed off the 18 I/O data lines and into the memory location specified by the current address.

5. During this operation, the device increments its own word count, and disables itself on overflow. It then posts an interrupt to the monitor to indicate that its operation has been completed.

Burst Mode

The usual method of data transfer is one word per data channel request, whether it is single cycle or multicycle; however, there is one special case.

If the data channel request signal should remain true at the end of the first word (i.e., the device holds it so), then the data channel controller will go into Burst mode (also known as Back-to-Back).

Once in this mode, the CPU is held "locked-out" until the device drops the data channel request signal, and the I/O transfer is completed. This mode will transfer one 18-bit word approximately every microsecond. This mode is only used by certain devices that can handle the 1 MHz rate.

Increment Memory

The Increment Memory mode allows an external device to add one to the contents of any memory location in a single cycle; this feature is most commonly employed in the accumulation of data in histogram form. Effectively, the Increment Memory mode simply goes through the word count cycle of a multicycle channel transfer, and then stops. The maximum rate at which it can increment is 333 kHz. This feature is particularly useful for in-core scaling and counting in pulse height analysis.

Add-to-Memory

Add-to-memory is a standard feature of the XVM that adds unique capabilities to the already powerful I/O facilities. In Add-to-Memory mode, the contents of an external register can be added to the contents of a memory location in four cycles. This feature is extremely valuable in signal averaging and other processes requiring successive sweeps for signal enhancement.

The add-to-memory operation is a combination of multicycle data channel input and multicycle data channel output operations. The data transmitted by the device is added to a word read-out of memory as specified by the current address, and the result is rewritten into the same location. It is simultaneously transmitted to the device via the I/O bus. The maximum add-to-memory rate is 130 kHz.

KW15 Real-Time Clock

When enabled, the KW15 Real-Time Clock counts, in memory location 00007, the number of cycles completed by the line voltage (50 or 60 Hz) or any standard DEC clock module that may be optionally installed. Maximum recommended clock frequency is 10 kHz.

When location 00007 overflows, an internal program interrupt (or API request, if available) is generated, informing the monitor that its preset interval is over. The monitor must either disable the clock or reinitialize location 00007 to the 2's complement of the number of counts it needs to tally.

The incrementing of location 00007 during a real-time clock request occurs via the I/O processor's increment memory facility. A real-time clock request takes priority over API, PI, and IOT requests, but not over block transfers (DCH).

ADDRESSABLE I/O BUS

The addressable I/O bus implements the program-controlled transfers. It also contains the program interrupt and the automatic priority interrupt (API) feature.

Program-Controlled Transfer

Program-controlled transfers, implemented by input/output transfer (IOT) instructions, can move up to 18 bits of data between a selected device and the accumulator (AC) in the CPU. The devices involved are connected to the addressable I/O bus portion of the I/O processor. A total of up to 50 device controllers may be attached to this bus and to the data channel. IOT instructions are micro-coded to effect response only for a particular device. The microcoding includes issuing both a unique device selection code and the appropriate processor-generated input/output pulses to initiate a specific operation. For an "output" transfer, the program reads a data word from memory into the AC. A subsequent IOT instruction places the data on the bus, selects the device, and transfers the data to the device. For an "input" transfer, the process is reversed; an IOT instruction selects the device and transfers data into the AC. A subsequent instruction in the program transfers the word from the AC to memory. Maximum transfer rate in this mode is about 50 kHz.

IOT instructions are also used to initialize the single and multicycle channels and the transfer word count and current address information to the single cycle device controllers. In addition, these instructions are used to test or clear device flags, select modes of device operation, and control a number of processor operations. An IOT instruction, Figure 1-21, contains the following information:

- a. An operation code of 70_8 .
- b. An 8-bit device selection code to discriminate between up to 256 user peripheral devices (selection logic in a device's I/O bus interface responds only to its pre-assigned code). In normal practice, bits 6 through 11 perform the primary device selection between up to 64 device codes. Bits 12 and 13 are coded to select an operational mode or subdevice.
- c. A command code (bits 14 through 17) capable of being microprogrammed to clear the AC and issue up to three pulses via the I/O bus.

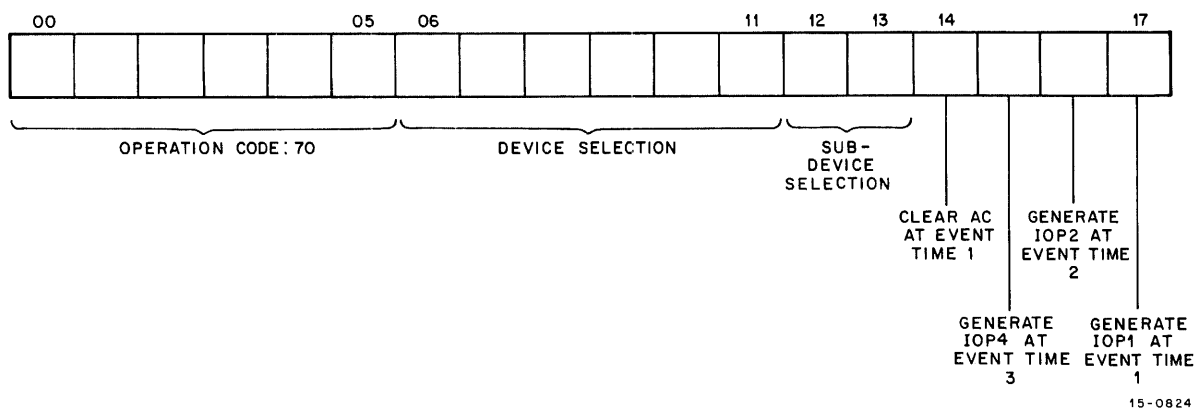


Figure 1-21 IOT Instruction Format

Up to four machine cycles may be required to execute an IOT instruction. These include the IOT fetch from core memory (memory is not accessed thereafter until completion of the IOT), and three sequential cycles designated event times 1, 2, 3 (IOP 1, 2, and 4) (Figure 1-22). In IOT skip instructions, however, only IOP1 is used. These are 2-cycle instructions. Bits 14 and 17 can be coded to initiate clearing of the AC and generation of an IOP1, respectively, during event time 1. Bits 16 and 15 can be coded to initiate generation of an IOP2 and IOP4 pulse during event times 2 and 3, respectively. IOT skip instructions are microprogrammed to produce an IOP1 pulse for testing a device status flag. IOP2 pulses are normally used to effect programmed transfers of information from a device to the processor. Because the AC serves as the Data register for both "input" and "output" transfers, the "clear AC" microinstruction (bit 14) is usually microprogrammed with the IOP2 microinstruction; this combination effects clearing the AC during event time 1. IOP4 pulses are normally used to effect programmed transfers of information from the AC to a selected device. These conventions do not, however, preclude use of the IOP pulses to effect other external functions if the following restrictions are observed.

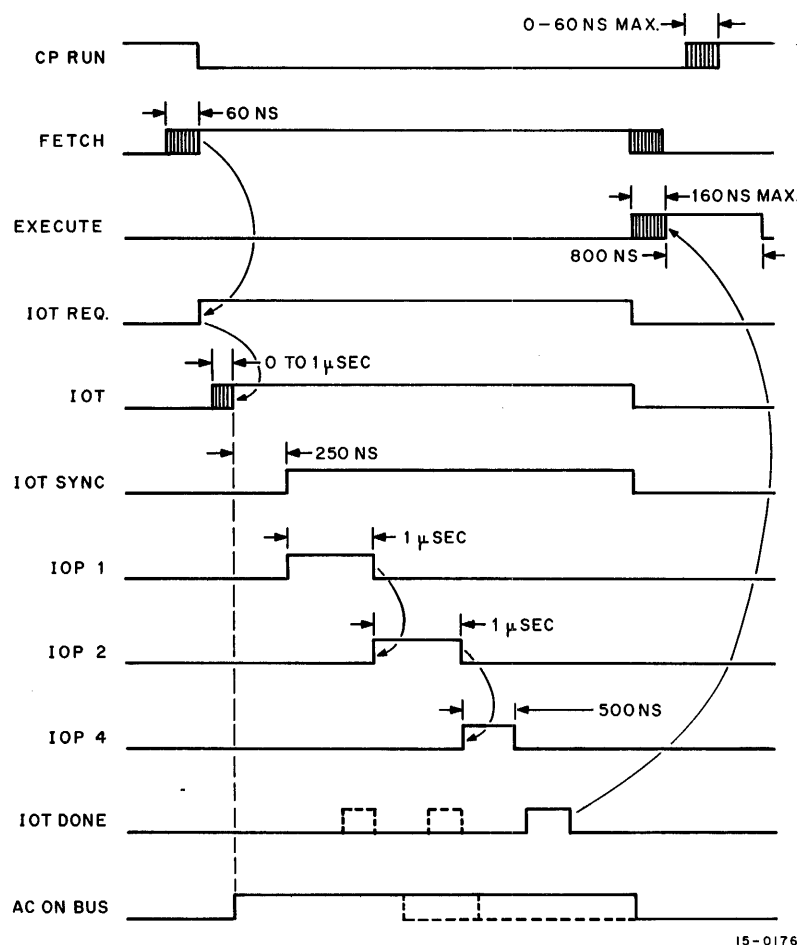


Figure 1-22 IOT Instruction Timing

The uses of IOPs are:

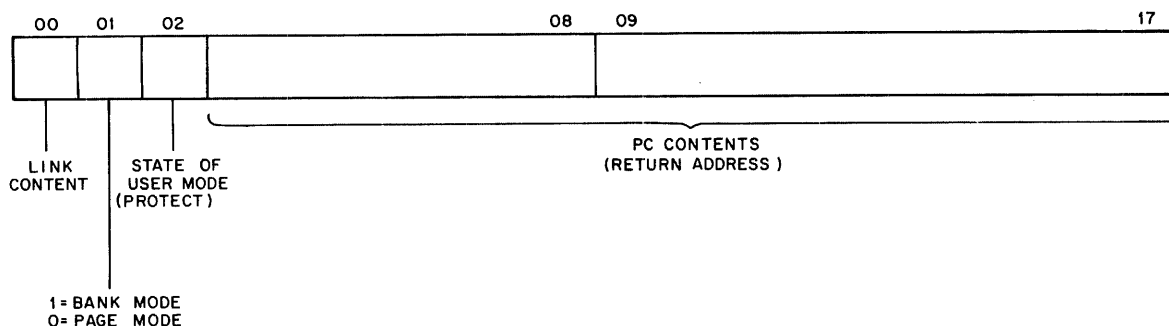
IOP1 – Only used in an I/O skip instruction to test a device flag.

IOP2 – Usually used to transfer data from the device to the computer, or to clear device's Information register. May not be used to determine a "skip" condition.

IOP4 – Used only to transfer data from the computer to the device. May not be used to determine a "skip" condition or to transfer data to the computer.

PROGRAM INTERRUPT FACILITY

The program interrupt (PI) system, standard on all systems, provides for servicing a peripheral device at rates up to 20 kHz. The program interrupt (PI) facility, when enabled, relieves the main program of the need for repeated flag checks by allowing the status of I/O device flags to automatically cause a program interrupt. The CPU can continue with execution of a program until a previously selected device signals that it is ready to transfer data. At that time, the program in progress is interrupted and automatically the contents of the program counter (15 bits), User/Exec mode (1 bit), bank or page addressing mode, and the link bit (1 bit) is stored in location 000000 (Figure 1-23).



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Figure 1-23 Memory Location Just After a Program Interrupt

The instruction in location 000001 is then executed, transferring control to an I/O service routine for IOT instructions. When completed, the routine restores the system to the status prior to the interrupt with a single instruction, allowing the interrupted program segment to continue. Where multiple peripherals are connected to the PI, a search routine containing device status testing (skipping) instructions must be added to determine which device initiated the interrupt request. The program interrupt (PI) control is enabled or disabled by programmed instructions (IOTs). When disabled, the PI ignores all service requests, but such requests normally remain on-line and are answered when the PI is enabled again, unless they are cleared.

Mnemonic	Octal	Code Function
ION	700042	Enable the PI
IOF	700002	Disable the PI

The PI is automatically disabled when an interrupt is granted or when the RESET key (on the console) is pressed. The PI is temporarily inhibited while the automatic priority interrupt system is processing a priority interrupt request. The PI Enable indicator (PIE on the console) is lighted while the PI is enabled.

Free Instruction

When a program interrupt has been accepted, one “free instruction” follows. Simply, this means that program interrupt enable is turned off to prevent another program interrupt from occurring while the hardware is transferring control from one program to the interrupt service routine.

Conditional Skip-On Device Status

The XVM order code includes a group of instructions for testing the status of peripherals. Instructions of this type direct the processor to skip the next instruction if the tested condition is true. This group of instructions allows the test of peripheral devices at the programmer's option. Normally, rather than tying the processor up in a “wait” loop, the device signals that its buffer is ready by generating an interrupt. If it is a program interrupt, the “conditional skip” is used in a “skip chain” to find which device initiated the interrupt. Each skip instruction takes an average of 1.8 μ s.

COMMON I/O BUS

The I/O processor contains a common I/O bus (Figure 1-24) to transfer both data and IOT instructions to the block transfer channels and to the addressable I/O bus. The bus is the major communication path for I/O devices. It consists of cables that link all the I/O device controllers to a common interface point at the I/O processor. All signal lines for command and data transmission arising from the data channels, addressable I/O bus, operation of the multi-level automatic priority interrupt system, program interrupt, I/O status read, and I/O skip facilities, are contained on this bus. The bus length can be up to 75 ft.

Data Lines

Eighteen data lines constitute the bidirectional facility for transferring data bytes of up to 18 bits between the I/O processor and all I/O devices. Transfers are made on a dc basis with the processor or device allowing bus settling time before data on the lines is strobed into the receiving register. The data lines convey data between the Memory Buffer register and a selected Device Buffer register for block transfer channel operation; they transfer data between the accumulator and a selected Device Buffer register for program-controlled transfers.

Output Control Signals

Eight output control signals are generated to effect specific functions in a selected device.

I/O Power Clear

The I/O power clear signal resets all flip-flops storing device-to-processor flag indications (e.g., ready, done, busy). It is generated when power is turned on and off, the occurrence of a clear-all-I/O flags (CAF) instruction, and by actuation of the RESET key on the control console.

I/O Sync

I/O sync is used to synchronize I/O device control timing to the processor.

IOP1, IOP2, IOP4

Microprogrammable signals are used to effect IOT instruction-specified operation within a selected I/O device. The I/O processor generates IOP2 or IOP4 for data channel input or output transfers. The uses of the IOPs are:

IOP1 – To test a device flag (in an I/O skip instruction). It may not be used as a command pulse or to initiate loading, reading from a Device Buffer register.

IOP2 – To transfer data from a selected device to the processor or load a device. Not used for skip.

IOP4 – To transfer data from the processor to a selected Device register. It may not be used to determine a skip condition or to transfer data to the processor.

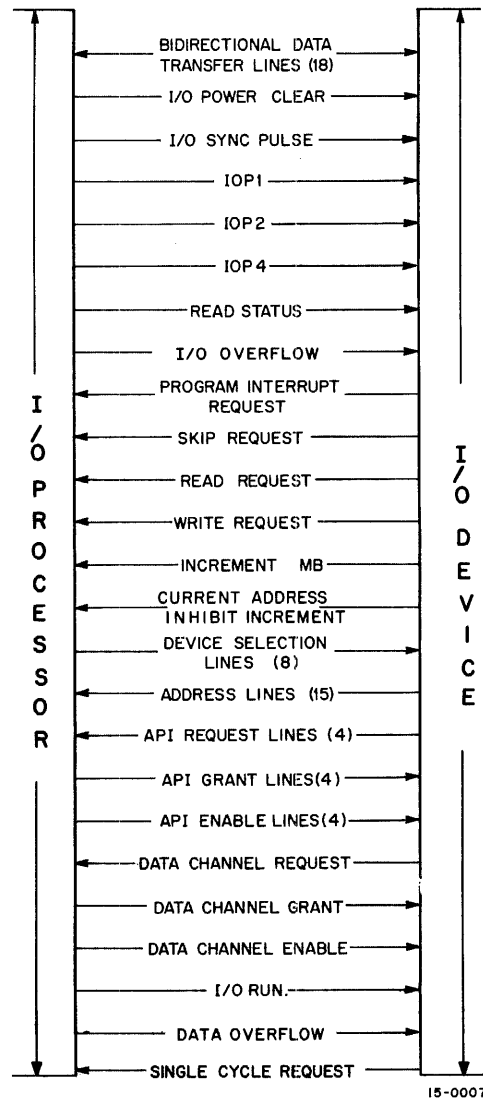
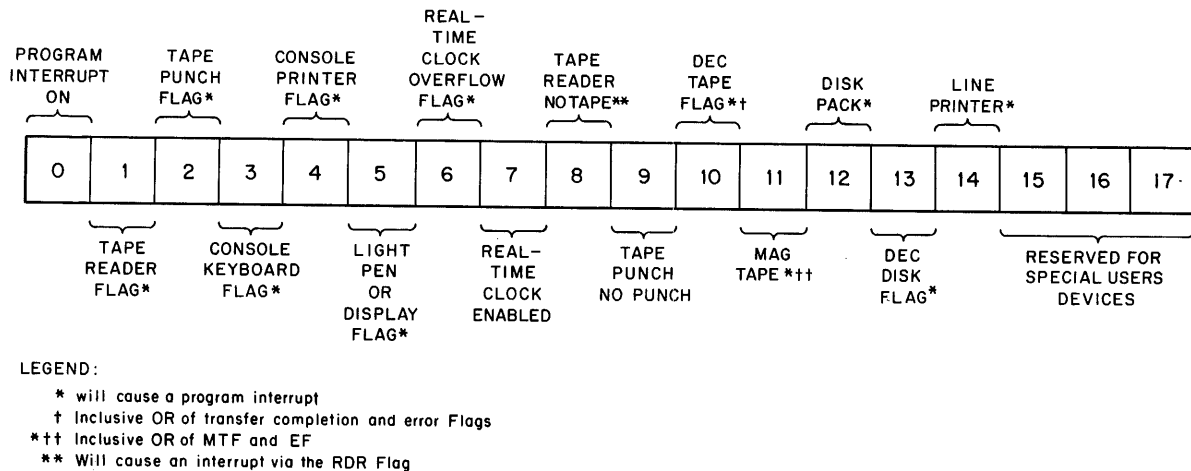


Figure 1-24 Common I/O Bus

Input/Output Read Status

The input/output read status facility provides for programmed interrogation of the status of those external devices using this facility. Upon execution of an input/output read status (IORS) instruction, the states of those device flags (Done, Busy, Not Ready, etc.), interfaced to this facility by the I/O bus, are transferred to specific assigned bit positions of the AC. This allows the program to check for specific flag conditions or display the flag states on the operator's control console. Figure 1-25 shows the bit positions associated with the commonly interfaced flags. The IORS word can contain up to 18 flag bits. Those bits not used are zeroed. The presence of a flag is indicated by a 1 state in the corresponding AC bit.

Switching the REGISTER DISPLAY control (on the console) to the Status position simulates execution of the IORS instruction (with the processor in the "program stop" condition). The contents of the IORS word (i.e., the states of the device flags) are displayed in the REGISTER indicators (on the console) at this time.



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Figure 1-25 I/O Read Status Bit Assignments

I/O Overflow

I/O overflow is issued during the first cycle of the block transfer operation if the contents (2's complement) of the word counter assigned to the currently active channel device becomes 0 when incremented. This indicates that the program-specified number of words will have been transferred at completion of the channel transfer in progress. It is normally used to turn off the device, thereby preventing further channel action by that device until a service subroutine reinitializes the channel's word counter and Current Address registers, and the program turns on the device request flag. The overflow signal may also be used to initiate a program interrupt through the program interrupt or automatic priority interrupt facility for access to the initializing subroutine. Additionally, I/O overflow occurs when an I/O increment memory operation causes the location to overflow.

Data Overflow

Data overflow is issued during the third cycle of a four-cycle add-to-memory data transfer when the addition operation generates an arithmetic overflow.

Input Control Levels

Six input control level signals arrive at the I/O processor:

Program Interrupt Request – A device delivers this signal to request interruption of the program in progress. The program traps to location 00000 when no I/O transfer action of higher priority is in progress. The instruction resident in location 00001 is fetched and executed. If more than one device is connected to the program interrupt, this instruction transfers control to a subroutine, which determines through a search process (skip chain) the device making the program interrupt request. The appropriate service routine is then accessed.

Skip Request – The return of this signal to the processor indicates that an IOT instruction test for a skip condition in a selected device has been satisfied (e.g., a test of ready status). The program counter is subsequently incremented by one to effect a skip of the next instruction of the program in progress.

Read Request – This signal is used by the device to specify to the I/O processor that an input to the CPU data transfer is required.

Write Request – This signal requests that the processor execute a data-channel-write transfer of a data word into the selected device's Information register.

MB Increment – This level requests that the processor increment (by one) the contents of the memory location address specified by the 15-bit address on the I/O bus address lines. Used in increment memory operation.

+1 to CA Inhibit – This is a special signal line required by devices that automatically search for records, etc.; typical are DECtape and magnetic tape. The presence of this signal level inhibits normal incrementing of the device assigned Current Address register during a data channel transfer.

Device Selection Levels – Identification of the current instruction as an IOT causes the bit pattern placed in the CPU MI 06 through 13 at the fetch of the instruction to be bus-driven and sent via eight bus lines to device selection modules contained in the control logic for each device. These eight levels form a 6-bit device selection code and 2-bit sub-device or mode selection code.

Address Lines

Fifteen lines constitute an input bus for the devices which must deliver address data to the processor. There are three uses for the address bus:

1. When a device interfaced to the multi-level automatic priority interrupt system receives an I/O processor grant of its interrupt request, it delivers a hardware-defined address to the CPU, relating to its API channel assignment. This channel address indicates the location of the pointer to the device's service routine.
2. When a block transfer channel device receives a processor grant of its transfer request, it delivers to memory a hardware-defined address indicating the assigned channel's word count location.
3. A single-cycle data channel device delivers a 15-bit address plus two dual purpose lines for 17-bit 131072 accessibility. The dual purpose lines are SKP REQ and WRT REQ as address bits 01 and 02, respectively.

Multiplexed Control Lines

Sixteen control lines serve as processor-to-device control information paths, four for the block transfer channel facility and twelve for the priority levels on which the automatic priority interrupt system processes requests for service. Control lines are used in the following ways:

Request – A device transmits a service request to the processor via the appropriate request line. There are four automatic priority interrupt request lines (one for each level) and two data channel request lines (single cycle requests and multicycle requests).

Grant – The processor indicates a grant of the service request. There are four API grant lines (one for each hardware level) and one data channel grant line to answer both single and multicycle requests.

Enable – The enable signals control the priority order for answering service requests of devices interfaced to the block transfer data channel or to one of the API's device channels. Priority for a channel (data or API) is allocated in descending order from the device nearest the processor I/O bus interface. An enable signal permits servicing the requesting device with the highest priority and inhibits all lower priority devices from making requests during the interval of service. The enable signals are the only I/O signals that are actually broken and regenerated by each device on the associated channel.

I/O Run

The I/O Run signal is available at the interface for use as the interface designer requires. This bus-driven level switches to the +2.5 V level and remains there while the I/O Run flip-flop in the CPU is set. A ground level indicates that the RUN flip-flop has been cleared, and all operations in the CPU have been stopped.

Console Device Interface

The I/O processor includes a console terminal and the interface as standard I/O equipment. See Table 1-1 for devices that operate with this interface. The console terminal transmits and receives an 8-level ASCII code over a 4-wire cable connecting the terminal to its interface in the I/O processor.

Table 1-1
Interface Devices

Terminal Type	DEC Type No.	Baud Rate (max.)
Teletype®	LT33	110
Teletype	LT35	110
DECwriter	LA30	300
DECwriter II	LA36	300
Alphanumeric terminal	VT05	2400
DECscope	VT52	9600

®Teletype is a registered trademark of Teletype Corporation, Skokie, Illinois.

Hardware Read-In

A hardware-controlled read-in facility exists as standard in all systems. It is used with the PC05 High-Speed Reader and its associated PC15 controller. When a suitable tape is placed in the reader and the READ-IN key is pressed, the I/O processor instructs the reader to read data from the tape. The I/O processor assembles the data into 18-bit words and stores them in memory. When the tape is finished, control is transferred to the beginning of the program to initiate execution.

Priority

In view of the autonomous substructures of the XVM, three types of priority must be considered: memory access priority, priority on the common I/O bus, and priority on the use of the CPU.

Memory Access – The I/O processor always has priority over the CPU in accessing memory. However, once a CPU memory request has been granted, it will be allowed to complete its cycle before control can be returned to the I/O processor.

Common I/O Bus – Priority on the I/O bus is of concern only when more than one device is transferring information on the I/O bus and the I/O bus requests are received by the I/O processor. The following order of priority occurs:

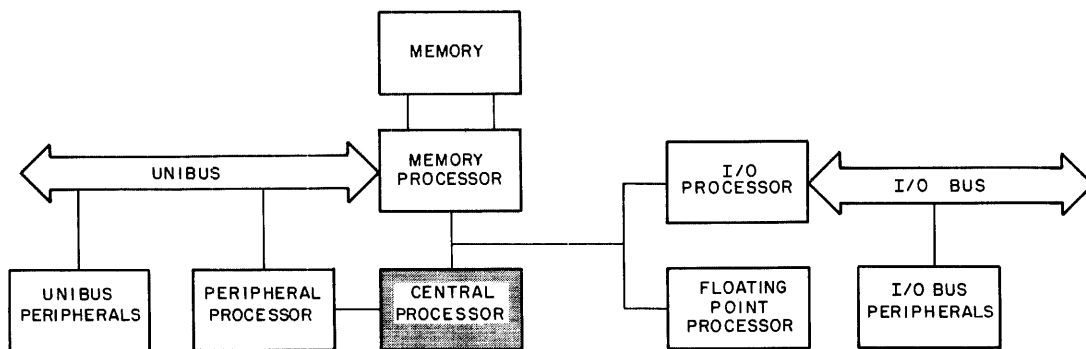
1. **Block Data Transfer Channel** – This is the highest level of priority on the I/O bus. However, as it is normally used to transfer only one word at a time, it can operate at very high speeds without disturbing the other levels of priority. The priority of devices on the Data Channel are determined by their physical position on the I/O bus.
2. **Real-Time Clock** – The real-time clock has priority after the block data transfer channel. The real-time clock uses the I/O processor to fetch the contents of a reserved core memory cell (000007₈), increment the count, and then restore the new count.

3. **Automatic Priority Interrupt** – The automatic priority interrupt (API) system adds eight additional levels of priority to the XVM. The upper four levels are assigned to devices and are initiated by flags (interrupt requests) from these attached devices. The lower four levels are assigned to the programming system and are initiated by software requests. The priority network ensures that high data rate or critical devices will always interrupt slower device service routines while holding off still lower priority interrupt requests until they can be serviced. The API identifies the source of the interrupt directly, eliminating the need for a service routine to flag-search.
4. **Program Interrupt** – The program interrupt (PI) facility offers an efficient method of I/O servicing, if the API system is not used. The computer continues with execution of a program until a previously-selected peripheral device signals that it is ready. At that time, the program in process interrupts and transfers control to a service subroutine. When completed, the subroutine restores the computer to the status existing prior to the interrupt, allowing the interrupted program segment to continue. Where multiple peripherals are connected to the PI, a search routine with device status testing (skipping) instructions must be added to determine which device initiated the interrupt request. The priority is established by the program skip routine.
5. **IOT's** – Program controlled transfers at the main program level.

CPU – Priority on the use of the CPU is established by the API level, the program interrupt, and the main program, in that order.

Latency

I/O transfer latency is a measure of the time between a device's request for service and the actual performance of that service. Regardless of a device's priority, once its request for service has been granted, the I/O processor holds all other devices off until the current service request is complete. For example, a single cycle data channel device requesting service just after the initiation of a multicyle output transfer would have to wait for four I/O processor cycles before using the I/O bus. Finally, synchronization can take additional time resulting in a worst case latency of less than 9.9 μ s for the requesting single-cycle device.



CP-1888

1.4 MEMORY

INTRODUCTION

The magnetic core memory is the primary storage facility of the XVM. It provides rapid, random access data instruction storage for both the CPU and the I/O processor.

Memory Data Transfer

The XVM memory communicates with the CPU and the I/O processor through the memory bus. Data and instruction words of each are read from and written into individual memory cells through a buffered register referred to as the Memory Data Buffer.

Words in a memory bank are selected according to the address in the Memory Address Buffer.

The 13-bit capacity of the Memory Address Buffer allows 2^{13} or 8192 words to be referenced in each bank. The Memory Address Buffer receives the memory cell address from the CPU or I/O processors. The address provides the coordinates for locating a word in a memory bank.

The Memory Address Buffer receives the memory cell address from the CPU or I/O processors. The address provides the coordinates for locating a word in a memory bank.

The XVM systems are provided with two types of memory, designated ME15 and MF15. These are compact and economical data storage devices, capable of holding up to 131,072 18-bit words. The ME15 is built in 8K segments, and the MF15-U in 16K segments: for a fixed memory capacity, (e.g., 64K) the MF15-U is more economical than the ME15, but does not provide the same interleaving capacity. It is possible to mix ME15 and MF15-U memories, even on the same output port, but careful consideration must be given to the configuration to ensure that the facilities of the memories are not inhibited.

MF15-W memory is also available in later models of XVM systems. This high density memory is manufactured in 32K units and packs twice the storage capacity of MF15-U memory into the same mounting space. This allows 64K to be mounted in the XM15 MPU assembly and 128K to be mounted in the basic XVM cabinet. Except for this increased density and slightly slower operation, the MF15-W is very similar to the MF15-U memory.

The XM15 unit has sufficient space for 32K of MF15-U, or 24K of ME15 (one has four modules; the other, three). The rear door of the XVM processor cabinet can accommodate 48K of ME15, or 64K of MF15-U. If greater memory storage capacity is required, then a separate expansion box must be added to the system in an extra cabinet which is normally mounted immediately to the left of the XVM cabinet.

NOTE

The ME15, MF15-U and MF15-W Core Memories are current types of memory that will operate on the output ports of the XM15.

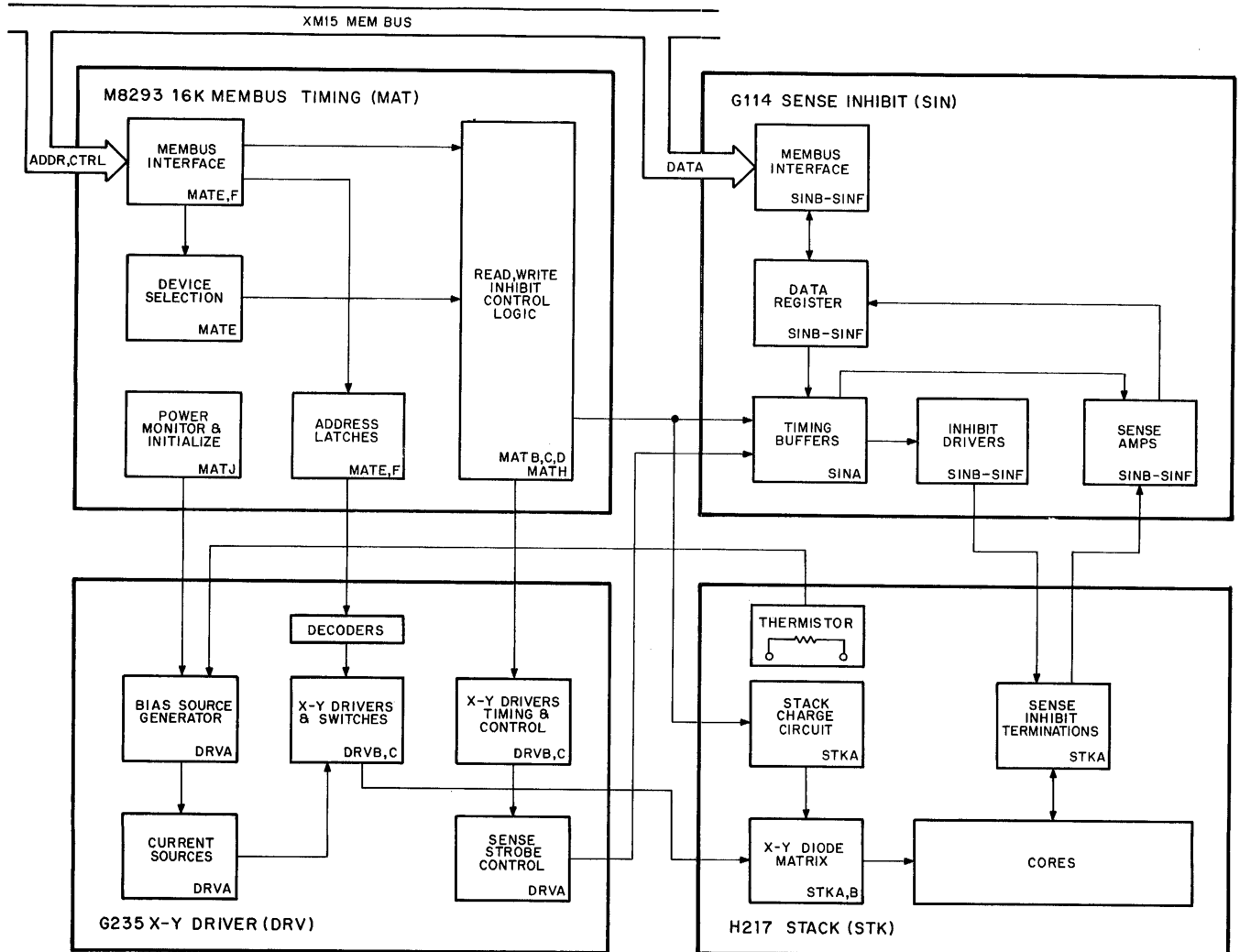
MF15-U General Description

This section briefly describes the characteristics of the MF15 Core Memory. The following modules make up a 16K memory unit, providing storage for 16384 18-bit words:

M8293	16K Timing Module
G114	Sense/Inhibit Module
G235	X-Y Driven Module
H217C	Stack Module
70-09295	Backplane Assembly

Table 1-2
MF15-U Core Memory, Specification Summary

Type	Magnetic core, read/write, coincident current, random access		
Organization	Planar, 3D, 3-wire		
Capacity	16,384 (16K) words		
Maximum Access Time and Cycle Time	Bus Mode	Cycle Time	Access Time
	DATI	1000 ns	425 ns
	DATIP	425 ns	425 ns
	DATO–DATOB (PAUSE L)	1000 ns	125 ns
	DATO–DATOB (PAUSE H)	680 ns	100 ns
X-Y Current Margins	$\pm 6\%$ @ 0°C , $\pm 7\%$ @ 25°C , $\pm 6\%$ @ 50°C		
Voltage Requirements	+5 V $\pm 5\%$ with less than 0.2 V ripple +20 V $\pm 5\%$ with less than $\pm 5\%$ ripple -5 V $\pm 5\%$ with less than $\pm 5\%$ ripple		
Average Current Requirements	Stand by:	+5 V: 5.38 A–5 V: 0.41 A +20 V: 0.5 A	
	Memory Active:	+5 V: 6.1 A–5 V: 0.51 A +20 V: 3.4 A	
Power Dissipation (Worst Case):	M8293 Control Module $\sim 7\text{ W}$ G235 Drive Module $\sim 33\text{ W}$ H217D Stack Module $\sim 40\text{ W}$ G114 Sense Inhibit Module $\sim 40\text{ W}$ Total at Maximum Repetition Rate: 120 W		
Environment			
Ambient Temperature	0°C to 50°C (32°F to 122°F)		
Relative Humidity	0–90% (non-condensing)		



11-3440

Figure 1-26 MF15-U Simplified Block Diagram

The Backplane Assembly provides sufficient space to mount two MF15 Units, having a total capacity of 64K 18-bit words, as shown in Figure 1-26. MF15-U specifications are summarized in Table 1-2.

Functional Description

The MF15-U Memory is a read/write, random access coincident current, magnetic core type with a maximum cycle time of 980 ns and a maximum access time of 425 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 18 bits and the memory consists of 16,384 words (normally referred to as 16K).

The memory can be interleaved in 32K increments for faster operation. Interleaving causes consecutive bus addresses to be located within alternate 16K memory blocks. The major functional units of the memory (Figure 1-26) are described briefly in the following paragraphs.

ME15 General Description

The ME15 Core Memory provides the XVM with a compact, economical storage device capable of storing up to 131,072 18-bit words. The ME15 is mounted on the rear door of the central processor cabinet and in the XM15 drawer. The entire memory is enclosed in a cooling box with fans at both top and bottom. Each of the four logic panels is six module plots high and nine module slots wide. The ME15 modular complement consists of G109, G231, and H215 modules. Every 8K of installed memory requires one each of the G109, G231, and H215 modules. Figure 1-27 shows the assigned module slots for one panel.

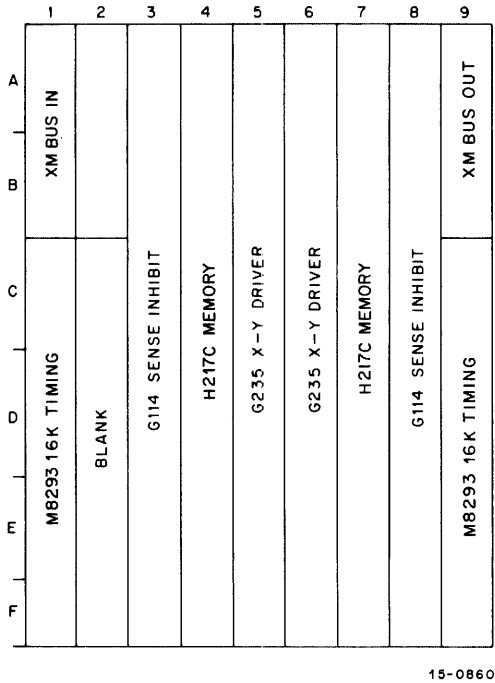


Figure 1-27 Assigned Module Slots

Memory Specifications

The general memory specifications are listed in Table 1-3.

Table 1-3
ME15 Memory Specifications

Type	Magnetic core, read/write, coincident current, random access								
Organization	Planar, 3D, 3-wire								
Maximum Capacity	131,072, 18-bit								
	<table> <tr> <th>Bus Mode</th><th>Cycle Time*</th></tr> <tr> <td>Read</td><td>980 ns</td></tr> <tr> <td>Write</td><td>980 ns</td></tr> <tr> <td>Read/Pause</td><td>1.56 μs</td></tr> </table>	Bus Mode	Cycle Time*	Read	980 ns	Write	980 ns	Read/Pause	1.56 μ s
Bus Mode	Cycle Time*								
Read	980 ns								
Write	980 ns								
Read/Pause	1.56 μ s								
X-Y Current Margins	$\pm 6\%$ @ 0° C, $\pm 7\%$ @ 25° C, $\pm 6\%$ @ 50° C								
Strobe Pulse Margins	± 30 ns @ 0° C, ± 40 ns @ 25° C, ± 30 ns @ 50° C								
Voltage Requirements	+5 V $\pm$ 5% with less than 0.05 V ripple -15 V $\pm$ 5% with less than 0.05 V ripple								
Average Current Requirements	Stand by: +5 V: 2.2 A -15 V: 0.5 A Memory Active: +5 V: 5.4 A -15 V: 6.0 A								
Power Dissipation (Worst Case)	G109 Control Module $\sim$ 60 W G231 Drive Module $\sim$ 40 W H214 Stack Module $\sim$ 20 W Total at maximum repetition rate: 140 W								
Ambient Temperature	0° C to 50° C (32° F to 122° F)								
Relative Humidity	0–90% (noncondensing)								
*Nominal									

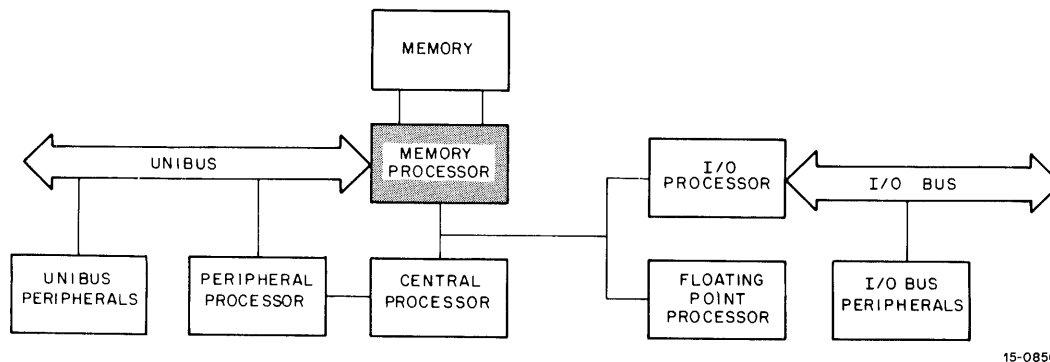
For a detailed description of the ME15 and MF15-U Core Memories, refer to the manuals listed below:

ME15 Core Memory Maintenance Manual, EK-ME15-MM-001
MF15-U Core Memory Maintenance Manual, EK-MF15-MM-001

CHAPTER 2

SYSTEM PROCESSORS

Section 1. XM15 MEMORY PROCESSOR

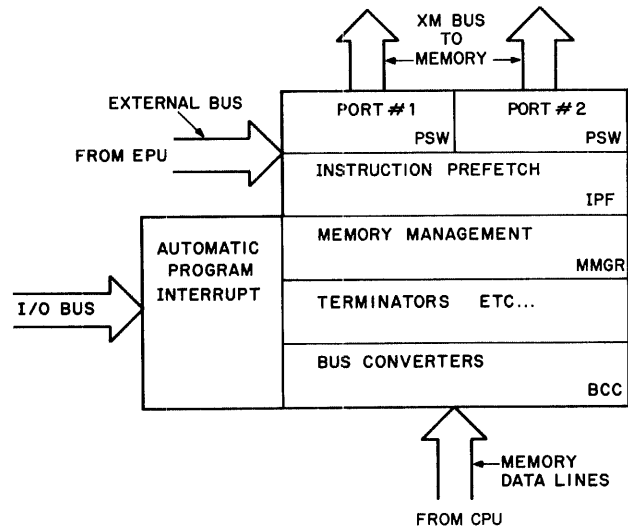


The XM15 Memory Processor is located logically between the XVM Central Processor and the Memory and performs the following specialized functions:

- Arbitrates between the three requesting elements for access to memory.
- Instruction pre-fetch to accelerate XVM CPU operation (IPF).
- Contains Automatic Priority Interrupt (API) logic.
- Contains Memory Management (MMGR) logic which enables different addressing modes.

The XM15 makes it possible for the CPU to run programs above 32K, and also provides the means whereby more than one user's programs are resident at the same time. This processor has a high resolution accounting clock and associated logic. The XM15 also has a bus converter which enables separate processors with different memory busses to communicate with the same memory on a common XM memory bus.

The XM15 basic block diagram is shown in Figure 2-1.



15-0820

Figure 2-1 XM15 Basic Block Diagram

The Port Module of the XM15 functions as a buffered multiplexer. It has three separate input ports, termed CP (Central Processor) port, EP (External processor) port, and the UF port. The output of the XM15 is also dual-ported, and these ports may be interleaved depending upon memory size and configuration. The Port Module will also function as a short-term buffer so that its inputs and outputs are not held busy for long periods. There are two methods by which the Port accomplishes this:

1. When executing a write, once the address and data have been supplied, the requesting processor usually has to wait for the memory to signify that the write function has terminated. With the Port module, the requesting processor may begin another function as soon as address (Interface module) and data (Port module) have been latched.
2. With an external processor request for a read, the Port module will latch the data when it becomes available, and hold it until the processor is ready to accept it. However, the output port is released immediately for possible use by the other processor. The interface acts in a similar manner for the CPU.

The IPF (Instruction Pre-Fetch) is a special unit within the XM15 that speeds up the overall operation of the system by attempting to supply, immediately, the contents of the location in memory containing the instruction required by the CPU. It is capable of obtaining data from memory and storing it in an internal file until requested by the CPU. Obviously, the CPU will be faster if demands for instructions from memory can be filled immediately, and this is what the IPF tries to accomplish.

If processors always executed "straight-line" code (i.e., if they never jumped out of sequence), then there would be a strong case for holding a large number of words in a file and pre-processing. However, efficient programming demands that Jumps and Jumps to Subroutines be made to prevent repetitive code. To determine the optimum size of the IPF file, exhaustive tests were performed on various systems, under different monitors, and the results showed that four words would be sufficient. Thus, on an XVM system, when the CPU breaks the sequence, the IPF waits until the new sequence is established, then the IPF loads up its file with the next sequential words. The IPF will then stay ahead of the CPU, supplying instructions upon each request, until the CPU breaks the sequence again.

2.1 AUTOMATIC PRIORITY INTERRUPT

The automatic priority interrupt (API) system ensures efficient handling of service requests at high rates.

The API system contains eight levels of priority. The lower four of these are allocated to the monitor systems, the upper four to the I/O processor. Up to 32_{10} individual interrupts are available at the I/O processor.

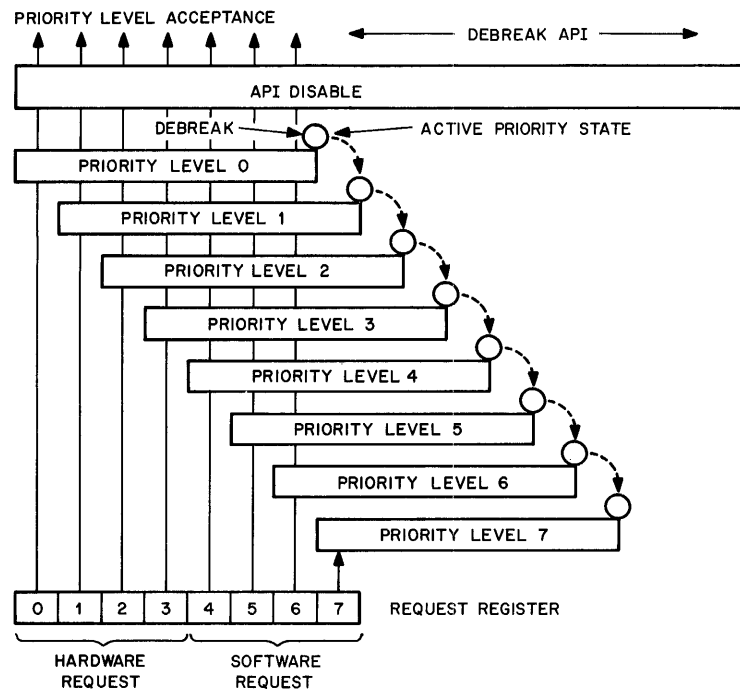
A device initiates an interrupt request on its preassigned level by raising a request flag, and identifies itself by posting a unique core address. There is one unique core address for each of the 32_{10} interrupts (44_8 through 77_8 are reserved in the standard software). This address serves as the entry point (trap address) to the device's service routine.

Each monitor API level services one interrupt and uses a single trap address between locations 40_8 and 43_8 . The monitor requests are initiated by a program issuing an ISA instruction.

The I/O interrupts permit the asynchronous operation of many devices, each at its proper priority level. The software priority levels are used to establish a priority queue for processing real-time data without inhibiting the hardware interrupts to service devices.

2.2 API HARDWARE

Figure 2-2 relates the activity of the Automatic Priority Interrupt (API) system from the initiation and acceptance of the request, the servicing of the accepted request, and the debreak from the serviced priority level.



15-0054

Figure 2-2 API System, Simplified Block Diagram

The API Request register contains eight levels; four levels are activated by the devices (hardware) on the I/O bus, and four are activated under software supervision. The hardware requests are assigned the highest priority, and are designated request levels 0, 1, 2, and 3. The software requests are designated request levels 4, 5, 6, and 7, and are initialized by the ISA instruction with the associated AC bits set.

The priority level bars in Figure 2-2 depict the priority level that is selected by the ISA instruction, or that is raised by the API control when it has granted a break request on that specific level. The priority level (PL) bars indicate that any request equal to, or less than the priority level which is active, will not be accepted. At the end of the subroutine currently being performed by an active request, a debreak and restore instruction is issued. This will lower the priority to the next requesting priority level. The ball, representing the priority debreaking, will fall as long as there is no bar present (i.e., no priority level set). If a lower priority level is set, the debreaking will cease at that level.

The API Request register (RQ) buffers the inputs from the hardware interrupt on levels 0 through 3 and the inputs from the monitors on levels 4 through 7. If two or more hardware interrupts on one level make simultaneous interrupt requests, the device controller closest to the processor is given priority and interrupts at its unique location. An interrupt request sets a bit in the RQ according to its preassigned priority level. The API system signals the CPU to stop execution at the completion of its current instruction. It then gates the I/O processor's address lines, which contain the address of the interrupt's unique core location, into the CPU Memory Output register. The CPU then requests a memory cycle and executes the instruction it fetched from that location. During this operation, the program counter remains unchanged. The instruction is normally a jump to subroutine (JMS) that stores the contents of the L, BM, UM and program counter, which, in turn, points to the location where the current program was interrupted in the first location of the subroutine and begins execution at the subroutine's second location.

The API system also sets a PL corresponding to the level of the interrupt. This prevents interrupts on the same level or lower levels from interrupting the current interrupt. Higher priority devices can still interrupt lower priority devices. The JMS instruction allows nesting of all levels. At the completion of the interrupt subroutine, a debreak and restore (DBR) instruction must be issued to reset the bit in the PL and in the RQ.

The API hardware ensures that simultaneous requests by multiple devices are handled in the proper priority sequence. If interrupt requests occur at different priority levels, the highest priority requests will be serviced first. Higher priority devices may interrupt lower priority devices. The entire API system may be enabled or disabled with a single instruction; however, most devices provide facilities to enable and disable their flags from the interrupt separately. If the API system is disabled, the device will automatically signal the program interrupt to obtain a response at that priority level.

The program interrupt (PI) sets level 3 if priority levels PL 0-3 are 0, PL 3 is enabled, and no other API request has been synchronized.

Under program control, the level of a priority request may be raised to provide dynamic priority reallocation. It does this by issuing an ISA.

ISA	705504	Initiate selected activity. The API activity specified by a set bit in the AC is initiated.

The ISA instruction places a bit into a priority level specified. This effectively masks all lower priority levels. A debreak instruction (DBK) is used to reset this bit when the higher priority level is no longer required. For example, a priority-2 interrupt routine is designed to enter data in memory locations A through A + 10 during an interim period when the priority-2 device is inactive and, based on a calculation made by a software priority-6 routine, it becomes necessary to move the data to memory

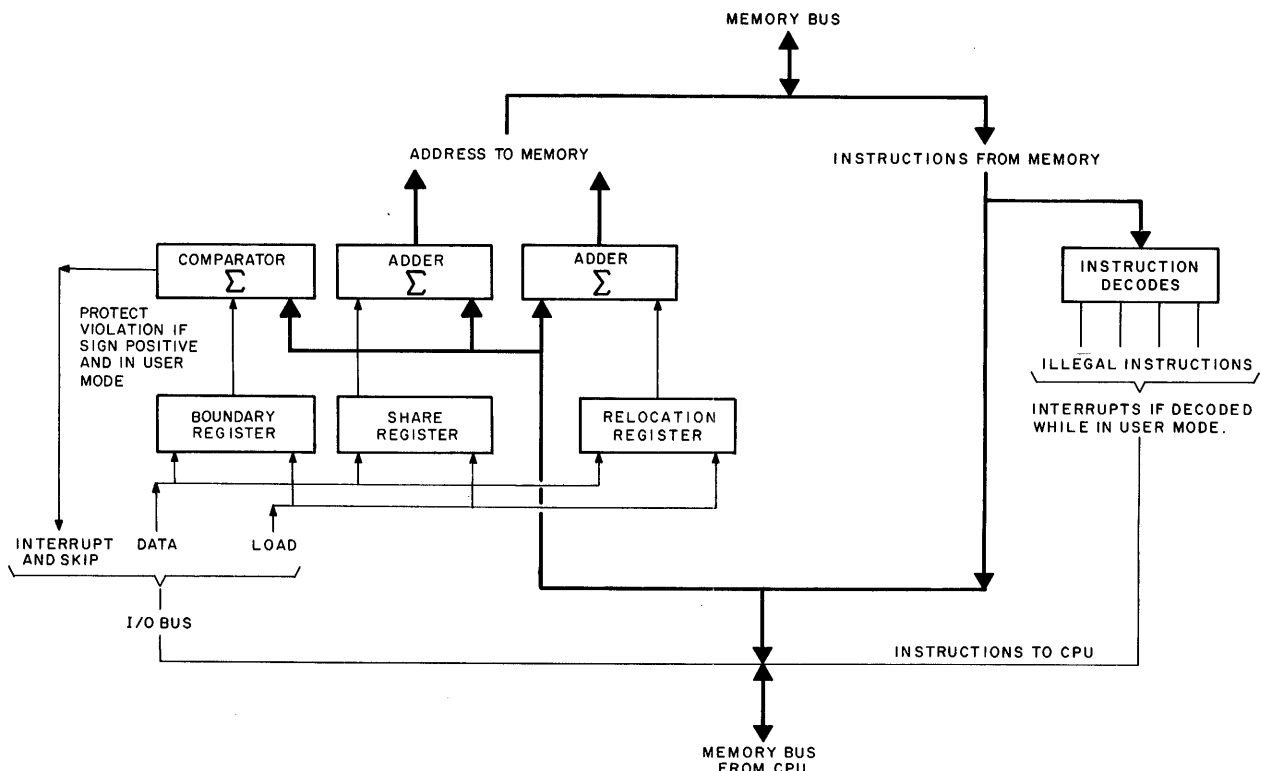
locations B through B + 20. The changes in the routine at level 6 must be completed without interrupt once they are started. This is possible by causing the level 6 program to raise itself to level 2 (devices on the same or lower priority may not interrupt), complete the change, and debreak back to level 6. Note that the ISA is also used to trigger the API levels dedicated to software priority queues. This unique advantage of the API system lies in the proper use of its software levels. In the real-time environment, it is necessary to maintain data input/output flow, but it is not possible to perform long complex calculations at priority levels which shut out these data transfers. With the API, a high-priority data input routine that recognizes the need for complex calculations can call for a software-level interrupt. Since the calculation is performed at a lower priority than the device handling, the latter can go on undisturbed. The monitor task of establishing a multi-priority request queue at the software level is greatly simplified by utilization of the API hardware.

2.3 MEMORY MANAGEMENT (MMGR)

The Memory Management logic (Figure 2-3) within the XM15 provides the system with a wide range of real-time control by performing the following three tasks:

1. dynamic address modification
2. extended internal address control
3. selective instruction checking

The three functions listed above are executed when the system is in a real-time mode of operation called USER MODE. This mode can be entered by two main methods: 1. the execution of the MPEU IOT; and 2. when a DBR IOT is executed, and bit 02 of the Restore word contains a 1.



15-0178

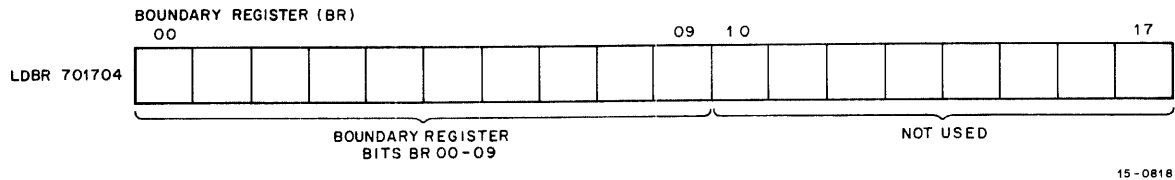
Figure 2-3 Memory Management Block Diagram

The status of the User mode flip-flop is saved whenever the program is interrupted. The User mode state, bit 02 is stored, usually with the contents of the Program Counter (PC) in the first location of the service routine. The relevant instructions are CAL and JMS, and both Program Interrupt (PI) and Automatic Priority Interrupt (API) cause the same effect.

There are three registers associated with this logic:

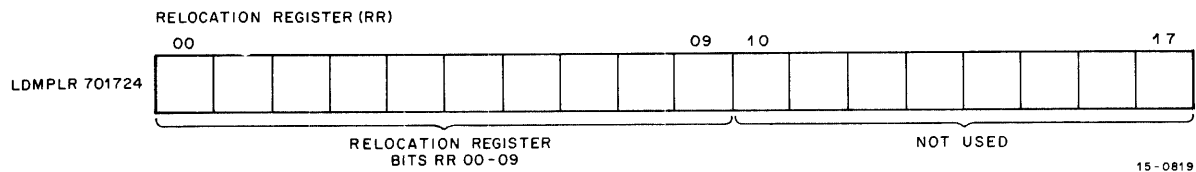
1. **Boundary Register**

The contents of this register corresponds to the highest ten bits of the memory address.



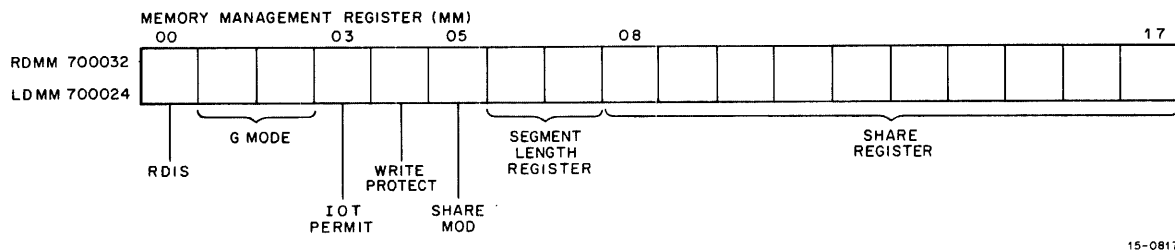
2. **Relocation Register**

The contents of this register are used with the 18 bits of memory address.



3. **Memory Management Register**

The contents of this register, bits 08-17, are used similarly to the bits in the relocation registers, i.e., they are used with the highest 10 bits of memory address. The remainder of this register is divided into individual signals.



Segment Length Register (SLR) – Bits MM06 and 07 are used to select one of four possible sizes of External Shared Address Space (ESAS).

Share Mode (SH) – Bit MM05 is used to determine whether or not the system can go into Share mode. This bit will only have effect when the system is in User mode.

Write Protect (WP) – Bit MM04 signifies whether it is possible to write to the ESAS. The system must be in Share mode before this bit has any effect. That means that TRAPs will occur only if an attempt is made in User mode, with Share mode on.

IOT Instruction Permit (IOTP) – Bit MM03 defines whether or not TRAPs will occur, should an IOT instruction be executed while in User mode.

G-Mode (GM) – Bits MM01 and 02 are the G-Mode selectors. When in User mode, the type of G-Mode (0-3) determines the starting address of the Shared Address Space (SAS). The width of the address passed to the memory is also affected by the G-Mode bits when User mode is set. GM0, which is not G-Mode, allows only 15 bit indirect addressing. GM1 will allow 16 bits of indirect addressing. GM2 allows all 18 bits, and GM3 only 17 bits, under similar circumstances.

Relocate Disable (RDIS) – Bit MM00, when set, inhibits relocation of the address in User mode, and prevents TRAPs from occurring when boundary violations occur, or when OAS, HLT, or an XLT of an XCT is performed.

IOT Instructions

Mnemonic	Code	Description
RDMM	700032	Read MM Reg to AC00-17.
LDMM	700024	Load MM Reg from AC00-17.
MPLD	701704	Load Boundary Reg from AC00-09.
MPLR	701724	Load Relocation Reg from AC00-09.
MPEU	701742	Enable User Mode.

2.4 DYNAMIC MAPPING

There are four possible modes of address modification, or “mapping”, as follows:

1. Direct Mapping (D-MAP)
2. Relocated Mapping (R-MAP)
3. Shared Mapping (S-MAP)
4. Protected Mapping (P-MAP)

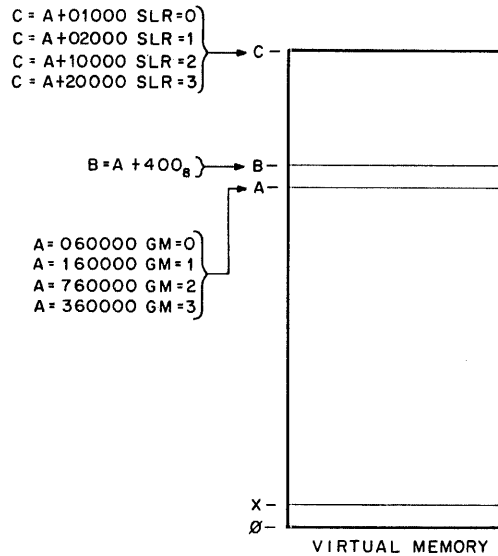
Mapping is the name given to the process of translating from “virtual” addresses, which are those the CPU uses, to “real” addresses, which are absolute core memory locations. For a detailed description of the various types of mapping, refer to Chapter 1, Paragraph 1.2, Addressing. A brief description of the hardware aspect follows.

D-MAP – The Memory Management can accomplish direct mapping in either of two states:

1. Not in User mode, in which case the “virtual” address from the CPU passes straight through and is the “real” address.
2. In User mode, but R-DIS (MM00=1) is set. This mode allows the use of wide (G-Mode) addressing and NEXM protection, but does not relocate the CPU address. In this case, the “virtual” address is the same as the “real” address except as affected by G-Mode.

R-MAP – The Memory Management must be in User mode for this type of mapping to come into effect. The SH bit must be reset (MM05=0). The “virtual” address sent from the CPU will have the current contents of the Relocation register added to it. The sum of these two (RR00-09 + PC00-17) will be the “real” address presented to the memory. If the virtual address should exceed the value in the Boundary register, a trap will occur and the program will be interrupted.

S-MAP – This type of mapping has three separate mapping functions, depending what area of the “virtual” address space is referenced (Figure 2-4).



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Figure 2-4 User's Virtual Address Space in S-MAP

If the "virtual" address should refer to a location between 0 and A, then the virtual address will be treated in the same way as it would be in R-MAP.

If the location addressed is greater than A but less than B, then the address is termed "share internal". This means that a reference has been made to the Internal Shared Address Space (ISAS), and the address is modified by concatenating the address (PC10-17) with the contents of the Relocation register (RR00-09). The result of this process will in fact refer to a "virtual" address somewhere within the range 0 to 377_8 . This relocated value of the address is then forwarded to memory.

If the "virtual" address is greater than B, but less than C, then a reference has been made to the External Shared Address Space (ESAS). Note that C is not a fixed address, because the length of the Shared Address Space ($SAS = ESAS + ISAS$) is defined by the contents of the Segment Length Register (SLR).

A reference to ESAS will cause the address bits (PC05-17) to be added to the contents of the Share Register (SR00-09). The result of this addition will be sent to the memory. This relocates the address to an area of core reserved for shared addressing. The use of the S-MAP mode of operation allows several independent tasks access to a designated area of core memory that is not physically contained within any of the user's partitions. A diagram that illustrates the points of S-MAP, is shown in Figure 2-5.

NOTE

The function of the G-Mode bits with regard to address truncation is still in effect, and the "virtual" addresses will be truncated depending upon which GM is set.

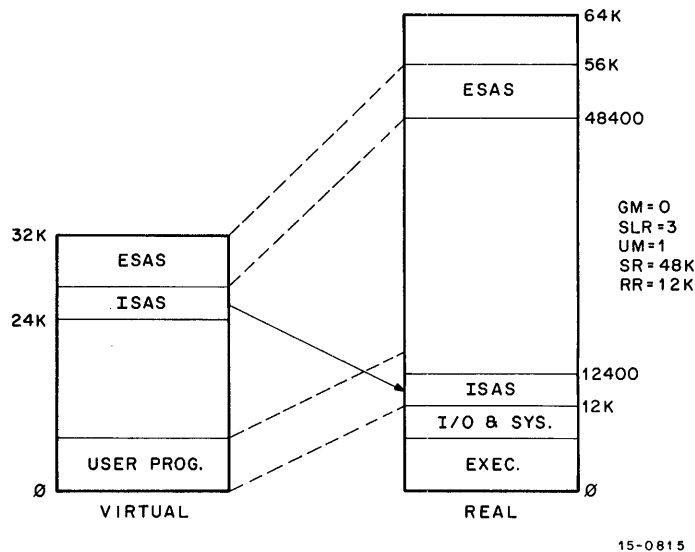


Figure 2-5 S-Mapping

P-MAP

NOTE

This is a special mode of operation that is not selectable by program on a standard XVM system. If a user should want this mode of operation, he or she must contact their local Digital Field Service office. Enabling this mode of operation makes R- or S-Mapping inaccessible.

This type of mapping does not use the Relocation register or the Share register. In this type of operation, the Boundary register is loaded to establish a lower boundary in memory. If an attempt should be made to reference an address below the boundary while in User mode, the Memory Management logic will trap.

2.5 G-MODES

There are four possible G-Modes, GM0-GM3. A brief description of each follows.

GM0 (MM1 & 2=0) – This mode is “Normal mode” and makes the system operate in a similar manner to the PDP-9 and PDP-15. This is necessary for compatibility with these earlier systems. When a JMS is executed, the state of the LINK, BANK MODE, and USER MODE flip-flops are stored in bits 00-02 respectively, of the entry-point address along with the 15 bits of the current virtual PC. When the XVM system is in Share mode (which implies User mode) the G-Mode field also defines the starting “virtual” address of the SAS as 060000.

GM1 (MM01=0, 02=1) – When this mode is in effect, 16 bits of each indirect address will be used, and the maximum user “virtual” address will be 65536. In addition, when a JMS is executed, the return address location will contain 18 bits of the PC. The previous state of the LINK, BANK MODE, USER MODE, are not saved. The starting address of the SAS is defined in this mode as Y60000. The letter Y is used because real addresses 160000, 360000, 560000, and 760000 all look the same because of address truncation.

GM2 (MM01=1, 02=0) – The effects of this mode are like those of GM1, but with two exceptions. First, all 18 bits of “virtual” address are passed and all 18 bits are used with an indirect reference, making a maximum of 262144 memory locations available. Second, the starting address of the SAS is 760000. The execution of a JMS instruction will have the same effect as in GM1.

GM3 (MM01 & 02=1) – This mode defines the starting address of the SAS as 360000. Bit 00 of the address is truncated by this mode, limiting the maximum virtual address to 131072. The effect of the execution of a JMS is the same as for the two previous G-Modes. This mode, and GM0, are supported by the appropriate Digital-supplied software systems.

2.6 TRAPS

TRAP is the term used to indicate that the XVM system user program has attempted to execute some instruction that is deemed “illegal”. Traps only occur in User mode, and are produced by any of the following conditions:

1. An attempt to execute a HLT instruction or,
2. An attempt to execute an IOT instruction or,
3. A microcoded instruction containing an OAS instruction or,
4. An instruction XCT of an XCT instruction or,
5. An attempt to reference a location that is “non-existent” memory (NEXM) or,
6. An attempt to read or write to a location which is:
 - a. Below the boundary, with the system in P-MAP or,
 - b. Above the boundary, with the system in R-MAP or,
 - c. Above the boundary, but outside the SAS, with the system in S-MAP or,
7. An attempt to write into the Extended Shared Address Space (ESAS), while in S-MAP, and with the Write Protect bit set (MM04=1).

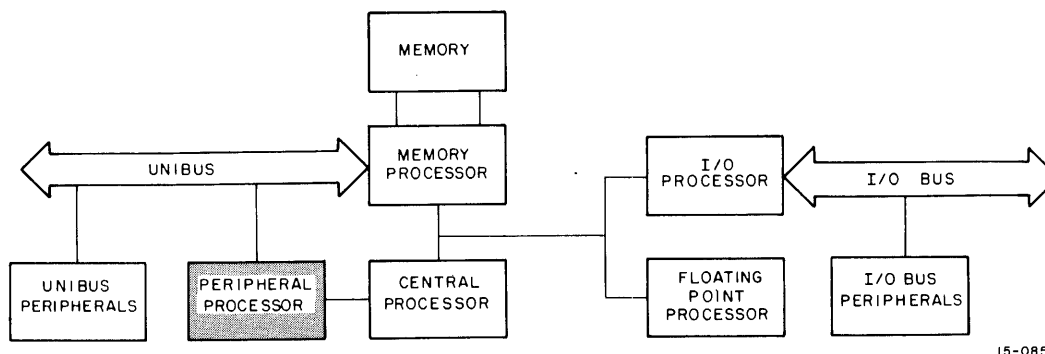
The effect of a trap is that the user’s program will be interrupted and program control will transfer to location 000001, after storing the current PC + 1 in location 000000. The trap is then handled as if it were a normal interrupt. This sequence can only happen if Program Interrupt Enable is on (PIE=1). If this is not the case, then the trap is treated like a CAL. The PC + 1 is stored in location 000020, and the instruction in 000021 is executed. There are a number of IOT instructions that can be used to determine which type of violation occurred.

IOT Instructions

Mnemonic	Code	Description
MPSK	701701	Skip if protect violation occurred.
MPSNE	701741	Skip if NEXM reference attempted.
MPCV	701702	Clear violation flag.
MPCNE	701744	Clear NEXM flag.

It is possible for IOT instructions to be executed in User mode without a trap occurring by setting bit MM03 in the Memory Management register. This is termed “User IOT mode.”

Section 2. PERIPHERAL PROCESSOR



The XVM Peripheral Processor consists of one of the computers from the PDP-11 family with some of its own memory (normally 8192 words) on the Unibus, and is used as the XVM system's second input/output processor.

The Unibus is connected to the External Processor Port of the XM15 Memory Processor. There is an address translation unit built in to enable the peripheral processor to access the XVM memory.

The peripheral processor enables the XVM to appear as a Unibus Memory Subsystem, thus allowing the use of standard Unibus peripherals as I/O devices.

A means by which the processors may interrupt each other is provided. The Peripheral Processor Unit (PPU) is allowed to provide interrupts to the XVM CPU at one of four levels, with up to 128 vector addresses.

The XVM CPU can interrupt the peripheral processor at one of two levels, with one of two vector addresses, usually to transfer a data control word to the PPU.

2.7 MEMORY ADDRESS TRANSLATION (Figure 2-6)

Remember that the PDP-11 family PPU is a byte-oriented machine. The XVM CPU and memory are 18-bit word-oriented systems. Therefore, some processing must be done to relocate the PPU byte addresses to MPU word addresses.

The first process is to subtract from the top five bits of the address, a value corresponding to the amount of local memory resident on the PPU. Once this has been done, the address is then shifted one place to the right to compensate for the fact that the PDP-11 family PPU uses byte addresses. This can be seen in Figure 2-6. There is a "28K limit" mark on the common memory in Figure 2-6; this shows the maximum PPU memory addressing capability without PPU memory management.

This limit of addressing capability refers only to the PPU. NPR devices have no such limit although the absolute core limit is still 760000, due to device registers starting at that Unibus address.

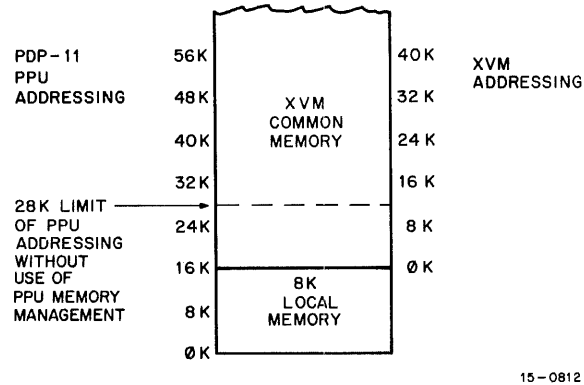


Figure 2-6 Memory Address Translation

Unibus device addresses, which reference locations 160000 or greater, are transformed to 760000 or greater and refer to PPU or I/O device registers. Although the PDP-11 may have 8K (8192) of memory, there are two bytes in each word and each one is separately addressable. Thus, it takes addresses 000000 to 016384 to address the first 8K words. On an 8K PPU therefore, address 016385 actually addresses the first location in common memory. The memory address shifting process is shown in Figure 2-7.

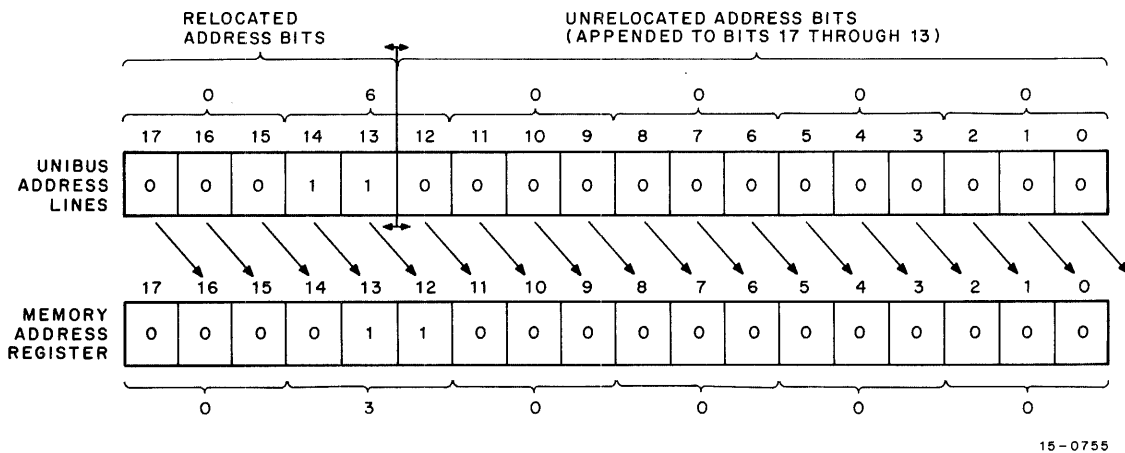


Figure 2-7 Memory Address Shifting Process

For further information on PPU address manipulation, refer to the *Unichannel System Maintenance Manual* (DEC-15-HUCMA-B-D), Chapter 4.

2.8 XM15 EXTERNAL PORT

The external port of the XM15 Memory Processor provides the unique facility of “floating” the EPU input address. This address float is used primarily in multiprocessor XVM systems to enable different processors access to core on other systems.

On standard systems supplied by DEC, the address float will be set to zero. When an address is received by the XVM external port, it is checked to ensure that it lies within the “EP Address Window”. This is an upper and lower address, the parameters of which are set by the factory.

DEC standard software will operate only with the factory-authorized settings of the “EP Address Window”.

The width of the EP Address Window should always be less than the address “float”, on systems where this facility is used. If it is not, the system will act as if it had “memory wrap-around”.

2.9 UNICHANNEL LINK

The link between the two processors is one DR15-C Device Interface, whose external connections (those at the opposite end, logically, to the I/O bus) are coupled to the similar connections of two DR11-C Interfaces. This system provides a method of transferring 17-bit data words from the I/O bus to the Unibus and the facility to generate one of four levels of interrupt, with up to 128 vector addresses. The manner in which the data word is transferred is depicted in Figure 2-8.

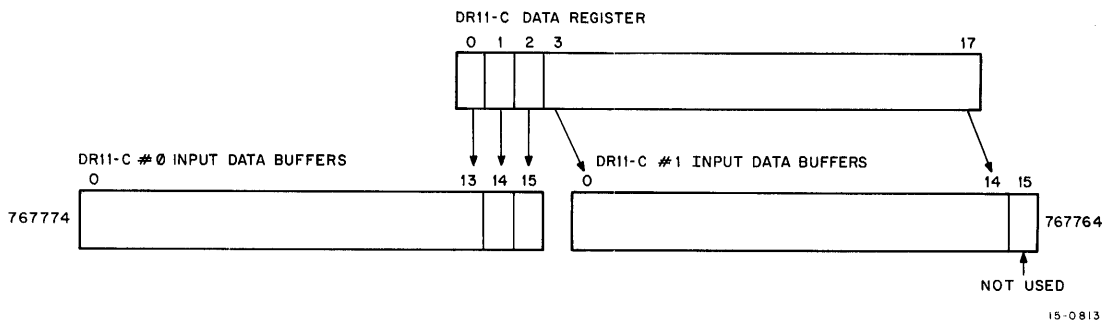
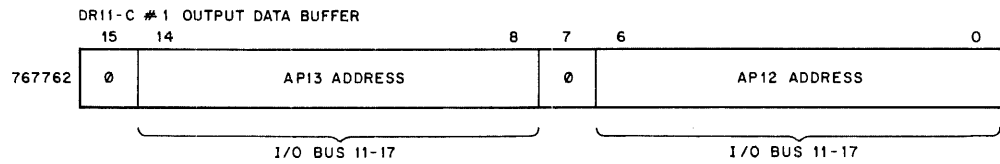
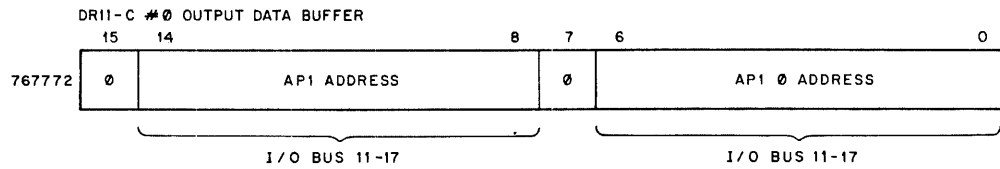


Figure 2-8 Data Input

Figure 2-9 shows how the output data buffers of both DR11-Cs are used to hold API-break addresses. These addresses are enabled on to the XVM I/OA Bus when the respective interrupt level is being serviced.

The remaining registers in the DR11-Cs and the DR15-C contain status information. This is shown in Figure 2-10.



15-0814

Figure 2-9 Data Output

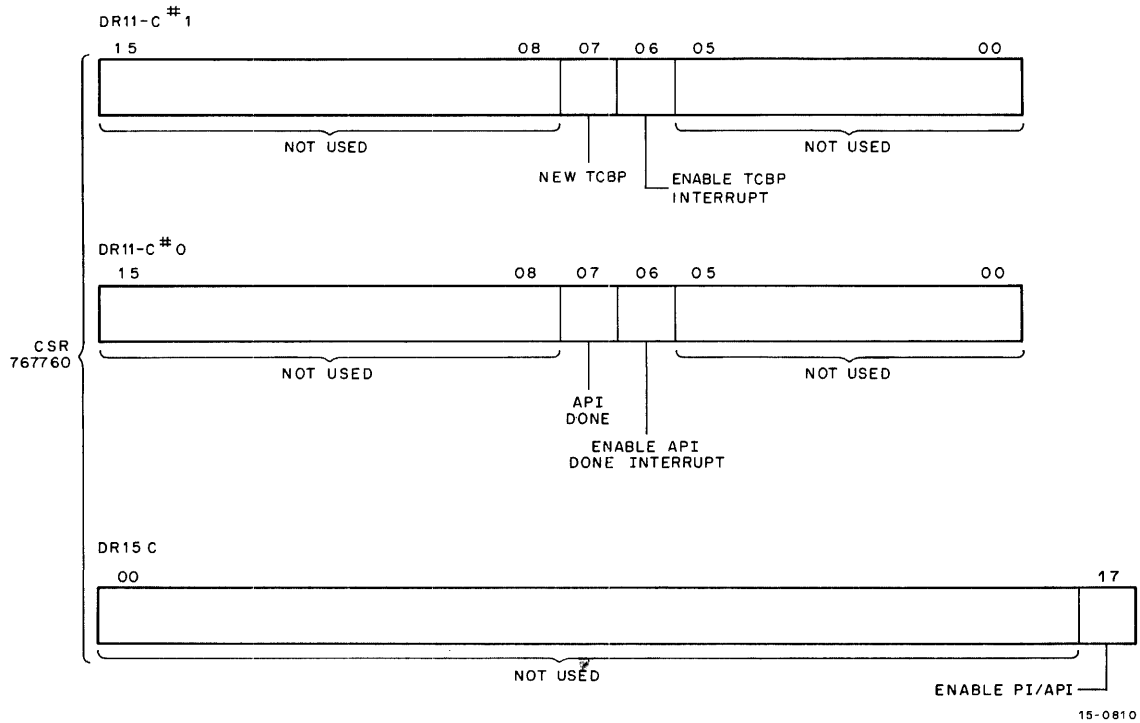


Figure 2-10 Status Information

2.10 IOT INSTRUCTIONS

Mnemonic	Code	Description
SIOA	706001	Skip if I/O data accepted (if TCBP DONE = 1)
CIOD	706002	Clear I/O done (set TCBP DONE = 0)
LIOR	706004	Load I/O Register
SAPI0	706101	Skip if API0 flag = 1
RDRS	706112	Read OR status register to AC
CAPI0	706104	Clear API0 flag
SAPI1	706121	Skip if API1 flag = 1
LDRS	706122	Load DR status register from AC
CAPI1	706124	Clear API1 flag
SAPI2	706141	Skip if API2 flag = 1
CAPI2	706144	Clear API2 flag
SAPI3	706161	Skip if API3 flag = 1
CAPI3	706164	Clear API3 flag

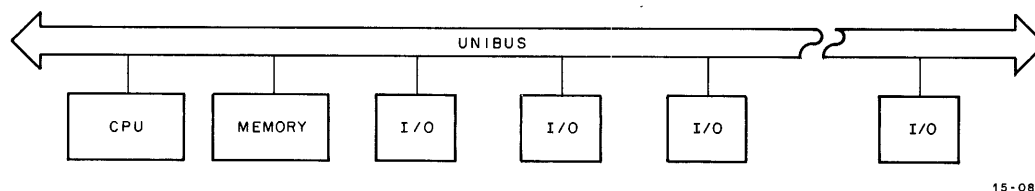
2.11 REGISTER ADDRESSES

DR11-C #0	767770	Control Status Register
BR5	767772	Output Data Buffer
VA=300	767774	Input Data Buffer
DR11-C	767760	Control Status Register
BR7	767762	Output Data Register
VA=310	767764	Input Data Register

2.12 THE UNIBUS AND THE PDP-11 PROCESSOR

2.12.1 The Unibus

All the PDP-11 computer system components and peripherals connect to and communicate with each other on a single high-speed bus, the Unibus. All elements of the PDP-11 system, including the central processor, communicate with each other in identical fashion via the Unibus; thus, the processor can easily access both peripherals and memory (Figure 2-11).



15-0811

Figure 2-11 PDP-11 System, Simplified Block Diagram

With bidirectional and asynchronous communications on the Unibus, devices can send, receive, and exchange data independently without processor intervention. Because it is asynchronous, the Unibus is compatible with devices operating over a wide range of speeds.

Device communications on the Unibus are interlocked. For each command issued by a "master" device, a response signal is received from a "slave" completing the data transfer.

I/O devices transferring directly to or from memory are given highest priority and may request bus mastership and steal bus and memory cycles during instruction operations. The processor resumes operation immediately after memory transfer. Multiple devices can operate simultaneously at maximum direct memory access (DMA) rates by “stealing” bus cycles.

2.12.2 PDP-11 Processor

Central Processor

The central processor, connected to the Unibus as a subsystem, controls the time allocation of the Unibus for peripherals and performs arithmetic and logic operations and instruction decoding. It contains multiple high-speed general purpose registers which can be used as accumulators, address pointers, Index registers, and other specialized functions. The processor can perform data transfers directly between I/O devices and memory without disturbing the processor registers; and it performs both single and double operand addressing and handles both 16-bit word and 8-bit byte data.

Instruction Set

The instruction complement uses the flexibility of the general purpose registers to provide over 400 powerful hard-wired instructions the most comprehensive and powerful instruction repertoire of any computer in the 16-bit class. Unlike conventional 16-bit computers, which usually have three classes of instructions (memory reference instructions, operate or AC control instructions, and I/O instructions), all operations in the PDP-11 are accomplished with one set of instructions. Because peripheral device registers can be addressed as easily as core memory by the central processor, instructions that are used to manipulate data in core memory may be used equally well for data in peripheral device registers. For example, data in an external device register can be tested or modified directly by the CPU, without bringing it into memory or disturbing the general registers. One can add data directly to a peripheral device register, or compare logically or arithmetically contents with a mask and branch. Thus, all PDP-11 instructions can be used to create a new dimension in the treatment of computer I/O and the need for a special class of I/O instructions is eliminated.

Priority Interrupts

A multilevel automatic priority interrupt system permits the processor to respond automatically to conditions outside the system. Any number of separate devices can be attached to each level.

Each peripheral device in the PDP-11 system has a hardware pointer to its own pair of memory words (one points to the device's service routine, and the other contains the new processor status information). This identification eliminates the need for polling devices to identify an interrupt, because the interrupt servicing hardware selects and begins executing the appropriate service routine after having automatically saved the status of the interrupted program segment.

The device's interrupt priority and service routine priority are independent. This allows adjustment of system behavior in response to real-time conditions by dynamically changing the priority level of the service routine.

The interrupt system allows the processor to continually compare its own programmable priority with the priority of any interrupting devices and to acknowledge the device with the highest level above the processor's priority level. Servicing an interrupt for a device can be interrupted for servicing a higher priority device. Service to the lower priority device is resumed automatically upon completion of the higher level servicing. Such a process, called nested interrupt servicing, can be carried out to any level without requiring the software to save and restore processor status at each level.

Re-entrant Code

Both the interrupt handling hardware and the subroutine call hardware facilitate writing re-entrant code for the PDP-11. This type of code allows a single copy of a given subroutine or program to be shared by more than one process or task. This reduces the amount of core needed for multitask applications such as the concurrent servicing of many peripheral devices.

Addressing

Much of the power of the PDP-11 is derived from its wide range of addressing capabilities. PDP-11 addressing modes include addressing forward or backward, address indexing, indirect addressing, 16-bit word addressing, 8-bit byte addressing, and stack addressing. Variable length instruction formatting allows a minimum number of bits to be used for each addressing mode. This results in efficient use of program storage space.

Stacks

In the PDP-11, a stack is a temporary data storage area that allows a program to make efficient use of frequently accessed data. The stack is used automatically by program interrupts, subroutine calls, and trap instructions. When the processor is interrupted, the central processor status word and the program counter are saved (pushed) onto the stack area, while the processor services the interrupting device. A new status word is then automatically acquired from an area in core memory that is reserved for interrupt instructions (vector area). A return from the interrupt instruction restores the original processor status and returns to the interrupted program without software intervention.

Direct Memory Access

All PDP-11s provide for direct access to memory. Any number of DMA devices may be attached to the Unibus. Maximum priority is given to DMA devices, thus allowing memory data storage or retrieval at memory cycle speeds. Latency is minimized by the organization and logic of the Unibus, which samples requests and priorities in parallel with data transfers.

Power Fail and Restart

The PDP-11 power fail and restart system not only protects memory when power fails, but also allows the user to save the existing program location and status (including all dynamic registers), thus preventing harm to devices, and eliminating the need for reloading programs. Automatic restart is accomplished when power returns to safe operating levels, enabling remote or unattended operations of PDP-11 systems. All standard peripherals in the PDP-11 family are included in the systemized power-fail protect/restart feature.

2.13 SYSTEM OPERATION

The Unichannel system when installed on an XVM system, can be used in a variety of ways. DIGITAL software systems supplied with the system aid in making the link-up between the two processors as flexible as possible. The Unichannel can be made to operate in one of four possible modes:

1. Pure I/O – The PDP-11 excels when used as an I/O controller. This mode of usage frees the XVM from the chores of tending to slow devices, plotters, and printers, for example.
2. Sophisticated I/O – In an effort to make the Unichannel perform more of the XVM system's chores, some valuable routines were included in the PPU Monitor. SPOOL helps the XVM by relieving it of the necessity of holding data buffers for slow devices in the CPU's memory. The disk, normally included in a Unichannel, functions as a large temporary store, while the PPU doles out words to devices when they are ready.
3. Pure computing – Programs can be written and assembled by the PPU to run on the PPU.

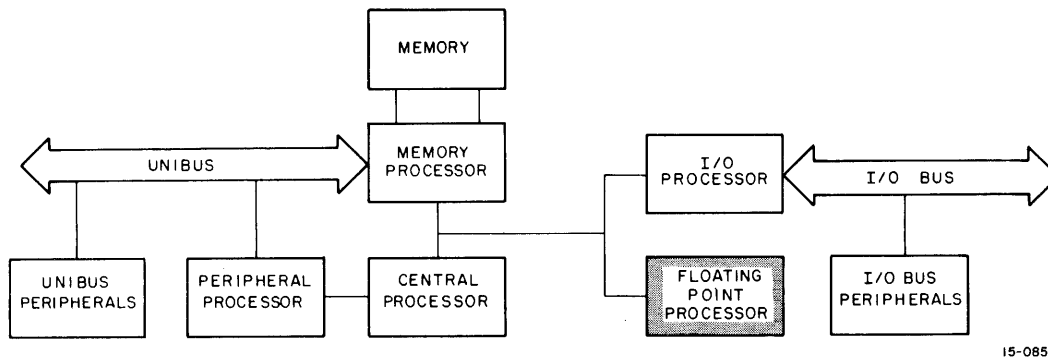
The three cases above have been catered for by the inclusion of programs in the standard software packages.

4. Independent – The PPU and the XVM can function as separate systems, provided care is taken to prevent interference between PPU and CPU peripherals.

PPU peripheral devices include the following:

CR11	Card Reader
DL11	Asynchronous Communications Interface
KG11	Communications Arithmetic for DL11
LP11	Line Printer
LV11	Electrostatic Printer/Plotter
RK11	Cartridge Disk
XY11	Plotter
XY311	3 Pen Plotter

Section 3. FP15 FLOATING POINT PROCESSOR



FP15 operations consist of memory transfers to obtain or store data, and arithmetic calculations in the FP15 unit itself. The cycle time of memory, the central processor, and the I/O processor, as well as data channel latency, are unaffected by the FP15 option. Data channel transfers to and from memory may occur simultaneously with FP15 arithmetic operations. Program and priority interrupts are inhibited and queued for priority-ordered response upon completion of the FP15 instruction. (The longest FP15 instruction takes 21 μ s.)

An XVM computer system was timed running five FORTRAN programs with and without floating point hardware. The results are as follows:

Program Description	XVM	XVM & FP15
One hundred iterations of the analysis of three body final states. A physics application program.	37.0 sec	3.0 sec
A least squares fit of data to a straight line.	5.1 sec	0.7 sec
A matrix inversion.	12.0 sec	5.0 sec
A test of all floating point functions.	11.4 sec	1.4 sec
A Fourier transform program.	16.9 sec	2.9 sec

FP15 System Features

- Directly or indirectly addressable up to 128K of core.
- Performs arithmetic operations on 18- or 36-bit integers and 36- or 54-bit floating-point numbers.
- Allows execution of in-line code – CPU instructions and floating point instructions may be interspersed as desired.
- I/O Processor can access memory on a shared basis with the floating point processor; however, the I/O processor takes priority over the FP15.
- When an undesired condition (underflow, overflow, abnormal division, or memory protect violation) occurs, the FP15 interrupts the CP stored program and automatically identifies the source of the interrupt.
- Worst-case multiplication and division times on normalized operands do not exceed 21 μ s.
- Possesses ability to convert floating point numbers to integers and integers to floating-point numbers.
- Remainder, product, and align bits in FMQ are accessible by appropriate software.
- Unnormalized and unrounded arithmetic may be specified.
- A class of non-memory reference instructions is available. These instructions use existing contents of FMA and FMB and require no memory reference.
- Built-in maintenance logic (maintenance mode) allows single or multiple substeps of an instruction. All major registers and control can be examined at the end of each step.
- Designed to operate with existing XVM options (Memory Management, etc.) with no increase in cycle time.

2.14 FP15 FUNCTIONAL DESCRIPTION

Figure 2-12 is a simplified block diagram of the FP15 Floating Point Processor. The FP15 is in parallel with the CPU on the memory bus, and monitors each instruction fetched by the CPU from core. If bits 00 through 05 of the instruction are equal to 71₈, it is recognized as a floating point instruction; the CPU treats the instruction as an NOP. The FP15 takes control of memory, inhibits the CPU, and then simulates the CPU by completing the normal interface between CPU and memory. After the floating point instruction has been executed, the CPU is enabled, and both the CPU and FP15 are free to monitor the next instruction.

Functionally, the FP15 contains a Memory Buffer register and two operand registers. The Memory Buffer register provides temporary storage for all words transferred to the FP15. One operand register consists of an 18-bit exponent register (EPA), a 35-bit mantissa register (FMA), and a 1-bit sign register (A SIGN).

This operand register is referred to as the floating point accumulator. An additional 35-bit register, designated FMQ, serves as an extension to the floating point accumulator.

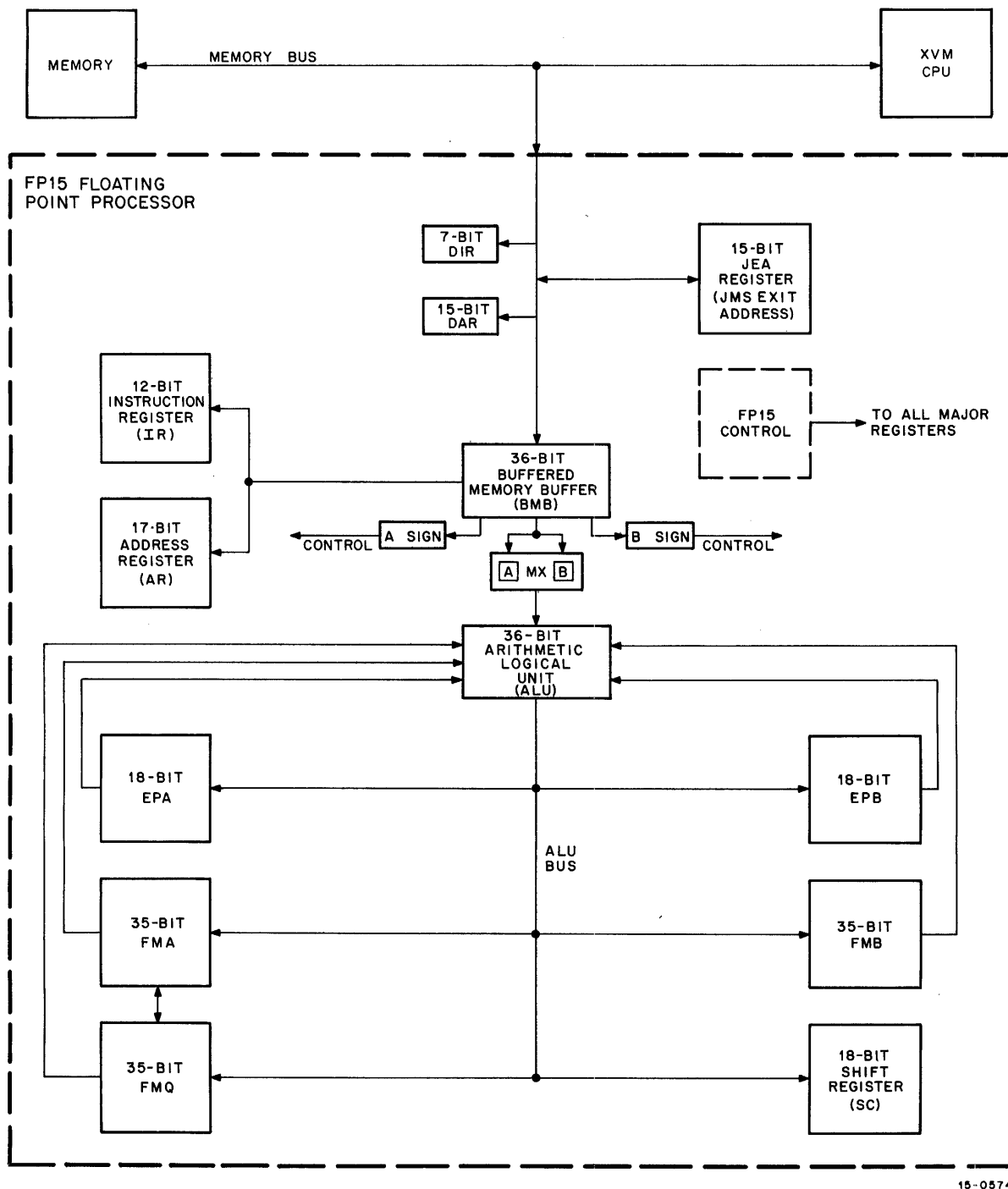


Figure 2-12 FP15 Floating Point Processor
Simplified Block Diagram

A second operand register consists of an 18-bit exponent register (EPB), a 35-bit mantissa register (FMB), and a 1-bit sign register (B SIGN). This second operand register, [EPB(B SIGN)FMB], serves as a temporary accumulator to hold the argument fetched from core.

The exponent registers store the exponents associated with floating point numbers and are not used during integer operations. Basically, if two numbers (integer or floating point) are to be manipulated, one number is loaded in the floating point accumulator by a load type instruction. The second number is normally loaded in the temporary accumulator [EPB(B SIGN)FMB] by an instruction specifying an arithmetic operation. Both numbers are gated into a 36-bit adder, where the arithmetic operation is performed. The result is then transferred to the floating point accumulator. The major registers are described below:

Memory Buffer Register – A 36-bit register that provides the FP15/memory interface. All data transferred into the FP passes through this register.

Adder – A 36-bit arithmetic logic unit (ALU) that serves as the central point in the FP15 and performs all arithmetic and logic operations. The output of the adder is connected to all major registers via an adder bus.

A SIGN – A 1-bit register used to store the polarity of the associated operand (A mantissa).

EPA – An 18-bit register used to store the 2's complement of the exponent associated with the mantissa loaded in the FMA. The most significant bit of the EPA represents the sign of the exponent; in single precision floating arithmetic, the most significant bit of the exponent is bit 09. It is therefore necessary to extend the value of this bit from bits 00 through 08. If bit 09 is a 1, bits 00 through 08 in the EPA are forced to 1s, and if bit 09 is a 0, bits 00 through 08 in the EPA are forced to 0s. The EPA and FMA serve as the floating point accumulator.

FMA – A 35-bit register used to store the integer in integer arithmetic, or the mantissa in floating point arithmetic. The binary point is located between bit 00 and bit 01 of the FMA.

FMQ – A 35-bit extension of the FMA register used during multiplication and division operations.

B SIGN – A 1-bit register used to store the polarity of the associated operand (B mantissa).

EPB – An 18-bit register used to store the exponent associated with the mantissa in the FMB. The most significant bit of the EPB represents the sign of the exponent. In single precision arithmetic, where the most significant bit in the EPB is bit 09, the value of this bit is extended to bits 00 through 08 (refer to EPA register). The EPB and FMB serve as a temporary accumulator to store the argument fetched from core. The EPB is a dynamic register and is therefore not directly accessible by software.

FMB – A 35-bit register used to store the integer in integer arithmetic or the mantissa argument in floating point arithmetic. The binary point is located between the most significant bit (bit 00) and bit 01 of the FMB. The FMB is a dynamic register and is therefore not directly accessible by software.

JEA (JMS Exit Address) – A 17-bit register used to store two status bits and a 15-bit base exit address for floating point interrupts. When an interrupt condition (overflow, underflow, abnormal division, or memory protect violation) occurs in the FP15, the base exit address (a unique address for each type of interrupt) is returned. This indicates a service routine associated with the interrupt. The guard bit is used in rounding operations.

Shift Counter – The shift counter performs the following functions:

- a. Keeps track of the number of words to be fetched from memory during the OPAND cycle.
- b. Keeps track of the number of words written into memory during the WRITE cycle.
- c. Keeps track of the number of shifts required for multiply and divide operations.
- d. Limits the number of shifts during normalizing to a maximum of 35_{10} .
- e. Controls the number of shifts required during alignment.
- f. Checks for exponents having differences which exceed 35_{10} .

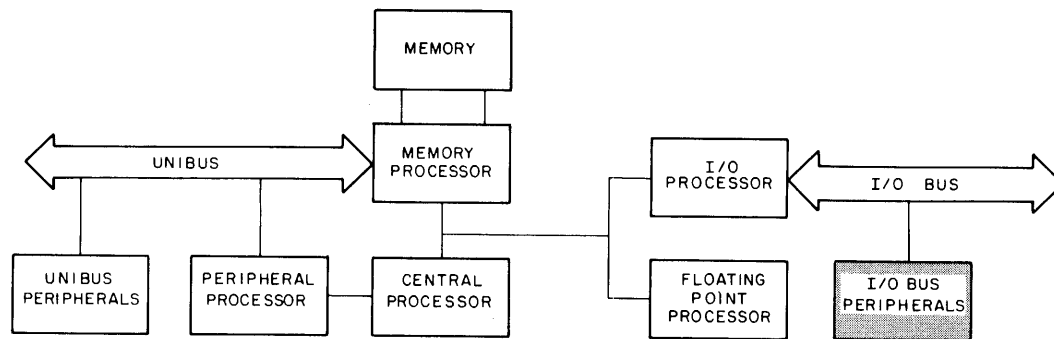
Diagnostic Instruction Register (DIR) – The 7-bit DIR determines the number of steps through which an instruction is to be sequenced.

Diagnostic Address Register (DAR) – The 15-bit DAR specifies the address in core where the contents of the registers are to be stored.

CHAPTER 3

PERIPHERALS

Section 1. Input/Output Peripherals



15-0855

There is a comprehensive range of peripherals available, built especially for the XVM I/O bus. The peripherals cover almost the entire spectrum of computer usage. For the user who wishes to expand into a new realm of data processing, the Computer Special Systems department of DIGITAL will cater to the demands of interfacing the XVM system to non-standard devices.

The more general types of peripherals attached to the XVM I/O bus are described in this section. One sub-section is allotted to each option, arranged in alphabetical order:

AA15-B*	Digital-to-Analog Multiplexer Control
AD15*	Analog-to-Digital Converter
BD15*	Industrial Control System (AFC-15/UDC-15)
CR15	Card Reader Controller
DC01-ED	Eight-Terminal Asynchronous Line Scanner
DP09-A	Synchronous Communications Control
GT15	Graphics Sub-system
LA36	DECwriter II
LP15	Line Printer Controller
LT15-A	Single Terminal Asynchronous Line Control
LT19-D	Multi-Terminal Asynchronous Line Control
PC15	High-Speed Reader/Punch Control
RF15	DECdisk Controller
RP15	Disk Pack Controller
TC15	DECtape Controller
TC59-D	Magnetic Tape Controller
VP15	Point-Plot Display Control
VT50	DECscope Video Terminal
VW01-B	Writing Tablet
XY15	X-Y Plotter Controller

*Currently available only on a special order basis.

AA15-B DIGITAL-TO-ANALOG MULTIPLEXER CONTROL

The AA15-B is an XVM-compatible option for controlling up to 32 digital-to-analog converters. The converters have a double-buffered, 12-bit input, and a bipolar output with a range from -10.24 to +10.235 V. Data is transferred by the XVM system processor to the AA15-B via its accumulator (AC) and the I/O bus.

The maximum capacity of the system is 32 digital-to-analog converter channels. The 18-bit word transferred from the AC to the AA15-B contains both the channel address (bits 00-05) and the data word (bits 06-17).

IOT Instructions

Mnemonic	Code	Description
ACB	705101	Clear B Buffer, all channels.
ALSC	705102	Load selected channel.
AUEC	705104	Update every channel.
ALSU	705106	Load selected and update every channel.
ALEC	705122	Load every channel.
ALU	705126	Load and update every channel.
ACA	705132	Clear A Buffer, all channels.
ACAB	705133*	Clear Buffers, all channels.

Analog Output Specifications

Absolute Accuracy	$\pm 0.05\%$
Linearity	± 0.5 L.S.B.
Resolution	1 part in 4096
Temperature Coefficient	± 40 ppm/ $^{\circ}\text{C}$
Output Voltage Swing	-10.240 V to +10.235 V
Output Current	± 5 mA
Output Impedance	100 m ohm
Output Slewing Rate	10 V/ μs
Settling Time	10 μs to +0.05% of full scale

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	47-63 Hz
Power Dissipation	60 W

Mechanical

Mounting	10.5 in. logic assembly mounted in H015 cabinet (H950)

Environmental

Temperature Range	0 $^{\circ}$ -50 $^{\circ}$ C (32 $^{\circ}$ -122 $^{\circ}$ F)
Humidity Range	10-90% without condensation

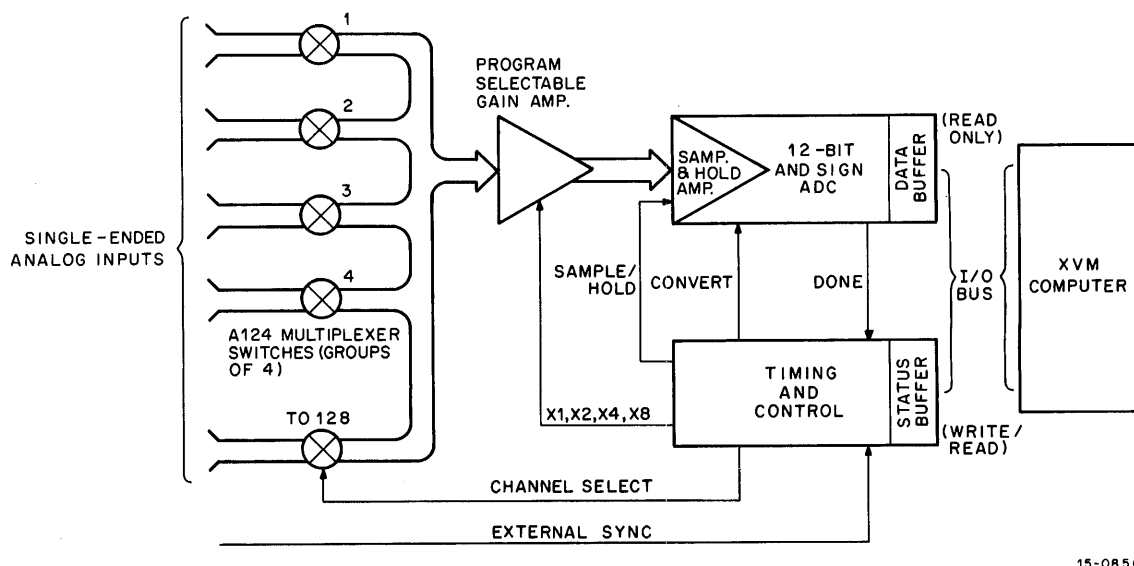
*Also clears the XVM accumulator.

AD15 ANALOG-TO-DIGITAL CONVERTER

The AD15 is a flexible high-performance, multichannel analog-to-digital conversion subsystem interfaced to the data channel of an XVM computer. Offering conversion rates of up to 22,000 per second, the AD15 satisfies laboratory, industrial and general purpose data acquisition applications.

The AD15 provides 13-bit digitization of up to 128 single-ended, bipolar analog signals having a nominal full-scale programmable input selection range of ± 1.25 , ± 2.5 , ± 5.0 , and ± 10.00 V. This performance allows input voltage as low as $\pm 300 \mu\text{V}$ to be detected. An integral sample and hold amplifier (S & H) provides a subsystem conversion aperture of 100 ns.

A choice of operating modes enables data transfers through either the accumulator or data channel with random or sequential sampling and internal or external synchronization (Figure 3-1).



15-0850

Figure 3-1 AD15 Analog-to-Digital Conversion Subsystem

The add-to-memory feature allows a converted analog input to be added to the contents of a memory location. If the value added to memory is sufficient to cause a sign change in the result, an interrupt will occur should the programmer so desire.

External synchronization may be used to trigger the analog-to-digital converter, thus allowing external real-time response and signal averaging.

Gains of 1, 2, 4, and 8 may be selected on the basis of the voltage range of the analog inputs.

The system provides bipolar operation of up to ± 10 V. Overload protection is ± 20 V. Recovery time is adequate to perform the next conversion within the specified accuracy.

“Power off” isolation and channel-to-channel isolation are maintained during power off periods.

IOT Instructions

Mnemonic	Code	Description
ADCV	701304	Load status register from accumulator, clear A/D done flag, and initiate conversion.
ADRB	701302	Read data buffer into accumulator and clear A/D done flag.
ADRS	701342	Read status register into accumulator.
ADCF	701362	Clear all AD15 flags.
ADSF	701301	Skip on A/D flag.
WCSF	701341	Skip on word count overflow flag.
MSSF	701321	Skip on memory overflow.

System Specifications

Resolution	12 bit + sign, 1 part in 4096 of full scale, 1 part in 8192
Code	2's complement, extended sign, right justified
No. of Analog Inputs	4 minimum, expandable to 128 in groups of 4
Input Voltage Range (Program Selectable)	± 1.25 V, ± 2.5 V, ± 5.0 V, ± 10.0 V full scale
Analog Input Connectors	16-channel Amphenol (Mating connector supplied) or BNC
Overload Capability	± 20 V on all ranges without damage
Noise	Less than ± 4 mV (p-p) RTO, 3 sigma confidence
Cross Channel Attenuation	-80 dB, 20 Vdc, 400 Hz for (p-p) signals, 100 ohm source impedance
Input Gain	Program selectable

Modes of Operation

Synchronization	Internal or external
Data Transfer	Program or data channel
Multiplexer	Random or sequential

Data Channel Addresses:

Status Word Count	24
Status Current Address	25
Data Word Count	26
Data Current Address	27
API Address	57
API Priority	0
Accuracy	$\pm 0.4\% \pm 1/2$ L.S.B. (including S & H and multiplexer)
Quantizing Error	$\pm 1/2$ L.S.B
Throughput Rate	22 kHz (including S & H and multiplexer)
Conversion Aperture	100 ns
Temperature Coefficient	± 30 ppm/ $^{\circ}$ C
Offset	$\pm 20 \mu\text{V}/^{\circ}$ C RTI $\pm 50 \mu\text{V}/^{\circ}$ C RTO
Input Impedance	1000 megohms in parallel with 20 pF (exclusive of wiring capacitance)
Input Isolation	Enhancement mode MOSFET switches, "off" when unselected or power off

Power Requirement	Single Phase
Input Voltage	115 Vac/230 Vac, single phase
Input Frequency	47 to 63 Hz, single phase
Power Dissipation	150 W

Mechanical

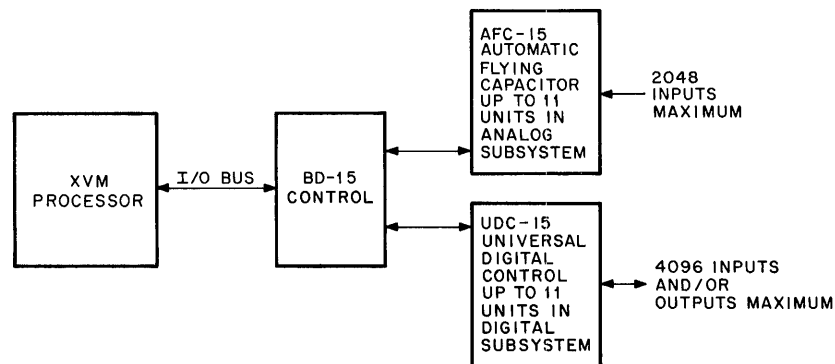
Dimensions	Mounted in H950 cabinet
Weight	175 lb (79.4 kg)

Environmental

Temperature Range	0°–50° C (32°–122° F)
Humidity	10–90% without condensation

BD15 (AFC15/UDC15) INDUSTRIAL CONTROL SYSTEM (Figure 3-2)

The Universal Digital Control (UDC-15) and Automatic Flying Capacitor (AFC-15) subsystems have been integrated to offer a unique, highly flexible digital input/output and analog data acquisition system for use with XVM computers. A single controller, the BD-15, acts as an interface between the computer and the UDC-15 and AFC-15 subsystems. All communications between the computer and the BD-15 controller are done through the I/O bus via the accumulator.



15-0541

Figure 3-2 Industrial Control System

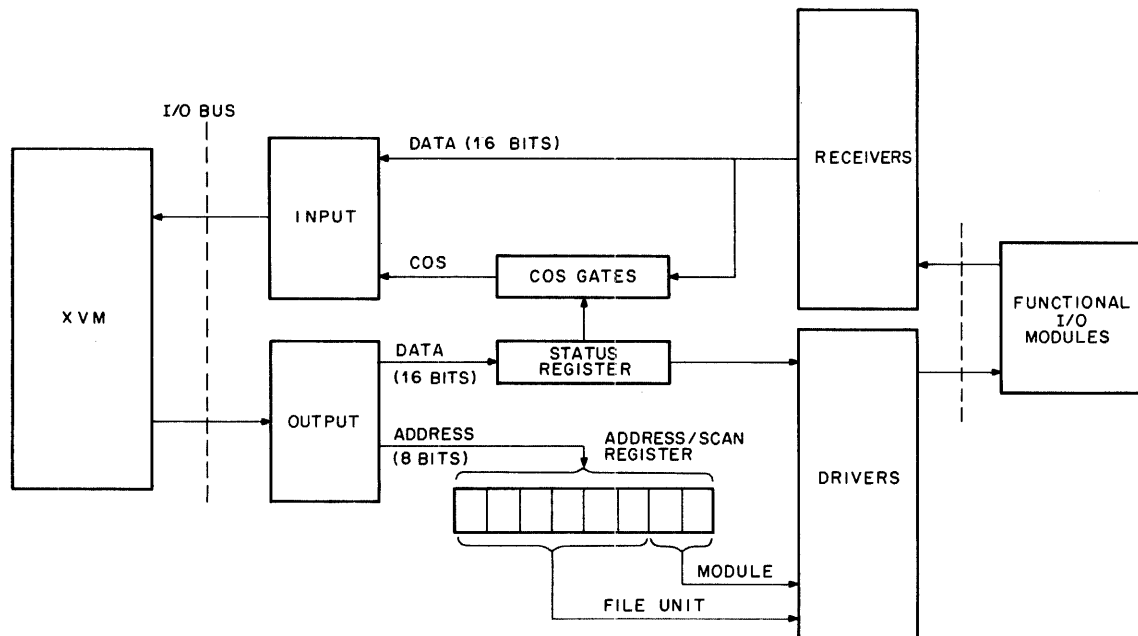
UDC-15 Digital Input/Output Subsystem

The UDC-15 is a digital information input/output option for industrial and process control applications. Through the central control unit (BD-15), it interrogates or drives up to 256 directly addressable digital sense and control functional I/O modules, each module containing 16 digital points for total system capability of 4096 digital points.

Automatic hardware logic rapidly identifies interrupting inputs according to input module type and address. Input change of state and direction are determined by hardware gating. Since both features are hardware implemented, the computer overhead usually associated with digital I/O is significantly reduced.

The UDC-15 and its controller, the BD-15, operate under computer program control as a high level digital multiplexer which interrogates digital inputs and drives digital outputs located in directly addressable modules. A 16-bit word transferred from the XVM accumulator and decoded in the BD-15 controller selects the address of either an output or an input module. Depending upon the module type selected, a 16-bit data output word can represent the single digital word required by a D/A converter or a counter, or 16 individual points for contact closure, pulse outputs, etc.

Input data is similarly handled. For example, a single 16-bit word can represent a counter or 16 contact sense points or 16 contact interrupt points. A "COS" gate function permits the system to detect any change of state and/or direction from the previous sampling before the word is transferred into the accumulator of the XVM (Figure 3-3).



15-0851

Figure 3-3 UDC-15 Input/Output Operation

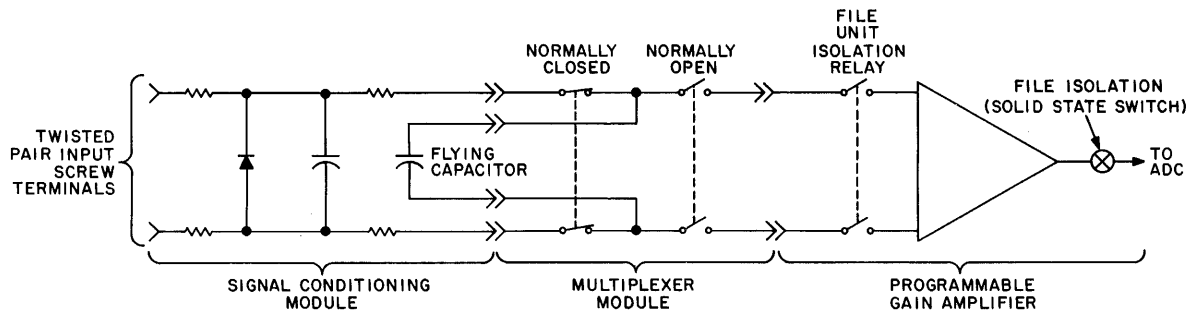
AFC-15 Analog Input Subsystem

The AFC-15 is an analog data acquisition subsystem for industrial and process control. Under control of the BD-15, the AFC-15 subsystem will multiplex up to 2048 differential analog inputs. The signals will then be converted to a 12-bit digital word and routed to the processor. The variable gain, selected by program and the signal conditioning modules, allows the subsystem to handle a wide range of input signals.

The AFC-15 analog input subsystem is particularly suited for data acquisition in the high-noise environments encountered in process monitoring and control, production testing, and laboratory applications. In such environments, common and normal mode noise, cabling, and grounding problems can greatly affect the operation of such transducers as thermocouples, strain gages, analytical bridges, and industrial milliamp current transmitters. These problems can also affect the accuracy and performance of the measuring system.

The flying capacitor multiplexing technique permits microvolt signals to be isolated, switched and digitized by an analog-to-digital converter with a high degree of noise immunity.

The flying capacitor is a two-pole RC filter network in which a second or "flying" capacitor is charged, then isolated, and switched to the measuring circuit. Since the source is never directly connected to the measuring circuit, extremely high isolation (10^{12} ohms) is achieved (Figure 3-4).



15-0545

Figure 3-4 Flying Capacitor Circuit

Lo-pass filtering per point (2.5 Hz cutoff) plus the high isolation of the flying capacitor technique provides high common mode noise rejection (120 dB at 60 Hz) without requiring expensive individually shielded input wiring.

AFC-15 Specifications

Resolution	Sign + 11 bits (2's complement)
Accuracy (for direct input)	$\pm 0.05\%$ of f.s. or $\pm 25 \mu\text{V}$ (whichever is larger); $\pm 1/2$ L.S.B.
Repeatability	$\pm 0.05\%$ or $\pm 10 \mu\text{V}$ same channel; $\pm 0.05\%$ or $\pm 20 \mu\text{V}$ channel-to-channel (whichever is larger); $\pm 1/2$ L.S.B.
Scan Rate, Including A/D Conversion	200 channels/second, maximum (20 samples/second, same channel)
Normal Mode Rejection	53 dB for frequencies 60 Hz or above
Common Mode Rejection	120 dB dc to 60 Hz
Input Overload	Amplifier fused against overload
Effect of Overload	Recovers to within stated accuracy for next channel
Channel-to-Channel Isolation	10^{12} ohms at dc, channel-to-channel; 10^8 ohms at dc, channels on same multiplexer module
Gain Accuracy	$\pm 0.02\%$
Gain Linearity	$\pm 0.01\%$
Temperature Coefficient	
Gain: 1,2	$10 \mu\text{V}/^\circ\text{C}$ RTI
Gain: 10 to 1000	$0.3 \mu\text{V}/^\circ\text{C}$ RTI + $100 \mu\text{V}/^\circ\text{C}$ RTO
Noise	$7 \mu\text{V}$ p-p RTI + $500 \mu\text{V}$ p-p RTO
Offset	Adjustable to zero
Electrical	
Input Voltage	115/230 Vac, single phase
Input Frequency	47-63 Hz
Power Dissipation	200 W
Mechanical	
Mounting	Mounted in its own H950 cabinet
Weight	150 lb (68 kg)

Environmental

Temperature Range	10–50° C (50° – 122°F)
Humidity Range	10–90% without condensation

BD15 SPECIFICATIONS**Electrical**

Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	200 W

Mechanical

Mounting	Mounted in H950 cabinet
Weight	150 lb (68 kg)

Environmental

Temperature Range	0°–50° C (32°–122° F)
Humidity Range	10–95% without condensation

UDC-15 Specifications

Modes of Operation	Programmed digital output, programmed digital input, and interrupt-controlled input.
Data format	16-bit I/O data words
Digital inputs/outputs	256 16-bit words maximum
I/O module selection	Directly addressable
Interrupt module identification	Module type code and module address
Interrupt scan	Locates address and type in 5 microsecond (typical); 20 μ s (worst case)
I/O data rate	10 ⁵ 16-bit word/second
Computer interface	Direct interface to XVM
System clock rates	Three available to each I/O word: line frequency 1.0 Vac; 175 Hz 1.75 kHz, adjustable; 1.75 kHz 17.5 kHz adjustable

Environmental

Temperature Range	0°–50° C (32°–122° F)
Humidity Range	10%–95% without condensation
Cooling/filtering	Dust filters and blowers provided in H963-R Cabinet, bottom exhaust

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	200 W

Mechanical

Mounting	Mounted in H950 cabinet
Weight	150 lb (68 kg)

CR15 CARD READER CONTROLLER

The CR15 Card Reader Controller is designed to read reliably the industry standard 80-column card.

The option consists of two main parts – the CR15 Controller, and the CR04 Card Reader. In addition, there are two types of card readers; one which reads at 300 cards per minute; and another which reads at 1000 cards per minute:

CR15-D – 1000 cpm reader plus interface

CR15-F – 300 cpm reader plus interface

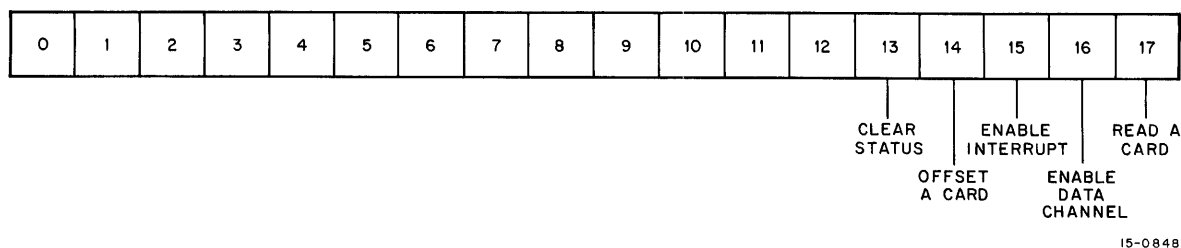
Both systems are available in 115 V, 60 Hz versions as well as 230 V, 50 Hz.

The CR15 has device I/O handlers to enable the unit to be used under any of the currently supported XVM software systems. The Controller operates in either of two modes:

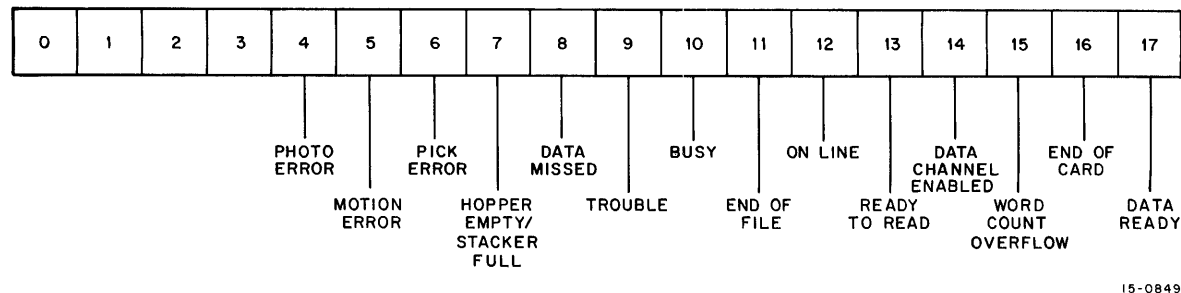
1. Program Controlled Transfer – Where the I/O handler relies upon the interrupt system to indicate when the next column of data is waiting to be read.
2. Data Channel Transfer – In this mode, the controller will transfer the contents of a card to a predefined buffer; an interrupt will only be generated when the entire card has been read, or when the required number of words have been read. (For a detailed explanation of multi-cycle data channel, refer to Paragraph 1.3, Chapter 1.)

IOT Instructions

Mnemonic	Code	Operation
CRCON	706704	Load control word from accumulator.



CRSKP	706701	Skip if card reader interrupt is set.
CRLD	706702	OR CR data buffer into bits 6–17 of AC.
CRLS	706772	Read CR status into AC.
CRPC	706724	Clear status register (except end of card bit).



Data Channel Addresses

Word Count	22
Current Address	23
API Address	55
API Priority	2

Card Reader Specifications

	CR15DA* and CR15DB Table Top	CR15FA* and CR15FB Table Top
Reading Rate (cpm)	1000	300
Input Hopper Capacity (cards)	950–1000**	550–600**
Output Hopper Capacity (cards)	950–1000**	550–600**
Size Envelope (H × W × D)		
Inches	17 × 24 × 19	13 × 20 × 15
Centimeters	43 × 61 × 48	33 × 50 × 38
Weight (max.)		
Pounds	100	70
Kilograms	45.4	31.8
Power Consumption (VA)		
Starting	1500	1500
Running	460	460
Heat Dissipation		
Btu/hour	1600	1600

Controller

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	100 W

Mechanical

Mounting	5.25 in. logic assembly mounted in LP15 cabinet (H950)

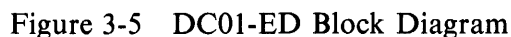
Environmental

Temperature Range	0°–50° C (32°–122° F)
Humidity Range	10–95% without condensation

*A suffix denotes 115 V, 60 Hz; B suffix denotes 230 V, 50 Hz

**Depending on card stock

The DC01-ED scanner is designed as an efficient monitoring device requiring a minimum of computer control. The scanner, once started, continuously samples all eight device lines. When an active line is sampled and found to have set flags, an indication is given to the computer. A raised flag indicates that a device has been active. If the flag is sensed following transmittal of data, that data is in the receiver awaiting read-in. Because an active teletype does not give an indication whether data has been transmitted or received, the computer must monitor the status of every device (Figure 3-5).



Serial-to-parallel and parallel-to-serial conversions are accomplished within the DC01-ED for each of the eight serial lines.

An IOT instruction enables the scanner which sequentially samples each of the eight serial lines searching for a receive flag. When a flag is recognized, the scanner stops and an interrupt is requested. (The XVM must recognize only this one flag.) The service routine may be called for by either program interrupt (PI) or by automatic priority interrupt (API). The active line number and the received data are read into the computer accumulator by means of an IOT instruction; the scanner is then released.

The scanner is stopped and loaded with a line number by means of program instruction. The character to be transmitted is loaded into the appropriate transmitter of the DC01-ED by the logic. Then the scanner is released. No transmit-done flag exists. All transmitted data is echoed back to the receive logic; therefore, only one flag is required for each connection. Comparison of the transmitted character with the received echo must be performed by the software.

Both total loss of data and dropping of bits down the transmission line can be detected by the software. Operator error (using the terminal keyboard during message transmission) is detected in a similar manner.

IOT Instructions

Mnemonic	Code	Description
SSF	70XX01	Skip on scanner flag.
RSD	70XX02	OR the scanner line number and the selected receiver flag and the scanner flag.
DIS	70XX04	Disable scanner (stop scanner and clear all flags).
LSA	70XX21	Stop scanner and load scanner line register.
LSD	70XX22	Load selected transmitter line data.
STS	70XX24	Clear scanner flag and start scanner at present line number.
	70XX27	Stop scanner, load line address and transmitter, and restart scanner at selected line address.

Specifications

Capacity	To eight terminals, private modems, or other serialized terminal equipment
Line Driving Capability	20 mA current-loop (1500 feet) at 110 baud; EIA levels (50 feet)
Transfer Rates	75, 110, 150, 300, 600, 1200 and 2400 baud. Additional rates optional
Rate Assignments	Strappable per Transmit/Receive pair
Operational Mode	Half-duplex with echo or echo-plex
Data Code	Five to eight bit serial-start-stop
Stop Code	1, 1.5 or 2 units

Environmental

Temperature Range	0° – 50° C (32° – 122° F)
Humidity Range	10–95% without condensation

Electrical

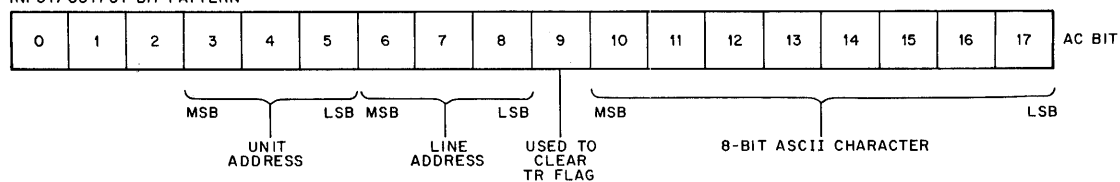
Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	400 W

Mechanical

Mounting	Up to four DC01 units may be mounted in an H950 cabinet
Weight	200 lb (90.7 kg)

Unit No.	Device No.	Subdevice No.	API Address
1	44	0-2	70
2	44	4-6	71
3	45	0-2	72
4	45	4-6	73
5	46	0-2	74
6	46	4-6	75
7	47	0-2	76
8	47	4-6	77

INPUT/OUTPUT BIT PATTERN



15-0846

DP09-A SYNCHRONOUS COMMUNICATIONS CONTROL

The DP09-A is a bit-synchronous data communications interface and control. It may be used to connect the XVM I/O bus to serial communications devices such as the Bell System type 201 or 301. Operation is full duplex, both transmit and receive sections being double-buffered. Character length may be from 5 to 9 bits, and is selected by different jumpers on a 50-pin Cannon connector.

The DP09-A is in the idle state until made active by either the XVM processor transmitting a sync character to the DP09-A or the DP09-A receiving a sync character from the data set.

The sync characters are:

Character Length (N)	Sync Character
6	010 110
7	0 010 110
8	10 010 110
9	X10 010 110 (X not used in sync character determination)

The DP09-A will return to the inactive (idle) state if:

1. While transmitting, Idle mode is disabled and no character has been transferred to the DP09-A from the computer within $Nt \mu s$ of the transmit flag being set. (N is the number of bits/character, t is the time to transmit a bit on the line. Nt is therefore the time to transmit a full character on the communications line.)
2. While receiving, the Clear Receive Active (CRA) command is issued, or if no character is received from the communication line for 1.5 bit times.

Idle mode is a feature of the DP09-A which permits retaining the communications system in an active (and synchronous) state when no new characters are available. When Idle mode is enabled, the last character continues to be transmitted until such time that a new character is ready. The transmit flag continues to be raised at the end of each character transmission.

IOT Instructions

Mnemonic	Code	Description
SRE	702544	Set Ring Enable
CRE	702604	Clear Ring Enable
SRI	702561	Skip on Ring Indicator
CRF	702562	Clear Ring Flag
STR	702564	Set Terminal Ready
CTR	702602	Clear Terminal Ready
SSR	702601	Skip on Data Set Ready
CRA	702622	Clear Receive Active
STF	702521	Skip on Transmit Flag
TAC	702501	Transmit a Character
CTF	702502	Clear Transmit Flag
CIM	702504	Clear Idle Mode
SIM	702524	Set Idle Mode
SRF	702621	Skip on Receive Flag
RRB	702522	OR Receive Buffer to AC
SEF	702541	Skip on Receive End Flag
CEF	702542	Clear End Flag

Specifications

TRANSMIT FLAG	Set when DP09-A is ready to receive a character from the computer for transmission.
RECEIVE FLAG	Set when the DP09-A is ready to transfer a character to the computer.
RECEIVE END FLAG	Set when no bit is received from the sending device within 1.5t (t is the normal interbit spacing, the reciprocal of the baud rate).
RING FLAG	Set when a remote communications device calls up the DP09-A and is ready to transmit. Only causes an interrupt if Ring Enable is set (see instruction list).
DATA SET READY FLAG	Set when the local Data Set is ready for operation. (This flag cannot cause an interrupt)
API Address	62
API Priority	2

Mechanical

Mounting	10.5 in. logic assembly mounted in negative bus cabinet

GT15 GRAPHICS SUBSYSTEM

The GT15 Graphics Subsystem consists of four interconnected units:

1. VT15 Graphics Processor
2. VV15-A Arbitrary Vector Generator
3. VT07 Graphics Console (or VT04)
4. VL07 Light Pen (or VL04)

VT15 Graphics Processor

The VT15 Graphics Processor is connected to the XVM Processor via the I/O bus (Figure 3-6). Once the VT15 has received the start signal and address, it will run continuously. The display file for the VT15 is held in XVM memory so that the XVM Processor and VT15 processor interact easily through the hardware; their programs can interact in memory.

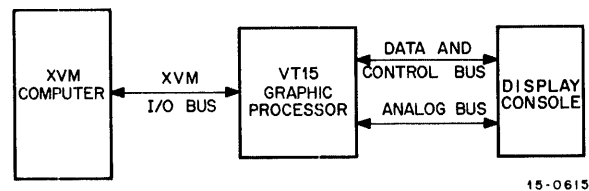


Figure 3-6 VT15 Graphic Processor, Block Diagram

Two 18-bit registers are used for memory buffer functions which permit overlap for memory cycle times and allow faster instruction execution times. The VT15 has a set of basic machine language instructions that give the Graphic 15 System the utmost versatility in the display of points, basic vectors, graph plots, and ASCII characters.

Vectors are drawn on the scope by use of a “stroke vector” technique for maximum speed and accuracy.

VT15 Specifications

Virtual Paper Size	12 bits × 12 bits
Screen Display Size	10 bits × 10 bits
Scales	4-bit increment register (0–15) characters and vectors
Brightness	3-bit register (8 levels)
Line Types	4; 1 solid and 3 types of broken lines
Vector Specification	Relative
Point Specification	Absolute
Name Register	6 bits (128 values)
Synchronization	Display refresh rate can be synchronized to line frequency or harmonics
Characters	64 printing characters 4 special (alt mode ESC, CR, LF, TAB)

Controller

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	1.0K W

Mechanical

Mounting
Weight

Mounted in H950 cabinet
300 lb
(136 kg)

VV15-A Arbitrary Vector Generator

The VV15-A Arbitrary Vector Generator computes the angle of a vector from its X and Y components. The VV15-A speeds up the display and saves space in memory by reducing the size of the display files.

VT07, VT04 Graphics Console (Figure 3-7)

The VT07 and VT04 are rectangular self-contained CRT monitors with CRT power supplies, deflection amplifiers, and six console pushbuttons which generate program interrupts. Provision for implementing a light pen, writing tablet and keyboard options is also included.

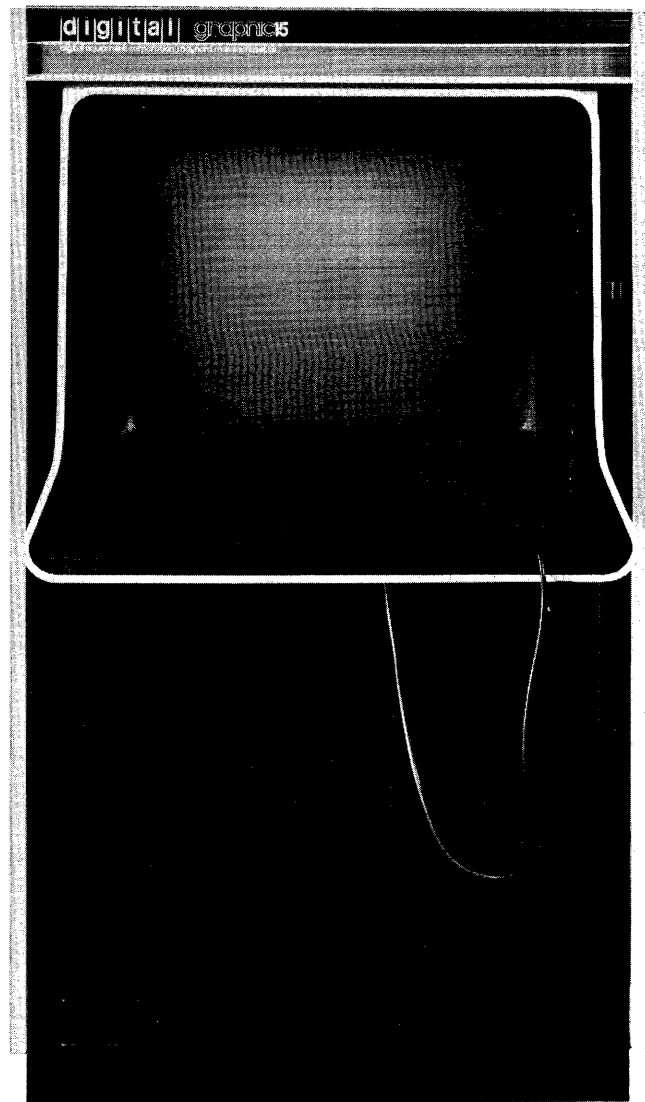
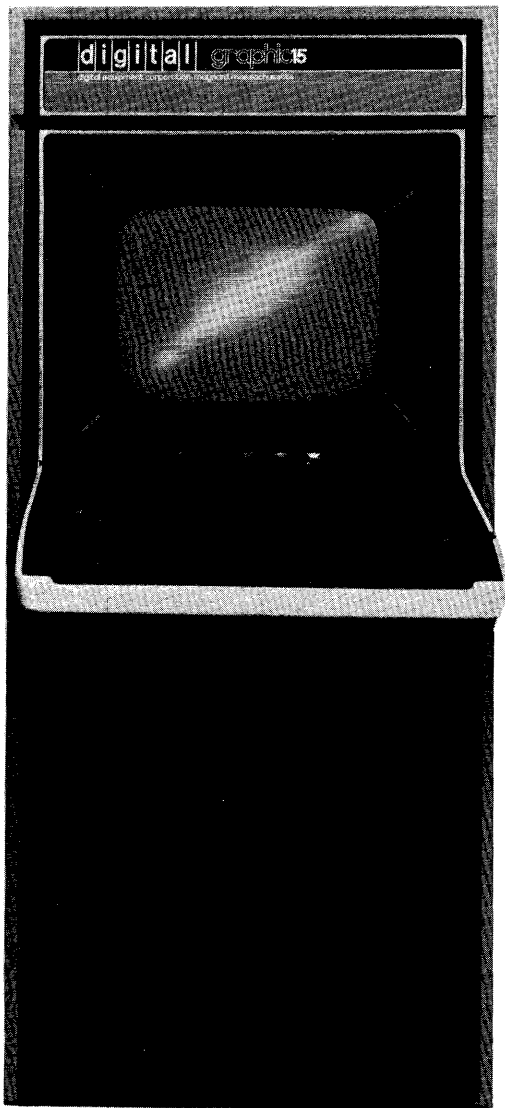


Figure 3-7 VT07 and VT04 Graphic Display Consoles

VT07, VT04 Specifications

	VT07	VT04
Screen Size	21 inches diagonal	17 in. diagonal
CRT Shape	Rectangular, 12 in. × 14 in.	Rectangular, 9 in. × 10-1/2 in.
Major Display Area	12 in. × 12 in.	9 in. × 9 in.
Minor Display Area	2 in. × 12 in. (programmable)	1-1/2 in. × 9 in.
Vector Drawing Rate	0.33 in. per μ s	0.25 in. per μ s
Flicker-free* Presentation	10,000 vector inches	7,000 vector inches
Character Drawing Capability	2,800 maximum	Same as VT07
Spot Size	0.015 in. (within 10-in. diameter circle about CRT center)	Same as VT07
Spot Jitter	0.005 in.	Same as VT07
Display Drift	1% of full screen (over 24 hours)	Same as VT07
Spot Repeatability	±0.020 in.	Same as VT07
Linearity	±0.5% of full screen	±1% full screen
Brightness	30 ft lamberts (min) with 100 line raster	50 ft lamberts with 200 line raster PT385 standard, others optional
Physical Dimensions	51-1/2 × 30-3/4 × 45-3/4 in. (130.8 × 78.1 × 116.2 cm)	
Power Dissipation	At 110 Vac 12 A surge, 6 A running	Same as VT07
Environmental		
Temperature Range	5° – 35°C (40° – 95°F)	
Humidity Range	20–55% (relative)	

*Assuming no CPU intervention

VL07, VL04 Light Pen

The VL07 (or VL04) Light Pen is a photosensitive device that detects the presence of illuminated phosphors on the screen of the VT07 (or VT04). The light pen photo-amplifier is interfaced to the VT15 Graphics Processor via the VT07 (or VT04) logic panel. The uses of the light pen depend upon the program, but normal software includes routines to allow the light pen to indicate unwanted lines, draw new lines, and choose routines by indicating legends in the "menu" or "offset" area on the display.

VM15 Display Console Multiplexer

The VM15 Display Console Multiplexer permits up to four Type VT07 or VT04 Display Consoles, and four Type VL07 or VL04 Light Pen options to be interfaced with a single VT15 Graphic Processor. This option permits these equipments to be situated at remote locations and to share the use of the VT15 Graphic Processor and XVM computer.

NOTE

The maximum number of display consoles is four, however the video display is limited in the number of vector inches it can support. Two consoles can be handled easily without noticeable flicker.

LA36 DECwriter II

The LA36 DECwriter II is a fast, reliable, data terminal. The unit prints at a speed of 30 characters per second continuously. If, due to a carriage return or other control character, the 16-character buffer should have more than one character in it, then a 60-character per second "Catch-up" mode is used to clear the buffer. Data entry is made from a 96- or 128-character keyboard.

The DECwriter II will make a hard copy original plus up to five copies on any width of continuous, tractor-driven paper between 3 and 14-7/8 inches wide.

The LA36 is compatible with all XVM Terminal Controllers, e.g., DC01-ED, LT19-D, LT15-A, and is also the standard console terminal device on XVM Systems.

Standard Features

- True 30-character per second throughput
- Accommodates 6-part form (0.020 maximum thickness)
- Handles variable width forms; 3 through 14-7/8 in. wide
- 132-column printing; 10 characters per inch horizontal
- 6 lines per inch vertical spacing
- 128-character ASCII upper/lower case set
- 7 × 7 dot matrix
- ANSI-standard typewriter-like keyboard
- Quiet operation
- Excellent character readability
- Integrated, 20 mA current loop interface with jumpers for active and passive modes
- Fine vertical adjustment for accurate forms placement

Optional Features

- Paper stacking tray
- Casters for rear of cabinet
- Right and/or left work surface

Operator Controls

Power On-Off	Applies and removes ac power to entire machine
Line/Local	Selects on-line or local operation
Baud Rate-110, 150, 300	3-position switch selects the baud rate clock frequency for communications line operation
Forms thickness adjustment	Located on right side of print head carriage. Selects proper gap for 1-through 6-part form. Approximately 1 click for each part.
Right tractor adjustment	Thumb screw may be loosened to allow movement of right tractor for various forms widths
Fine vertical tractor release	Line feed knob may be pressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

Specifications

Main

Printing Speed	30 char/sec, asynchronous
Number of columns	132
Printing characters	64/96 character ASCII set
Keyboard characters	97 or 128 (switch selectable)

Printing

Type	Impact 7 × 7 dot matrix
Vertical spacing	6 lines/inch
Horizontal spacing	10 char/inch

Paper

Type	3-14-7/8 in. wide, continuous form tractor-driven, original plus 5 copies (20 mils maximum pack thickness)
Slew speed	30 lines/sec

Mechanical

Mounting	1 free-standing unit
Size	33.2 inches high (84.3 cmm) × 27.5 inches wide (69.8 cm) × 24 inches deep (61 cm)
Weight	102 lb (46.3 kg)

Power

Input current	2 A at 115 V, 1 A at 230 Vac
Heat dissipation	300 W printing; 160 W nonprinting

Environment

Operating temperature	10° C to 40° C (50° – 104° F)
Relative humidity	10% to 90%

Ribbon

Digital-specified nylon fabric, spool assembly 0.5 inches wide × 40 yards. Order No. 36-10558

LP15 LINE PRINTER CONTROLLER

The XVM Systems currently have three models of LP15 Line Printers available. The types and their differences are:

Option	Lines/Min	Columns	Characters
LP15-R	1200	132	64
LP15-V	300	132	64
LP15-W	300	132	96

All of these printers may use the same system programs, allowing for the differences in line lengths and considering that the 64-character printers convert all lower case character codes to upper case before printing.

Once started by an LPP1 or LPPM command, the line printers use the multi-cycle data channel facility of the XVM to access a character buffer in core. This buffer contains up to 256 lines of characters, each line terminated by a line feed or other control character. In this way, up to 256 lines may be printed without further attention from the program.

The data buffer area must begin with a 2-word header in the format shown (Figure 3-8).

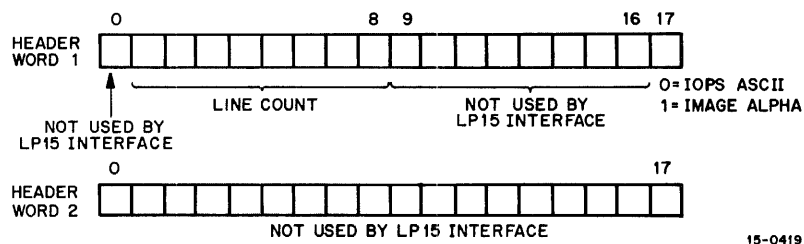


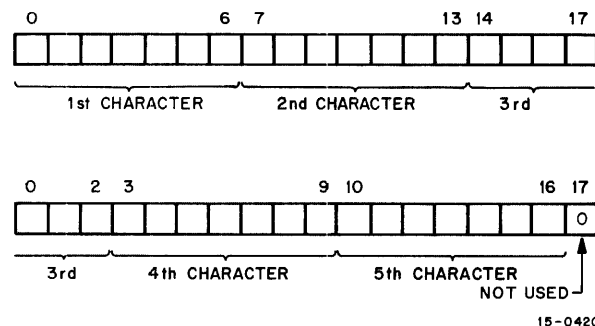
Figure 3-8 LP15 Data Buffer Header Format

Bit 0 and bits 9-16 of header word 1 are not used by the hardware. Bit 0 indicates the line printer mode of operation to the software. It is set in multi-line mode and cleared in single-line mode. Bits 9-16 contain software flags not used by hardware.

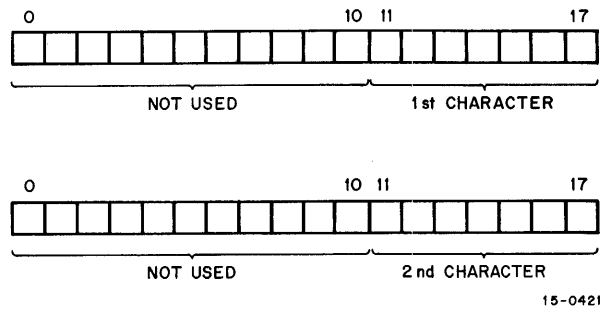
Data Word Formats

1. IOPS ASCII (5/7 ASCII Packing Scheme)

In the IOPS ASCII format, five 7-bit character codes are contained in two consecutive words, as shown below.



2. IMAGE ALPHA Format



IOT Instructions

Mnemonic	Code	Description
LPP1	706541	The line printer prints a single line of text.
LPPM	706521	The line printer enters Multi-line mode.
LPSF	706501	Skip if Done or Error. Skips the following instruction if the printer's Done or Error flag is set.
LPEI	706544	Enable interrupt system. Connects the printer to the XVM priority interrupt system. Either the Done or Error flag will cause an interrupt if enabled.
LPCD	706621	Clear Done flag.
LPCF	706641	Clear status register and Error flag.
LPRS	706642	OR status register. This IOT reads into the AC a register made up of the following system flags:

Bit	Flag
0	Error
1	LP Alarm
2	Line Overflow
3	Illegal HT
4	Busy
5	Done
6	Interlock

Data Channel Addresses and Priority

Word Count	34
Current Address	35
API Address	56
API Priority	3

Controller

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	47-63 Hz
Power Dissipation	400 W

Mechanical

Mounting
Height

Mounted in H950 cabinet
200 lb (90.7 kg)

LP05 Printer**Electrical**

Input Voltage
Input Frequency
Power Dissipation

115/230 $\pm$ 10% Vac, single phase
50/60 Hz $\pm$ 2%
500 W

Environmental

Temperature Range
Humidity Range

50°–100° F (10° – 38°C)
30–90% without condensation

Mechanical

Dimensions
Weight

22(56 cm) $\times$ 34 (86 cm) $\times$ 45 (114 cm) in.
340 lb (154 kg)

LT15-A SINGLE ASYNCHRONOUS LINE CONTROL

The LT15-A Single Asynchronous Line Control is a device whose sole purpose is to interface one terminal to the XVM I/O bus. In standard form, any 20 mA device operating at 110 speeds to 2400 baud can be connected.

The LT15-A is handled in a similar fashion to the console terminal IOT instructions.

IOT Instructions

Mnemonic	Code	Description
TSF1	704001	Skip on transmit flag
TCF1	704002	Clear transmit flag
TLS1	704004	Load transmit buffer
KSF1	704101	Skip on receiver flag
KRB1	704102	OR buffer to AC and clear flag

Mechanical

Mounting	Occupies space in the BA15 logic assembly

API Addresses

Transmit	74
Receive	75
Priority	3

NOTE

The IOT instructions and API assignments are also those which are used on the first channel of an LT19-D. This means that if both devices are connected to the system, only one can be used. Either LT15-A or channel 0 of the first LT19-D must be removed. Fortunately, it is not necessary to add LT19-D channels in strict numerical order. Therefore, a system could have both devices installed and used as shown below:

LT15-A	As channel 0
LT19-E(1)	As channel 1
LT19-E(2)	As channel 2

etc., up to LT19-E(4).

LT19-D MULTI-TERMINAL ASYNCHRONOUS LINE CONTROL

The LT19 Multi-Terminal Asynchronous Line Control increases the basic terminal facility by permitting data transfers between the XVM Processor and any combination of up to five terminals or level-operated data terminal devices that are EIA-compatible* (Figure 3-9).

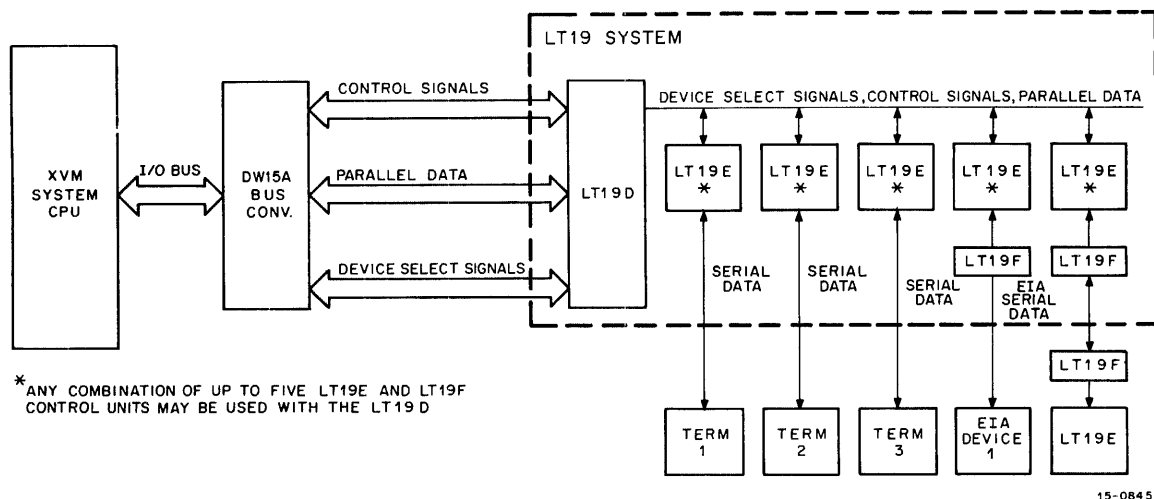


Figure 3-9 Typical LT19 System Configuration

The LT19 system performs two types of programmed-controlled operations during which data is transferred between a processor and a terminal or EIA device (for example, Dataphone® interface). A transmit operation is performed to transfer data from the XVM Processor to a terminal (or EIA device) and a receive operation is performed to transfer data from a terminal keyboard (or EIA device) to a processor.

Each LT19-E can support one LT19-F. The LT19-F supplies EIA logic levels which are compatible with certain types of Dataphones, such as the Bell 103A. Although the LT19-E,F combination supplies the necessary data signals to the Dataphone, it does not supply control signals.

NOTE 1

The overall speed for all LT19-E channels is limited to 30,000 baud, for all N channels combined, where $N=1$ to 16_{10} . This limitation is imposed so that the normal processor service routines may handle all N channels concurrently.

NOTE 2

Assign the highest speed channels to the first channels in the system to keep the skip chain short. In a multiple LT19-D system, all high-speed channels must be first to prevent a low-speed channel from locking out a high-speed unit.

®Dataphone is a registered trademark of Bell Systems.

*Logic levels specified in Electronic Industries Association (EIA) Standard RS-232C, "Interconnection of Data Terminal Equipment with a Communication Channel."

LT19-H DATA COMMUNICATIONS CABLE OPTION

The LT19-H is a data communications cable option used for interprocessor buffer applications. It is used between an LT19 and PT08, between two LT19s, or between the LT19 and other devices with equivalent interface and timing characteristics. The cable is available in five lengths:

Option	Length (ft)
LT19-HA	50
LT19-HB	100
LT19-HC	150
LT19-HD	200
LT19-HE	250

IOT Instructions

Terminal Instructions

Code	Description
704001	Skip if transmitter flag is set.
704002	Clears transmitter flag.
704004	Loads transmitter module and sends character to terminal.
704101	Skip if receiver flag is set.
704102	ORs contents of receiver module and clears receiver flag.

Specifications

Character Code	5- or 8-bit* character code
Start Code	One unit start code
Stop Codes	1-, 1.5-, or 2-units* stop code
Operation	Full duplex
Service	Up to five units per LT19-D
Speed, LT19-E	Variable to 30,000 baud. See Note in text.
Transmission distance	1500 ft, maximum; 20 mA current Loop only; 110 baud. Maximum length of LT19-H is 250 feet.
Temperature Range	55°–122° F (15°–50° C)
Humidity Range	10–95%
Primary Power Requirements	115 V, 60 Hz, 250 W (approximately)
API Addresses	
Transmit	74
Receive	75
Priority	3

Mechanical

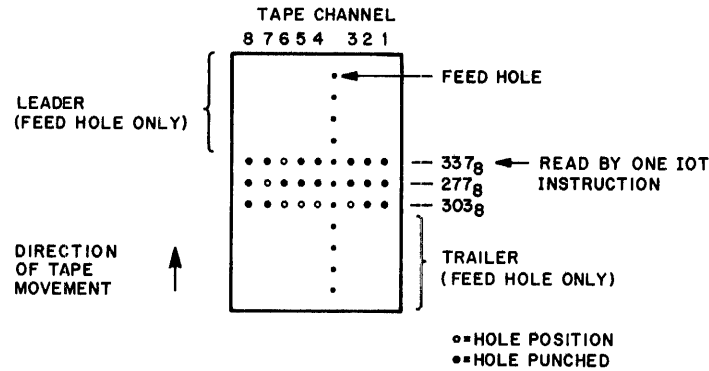
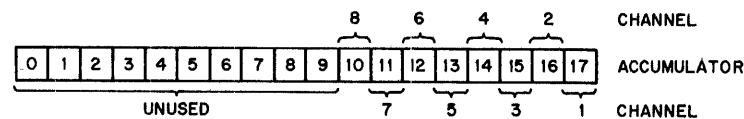
Mounting

LT19D 10.5 in. logic mounts in a negative bus H950 cabinet

PC15 HIGH-SPEED PAPER-TAPE READER PUNCH CONTROLLER

The PC15 High-Speed Paper-Tape Reader/Punch is used to input perforated paper-tape programs into core memory, or to punch core memory programs or data on paper tape. Information is punched on eight-channel fanfolded paper tape in the form of six- or eight-bit characters at a maximum rate of 50 characters/second. Information is read at a maximum rate of 300 characters/second. The PC15 consists of a PC05 Paper-Tape Reader/Punch with interface and control logic for using the reader/punch with an XVM System. Two modes of operation are possible: alphanumeric and read-in.

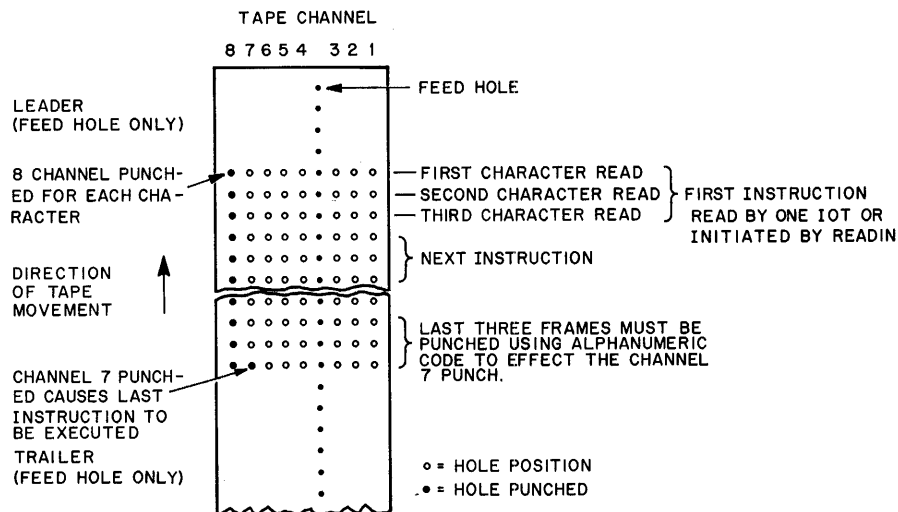
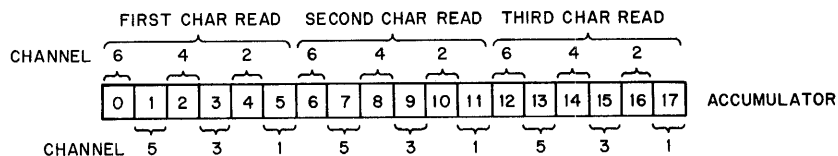
1. **Alphanumeric Mode** – The reading of data in this mode is accomplished by the reader sending one eight-bit character to the AC on receipt of the requisite 301.



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2. **Binary In Mode** – In this mode, the reader assembles three six-bit characters into an 18-bit word, and then they are transferred directly to memory. Only characters that have hole 8 punched are read.

Hole 7 is used in Hardware Read-In (a form of binary) and will cause the system to execute the last instruction that was read from the tape.



15-0233

Reader IOT Instructions

Mnemonic	Code	Description
RSF	700101	Skip next instruction if reader flag is a 1.
RCF	700102	Clear reader flag. Read reader buffer, inclusively OR contents of reader buffer with AC, and deposit result in AC.
RRB	700112	Read reader buffer and clear reader flag. Clear AC and transfer contents of reader buffer to AC.
RSA	700104	Select alphanumeric mode. RSB 700144 Select binary mode.

Punch IOT Instructions

Mnemonic	Code	Description
PSF	700201	Skip next instruction if punch flag is a 1.
PCF	700202	Clear punch flag and punch buffer.
PSA	700204	Select alphanumeric mode and punch one character. Set punch flag when punch is complete.
PSB	700244	Select binary mode and punch one six-bit character. Set punch flag when punch is complete.

Programming Considerations

To use the reader at the transfer rate of 300 cps, a select IOT (RSA or RSB) must be issued within 1.67 ms after each flag. This action is required because a 40 ms reader stop delay is present. When this delay is activated, it overrides the select IOT input and subsequently stops the tape. Thus, if a new select IOT is not received within 1.67 ms of the setting of the flag, the reader operates start-stop and reads characters at a maximum of 25 cps rate. No data is lost.

The RSA (700104) and RCF (700102) can be microprogrammed to form a 700106 instruction. This instruction reads the character, transfers the character to the accumulator, and advances the tape in one operation. An RSF (700101) and RRB (700112) cannot be microprogrammed.

Channel 7 can be punched using only the Alphanumeric mode. Therefore, when punching the last character of a tape for hardware read-in operation, the last character must be punched in the alphanumeric mode.

The PCF instruction can be microprogrammed with a PSA or PSB instruction to form 700206 or 700246. This instruction clears the punch flag and buffer, selects the applicable mode, loads the punch buffer, advances the tape, and perforates the character on tape. After completing the punching, the punch flag is set to denote that the punch can accept another character. Microprogramming the PCF and PSF instructions is not allowed.

API Address	50
API Priority	2

NOTES

1. Fanfold paper tape is DEC Part No. 36-05363-01.
2. All PC05 units are 115 Vac.
3. This device is cabinet-mounted, thus it cannot be operated remotely.

Environmental

Temperature Range	55°–110° F (13° –43°C)
Humidity Range	20–95% without condensation

Electrical

Input Voltage	115 Vac $\pm$ 10%
Input Frequency	50/60 Hz, single phase

Mechanical

Mounting	Occupies 10.5 in. cabinet space in the XV100 cabinet

RF15 DECdisk CONTROLLER

The XVM DECdisk system (Figure 3-10) consists of two elements: an RF15 Control Unit and up to eight RS09 Disk Units. The control unit and up to two disks may be mounted in one cabinet. Up to three disk units may be housed in each additional cabinet.

The control communicates directly with the XVM I/O processor. All transfers – data, address, and control – take place through the I/O bus. Data and address transfers use the multi-cycle block transfer facility. Control transfers use the programmed IOT (Input Output Transfer) mode.

The fixed head assemblies eliminate head positioning mechanics and stringent vibration limitations.

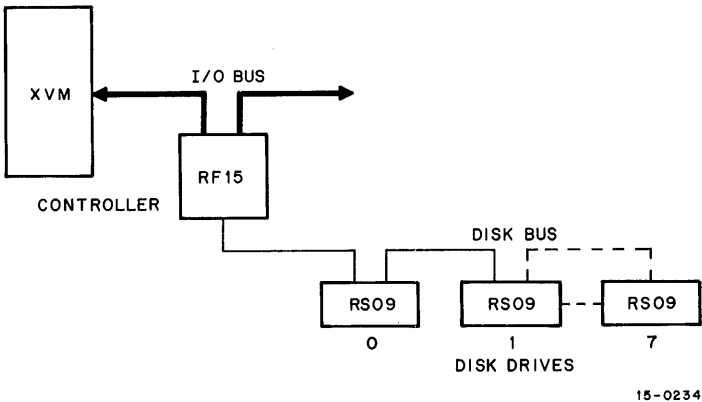
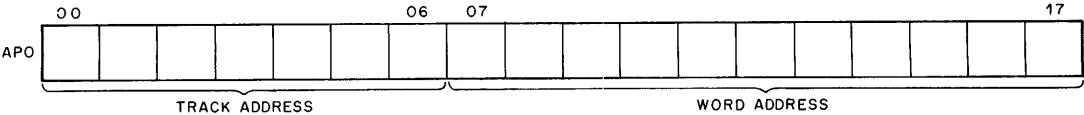


Figure 3-10 XVM DECdisk System

Data are recorded serially on each track in 24-bit words; 18 data bits, one parity bit, four guard bits, and one data control bit. Each 24-bit word unit is identified by an address that is prerecorded serially exactly one word before the word with which it is associated. The controller can then assemble and identify the address before the heads reach the word itself. Each address is 13 bits long; 11 bits supply addressing data, one bit is a control bit, and one bit is a parity bit.

IOT Instructions

Mnemonic	Code	Description
DSSF	707001	Skip on disk flag.
DSCC	707021	Clear the disk control and disable the “freeze” status. A “freeze” is caused either by a timing or data track hardware error or an address parity error.
DRAL	707022	OR the contents of Address Pointer 0 (APO) into the AC.

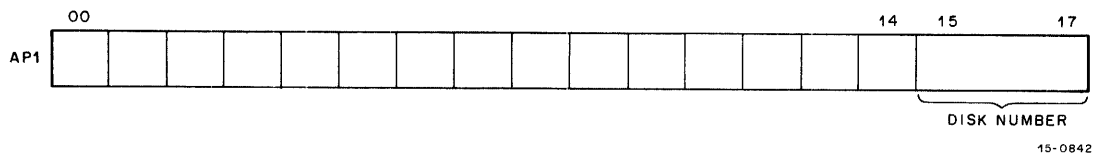


15-0841

DRAH

707062

OR the contents of Address Pointer 1 (AP1) into the AC. Bit 14 signifies a non-existent disk error.



DLAL

707024

Load the contents of the AC into AP0.

DLAH

707064

Load the contents of the AC into AP1.

DSCF

707041

Clear the function register and the interrupt mode.

DSFX

707042

XOR the contents of AC15, 16, 17 into the function register.

DSCN

707044

Execute the condition held in the function register.

Function Register

F0

F1

INT

15

16

17

0

0

X

NO EFFECT

0

1

X

READ

1

0

X

WRITE

1

1

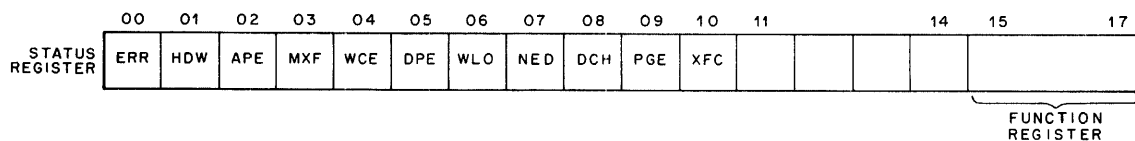
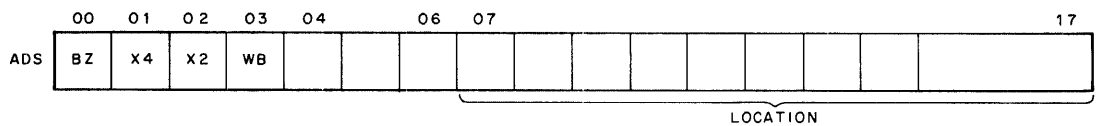
X

WRITE CHECK

DLOK

707202

OR the disk segment address (ADS) register into the AC.



DSCD

707242

Clear the Status Register and Disk Flag.

DSRS

707262

OR the Status Register with the AC.

Specifications

Storage Capacity	262,144 18-bit words expandable to 2,097,152 words	
Addressing Means	Disk unit, track, and word. Single word addressability is provided.	
API Address	63 ₈	
API Priority	1	
Transfer Means	XVM multi-cycle block transfer facility	
Average Access Time	60 Hz Power	50 Hz Power
Minimum Access Time	16.7 ms	20.0 ms
Worst-Case Access Time	250 μ s	250 μ s
Word Transfer Rate	33.3 ms	40.0 ms
	@ 16 μ s/word	61.8 kc 50 kc
	@ 32 μ s/word	31.2 kc 25 kc
	@ 64 μ s/word	15.6 kc 12.5 kc

Power Requirements

Input Frequency	50 Hz/60 Hz $\pm$ 3 Hz
Power Dissipation	1.2 kW
Input Voltage	

Environmental

Temperature Range	18°–35° C (65°–90° F)
Humidity Range	10–55% without condensation

Mechanical

Mounting	Controller and first two disks mount in H950 cabinet

RP15 DISK PACK CONTROLLER

The RP15 interfaces bulk storage disks to the XVM System. Currently there are two versions of disk drive; RPR02 and the RP03. The former, when fitted with an RP02P removable disk pack, will provide the XVM System with 10.24M 18-bit words of storage. The RP03 is a double-density version of the RPR02 and can, therefore, store 20.48M 18-bit words on one disk pack. The total system capacity, with eight RPR02s would be 81.92M words, and with eight RP03s, 163.84M words (that is, 163.84 million words).

The total capacity of the RPR02 Disk Pack is 232,000,000 bits, which is equivalent to 12,900,000 18-bit words. In actual practice, the two outside surfaces are not used; on all surfaces, tracks 200, 201, and 202 are reserved for maintenance. When these conditions are recognized, along with the data required for two synchronization areas, word and longitudinal parity, and a header word for each sector, the relative characteristics yield a total data word capacity of 10,240,000 18-bit words.

In the RPR02, each disk contains 203 cylinders (406 in the RP03). Movable heads, connected to a common positioning actuator, access one cylinder at a time. Track-to-track, average, and maximum positioning times are 20, 50, and 80 ms, respectively. Rotation speed is 2400 rpm (or a rotational time of 25 ms), providing average and maximum latency times of 12.5 and 25 ms, respectively. Data are recorded by a double frequency, non-return-to-zero technique. Data are formatted into 128 36-bit word sectors that are individually addressable; each word provides storage space for two 18-bit words.

The drive has 20 read/write heads that record data at 2.5M bps. Each track contains 10 sectors. Word transfer rate is 14.8 μ s for each 36-bit word or 7.4 μ s for each 18-bit XVM Processor word.

IOT Instructions

Mnemonic	Code	Description
DPSN	706421	Skip the following instruction if FORMAT/NORMAL switch is in NORMAL position.
DPOA	706422	OR the Cylinder, Head, and Sector Address registers into the AC.
DPRA	706432	Read the Cylinder, Head, and Sector Address registers into the AC.
DPLZ	706424	Load the Accumulator zeros into Status register A and execute bits 0-8 if GO bit is set.
DPOC	706442	OR the Current Address register into the AC.
DPRC	706452	Read the Current Address register into the AC.
DPLO	706444	Load the Accumulator 1s into Status register A and execute bits 0-8 if GO bit is set.
DPCN	706454	Equivalent to a continue command. Clear the AC. execute the Function register.E The FR is unchanged.
DPOW	706462	OR the Word Count register into the AC.

DPRW	706472	Read the Word Count register into the AC.
DPLF	706464	Load Status register A from AC 0–8. Execute the new contents if the GO bit is set.
DPSF	706301	Skip on DISK flag.
DPOSA	706302	OR Status register A into the AC.
DPRSA	706312	Read Status register A into the AC.
DPLA	706304	Load the Address register from AC 00–17.
DPSA	706321	Skip on ATTENTION flag.
DPOSB	706322	OR Status register B into the AC.
DPRSB	706332	Read Status register B into the AC.
DPCS	706324	Clear the Status bits.
DPSJ	706341	Skip the following instruction if the JOB DONE flag is set.
DPOM	706342	OR the Maintenance register into the AC.
DPRM	706352	Read the Maintenance register into AC 0–5. Clear AC 6–17.
DPCA	706344	Load the Current Address register from AC 0–17.
DPSE	706361	Skip the following instruction if an error condition is present.
DPWC	706364	Load the 2's complement of the word count into the Word Count register.
DPED	706401	Execute the maintenance instructions as defined by AC 9–17.
DPLM	706411	Clear the AC and leave Maintenance mode.
DPOU	706402	OR the Selected Unit Cylinder Address register into the AC 10–17.
DPRU	706412	Read the Selected Unit Cylinder Address register into the AC 10–17.
DPCF	706404	Clear the Function register.

Controller**Electrical**

Input Voltage	115/230 Vac, single phase
Input Frequency	47–63 Hz
Power Dissipation	800 W

Environmental

Temperature Range	55°–100° F (13° – 38°C)
Humidity Range	25–95% without condensation

Mechanical

Mounting	Mounted in H950 cabinet
Weight	305 lb (138 kg)

Drive (RP02/RP03)**Electrical**

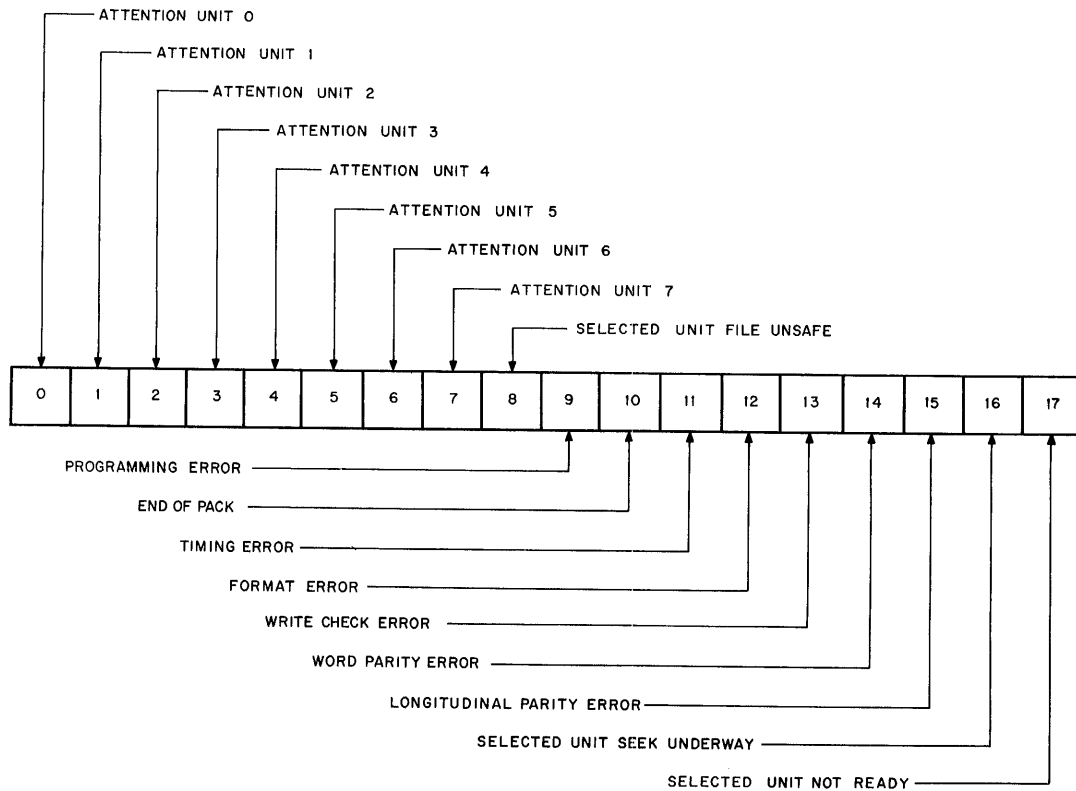
Input Voltage	208/230 Vac $\pm$ 10% of 3 phases
Input Frequency	50/60 Hz $\pm$ 1%
Power Dissipation	1250 W

Environmental

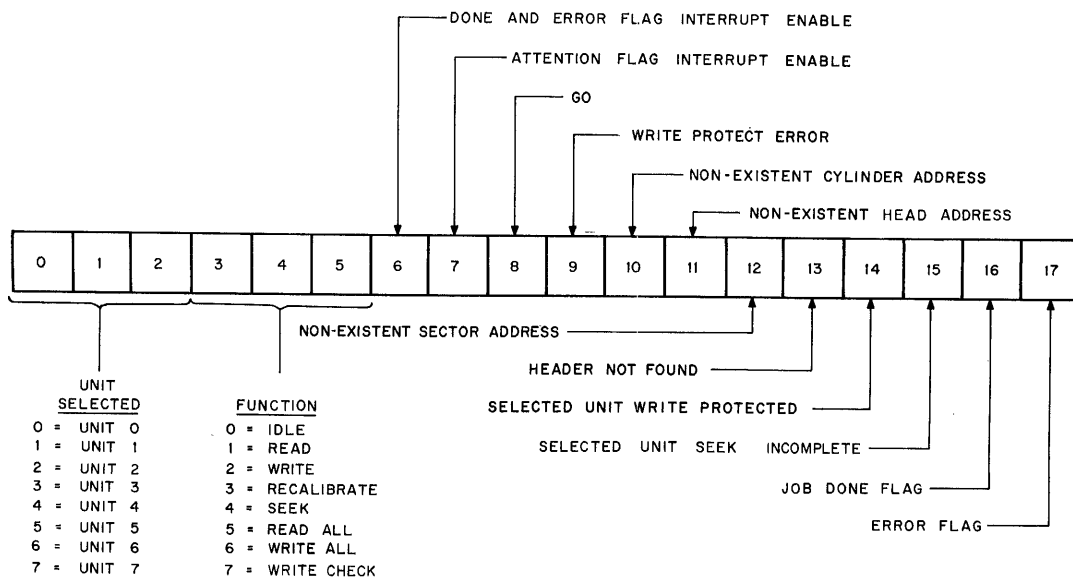
Temperature Range	60°–90° F (16° – 3C)
Humidity Range	8–80%

Mechanical

Dimensions	24 (61 cm) $\times$ 36 (91 cm) $\times$ 40 (102 cm) in.
Weight	400 lb (181 kg)



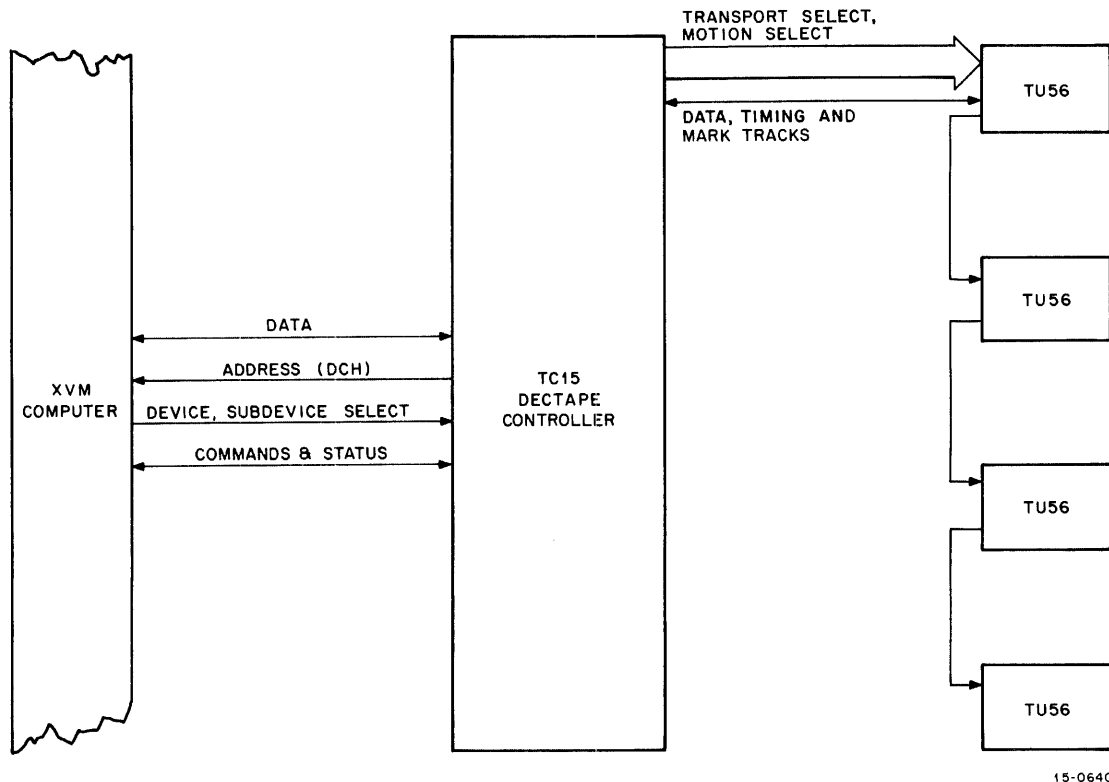
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09-0341

TC15 DECTape CONTROLLER

The DECTape system is a computer peripheral device that stores digital data on 0.75 in. magnetic tape in a three-track parallel/serial format. The tape, called DECTape, is wound on 3-1/2 in. pocket-size reels, which are easy to carry and load. Each reel has a capacity of 3 million bits for 260 ft of tape.



The DECTape device is a fast, convenient, reliable, low-cost input/output data storage facility and updating device. Each DECTape system consists of a controller and from one to four TU56 Dual DECTape Transports. The controller is connected to the computer I/O bus and communicates with the processor for control and status information and with memory through the I/O processor for data information. Each drive is connected to the controller through a parallel bus; both control and data information pass through this bus.

Data Storage Format

The DECTape system stores data in a parallel format; each 18-bit data word is divided into six three-bit bytes which are stored in parallel across three data tracks. The system stores the complete 18-bit word serially along the tape in six three-bit bytes.

DECTape stores data in blocks (or groups), using prerecorded, fixed-position addressing that allows selective updating of tape information; this feature is also used in magnetic disk or drum storage devices. Each data block has its own address and is numbered to provide random accessing. Another DECTape feature is bidirectional operation; i.e., each block can be identified by the computer regardless of the direction in which the tape is moving. Consequently, the tape can be read from or written on in either direction. This feature provides the programmer with a relatively fast search time, because the tape does not have to be rewound before a block can be found, and thus the programmer can begin to write at either end of the block as soon as the correct block number is found. It is important that the programmer read and write data in the same direction, however, or be prepared to unscramble it in the computer.

The number of words in each block (block length) is predetermined when the tape is formatted. A standard block consists of 256 18-bit words. Tape formatting involves the writing of a timing track (which furnishes timing pulses to the controller) and the writing of a mark track (which contains codes to inform the controller where the tape is within a given block). Special timing and mark tracks are contained on the tape for this purpose. Formatting also involves numbering the data blocks and also specifying the length of the data blocks. When the block lengths are established by the programmer, they cannot be changed without destroying the data on the tape.

IOT Instructions

Mnemonic	Code	Description
DTCA	707541	Clear Status register A.
DTRA	707552	Read Status register A.
DTXA	707544	XOR Status register A.
DTLA	707545	Load Status register A.
DTEF	707561	Skip on Error flag.
DTRB	707572	Read Status B.
DTDF	707601	Skip on DECTape flag.

Data Channel Address

Word Count	30
Current Address	31
API Address	44
API Priority	1

Electrical

Input Voltage	115/230 Vac, single phase
Input Frequency	50/60 $\pm$ 2 Hz
Power Dissipation	1600 W

Environmental

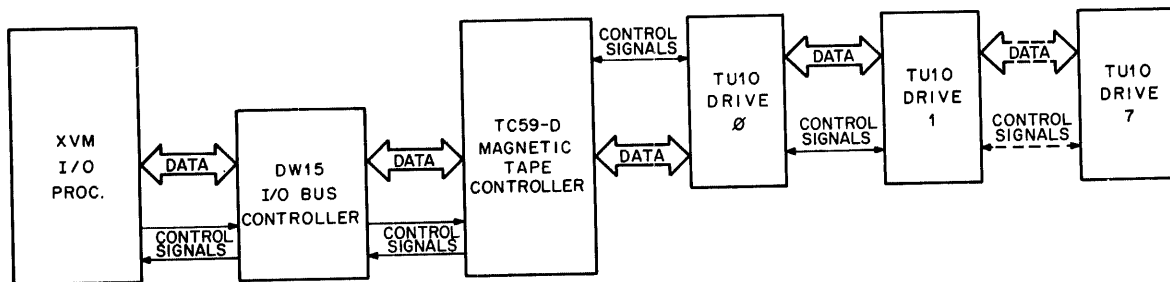
Temperature Range	65°–90° F (18° – 32°C)
Humidity Range	10–55% without condensation

Mechanical

Mounting	Controller and first three TU56 Drives are mounted in an H950 cabinet
Weight	300 lb (136 kg)

TC59-D MAGNETIC-TAPE CONTROLLER

The TC59 consists of tape control logic, which, under the direction of the XVM, controls the operation of up to eight magnetic tape transport units. The TC59 operates under program control to transfer data between core memory and the selected tape transport. To transfer data to or from core memory, the TC59 uses the data channel facility of the processor, the data channel WC (word count) register specifies the record length (number of words), and the CA (current address) register specifies the starting core memory address of the data transfer.



15-0840

The TC59 functions in either 7-track operation or 800 bpi 9-track operation; either 200, 556, or 800 bpi density modes are selectable in 7-track operation. It can operate in either Binary or BCD Parity mode. For writing on tape, the 18-bit data words are transferred from core memory to the data buffer in the tape control logic. The data buffer logic supplies the character to the tape transport write logic as three 7-bit (6-bit character plus parity bit) characters for 7-track operation or two 9-bit characters for a 9-track operation. For reading, the sequence is reversed, information is read from tape as characters and sent to the data buffer. When a complete (18-bit) word has been assembled in the data buffer, a data-channel break (word transfer) is initiated to transfer the data buffer word into core memory.

The TC59 controls the operation of a maximum of eight magnetic tape transports and uses the processor data channel facility to transfer data between system core memory and magnetic tape. The data transfers are controlled by the memory-resident word counter (WC) and current address (CA) registers associated with the assigned data channel. The TC59 is assigned memory location 32₈ and 33₈ for WC and CA, respectively. The CA is incremented before each data transfer; therefore, the initial contents should be set to the desired initial address minus one. The WC is also incremented before each transfer and must be set to the 2's complement of the desired number of data transfers. In this way, the word transfer that causes the word count overflow (WC = 0) is the last transfer to take place.

IOT Instructions

Mnemonic	Code	Description
MTSF	707341	Skip on error flag or magnetic tape flag.
MTCR	707321	Skip on tape control ready (TCR).
MTTR	707301	Skip on tape transport ready (TUR).
MTAF	707322	Clear the Status and Command registers, and the EF and MTF, if Ready. If Busy, clear MTF and EF flags only.

MTCM	707324	Inclusively OR the contents of the AC bits 0 through 5, 9 through 11 into the Command register; JAM transfer bits 6, 7, 8.
MTLC	707326	Load the contents of AC bits 0 through 11 into the Command register.
-	707342	OR the Status register into AC 00-11.
MTRS	707352	Read the Status register into AC 00-16.
-	707302	OR the Command register AC 0-11.
MTRC	707312	Read the Command register to AC 00-11.
MTGO	707304	Set "go" bit to execute, if legal.

Specifications

Recording Mode	NRZ1, industry compatible
Magnetic Head	Dual gap, read after write
Data Transfer Method	Multi-cycle data channel facility
Tape Handling Method	Direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer chambers with constant tape winding tension. There are no dancer arms to cause non-uniform tape tension and stretching
BOT, EOT Detection	Photoelectric sensing of reflective strip, industry compatible
Skew Control	Deskewing electronics included in TU10 Transport to eliminate static skew
Write Protection	Write protect ring sensing on TU10 Transport
Data Checking Features	Read-after-write parity checking of characters; Longitudinal Redundancy Check (7- and 9-channel); Cyclic Redundancy Check (9-channel)
Packing Density	7-channel: 800, 556, and 200 bpi; selectable under program control. 9-channel: 800 bpi
Maximum Transfer Rate	36,000 characters per second
Rewind Speed	150 ips
Interrecord Gap	Will read tape with gap of 0.48 in. or more; will write tape with gap of 0.52 in. or more (compatible with industry standard)

Tape 0.5 in. wide, industry standard

Tape Speed 45 ips, reading and writing

Word Count **Data Channel Addresses**
32

Current Address 33

API Address 45

API Priority 1

Controller

TU10

Electrical

Input Voltage	115/230 Vac $\pm$ 10%
Input Frequency	50/60 $\pm$ 2 Hz Single phase
Power Dissipation	500 W 1000 W

Environmental

Temperature Range	7°–35° C (45°–95° F)
Humidity Range	20–75% without condensation

Mechanical

Mounting	Drive and Controller normally mount in separate H950 cabinets but may be combined in the same cabinet.	
Weight	300 lb (136 kg)	250 lb (113 kg)

VP15 POINT-PLOT DISPLAY CONTROLLER

The VP15 Controller is the foundation of the point plotting family. It serves as an interface between the XVM and the display device. The VP15 converts program-generated digital commands (IOT instructions) to analog voltages applicable to the display device. However, because the instructions for all displays are not exclusive, only one model, VP15, is permitted.

At present, four VP15 models are available:

1. VP15-A – Controller plus VT01-A storage tube
2. VP15-B – Controller plus VR01-A refresh tube
3. VP15-C – Controller plus VR14 refresh scope
4. VP15-D – Controller plus VR20, two-color refresh tube

VP15-A

The VP15-A is designed to meet the needs of those with a very large data base to be displayed – textual data or static pictures. It is ideal for use when one cannot afford the central processor time required for picture refreshing. There are two program-selectable modes of operation – Store and Non-store mode. Points are drawn on a 1024×1024 raster matrix. Those plotted in Non-store mode must be refreshed 30 times/second; points plotted in Store mode remain visible for 15 minutes (although hardware considerations require pressing the VIEW button every 90 seconds). Modes may be intermixed.

Erasing may be done either under program control or by pressing the ERASE button on the display. Immediate point deletion is only possible in Refresh mode. In Store mode, the entire picture must be erased and redrawn.

The VP15-A is a table-top mounted device which can be remoted up to 15 feet from the computer.

VP15-A IOT Instructions

Mnemonic	Code	Description
CXB	700502	Clear x-coordinate buffer
CYB	700602	Clear y-coordinate buffer
LXB	700504	Load x-coordinate buffer from AC8-17
LYB	700604	Load y-coordinate buffer from AC8-17
EST	700724	Erase storage tube
SDDF	700521	Skip on display Done flag
CDDF	700722	Clear display Done flag
LXBD	700564	Load x-coordinate buffer and display the point specified by XB and YB (Store mode)
LYBD	700664	Load the y-coordinate buffer and display the point specified by XB and YB (Non-store mode)
LXDNS	700544	Load the x-coordinate buffer and display the point specified by XB and YB (Non-store mode)

LYDNS

700644

Load the y-coordinate buffer and display the point specified by XB and YB (Non-store mode)

VP15-A Specifications

Point Plotting Rate	100 μ s/point in Store mode 82 μ s/point in Refresh mode
Display Area	8-1/4 in. $\times$ 6-3/8 in. (21 cm $\times$ 16.3 cm)
Resolution (raster units)	1024 $\times$ 1024
Refresh Rate	30 Hz
Phosphor Type	Similar to P1
Mounting	Table-top
Width	11-5/8 in. (29.5 cm)
Height	11-7/8 in. (30.1 cm)
Depth	22-3/8 in. (56.8 cm)
Weight	51 lb (23.1 kg)
Temperature Range	+65° F to +80° F +18°C to +27.5° C
Humidity Range	40% to 55% without condensation
Power Requirements	120/240 Vac 60 Hz 210/230 Vac 50 Hz
Power Dissipation	250 W

Controller

Mounting	Mounted in BA15 logic assembly

VP15-B, VP15-BL

In environments and applications where low cost is the most important criterion, the VP15-B X-Y Display System can be used to full advantage.

The system uses a rack-mounted Tektronix Type RM503 X-Y Oscilloscope. Points are plotted on a 1024 $\times$ 1024 raster matrix on the 8 cm $\times$ 10 cm display area and should be refreshed 30 times/second. Operator controls on the RM503 front panel provide simple user manipulation of the display presentation – expansion, compression, centering, shifting – without changing program parameters.

Four levels of intensity are provided, and the light pen can be optionally specified, forming the VP15-BL X-Y Oscilloscope display. Both displays are rack-mounted.

VP15-B, VP15-BL IOT Instructions

Mnemonic	Code	Description
DXL	700504	Load the x-coordinate buffer from AC8-17.
DXS	700544	Load the x-coordinate buffer and display the point specified by XB and YB.
DYL	700604	Load the y-coordinate buffer from AC8-17.
DYS	700644	Load the y-coordinate buffer and display the point specified by XB and YB.
DXC	700502	Clear the x-coordinate buffer.

DYC	700602	Clear the y-coordinate buffer.
DLB	700704	Load the Brightness register from bits 16-17 of the AC.

NOTE

This instruction clears the Display flag associated with the light pen.

DSF	700501	Skip if Display (light pen) flag is a 1.
DCF	700702	Clear Display (light pen) flag.

VP15-B, VP15-BL Specifications

Point Plotting Rate	12 μ s/point
Display Area	3.1 in. $\times$ 3.9 in. (8 cm $\times$ 10 cm)
Resolution (raster units)	1024 $\times$ 1024
Refresh Rate	30 Hz

Terminal Specifications

Phosphor Type	P2
Mounting	Option cabinet not supplied
Physical	
Width	19 in. (48.3 cm)
Height	7 in. (17.8 cm)
Depth	17 in. (43.2 cm)
Weight	28 lb (12.7 kg)
Power Requirements	120/240 Vac 60 Hz
	210/230 Vac 50 Hz
Power Dissipation	120 W

VP15-C, VP15-CL

This system uses a DEC Type VR14 X-Y Display. Points are plotted on a 1024 $\times$ 1024 raster matrix and can be refreshed 30 or 60 times/second. Useful screen dimensions of 6-3/4 $\times$ 9 in. and an impressive physical appearance make the VP15-C an attractive and useful terminal. The display is available in rack-mounted and table-top configurations. Various optical filters can be specified to suit particular applications. Modular construction provides maximum flexibility and increased maintainability. The VP15-C is an ideal display terminal for environments where security is of a paramount importance. The only front panel control that is readily accessible is the ON/OFF/BRIGHTNESS control – the others are screwdriver adjustments. The light pen can be optionally specified, forming the VP15-CL X-Y Display System.

VP15-C, VP15-CL IOT Instructions

The IOT instructions for the VP15-C are identical to those for the VP15-B.

VP15-C, VP15-CL Specifications

Point Plotting Rate	20-25 μ s/point
Display Area	6-3/4 $\times$ 9 in. (17.1 cm $\times$ 22.8 cm)
Resolution (raster units)	1024 $\times$ 1024
Refresh Rate	30 or 60 Hz

Terminal Specifications

Phosphor Type	P31 or P7
Mounting	Option cabinet not supplied
Physical	
Width	19 in. (48.3 cm)
Height	10-1/2 in. (26.7 cm)
Depth	17 in. (43.2 cm)
Weight	53 lb (24 kg)
Power Requirements	110/240 Vac 60 Hz 210/230 Vac 50 Hz
Power Dissipation	150 W

VP15-D

The VP15-D is a completely self-contained two-color CRT display that provides a $6\frac{3}{4} \times 9$ in. viewing area in a compact 19 in. package. The dual-energy phosphor screen presents information as either a red or green trace. The VP15-D requires only analog X- and Y-position information and an intensity pulse to generate sharp, bright point-plot displays. Except for the high-voltage power supply and the CRT, the unit is composed of solid-state circuits and utilizes high-speed magnetic deflection to enhance brightness and resolution. The inputs for the X- and Y-deflection may be balanced or single-ended, bipolar or offset, and positive- or negative-going without any modification to the VP15-D. The intensity pulse may be time-multiplexed or gated by a separate input to allow the screen to be time-shared between two inputs; TTL-compatible signals are required. The VP15-D is available in a standard 19-inch rack-mounted unit or in a table-top version.

VP15-D IOT Instructions

The instructions for the VP15-D are identical to those of the VP15-C, except when the DLB instruction is being used, bit 15 denotes color. If bit 15 is a 0, the color is red; if bit 15 is a 1, the color is green.

VP15-D Specifications

Color Registration	< 25 mils within a central 4 in. diameter circle; < 60 mils elsewhere on the screen (distance between like-addressed points in red and green)
Spot Size	20 mils inside the usable screen area at a brightness of 30 fl (green); 30 mils at 10 fl (red)
Color Mode Maximum Setup Time	1600 μ s for green mode; 300 μ s for red mode
Deflection	Full screen deflection and settling time to within ± 1 spot diameter, <20 μ s for green and <16 μ s for red
Power Requirements	
Voltage	115 V $\pm$ 10%; 230 V $\pm$ 10%
Frequency	50-60 Hz
Power	500 W
API Address	54
API Priority	2

High Voltage	High-voltage switches between approximately 6 kV and 10 kV for red and green modes, respectively.
Overload Protection	Unit is protected against fan failure or air blockage by thermal cutouts. Power supply and amplifiers are current limited. Phosphor protection is provided against fault conditions.
Temperature Range	0°C to 45°C (operating) (32° – 113°F)
Input Specifications	• Inputs are differential • Differential input impedance, 5K minimum • Input sensitivity, 500 mV/in. maximum (changeable with resistors to 200 mV/in.) • Maximum operating input, $\pm 6V$ (maximum operating input is the sum of the Common mode and the differential input) • Input offset not to exceed $\pm 1/2$ peak-to-peak input signal • Z Input, TTL compatible, +2.4 V to 0 transition will cause CRT to unblank for 1 μs in green mode, 5 μs in red • Z Direct, AC coupled, 45 V; 10 μs pulse will unblank CRT
Color Bit	Single bit selects green (high) or red (low)
Dimensions	10-1/2 in.H $\times$ 19 in.W $\times$ 17 in.D (26.7 cm $\times$ 48.3 cm $\times$ 43.2 cm)
Weight	80 lb (36.2 kg)
Repeatability	$< \pm 1$ spot diameter (repeatability is the deviation from the nominal location of any given spot)

VT50 DECSCOPE VIDEO TERMINAL

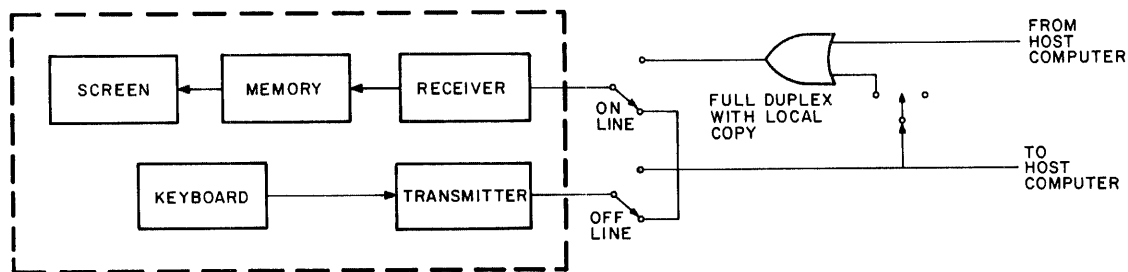
The VT50 DECscope is an on-line graphics terminal, and gives fast interaction at a price comparable with that of 10 cps teletypewriters. It has a range of operating modes and transmission speeds that may be selected by switches, and it is compatible with any device or system that uses asynchronous transmission of ASCII codes.

Two control dials let the programmer select transmission rates from 75 to 9600 baud (75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud). These control dials can be set so the VT50 transmits data at one speed and receives data at another speed.

Up to 12 lines of information can be displayed at one time. When the bottom line on the screen is displayed, and the cursor is directed to move to the next line, the top line automatically “scrolls” off the screen to allow space for the new line. When receiving data at high baud rates, scrolling can occur so rapidly that a visual inspection of screen information is impossible. For example, at 9600 baud, the VT50 can receive 960 characters per second – enough to fill the whole screen. A simple command directs the VT50 to give the operator or host computer control over scrolling so the display can be updated on a line-by-line or screen-by-screen basis.

Movable Cursor

The cursor can be moved from the keyboard or, under program control, to the home position (top left corner of the screen), right one position, left one position, up one line, and down one line.



15-0825

The VT50 has tabs that are fixed at every eight spaces, as well as the ability to erase characters from the cursor to the end of a line and from the cursor to the end of the screen.

Extended Functions

Programmer-assigned functions can be written into system software and accessed by using the VT50's ESC key. (Commands created in this way are called Escape Sequences.) The host computer can be programmed so that the receipt of ESC 1 implements one routine, ESC 2 another, and so on.

A means of identifying unique Escape Sequence functions is incorporated into the VT50's architecture. Labels above the top ten keys direct the operator to the proper key for each sequence. Labels can be easily changed to accommodate new functions and applications.

A special self-test feature is built into the VT50 – it permits you to check the circuitry prior to any network installation. No special interfacing is necessary. The VT50 can be wired directly to a computer or to other terminals via its standard 20 mA current loop interface. It can be installed as an active device, a passive device, or active during transmission and passive upon reception. EIA or other interfacing for use with modems, data phones, or acoustic couplers is optional.

Minimal Maintenance

Few mechanical parts (the keyboard and audio/tactile response mechanism) give the VT50 built-in reliability, lowering the cost of ownership. Extensive keyboard testing – for over 100,000,000 failure-free keystrokes – proves switch reliability.

Specifications

Dimensions	Height: 360 mm (14.1 in.) Width: 530 mm (20.9 in.) Depth: 690 mm (27.2 in.)
Weight	19.4 kg (43 lb)

Environmental

Temperature Range	10° C to 40° C (50° F to 104° F)
Humidity Range	10% to 90% with maximum wet bulb 28° C (82° F) and minimum dew point 2° C (36° F)

Electrical

Input Voltage	230 V: 210–250 V @ 50 Hz $\pm$ 1 Hz 115 V: 100–126 V @ 60 Hz $\pm$ 1 Hz
Power Consumption	110 W

Display

Format	12 lines $\times$ 80 characters
Character Matrix	5 $\times$ 7
Character Size	2.7 mm $\times$ 5.0 mm (0.11 in. $\times$ 0.20 in.)
Screen Size	220 mm $\times$ 110 mm (8.7 in. $\times$ 4.3 in.)
Transmission Rates	Switch-selectable Full Duplex: 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud Full Duplex with Local Copy: 110, 600, 1200, 2400, 4800, and 9600 baud
Keyboard	• Character set: 64 ASCII upper case, alpha, numeric, and punctuation characters • Typewriter format keyboard • Audio/tactile response mechanism for fast operator feedback • Three-key rollover feature to minimize typing errors • BREAK key included for half duplex software
Terminal Modes	Off-line mode On-line mode: Full duplex or full duplex with local copy
Page Overflow	Upward scroll
Parity	Even or mark (no parity) selectable
Cursor	Control: Up or down one line, right or left one position, home, erase from cursor to end of line, erase from cursor to end of screen
Communications	Type: non-destructive, underscore
Transmission Code	20 mA current loop standard; EIA interface optional
Operator Controls	USASCII extended through Escape Sequences Power on/off, intensity control, baud rate switches, full duplex or full duplex with local copy switch

VW01-B WRITING TABLET

The writing tablet option is an acoustical X-Y digitizer connected directly to the controller. Its horizontal surface provides free arm movement.

The VW01 operates in one of two modes: Single Point or Data Input. In the Single Point mode, a single spark is generated each time the pen is pressed against the writing surface. This operation is used when the operator desires to plot specific points in the X- or Y- axis.

In the Data Input mode, the spark pen produces a continuous series of sparks at a constant rate (normally 200 Hz). This mode allows the user to draw continuous lines, circles, curves, etc. The dual mode capability of the VW01 enables the user to perform a myriad of graphic analytical tasks quickly and accurately.

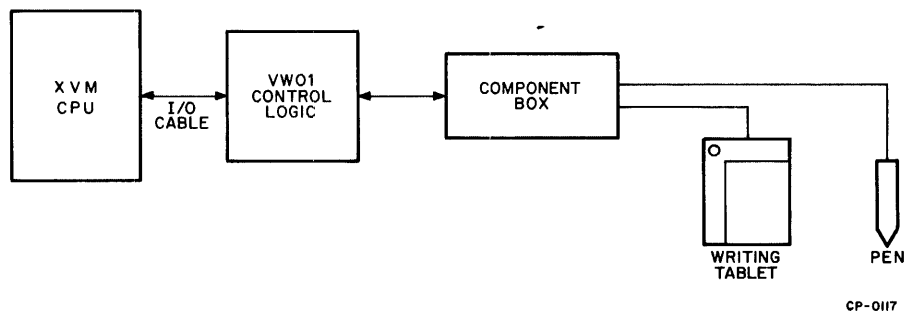
Both right- and left-handed users are catered to by this device by physically rotating the table 90°. A switch rotates the signals electrically by 90°.

IOT Instructions

Mnemonic	Code	Description
WTSC	703224	Set Tablet Controls
WTRX	703222	Read X
WTRY	703242	Read Y
WTRS	703262	Read Status
WTCD	703241	Clear DATA READY flag
WTCP	703221	Clear PEN DATA flag
WTSK	703261	Writing Table Skip
WTSE	703264	Select Tablet
CAF	703302	Clear All Flags
IORS	700314	Input/Output Read Status

Maintenance IOT*

WTMN	703244	Clear Set XY



*The IORS IOT instruction will display the VW01 Writing Tablet interrupt status in accumulator bit 05.

Specifications

Digital Resolution
Graphic Resolution
Reproducibility
Drift

10-bit resolution in both X- and Y-axes.
1000 × 1000 line pairs; 90 lines per in.
One (least significant) bit in 1000, in both X- and Y-axes.

Constant Temperature
4.4° to 32° C

With the spark pen stationary, the X- and Y-registers will not vary more than ± 1 bit of 1024.

+40° to 90° F

With the spark pen stationary, the X- and Y-registers will vary by a group undefined or illegal by a group undefined or illegal by a group undefined or illegal 6.2 bits per thousand per degree change centigrade.

With the spark pen stationary, the X- and Y-registers will vary by a group undefined or illegal by a group undefined or illegal by a group undefined or illegal 6.14 bits per thousand per degree change Fahrenheit.

Data Rate

SCAN Single Tablet

200 X-Y coordinate pairs per second. The data rate can be decreased to 1 X-Y coordinate pair per second.

SCAN Multiple Tablet

100 X-Y coordinate pairs per second per tablet; used only with VW01MX Multiplex option.

Single Point

Determined by user's manual activation of the spark pen microswitch.

Multiplex Latency

With the VW01MX Multiplex option, the interval from each writing tablet Data Ready flag to the time the next writing tablet is enabled is 1.4 ms.

API Address

73

API Priority

2

Controller

Mounting

Mounted in VT15 controller cabinet

Electrical

Input Voltage

115/230 Vac $\pm 10\%$, single phase

Input Frequency

47–63 Hz

Power Dissipation

500 W

Environmental

Temperature Range

45°–90° F (7° – 32°C)

Humidity Range

20–50%

XY15 X-Y PLOTTER CONTROLLER

The XY15 Plotter Controller interfaces two types of CALCOMP Plotters to the XVM I/O bus – the CALCOMP types 563 and 565.

The plotters, whose specifications follow, may be purchased directly from DIGITAL for inclusion in the system. Users may also purchase these plotters, or their equivalents, directly from the manufacturer for use with the XY15.

IOT Instructions

Mnemonic	Code	Description
PLSF	702401	Skip if plotter flag is a 1.
PLCF	702402	Clear plotter flag.
PLPU	702404	Plotter pen up.
PLPR	702421	Plotter pen right.
PLDU	702422	Plotter drum (paper) upward.
PLDD	702424	Plotter drum (paper) downward.
PLPL	702441	Plotter pen left.
PLUD	702442	Plotter drum (paper) upward.
PLPD	702444	Plotter pen down.

CALCOMP-563 Specifications

(Manufactured by California Computer Products, Inc.).

Mechanical

Dimensions	9.8 in. H, 39.5 in. W, 14.7 in. D
Type	Drum, tabletop

Electrical

Input Power	105-125 Vac, 50/60 Hz
Current	1.5 A

Operational

Plot Size	Y-axis = 28.55 in. X-axis = 120 ft
Stepping Increments	0.01 in. and 0.005 in.
Stepping Speed	200 and 300 steps/sec
API Address	65
API Priority	2

CALCOMP-565 Specifications

(Manufactured by California Computer Products, Inc.).

Mechanical

Dimensions	9.8 in. H, 18 in. W, 14.7 in. D
Type	Drum, tabletop

Electrical

Input Power	105-125 Vac, 50/60 Hz
Current	1.5 A

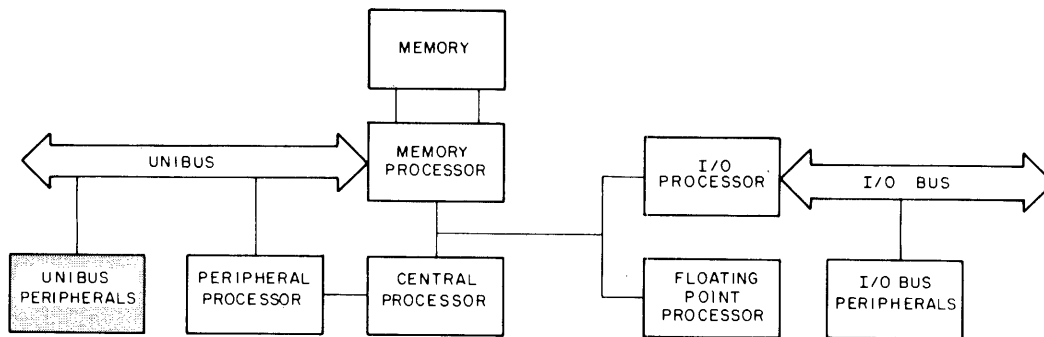
Operational

Plot Size	Y-axis = 11 in. X-axis = 120 ft
Stepping Increments	0.01 in. and 0.005 in.
Stepping Speed	300 steps/sec
API Address	65
API Priority	2

Controller**Mechanical**

Mounting	5.25 in. logic assembly mounts in negative bus cabinet

Section 2. UNIBUS PERIPHERALS



15-0854

Unibus peripherals are PDP-11 type system components which are controlled by the XVM Peripheral Processor.

One of the many advantages of the Unichannel system is that large data sets destined for slow devices (e.g., printer plotter, etc.) can be transferred out of the XVM memory and onto the Unichannel disk. Once this process is completed, the XVM Main Memory is free again, and the files can be output slowly to the devices without delaying the main processor.

A brief discussion of Unibus peripherals follows. The devices included are those that are currently supported by XVM software:

CR11	Card Reader Controller
DP11	Synchronous Interface
LP11	Line Printer Controller
LV11	Printer-Plotter
RK11-E	DECpack Controller
XY11	Plotter Controller
XY311	Plotting System Controller

CR11 CARD READER CONTROLLER

The CR11 Card Reader reads EIA standard 80-column punched data cards at 300 cards per minute.

The punched-card reader uses a vacuum picker that works with riffle air to make card wear insignificant, card jam virtually impossible, and provide extreme tolerance to damaged cards. The riffling action separates the cards in the input hopper to prevent sticking. The picker uses a strong vacuum to grasp the bottom card and deliver it to the read station on demand. The picker and associated throat block prevent the unit from multiple picking to the extent that taped or stapled cards are not allowed to enter the card track. In such cases, the reader stops with pick check alarm. The operator can then separate the cards and enter them into the input hopper for normal reading. The card track is very short, so that only one card is in motion at a time. The combination of tolerance to damaged cards, gentle card handling, and short card track provide virtually jam-proof operation for the CR11.

Operation

Cards are read by column, beginning with Column 1. A select instruction starts the card moving past the read station. Once a card is in motion, all 80 columns are read. Column information is read in one of two program-selected modes: Compressed or Image. In the Compressed mode, the 12 information bits in one column are automatically decoded and transferred into the least significant half of the Card Reader Data Buffer (CRB2) as 8-bit compressed code. In the Image mode, the 12 bits of a column are transferred directly into the CRB1 so that Zone 9 is transferred into the CRB00 and Zone 12 is transferred into CRB11. A punched hole is interpreted as binary 1, and the absence of a hole as binary 0.

CR11 Registers

Mnemonic	Code	Description
CRSR	777160	Reader Status Register
CRB1	777162	Data Buffer Register 1 (normal)
CRB2	777164	Data Buffer Register 2 (encoded)

Specifications

Reading Rate (cpm)	300
Input Hopper	Capacity (cards*)550 – 600
	Output Hopper
Capacity (cards*)	550 – 600
Size Envelope	11 in. H × 19 in. W × 14 in. D (28 cm H × 48 cm W × 36 cm D)
Weight (max.)	70 lb (32 kg)
Head Dissipation	1360 Btu/hour

Environmental

Temperature Range	+10° to +50° C (50° – 122°F)
	Humidity Range 10 to 90%, without condensation

Electrical

Input Power	115 Vac, ±10%, 60 Hz 230 Vac, ±10%, 50 Hz Single Phase
Power Consumption	950 VA starting, 400 VA running
Interrupt Priority	BR6 (may be changed by jumper)
Interrupt Vector Address	Location 230
Mounting	Occupies one SPC slot.

*Depending on card stock

DP11 SYNCHRONOUS INTERFACE

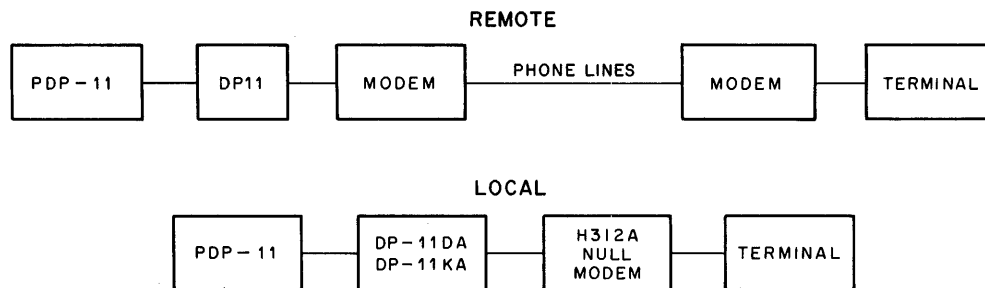
The DP11 is a fully character-buffered synchronous serial line interface capable of two-way simultaneous communications. The DP11 translates between serial data and parallel data. Output characters are transferred in parallel from the computer to a Buffer register where they are serially shifted to the communication line. Input characters from the modem are shifted into a register, transferred to a Buffer register, and made available to the PDP-11 on an interrupt basis.

Both the receiver and the transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts.

The clocking necessary to serialize the data is normally provided by the associated high-speed synchronous modem. Alternately, the internal clocking option can be used for local terminals when no external clocking is available.

The DP11 provides a double-buffered program interrupt interface between a PDP-11 and a serial synchronous line. This interface allows the PDP-11 to be used in remote batch and remote concentrator applications. With the DP11, a PDP-11 can also be used as a front end synchronous line controller to handle remote and local synchronous terminals.

The DP11 interface offers flexibility. It handles a wide variety of terminals and line disciplines (i.e., line control procedures and error control techniques). A programmer can vary sync character, character size, and modem control leads. Automatic sync character stripping and automatic idling are also program selectable. While idling, the DP11 transmits the contents of the sync buffer.



15-0839

The DP11 design provides individual interrupt vectors and hardware interrupt priority assignments for the transmitter and receiver. Interrupt priority is jumper-selectable. This feature, coupled with the automatic transmit idle capability, enables dynamic system adjustment to peak message activity. For example, the programmer can temporarily ignore the transmitter if receive activity is high.

Because the PDP-11's Unibus serves as a multiplexer, multiple synchronous lines can be added to a PDP-11. One PDP-11 system unit mounting space is used for each independent synchronous line interface unit.

DP11 Registers

Mnemonic	Code	Description
DPRS	174770	Receiver Status Register
DPRB	174772	Receiver Buffer
DPSR	174773	Sync Register
DP	174774	Transmitter Control and Status Register
DPTB	174776	Transmitter Buffer

Specifications

Type	Double-buffered transmit and receive
Operating Mode	Full or half duplex selected under software control
Maximum Data Rate	50,000 bits per second (9600 bits per second with the DP11-DA)
Data Format	Character size is variable under program control to 6, 7, or 8 bits (10, 11, or 12 bits optional)
Clocking	Synchronous clock from the modem (internal clock optional)
Sync Character	Programmable
Sync Detection	Two successive sync characters are required to activate the unit
Order of Bit Transmission	Low order bit first
Parity	Parity check bit provided on incoming characters
Power Required	2.5 A of +5 V
Temperature Range	0-40° C (32° - 104° F)
Humidity Range	20 - 90% without condensation

Modem Compatibility (Typical)

Type	Speed (Baud)	Communications Channel
Bell 201A	2000	(Direct distance dialing network - Type 3002 (C2))
Bell 201B	2400	(Leased line only - Type 3002 (C2))
Bell 303B	19,200	(Leased line only - half group (6 voice-band lines))
Bell 303C	50,000	(Leased line only - group (12 voice-band lines))

Data and Modem Control Signals

All leads of Bell 201 and 303 modems are brought into the unit. All leads are EIA RS-232-C and CCITT compatible for the 201 modem. All leads for the 300 Series are Current mode as defined in the appropriate reference manual.

Bus Load

One line unit represents one unit load to the PDP-11 Unibus. The Unibus provides 18 unit loads. To add more than 18 unit loads, a bus extender (DB11-A) must be used.

Physical Connection

For 201 modems, 25-foot cable with RS-232-C compatible 25-pin male connector. For 303 modems, 25-foot coaxial cable with appropriate connector.

Mounting

Backplane is a four-slot system unit.

LP11 LINE PRINTER CONTROLLER

The LP11 is the high-speed printer available for the Peripheral Processor. Characters are loaded into a printer memory serially until either a control character occurs or a count of 132 is reached, then the entire line is printed.

Specifications

Main Specifications

Number of columns	132
Number of characters	64 or 96
Printing speed	300 lines/min (230 lines/min with 96 char.)
Slew speed	20 inches/sec
Line advance time	45 ms

Printing

Method	Drum
Size of Characters	0.095 in. H × 0.065 in. W
Vertical Spacing	6 or 8 lines/inch (switch selectable)
Horizontal Spacing	10 char/inch

Character Set

64 Characters	Upper-case letters, numbers, symbols
96 Characters	Upper- and lower-case letters, numbers, symbols

Paper

Type	Standard fanfold, edge-punched, 11 switch-selectable positions between folds (3 to 14 inches), 15 lb bond for single copy, 12 lb bond with single shot carbon
Number of copies	1 to 6
Width	4 to 16-3/4 inches
Paper feed	One pair of pin-feed tractors for 1/2-inch hole center, edge-punched paper

Ribbon

Type	Inked roll
Width	15 inches
Length	240 feet
Thickness	0.004 inches

Register Addresses

Printer status (LPS)	777514
Data buffer (LPB)	777516

Unibus Interface

Interrupt Vector	
Address	200
Priority level	BR4
Bus loading	One bus load

Mechanical

Mounting	One free-standing unit + 1 SPC slot
Size	45 in.(114 cm) H × 33 in. 84 cm) W × 22 (56 cm) in. D
Weight	340 lb

Power

Input current	4.5 A @ 115 Vac
Current for control	1.5 A @ +5 V
Power dissipation	500 W

Environmental

Temperature Range	10° C to 40° C (50° – 104°F)
Humidity Range	10% to 90%, max wet bulb 28° C

Models

LP11-VA
LP11-VD
LP11-WA
LP11-WD

Line printer and control, 64 characters, 115 Vac, 60 Hz
Line printer and control 64 characters, 230 Vac, 50 Hz
Line printer and control 96 characters, 115 Vac, 60 Hz
Line printer and control 96 characters, 230 Vac, 50 Hz

LV11 PRINTER-PLOTTER

The LV11 Printer-Plotter provides quieter and more reliable operation than conventional impact printers and pen plotters, especially under heavy, continuous use. The entire ASCII character set (including upper- and lower-case alphabet) is printed in 132 columns per line at 500 lines per minute. The supplied, program-controlled interface allows both printing and plotting, and accommodates most DIGITAL line printer software. In the Plotting mode, the LV11 prints 122,880 dots per second (independent of picture complexity) with a resolution of 10 bits (1024 dots per line). The printer-plotter uses roll paper for continuous plots and printouts (up to 500 ft), or fanfold paper for easier handling.

The electrostatic printing technique employs a fixed writing head with 1024 addressable writing electrodes. As the paper passes over the writing head, any (or all) of the electrodes may be requested to deposit a charge on the coated paper. The charged paper then passes over a liquid toner containing carbon particles; the particles are attracted to the charged areas on the paper, causing the appearance of black dots.

The only moving parts in the LV11 are the paper-moving motor and a small toner pump – simplicity of design that guarantees long, trouble-free operation that more than offsets the small additional cost of the coated paper.

Specifications

Printing

Columns	132 per line
Character spacing	12.5 per inch
Line spacing	7.6 per inch (63 line/page)
Font	7 × 10 dot matrix
Speed	Asynchronous up to 600 lpm
Input Code	USASCII – serial and parallel
Character Set	96 (special)

Graphics

Plotting Width	10.24 inches
Total Writing Nibs	1024 (100 per inch)
Nib Spacing	10.0 mils center to center
Paper Drive Increment	10.0 mils
Input	Parallel 8-bit bytes (128 bytes comprise 1 scan)
Input rate	Asynchronous up to 120 scans/sec
Plotting Speed	Up to 120 increments per second (1.20 inches per second)

General

Writing Method	Electrostatic
Paper Drive	Incremental
Paper Advance Speed	1.20 inches per second

Manual controls, switches, and indicators

Matrix switch panel	• Illuminated power on-off • Paper advance • Illuminated out-of-paper indicator • Form feed
Frame mounted	• Contrast • Master reset • Fan-fold/roll mode selector

Power required

LV01 BA LO	102 +12%	48 to 62 Hz	600 W max
LV01 BA HI	118 +12%	48 to 62 Hz	600 W max
LV01 BB LO	204 +12%	48 to 62 Hz	600 W max
LV01 BB HI	236 +12%	48 to 62 Hz	600 W max

Size 19 in. (48 cm) W x 18 in.(46 cm) D x 38 in. (97 cm) H

Net Weight 160 lb (73 kg)

Paper Width 11 inches

Paper Length 500 foot roll or 1000 sheet continuous form fan-fold 11 × 8-1/2 inches

Toner Supply 2 gallons

Concentrate Supply 8 ounces

Environmental

Temperature Range 50° to 110° F (10° – 43°C)

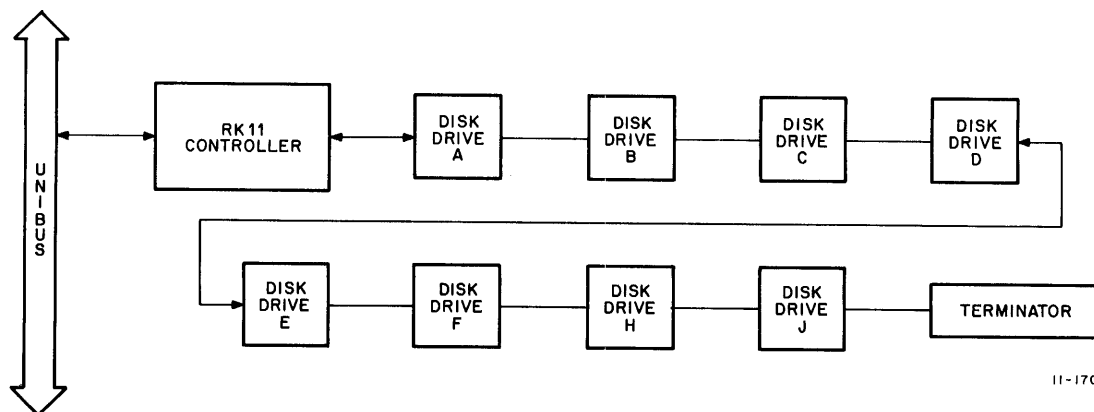
Humidity Range 20% to 80% R.H.

Controller

Mounting Occupies one SPC slot.

RK11-E DECPACK CONTROLLER

The RK11-E is a controller for rotating mass memories, and is capable of communicating with up to eight daisy-chained disk drives. The system is block-oriented, and can handle transfers from 1 to 2^{16} consecutive words without processor intervention. These transfers occur on the Unibus, and are termed Non-Processor Request (NPR) transfers.



The drives used with the RK11-E are the DECpack disk drives, model RK05J. This is a random-access data storage device which uses a high-density single disk cartridge as the storage medium. It has two movable heads which fly, one above, and one below the rotating disk surface, and can read or write (magnetically) up to 400 data tracks, at 1500 rpm. The double-frequency, non-return-to-zero (NRZ) method of recording used in this device can store up to 25 million bits of data. The data formatting is governed by the operating system.

As the drive address logic resides in each device, up to eight RK05 disk drives can be serially connected to the drive bus and operated by one RK11-E controller.

RK11-E Registers

Mnemonic	Code	Description
RKDS	777400	Drive Status Register
RKER	777402	Error Register
RKCS	777404	Control Status Register
RKWC	777406	Word Count Register
RKBA	777410	Bus Address Register
RKDA	777412	Disk Address Register
RKDB	777416	Data Buffer Register

Specifications

Storage Medium

Type

Single disk magnetic cartridge

Disk Diameter

14 in.

Magnetic Heads Number

Two

Recording Density and Format

Density

2200 bpi max

Tracks

406 (200 plus 3 spares on each side of the disk)

Cylinders

203 (two tracks each)

Sectors (records)

4872 (12 per revolution)

Bit Capacities (unformatted)

Per Disk	25 million
Per Inch	2040 (max at inner track)
Per Cylinder	115,200
Per Track	57,600
Per Sector	4,800/3,844

Access Times

Disk Rotation	1500 + 30 rpm
Average Latency	20 ms (half rotation)
Head Positioning	
(including settling time)	10ms – for adjacent tracks 50 ms – average 85 ms – for 200 track movement

Bit Transfer

Transfer Code	Double frequency, non-return-to-zero recording
Transfer Rate	1.44M bits per sec

Electrical

Voltage	115/230 Vac @ 50/60 Hz
Power	250 VA
Starting Current	Power only: 1.8 A Start spindle: 10 A (for 2 sec)

Model Designation

RK05J-AA	95-130 Vac @ 60 ± 0.5 Hz
RK05J-AB	190-260 Vac @ 60 ± 0.5 Hz
RK05J-BA	95-130 Vac @ 50 + 0.5 Hz
RK05J-BB	190-260 Vac @ 50 + 0.5 Hz

Environmental

Ambient Temperature	50° to 110° F (67° to 73° C nominal)
Relative Humidity	8% to 80% (without condensation)
Barometric Pressure	30 + 3 mm hg

Dimensions and Weight

Width	19 in. (48 cm)
Depth	26-1/2 in. (66 cm)
Height	10-1/2 in. (29 cm)
Weight	110 lb (50 kg)

Controller

Mounting	Backplane is a four slot system unit.

XY11 PLOTTER CONTROLLER

The XY11 Plotter Controller provides the user with a versatile plotting capability. Plots of either 0.01 in. or 0.005 in. steps can be generated at speeds up to 300 steps per second maximum.

The XY11 Controller plugs directly into any available PDP-11 Small Peripheral Controller slot. All operations are under program control; either axis (or both axes) can be addressed in positive or negative incremental steps.

A variety of popular plotters can be interfaced to the XY11 Controller to provide the user with drum, fan-fold, or flat-bed capabilities. Detailed specifications concerning available plotters can be obtained directly from DIGITAL or from the appropriate manufacturer. The following models are currently available:

CALCOMP 563
CALCOMP 565
Houston Complot DP-1
Houston Complot DP-10

Full warranties and maintenance contracts are available for all plotters supplied by DIGITAL.

CALCOMP-563 Specifications

(Manufactured by California Computer Products, Inc.).

Mechanical

Dimensions	9.8 in. (25 cm) H, 39.5 in.(100 cm) W, 14.7 in.(37 cm) D
Type	Drum, table-top

Electrical

Input Power	105-125 Vac, 50/60 Hz
Current	1.5 A

Operational

Plot Size	Y-axis = 28.55 in. X-axis = 120 ft.
Stepping Increments	0.01 in. and 0.005 in.
Stepping Speed	200 and 300 steps/sec

CALCOMP-565 Specifications

(Manufactured by California Computer Products, Inc.).

Mechanical

Dimensions	9.8 in. (25 cm) H × 18 in. (46 cm) W × 14.7 in. (37 cm) D
Type	Drum, table-top

Electrical

Input Power	105-125 Vac, 50/60 Hz
Current	1.5 A

Operational

Plot Size	Y-axis = 11 in. X-axis = 120 ft
Stepping Increments	0.01 in. and 0.005 in.
Stepping Speed	300 steps/sec

Complot DP-1 Specifications

(Manufactured by Houston-Instrument Division of Bausch & Lomb)

Mechanical

Dimensions	9.5 in. (24 cm) H × 19.75 in. (50 cm) W × 14 in. (36 cm) D
Type	Fan-fold, table-top

Electrical

Input Power

115/230 Vac, 50/60 Hz

Operational

Plot Size

Y-axis = 11 in.

X-axis = 8.5 in. (144 ft overall)

Stepping Increments

0.01 in. and 0.005 in.

Stepping Speed

300 steps/sec

Complot DP-10 Specifications**Mechanical**

Dimensions

6.5 in. (17 cm) H × 19.0 in.(48 cm) W × 15.33 in.(39 cm) D

Type

Flat bed, table-top or rack-mounted

Electrical

Input Power

115/230 Vac, 50/60 Hz

Operational

Plot Size

Y-axis = 11 in.

X-axis = 8.5 or 17 in.

Stepping Increments

0.005 in.

Stepping Speed

300 steps/sec

Controller

Mounting

Occupies one SPC slot.

XY311 PLOTTING SYSTEM CONTROLLER

The XY311 Plotting System is the latest in high-speed plotting facilities for the XVM Peripheral Processor. The plotter has a large number of features, for example, three pens, giving the choice of either three colors or three line widths.

Specifications*

Standard Drums	One drum for 36.72 inches (93.3 cm) of paper, accommodates roll paper up to J-Size (or equivalent millimeter size). Y-axis electronic trim adjusts for external scaling for paper variances.
Increment Size	0.002 in. or 0.05 mm – must be specified when ordering
Pens	
Number	3
Spacing	0.6 in. (1.52 cm)
Type	Liquid ink or pressurized ballpoint (interchangeable)
Plot Area	Width (outside pens) 34.2 in. (86.9 cm) Width (any one pen) 33 in. (83.8 cm) Length: 120 ft (36.6 m)
Physical	
Height	42 in. (106.7 cm)
Width	50 in. (127 cm)
Depth	24 in. (61 cm)
Weight	350 lb (158 kg)
Power Requirements	115 Vac; 60 Hz; 6 A (standard)
Heat Dissipation	3413 Btu/hr (860K Calories/hr)
Environmental	
Temperature	77° F $\pm$ 18° F (25° C $\pm$ 10° C)
Relative Humidity	25 to 75%
Options	
Drum	Narrow paper drum
Power	100 V, 208 V, 230 V
Line Frequency	50 Hz
Controller	
Mounting	Occupies one SPC slot.

*Specifications are subject to change without notice.

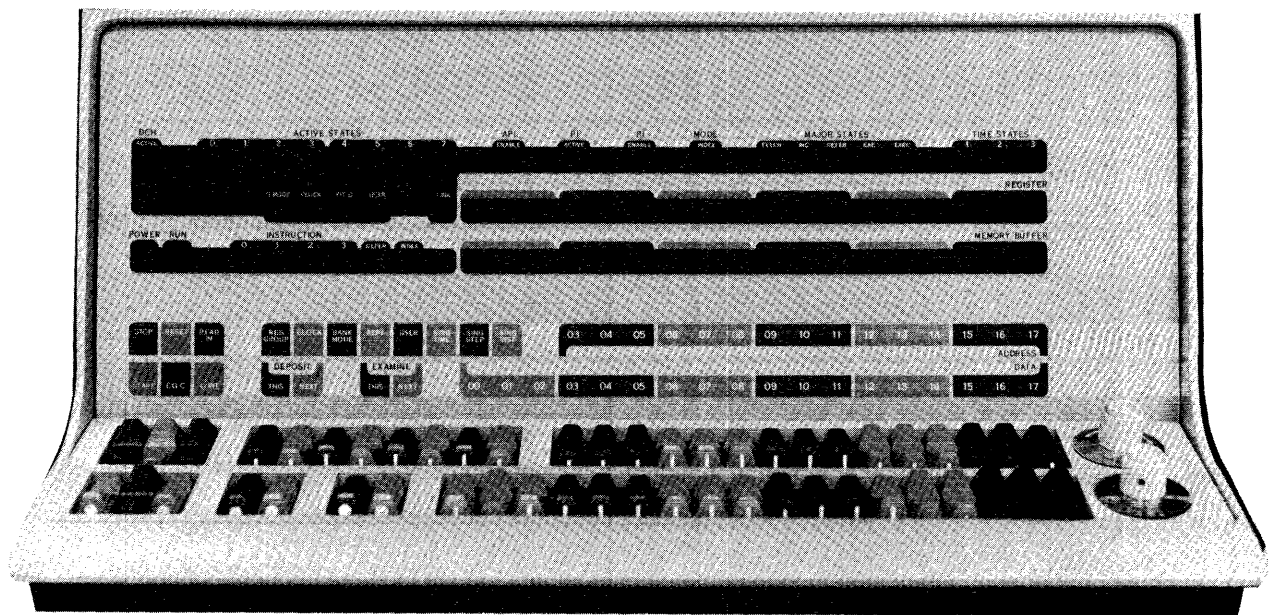
CHAPTER 4

SYSTEM OPERATION

4.1 XVM PROCESSOR

CONSOLE CONTROLS AND INDICATORS

The XVM Console (Figure 4-1) provides the switches and indicators required for operator initiation, control, monitoring, and maintenance of the system. Any of twenty-four 18-bit registers can be displayed selectively to provide the operator with visual indications of all registers and buses.



7882-8

Figure 4-1 XVM Console

Console controls and indicators are described in Tables 4-1 and 4-2, respectively. The two rows of key-type switches are identified by corresponding rows of labels located just below the indicator portion of the console. The upper row of labels identifies the rear switches; the lower row of labels identify the front switches. Unless otherwise indicated, a switch function is active when the rear half of the switch is pressed, or in the case of momentary contact switches, when the elevated half of the switch is momentarily pressed.

Table 4-1
Console Controls

Control	Type	Function
Repeat Speed/ System Power	Potentiometer/ switch	Controls the rate of repeat activity when the system is in Repeat mode. The repeat rate is continuously variable from 1 Hz to 10 kHz. When rotated beyond detent at full counterclockwise position, removes all power to system.
DATA	Eighteen two-position rocker switches	Word length (bits 00–17) register switches to provide binary data that can be read either into the accumulator by execution of an OAS (OR the switch content with the accumulator content) instruction, or into memory under control of the DEPOSIT or executed by the EXEC switch.
ADDRESS	Fifteen two-position rocker switches	Specifies a memory location. These switches are used with the START, DEPOSIT and EXAMINE switches.
START	Spring-loaded momentary-contact switch	Initiates program execution at the memory location specified by the setting of the ADDRESS switches.
CONT	Spring-loaded momentary-contact switch	1. Resumes program execution at the point that it was halted, determined by the contents of the program counter (PC). 2. In conjunction with other control switches (SING TIME, SING STEP, SING INST), steps the program sequentially through the desired time states (SING TIME), major states (SING STEP), or instruction (SING INST).
DEPOSIT THIS	Spring-loaded momentary-contact rocker switch	Places the contents of the DATA switches in the memory location designated by the ADDRESS switches.
DEPOSIT NEXT	Spring-loaded momentary-contact rocker switch	Places the contents of the DATA switches in succeeding memory locations; the location is specified by the ADDRESS switches plus the number of times the NEXT switch is pressed.

Table 4-1 (Cont)
Console Controls

Control	Type	Function
EXAMINE THIS	Spring-loaded momentary-contact rocker switch	Places the contents of memory location specified by the ADDRESS switches in the Memory Buffer (MB) register.
EXAMINE NEXT	Spring-loaded momentary-contact rocker switch	Places the contents of the memory location specified by the ADDRESS switches plus the number of times the NEXT switch is pressed into the Memory Buffer (MB) register. NOTE Operation of the DEPOSIT THIS/NEXT and EXAMINE THIS/NEXT switches does not affect the AC, LINK, XR, LR and PC registers.
STOP	Spring-loaded momentary-contact rocker switch	Terminates program execution when the instruction that is in progress has been executed. NOTE Operation of the STOP switch does not inhibit I/O data channel activity.
SING TIME	Two-position rocker switch	Used with the Continue (CONT) switch to permit the manual stepping of the program through individual time states of each major state.
SING STEP	Two-position rocker switch	Used with the Continue (CONT) switch to permit the manual stepping of the program through individual major states of each instruction.
SING INST	Two-position rocker switch	Used with the Continue (CONT) switch to permit the manual stepping of the program through one instruction at a time.

Table 4-1 (Cont) Console Controls

Control	Type	Function
REPT	Two-position rocker switch	With this switch in the ON position, the processor will repeat the key function pressed by the operator at the rate specified by the repeat speed setting. START – The program execution will restart at a repeat rate of from 1 Hz to 3 kHz after the machine halts. EXECUTE – The instruction in the data switches will be executed at the repeat clock rate (1 Hz to 10 kHz). CONTINUE – Program execution will continue at the repeat clock rate (1 Hz to 10 kHz) after halting. DEPOSIT: The Deposit This; Deposit THIS, NEXT Next or Examine This; EXAMINE: Examine Next function will be THIS, NEXT repeated at the rate of from 1 Hz to 3 kHz. Pressing STOP or turning off the Repeat (REPT) switch will halt the repeat action.
USER	Two-position rocker switch	When set (back half of switch pressed), pressing START causes the system to start in User mode.
BANK MODE	Two-position rocker switch	When set (back half of switch pressed), pressing START causes the system to start in Bank mode permitting direct addressing of 8,192 (17777_8) words of core memory. When switch is not set (front half pressed), pressing START causes the system to start in Page mode permitting direct addressing of 4,096 (7777_8) words of core memory.
CLOCK	Two-position rocker switch	Inhibits program control of the real-time clock. Program control of the real-time clock resumes when the CLOCK switch is OFF.

Table 4-1 (Cont)
Console Controls

Control	Type	Function
EXEC	Spring-loaded momentary-contact rocker switch	Causes the instruction specified by the contents of the DATA switches to be executed. Program will stop following execution of the one instruction.
RESET	Spring-loaded momentary-contact rocker switch	Clears major registers (MB, AC, LINK, PC, IR, XR, LR) and control flip-flops (flags, option select). The clearing prevents any overlap of previous operations from interfering with new operations. Typically RESET is activated prior to reading in programs from paper tape.
READIN	Spring-loaded momentary-contact rocker switch	Initiates the hardware read-in process when transferring information from paper tape into memory. The data is read into memory starting at the location specified by the ADDRESS switches.
		NOTE STOP is the only switch active while the machine is running. If, at any time, the machine must be reset while the RUN light is on, the RESET and STOP switches should be pressed simultaneously. This is an unconditional reset procedure that should be used with caution, because data can be lost.
REG GROUP	Two-position rocker switch	Determines which group of registers the Register Select switch can access for display in the REGISTER indicators. When the front of the REG GROUP switch is pressed, the contents of the register specified in the left-hand window of the Register Select switch are displayed in the REGISTER indicators. When the rear of the REG GROUP switch is pressed, the register, bus, or status information specified in the right-hand window of the Register Select switch are displayed on the REGISTER indicators; typically this second group is used for maintenance purposes.

Table 4-1 (Cont)
Console Controls

Control	Type	Function
Register Select	Twelve-position rotary switch	Used with the REG GROUP switch to select the register, bus, or status data and control signals to be displayed in the REGISTER indicators. The following summarizes the REGISTER display contents for each position of the Register Select and REG GROUP switches. With REG GROUP switch down (left-hand Register Select switch window determines REGISTER display) the REGISTER indicators display the contents of:
AC	Register Bits 00–17	Accumulator register
PC	00–17	Program Counter register
OA	00–17	Operand Address register
MQ	00–17	Multiplier Quotient register
PL/SC	PL0–7, SC11–17	Priority Level/Step counter
XR	00–17	Index register
LR	00–17	Limit register
EAE	States 0–7	Extended Arithmetic Element
	Operations 8–17	Discrete States
DSR	00–17	Data Storage register
I/OB	00–17	Input/Output bus
STA	00–17	Input/Output Status (indicates only when the processor is stopped)
MO	00–17	Memory Output register

Table 4-1 (Cont)
Console Controls

Control	Type	Function
Register Select Switch in position:		With REG GROUP switch up (right-hand Register Select switch window determines REGISTER display) the REGISTER indicators display contents of:
ABU	00–17	A bus
BBU	00–17	B bus
CBU	00–17	C bus
SFT	00–17	Shift bus
IOA	00–17	Input/Output address
SUM	00–17	Sum bus
		NOTE The EAE, A bus, B bus, C bus, and Shift bus output indications are complementary. Therefore, when these functions are selected for display, a lamp is off to indicate a logic 1 (assertion) and lighted to indicate a logic 0 (negation).
Register Select Switch in position:	Twelve-position rotary switch	With REG GROUP switch up (right-hand Register Select switch window determines REGISTER display), the REGISTER indicators display contents of:
M1	Register Bits 00–17	Control Discretes Group 1 Bit 00 – Division shift to the D bus 01 – Multiply shift to the D bus 02 – Single left rotate (RAL) to the D bus 03 – Single right rotate (RAR) to the D bus 04 – Double left rotate (RTL) to the D bus 05 – Double right rotate (RTL) to the D bus 06 – No shift to the D bus 07 – Console switches to the D bus 08 – C bus to the A bus 09 – A bus to the C bus inverted 10 – Index register to the A bus

Table 4-1 (Cont)
Console Controls

Control	Type	Function
M1 (Cont)		11 – Read-in 12 – Shift left 6 to the A bus 13 – I/O address to the A bus 14 – ADDRESS switches to the A bus 15 – Operand address register (OA) to the A bus 16 – Data in 17 – Data out
M2	00–17	Control Discretes Group 2 Bit 00 – SKIP (1) H 01 – Memory Input register (MI) inverted to the B bus – MI-B 02 – Limit Register (LR) to the C bus – LR-C 03 – AND to the B bus 04 – Load the Accumulator (AC) 05 – Load the Memory Output register (MO) 06 – Load the Program Counter (PC) 07 – Load the Operand Address register (OA) 08 – Load the Limit Register (LR) 09 – Load the Index Register (XR) 10 – Buffered AC to the C bus – (B)AC-C 11 – Index Register (XR) to the B bus – XR-B 12 – I/O bus to the C bus – IOB-C 13 – Exclusive OR to the C bus – XOR-C 14 – Central Processor Memory Request CP MEM REQ (1) H 15 – Start READ 16 – Start WRITE 17 – Request Central Processor Memory Release REQ CP MRLS (1) H

Table 4-1 (Cont)
Console Controls

Control	Type	Function
MMA	00–17	00 – ADD 00 H 01 – ADD 01 H 02 – ADD 02 H 03 – ADD 03 H 04 – ADD 04 H 05 – ADD 16 H 06 – NEXM (1) H 07 – MSYNC (1) H 08 – RR00 H 09 – RR01 H 10 – RR02 H 11 – RR03 H 12 – RR04 H 13 – RR05 H 14 – RR06 H 15 – RR07 H 16 – RR08 H 17 – RR09 H
MMB	00–17	00 – USER MODE (1) H 01 – GM(ODE) 1 (1) H 02 – GM 0 (1) H 03 – SHARE H 04 – R DIS (1) H 05 – Not used 06 – PV (1) H 07 – PRE (1) H 08 – BR00 09 – BR01 10 – BR02 11 – BR03 12 – BR04 13 – BR05 14 – BR06 15 – BR07 16 – BR08 17 – BR09
MST	00–12	Not Used

Table 4-2
Console Indicators

Indicator	Function
POWER	Indicates that the power supply voltages are at operating levels.
RUN	Indicates that the program execution is in progress.
G MODE	Indicates that system is in GM 1, 2, or 3.
CLOCK	Indicates that the real-time clock facility is enabled.
IOTD	Indicates that IOTs are trapped in User mode.
USER	Indicates that system is in User mode.
DCH ACTIVE	Lights when the data channel is being serviced, i.e., data is being transferred between core memory and a device via the I/O bus.
API ENABLE	Lights when the automatic priority interrupt system is activated.
API STATES ACTIVE	Indicates API level(s) active.
0–3	Hardware levels
4–7	Software levels
MAJOR STATES	
FETCH	Indicates that the processor is in the Fetch state.
INC	Indicates that the processor is in the Increment state.
DEFER	Indicates that the processor is in the Defer state.
EAE	Indicates that the processor is in the EAE (extended arithmetic element) instruction state.
EXEC	Indicates that the processor is in the Execute state.
TIME STATES 1, 2, 3	Indicates the processor time states. When all time states are off, machine is in time state 2A of the ADD instruction.
PI ACTIVE	Indicates that a program interrupt is pending service.
PI ENABLE	Indicates that the program interrupt system is enabled (under program control).

**Table 4-2 (Cont)
Console Indicators**

Indicator	Function
MODE INDEX	Indicates that the processor is operating in Page mode and therefore indexing can be accomplished.
LINK	Displays state of the Link bit.
INSTRUCTION 0–3	Displays contents of the 6-bit program word instruction field. Displays the instruction operation code.
DEFER	Indicates that the operand is indirectly addressed.
INDEX	Indicates that the operand address is indexed when in Page mode or that the upper 4K (of an 8K bank) is addressed when in Bank mode.
MEMORY BUFFER 00–17	Displays the contents of the currently accessed memory address.
REGISTER 00–17	Used with the setting of the REG GROUP and Register Select switches to display: a. Data in a register. b. Data on a bus. c. Control signal levels.

OPERATING PROCEDURES

Power On

1. Set the Repeat/Power switch to OFF.
2. Set primary ac power circuit breaker on 861 Power Controller at rear to ON.
3. Set peripheral ac power circuit breakers to ON.
4. Rotate the Repeat/Power switch clockwise from the OFF position.

NOTE

To prevent power from being turned off, and switches being activated on console, set the console LOCK switch to ON. This switch is located on the BA15 logic panel, at the bottom of the CP cabinet (Bay 00), behind the short door. For normal use leave the switch in the UNLOCK position (down).

Program Load Procedure

To load a program from paper tape, perform the following steps:

1. Turn System power switch ON.
2. Load program tape in high-speed paper-tape reader.
3. Set program start address into Console Address switches.
4. Press STOP switch.
5. Press RESET switch.
6. Press READIN switch. Paper-tape is now read into core memory.

NOTE

At completion of paper-tape read-in, the processor executes the last word read-in as an instruction.

This procedure is also used for tabulating other types of data stored on paper tape.

Start Program Procedure

To begin data processing at a specified address, perform the following steps:

1. Press STOP switch.
2. Press RESET switch.
3. Enter desired starting address in ADDRESS switches.
4. Press START switch. Selected program will now be executed.

Manual Control of Processing

To observe the program progress on a step-by-step basis, perform the following steps:

1. Set the SING INST, or SING STEP, or SING TIME switch for the desired operation; single instruction, single step (major state) or single time (time state), respectively.
2. Set the ADDRESS switches to specify the selected starting address.
3. Press the START switch. The results of the instruction, step, or time is available at the console displays.
4. Advance the program operation by pressing the CONT (continue) switch; or if desired, control the functions repetition rate with the repeat speed control portion of the Repeat Speed/System Power potentiometer switch.

Memory Examination

To examine the contents of a selected core memory address, perform the following steps:

1. Set the ADDRESS switches to the memory location to be examined.

2. Press the EXAMINE THIS switch to observe the contents of the selected address.
3. To observe the next sequential memory address in the MEMORY BUFFER display, press the EXAMINE NEXT switch. Each time the EXAMINE NEXT switch is pressed, the MEMORY BUFFER display will show the contents of the next sequential memory location; or, with the REPT switch pressed, will advance through memory locations automatically at the rate determined by the repeat speed control portion of the Repetition Speed/System Power potentiometer switch up to a maximum of 3 kHz.

Data Storage from Console

To manually insert data into a specific memory location, perform the following steps:

1. Set the DATA switches to the binary configuration of the data that is to be deposited into core memory.
2. Set the ADDRESS switches to specify the memory location where the data is to be stored.
3. Press the DEPOSIT THIS switch; or, to deposit data in sequential memory locations, set the DATA switches to the data word configuration and press the DEPOSIT NEXT switch. Each time the DEPOSIT NEXT switch is pressed, the current DATA switch configuration will be deposited in the next sequential memory location.

NOTE

Examining and depositing information into or out of memory can be conducted without affecting the contents of the PC, AC, XR, LR, and L. Thus a program can be stopped, an arbitrary location can be loaded or examined, and the program can be continued by pressing the Continue (CONT) switch. While the program is running (RUN indicator light on), the EXAMINE, EXAMINE NEXT, DEPOSIT, DEPOSIT NEXT, START, EXEC (execute), and CONT switches are not effective. The program must be stopped by pressing the STOP switch or by pressing the SING TIME, SING INST, or SING STEP switches. This interlock was provided to prevent accidental destruction of an operating program. Switches which are active during RUN are located on the upper left of the console panel.

Manual Execution of Instruction

To manually execute an instruction encoded at the console, proceed as follows:

1. Set the DATA switches to the binary format of the instruction word.
2. Press the EXEC key. The processor will halt after executing the instruction.

Reset

To clear the machine states, and the I/O control and devices, press the RESET key. If the machine is hung, press both the STOP and RESET keys at the same time.

Peripheral Processor

The Peripheral Processor (Figure 4-2) indicator and switch functions are described in the following paragraphs.

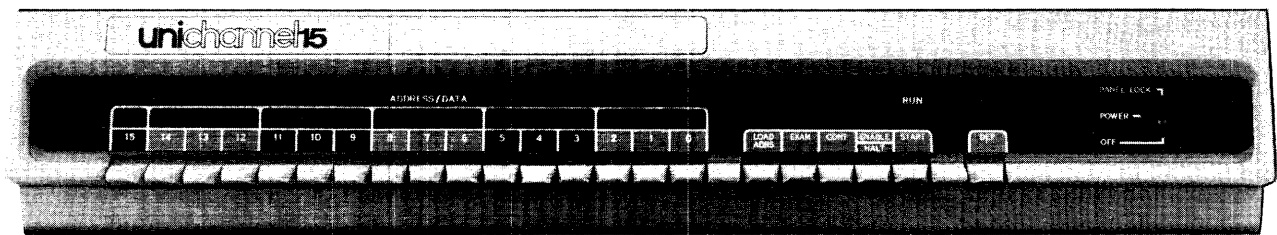


Figure 4-2 Peripheral Processor (PDP-11/10)

The key lock power switch (Figure 4-2) has three positions:

- OFF – Fully counterclockwise
- POWER – 90° clockwise from OFF
- PANEL LOCK – 180° clockwise from OFF

In the OFF position, ac power is removed from the primary of the computer power supply. In the other two positions, the ac power is applied to the computer power supply and the cabinet power control contacts are short-circuited. In the POWER position, the console function switches (the right six switches) are fully operative. In the PANEL LOCK position, the console function switches have no effect on the computer's operation. PANEL LOCK is used to secure a running computer from mischievous tampering.

Function Switches

The six right switches are called function switches. They are listed below in order of their appearance from left to right.

1. LOAD ADS (load address)
2. EXAM (examine)
3. CONT (continue)
4. ENABLE/HALT
5. START
6. DEP (deposit)

Function switches 1 through 5 are actuated by being pressed as is the ENABLE/HALT switch in Figure 4-2. The DEP switch must be lifted for actuation. All of the function switches, with the exception of ENABLE/HALT, are spring loaded and return to their rest state when released.

Address/Data Switches

The 16 ADDRESS/DATA switches are to the left of the function switches (Figure 4-2). These 2-position switches represent a manually set flip-flop register with the up position representing a logical 1 and the down position a logical 0. The ADDRESS/DATA switches may be used with the function switches or in conjunction with a program stored in the computer's memory. The ADDRESS/DATA switches are often referred to as the Switch register in DIGITAL documentation. In Figure 4-2, the contents of the Switch register is equal to 200₈ because bit 7 is set to a 1 and all others are set to a 0.

Console Indicators

There are 17 indicators on the computer console. The contents of the 16 ADDRESS/DATA lights either represent a 16-bit Unibus address or the contents of a 16-bit Unibus address. Note that the state of the ADDRESS/DATA lights is defined only when the computer RUN light is not illuminated.

CONSOLE OPERATION

The following paragraphs describe the operation of the function switches. Table 4-2 indicates the meaning of ADDRESS/DATA lights for all cases where the contents of these lights are defined.

Load Address Switch

Pressing the LOAD ADRS switch when the computer is halted causes the contents of the Switch register to be stored in a temporary register within the computer. This data is also displayed in the ADDRESS/DATA lights for verification. The load address operation performs the following functions:

1. Selects a Unibus address for a subsequent examine operation.
2. Selects a Unibus address for a subsequent deposit operation.
3. Selects the starting address of a program.

Examine Switch

The EXAM switch permits the display of the contents of a selected Unibus address in the ADDRESS/DATA lights. Select the appropriate address in the Switch register and press the LOAD ADRS switch. Then press and release the EXAM switch. The contents of the selected address will then be displayed in the ADDRESS/DATA lights. Several features are built into the examine function to aid in programming the computer.

1. While the EXAM switch is pressed, the address to be examined is displayed. The data itself is displayed when the switch is released.
2. If the EXAM switch is pressed repeatedly, the Unibus address is incremented by two each time*. This permits the examination of a list of addresses without repeated load address operations.
3. If an attempt is made to examine non-existent memory, it is necessary to perform the initialize operation, by pressing START with ENABLE/HALT in the HALT position.
4. Only full words are displayed in the ADDRESS/DATA lights; thus, bit 0, the byte address bit, is ignored when using the EXAM switch with the following exception. Note that the general registers are located on byte addresses. Therefore, when examining the general registers, address bit 0 is recognized and the increment feature is modified so that sequential registers may be examined by repeated use of the EXAM switch.

Note that the EXAM switch has no effect while the computer is in the RUN state or when the key operated power switch is in the PANEL LOCK position.

*The Unibus address is incremented by one when examining general registers.

Significance of ADDRESS/DATA Indicators

Action	Qualification	Information Displayed in ADDRESS/DATA Indicators
Power On	1. ENABLE/HALT switch in HALT position 2. ENABLE/HALT switch in ENABLE position	1. Contents of location $(24)_8$ 2. Undefined — Depends on contents of memory
Load Address	LOAD ADRS switch pressed	Contents of Switch register
Examine	1. EXAM switch pressed 2. EXAM switch released	1. Unibus address that is to be examined 2. Contents of Unibus address that was examined
Deposit	1. DEP switch raised 2. DEP switch released	1. Unibus address that is to be deposited 2. Contents of Switch register which is the data deposited
RUN Light On		Undefined
Program Halt	1. ENABLE/HALT switch in HALT position 2. HALT instruction executed 3. Double bus error which is two successive attempts to access nonexistent memory or improper odd byte address.	1. Address of instruction to be executed when CONT switch is actuated 2. Same as 1 3. Contents of program counter (R7) at time double bus error occurred
Program Execution	1. START switch pressed 2. CONT switch pressed	1. Address of last load address 2. Address of instruction to be executed

Deposit Switch

The physical operation of the DEP switch requires that it be lifted for actuation. The DEP switch permits the contents of the Switch register to be deposited in a Unibus address, which is typically specified by a previous load address operation. To deposit the instruction **BRANCH SELF** (777_8) in location 200_8 , first set the Switch register to 200_8 , as shown in Figure 4-2, and actuate the LOAD ADRS switch. Set the Switch register to 777_8 , then lift and release the DEP switch.

Several additional features are built into the deposit function:

1. While the DEP switch is actuated, the Unibus address to be effected is displayed in the ADDRESS/DATA lights. When the switch is released, the data deposited is displayed for verification.
2. If the DEP switch is repeatedly pressed, the Unibus address is incremented by two each time* This permits the depositing of an entire program with only one load address operation.
3. If an attempt is made to deposit into non-existent memory, it is necessary to perform the initialize operation by pressing the START switch with the ENABLE/HALT switch in the HALT position.
4. All deposit operations affect full 16-bit words. Bit 0 of the address is used only when depositing into general registers, otherwise, bit 0 of the address is ignored.

Enable/Halt Switch

Place the ENABLE/HALT switch in the HALT position; the computer will halt at the end of the current instruction, providing the key switch is not in the PANEL LOCK position. All interrupts and traps will be executed prior to halting. This switch may be used with the CONT switch to step through programs. With the ENABLE/HALT switch in the ENABLE position, programs may be executed once started by pressing the START switch, pressing the CONT switch, and actuating the auto-restart power-up sequence.

Start Switch

The sequence for starting a program from the console is as follows:

1. Set the starting address of the program in the Switch register.
2. Press the LOAD ADRS switch.
3. Position the ENABLE/HALT switch in the ENABLE position.
4. Press and release the START switch.

While the START switch is pressed, the following actions occur:

1. An initialize signal is generated on the Unibus. This initialize signal resets all peripherals.
2. The program status word is reset to zero.
3. The program counter, R7, is loaded with the last address loaded with the LOAD ADRS switch.

When the START switch is released, program execution begins with the instruction contained in the location specified by R7 and the RUN light is turned on. If the ENABLE/HALT switch is in the HALT position, the computer remains in the HALT state following the release of the START switch.

Observe the following precautions when using the START switch:

1. If the keylock is not in the PANEL LOCK position, pressing the START switch while a program is running initializes the computer system and restarts the program.

*The Unibus address is incremented by one when depositing into general registers.

2. It is good practice to precede every program start with a load address operation.
3. A program should not be started at an odd address or the first fetch operation will be aborted and an odd address trap will be attempted. If the stack pointer, R6, is not properly set up, the program in memory may be destroyed.

Continue Switch

The CONT switch is used to continue a program without altering the program counter, R7, or the machine state. To continue a halted program, press and release the CONT switch. The program is resumed when the CONT switch is released.

The CONT switch is used with the ENABLE/HALT switch to step through programs one instruction at a time. If the CONT switch is actuated while the ENABLE/HALT switch is in the HALT position, a single instruction will be executed. Note that interrupts are serviced in Single Instruction mode. In Single Step mode, the address of the next instruction to be executed is displayed in the lights.

UNCONDITIONAL COMPUTER AND UNIBUS INITIALIZATION

Unconditional initialization of the computer system usually occurs because of an attempt to examine from, or deposit into, non-existent memory from the console. However, a peripheral or processor error may occur that can only be overcome by initializing the system from the console. The procedure is simply to press the START switch with the ENABLE/HALT switch in the HALT position.

LOADING PROGRAMS FROM PAPER TAPE

The peripheral processor has no direct means of loading paper tapes as the XVM does; however, there is a procedure whereby the XVM helps the peripheral processor to load.

The first operation is to load the ABSL11 tape DEC-15-ODABA-A-PH into the XVM memory at a starting address of 17700. The XVM will then wait for the operator to load the requisite tape to be transferred to the peripheral processor.

When this tape is loaded, start the peripheral processor at 100000₈ (for 8K of local memory), 140000 (for 12K). Then press CONT on the XVM Console. The XVM will halt when the operation is complete. The peripheral processor will obey the last instruction on the tape.

4.2 PC15 HIGH-SPEED PAPER-TAPE READER AND PUNCH

The PC15 High-Speed Paper-Tape Reader and Punch is standard on XVM Systems. The perforated paper-tape reader photoelectrically senses eight-channel paper-tape at a rate of 300 lines per second. Under program control, data is read in either Alphanumeric (one-line) or Binary (three-line) modes. The use of a paper-tape reader buffer and buffer-full flag permits the continuation of processing during the reading functions.

The paper-tape punch (50 characters per second) is mounted on the same chassis as the reader. In Alphanumeric mode, an output instruction causes an 8-bit character to be transferred from the XVM Accumulator to a punch buffer, from which it is punched on the tape. In Binary mode, an 18-bit word is transferred from the Accumulator. Fan-fold paper-tape is normally used with the high-speed paper-tape reader and punch.

Controls

Front Panel Controls are illustrated in Figure 4-3 and described in Table 4-3.

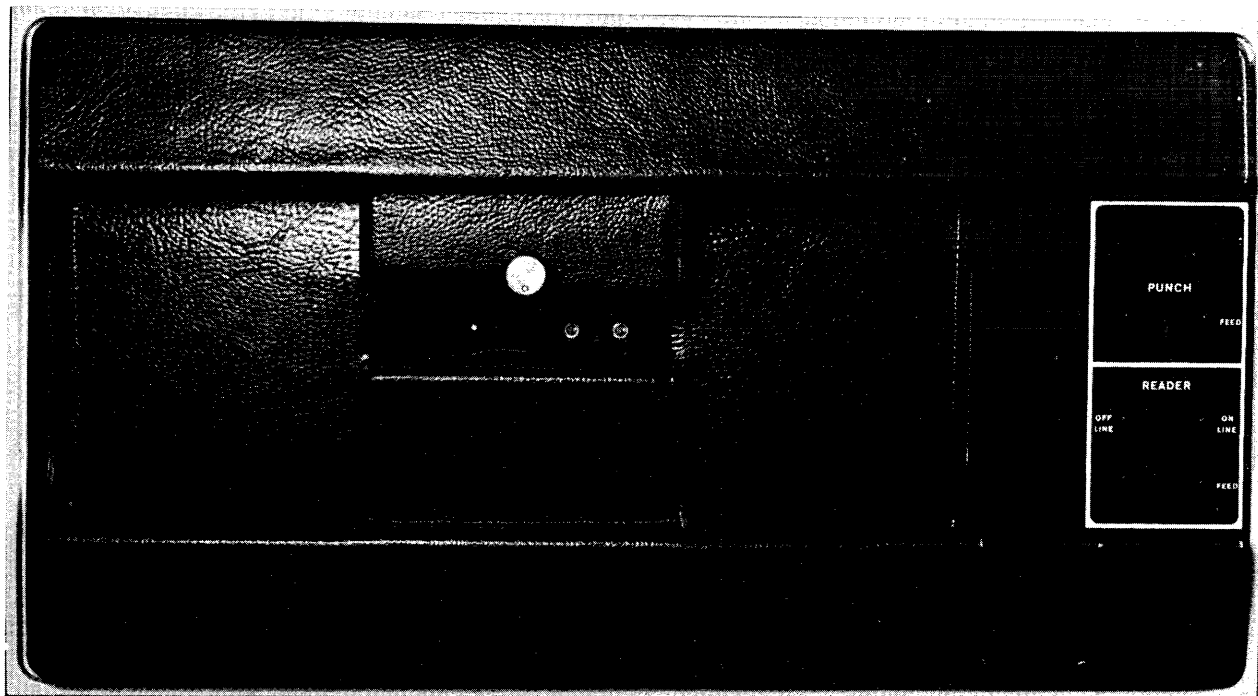


Figure 4-3 Paper Tape Reader and Punch

Table 4-3
Paper-Tape Reader and Punch Controls

Control	Type	Function
FEED (Reader)	Momentary-contact pushbutton	When pressed, causes tape to advance without reading; also clears the reader out-of-tape flag to permit automatic read operation.
ON LINE/ OFF LINE FEED (Punch)	Two-position rocker switch Momentary-contact pushbutton	When in ON LINE position, the reader can be activated from the computer. When pressed, causes tape to advance, punching only feed holes.

Paper Tape Reader Operating Procedure

Directions for initiating read-in from the console are given in the console operating procedures, Paragraph 4.1. The only operator function directly associated with the tape reader is loading the tape. The tape is stored in flat packets of fan-fold form; that is, the tape is folded back and forth upon itself. One of the tape surfaces is imprinted with arrows at frequent intervals along the length of the tape. The arrows indicate the direction which the tape must advance in the read operation. To install a tape in the reader, proceed as follows:

1. Set the processor POWER switch ON.
2. Set ON LINE/OFF LINE switch to OFF LINE.

3. On the tape reader, rotate tape hold-down knob clockwise (Figure 4-3).
4. Hold the packet of tape in both hands as shown in Figure 4-4 and open it to a fold at which printed arrows are visible. Orient the tape so that the arrows point from the operator's right to left.



Figure 4-4 Orienting the Tape

5. Without changing its relative position, fold the complete packet into the right hand. With the left hand, pull the end of the tape toward the direction in which the arrows point, opening out the first two folds.
6. Place the lower end of the packet diagonally into the corner of the lower feed pocket, as shown in Figure 4-5a.
7. Bend the upper end of the packet toward the read station and thrust it into the upper feed pocket (Figure 4-5b). The packet will be supported in the feed position.
8. Place the extended part of the tape edgewise under the tape retainer, shown in Figure 4-5c. The tape should now be lying flat across the read station, the printed side should be up, and the arrows should point from right to left.
9. Position the tape so that the first crease is a few inches beyond the read station and ensure that the feed holes are engaged by the feed sprocket. Rotate the tape hold-down knob counterclockwise.
10. Stand the free end of the tape in the receiving pockets so that the first fold is oriented toward the read station.

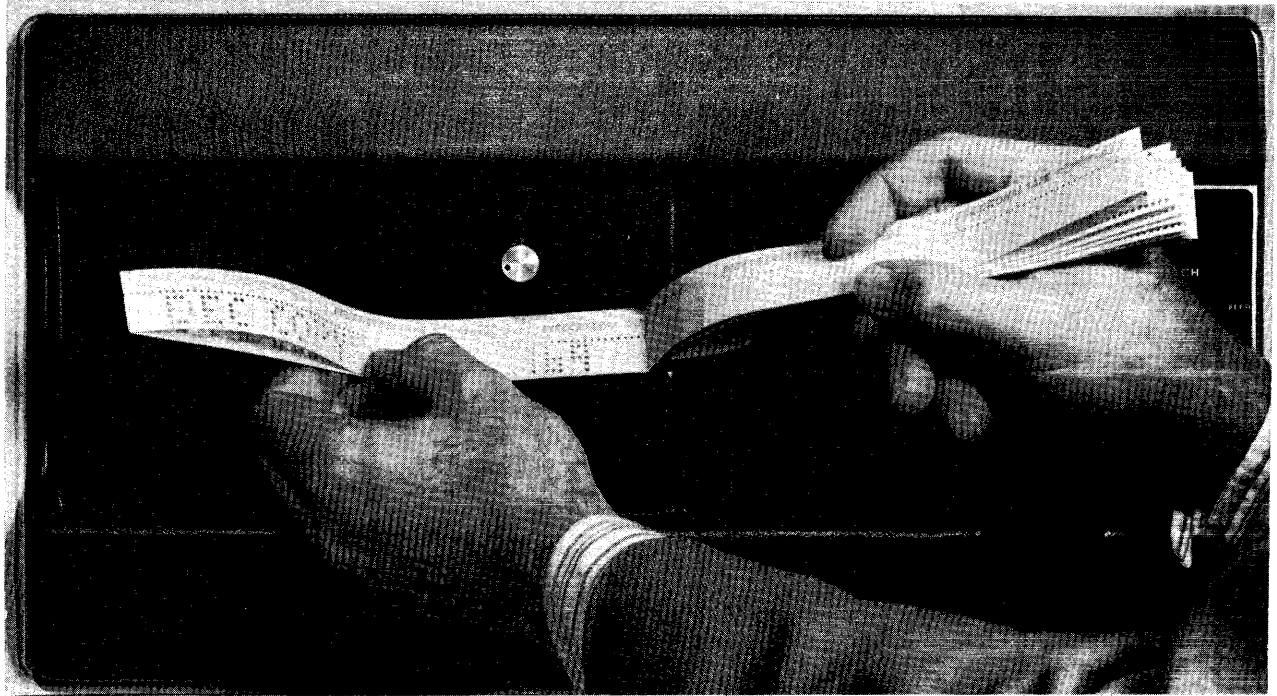


Figure 4-5a Installing Tape in Paper Tape Reader

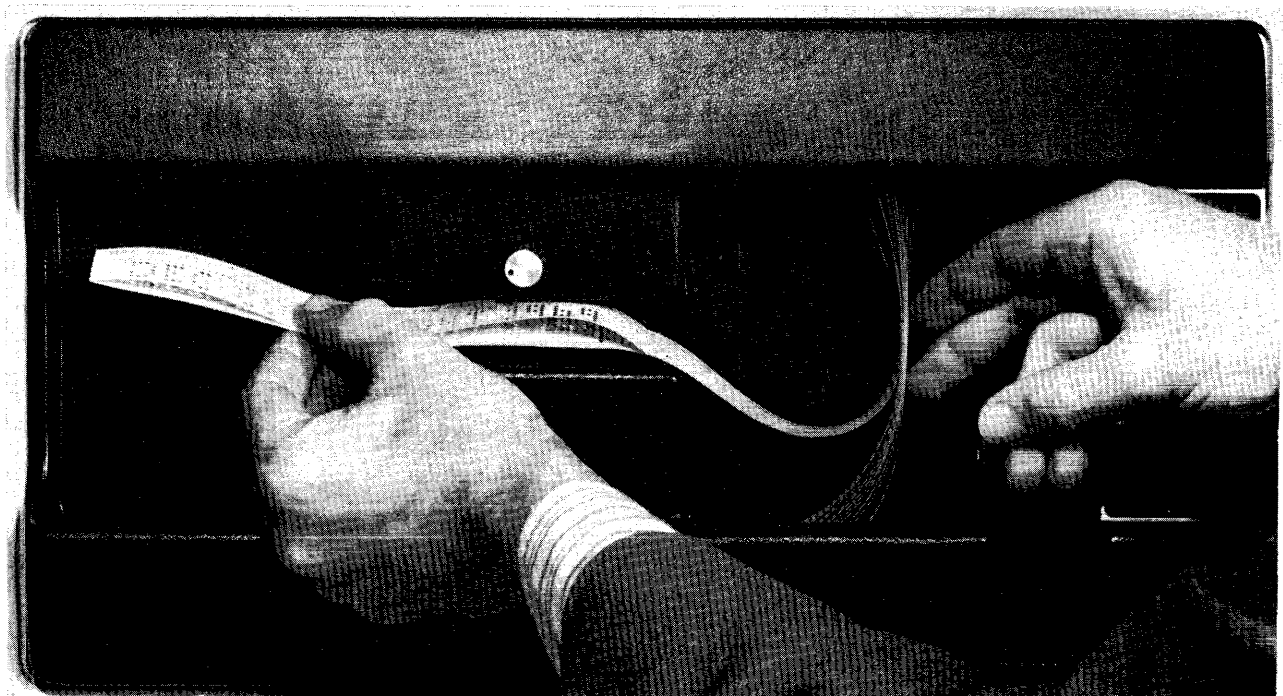


Figure 4-5b

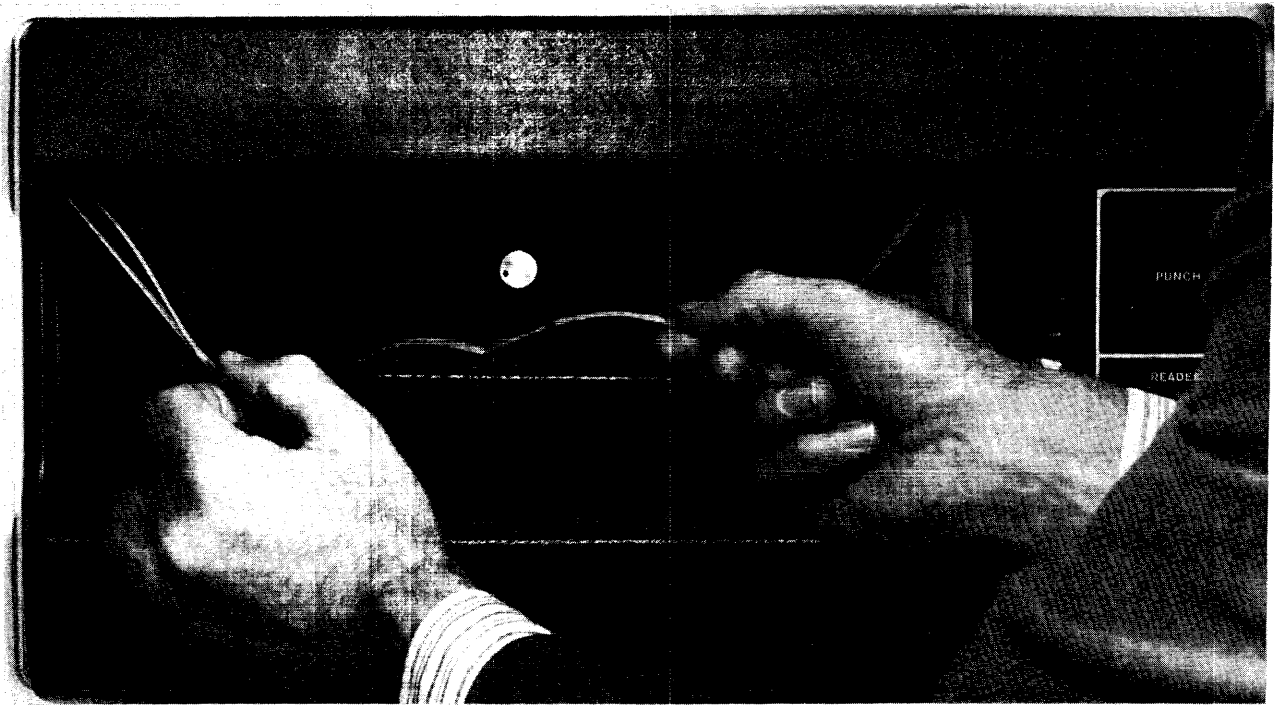


Figure 4-5c

11. Press the FEED switch momentarily, and observe that the tape moves from right to left and begins to fold automatically into the receiving pockets. Advance the tape sparingly; do not let the data portion of the tape reach the read station (Figure 4-5d).

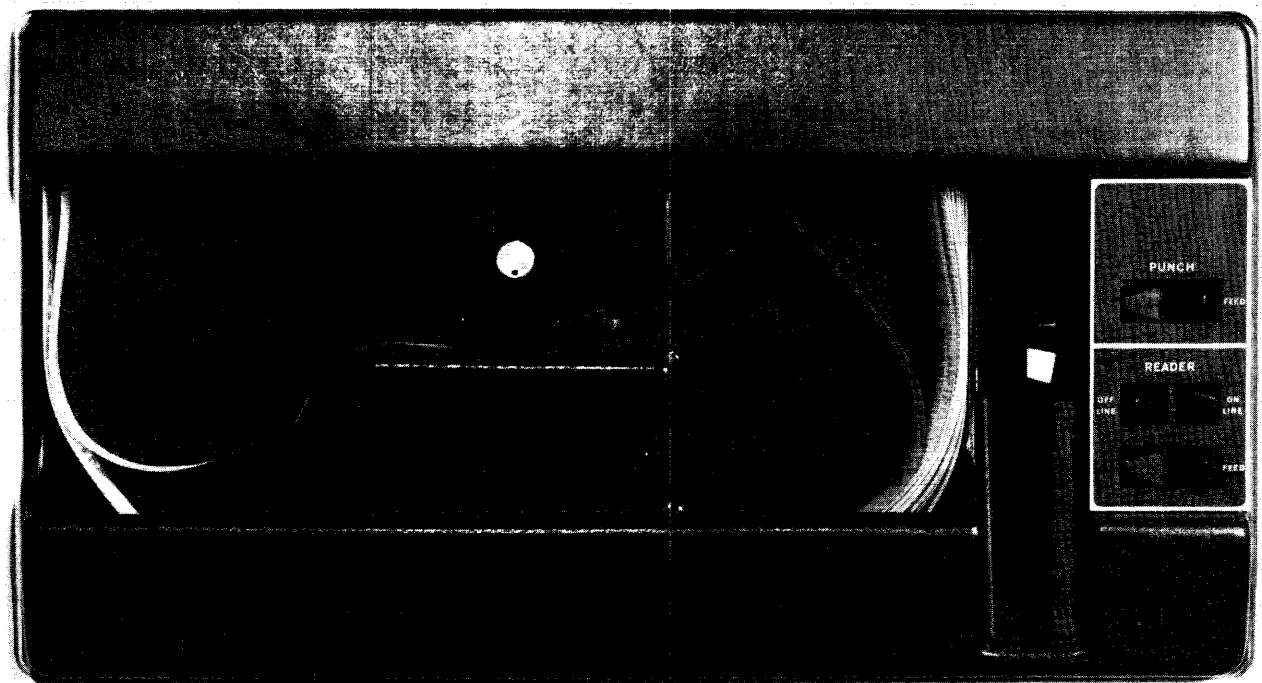


Figure 4-5d

NOTE

Always press the reader FEED switch momentarily. This action is necessary to clear the out-of-tape flag which was set automatically when the last tape was removed.

12. Set ON LINE/OFF LINE switch to ON LINE.

The tape is now prepared for read-in. If read-in is to be under control of the program, no further action is required. If the program directions specify manual read-in, follow the console procedure for reading-in from paper-tape.

Paper Tape Punch Tape Installation

New paper-tape is printed with directional arrows, and has no perforations of any kind. Tape is furnished in 1000-ft lengths in fan-fold form, packed in pasteboard boxes. To install tape in the punch unit, remove the top of the box completely, then proceed as follows:

1. Slide the reader/punch unit out from the cabinet frame and insert the box of tape. Position the box with the open side up so that the arrows on the tape are pointing from right to left (Figure 4-6a).
2. Draw the end of the tape off to the right, arrow side down, twist the end slightly counterclockwise and pass it through the tape guides (Figure 4-6a).
3. Pass the tape over the arm of the out-of-tape microswitch and under the backing plate, making sure that the arrows are on the under side of the tape (Figure 4-6a).
4. Open the hinged tape retainer outward, exposing the drive sprocket (Figure 4-6b).
5. Place the end of the tape between the metal tape guide-plates which are under the chad chamber. Push the tape forward until the end passes over the sprocket; close the tape retainer (Figure 4-6b).
6. Turn the tape-advance control counterclockwise and observe that the tape advances; then slide the unit back into position in the cabinet frame (Figure 4-6b).

NOTE

Make it a habit to empty the chad box when replacing tape!

Placing Punch in Service

To place the punch in service, proceed as follows:

1. Set the processor POWER switch ON. This applies power to both the processor and the tape unit.
2. Press and hold the FEED switch until four or five folds (about three feet) of tape are run into the tape punch output hopper (Figure 4-3).
3. Since the punching of feed holes starts only at some distance from the beginning of tape, tear off the tape end neatly at the first crease and discard it. This will leave about two feet of data-free leader fully punched with feed holes for handling and threading the finished tape.

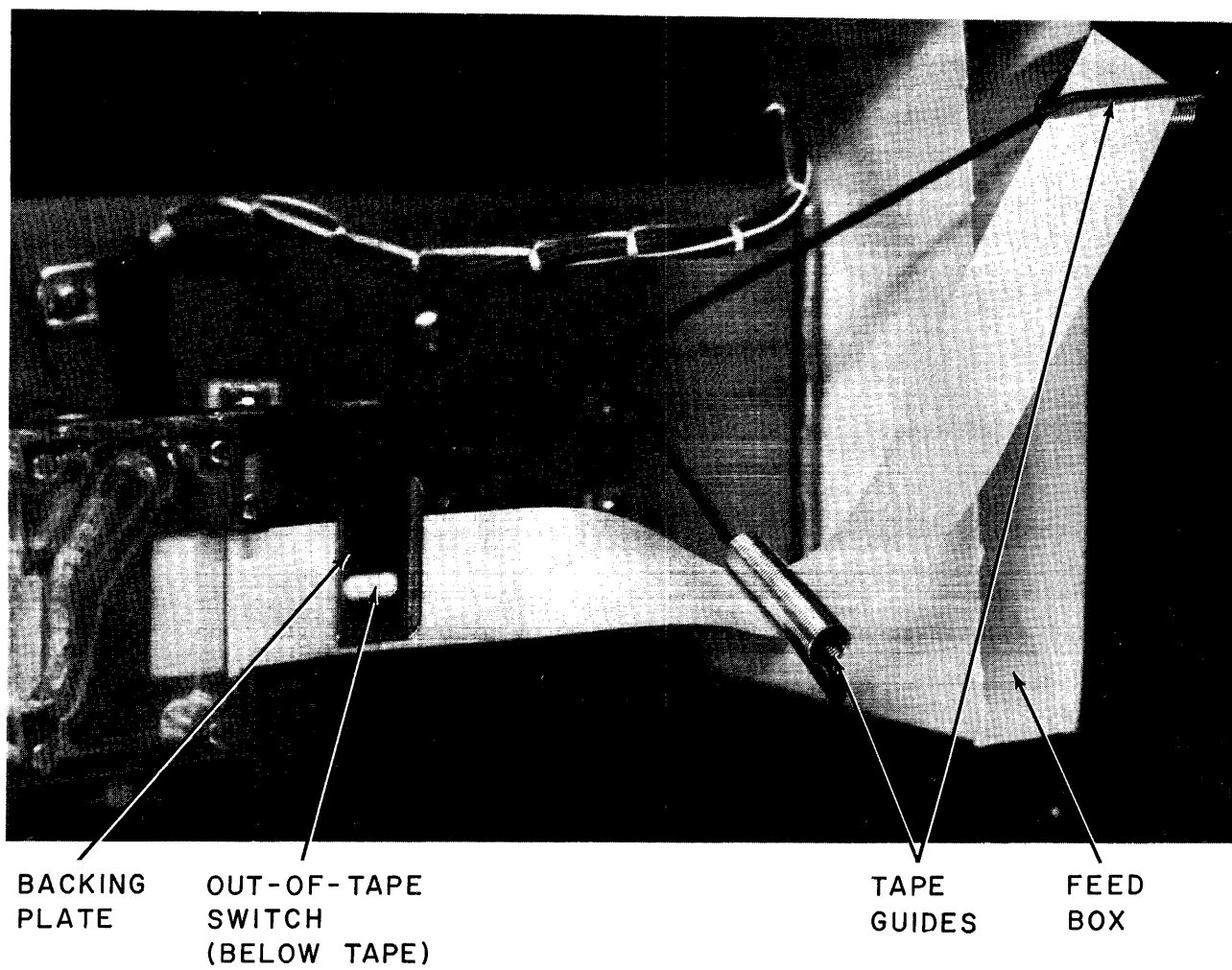
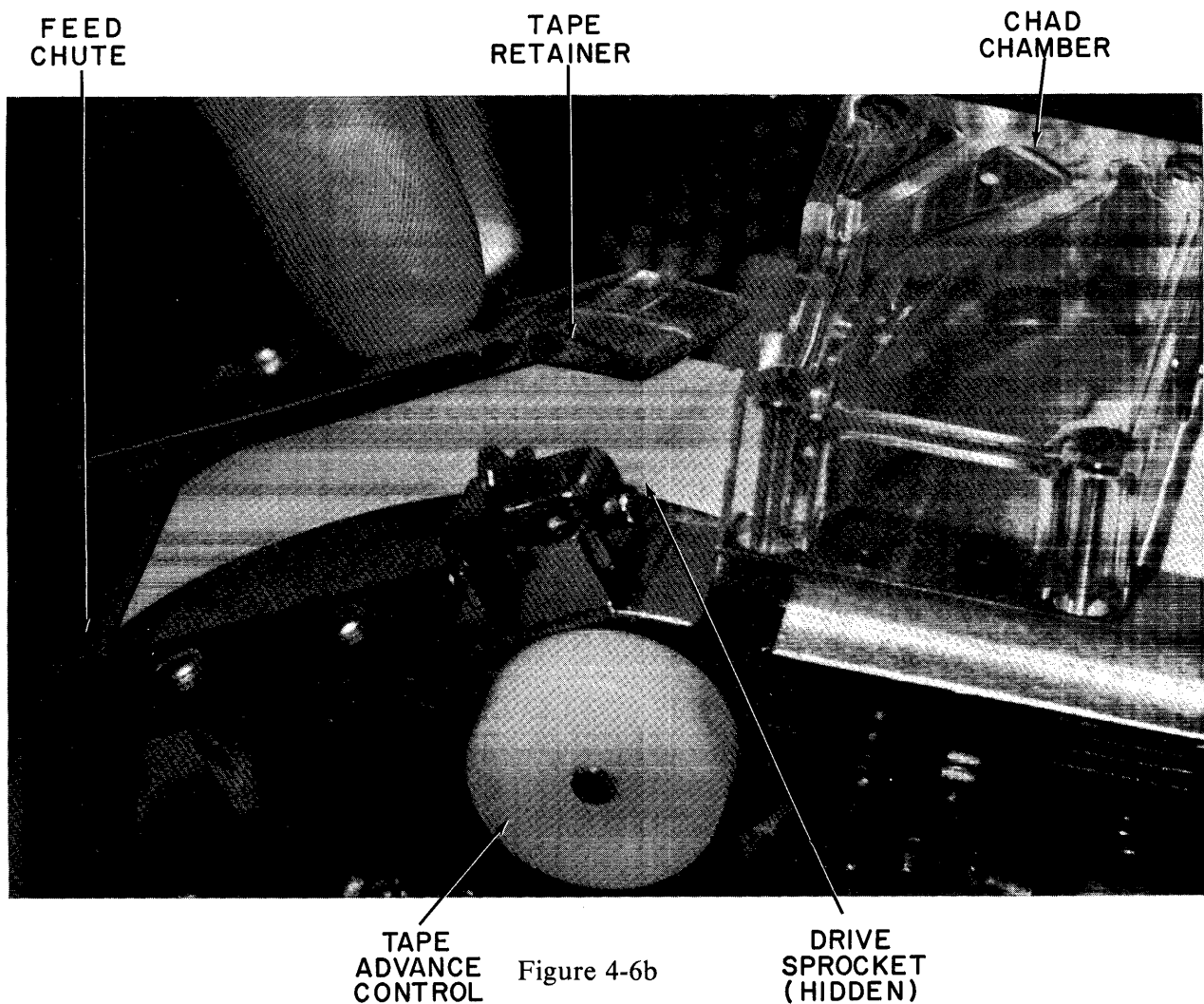


Figure 4-6a Installing Tape in High-Speed Paper Tape Punch



Removing Punched Tape

To remove punched tape, perform the following steps:

1. After punching has been completed, press the punch FEED switch and run off about two feet of data-free trailer; tear off the output tape at a crease and remove it.
2. Press the punch FEED switch again to run off a new leader. The unit is now prepared for the next program.

Chad Removal

The small disks of paper which are punched out of the tape are called chad. The punches at the punch station strike upward and deposit the punch-outs in the chad chamber (Figure 4-6b). From there, the chad is conducted by gravity through a tube into a removable box.

CAUTION

Remove the chad as directed.

1. Remove and empty the chad box before it becomes one-quarter full.
2. Remove any chad or dust which has accumulated elsewhere in the compartment using a suitable vacuum cleaning device or a clean, slightly dampened cloth.
3. Replace the chad box.

Splicing and Repairing Paper Tape

Splicing tape is not desirable, but may be necessary in the following situations:

End of Tape – After most of the tape in the box has been punched, the approaching end of the supply is indicated by special coloring on the remaining tape. When this coloring is observed, install new tape as soon as possible to avoid running out of tape during a program. If the specially colored portion of the tape should appear during a program, proceed as follows:

1. Press the control console STOP switch.
2. Press the punch FEED switch and feed out the last of the tape.
3. Load new tape into the unit.
4. Place the unit in service.
5. Restart the program by pressing the CONT switch on the control console.
6. Remove the finished tape.
7. Splice the leader of the second length of tape to the trailer of the first length, using rubber cement, so that the spliced section has the following characteristics:
 - a. The splice overlap is about three inches.
 - b. The portion containing the splice forms a flag segment of the same length as others in the tape (8-1/2 in.). Do not splice over a fold.
 - c. The folds at each of the spliced segments are opposite directions.
 - d. The arrows of both tape portions are on the same side of the tape and point in the same direction.
 - e. The feed holes in the overlap coincide exactly.
 - f. The splice does not overlap the data portion of either tape.

Torn Tape – If a punched tape has been torn between data holes or through the data portion and duplicate tape is not readily available, proceed as follows:

1. Align the torn edges to restore the original unbroken form as closely as possible.
2. Secure the two pieces together with transparent mending tape on each side of the line of feed holes.

NOTE

If the feed holes are covered, punch the mending tape to clear the holes.

CHAPTER 5

SYSTEM INSTALLATION

5.1 INTRODUCTION

The purpose of this chapter is to assist the reader in making decisions about the environment before the delivery of a DIGITAL computer system. This chapter does not deal with specific devices, nor does it supersede installation instructions in existing manuals.

There are, at present, two manuals published by DIGITAL to help prospective computer owners plan their installation. These are:

1. *Computer Site Preparation Handbook*, DEC-00-ICSPA-A-D, and
2. *Site Preparation and Planning Guide*, DEC-00-HSPPG-A-D.

NOTE

Due to the multiplicity of standards throughout the world, no reference materials have been included in this chapter. There are, however, DIGITAL Field Service and Sales Engineers available to answer any questions that arise.

The complexity of the system determines, to a large extent, the quality of the environment necessary for a trouble-free installation.

Magnetic storage devices have the narrowest operating range and this should be kept in mind when planning an installation.

It is very unusual for a system to remain in the same configuration as when initially installed. The majority of customers decide to "add on" options after a time. This leads to changes in existing environmental control of installations. It is therefore wise to plan computer sites with plenty of room for expansion.

5.2 PREDELIVERY PLANNING

Each computer system installation differs in some ways from every other installation, so that no single overall schedule of predelivery activity will apply in all cases. Table 5-1 shows a typical list of general site preparation and installation functions, indicating those areas in which a Digital Equipment Corporation representative might be of substantial assistance.

It is important that a detailed schedule tailored for the specific installation be prepared as soon as possible after the site has been selected and the equipment ordered. DIGITAL Sales Engineers will be available for advice and consultation in formulating such a schedule.

Table 5-1
Summary of Site Preparation and Installation Functions

Responsibility	Function
User	Identify space and power required for the system configuration.
User/DEC Representative	Survey the proposed site.
User/Optionally DEC Representative	Prepare site in accordance with environmental, space, and power requirements.
DEC Representative	Unpack and inventory the equipment.
DEC Representative	Install the equipment.
User/DEC Representative	Run customer acceptance test and perform preparation checks.

Milestone Chart

Every operation involved in computer system installation must be considered not only individually, but also in relation to the overall installation schedule. This can be accomplished graphically by preparing a site preparation and facilities milestone chart showing all of the necessary operations in order and assigning a starting date and a duration to each. Using this chart, progress can be reviewed frequently and action can be taken, where necessary, to ensure that the overall installation program proceeds in an orderly and timely manner.

In the case of a small computer installation, neither the schedule nor the chart will be particularly elaborate. However, some of the larger systems will demand correspondingly more preparation and a more involved chart.

The following paragraphs describe predelivery activity for what would probably represent a "worst-case" installation. Most DIGITAL computer system installations are less demanding in varying degrees.

3-6 Months Before Delivery – The Site Preparation Worksheets, which have been used in site selection to plan the layout and determine power and cabling requirements, can also be used to help determine the nature and location of structural renovations (floors, doors, walls, windows, etc.), air-conditioning facilities, electrical service, and fire protection and personnel safety features. During the period from three to six months before the scheduled delivery date, this information should be used to prepare specifications and drawings, request bids, order equipment and material, arrange for insurance coverage, and begin construction or renovation.

1-3 Months Before Delivery – As soon as the condition of the premises permits, work should begin on floors, walls, ceilings, doors, and windows, as well as on such major electrical and plumbing projects as the air-conditioning and sprinkler systems. This is also the time when telephone and other communications equipment, furniture, drapes, and similar equipment and furnishings should be ordered. Some of the data sets may entail considerable delay and should be ordered enough in advance of delivery to ensure their timely receipt.

As the interior construction nears completion, installation can begin on fire and smoke detectors, power receptacles, and lighting fixtures. Arrangements should also be made for any special rigging or other equipment that will be needed for the delivery of the computer system.

Final Month Before Delivery – During this period, support facilities such as supply and service areas should be completed and equipped, all electrical and power connections should be installed, and the interior decor (painting, plastering, finished carpentry, and decorating) should be completed. The air-conditioning system should be tested and operating before the computer system is delivered, and should be balanced as soon as possible after system installation.

Delivery Constraints – The route the equipment is to travel from the receiving area to the installation site should be studied in advance, and measurements should be taken to ensure problem-free delivery of the equipment. Among the factors to be considered are the height and location of the loading door, the size, capacity, and availability of any elevators, the number and size of the aisles and doors en route, and any restrictions, such as bends or obstructions, in the hallways. Any constraints should be reported to DIGITAL as soon as possible, so the equipment can be packed to suit the requirements of the installation site. At least one interior door should be no less than 3 ft wide and 7 ft high, and without saddles and sills, to facilitate movement of dollies.

5.3 SITE PLANNING

Adequate site planning and preparation can simplify the installation process and produce efficient, reliable system operation. For the most effective site preparation, design work should be assigned to professional engineers and architects, and construction work should be performed by qualified electrical, mechanical, and structural contractors, all supervised and coordinated by a qualified and knowledgeable representative of the customer.

Digital Equipment Corporation sales engineers and field service representatives are available for consultation regarding the objectives, course of action, and progress of the installation.

Space Requirements

Space and layout requirements will differ with each computer installation, depending upon the system selected, the intended applications, and the available physical area. The following categories of required space should be considered.

Primary – The floor area required for the computer system itself will depend upon the components selected, the length-to-width ratio of the area, and the location of walls, partitions, windows, and doors. To determine the exact area required for a specific group of components, a layout should be prepared using worksheets scaled to the measurements of the area under consideration. Operating needs will determine the precise location of free-standing peripherals, but they must be located so that the length of the connecting cables will not exceed the maximum limits permitted.

Within a system, there may be reasons that components are located in specific areas within cabinets or with respect to one another. Certain pieces of equipment should be located close to one another because of speed and timing considerations, or spread out so as not to overheat a cabinet or overload a power supply. Equipment such as disks or tapes must be located at convenient heights because of the nature of their operation.

Light levels should be such that illuminated display and readout devices and control units are visible to operating personnel. The power distribution panel for the computer system should be located in an unobstructed, well-lighted area in the computer room.

Related – Space should be provided for the daily storage of documentation, tape, cards, printed forms, etc., within the computer area. All other combustible materials such as permanent master documents, punched card records, magnetic tape, etc., should be stored in properly designed and protected areas. In locating storage areas, principal consideration should be given to minimizing the amount of space required and the travel time between related areas.

Space must also be allocated for printed forms stands, storage cabinets, card and record files, work tables, desks, communications facilities, etc. The integration of the computer work area with other associated areas and with storage areas must be taken into consideration. Work flow to and from other areas should also be considered when aisles and intermediate storage locations are planned. The central processor or other control consoles should not be placed directly on main aisles or traffic centers. If a raised floor is used for the computer area, the storage and service areas should be at the same floor level.

Similar environmental conditions should be maintained for all areas, including magnetic tape and paper tape storage areas. If it is not possible to maintain the storage area environment exactly the same as that of the computer system, adequate time must be allowed to acclimate the stored materials to the equipment environment before they are used.

In large installations where test equipment is maintained, the test equipment storage area should be within or adjacent to the computer room. Exact space requirements should be determined by the local DIGITAL Field Service Manager.

Potential – Future expansion through addition of equipment and enlargement of the computer area will dictate added electrical and air-conditioning requirements. This possibility should be considered when planning the initial site because this is the most efficient and economical time to plan for expansion.

Alternative System Configurations

Systems may be ordered under either standard or nonstandard layout plans. Standard plans provide a fixed configuration, including standard cable lengths to free-standing peripherals. Nonstandard plans contain either cabinet-mounted or free-standing peripherals that differ from DEC standard configurations.

NOTE

Nonstandard configurations are subject to approval by DEC Engineering and Field Service.

5.4 ENVIRONMENTAL PLANNING

Digital Equipment Corporation XVM Systems are noted for performing well in marginal environments. However, the operating environment of any computer system is defined by the most restrictive device of the system, usually magnetic tape and disks. Table 5-2 shows recommended system environmental ranges. Storage temperature refers to the recommended temperature limits when the system is in its operating configuration without power applied. When suitably packed for shipment, the system may be subjected to short-term storage with temperature limits of -20° F to +140° F (-30° C to +60° C) as long as no condensation occurs and rapid changes in temperature are moderated by the packing materials.

**Table 5-2
Recommended System Environmental Ranges**

Operating		Storage
Temperature	65° – 75° F (18° – 24° C)	40° – 110° F (5° – 45° C)
Relative Humidity	40 – 60%	10 – 80% (without condensation)

Maintaining close control of the environment usually results in even more reliable operation. For most DIGITAL systems, the optimum temperature is 70°F (20°C) and the optimum relative humidity is 50 percent.

Low humidity allows static electricity to build up, while lack of air cleanliness results in dust that reduces tape life and leads to excessive head wear and early data errors in all moving magnetic storage media (drums and disks).

Vibration can also cause slow degradation of mechanical parts and, when severe, may cause errors on disks and drums.

Hardware logic errors can be caused by high-power radio frequency pulses conducted through power mains or radiated through space. Such pulses could come from nearby radar installations, broadcasting stations, or welding operations, from the arcs that occur when static electricity is discharged, or from arcing relay or motor contacts.

Air Conditioning

The ideal computer room air-conditioning system should be able to heat the room with all equipment off, cool the computer when fully powered and active on the warmest day expected, and humidify or dehumidify to within predetermined parameters under all anticipated weather conditions.

Room construction can be a major factor in attempting to air-condition an area. Insulation of ceilings and walls reduces operating costs by increasing the efficiency of the system. As a result, metal walls and partitions are not recommended unless their conditioned surfaces are insulated. Windows and doors should be weather-tight, with double glass recommended for large window areas. Slow-operating mechanical door-closers should not be used.

DIGITAL computer systems are air-cooled, with the cooling air circulated internally by blowers in each unit. The airflow pattern varies slightly from one unit to another, but generally air enters standard cabinets through a filter and blower in the top of the cabinet and exits through the bottom. In short cabinets, air enters through a filter and blower at the bottom of the unit and exits at the top rear.

For efficient equipment cooling, a minimum clearance of 30 inches (76 cm) above the equipment cabinets is recommended. If this requirement cannot be met, other means of allowing the free flow of air above and around the equipment must be devised.

To determine approximate cooling requirements for the entire system, add the heat dissipation figures for all of the components, and then adjust the total to allow for such factors as the number of personnel, heat radiation from adjoining areas, sun exposure through windows, system efficiency, and potential expansion. It is advisable to allow a safety margin of at least 25 percent above maximum estimated requirements.

NOTE

Long-term reliability of the air-conditioning system can be adversely affected by powering up and down daily. If possible, it is recommended that the system be left on.

Air Filtration

High-efficiency mechanical filters will generally suffice unless the installation is subjected to corrosive gasses, salt air, or other unusual conditions. If these conditions exist, an air-filtration specialist should be consulted.

Storage of Supplies

Sufficient storage facilities must be provided for magnetic tape, disk cartridges, punched cards, line printer paper, and any other necessary supplies in an environment roughly comparable to that of the overall system. In addition, such supplies should be stored in a closed cabinet to eliminate contamination by foreign matter.

Magnetic Tape and Disk Cartridges – Tape and disk cartridges should be protected from rough handling, magnetic fields, dust, and extremes of temperature and humidity, all of which can have adverse effects on performance. They should be stored in fire-resistant cabinets away from magnetic fields, and kept in their original dustproof containers when not in use.

The storage area should be held between 60°F and 80°F (15°C and 27°C) with a relative humidity of from 40 percent to 55 percent. Tape subjected to extremes beyond these ranges should be allowed 24 hours to reach equilibrium with the computer room before use.

Punched Cards – Punched cards, like any paper or card stock, are affected by variations in temperature or relative humidity, especially the latter. For this reason, cards should not be stored near heated pipes, radiators, air ducts, or windows, where abrupt environmental changes are likely to occur.

Line Printer Paper – One leading manufacturer recommends that line printer paper be stored at 75°F (24°C) with a nominal relative humidity of 45 percent. Recommended operating ranges include temperatures from 60° to 85°F (15° to 30°C) and humidity from 40 to 60 percent.

Radiated Emissions

Sources of radiation such as broadcast stations, vehicle ignitions, and radar transmitters located in proximity to the computer system may affect the operation of the processor and the related peripheral equipment. The effects of these emissions can be reduced by taking the following precautions:

1. Grounding window screens and other large metal surfaces.
2. Shielding interconnection cables with grounded shields.
3. Providing additional grounding to the system cabinets and chassis.
4. In extreme radiation environments, providing a grounded cage for the system.

Disk packs must be shielded from magnetic fields. A magnetic field with an intensity of 50 oersteds might destroy all of the information on an individual disk pack.

Altitude

Computer system operation at high altitudes encounters problems with heat dissipation. Systems operated at altitudes above 2000 m (7000 ft) may require additional internal blowers for adequate cooling. Disk subsystems have a maximum altitude specification of 3500 m (12,000 ft).

If operation at high altitudes is anticipated, DIGITAL should be notified when the equipment is ordered.

Static Electricity

Static electricity can be an annoyance to operating personnel and can, in many cases, affect the operational characteristics of the processor and related peripheral equipment. The two major contributors to static electricity in computer installations are floor covering material and furniture.

Floor covering material can contribute to the buildup of high static electrical charges through the motion of people, carts, furniture, etc., in contact with it. All raised metallic flooring, including metal panels, should be grounded. Whatever tile or other surface material is used to cover the floor should have a surface resistance of 0.5 megohms (minimum) to 20,000 megohms (maximum) at operating limits of 20 to 80 percent relative humidity and temperatures from 60°F to 90°F (15°C to 32°C).

Use of carpeting in a computer room is discouraged unless the carpet can meet the same requirements as tile covering.

Cloth-covered chairs are normally less susceptible to the generation of static charge than plastic-covered chairs. Rubber or other insulating feet for furniture should be avoided. If casters or ball bearings are used, they should be lubricated with a graphite or other conductive grease. Casters or wheels with rubber tread should contain conductive material.

Lighting

The recommended light intensity in the computer room area should be in the neighborhood of 60 footcandles (650 lumens/m²) measured at desk level, approximately 30 inches (76 cm) above the floor. This intensity is sufficient for general work in the area. In the areas immediately surrounding cathode ray devices, illumination should be reduced to 40 footcandles (430 lumens/m²). Direct sunlight should be avoided. The design and position of the lighting fixtures, which must be free from glare, should consider that personnel will be operating equipment and reading indicators.

Fluorescent lighting is popular for computer installations because it generates little heat, yet illuminates the work area evenly. The lights for general illumination should be sectionally controllable by switches, i.e., should not be powered from the computer power distribution panel, so that portions of the lighting can be turned off as desired.

Even where not required by code, some type of emergency lighting should be provided to protect personnel and equipment against a sudden lighting failure.

Windows that do not face north (in the Northern Hemisphere; south in the Southern Hemisphere) should be fitted with venetian blinds, glazed with tinted glass, or treated with protective material against sunlight.

Cleanliness

Although cleanliness is important to all computer installations, it becomes a crucial consideration in many cases. Figure 5-1 shows the degree of cleanliness required for RK05 disk drive read/write heads, for example, which "fly" on a 100 μ in film of air (air bearing).

5.5 ELECTRICAL PLANNING

The available supply of power should be adequate to handle not only the power loads represented by the computer system, but also any loads that are likely to be imposed by future expansion. The electrical system must conform to applicable national and local codes and ordinances.

A separate power transformer for the computer installation is desirable. Where this is not possible, the power mains for the computer system should not be used for any heavy variable loads of the sort generated by electric motors, air-conditioning systems, etc.

The feeder supplying power to the computer system should be protected by a mainline circuit breaker, accessible to operating personnel. The circuit breaker may be remotely operated, with remote controls placed near the main exit door. A light should indicate when power is on.

Voltage ranges can also be critical. Table 5-3 shows the 5, 10, and 20 percent limits for the most common voltages, rounded up for +, down for -.

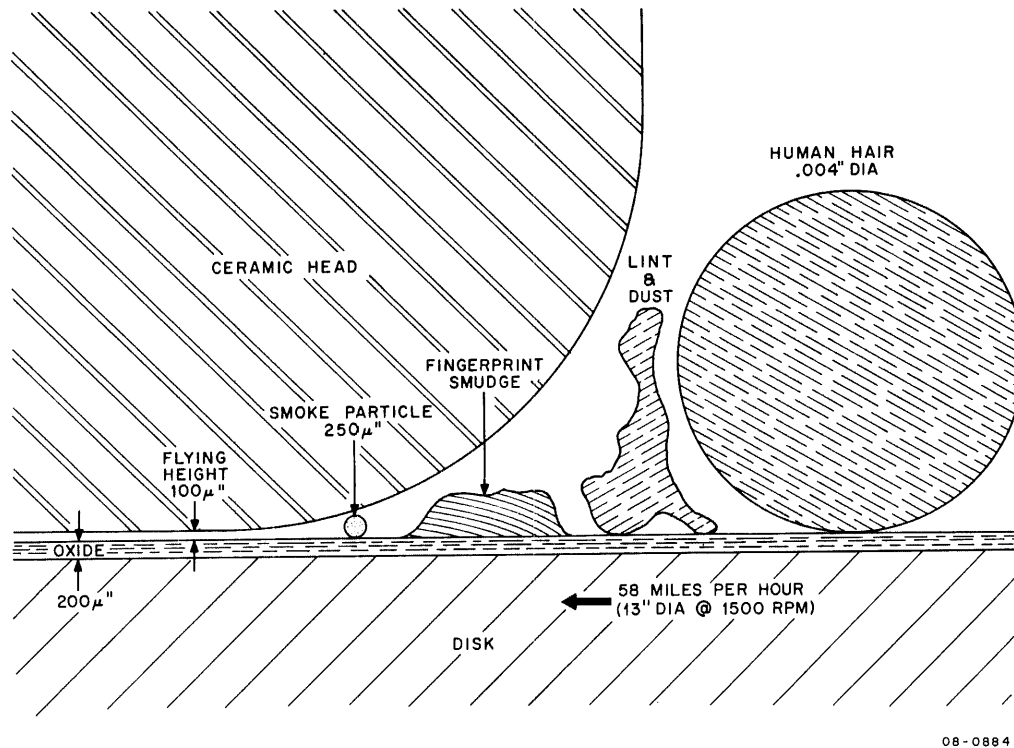


Figure 5-1 Relationship of Disk Head, Disk, and Contaminants

Table 5-3
Voltage Ranges

-20%	-10%	-5%	Nominal Voltage	+5%	+10%	+20%
80	90	95	100	105	110	120
84	94	99	105	111	116	126
88	99	104	110	116	121	132
92	103	109	115	121	127	138
96	108	114	120	126	132	144
102	114	121	127	133	140	152
120	135	142	150	158	165	180
176	198	209	220	231	242	264
184	207	218	230	242	253	276
192	216	228	240	252	264	288

Power Control System

The power control system used on Digital Equipment Corporation computers and components depends on input power that is normally single-phase 115 Vac or 30 Vac, $\pm 10\%$, 47 to 63 Hz, except for the power controller in the XVM Processor bay and memory expansion bay and the RPR02- and RP03-type of disk-pack drives, which require three phase (208 V or 415 V) power.

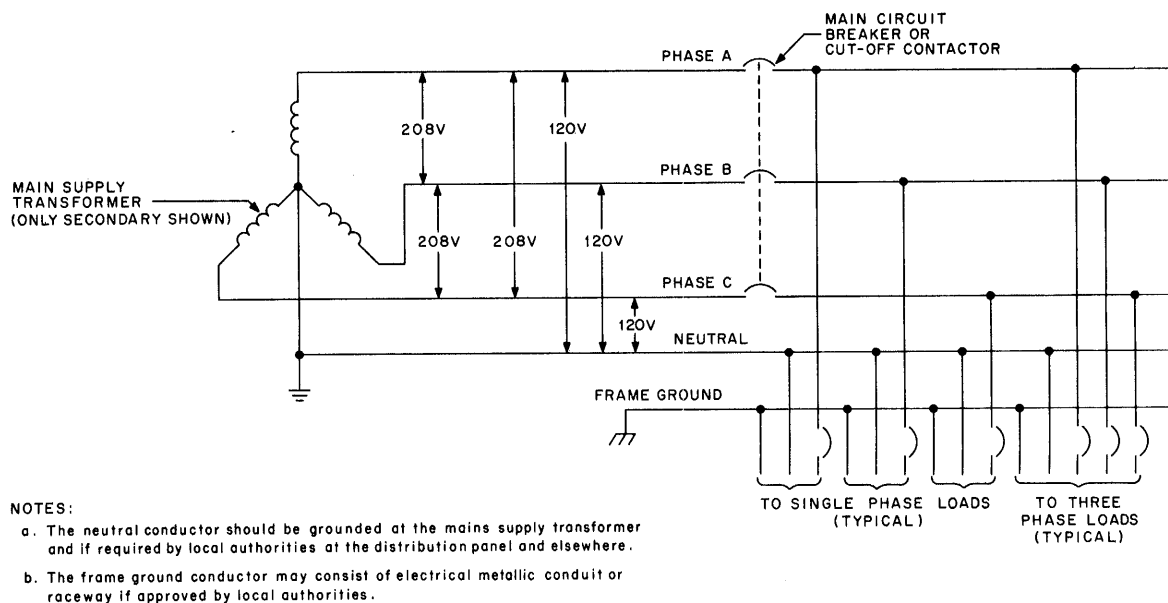
Cabinet Power Control – The cabinet power control is used in systems consisting of peripheral equipment or memory. It is operated from a remote control switch and is designed to switch and to distribute up to 24 A of 115 Vac or 16 A per phase or 230 Vac to outlets located within the cabinet. Eight outlets provide switched ac and four outlets provide unswitched ac for operating devices.

Every cabinet contains a power control, so that only one ac cord has to leave the cabinet.

Power Control Bus Cable – The power control bus cable interconnects all devices in the system. Other devices may be added to the system through connection to the bus in parallel at any convenient point. The number of power controls that can be added to any system is limited only by the amount of current that the master switch can handle. Each power control will cause 10 mA maximum to flow through the master switch. No terminators are required on the bus, and “T” connections may be made without any restrictions.

Power control bus cables may be standard 3-wire cables (joining two 3-wire male Mate-N-Lok connectors) or cables with special wiring used to connect earlier type 841B or 841C power control units into the power control system. The 841B or C requires 115 V or 230 V ac on its control bus before it connects the main power to the power supplies. The 841 Power Control Unit is standard on PDP-15 Systems.

Power Requirements, 60 Hz Systems – DEC 60 Hz systems operate from a 115/230 Vac $\pm 10\%$, 60 Hz $\pm 2\%$, 3-phase, Y-connected, 4-wire plus ground power system containing single-phase (115 Vac) and 3-phase (230 Vac phase-to-phase) loads. Figure 5-2 shows a typical 60 Hz power system.



10-0865

Figure 5-2 60 Hz Power System

The manner in which ac power requirements can vary from component to component is indicated by the following examples:

1. Some devices require an input of 115/230 V $\pm 10\%$, 60 Hz $\pm 2\%$, 3-phase, 4-wire plus ground and are supplied with a NEMA L21-30P, which mates with a NEMA L21-30R. A 20 A circuit is recommended for this type of service. Phase rotation sequence should be A-B-C or X-Y-Z.
2. Other devices require an input of 115 V $\pm 10\%$, 60 Hz $\pm 2\%$, single-phase, 2-wire plus ground, and are supplied with a NEMA L5-30P plug, which mates with a NEMA L5-30R receptacle. A 30 A circuit is recommended for this type of service.
3. Some smaller devices require an input of 115 V $\pm 10\%$, 60 Hz $\pm 2\%$, single-phase, 2-wire plus ground, and are supplied with 3-wire cord for use with all standard 3-wire, grounding-type convenience outlets. A standard appliance circuit is recommended.

In most systems it is convenient to provide one or more separate load centers or breaker panels for the computer, and to connect each 20 A or 30 A receptacle to its own circuit breaker, supplying single-phase receptacles from phase to neutral connections. Each circuit breaker should be rated for 30 A, 115 Vac (or 15 A, 230 Vac) even though the average current drawn is less than half of those amounts (15 A for 115 Vac, 7.5 A for 230 Vac).

A 25-ft (7.5 m) ac power cord is provided with most individual components, and is routed through the bottom of the cabinet to the power receptacle via a cable access hole.

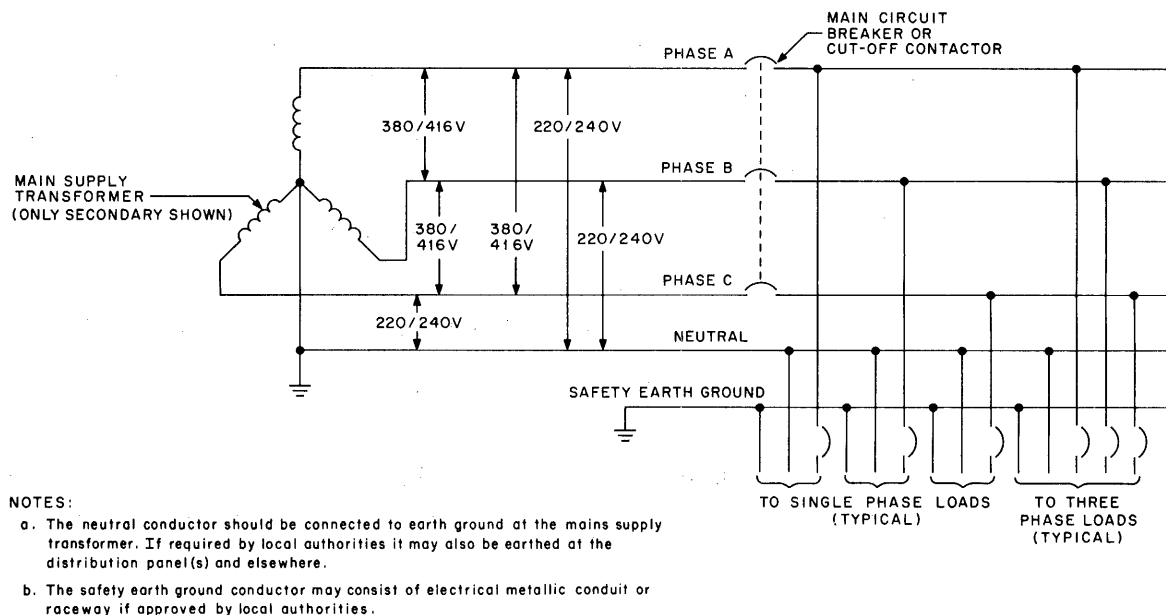
For details regarding grounding procedure, refer to Paragraph 5.5.

Power Requirements, 50-Hz Systems – DEC 50 Hz systems operate from 230/400 V $\pm 10\%$ 50 Hz $\pm 2\%$, 3-phase, Y-connected, 4-wire plus earth ground power mains providing single-phase (230 V) and 3-phase (400 V phase-to-phase) loads. Other main supply voltages can be accommodated upon request.

Figure 5-3 shows a typical 50-Hz power system. The following examples show how those requirements can vary from one component to another:

1. Some devices require an input of 230/400 V $\pm 10\%$, 50-Hz $\pm 2\%$, 3-phase, 4-wire plus ground, and are supplied with a 5-terminal pressure connector block. Plugs and receptacles are not supplied by DIGITAL. A 10 A circuit is recommended for this type of service. Phase rotation sequence should be A-B-C.
2. Other devices require an input of 230 V $\pm 10\%$, 50 Hz $\pm 2\%$, single-phase, 2-wire plus ground, and are supplied with a 3-terminal pressure connector block and 25 ft (8.2 m) of 3-conductor wire. Plugs and receptacles are not supplied by DIGITAL. A 15 A circuit is recommended for this type of service.
3. Plotters and other small devices require an input of 230 V $\pm 10\%$, 50-Hz $\pm 2\%$, single-phase, 2-wire plus ground, and are supplied with DEC part number 90-08853 plugs (Figure 5-4). During equipment installation, these plugs may be replaced by plugs which fit local outlets. A standard appliance circuit is recommended for these devices. (The console device plugs into the processor and does not require a receptacle.)

In most systems, it is convenient to provide a separate load center or circuit breaker panel for the computer, and to connect each 10 A or 15 A receptacle to its own circuit breaker, supplying single-phase receptacles from phase to neutral connections.



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Figure 5-3 50 Hz Power System

Power Source

Computer equipment requires a power source with minimum voltage and frequency disturbances. Line voltage disturbances greater than $\pm 10\%$ from nominal and of a duration greater than $1/4$ cycle (measured at the receptacle during system operation) are undesirable. Unstable frequencies, where local power may drift several Hertz away from nominal, may cause wobble of up to 0.4 mm (0.015 in.) or more, in the pictures of raster-scan cathode-ray tube displays.

Power Wiring (ac)

DIGITAL power wiring conforms to Underwriters Laboratories, Inc., Handbook U.L. No. 478, National Electrical Code (NFPA 70) standards, and the Type II Requirements of the National Fire Protection Association. This means that in the United States the wire used as equipment ground is green; it carries no load current (except in emergency), but does carry leakage current. No equipment is permitted to leave DIGITAL that does not have a grounding connection to its frame.

The grounded conductor (also called the "identified" conductor, neutral, common, ac return, cold lead, etc.) is light grey or white. It must not be used to ground equipment, as its purpose is to conduct current.

Lines 1, 2, and 3 are represented by black, red, and orange wires, respectively, and phase rotation is in that order.

NOTE

On single phase cables, the power lead (or hot, etc.) is black. This conflicts with some countries' wiring codes. The black conductor is used as neutral in some countries.

Primary Power Receptacles

The type of primary power receptacles used depends largely on the requirements of the country in which the system is being installed. In the United States, power lines should terminate, where possible, in National Electric Manufacturers Association (NEMA) receptacles to be compatible with the NEMA plugs supplied with most DIGITAL equipment. Waterproof power receptacles, and connectors, should be used under false floors.

Figure 5-4 details each of the approved electrical plugs and receptacles together with the NEMA designation and the DEC part number.

To facilitate plug and cord replacement in the field, equipment designed for greater than 12 A service is provided with terminals for solderless power connections and shipped with 12 A convenience plugs, which require receptacles NEMA 5-15R (120 V) and NEMA 6-15R (240 V).

Separately fused and switch-controlled ac convenience outlets should be provided for test equipment used in maintenance tasks. The outlets should be situated near the system and its related equipment, and should be installed at approximately 10-ft intervals. In the United States, service receptacles should be NEMA 5-15R.

Ground Requirements

A system involving a digital/analog interface usually requires that the digital system ground be tied to the analog system ground at a single point, often at the analog/digital interface. A low-resistance ground connection is required in such cases. Systems involving no analog interface may require no more than the grounding provided by a large electrical conduit, although electrical conduit systems are often poorly connected in terms of a low-resistance path to ground.

Each cabinet of a DIGITAL computer system is equipped with ground lug terminals which should be connected to a low-resistance earth ground by No. 4 AWG (5 mm, 0.20 in.) copper wire or stranded No. 4 AWG welding cable. A Burndy QA4C-B solderless lug (or equivalent) is recommended for terminating the cable. DIGITAL supplies a standard grounding conductor with each I/O and memory cabinet.

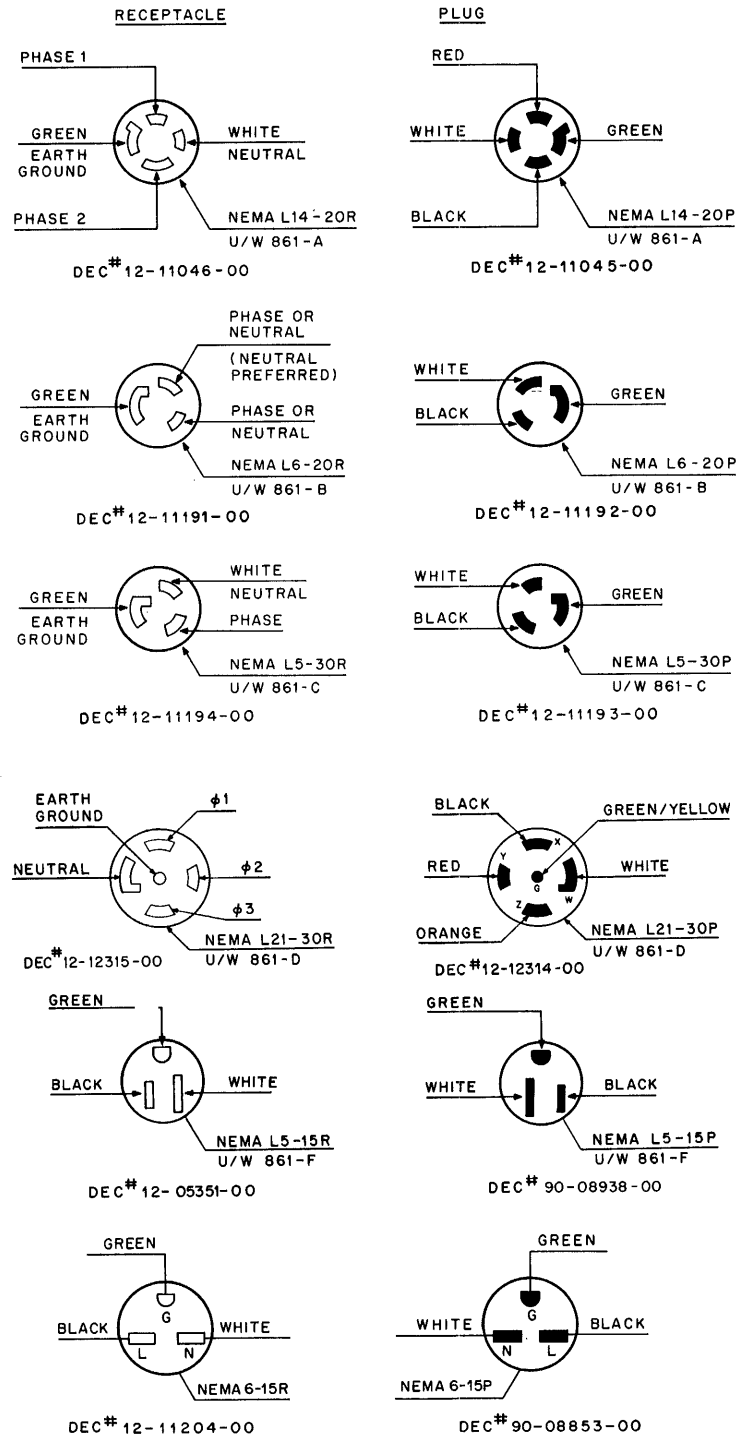
A large water pipe or a steel building beam is adequate in many instances, but some of the larger systems may require additional connections to earth ground, over and above the ground leads carried through the various signal buses and the ground conductors contained in the power cables.

Whenever possible in the larger systems, the system power panel must be mounted in contact with bare building steel by bonded joints or connected to it by a short length of cable. An adequate ground can be made by driving a metal rod 1.5 cm (0.625 in.) in diameter or larger into earth that is permanently moist to a depth of at least 12 ft (3.5 m), or by burying a metal plate or grid with an area of at least 16 ft² (1.6m²) in permanently moist earth.

Whatever grounding system is used, it must provide less than 10 ohm impedance to moist earth from dc to 10 MHz. It must also be isolated from electrical noise sources to prevent electrical noise from being transmitted into the system via the grounding system.

When two cabinets are bolted together, DIGITAL bonds them electrically by a No. 4 AWG conductor (0.20 in., 5 mm) or by several copper mesh straps connected between the two cabinet frames. Auxiliary units such as line printers or card readers may be grounded to their associated control cabinets with No. 4 AWG copper wire.

After the grounding system is completed, it is advisable to take a voltage reading from the computer frame to the nearest grounded metal object before touching the computer.



15-0861

Figure 5-4 NEMA Plugs Supplied with Digital Equipment Corporation's Products

Operational Considerations

Daily powering up and down of a computer system is detrimental to long-term reliability. Where proper safety devices exist, it is recommended that the system remain powered up, with the computer stopped and peripherals placed off-line when not in use.

5.6 COMMUNICATIONS

Communications data sets may be used with communications systems. They should be located near communications interface hardware, and away from noisy equipment such as printers or punches.

If the data sets are to be supplied by the customer, they should be ordered well in advance of the installation date, as the delay between ordering and installing data sets may vary from two weeks to two years, depending upon the model and the supplier.

Before the system is installed, synchronous data circuit installations should be tested in full duplex operation. Digital Equipment Corporation's Field Service organization may be of assistance in such performance verification.

EIA/CCITT Standards

Commercial standards for carriers and data communications and terminal equipment manufacturers are defined in EIA Standard RS-232C, prepared by the Electronics Industries Association. The Comité Consultatif International de Telephonie et Telegraphie (CCITT) publishes similar standards for European data communications users. Equipment for transmitting or receiving data over voice-grade lines normally conforms to EIA RS-232C and CCITT recommendations.

20 mA Loop Current

Because they are suitable for a wide range of applications, currents in the vicinity of 20 mA are frequently used for transmission of binary serial data. Connections are usually made by means of Mate-N-Lok connectors (Figure 5-5). The computer interface normally includes a module with a female connector; the terminal cable normally terminates in a male connector.

5.7 UNPACKING

Based on the terms and conditions of sale, it may be necessary for a Digital Equipment Corporation representative to unpack and install certain equipment at the computer site, and perhaps even to perform customer acceptance tests. In such cases, the customer must not attempt to unpack or install the system or equipment without prior approval from Digital Equipment Corporation, as this would invalidate the DIGITAL warranty.

WARNING

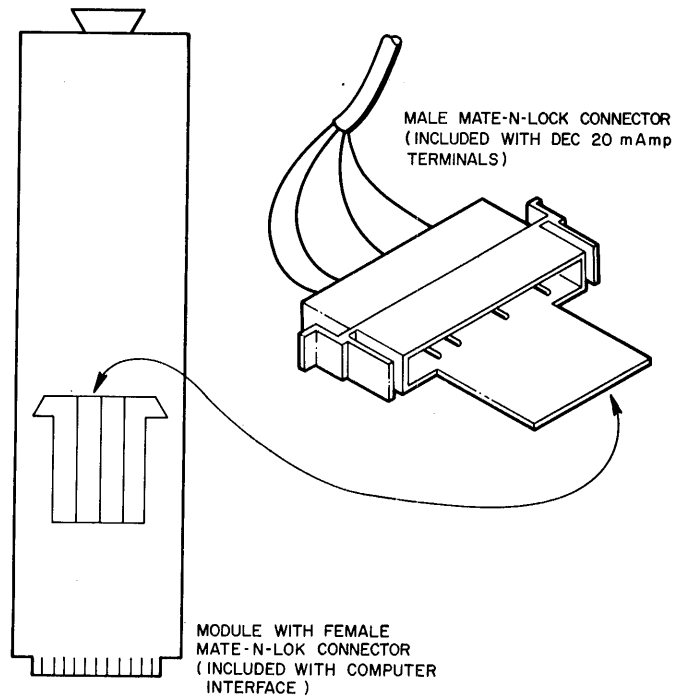
Do not attempt to install the system until DIGITAL has been notified and a Field Service Representative is present.

Unpack the equipment using the following procedures:

1. Remove the outer shipping container.

NOTE

The container may be either heavy corrugated cardboard, plywood, or simply a polyethylene covering depending upon travel requirements. In either case, remove all metal straps first, and then remove any fasteners and cleats securing the container to the skid. If applicable, remove the wood framing and supports from around the cabinet perimeter.



11-1578

Figure 5-5 20 mA Mate-N-Lok Connector

2. Remove the polyethylene cover from the cabinets.
3. Remove the tape or plastic shipping pins, as applicable, from the cabinet(s) rear access door(s).
4. Unbolt the cabinet(s) from the shipping skid. Access to the bolts, located on the lower supporting siderails, is facilitated by opening the access door(s). Remove the bolts.
5. Raise the leveling feet above the level of the roll-around casters.
6. Use wooden blocks and planks to form a ramp from the skid to the floor and carefully roll the cabinets onto the floor.
7. Roll the system to the proper location for installation.
8. If applicable, repeat Steps 1 through 8 for the remaining system cabinets.
9. When the cabinets are oriented properly, follow the procedure of Paragraph 5.9 to install the cabinet(s).

5.8 INSPECTION

After removing the equipment packing material, inspect the equipment. Report any damage to the local DIGITAL sales office. Inspection procedures are as follows:

1. Inspect the external surfaces of the cabinets and related equipment for surface, bezel, switch, and light damage, etc.

2. Remove the shipping bolts from the rear door and open the rear door of the cabinet. Internally inspect the cabinet for console, processor, and interconnecting cable damage; loose mounting rails; loose or broken modules; blower or fan damage; loose nuts, bolts, screws, etc.
3. Inspect the wiring side of the logic panels for bent pins, cut wires, loose external components, and foreign material. Remedy any defects found.
4. Inspect the power supply for the proper seating of fuses and the proper seating of power-connecting plugs.

5.9 CABINET INSTALLATION

The XVM Cabinets are provided with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). Cabinet installation procedures are as follows:

NOTE

In multiple cabinet installations, receiving restrictions may necessitate shipping cabinets individually or in pairs. In such cases, the cabinets are connected at the installation site.

1. With the cabinets positioned in the room, install the filler strips between cabinets. Remove the 4 bolts securing the front and rear filler strips, butt the cabinets together, hold the filler strips in place, and rebolt through both cabinets and the filler strips (Figure 5-6). Do not tighten the bolts securely at this time.
2. Lower the leveling feet, making sure that the cabinet(s) are not resting on the roll-around casters but are supported on the leveling feet.
3. Level all cabinets with a spirit level and ensure that all leveling feet are seated firmly on the floor.
4. Tighten the bolts that secure the cabinet groups together and then recheck the cabinet leveling. Again ensure that all leveling feet are seated firmly on the floor.
5. Remove the shipping bolts and tape from the slide runners of the reader/punch assembly.

5.10 PERIPHERAL EQUIPMENT INSPECTION

All peripheral equipment should be inspected for internal and external damage. This includes inspection of magnetic tape and DECTape transport heads, motors, paper-tape sprockets, etc.

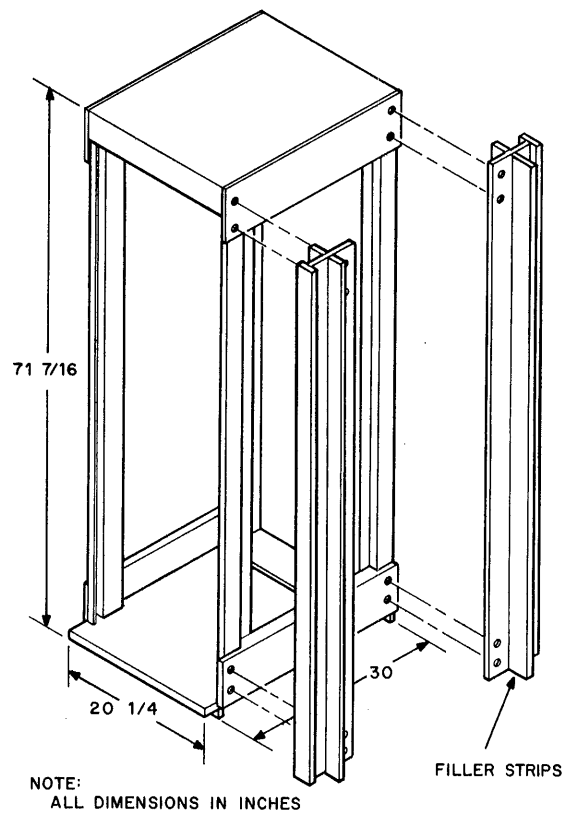
CAUTION

Do not operate any peripheral device that employs motors, tape heads, sprockets, etc., if they are damaged.

5.11 ELECTRICAL AND MECHANICAL SPECIFICATIONS

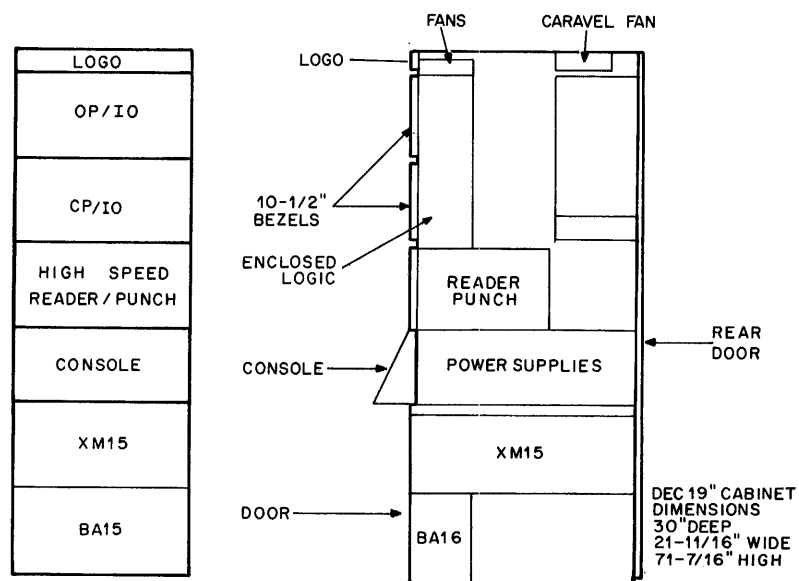
Figures 5-7 through 5-11, and Tables 5-4 and 5-5 provide mechanical and electrical specifications which are useful when planning the installation of an XVM System. Additional installation information is contained in the various manuals supplied with the system.

Table 5-6 provides cable lengths for optional peripheral equipment. For I/O bus cabling information refer to print XV100-0-2.



18-0098

Figure 5-6 Cabinet Bolting Diagram



15 - 0013

Figure 5-7 XVM Basic Configuration

	BAY 06 L	BAY 05 L	BAY 04 L	BAY 03 L	BAY 02 L	BAY 01 L	BAY 00	BAY 01 R	BAY 02 R	BAY 03 R	BAY 04 R	BAY 05 R	BAY 06 R	BAY 07 R	BAY 08 R	BAY 09 R	BAY 10 R
1st PDP-11 OPTION CABINET	RS09 8	RS09 5	RF15 SEE NOTE 4	INDICATOR	BLANK	DR15 C	XVM KP 15-C CENTRAL PROCESSOR	IND TC15 IND FP15	BLANK	SEE NOTE 1	BLANK	INDICATOR	INDICATOR	INDICATOR	BLANK	BLANK	TU10
				INDICATOR								BLANK	INDICATOR	BLANK	AFC 15 SEE NOTE 3	UDC15 SEE NOTE 3	
				RP15 - SEE NOTE 4	MEMORY BA11-K	RK05 2	H.S.READER /PUNCH	TU56 #3 SEE NOTE 2	BLANK		AD15	LP15	VT15 A	BD15	BLANK	BLANK	
	RS09 7	RS09 4	RS09 2			RK05 1		TU56 1	TU56 4		BLANK	CR15			SCREW TERMINAL CONNCTORS		
				FANS		PDP-11	CONSOLE KC15-C	TU56 2	TU56 3		DW15	BLANK	BLANK	VT15 B	BLANK	BLANK	
	RS09 6	RS09 3	RS09 1														
	FAN/ FILTER SYSTEM	FAN/ FILTER SYSTEM	FAN/ FILTER SYSTEM	BLANK	MEMORY BA11-K		XM15	TC15	BLANK		TC59	AA15				BLANK	VT15 B
					BLANK	BA11 (RK11-E, etc)	BA15	POWER SUP. H721				POWER SUP. H721	POWER SUP. H721				
											BLANK	POWER SUP. H721	POWER SUP. H721		POWER SUP. H721	POWER SUP. H721	POWER SUP. H721
SURGE /NORMAL BTU /HR LBS /KKG	14 / 6.5 2542 420 / 190	14 / 6.5 2542 420 / 190	23 / 8.5 3324 600 / 270	25 / 7 2737 NOTE 6	325 / 16 6256 NOTE 6	41 / 14.A 5630 460 / 211	375 / 18 7038 600 / 271	2017 2737 NOTE 6	18 / 6 2346 NOTE 6	11 / 3. 5 — NOTE 6	30 / 12 4672 NOTE 6	30 / 12 4672 NOTE 6	18 / 6 2346 NOTE 6	30 / 12 4692 NOTE 6	30 / 12 4692 NOTE 6	30 / 12 4692 NOTE 6	

- Notes:
1. Options LT19, DP09, XY15 or and the DB09 and DB08 are located in available space in the H963-J cab. Order of preference is TC59, LT19 DP09 etc. placed in the order listed above from bottom to top. In the event that all options are included a second cab. is required.

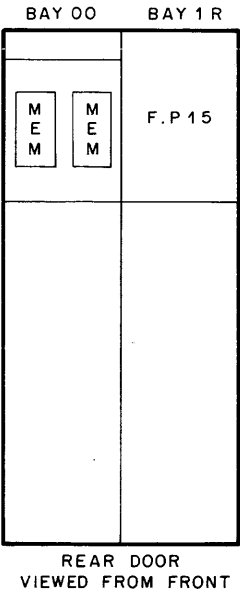
2. If four TU56's are ordered, TU56 #3 and #4 are installed in second cab. as shown.

3. AFC-15 and UDC-15 cabinets could be a max of 11UDC and 11AFC cabinets each to meet the requirements of the customer.

4. If extensive system is installed , disk system (RF15 and/or RP15) cabinets may be physically separated and repositioned at installation to maintain cable lengths.

5. Bay 2L is required only to expanded beyond 96K for MF15 memory or 72K of ME15 memory.

6. When weights are unknown, usage of an average cabinet weight of 500 lbs./178 kg is recommended (800 lbs./284 kg is considered maximum worst case.)

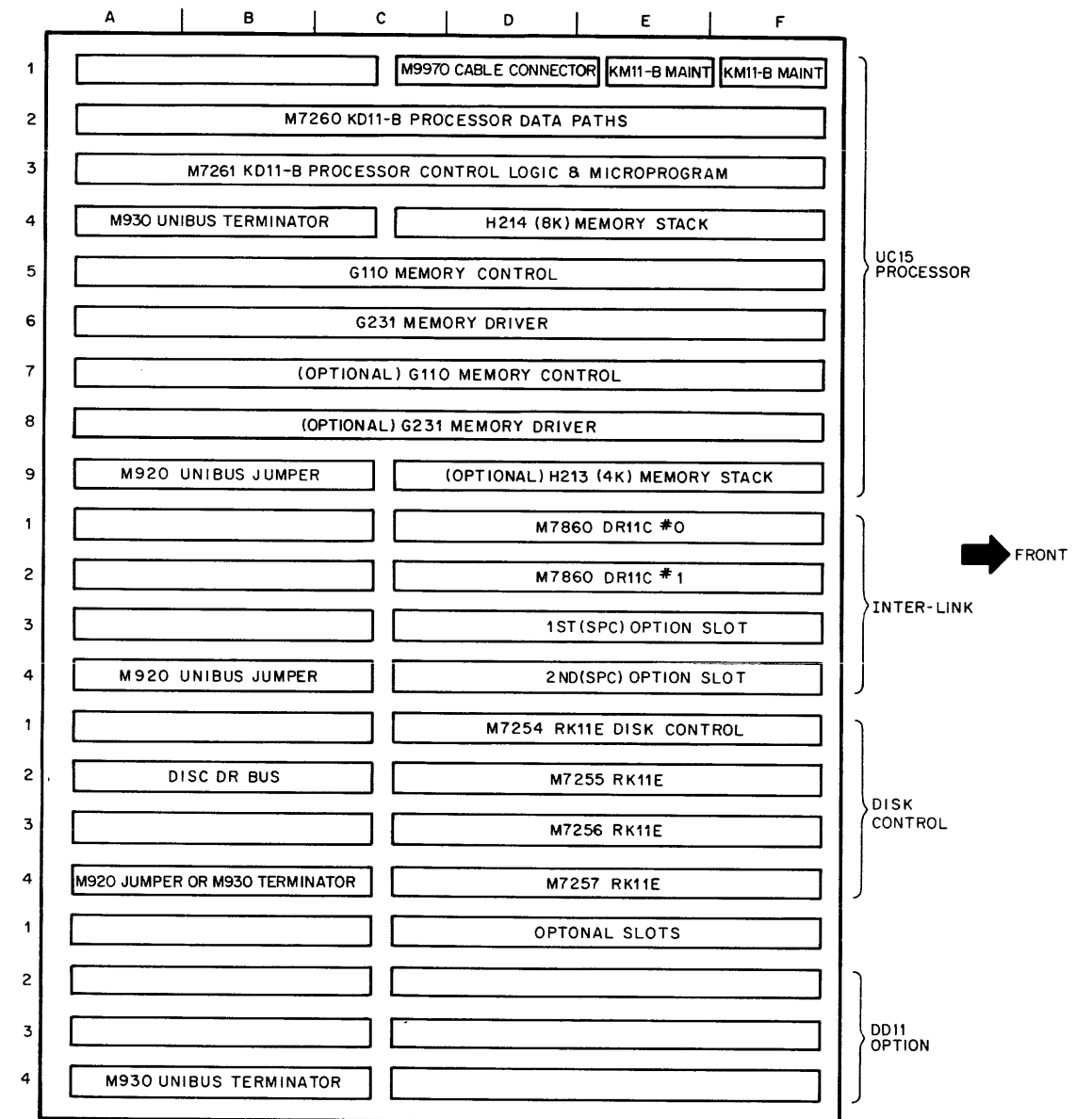


- Note:
- Rear door of Bay 00 may contain:
1. Up to 64k of MF15 Memory

2. Up to 48k of ME15 Memory

3. Up to 24kof ME15 and 32K of MF15 Memory

Figure 5-10 System Configuration Diagram



15-0853

Figure 5-11 Peripheral Processor Configuration Guide (PDP-11/05-NC version)

Table 5-4
Cabinet-mounted Options

Option	Description	Ht (in.)	Wt (lb)	Amps at 115 Vac		Heat (Btu/hr)	Power (W)
				Run	Surge		
TC15	DECtape Control	15.75	38	0.8	4.0	327	96
TC59-D	Magtape Control	21.0	50	2.0	5.0	784	230
BA15	I/O Bus Expander	5.25	13	2.0	5.0	1000	230
DW15-A	I/O Bus Converter	5.25	16	0.6	3.0	112	33
FP15	Floating Point Arithmetic	21.0	150	18.0	35.0	13650	4000
PC05	H.S. Reader/Punch	10.5	60	3.0	9.0	1040	306
XY15	Plotter Control	5.25	16	1.5	4.0	600	180
CR15	Card Reader Control	5.25	16	0.6	4.0	286	82
LT19-D	Terminal Controller	10.5	25	2.0	5.0	47	14
LT19-E	Terminal Unit (max 5)	—	2	2.0	5.0	51	15
DC01-ED	Terminal Control	10.5	22	1.1	4.2	410	115
DP09-A	Asynchronous Data Control	10.5	25	0.7	4.0	253	75
DB09-A	Interprocessor Buffer	10.5	25	0.8	5.0	333	97
AA15	D-to-A Max Control	10.5	22	0.6	3.0	95	28
TU56	DECtape Transport	10.5	80	3.0	9.0	1900	350
RF15	DECdisk Control	10.5	150	5.0	12.0	1955	575
RS09	DECdisk Drive (each) ²	15.75	100	1.5	9.0 ¹	585	172
AD15	A-to-D Converter	21.0	40	1.0	3.0	342	100
ADF15	A-to-D Converter	21.0	40	1.0	3.0	342	100
RP15	Disc Pack Control	21.0	55	7.0	25	2747	805
VT15-A	Graphics Processor	21.0	50	3.0	9.0	2346	690
BD15	Industrial Control	10.5	26	2.0	7.0	306	98
AFC15	Auto-flying Cap ³	—	—	12.0	30.0	1700	500
UDC15	Univ. Digital Control ³	—	—	12.0	30.0	1700	500
LP15-V	Line Printer Control	10.5					
TU10-E	Magnetic Tape Drive	26.0 ⁴	150	3.0	5.0	3400	1000
CA15-A	CAMAC Control	21.0	83	9.0	28.0	986	241
NP15	Nuclear Interface	10.5	39	1.8	55.0	322	103
LS15	Line Printer Control	5.25	24	0.6	2.5	250	762

Notes: ¹ This is starting current. Disk is rarely switched off.
² If more than one full disc drive, start only one motor at a time.
³ Applies to one cabinet. Installation may include up to 11 cabinets.
⁴ Applies to tape unit only. Normally supplied in standard cabinet.

Table 5-5
Current Free-Standing Peripherals

Designation	lb/kg	H × W × D <u>in.</u> cm	Surge/Normal Amps	Btu/hr	W (Max)
CR04D	100/45.4	$\frac{17 \times 24 \times 19}{34 \quad 61 \quad 48}$	12/4	1600	1500
CR04F	70/31.8	$\frac{13 \times 20 \times 15}{33 \quad 50 \quad 38}$	10/3.5	1500	1400
LP05	340/154.5	$\frac{45 \times 32 \times 22}{112 \quad 80 \quad 55}$	/4.5	1800	700
LA36	102/45.9	$\frac{33.2 \times 27.5 \times 24}{83 \quad 68.7 \quad 60}$	/2.6	1000	300
LS01	155/70		5/1.8	700	210
LV01	160/73	$\frac{38 \times 19 \times 18}{95 \quad 47 \quad 45}$	15/5.2	2040	600
RP02	295/133	$\frac{40 \times 30 \times 24}{102 \quad 76 \quad 60}$	25/6	4250	700
RP03	415/190	$\frac{40 \times 30 \times 24}{102 \quad 76 \quad 60}$	30/6	3800	700
VT01	51/23	$\frac{12 \times 12 \times 22}{30 \quad 30 \quad 57}$	/2	800	250
VT04	260/118	$\frac{52 \times 21.5 \times 48.5}{132 \quad 55 \quad 122}$	14/7	2730	800
VT05					
VT07	300/136	$\frac{52 \times 29 \times 46}{132 \quad 72 \quad 116}$	15/8	3120	920
VT50	43/19.4	$\frac{14 \times 21 \times 27}{36 \quad 53 \quad 69}$	/1	390	110
XY15A	33/15	$\frac{9.75 \times 18 \times 14.7}{25 \quad 45 \quad 37}$	3/1.5	595	175
XY15B	53/24	$\frac{9.75 \times 39.4 \times 14.7}{25 \quad 100 \quad 37}$	3/1.5	626	184

Table 5-6
Optional Peripheral Equipment Cable Lengths

Peripheral Equipment		Cable Length* ft/m	
		Standard	Maximum
Mass Storage Devices			
TC15	DECtape control for up to 4 TU56 Dual DECtape Transport Units		
TU56	Dual DECtape Transport	4/1.2	15/4.5
TC59D	Magnetic Tape Transport Control for up to 8 TU20B, TU20A, TU30B, TU30A Magnetic Tape Transport Units		
TU10F	7-Track, 45 ips Magnetic Tape Transport 200, 556 and 800 bpi	10/3.048	100/30.48
TU10E	9-Track, 45 ips Magnetic Tape Transport 800 bpi	10/3.048	100/30.48
RF15	DECdisk Control for up to 8 RS09 DECdisk Units		
RS09	262,144 Word DECdisk		
RP15	Disk Pack Control for up to 8 RP02 Disk Pack Units		
RP02	10.24 million-word Drive Unit – Includes one RP02P Disk Pack	20/6.1	50/15.24
RP03	20.48 million-word Drive Unit – Includes one RP02P Disk Pack	20/6.1	50/15.24
Display Devices			
VP15A	Storage Tube Display VT01 Storage Display Unit Control and Mounting Hardware	15/4.5	15/4.5
VP15B	Oscilloscope Display Tektronix RM503 X-Y Oscilloscope, Control, and Mounting Hardware	15/4.5	15/4.5
VP15BL	Oscilloscope Display Tektronix RM503 X-Y Oscilloscope, Control, Mounting Hardware, and DEC Type 370 Light Pen	15/4.5	15/4.5

*Special quotations are required for nonstandard cable lengths.

Table 5-6 (Cont)
Optional Peripheral Equipment Cable Lengths

Peripheral Equipment		Cable Length* ft/m	
		Standard	Maximum
Display Devices (Cont)			
VP15C	Oscilloscope Display VR12 X-Y Display Unit (7 X 9 in. CRT) Control, and Mounting Hardware	15/4.5	15/4.5
VP15CL	Oscilloscope Display VR12 X-Y Display Unit (7 X 9 in. CRT) Control, Mounting Hardware, and DEC Type 370 Light Pen	15/4.5	15/4.5
VT15	Graphic Processor	75/22.5	120/22.5
VT04	Graphic Display Console	25/7.5	75/7.5
VT07	Graphic Display Console	25/7.5	75/7.5
Card Input			
CR15	Card Reader (Table Top) – 300 characters/minute Reader and Control	10/2.134	15/4.5
Paper Tape Input			
PC15	Paper Tape Station – 300 characters/second Reader, 50 characters/second Punch		
Printers and Plotters			
LP15R	Line Printer – 1000 ipm Line Printer and Control	25/7.62	25/7.62
LP15V	Line Printer – 300 ipm Line Printer and Control	15/4.5	25/7.62
CalComp Plotter and Control			
XY15AA	12 in. Drum Plotter, Model 565, and Control 0.01 in. Step 18,000 Steps/Minute	10/3.048	10/3.048
XY15AB	0.005 in. Step 18,000 Steps/Minute	10/3.048	10/3.048
XY15BA	31 in. Drum Plotter, Model 563, and Control 0.01 in. Step 12,000 Steps/Minute	10/3.048	10/3.048

*Special quotations are required for nonstandard cable lengths.

Table 5-6 (Cont)
Optional Peripheral Equipment Cable Lengths

Peripheral Equipment		Cable Length* ft/m	
		Standard	Maximum
CalComp Plotter and Control (Cont)			
XY15BB	0.005 in. Step 18,000 Steps/Minute	10/3.048	10/3.048
XY15	Control Only		
Data Communications			
LT19D	Multi-Station Teletype Control (Expands to 5 LT19B Line Units)	12/3.66	Up to 2000/609.6
LT19E	Line Unit (One Required for each Teletype or EIA Line Adapter)	12/3.66	Up to 2000/609.6
LT19F	EIA Line Adapter (Per Line)		
LT15A	Single-Teletype Control		
	Teletype Model 33 Keyboard Send-Receive Unit	12/3.66	Up to 2000/609.9
	Teletype Model 33 Automatic Send-Receive Unit with Paper Tape Reader and Punch	12/3.66	Up to 2000/609.9
	Teletype Model 35 Keyboard Send-Receive Unit	12/3.66	Up to 2000/609.9
	Teletype Model 35 Automatic Send-Receive Unit with Paper Tape Reader and Punch	12/3.66	Up to 2000/609.9
DP09A	Data Communications System compatible with EIA RS232B Interface, Bell System Type 201 Dataphone		

*Special quotations are required for nonstandard cable lengths.

5.12 MISCELLANEOUS PART NUMBERS

The following is a list of part numbers, mainly expendable parts, which may help during an installation:

DEC Part No.	Description	Use
90-06066-03	Screw Truss head 1/4-20 × 2-1/2	Holds logo to cabinet top
90-06074-01	Screw, Phillips Phill head 10-32 × 5/8	Holds items to cabinet
90-07786-00	Nut Tinnerman, 10-32	Spring nuts for cabinet
90-06074-02	Screw Cntrsunk, flat head 10-32 × 5/8	Holds logic and latch molding
90-08887-00	Ground strap	
90-06374-08	Screw Skt hd cap 1/4-20 × 1	Holds cabinets together
90-08203-00	Nut, 10-32 keps	Holds cabinets with screw above

5.13 MAINTENANCE AND SERVICE OPTIONS

Digital Equipment Corporation's Field Service Organization offers a wide range of services for DIGITAL equipment users. Customers may choose from a broad selection of Service Contract Options and Per-Call Service of Depot Repair Maintenance plans to ensure optimum operating efficiency for their DIGITAL equipment.

Service Contracts

Service Contracts are tailored to the user's individual operation. In addition to providing all the necessary parts, labor, and test equipment required for remedial maintenance, Service Contracts also ensure system reliability by providing scheduled, systematic preventive maintenance. Planning and budgeting are greatly simplified because these contracts allow the user to fill his maintenance needs at a fixed, monthly charge.

Service Contract Options

On-Call Service Contract Coverage provides remedial maintenance when the customer notifies DIGITAL of a system malfunction. Preventive maintenance is scheduled and performed during the period selected by the user. The principal period of coverage consists of eight consecutive hours of on-call coverage during the period 7 a.m. through 6 p.m., Monday through Friday. The user can extend his coverage from the principal period by selecting:

1. Twelve consecutive hours of on-call coverage
2. Sixteen consecutive hours of on-call coverage
3. Twenty consecutive hours of on-call coverage
4. Twenty-four consecutive hours of on-call coverage

Coverage of 24 consecutive hours, Monday through Friday, begins on Monday of each week at 7 a.m. and terminates on Saturday of each week at 7 a.m.

The Saturday period of coverage consists of eight consecutive hours of on-call coverage during the period 7 a.m. through 6 p.m. The Sunday period of coverage consists of eight consecutive hours of on-call coverage during the period 7 a.m. through 6 p.m. As with the principal period of coverage, Saturday/Sunday coverage can be extended to 12, 16, 20, and 24 hours.

An on-site resident engineer plan can be implemented if the size, complexity, and/or critical nature of an installation require such a plan. The services of a resident engineer consist of 40 hours of coverage during the normal work week. In addition, all necessary spare parts, materials, and test equipment are

physically stationed at the user's site to further ensure prompt and efficient remedial and preventive maintenance services. Monthly rates for contracted coverage are supplied on request.

There are no additional charges for travel in connection with service contracts except for remote installations. Remote installations are defined as installations located at a distance greater than 100 miles from a DIGITAL Field Service Office.

Eligibility for Service Contract Coverage

A Pre-Service Contract Inspection is required for installations that were not under DIGITAL's maintenance responsibility immediately prior to the requested commencement date of the service agreement. All charges associated with this inspection (including travel, labor, and parts) are billed to the user at the prevailing standard DIGITAL rates. A minimum charge is associated with the Pre-Service Contract Inspection. No inspection is required for service agreements that are scheduled to commence immediately after the expiration of a standard DIGITAL Warranty or Service Contract.

Per-Call Coverage

Per-Call Coverage is designed to permit the users of DIGITAL equipment to obtain service on a time and materials basis. Requests for Per-Call Coverage are considered after requests for Service Contract Coverage; thus, only users with their own service capabilities or users who are not critically tied to their equipment are encouraged to use this form of coverage. All charges for Per-Call Coverage are computed on a portal-to-portal basis. Commercial travel expenses related to the performance of services are billed as incurred. Material and parts consumption associated with Per-Call Coverage are charged to the user at the prevailing prices listed in the DEC Spare Parts Catalog. Labor charges for Per-Call Service are on an hourly basis and are available on request.

A minimum charge for Per-Call Service applies to each service call; in addition, DIGITAL neither implies nor guarantees the availability of Per-Call Coverage outside the hours of 7 a.m. through 6 p.m., Monday through Friday. Users in need of extended periods of coverage are encouraged to use the many Service Contract options available.

Users receive an invoice for all service rendered under Per-Call Coverage. It is the responsibility of the user to inform the DIGITAL Field Service Office servicing the equipment of any special billing instructions related to the use of Per-Call Coverage. Such notification must be rendered before the commencement of any services on the part of DIGITAL; in the absence of such notification, invoicing shall be accomplished in accordance with procedures determined by DIGITAL. Installations requiring Purchase Orders for the authorization of work performed on a time and materials basis are encouraged to submit a blanket order for one year's duration to cover such services. There will be no additional charge for processing and administering such blanket orders. Terms for all services provided on a per-call basis are net 30 days. In addition to the charges outlined above, customers are also charged for all federal, state, municipal, or other government, excise, sales, use, occupational, or like taxes, now in force or enacted in the future, incurred as a result of the performance of per-call service. Installations enjoying tax exemption are requested to present their current exemption certificate number at the time that Per-Call Service is rendered or with the submission of the blanket Purchase Order.

Depot Repair

Depot repair facilities have been strategically located throughout the world to enable users of DIGITAL equipment to receive prompt, efficient service on many standard DIGITAL options. Depots are also fully equipped to service and completely rebuild, if necessary, ASR and KSR Teletypes®. Furthermore, users of DIGITAL equipment interested in purchasing rebuilt ASR and KSR Teletypes, or using their existing Teletypes on a trade-in basis toward the purchase of new machines, are urged to contact their nearest DIGITAL Field Service Office for further information.

®Teletype is a registered trademark of Teletype Corporation, Skokie, Illinois.

Depots are fully equipped and staffed with experienced personnel to offer rapid and economical repair services to the DIGITAL customer. At the user's option, a national transportation firm, contracted by DIGITAL, can be used to route equipment to and from the depot facility. Customers wishing to use the depot facilities are requested to contact the nearest depot and furnish the following:

1. Customer name
2. Customer address
3. Purchase order number
4. Billing address
5. Name and telephone number of individual
6. Type, model number, and serial number of equipment to be serviced
7. Brief description of service problem or malfunction
8. Mode of transportation to be used (DIGITAL carrier or other)

Upon receiving the above information, the depot issues a return authorization number that enables the user to ship the equipment for servicing.

Field Installation of Additional DIGITAL Options

Customers wishing to expand their present systems by purchasing additional DIGITAL options may elect to have the installation of the new equipment performed at a fixed rate to facilitate the budgeting and purchasing processes.

Field installation rates are available on request. To compute the installation charges for an option or group of options, the total charge is equal to the sum of the option installation charges plus a one-time travel charge.

For the purpose of performing field installations, remote locations are defined as areas outside those areas normally serviced by DIGITAL or its subsidiaries. Requests for installations in remote locations are considered on an individual basis. Field installations are performed from 7 a.m. to 6 p.m., Monday through Friday. A minimum charge is associated with a field installation.

5.14 FORMS AND CHECKLISTS

A large envelope, enclosed with the XVM Accessory Kit, contains the following items:

1. Customer acceptance forms
2. Key sheet
3. Customer data forms
4. Software trouble reports
5. DECUS information
6. Basic accessory checklists
7. Optional equipment checklists
8. Software checklists
9. Final distribution lists

Each of the items listed is discussed in the following paragraphs. The sole intent of this information is to produce uniformity in customer acceptance procedures.

Customer Acceptance Forms

The customer acceptance forms are logged at DIGITAL in Maynard, Massachusetts, prior to equipment acceptance. The form lists the equipment items that are included in the shipment. The customer name, the DEC installation code, the DEC order number, and the customer purchase orders are also included on the form. Personnel installing the equipment must check the keyed equipment serial numbers listing against the serial number on the equipment and enter the serial numbers in the appropriate column on the customer acceptance form. All serial numbers, including those on vendor-supplied material, are verified in this manner.

All future XVM System additions, modifications, and inquiries are solely dependent on the accuracy of the key sheet, which lists all system components by model and serial number, and the acceptance forms. Upon successful completion of acceptance testing, any "exceptions" are listed in the appropriate section on the customer acceptance form. The "exceptions" should include missing manuals or prints and any hardware, etc., that was not acceptable.

Customer Data Forms

The customer data form is used to establish an accurate mailing list and customer contact file. The form should be completely filled out and the appropriate copy returned to DIGITAL's Field Service Organization in Maynard, Massachusetts.

Software Trouble Reports

Software trouble reports enable the customer to communicate directly with the DIGITAL Software Group. Any software problems should be described in detail and, if possible, examples attached.

DECUS Information

The DECUS information and introductory letter familiarizes the user with the Digital Equipment Computer User's Society. The letter invites membership and includes application forms.

Basic Accessory Checklist

The basic accessory checklist contains an accurate list of all items that are normally supplied with the basic XVM. DIGITAL personnel check each item on this list with the customer, and the customer then signs the complete form. The appropriate copy is then returned to DIGITAL in Maynard, Massachusetts. The remaining copies should be distributed as indicated on the bottom of the form. Specified items that are not included should be listed as "exceptions" on the customer acceptance forms.

Optional Equipment Checklist

Accessory checklists for each option are supplied. The basic accessory checklist procedures apply.

Software Checklist

The software checklist enclosed has been checked at the factory and is rechecked with the customer. Any items missing should be listed as "exceptions". This form is also signed by the customer and returned to DIGITAL in Maynard, Massachusetts. Requests for additional copies of programs should be submitted to the DIGITAL Program Library.

Final Distribution of Forms

The return-addressed envelope is sent to DIGITAL in Maynard, Massachusetts with the following completed forms:

1. Customer acceptance forms
2. Customer data forms
3. Basic accessory list
4. Optional equipment checklist
5. Software checklist
6. Installation report
7. Final distribution lists

All of these items, except 2 and 6, require the customer's signature. Only items listed as "exceptions" are replaced at no cost. All other items must be substantiated by a customer purchase order.

A complete set of prints is supplied with the XVM System. The key sheet should be used to reference the Master Drawing List (MDL) or Drawing Directory for each subsection or option in the XVM System. Wire lists, parts lists, and mechanical assembly prints are not supplied with any print set. These may be obtained only by special order.

Computer System Layout Checkoff/Transmittal Sheet

When planning an XVM System installation, use the Computer System Layout Checkoff/Transmittal Sheet as a guide to keep track of key items that must be considered during the planning stage. After planning has been completed, forward the Computer System Layout Checkoff/Transmittal Sheet to the DIGITAL salesperson from whom the system was purchased.

CHAPTER 6

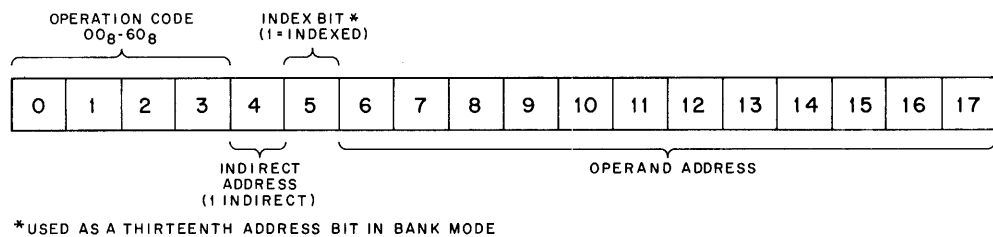
INSTRUCTION FORMATS

6.1 BASIC INSTRUCTION SET

The XVM Instruction Set is divided into “memory reference instructions,” which address core memory, and “augmented instructions,” which do not address core memory. Memory reference instructions address, either directly or indirectly, core memory locations for the purpose of retrieving, entering, or modifying the contents. The augmented instructions are used to execute a certain action or actions. This type of instruction is subdivided into four groups: operate instructions (Link and Accumulator operations including rotates, skips, clears, and complements); IOT instructions (input/output transfer of data, command and status between the central processor, and peripheral devices); EAE (extended arithmetic element, hardware multiply, divide, shift, and normalize); and index instructions (accumulator, limit register, and index register transfers, clears, additions, and skips).

Memory Reference Instruction Format

The memory reference instruction word consists of an operation code, an indirect address bit, and index bit, and an operand address (Figure 6-1). The operation code, bits 0 through 3, specifies one of the 13 XVM memory reference instructions. When the XVM is in Page mode, the indirect bit (bit 4) indicates whether the 12-bit (bits 6-17) operand address is to be directly or indirectly (bit 4=1) addressed and the index bit (bit 5) determines whether or not the index register should be added to the operand address. In Bank Mode, the indirect bit (bit 4) indicates whether the 13-bit (bits 5-17) operand address is to be used as the direct address or the indirect address (bit 4=1). The operand address is used to generate the effective address or the address in memory which will be referenced. A detailed description of addressing is located in Chapter 1, Paragraph 1.2.

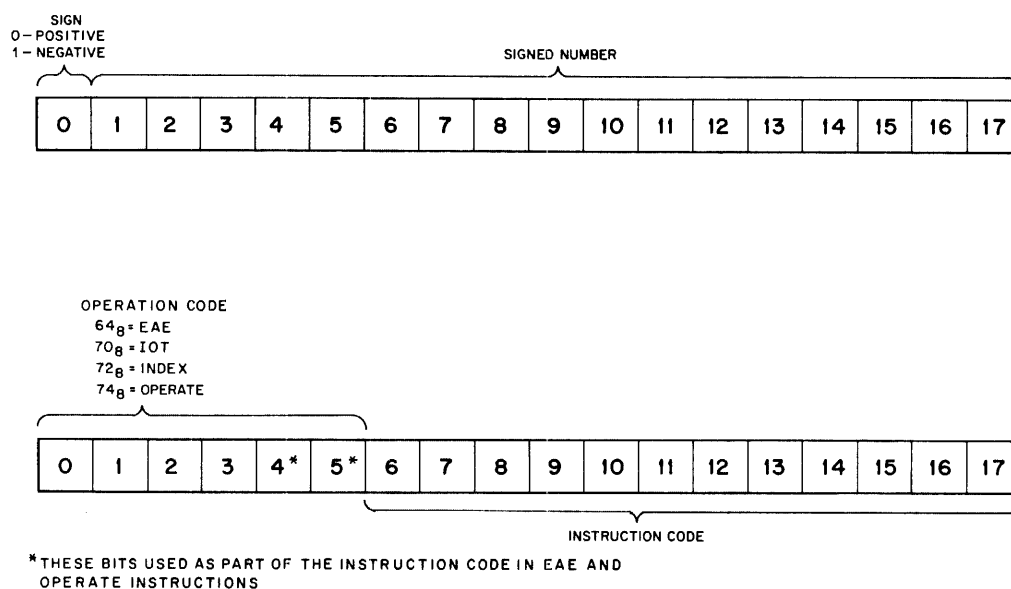


15-0188

Figure 6-1 Memory Reference Instruction Word

Augmented Instruction Format

The augmented instruction word (Figure 6-2) consists of an operation code and an instruction code. The operation code designates whether the instruction is an extended arithmetic element instruction, 64_8 (bits 0-3), an Input/Output transfer instruction, 70_8 (bits 0-5), an Index instruction, 72_8 (bits 0-5) or an operate instruction 74_8 (bits 0-3). The instruction code designates which action is to be taken by the augmented instruction. An important and useful feature of the XVM augmented instruction is its microprogramming capability. Multiple instruction codes having the same operation code can be combined to form one instruction word. Execution of all microprogrammed functions occurs during the time allocated to the type of instruction (operate instructions require one machine cycle, IOTs require two, three, or four cycles, EAE requires one or three, plus a variable time interval to complete their function, and index instructions require two cycles). Thus, microprogramming decreases program running time, lessens the number of instruction words required, and simplifies programming efforts.



15-0204

Figure 6-2 Augmented Instruction Format

Timing

The amount of time required to perform each instruction is expressed in the number of machine cycles.

Instructions that indirectly address memory require one extra machine cycle to fetch and compute the indirect address. Only one level of indirect addressing is allowed on the XVM.

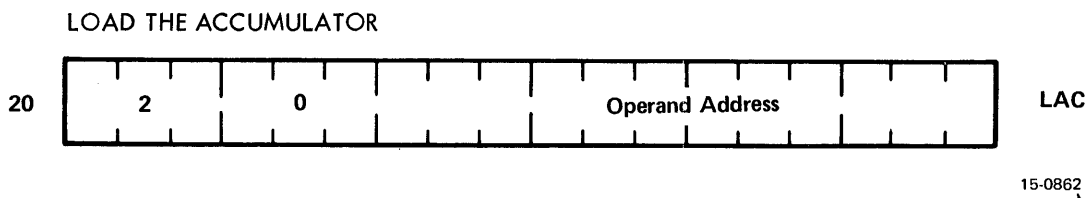
Instructions that use the auto increment locations indirectly require two extra machine cycles; one for the increment of the location, and one for the indirect address.

Memory Reference Instructions

In the memory reference instruction descriptions, and in succeeding paragraphs that describe other types of instructions, the following symbols are used:

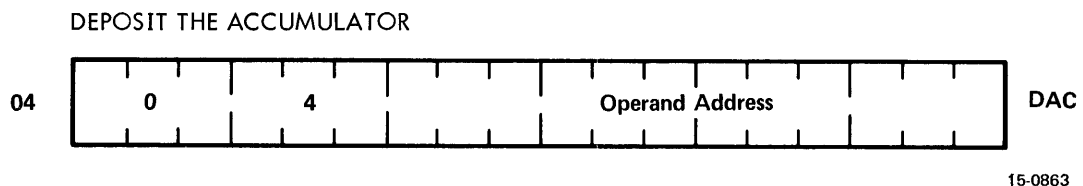
Symbol	Definition
Y	The effective address of the memory location
OR	Logic inclusive-OR
to	Indicates contents transferred from register or location to register or location.
AND	Logic AND
XOR	Logic exclusive-OR
-OR	Indicates complemented contents of register or location.
+	Addition

LOAD THE ACCUMULATOR



Mnemonic Name	LAC
Octal Code	20
Time	2 cycles
Operation	The contents of the effectively addressed memory location, Y, are read into the AC. The contents of Y are unchanged, the previous contents of the AC are lost.
Symbolic	Y to AC

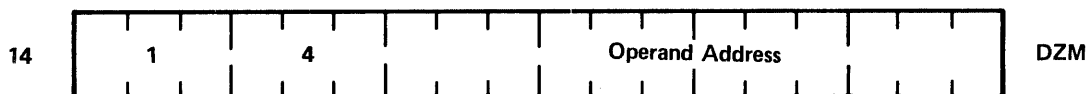
DEPOSIT THE ACCUMULATOR



Mnemonic Name	DAC
Octal Code	04
Time	2 cycles
Operation	The contents of the AC are deposited in the effectively addressed memory location Y. The contents of the AC are unchanged; the previous contents of Y are lost.
Symbolic	AC to Y

DEPOSIT ZERO IN MEMORY

DEPOSIT ZERO IN MEMORY



15-0864

Mnemonic Name	DZM
Octal Code	14
Time	2 cycles
Operation	An all-zeros data word is deposited in the effectively addressed memory location Y. The previous contents of Y are lost; the contents of the AC are unchanged.
Symbolic	0 to Y

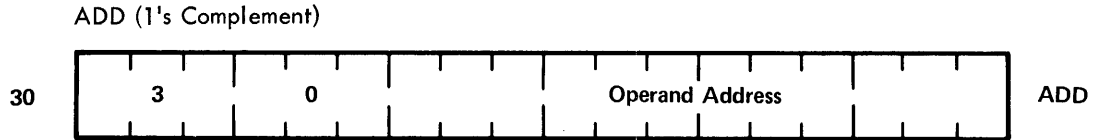
ADD (2's COMPLEMENT)



15-0865

Mnemonic Name	TAD
Octal Code	34
Time	2 cycles
Operation	The contents of the effectively addressed memory location Y are added to the contents of the AC, following the rules of 2's complement arithmetic. The result is left in the AC. An arithmetic carry from AC ₀ complements the link. The contents of Y are unchanged; the previous contents of the AC are lost.
Symbolic	$Y + (L, AC) \rightarrow (L, AC)$

ADD (1's COMPLEMENT)



15-0866

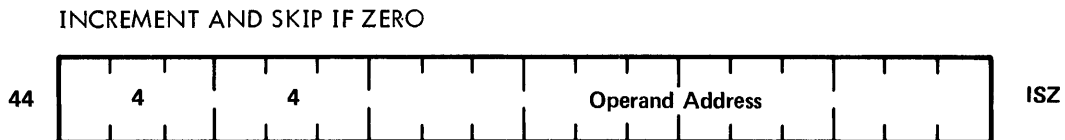
Mnemonic Name	ADD
Octal Code	30
Time	2.3 cycles
Operation	The contents of the effectively addressed location Y are added to the contents of the AC, following the rules of 1's complement arithmetic. The result is left in the AC. An arithmetic overflow sets the link to the binary 1 state. The contents of the AC are lost. The previous contents of the link are lost. Overflow occurs if the magnitude (absolute) of the algebraic sum of the operands exceeds $2^{17}-1$; if the operands were of like sign and the result is signed differently, overflow has occurred to set the link. Overflow cannot occur if the operands are of different sign.

NOTE

The link should be cleared prior to the ADD instruction, if an arithmetic overflow check is desired.

Symbolic	Y + AC to AC L OR Overflow to L

INCREMENT AND SKIP IF ZERO



15-0867

Mnemonic Name	ISZ
Octal Code	44
Time	3 cycles
Operation	The contents of the effectively addressed memory location Y are incremented by one (in 2's complement arithmetic) and tested. If Y now contains an all-zero word, the PC is incremented by one to skip the next instruction. If the contents of Y, after being incremented, are other than zero, the next instruction is executed. The previous contents of Y are lost; the contents of the AC are unchanged.
Symbolic	If $Y + 1 = 0$, PC + 1 to PC Y + 1 to Y

SKIP IF AC DIFFERS

SKIP IF AC DIFFERS

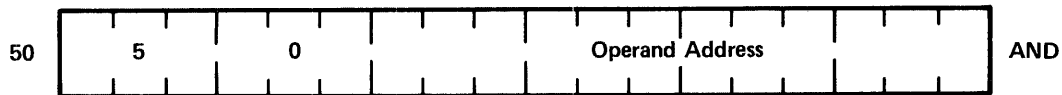


15-0868

Mnemonic Name	SAD
Octal Code	54
Time	2 cycles
Operation	The contents of the effectively addressed memory location Y are compared with the contents of the AC. If they differ, the PC is incremented by one to skip the next instruction. If they are the same binary quantity, the next instruction is executed. The contents of Y and the contents of the AC are unchanged.
Symbolic	If Y is not equal to AC, PC + 1 to PC

BOOLEAN AND

BOOLEAN AND



15-0869

Mnemonic Name	AND
Octal Code	50
Time	2 cycles
Operation	The contents of the effectively addressed memory location Y are logically ANDed with the contents of the AC on a bit-by-bit basis. The result is left in the AC. If corresponding Y and AC bits are in the 1 state, the AC bit remains a 1; otherwise, the AC bit is cleared to the 0 state. The contents of Y are unchanged; the previous contents of the AC are lost.
Symbolic	Y AND AC to AC

EXECUTE THE INSTRUCTION AT Y

EXECUTE THE INSTRUCTION AT Y

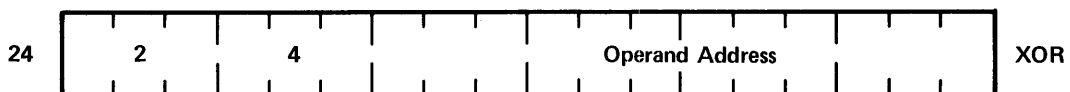


15-0870

Mnemonic Name	XCT
Octal Code	40
Time	1 cycle plus time of instruction at Y
Operation	The computer executes the instruction located at the effectively addressed memory location Y. The contents of the PC are unchanged unless Y contains a JMS, CAL, JMP, or skip instruction, each of which changes the contents of the PC to alter the program sequence. XCT could be thought of as a single-instruction subroutine causing a quasi-jump to Y, execution of the instruction specified there, and return to the program sequence (i.e., execution of the instruction following XCT) if the instruction has not changed the PC. When in User mode, an XCT of an XCT instruction is not allowed.
Symbolic	Y ₀₋₅ to IR

BOOLEAN EXCLUSIVE OR

BOOLEAN EXCLUSIVE OR



15-0871

Mnemonic Name	XOR
Octal Code	24
Time	2 cycles
Operation	The contents of the effectively addressed memory location Y are exclusively-ORed with the contents of the AC, on a bit-by-bit basis. The result is left in the AC. If corresponding Y and AC bits are in the same binary state (i.e., 1 or 0), the AC bit is cleared to the 0 state. If the corresponding bits differ in state, the AC bit is set to the 1 state. The contents of Y are unchanged. The previous contents of the AC are lost.
Symbolic	Y XOR AC to AC

UNCONDITIONAL JUMP

UNCONDITIONAL JUMP



15-0872

Mnemonic Name	JMP
Octal Code	60
Time	1 cycle
Operation	A new address is computed from the operand address of the Jump instruction and transferred to the PC. The next instruction fetched will be from the memory location specified by the new address. The contents of the AC are unchanged.
Symbolic	Y_{5-17} to PC

JUMP TO SUBROUTINE

JUMP TO SUBROUTINE



15-0873

Mnemonic Name	JMS
Octal Code	10
Time	2 cycles
Operation	The contents of the PC and the Link, and the status (on or off) of Bank mode and User mode are deposited in the effectively addressed memory location Y. The next instruction is read from the contents of memory location $Y + 1$, breaking the previous program sequence and starting a new sequence from $Y + 1$. The contents of the PC are changed, and the contents of the AC are unchanged. When not in the User mode, a free instruction follows the JMS. Therefore, a PI or API break cannot occur after the execution of the JMS instruction, but may occur after the execution of the next instruction.
Symbolic	L to Y_0 BM to Y_1 UM to Y_2 PC to Y_{3-17} $Y_{5-17} + 1$ to PC

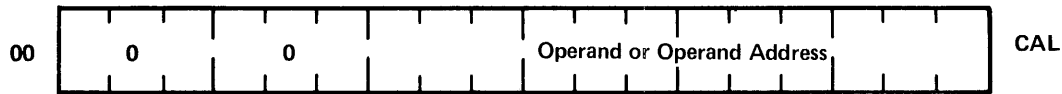
NOTE

If the system is in G-Mode 1, 2, or 3, and in User mode when a JMS is executed, PC 00-17 will be stored in addressed location Y. The state of the Link, Bank mode, and User mode will not be stored.

Symbolic	PC to Y_{0-17} , $Y_{5-17} + 1$ to PC

(JUMP TO) SYSTEM

CALL (JUMP TO) SUBROUTINE



15-0874

Mnemonic Name	CAL
Octal Code	00
Time	2 cycles
Operation	The CAL instruction is similar to a JMS 20 instruction. The contents of the PC and the Link, and the status (on or off) of Bank mode and User mode are deposited in real memory location 20. The next instruction is read from real memory location 21, breaking the previous program sequence and starting a new sequence from 21. The contents of the AC are unchanged. If the API system is enabled, priority level 4 will be activated after the execution of a CAL instruction if no higher priority level is set. When the CAL instruction is executed, the processor re-enters Exec mode and the instruction in location 00021 will be executed before an interrupt is allowed to occur.
	The CAL instruction is used in all XVM Software to enter and request services of the operating system.
Symbolic	L to 20 ₀ BM to 20 ₁ UM to 20 ₂ PC to 20 ₃₋₁₇ "21" to PC 0 to UM

Augmented Instructions

Operate Instructions

Operate instructions (operation code of 74₈) are used to sense and/or alter the contents of the AC and Link. Typical functions are: conditional or unconditional skips, complementing, setting, clearing, or rotating the contents of the two registers jointly or independently and incrementing the AC. A Halt (HLT) instruction is included. Operates are performed in one machine cycle, the actions specified by the microprogramming of the instruction code. Each bit of the 14-bit instruction code can effect a unique response; hence, they are "microinstructions" to the computer. The important feature of the operate class is its microprogramming capability, where two or three microinstructions can be combined to form one instruction word and, therefore, be executed in one cycle. Those microinstructions that logically conflict and occur at the same time should not be microprogrammed. Figure 6-3 illustrates the bit configuration of the instruction code. Figure 6-4 shows the allowable combinations of microinstructions.

CLA	CLL	Additional Rotate	0=OR of 1=AND of		SNL	SZA	SMA	HLT	Bit 7=0		OAS	CML	CMA
					SZL	SNA	SPA		RAR	RAL			
									RTR	RTL			
5	6	7	8	9	10	11	12	Bit 7=1			15	16	17
								13	14				

NOTE: Bits 7, 13, and 14 set: SWHA
Bits 13 and 14 set: IAC

15-0875

Figure 6-3 Instruction Bit Configuration

Order of Events	Column 1	Column 2	Column 3		Column 4
Level 1	SNL SZA SMA	CLA CLL	OAS CMA	CML IAC	HLT
Level 2	SZL SNA SPA		RAR or RAL		
Level 3	SKP		RTR or RTL or SWHA		

15-0876

Figure 6-4 Allowable Microinstruction Combinations

NOTE 1

When noninverted skip actions are microprogrammed (bit 8 is 0), the conditions to be met are inclusively ORed. For example, if SZA (740200) and SNL (740400) are combined (740600), the skip takes place if either or both conditions are present (contents of the AC are 0 or the content of the link is not 0).

NOTE 2

When inverted skip actions are microprogrammed (bit 8 is 1), the skip occurs only if the AND of the conditions is met. For example, when SNA (741200) and SZL (741400) are specified in a microprogrammed instruction (741600), the skip occurs only if both conditions are present (the contents of the AC are other than 0 and the content of the link is 0).

Programming Note

The XVM MACRO Symbolic Assembler accepts either HLT or XX (Figure 6-4) as a valid mnemonic for the operate class instruction to stop program execution. The latter facilitates visual scanning of a program listing to determine the occurrence of program halts.

1. Combine instructions from left to right.
2. Any instructions in a box can be combined, except the rotate instructions.
3. Instructions on different levels cannot be combined if they are in the same column. Instructions on any level can be combined if they are in different columns. For example, SZA!SMA!CLA!OAS!HLT! is legal – SZA!SPA is illegal.
4. CML and IAC cannot be combined. Either one can be combined with OAS and/or CMA (e.g., OAS!CMA!CML or OAS!CMA!IAC).
5. Instructions occur in order from column 1 to column 4.

OPERATE INSTRUCTIONS COMBINING CHART

1			2		3		4	
SNL	SZA	SMA	CLL	CLA	OAS	CMA	IAC	HLT
SZL	SNA	SPA				RAR		
	SKP					RAL		
						RTR		
						RTL		
						SWHA		

1. Instructions occur in order 1 through 4.
2. Instructions may be combined unless they are in different boxes in the same column.
3. The following skips are combined as if ORed: SNL, SZA, SMA.
4. The following skips are combined as if ANDed: SZL, SNA, SPA.
5. CML occurs at time 3 and can be combined normally with everything except IAC and Rotates.
6. CML combined with IAC executes as a CML! STL and therefore should not be used.
7. CML combined with a rotate will cause the new state of the L to be an OR of the compliment of the L and the state rotated in and therefore should not be used.
8. SWHA combined with CLA will leave the AC in the same state as it held before the instruction was executed and so should not be used.
9. SWHA and Rotates will cause the following to be ignored: OAS, CMA, IAC.
10. LAW will cause all other microcodes to be ignored.
11. All illegal combinations not otherwise mentioned will correspond to some correct microcode of different meaning and be executed as such.

OPERATE GROUP

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
79	OP	CEDE															
	LAW																
	CLA																
	CLL																
	ROTATE 2	(SWHA)															
	INVERT SKIP	SENSE (SKP)															
	SNL	(SZL)															
	SZA	(SNA)															
	SMA	(SPA)															
	HLT																
	RAR	(RTR, IAC, SWHA)															
	RAL	(RTL, IAC, SWHA)															
	OAS																
	CML																
	CMA																

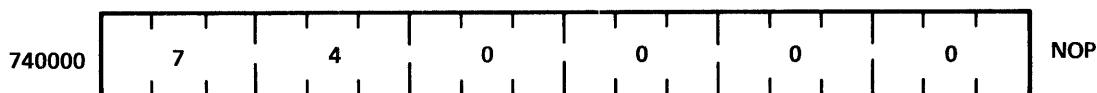
Condition	Code
AC>0	SPA! SNA
AC>=0	SPA
AC=0	SZA
AC<0	SMA! SZA
AC<=0	SMA
AC=0	SNA

NOTE

Level 1 skips (SNA, SZA, SMA) will occur if any one of the combined tests is satisfied (an OR condition). Level 2 skips (SZL, SNA, SPA) will occur only if all the combined tests occur (an AND condition). Combined rotates become a SWHA or an IAC, depending on bit 7.

NO OPERATION

NO OPERATION

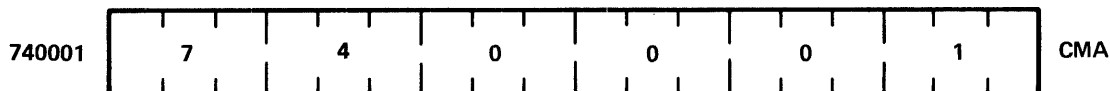


15-0877

Mnemonic Name	NOP
Octal Code	740000
Time	1 cycle
Operation	The program delays for one cycle before the next instruction is fetched.

COMPLEMENT ACCUMULATOR

COMPLEMENT ACCUMULATOR



15-0878

Mnemonic Name	CMA
Octal Code	740001
Time	1 cycle
Operation	Each bit of the AC is set or cleared to the inverse of its current state. The previous contents of the AC are lost.
Symbolic	-AC to AC

COMPLEMENT LINK

COMPLEMENT LINK

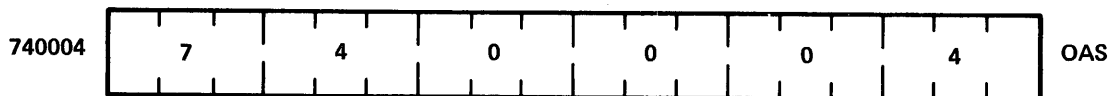


15-0879

Mnemonic Name	CML
Octal Code	740002
Time	1 cycle
Operation	The link is set or cleared to the inverse of its current state. Its previous content is lost.
Symbolic	-L to L

INCLUSIVE OR ACCUMULATOR SWITCHES

INCLUSIVE OR ACCUMULATOR SWITCHES



15-0880

Mnemonic Name	OAS
Octal Code	740004
Time	1 cycle
Operation	The word set up by manual positioning of the DATA switches is inclusive-ORed with the contents of the AC on a bit-by-bit basis. The result is left in the AC. If corresponding, AC and DATA switch bits are in the binary 0 state, the AC bit remains 0. If either or both of the corresponding bits are in the binary 1 state, the AC bit is set to 1. The previous contents of the AC are lost. The switch settings are not affected.
Symbolic	AC OR DATA switch to AC

INCREMENT THE ACCUMULATOR

INCREMENT THE ACCUMULATOR

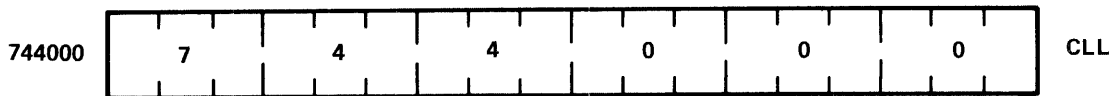


15-0881

Mnemonic Name	IAC
Octal Code	740030
Time	1 cycle
Operation	The contents of the Accumulator are incremented by one and the results placed in the Accumulator. When overflow occurs, bit zero complements the Link.
Symbolic	AC + 1 to AC

CLEAR THE LINK

CLEAR THE LINK

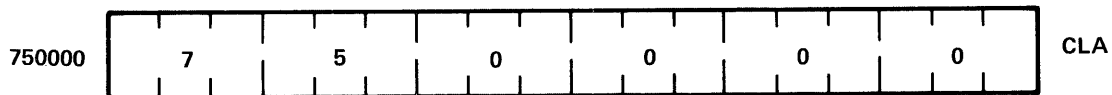


15-0882

Mnemonic Name	CLL
Octal Code	744000
Time	1 cycle
Operation	The content of the link is cleared to the binary 0 state.
Symbolic	0 to L

CLEAR THE ACCUMULATOR

CLEAR THE ACCUMULATOR



15-0883

Mnemonic Name	CLA
Octal Code	750000
Time	1 cycle
Operation	Each bit of the AC is cleared to the binary 0 state. The previous contents are lost.
Symbolic	0 to AC

HALT PROGRAM

HALT PROGRAM



Mnemonic Name	HLT
Octal Code	740040
Time	1 cycle
Operation	Program execution stops at completion of the current machine cycle. The run indicator is turned off. The HLT instruction will cause a trap to occur if executed while the XVM is in User mode with relocation engaged.
Symbolic	0 to RUN flip-flop

SWAP HALVES OF THE ACCUMULATOR

SWAP HALVES OF THE ACCUMULATOR



Mnemonic Name	SWHA
Octal Code	742030
Time	1 cycle
Operation	This instruction places the contents of AC bits 0-8 into AC bits 9-17 and at the same time places AC bits 9-17 into AC bits 0-8. The previous contents of the AC are lost.
Symbolic	AC ₀₋₈ to AC ₉₋₁₇ AC ₉₋₁₇ to AC ₀₋₈

SKIP ON NON-ZERO LINK

SKIP ON NON-ZERO LINK

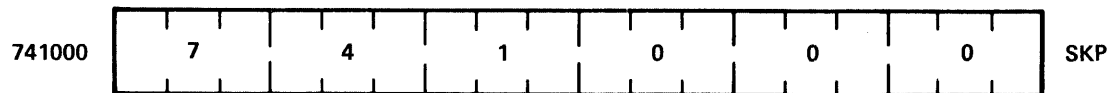


15-0886

Mnemonic Name	SNL
Octal Code	740400
Time	1 cycle
Operation	Test the content of the Link. If the Link is in the binary 1 state, the contents of the PC are incremented by one to skip the next instruction. If the Link has a binary 0, the next instruction is executed. The content of the Link is unchanged.
Symbolic	If L = 1, PC + 1 to PC

UNCONDITIONAL SKIP

UNCONDITIONAL SKIP



15-0887

Mnemonic Name	SKP
Octal Code	741000
Time	1 cycle
Operation	The contents of the PC are incremented by one to cause an unconditional skip of the next instruction.
Symbolic	PC+1 to PC

SKIP ON AC GREATER THAN ZERO (AC>0)

SKIP ON ACCUMULATOR GREATER THAN ZERO

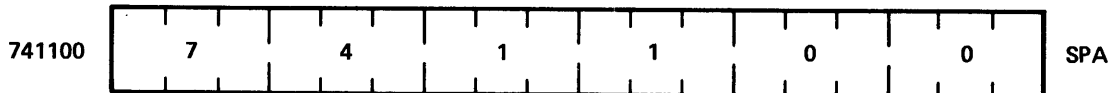


15-0888

Mnemonic Name	SPA!SNA
Octal Code	741300
Time	1 cycle
Operation	Test the contents of the sign bit AC_0 of the data word in the AC and also test that some bit in the AC (AC_{1-17}) is non-zero. If both conditions are true, then skip. The contents of the AC are unchanged.
Symbolic	If $AC_{0-17} > 0$, PC + 1 to PC

SKIP ON POSITIVE ACCUMULATOR (AC $\geq$ 0)

SKIP ON POSITIVE ACCUMULATOR

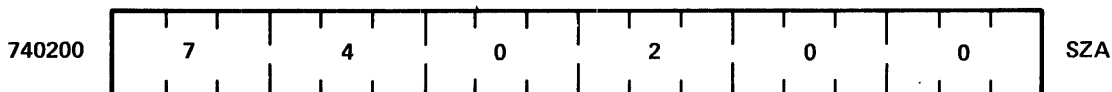


15-0889

Mnemonic Name	SPA
Octal Code	741100
Time	1 cycle
Operation	Test the contents of the sign bit, AC_0 , of the data word in the AC. If the bit is in the binary 0 state, the quantity in the AC is taken to be positive. Therefore, the contents of the PC are incremented by one to skip the next instruction. If the bit is found to be in the binary 1 state, the next instruction is executed. The contents of the AC are unchanged.
Symbolic	If $AC_0 = 0$, PC + 1 to PC

SKIP ON ZERO ACCUMULATOR (AC=0)

SKIP ON ZERO ACCUMULATOR

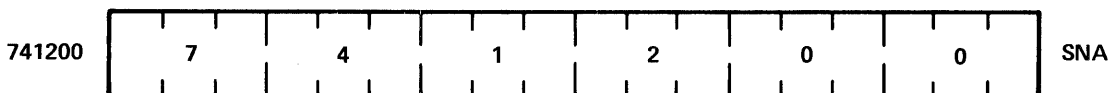


15-0890

Mnemonic Name	SZA
Octal Code	740200
Time	1 cycle
Operation	Test the contents of the word in the AC. If all bits are binary 0s, the quantity is taken to be zero (2's complement notation), and the contents of the PC are incremented by one to skip the next instruction. If any bit is in the binary 1 state, the next instruction is executed. The contents of the AC are unchanged.
Symbolic	If AC = 0, PC + 1 to PC

SKIP ON NON-ZERO ACCUMULATOR (AC is not equal to 0)

SKIP ON NON-ZERO ACCUMULATOR



15-0891

Mnemonic Name	SNA
Octal Code	741200
Time	1 cycle
Operation	Test the contents of the data word in the AC. If any bit is in the binary 1 state, the quantity is taken to be unequal to zero (2's complement notation only), and the contents of the PC are incremented by one to skip the next instruction. If all bits are found to be in the 0 state, the quantity is considered to be zero and the next instruction is executed. The contents of the AC are unchanged.
Symbolic	If AC is not equal to 0, PC + 1 to PC

SKIP IF AC LESS THAN OR EQUAL TO ZERO ($AC \leq 0$)

SKIP IF ACCUMULATOR LESS THEN OR EQUAL TO ZERO



15-0892

Mnemonic Name	SMA!SZA
Octal Code	740300
Operation	Test AC_0 , the sign bit of the data word in the Accumulator. Also test the entire AC_{0-17} for all zeros. If either of these conditions is true, skip the next sequential instruction. The contents of the AC are unchanged.
Symbolic	If $AC_{0-17} = 0$ or AC_0 is not equal to 0, PC + 1 to PC

SKIP ON MINUS ACCUMULATOR

ROTATE AC AND LINK LEFT

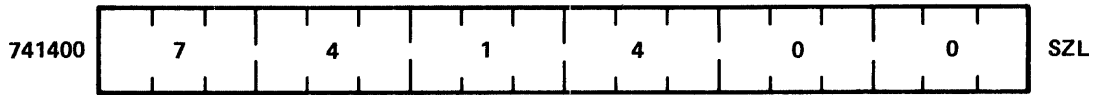


15-0893

Mnemonic Name	SMA
Octal Code	740100
Time	1 cycle
Operation	Test the contents of the sign bit, AC_0 , of the data word in the AC. If the bit is in the binary 1 state, the contents of the PC are incremented by one to skip the next instruction. If AC_0 is found to be in the 0 state, the next instruction is executed. The contents of the AC are unchanged.
Symbolic	If $AC_0 = 1$, PC + 1 to PC

SKIP ON ZERO LINK

SKIP ON ZERO LINK



15-0894

Mnemonic Name	SZL
Octal Code	741400
Time	1 cycle
Operation	Test the contents of the Link. If the Link is in the binary 0 state, the contents of the PC are incremented by one to skip the next instruction. If the Link has a binary 1, the next instruction is executed. The contents of the Link are unchanged.
Symbolic	If L = 0, PC + 1 to PC

ROTATE AC AND LINK LEFT

SKIP ON MINUS ACCUMULATOR

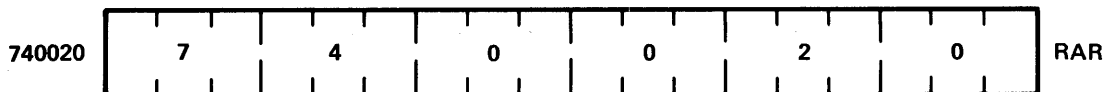


15-0895

Mnemonic Name	RAL
Octal Code	740010
Time	1 cycle
Operation	The contents of the AC and the Link are rotated one bit position to the left with AC ₀ entering the Link and the Link entering AC ₁₇ .
Symbolic	AC _i to AC _{i-1} ; i=1,17 AC ₀ to L L to AC ₁₇ .

ROTATE AC AND LINK RIGHT

ROTATE AC AND LINK RIGHT

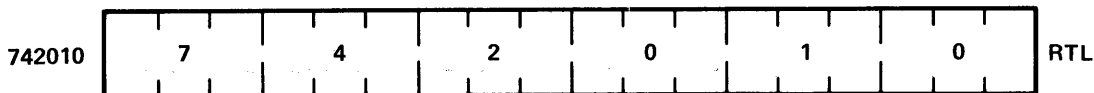


15-0896

Mnemonic Name	RAR
Octal Code	740020
Time	1 cycle
Operation	The contents of the AC and the Link are rotated one bit position to the right with AC_{1-17} entering the Link and the Link entering AC_0 .
Symbolic	AC_i to AC_{i+1} ; $i=0,16$ AC_{17} to L L to AC_0

ROTATE AC AND LINK TWO LEFT

ROTATE AC AND LINK TWO LEFT



15-0897

Mnemonic Name	RTL
Octal Code	742010
Time	1 cycle
Operation	The contents of the AC and the Link are rotated two bit positions to the left with AC_0 entering AC_{17} , AC_1 entering the Link, and the Link entering AC_{16} .
Symbolic	AC_i to AC_{i-2} ; $i=2,17$ L to AC_{16} AC_0 to AC_{17} AC_1 to L

ROTATE AC AND LINK TWO RIGHT

ROTATE AC AND LINK TWO RIGHT

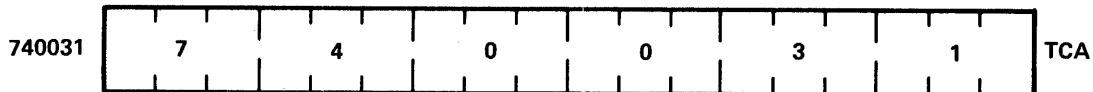


15-0898

Mnemonic Name	RTR
Octal Code	742020
Time	1 cycle
Operation	The contents of the AC and the Link are rotated two bit positions to the right with the Link entering AC_1 , AC_{17} entering AC_0 , and AC_{16} entering the Link.
Symbolic	AC_i to AC_{i+2} ; $i=0,15$ L to AC_1 AC_{17} to AC_0 AC_{16} to L

2'S COMPLEMENT ACCUMULATOR

2'S COMPLEMENT ACCUMULATOR



15-0899

Mnemonic Name	TCA
Octal Code	740031
Time	1 cycle
Operation	A microcoded instruction combines the complement of the AC and increments the AC, thereby performing a 2's complement operation on the contents of the AC and placing the result in the AC. The previous contents of the AC are lost.
Symbolic	$-AC + 1$ to AC

SET THE LINK

SET THE LINK



15-0900

Mnemonic Name	STL
Octal Code	744002
Time	1 cycle
Operation	A microcoded instruction equivalent to CLL+CML. The Link is first cleared to contain a binary 0; it is then complemented to contain a binary 1.
Symbolic	1 to L

CLEAR LINK, THEN ROTATE AC AND L LEFT

CLEAR LINK, THEN ROTATE AC AND L LEFT



15-0901

Mnemonic Name	RCL
Octal Code	744010
Time	1 cycle
Operation	A microcoded instruction equivalent to CLL + RAL. The Link is first cleared to the binary 0 state; then the contents of the AC and the Link are rotated one bit position to the left.
Symbolic	AC _i to AC _{i-1} ; i=1,17 AC ₀ to L 0 to AC ₁₇

CLEAR LINK, THEN ROTATE AC AND L RIGHT

CLEAR LINK, THEN ROTATE AC AND L RIGHT

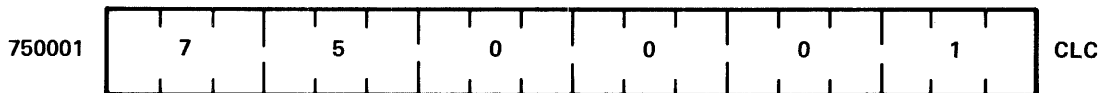


15-0902

Mnemonic Name	RCR
Octal Code	744020
Time	1 cycle
Operation	A microcoded instruction equivalent to CLL + RAR. The Link is first cleared to the binary 0 state; then the contents of the AC and the Link are rotated one bit position to the right.
Symbolic	AC _i to AC _{i+1} ; i=0,16 AC ₁₇ to L 0 to AC ₀

CLEAR AND COMPLEMENT ACCUMULATOR

CLEAR AND COMPLEMENT ACCUMULATOR



15-0903

Mnemonic Name	CLC
Octal Code	750001
Time	1 cycle
Operation	A microcoded instruction equivalent to CLA + CMA. Each bit of the AC is cleared to the binary 0 state. Then each bit is set to the binary 1 state. The previous contents of the AC are lost.
Symbolic	77777 to AC

LOAD AC FROM ACCUMULATOR SWITCHES

LOAD AC FROM ACCUMULATOR SWITCHES



15-0904

Mnemonic Name	LAS
Octal Code	750004
Time	1 cycle
Operation	A microcoded instruction equivalent to CLA + OAS. Each bit of the AC is cleared to the binary 0 state. Then the word set up by manual positioning of the DATA switches is entered in the AC. The previous contents of the AC are lost. The switch settings are not affected.
Symbolic	DSW to AC

GET THE LINK

GET THE LINK



15-0905

Mnemonic Name	GLK
Octal Code	750010
Time	1 cycle
Operation	A microcoded instruction equivalent to CLA + RAL. Each bit of the AC is cleared to the binary 0 state. Then the contents of the AC and the Link are rotated one bit position left with the Link contents entering AC ₁₇ . The previous contents of the AC are lost.
Symbolic	L to AC ₁₇ 0 to AC ₀₋₁₆ 0 to L

LOAD AC WITH n

LOAD AC WITH "n"



15-0906

Mnemonic Name	LAW
Octal Code	760000 + n (n = 13-bit number)
Time	1 cycle
Operation	A single-cycle instruction that loads itself into the AC for the purpose of generating a negative number, n, of the range of $0 \leq n \leq 17777_8$. Following the fetch, the computer enters the contents of the MI (the LAW instruction word) in the AC. The previous contents of the AC are lost. The first five AC bits will always be loaded with ones.
Symbolic	MI to AC

Index Instructions

The index instructions enable the programmer to transfer information between the Accumulator, Limit register, and Index register, clear the Limit register and Index register, add a number contained in the instruction itself (± 256) to the Accumulator, Limit register, or Index register, and test to determine if the Index register is greater than or equal to the Limit register.

All index instructions require two central processor cycles, but only one memory cycle, thus allowing the central processor to perform operations at the same time as the I/O processor.

PLACE ACCUMULATOR IN INDEX REGISTER

PLACE ACCUMULATOR IN INDEX REGISTER



15-0907

Mnemonic Name	PAX
Octal Code	721000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Accumulator are transferred to the Index register. The contents of the Accumulator remain unchanged.
Symbolic	AC to XR

PLACE ACCUMULATOR IN LIMIT REGISTER

PLACE ACCUMULATOR IN LIMIT REGISTER

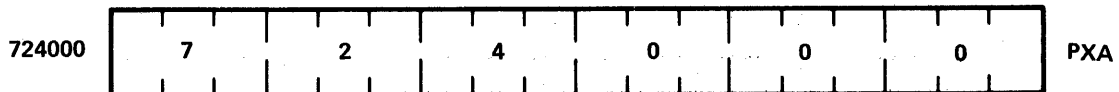


15-0908

Mnemonic Name	PAL
Octal Code	722000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Accumulator are transferred to the Limit register. The contents of the Accumulator remain unchanged.
Symbolic	AC to LR

PLACE INDEX REGISTER IN ACCUMULATOR

PLACE INDEX REGISTER IN ACCUMULATOR

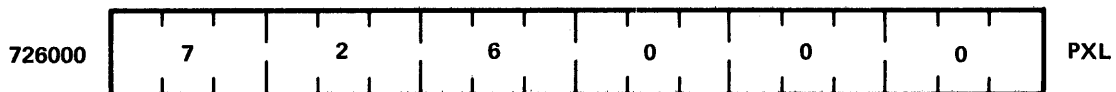


15-0909

Mnemonic Name	PXA
Octal Code	724000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Index register are transferred to the Accumulator. The contents of the Index register remain unchanged.
Symbolic	XR to AC

PLACE INDEX REGISTER IN LIMIT REGISTER

PLACE INDEX REGISTER IN LIMIT REGISTER

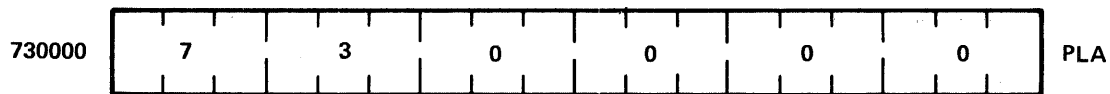


15-0910

Mnemonic Name	PXL
Octal Code	726000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Index register are transferred to the Limit register. The contents of the Index register remain unchanged.
Symbolic	XR to LR

PLACE LIMIT REGISTER IN ACCUMULATOR

PLACE LIMIT REGISTER IN ACCUMULATOR

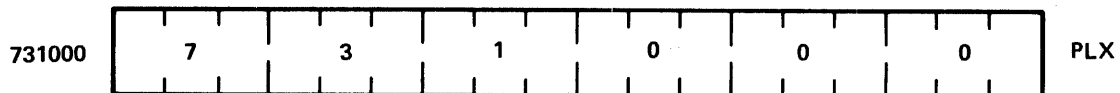


15-0911

Mnemonic Name	PLA
Octal Code	730000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Limit register are transferred to the Accumulator. The contents of the Limit register remain unchanged.
Symbolic	LR to AC

PLACE LIMIT REGISTER IN INDEX REGISTER

PLACE LIMIT REGISTER IN INDEX REGISTER

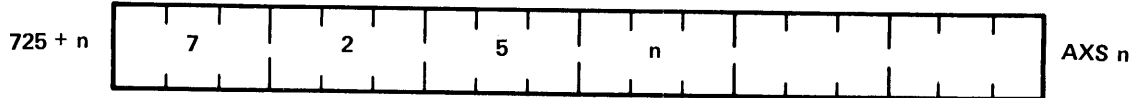


15-0912

Mnemonic Name	PLX
Octal Code	731000
Time	2 cycles (1 memory cycle)
Operation	The contents of the Limit register are transferred to the Index register. The contents of the Limit register remain unchanged.
Symbolic	LR to XR

ADD n TO INDEX REGISTER AND SKIP IF EQUAL TO OR GREATER THAN THE LIMIT REGISTER

ADD n TO INDEX REGISTER AND SKIP IF EQUAL TO OR GREATER THAN THE LIMIT REGISTER

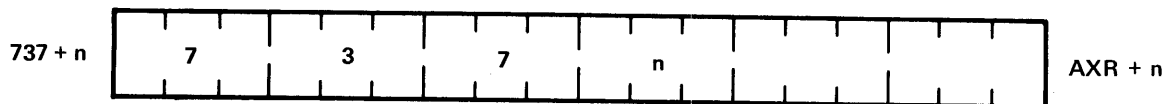


15-0913

Mnemonic Name	AXS n
Octal Code	725000 + n (n = 9 bits)
Time	2 cycles (1 memory cycle)
Operation	n, a signed 9-bit (8 bits plus sign) 2's complement integer is added to the contents of the Index register, and the result is placed in the Index register. If the sum is greater than or equal to the contents of the Limit register, then the program counter is incremented by 1 and thus the next instruction is skipped.
Symbolic	XR + N to XR If $XR \geq LR$, PC + 1 to PC

ADD TO INDEX REGISTER

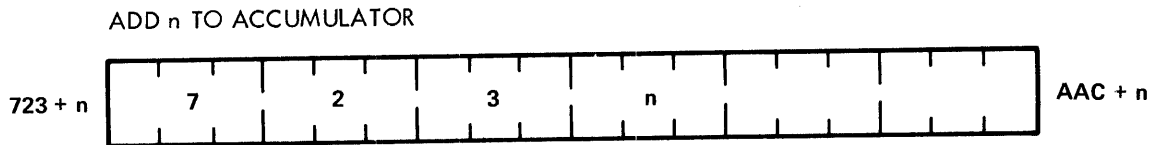
ADD TO INDEX REGISTER



15-0914

Mnemonic Name	AXR + n
Octal Code	737000 + n (n = 9 bits)
Time	2 cycles (1 memory cycle)
Operation	n, a signed 9-bit (8 bits plus sign) 2's complement integer is added to the content of the Index register, and the result is placed in the Index register.
Symbolic	XR + N to XR

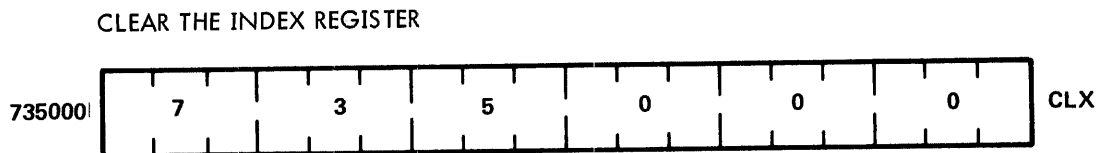
ADD n TO ACCUMULATOR



15-0915

Mnemonic Name	AAC + n
Octal Code	723000 + n (n = 9 bits)
Time	2 cycles (1 memory cycle)
Operation	n, a signed 9-bit (8 bits plus sign) 2's complement binary number, is added to the content of the Accumulator, and the result is placed into the Accumulator. The Link will not be complemented when overflow occurs.
Symbolic	AC + N to AC

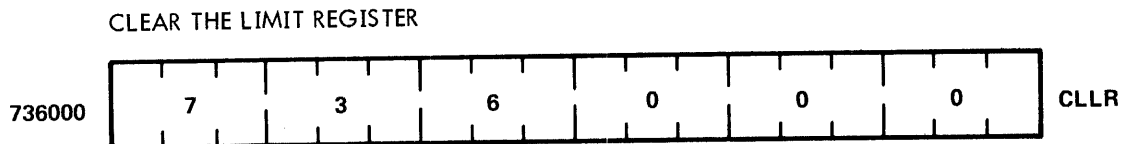
CLEAR THE INDEX REGISTER



15-0916

Mnemonic Name	CLX
Octal Code	735000
Time	2 cycles (1 memory cycle)
Operation	The content of the Index register is replaced with all 0s. Former content is lost.
Symbolic	0 to XR

CLEAR THE LIMIT REGISTER



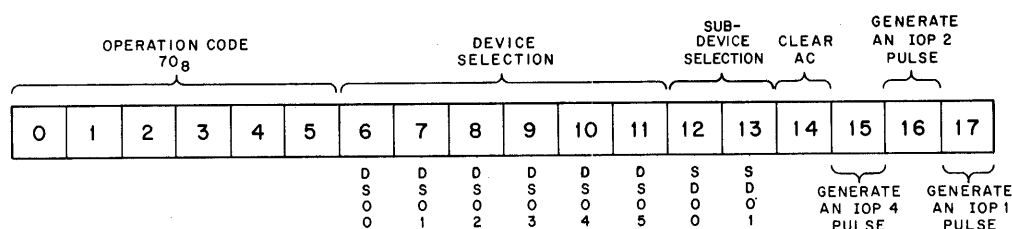
15-0917

Mnemonic Name	CLLR
Octal Code	736000
Time	2 cycles (1 memory cycle)
Operation	The content of the limit register is replaced with all 0s. The former content is lost.
Symbolic	0 to LR

Input/Output Transfer Instructions

Input/Output transfer (IOT) instructions initiate transmission of signals via the I/O bus to control peripheral devices, sense their status, and effect information transfers between them and the central processor. XVM IOT instructions contain the following information (Figure 6-5).

1. An operation code of 70_8 .
2. An 8-bit device selection code to differentiate between up to 256 peripheral devices (selection logic in a device's I/O bus interface responds only to its preassigned code). In normal practice, bits 6 through 11 perform the primary device differentiation between up to 64 devices with bits 12 and 13 coded to select an operational mode or subdevice. A number of these device codes are hardwired into the processor and cannot be used to control peripheral devices.
3. A command code (bits 14 through 17) capable of being microprogrammed to clear the AC and issue up to three pulses via the I/O bus.



15-0203

Figure 6-5 IOT Instruction Word Format

The two machine cycles required to execute an IOT instruction consists of decoding of the IOT from the central processor's memory input buffer, synchronization of the central and I/O processors, issuing three sequential cycles of $1\ \mu\text{s}$ each to ensure IOP pulses at event times 1, 2, and 4, and finally, the fetch of the next instruction to be executed. Bit 14 can be programmed to clear the Accumulator at event time 1 of the IOT instruction. Bits 15-17 can be microprogrammed in any manner to produce a pulse on the I/O bus for each bit set. Bit 17 causes an IOP 1 pulse, or the first pulse generated, and is normally used for testing the Device Status flags. Bit 16 generates an IOP 2 pulse, the second pulse, and can be used in transmitting to or from a device to the processors. On "In" transfers, data is ORed from the I/O bus into the Accumulator; therefore, bit 14, clear the Accumulator, is typically used when loading the accumulator from a device. Bit 15 produces IOP 4 pulse, the third pulse, and is used for control and transfer of data from the Accumulator to the device. A summary of IOP pulses is as follows (Figure 6-6):

1. IOP1 is normally used in an I/O skip instruction to test a Device flag; however, it can be used as a command pulse or a load of a device. It cannot be used to initiate a "read from" a device.
2. IOP2 is usually used to transfer data from the device to the computer, or to clear a device information register; it cannot be used to determine a "skip" condition.
3. IOP4 is usually used to transfer data from the computer to the device; it cannot be used to determine a "skip" condition or to initiate a read from a device.

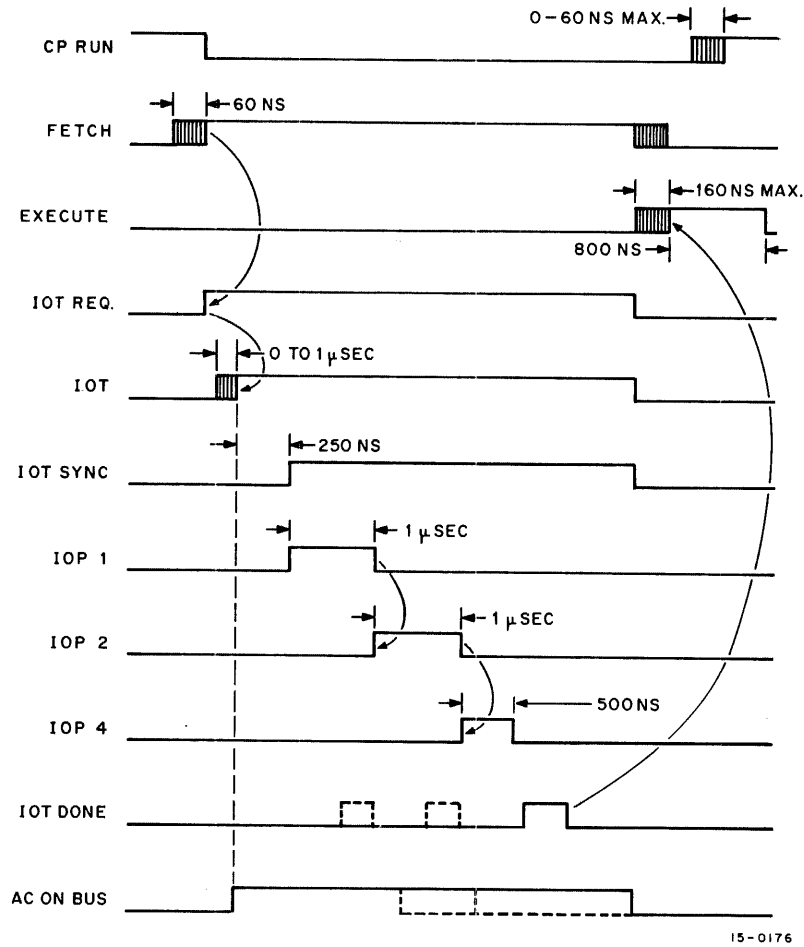


Figure 6-6 IOT Instruction Timing

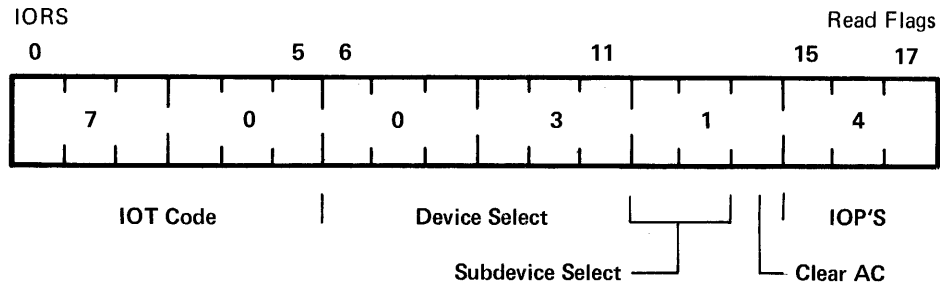
Programming Note

Execution of an IOT instruction and the next instruction in sequence cannot be interrupted; i.e., the XVM does not grant an interrupt request until the instruction following an IOT (and which is not an IOT itself) has completed its function.

XVM IOTs

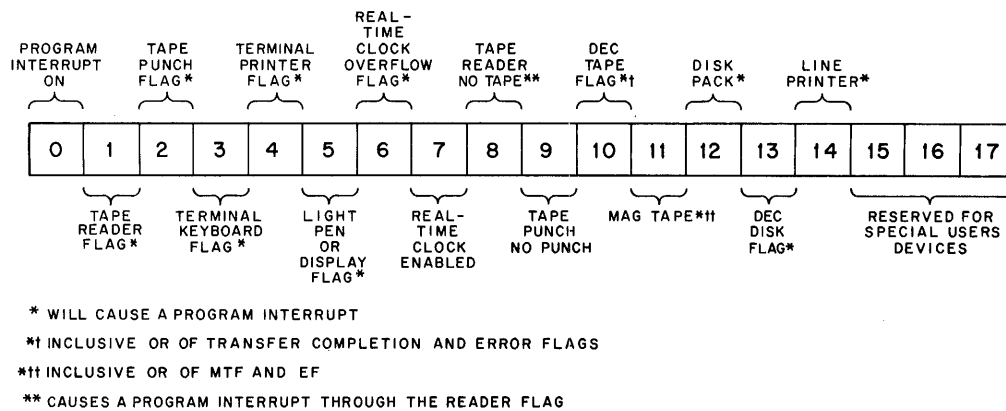
NOTE

An attempt to execute an IOT when the XVM System is in User mode with relocation engaged, will cause a trap unless the IOT ENABLE FUNCTION has been set in the memory processor.



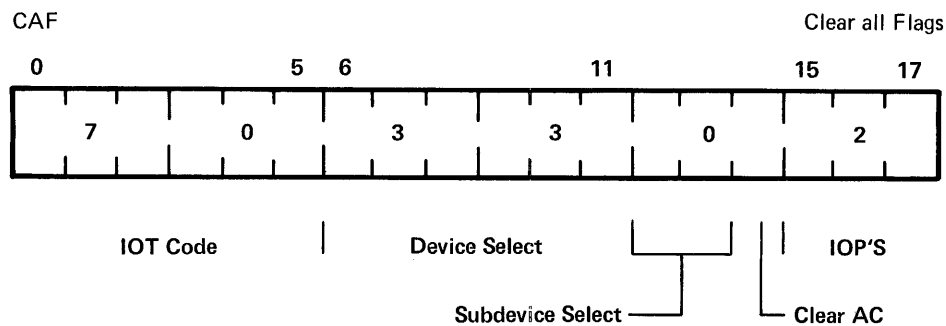
15-0944

The IORS read status instruction causes the transfer of an 18-bit system status word from the I/O bus to the Accumulator. During this instruction, each of the internal and external system devices gates its status bit onto preassigned data lines. The I/O processor transfers these bits to the Accumulator. Figure 6-7 shows the word/status/bit assignment.



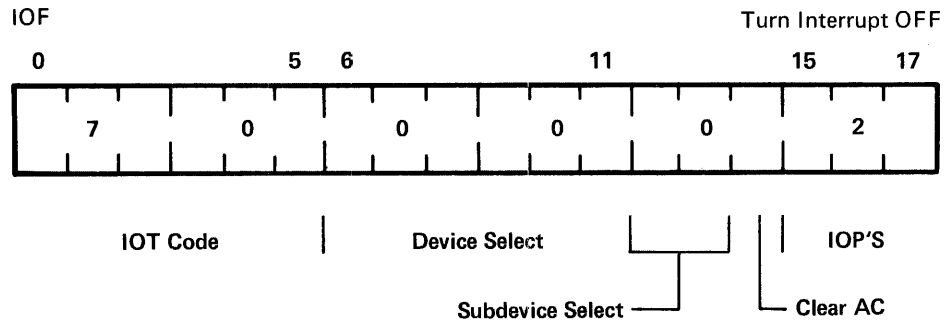
15-0202

Figure 6-7 IORS Word Status Bit Assignments



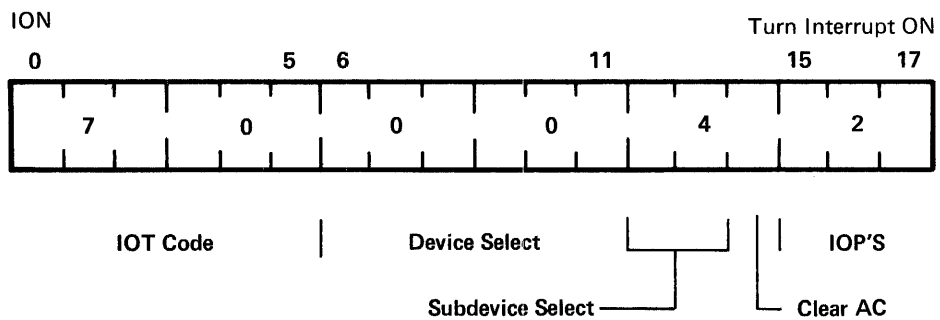
15-0945

The CAF instruction gates a pulse to the I/O bus to initialize (clear) all flags of any device that can call for interrupt service. Customer-installed equipment should make use of this pulse to reset flags and registers that must be cleared for system initiation. This instruction should not be used in an operating system controlled environment because it will interrupt on-going activities.



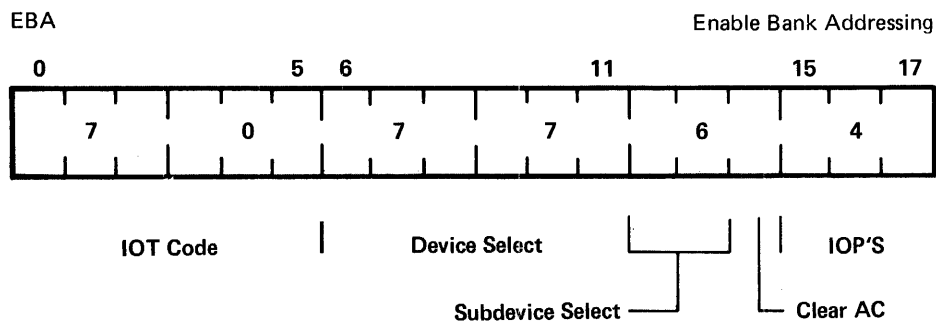
15-0946

The IOF input/output instruction turns off the program interrupt facility of the exchange.



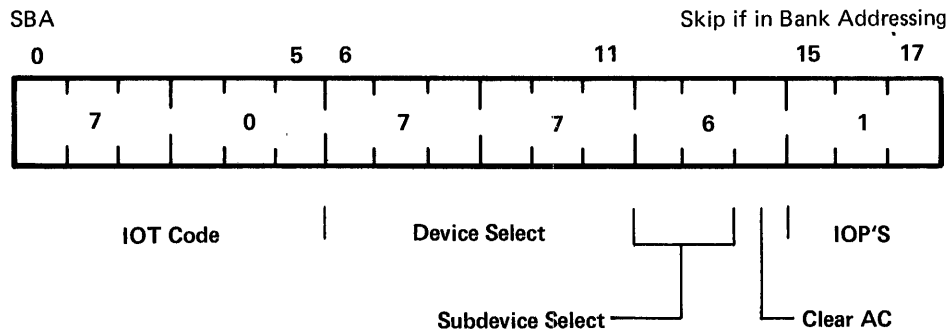
15-0947

The ION program interrupt facility is enabled.



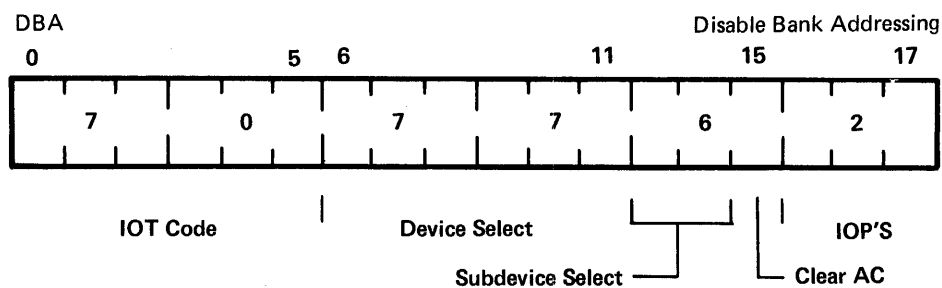
15-0948

The Index register is disabled and the sixth bit (bit 5), normally used to indicate an indexed operation, is gated to the memory address field, permitting direct addressing of 8192 words of memory.



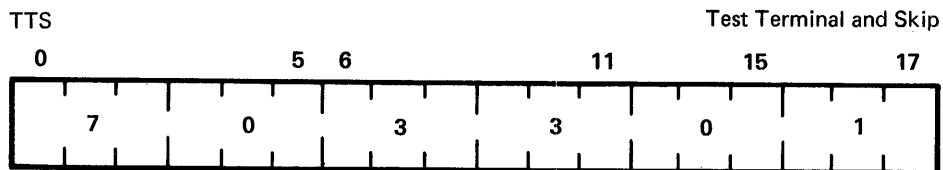
15-0949

If in Bank Addressing mode, the next instruction is skipped.



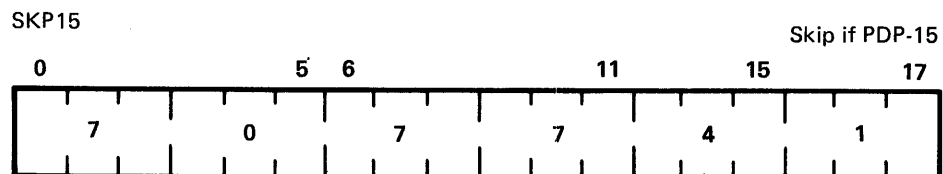
15-0950

Bank Address mode is disabled, and the XVM operates with indexing and addresses 4096 words of memory directly.



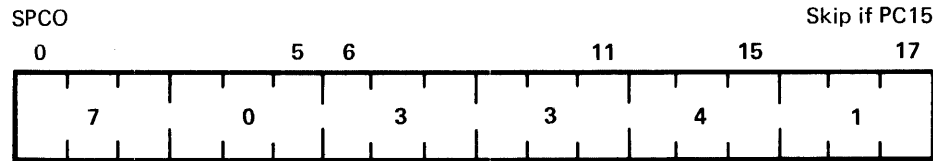
15-0951

Test if console terminal is connected to the XVM. Skip the next instruction if it is.



15-0952

Skip the next instruction if the processor is a PDP-15 or XVM.



15-0953

Skip the next instruction if a PC15 is connected to the system.

Console Device Keyboard

Mnemonic	Code
KSF	700301

Description

Skip on Keyboard Flag – Tests the console terminal keyboard flag and causes the next instruction to be skipped if the flag is set, indicating that the keyboard control has assembled a character from the terminal device.

KRB	700312

Read Keyboard Buffer – This IOT clears the AC and then reads the contents of the keyboard buffer into AC bits 10-17, and clears the keyboard flag.

KRS	700332

Keyboard Reader Select – This IOT clears the AC, reads the contents of the keyboard buffer into AC bits 10-17, and enables the keyboard reader to advance another character. Reading from the keyboard reader is done in full duplex mode (no character echo). This IOT can also be used to read, full duplex, from terminal device keyboard.

Console Device Printer

Mnemonic	Code
TSF	700401

Description

Skip on Console Printer Flag – Tests the status of the printer flag to determine if the last character has been printed. If the flag is set, the next instruction will be skipped.

TCF	700402

Clear Console Printer Flag – Clears the Printer flag which had been set at the completion of the previous character.

TLS	700406

Load and Select Console Printer – Clears the Printer flag, loads the printer buffer from AC bits 10-17, and initiates printing of the character. The flag is set when printing is completed.

6.2 EXTENDED INSTRUCTION SET

Extended Arithmetic Element

The extended arithmetic element (EAE) and its instructions, identified by an operation code of 64₈, perform high-speed data manipulation and multiply-divide operations as specified by microprogramming of individual instructions. Figures 6-8 through 6-12 illustrate the microinstruction capabilities for register setup, data shift, normalize, multiply, and divide.

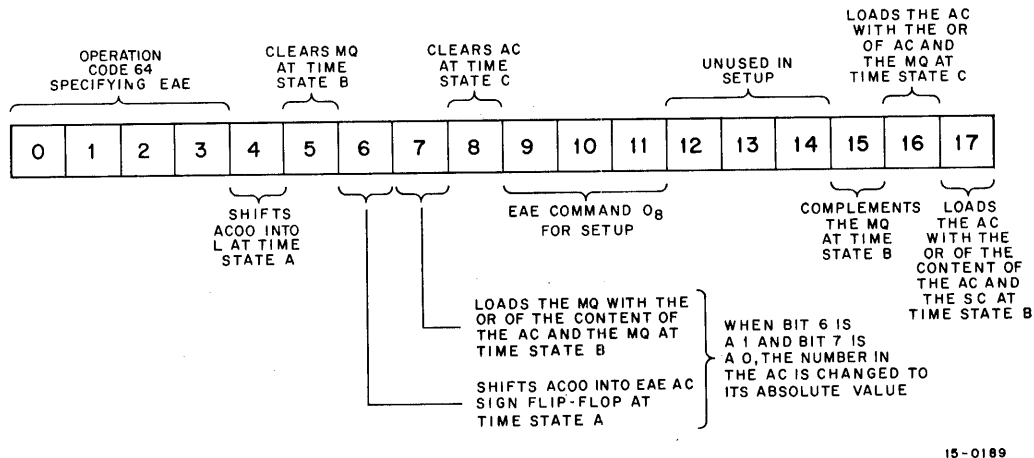


Figure 6-8 EAE Setup Microinstructions

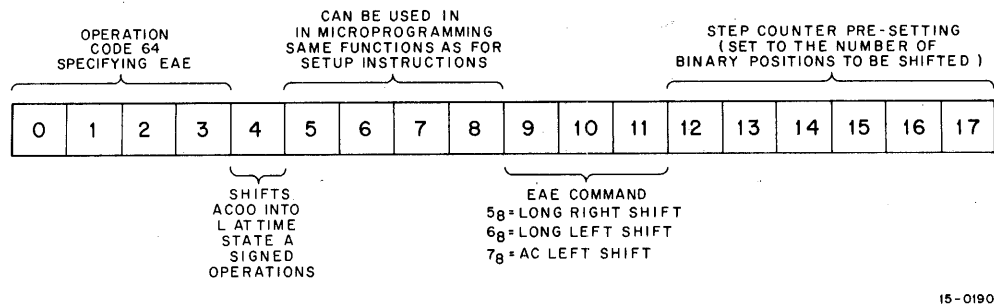


Figure 6-9 EAE Shift Microinstructions

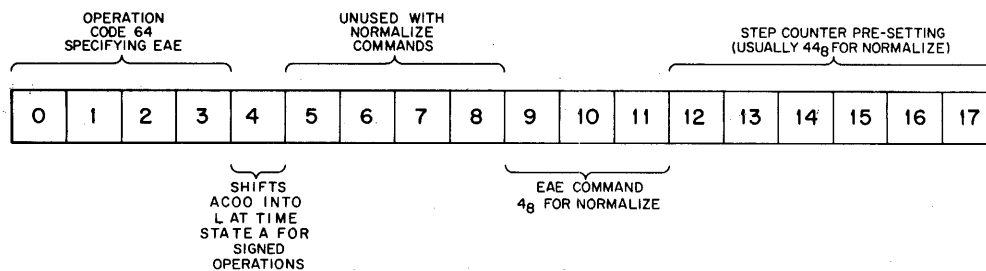
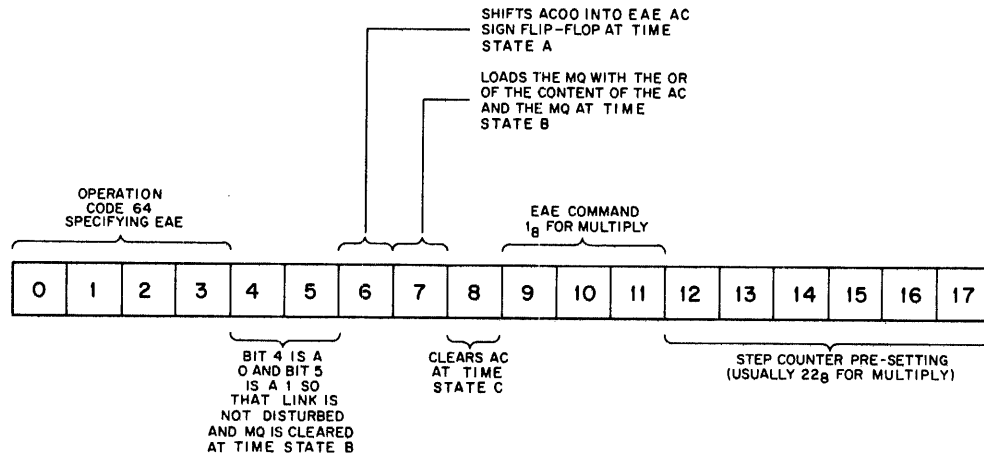
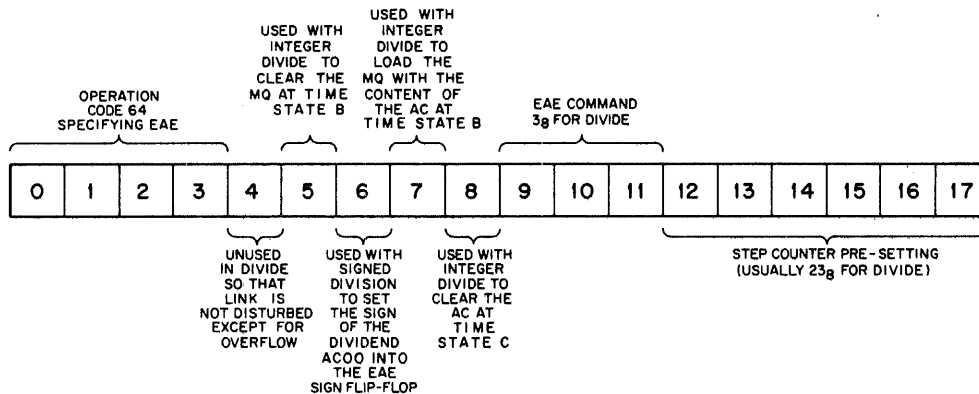


Figure 6-10 EAE Normalize Microinstructions



15-0192

Figure 6-11 EAE Multiplication Microinstructions



15-0193

Figure 6-12 EAE Division Microinstructions

The time required to execute an EAE instruction is a function of the operation and/or the shift, or step count specified by programming. In general, the following considerations apply to the different types of EAE operations:

1. All setup instructions require 1.325 microseconds.
2. Long register shift instructions require a time equal to 2.915 microseconds plus 0.133 microseconds per "n-1" bit-position shifts. This count is specified by the addition of n(octal) to the instruction code. For example, the input of the symbolic instruction LLS + 14 to the XVM assembler would result in an instruction code that specified a long left shift of the AC and MQ (taken as a 36-bit register) 12₁₀-bit positions to the left. This instruction would require 4.77 microseconds.
3. The ASL and ALSS instructions, respectively, AC left shift and AC left shift signed, also require the specification of "n."

4. The normalizing instructions, NORM and NORMS, require an execution time equal to 2.9 microseconds plus 0.133 microseconds per number of bit positions shifted to normalize (AC_0 is not equal to AC_1) quantity. These instructions are microprogrammed to set the 6-bit step count to $44_8(36_{10})$. Hence, $-xx + n_x$ (the step count is entered in 2's complement notation at execution) equals the biased scale factor of a normalized quantity.
5. Multiply instructions require a time equal to 7.4 microseconds. Multiply instructions are microprogrammed to set the step count to $22_8(18_{10})$, representing the multiplication of one 18-bit quantity (sign bit and 17 magnitude bits for signed quantities) by another to produce a 36-bit product. Where such precision is not required, the microprogrammed step count can be decreased by subtracting the appropriate number "n" (octal) from the instruction code. The product is always left-justified in the AC, MQ. If "-n" is appended to a multiply instruction, the "n" low-order bits in the long register are meaningless.
6. Divide instructions require a time equal to 7.65 microseconds. Divide instructions are microprogrammed to set count to $23_8(19_{10})$, representing division of a 36-bit dividend (actual or implied) by an 18-bit divisor. Where such precision is not required, the microprogrammed step count can be decreased by subtracting the appropriate number "n" (octal) from the instruction code). For example, the symbolic instruction DIV-12 would result in a right-justified quotient with the most significant bit in MQ_9 . The execution time is decreased in accordance with the decrease in the step count.

EAE Microinstructions

Figure 6-13 and Tables 6-1 and 6-2 describe the EAE instructions and illustrate the microinstructions of the EAE instructions. If an existing instruction is not satisfactory, the programmer can combine the appropriate microinstructions to achieve the required result.

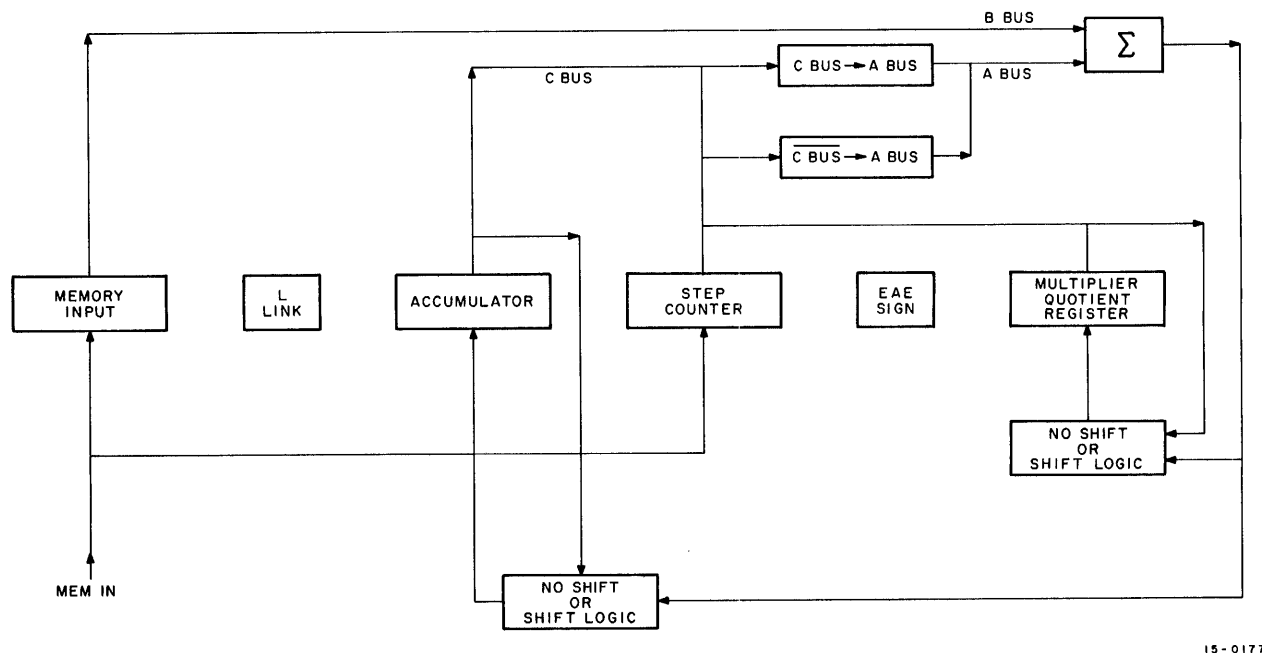


Figure 6-13 EAE Simplified Block Diagram

Table 6-1
EAE Microinstructions

EAE TIME STATES	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	EAE OP CODE (64) COMMON EVENTS (UNLESS OTHERWISE NOTED) AC → C BUS C BUS → A BUS			ACO → L			LD AC • AC → AC ACO → EAE SIGN	IF BITS = 10 and ACO = 1		EAE COMMAND 000 Setup 000 Multiply 010 011 Divide 100 Normalize 101 Long Right 110 Long Left 111 AC Left	EAE COMMAND ≠ 000 LOAD STEP COUNT							
B	MQ → C BUS C BUS → A BUS LD MQ • MQ → MQ					DISABLE MQ → C BUS		AC → C BUS • ACV MQ → MQ			EAE COMMAND = 000 (SETUP) C BUS → A BUS • MQ → MQ							
C	AC → C BUS C BUS → A BUS LD AC • AC → AC								DISABLE AC → C BUS		SC → C BUS • ACV SC → AC MQ → C BUS • ACV MQ → AC							
D	NO OPERATION																	
E,F	(EAE COMMAND ≠ 000) ALL SHIFT, MULTIPLY AND DIVIDE OPERATIONS																	

15-0422

Table 6-2
EAE Microinstructions

Bit Positions	Binary Code	Function
4	1	Enter the content of AC ₀ in the Link for signed operations.
5	1	Clear the MQ.
6	1	Read the content of AC ₀ into the EAE AC Sign register prior to carrying out a signed multiply and divide operation.
6,7	10	Take the absolute value of the AC. Takes place after the content of AC ₀ is read into the EAE AC Sign register.
7	1	Inclusive OR the AC with the MQ and read into MQ.
8	1	Clear the AC.
9,10,11	000	Setup. Accompanies code in bits 15, 16, and 17.
9,10,11	001	Multiply. Causes the number in the MQ to be multiplied by the number in the memory location following this instruction. If the EAE AC Sign register is 1, the MQ is complemented prior to multiplication. The exclusive OR of the EAE AC sign and the Link is entered in the EAE Sign register. The product is in the AC and MQ, with the lowest order bit in MQ bit 17. At completion, the Link is cleared and if the EAE sign is a 1, the AC and MQ are complemented.
9,10,11	010	Unused operation code.
9,10,11	011	Divide. Causes the 36-bit number in the AC and MQ to be divided by the 18-bit number in the Memory register following the instruction. If the EAE AC sign is 1, the MQ is complemented prior to starting the division. The exclusive OR of AC₀ and the Link is placed in the EAE Sign register. The AC portion of the dividend must be less than the divisor or divide overflow occurs. In such cases, the Link is set, and divide does not occur. Otherwise, the Link is cleared. At completion of this instruction, if the EAE sign was a 1, the MQ is complemented. Thus, the remainder has the sign of the dividend.

Table 6-2 (Cont)
EAE Microinstructions

Bit Positions	Binary Code	Function
9,10,11	101	Long right shift. Causes the AC and MQ to be shifted right together as a 36-bit register the number of times specified in the instruction. On each step, the Link fills AC bit 0, AC bit 17 fills MQ bit 0, and MQ bit 17 is lost. The Link remains unchanged.
9,10,11	110	Long left shift. Causes the AC and MQ to be shifted left together, the number of times specified in the instruction. On each step, MQ bit 17 is filled by the Link; the Link remains unchanged. MQ bit 0 fills AC bit 17, and AC bit 0 is lost.
9,10,11	100	Normalize. Causes the AC and MQ to be shifted left together, until the step count is equaled or AC bit 0 is not equal to AC bit 1. MQ bit 17 is filled by the Link; the Link is not changed. The step count of this instruction is normally 44 (octal). When the step counter is read into the AC, it contains the number of shifts minus the initial shift count as a 2's complement 6-bit number.
9,10,11	111	Accumulator left shift. Causes the AC to be shifted left the number of times specified in the shift count. AC bit 17 is filled by the Link, but the Link is unchanged.
12-17		Specify the step count for all EAE commands (9-11) except the setup command.
15	1	The setup command only, causes the MQ to be complemented.
16	1	The setup command only, causes the MQ to be inclusively ORed with the AC and the result placed in AC.
17	1	The setup command only, causes the AC to be inclusively ORed with the SC and the results placed on AC bits 12-17.

BASIC EAE INSTRUCTION

BASIC EAE INSTRUCTION

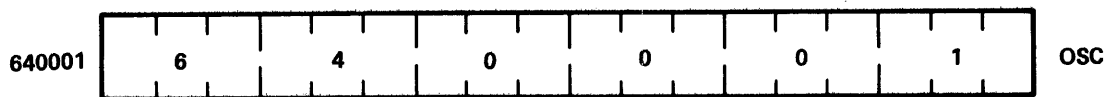


15-0918

Mnemonic Name	EAE + n
Octal Code	640000
Operation	The addition of n (octal) to the mnemonic converts the basic instruction into a microcoded instruction to accomplish a setup, shift, or arithmetic operation not already in the instruction repertoire. Refer to Table 6-1 for descriptions of the functional use of the individual bits of an EAE instruction. The sole restriction for the development of n is that the microcoded operations must not occur during the same time state, if they logically conflict.
Symbolic	No operation.

INCLUSIVE OR SC WITH AC

INCLUSIVE OR SC WITH AC



15-0919

Mnemonic Name	OSC
Octal Code	640001
Operation	The contents of the AC are inclusively ORed with the 6-bit contents of the step counter (SC) on a bit-by-bit basis. The result is left in AC ₁₂₋₁₇ . If corresponding SC and AC bits are in the binary 1 state, the AC bit is set to 1. The previous contents of the AC are lost. The contents of the SC are unchanged.
Symbolic	SC OR AC to AC

INCLUSIVE OR MQ WITH AC

INCLUSIVE OR MQ WITH AC

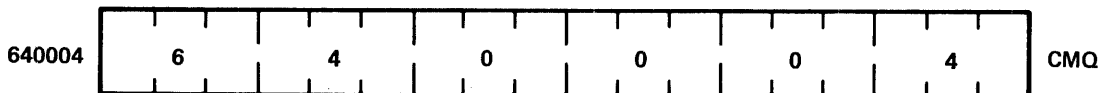


15-0920

Mnemonic Name Octal Code Operation Symbolic	OMQ 640002 The contents of the MQ are inclusively ORed with the contents of the AC on a bit-by-bit basis. The result is left in the AC. If corresponding MQ and AC bits are in the binary 0 state, the AC bit is cleared to 0. If either of the corresponding bits is in the binary 1 state, the AC bit is set to 1. The previous contents of the AC are lost. The contents of the MQ are unchanged. MQ OR AC to AC

COMPLEMENT MQ

COMPLEMENT MQ

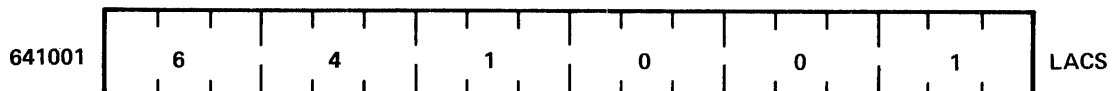


15-0921

Mnemonic Name Octal Code Operation Symbolic	CMQ 640004 Each bit of the MQ is set or cleared to the inverse of its current state. The previous contents of the MQ are lost. MQ to MQ

LOAD AC FROM SC

LOAD AC FROM SC



15-0922

Mnemonic Name Octal Code Operation Symbolic	LACS 641001 This microcoded instruction clears each bit of the AC to 0 and then enters the contents of the SC in AC₁₂₋₁₇. The previous contents of the AC are lost. The contents of the SC are unchanged. SC to AC

LOAD AC FROM MQ

LOAD AC FROM MQ



15-0923

Mnemonic Name	LACQ
Octal Code	641002
Operation	This microcoded instruction clears each bit of the AC to 0 and then enters the contents of the MQ in the AC. The previous contents of the AC are lost. The contents of the MQ are unchanged.
Symbolic	MQ to AC

LOAD AC WITH ABSOLUTE VALUE TO AC

LOAD AC WITH ABSOLUTE VALUE TO AC

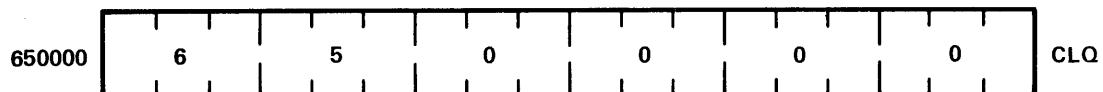


15-0924

Mnemonic Name	ABS
Octal Code	644000
Operation	A microcoded instruction which complements the contents of the AC (1's complement notation), if the content of AC ₀ is 1.
Symbolic	If AC ₀ = 1, -AC to AC

CLEAR MQ

CLEAR MQ

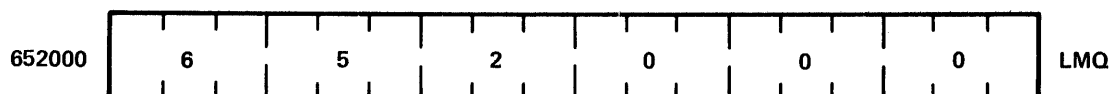


15-0925

Mnemonic Name	CLQ
Octal Code	650000
Operation	Each bit of the MQ is cleared to 0. The previous contents of the MQ are lost.
Symbolic	0 to MQ

LOAD MQ

LOAD MQ

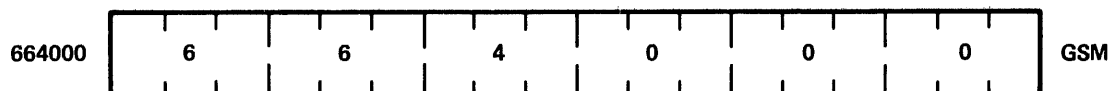


15-0926

Mnemonic Name	LMQ
Octal Code	652000
Operation	A microcoded instruction which clears each bit of the MQ to 0 and then enters the contents of the AC in the MQ. The previous contents of the MQ are lost. The contents of the AC are unchanged.
Symbolic	AC to MQ

GET SIGN AND MAGNITUDE OF AC

GET SIGN AND MAGNITUDE OF AC

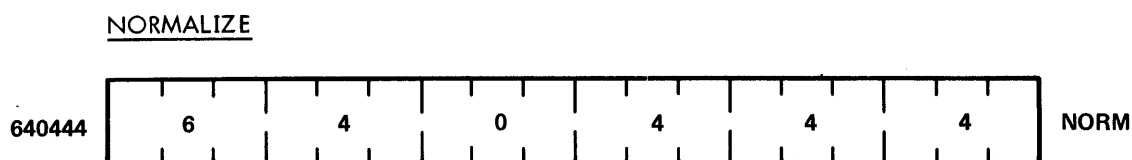


15-0927

Mnemonic Name	GSM
Octal Code	664000
Operation	A microcoded instruction which enters the contents of the AC ₀ in the Link and then complements the contents of the AC (1's complement notation), if AC ₀ is a 1. The previous content of the Link is lost.
Symbolic	AC ₀ to L If AC ₀ = 1, -AC to AC

EAE Shifting Instructions

NORMALIZE



15-0928

Mnemonic Name
Octal Code
Operation

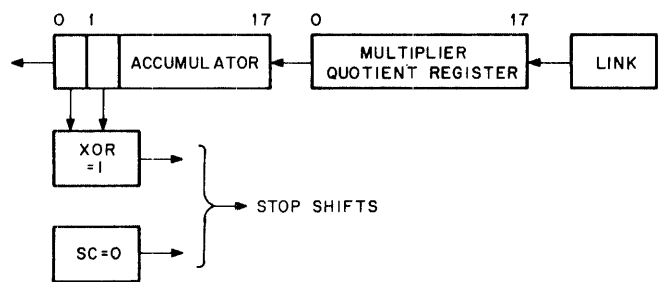
NORM
640444

The contents of the AC and the MQ are shifted left (i.e., leading zeros are shifted out) with the AC and MQ functioning as a serial 36-bit register until the content of the AC_0 does not agree with the content of AC_1 , i.e., the bits differ in their binary states, or the contents of the step counter reach zero.

This 6-bit counter is initialized to the 2's complement of $44_8(36_{10}\text{steps})$. The contents of the six low-order bits of the NORM instruction word specify the step count. For each shift step, the contents of MQ_0 enter AC_{17} and the contents shifted out of AC_0 are lost. The content of the Link, usually initialized to zero, enters MQ_{17} to replace the contents of vacated bits. If shifting halts because AC_0 does not equal AC_1 , the contents of the step counter reflect the number of steps executed to reach the condition. The counter's contents (2's complement of the step count plus the steps executed) are accessible through use of the OSC or LACS instruction.

Two free instructions follow the execution of the NORM instruction. A PI or API break cannot occur until the second instruction following the NORM instruction is completed.

Graphic



15-0194

NORMALIZE, SIGNED

NORMALIZE, SIGNED



15-0929

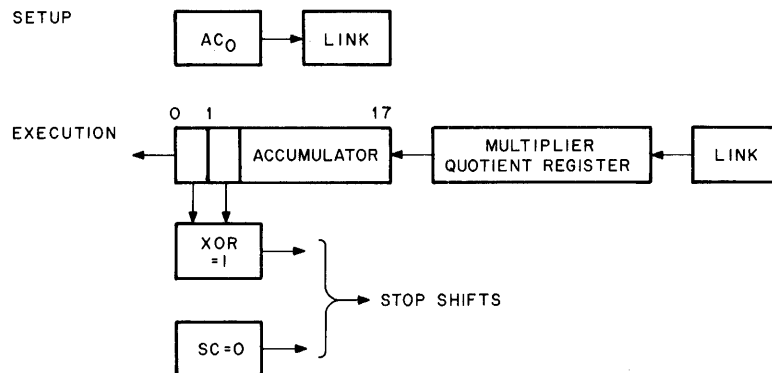
Mnemonic Name
Octal Code
Operation

NORMS
660444

The contents of AC_0 enter the Link. Then, the contents of the AC and the MQ are shifted left (i.e., leading zeros are shifted out) with the AC and MQ functioning as a serial 36-bit register until the contents of the AC_0 do not agree with the contents of AC_1 , i.e., the bits differ in their binary states, or the contents of the step counter reach zero.

This counter is initialized to the 2's complement of 44_8 (36_{10} steps). The contents of the six low-order bits of the NORMS instruction word specify the step count. For each shift step, the content of MQ_0 enters AC_{17} and the contents shifted out of AC_0 are lost. The content of the Link enters MQ_{17} to replace the contents of vacated bits. If shifting halts because AC_0 does not equal AC_1 , the contents of the step counter reflect the number of steps executed to reach the condition. The counter's contents (2's complement of the step count plus the steps executed) are accessible through use of the OSC or LACS instruction. Two free instructions follow the execution of the NORMS instruction. A PI or API break cannot occur until the second instruction following the NORMS instruction is completed.

Graphic



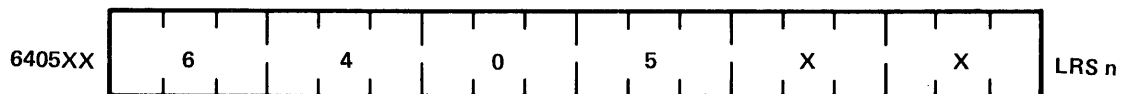
15-0195

Programming Note

The EAE instruction set does not provide a convenient way to restore the contents of the step counter. To obviate the need to do so, the XVM is designed to inhibit program or automatic priority interrupts occurring for two instructions following the NORM or NORMS (normalize, signed) instruction. These two instructions are normally a DAC followed by a LACS which saves the contents of the AC, then puts the contents of the step counter in the AC. Thus, if interrupt-accessed subroutines make use of the EAE, the AC and MQ are the only registers that must be preserved during the interrupt, then restored in the EAE at the completion of the interrupt service.

LONG RIGHT SHIFT

LONG RIGHT SHIFT



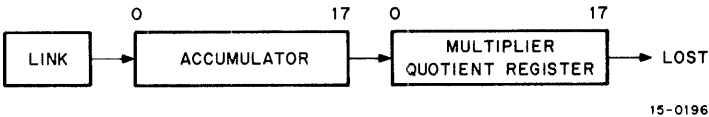
15-0930

Mnemonic Name
Octal Code
Operation

LRS n
6405XX + n

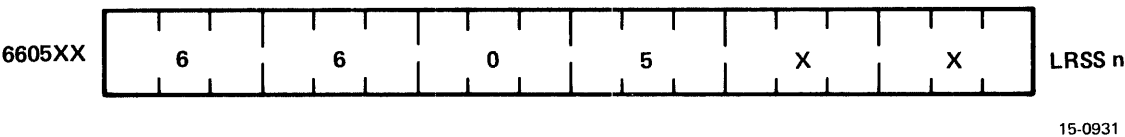
The AC and MQ function as a 36-bit register to permit serial shifting of their contents "n" bit positions to the right, "n" being specified by the contents of the six low-order bits of the instruction word. Shifting halts when the contents of the step counter, initialized to the 2's complement of "n", reach zero. For each shift step, the contents of AC₁₇ enter MQ₀ and the contents shifted out of MQ₁₇ are lost. The contents of the Link, usually initialized to zero, remain unchanged and enter AC₀ at each step to replace the contents of vacated bits.

Graphic



LONG RIGHT SHIFT, SIGNED

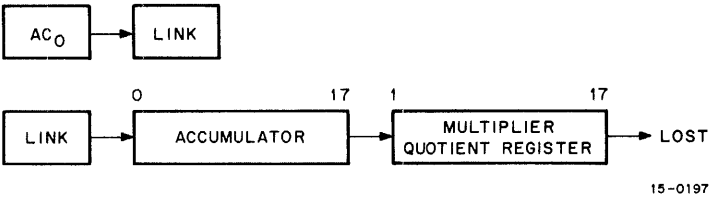
LONG RIGHT SHIFT, SIGNED



Mnemonic Name
Octal Code
Operation

LRSS n
6605XX + n
The content of AC_0 is entered in the Link. Then, the AC and the MQ function as a 36-bit register to permit serial shifting of their contents “n” bit positions to the right, “n” being specified by the contents of the six low-order bits of the instruction. Shifting halts when the contents of the step counter, initialized to the 2’s complement of “n”, reach zero. For each shift step, the contents of AC_{17} enter MQ_0 and the contents shifted out of MQ_{17} are lost. The content of the Link remains unchanged and enters AC_0 at each step to replace the contents of vacated bits.

Graphic



LONG LEFT SHIFT

LONG LEFT SHIFT



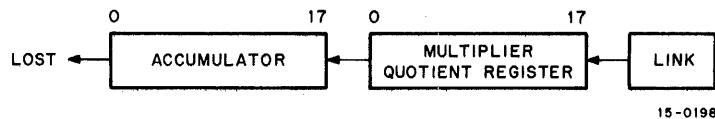
15-0932

Mnemonic Name
Octal Code
Operation

LLS n
6406XX + n

The AC and the MQ function as a 36-bit register to permit serial shifting of their contents "n" bit positions to the left, "n" being specified by the contents of the six low-order bits of the instruction word. Shifting halts when the contents of the step counter initialized to the 2's complement of "n", reach zero. For each shift step, the contents of MQ₀ enter AC₁₇ and the contents shifted out of AC₀ are lost. The content of the Link, usually initialized to zero, remains unchanged and enters MQ₁₇ at each step to replace the contents of vacated bits.

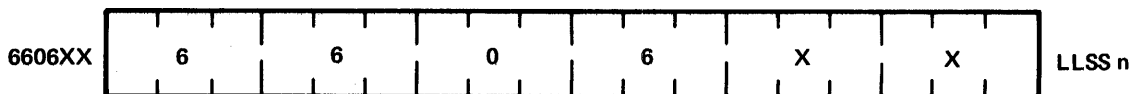
Graphic



15-0198

LONG LEFT SHIFT, SIGNED

LONG LEFT SHIFT, SIGNED



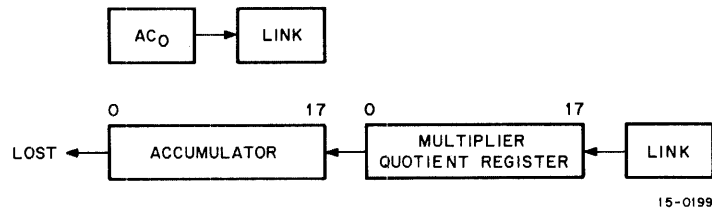
15-0933

Mnemonic Name
Octal Code
Operation

LLSS n
6606XX + n

The content of AC is entered in the Link. The AC and MQ function as a serial 36-bit register to permit serial shifting to their contents "n" bit positions to the left, "n" being specified by the contents of the six low-order bits of the instruction word. Shifting halts when the contents of the step counter, initialized to the 2's complement of "n", reach zero. For each shift step, the contents of MQ₀ enter AC₁₇ and the contents shifted out of AC₀ are lost. The content of the Link remains unchanged and enters MQ₁₇ at each step to replace the contents of vacated bits.

Graphic



ACCUMULATOR LEFT SHIFT

ACCUMULATOR LEFT SHIFT



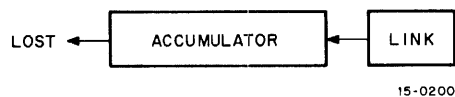
Mnemonic Name
Octal Code
Operation

ALS n

6407XX + n

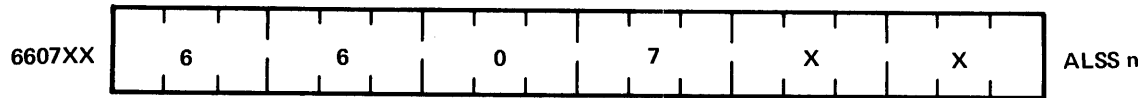
The contents of the AC are shifted “n” bit positions to the left, “n” being specified by the contents of the six low-order bits of the instruction word. Shifting halts when the contents of the step counter, initialized to the 2’s complement of “n”, reach zero. For each shift step, the content of the Link, usually initialized to zero, enters AC₁₇ to replace the contents of vacated bits. The contents shifted out of AC₀ are lost.

Graphic



ACCUMULATOR LEFT SHIFT, SIGNED

ACCUMULATOR LEFT SHIFT, SIGNED



15-0935

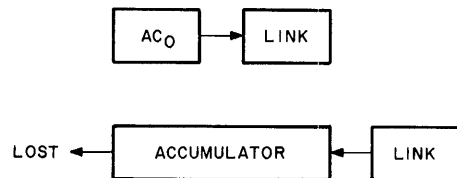
Mnemonic Name
Octal Code
Operation

ALSS n

6607XX + n

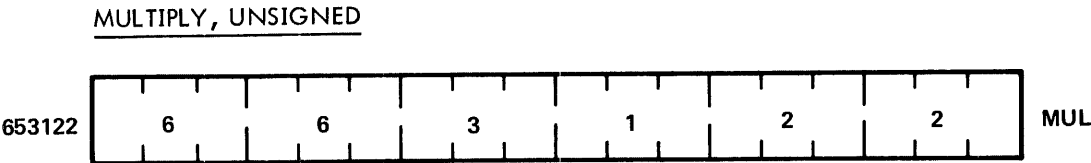
The content of AC_0 enters the Link. Then, the contents of the AC are shifted "n" bit positions to the left, "n" being specified by the contents of the six low-order bits of the instruction word. Shifting halts when the contents of the step counter, initialized to the 2's complement of "n", reach zero. For each shift step, the content of the Link remains unchanged and enters AC_{17} to replace the contents of vacated bits. The contents shifted out of AC_0 are lost.

Graphic



15-0201

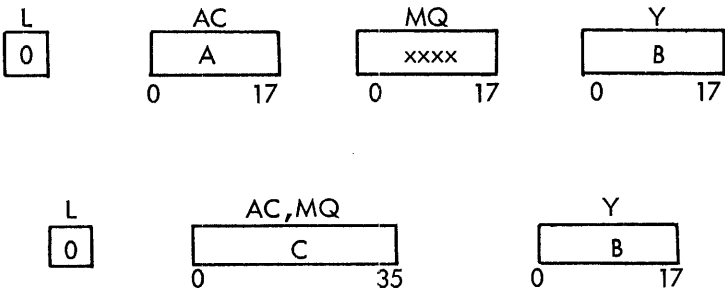
MULTIPLY, UNSIGNED



15-0936

Mnemonic Name	MUL
Octal Code	653122
Operation	Multiply the contents of Memory register Y (the multiplicand) by the contents of the MQ (the multiplier), and place the resulting 36-bit product in the AC and the MQ with the more significant half appearing in the AC. The address of Y is taken to be sequential to the address of the MUL instruction word. Prior to this instruction, the contents of the Link must be zero and the multiplier must be entered in the AC. During the set-up phase of MUL, the multiplier is transferred to the MQ, the AC is cleared to zero, and the step counter is initialized to the 2's complement of 22 ₈ (18 ₁₀ steps); the six low-order bits of the instruction word specify the step count. The arithmetic phase, executed as multiplication of one unsigned quantity by another (18 bits, binary point of no consequence), halts when the step counter counts up to zero. The content of the Link remains zero. The contents of Y are unchanged. The program resumes as the next instruction (Memory register Y + 1).
Symbolic	0 to SC Y±MQ to (AC,MQ) 0 to L PC + 2 to PC
Data Structure Pre-execution	C = A±B

Post execution



Instruction Sequence

Register	Contents
Y-2	LAC Multiplier
Y-1	MUL
Y	Multiplicand
Y+1	Next Instruction

MULTIPLY, SIGNED

MULTIPLY, SIGNED



15-0937

Mnemonic Name
Octal Code
Operation

Muls
657122

Multiply the contents of Memory register Y (the multiplicand) by the contents of the MQ (the multiplier), and place the signed product in the AC and MQ with the sign notation and more significant portion in the AC. Bits AC₀ and AC₁ each receive the sign of the product; the remaining AC and MQ bits represent the magnitude of the product in 1's complement form. The address of Y is taken to be sequential to the address of the Muls instruction word. The contents of the Y are taken to be the absolute value of the multiplicand; the contents of the Link are taken to be the original sign of the multiplicand (Muls assume previous execution of an EAE GSM instruction, q.v.). Just prior to this Muls instruction, the multiplier must be entered in the AC. During the setup phase of the Muls instruction, the multiplier is transferred to the MQ and 1's complemented if negative, the AC is cleared to zero, and the step counter is initialized to the 2's complement of 22₈(18₁₀ steps); the six low-order bits of the Muls instruction word specify the step count. The arithmetic phase, executed as multiplication of one signed quantity by another (sign bit plus 17 magnitude bits, binary point position of no consequence), halts when the step counter counts up to zero. The link is cleared to zero. The contents of Y are unchanged. The program resumes at the next instruction (Memory register Y + 1).

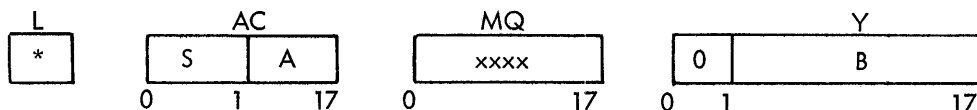
Symbolic

0 to SC
Y ± MQ to (AC, MQ)
0 to L

Data Structure
Pre-execution

PC + 2 to PC
C = A ± B

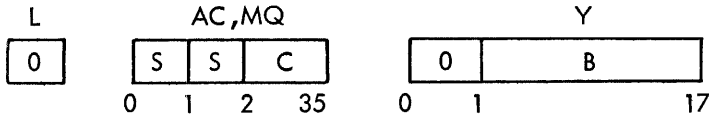
Pre-execution:



*Original sign of B.

Post execution

Post execution:



$S = L \nabla \text{Sign } A$

Instruction Sequence

Register	Contents
Y-5	LAC Multiplicand
Y-4	GSM (take absolute value and save sign in Link)
Y-3	DAC Y
Y-2	LAC Multiplier
Y-1	MULS
Y	Multiplicand (absolute value)
Y + 1	Next Instruction

DIVIDE, UNSIGNED

DIVIDE, UNSIGNED



15-0938

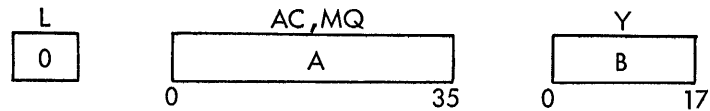
Mnemonic Name
Octal Code
Operation

DIV
640323
Divide the contents of the AC and the MQ (an unsigned 36-bit dividend) by the contents of Memory register Y (the divisor). The resulting quotient appears in the MQ. The remainder is in the AC. The address of Y is taken to be sequential to the address of the DIV instruction word. Prior to this, the contents of the Link must be zero, and the dividend must be entered in the AC and MQ (LAC least significant half). If the divisor is not greater than the AC portion of the dividend, divide overflow occurs (magnitude of quotient exceeds the 18-bit capacity of the MQ), and the Link is set to one to signal the overflow condition; data in the AC and the MQ are of no value. A valid division halts when the step counter, initialized to the 2's complement of $23_8(19_{10})$ steps, counts up to zero (the six low-order bits of the DIV instruction word specify the step count). The contents of the Y are unchanged. The program resumes at the next instruction (Memory register Y + 1).

Symbolic

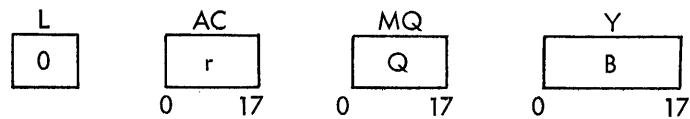
If $Y \leq AC$, 1 to L (divide overflow)
 If $Y > AC$, 0 to SC (AC, MQ)/Y to MQ (quotient), AC (remainder)
 0 to L
 $PC + 2$ to PC
 $A = BQ + r$

Data Structure
 Pre-execution



Post execution

(no overflow)



Instruction Sequence

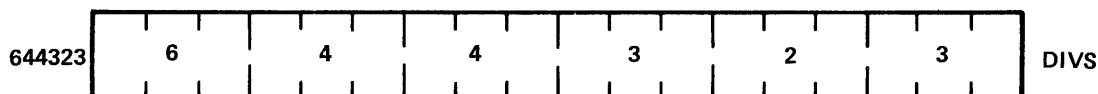
Register

Contents

Y-4	LAC Dividend (least significant half)
Y-3	LMQ
Y-2	LAC Dividend (most significant half)
Y-1	DIV
Y	Divisor
Y + 1	Next Instruction

DIVIDE, SIGNED

DIVIDE, SIGNED



15-0939

Mnemonic Name
Octal Code
Operation

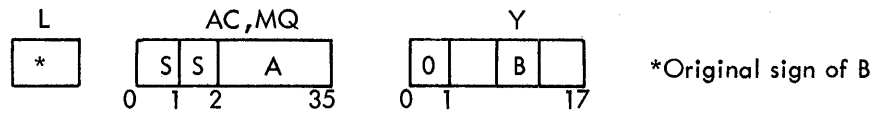
DIVS
644323

Divide the contents of the AC and MQ (a 36-bit signed dividend with the sign in bits AC_0 and AC_1 and the remaining 34 bits devoted to magnitude) by the contents of Memory register Y (the divisor). The resulting quotient appears in the MQ with the algebraically determined sign in bit MQ_{1-17} . The remainder is in the AC with bit AC_0 containing the sign of the dividend and bits AC_{1-17} containing the magnitude (1's complement). The address of Y is taken to be sequential to the address of the DIVS instruction word. The contents of Y are taken to be the absolute value of the divisor; the contents of the Link are taken to be the original sign of the divisor (DIVS assumes previous execution of an EAE GSM instruction, q.v.). Prior to this DIVS instruction, the dividend must be entered in the AC and MQ (LAC of least significant half, LMQ, and LAC of most significant half). The MQ portion of a negative dividend is 1's complement prior to the division. If the divisor is not greater than the AC portion of the dividend, divide overflow occurs (magnitude of the quotient exceeds the 17-bit plus sign capacity of the MQ), and the link is set to one to signal the overflow condition; data in the AC and the MQ are of no value. A valid division halts when the step counter, initialized to the 2's complement of 23_8 (19_{10} steps), counts up to zero (the six low-order bits of the DIVS instruction word specify the step count). The content of the Link is cleared to zero. The contents of Y are unchanged. The program resumes at the next instruction (Memory register Y + 1).

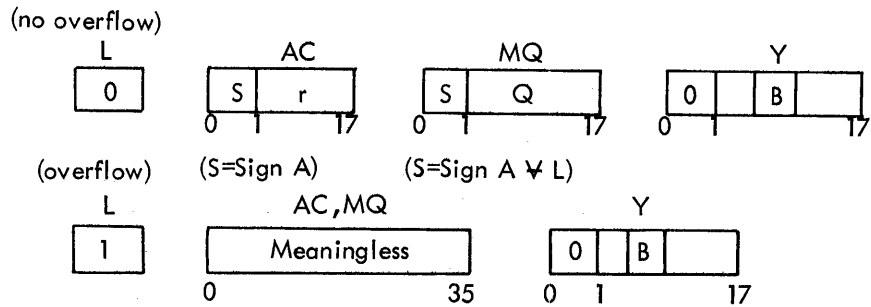
Symbolic

If $Y \leq AC$, 1 to L (divide overflow)
If $Y > AC$, 0 to SC (AC,MQ)/Y to MQ (quotient), AC (remainder)
0 to L
PC + 2 to PC

Pre-execution



Post execution

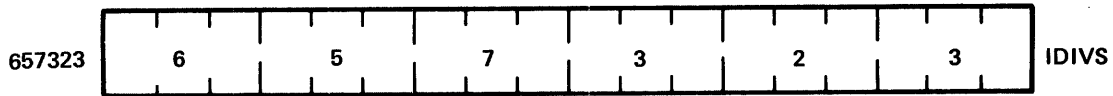


Instruction Sequence

Register	Contents
Y-7	LAC Divisor
Y-6	GSM
Y-5	DAC Divisor in Y
Y-4	LAC Dividend (least significant half)
Y-3	LMQ
Y-2	LAC Dividend (most significant half)
Y-1	DIVS
Y	Divisor (absolute value)
Y + 1	Next Instruction

INTEGER DIVIDE, SIGNED

INTEGER DIVIDE, SIGNED



15-0940

Mnemonic Name
Octal Code
Operation

IDIVS
657323

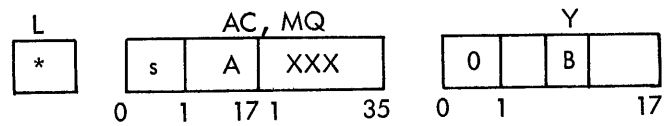
Divide the contents of the AC and the MQ (AC is zero, MQ contains a signed integer dividend) by the contents of Memory register Y (the divisor). The resulting quotient appears in the MQ with the algebraically determined sign in bit MQ_0 and the magnitude (1's complement) in bits $MQ_1 - 17$. The remainder is in the AC with bit AC_0 containing the sign of the dividend and bits $AC_1 - 17$ containing the magnitude (1's complement). The address of Y is taken to be sequential to the address of the IDIVS instruction word. The contents of Y are taken to be the absolute value of the divisor; the contents of the Link are taken to be the original sign of the divisor (IDIVS assumes previous execution of an EAE GSM instruction, q.v.). Prior to this IDIVS instruction, the dividend must be entered in the AC (the setup phase of IDIVS transfers the dividend to the MQ, clears the AC, and 1's complements the MQ if the dividend is negative). Divide overflow occurs only if division by zero is attempted; i.e., the quotient's magnitude will not exceed the 17-bit plus sign capacity of the MQ. The division halts when the step counter, initialized to the 2's complement of $23_8(19_{10})$ steps, counts up to zero (the six low-order bits of the IDIVS instruction word specify the step count). The contents of the Link are cleared to zero. The contents of Y are unchanged. The program resumes at the next instruction (Memory register $Y + 1$).

Symbolic

0 to SC
MQ/Y to MQ (quotient), AC (remainder)
0 to L
PC + 2 to PC

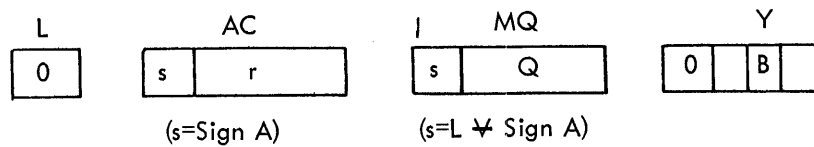
Data Structure
Pre-execution

$$A = B \cdot Q + r$$

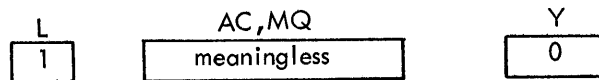


*Original sign of B

Post execution



If Y=0 (overflow)

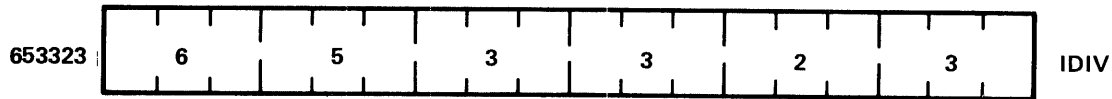


Instruction Sequence

Register	Contents
Y-5	LAC Divisor
Y-4	GSM
Y-3	DAC Divisor (absolute value) in Y
Y-2	LAC Dividend
Y-1	IDIVS
Y	Divisor (absolute value)
Y + 1	Next Instruction

INTEGER DIVIDE, UNSIGNED

INTEGER DIVIDE, UNSIGNED



15-0941

Mnemonic Name
Octal Code
Operation

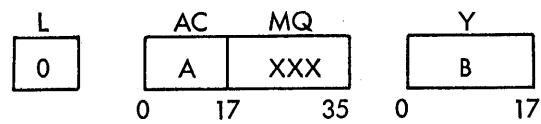
IDIV
653323

Divide the contents of the AC and the MQ (AC is zero, MQ contains an 18-bit integer dividend) by the contents of Memory register Y (divisor). The resulting quotient appears in the MQ; the remainder is in the AC. The address of Y is taken to be sequential to the address of the IDIV instruction word. Prior to this instruction, the contents of the Link must be zero, and the dividend must be entered in the AC (the setup phase of IDIV transfers the dividend to the MQ and clears the AC). Division overflow occurs only if division by zero is attempted, i.e., the quotient's magnitude will not exceed the 17-bit plus sign capacity of the MQ. The division halts when the step counter, initialized to the 2's complement of 23₀(19₁₀ steps), counts up to zero (the six low-order bits of the IDIV instruction word specify the step count). The content of the Link is cleared to zero. The contents of Y are unchanged. The program resumes at the next instruction (Memory register Y + 1).

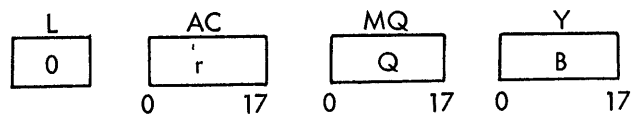
Symbolic

0 to SC
MQ/Y to MQ (quotient), AC (remainder)
0 to L
PC + 2 to PC

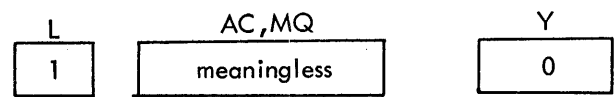
Pre-execution



Post execution



If Y=0 (overflow)



Instruction Sequence

Register	Contents
Y-2	LAC Dividend
Y-1	IDIV
Y	Divisor
Y + 1	Next Instruction

FRACTION DIVIDE, UNSIGNED

FRACTION DIVIDE, UNSIGNED



15-0942

Mnemonic Name
Octal Code
Operation

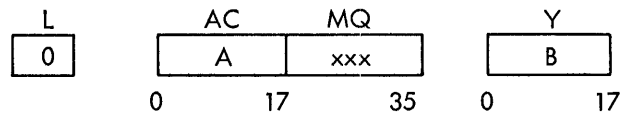
FRDIV
650323

Divide the contents of the AC and the MQ (AC contains an 18-bit fractional dividend, MQ is zeroed at setup) by the contents of Memory register Y (the divisor). The binary point is assumed at the left of AC₀. The quotient appears in the MQ; the remainder is in the AC. The address of Y is taken to be sequential to the address of the FRDIV instruction word. Prior to this instruction, the contents of the Link must be zero, and the dividend must be entered in the AC (the setup phase of FRDIV clears the MQ). If the divisor is not greater than the dividend, divide overflow occurs (magnitude of quotient exceeds the 18-bit capacity of the MQ), and the link is set to one to signal the overflow condition; data in the AC and the MQ are of no value. A valid division halts when the step counter, initialized to 23₈(19₁₀ steps), counts up to zero (the six low-order bits of the FRDIV instruction word specify the step count). The contents of the Link remain zero. The contents of Y are unchanged. The program assumes at the next instruction (Memory register Y + 1).

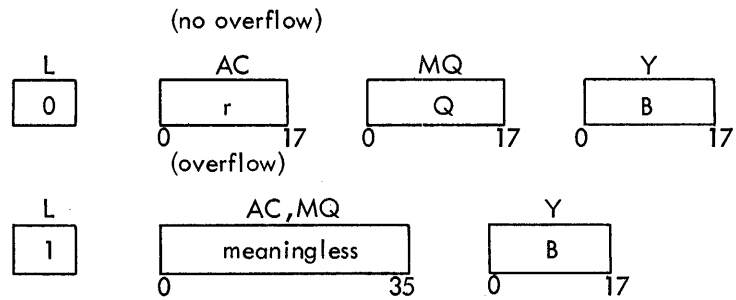
Symbolic

If $Y \leq AC$, 1 to L (divide overflow)
If $Y > AC$, 0 to SC AC/Y to MQ (quotient), AC (remainder)
0 to L
PC + 2 to PC

Pre-execution



Post execution



Instruction Sequence

Register	Contents
Y-2	LAC Dividend
Y-1	FRDIV
Y	Divisor
Y + 1	Next Instruction

FRACTION DIVIDE, SIGNED

FRACTION DIVIDE, SIGNED



15-0943

Mnemonic Name
Octal Code
Operation

FRDIVS

654323

Divide the contents of the AC and the MQ (AC contains an 18-bit signed dividend with the sign in bits AC_0 and AC_1 and the remaining 16 bits devoted to magnitude, MQ is zeroed at setup) by the contents of Memory register Y (the divisor). The binary point is assumed between AC_0 and AC_1 . The resulting quotient appears in the MQ with the algebraically determined sign in bit MQ_0 and the magnitude (1's complement) in bits $MQ_1 - 17$. The remainder is in the AC with bit AC_0 containing the original sign of the dividend and bits $AC_1 - 17$ containing the magnitude (1's complement). The address of Y is taken to be sequential to the address of the FRDIVS instruction word. The contents of Y are taken to be the absolute value of the divisor; the contents of the Link are taken to be the original sign of the divisor (FRDIVS assumes previous execution of an EAE GSM instruction, q.v.). Prior to this FRDIVS instruction, the dividend must be entered in the AC (the setup phase of FRDIVS clears the MQ and 1's complements the dividend, if negative, prior to the division). If the divisor is not greater than the dividend, divide overflow occurs (magnitude of the quotient exceeds the 18-bit capacity of the MQ) and the Link is set to one to signal the overflow condition. Data in the AC and the MQ are of no value. A valid division halts when the step counter, initialized to the 2's complement of $23_8(19_{10}$ steps), counts up to zero (the six low-order bits of the FRDIVS instruction word specify the step count). The contents of the Link are cleared to zero. The contents of Y are unchanged. The program resumes at the next instruction (Memory register $Y + 1$).

Symbolic

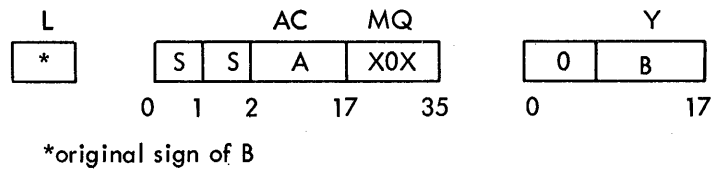
If $Y \leq AC$, 1 to L (divide overflow)

If $Y > AC$, 0 to SC AC/Y to MQ (quotient), AC (remainder)
0 to L

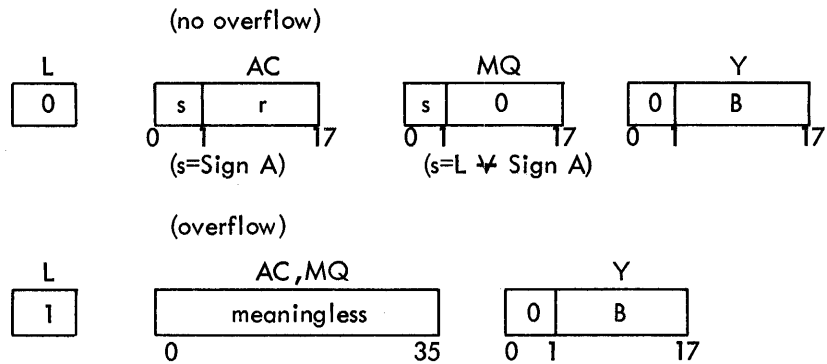
PC + 2 to PC

Data Structure
Pre-execution

$$A = BQ + r$$



Post Execution



Instruction Sequence

Register	Contents
Y-5	LAC Divisor
Y-4	GSM
Y-3	DAC Divisor (absolute value) in Y
Y-2	LAC Dividend
Y-1	FRDIVS
Y	Divisor (absolute value)
Y + 1	Next Instruction

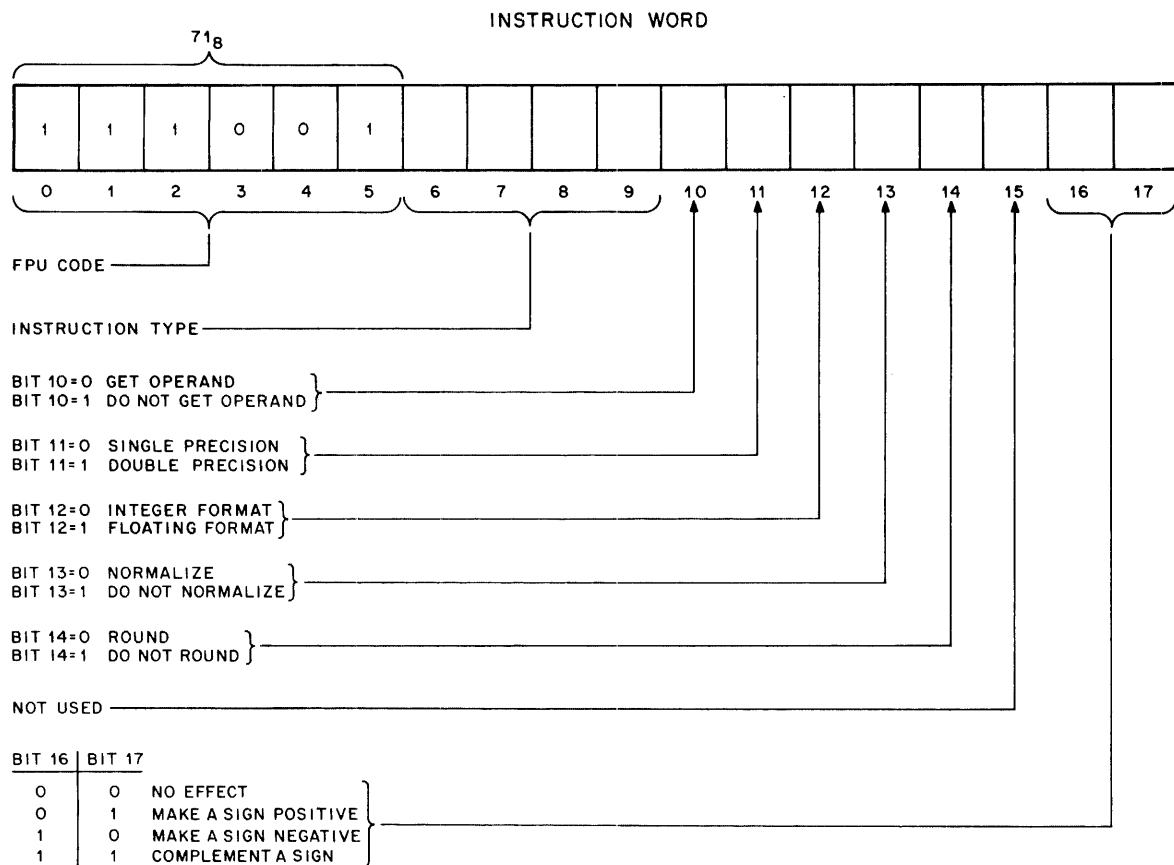
6.3 FLOATING POINT UNIT

The FP15 Floating-Point Processor (FPU) is a hardware option that enables the XVM to perform arithmetic and logic operations using floating-point arithmetic. The prime advantage is increased speed without the necessity of writing complex floating-point software routines. The FP15 has single-precision and extended-integer capability, as well as single- and double-precision floating point.

Floating-point instructions consist of two 18-bit words: an instruction word with a 71 code (Figure 6-14), followed by an address word (Figure 6-15). The instruction word specifies type of operation, type of precision, and data format. The address word specifies direct or indirect addressing and contains the address of the memory operand, if direct, or the address of a word containing the address of the memory operand, if indirect. Each instruction received from memory is monitored by both the FP15 and CPU. An instruction with an octal code of 71 in bits 00 through 05 is recognized as a floating-point instruction.

The single- and double-precision floating point and single-precision integer data formats are identical to those in the existing XVM floating-point software.

For single-precision integer words, the 18-bit 2's complement operand is loaded from memory into bits 18 through 35 of the FMA register. The value of bit 18 (sign bit) is loaded into the remaining bit positions (bits 17 through 00) to extend the sign bit (Figure 6-16).



15-0562

Figure 6-14 Floating Point Instruction Format

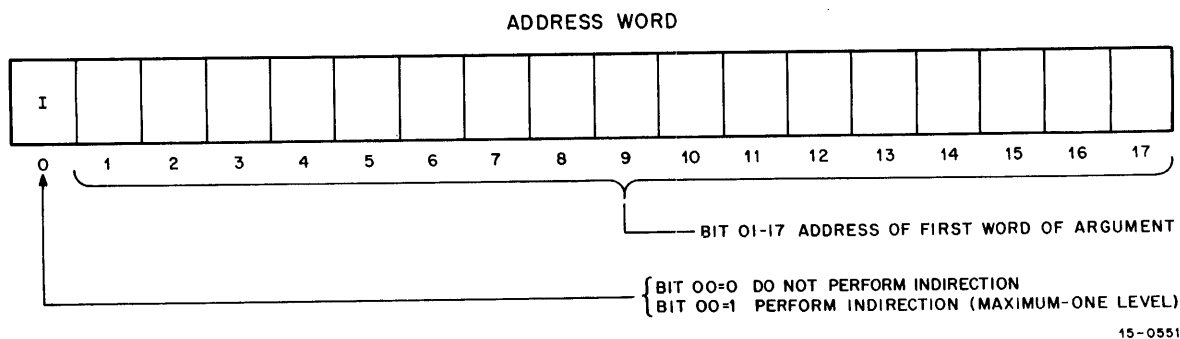


Figure 6-15 Floating Point Address Format

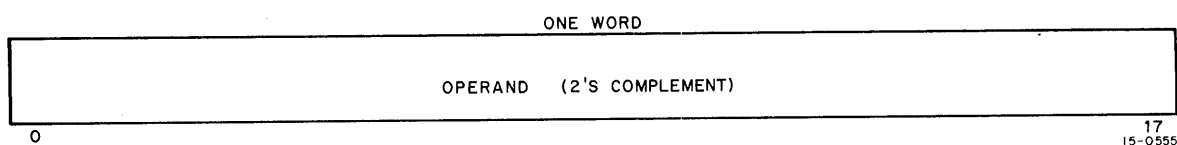


Figure 6-16 Single Precision Integer Format

For extended integer words, the high-order operand from memory is loaded into bits 00 through 17 of the FMA, and the low-order operand is loaded into bits 18 through 35.

All integers loaded into the floating-point processor are converted to 36-bit sign and magnitude numbers (Figure 6-17).

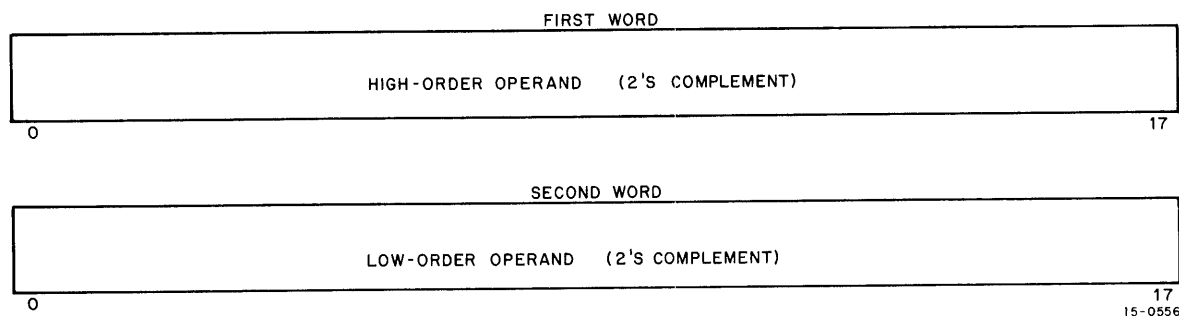


Figure 6-17 Extended Integer Format

For single-precision floating-point words, the first word from memory consists of nine bits of low-order mantissa and nine bits of exponent. The nine bits of mantissa are loaded into bits 18 through 26 of the FMA, and bits 27 through 35 are zeroed. The nine bits of exponent in 2's complement form are loaded into bits 09 through 17 of the EPA, with bit 09 representing the sign bit. Bits 00 through 08 are loaded with the value of bit 09. This extends the sign bit to bit position 00. The second word from memory is loaded into bits 00 through 17 of the FMA and represents the 18 bits of high-order mantissa (Figure 6-18).

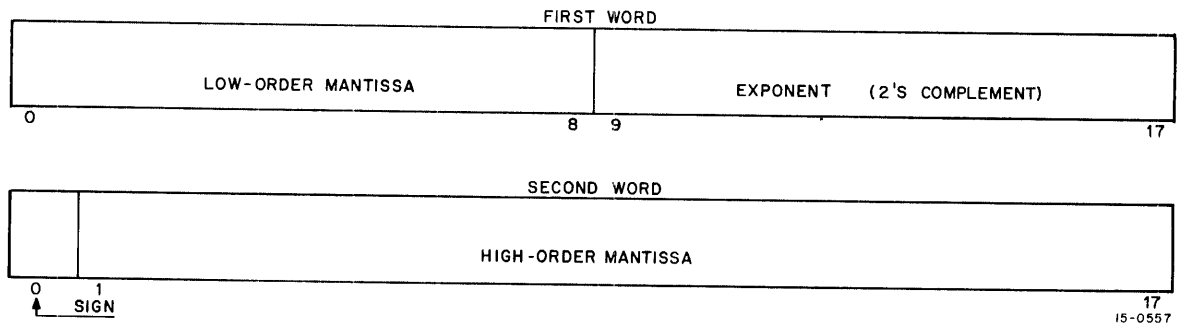


Figure 6-18 Single Precision Floating Point Format

For double-precision floating-point words, the 18-bit 2's complement exponent is first loaded into the EPA, the 18-bit high-order mantissa is loaded into A SIGN and bits 01 through 17 of the FMA, and the low-order mantissa is loaded into bits 18 through 35 of the FMA. All 36 bits of the FMA are loaded at one time (Figure 6-19).

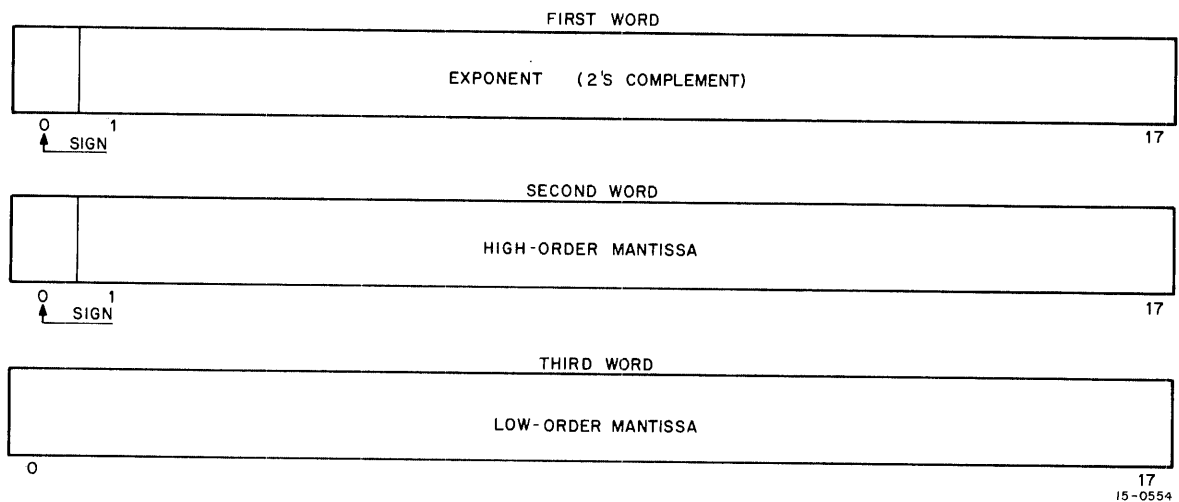


Figure 6-19 Double Precision Floating Point Format

Generally, the FP15 instructions are in the following format:

XX MODIFIER	X FORMAT	XX OPERATION

For example, if an unrounded, unnormalized, double-precision floating point Add instruction is specified, the mnemonic is specified as UUDAD; where the UU is the modifier, D is the format, and AD is the operation. Modify FMA instructions, branch instructions, and diagnostic instructions do not follow this general pattern.

All the FP15 instructions (except Floating-Point Test, Branch, Load or Store JEA, and diagnostic instructions) can be microprogrammed with bits 16 and 17 of the instruction word as described below:

Bit 16	Bit 17		
0	0	No effect	
0	1	Make A SIGN positive	Not used in FP test,
1	0	Make A SIGN negative	Load or Store JEA,
1	1	Complement A SIGN	Branch on condition, and diagnostic instructions.

For example, the instruction 710540 specifies double-precision floating-point subtraction. If desired to make A SIGN negative, the instruction would be specified as 710542.

Table 6-3
FP15 Instruction Summary

Mnemonic	Instruction Type	Octal Code
FPT	Floating-Point Test	710314
ISB	Single Integer Subtract	710400
ESB	Extended Integer Subtract	710500
FSB	Single-Precision Float Subtract	710440
URFSB	Unrounded, Single-Precision Float Subtract	710450
UNFSB	Unnormalized, Single-Precision Float Subtract	710460
UUFBS	Unrounded, Unnormalized, Single-Precision Float Subtract	710470
DSB	Double-Precision Float Subtract	710540
URDSB	Unrounded, Double-Precision, Float Subtract	710550
UNDSB	Unnormalized, Double-Precision Float Subtract	710560
UUDSB	Unrounded, Unnormalized, Double-Precision Float Subtract	710570
IRS	Single Integer Reverse Subtract	711000
ERS	Extended Integer Reverse Subtract	711100
FRS	Single-Precision Float Reverse Subtract	711040
URFRS	Unrounded, Single-Precision Float Reverse Subtract	711050
UNFRS	Unnormalized, Single-Precision Float Reverse Subtract	711060
UUFRS	Unrounded, Unnormalized, Single-Precision Float Reverse Subtract	711070
DRS	Double-Precision Float Reverse Subtract	711140
URDRS	Unrounded, Double-Precision Float Reverse Subtract	711150
UNDRS	Unnormalized, Double-Precision Float Reverse Subtract	711160
UUDRS	Unrounded, Unnormalized, Double-Precision Float Reverse Subtract	711170
IMP	Single Integer Multiply	711400
EMP	Extended Integer Multiply	711500
FMP	Single-Precision Float Multiply	711440
URFMP	Unrounded, Single-Precision Float Multiply	711450

Table 6-3 (Cont)
FP15 Instruction Summary

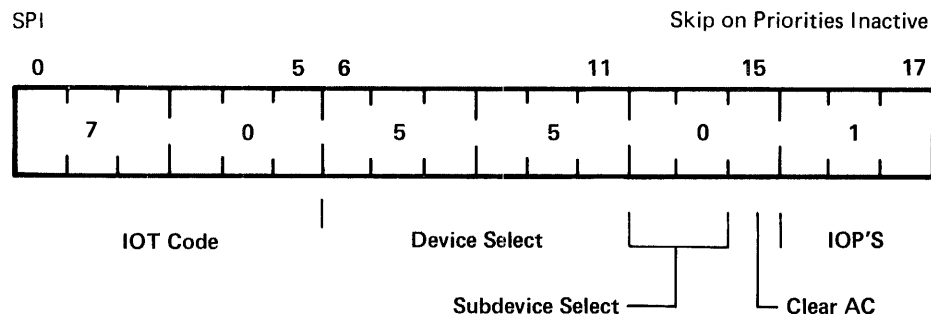
Mnemonic	Instruction Type	Octal Code
UNFMP	Unnormalized, Single-Precision Float Multiply	711460
UUFMP	Unrounded, Unnormalized, Single-Precision Float Multiply	711470
DMP	Double-Precision Float Multiply	711540
URDMP	Unrounded, Double-Precision Float Multiply	711550
UNDMP	Unnormalized, Double-Precision Float Multiply	711560
UUDMP	Unrounded, Unnormalized, Double-Precision Float Multiply	711570
IDV	Single-Precision Integer Divide	712000
EDV	Extended Integer Divide	712100
FDV	Single-Precision Float Divide	712040
URFDV	Unrounded, Single-Precision Float Divide	712050
DDV	Double-Precision Float Divide	712140
URDDV	Unrounded, Double-Precision Float Divide	712150
IRD	Single-Precision Integer Reverse Divide	712400
ERD	Extended Integer Reverse Divide	712500
FRD	Single-Precision Float Reverse Divide	712440
URFRD	Unrounded, Single-Precision Float Reverse Divide	712450
DRD	Double-Precision Float Reverse Divide	712540
URDRD	Unrounded, Double-Precision Float Reverse Divide	712550
ILD	Single-Precision Integer Load	713000
ELD	Extended Integer Load	713100
FLD	Single-Precision Float Load	713050
UNFLD	Unnormalized, Single-Precision Float Load	713070
DLD	Double-Precision Float Load	713150
UNDL D	Unnormalized, Double-Precision Float Load	713170
IST	Single-Precision Integer Store	713600
EST	Extended Integer Store	713700
FST	Single-Precision Float Store	713640
URFST	Unrounded, Single-Precision Float Store	713650
UNFST	Unnormalized, Single-Precision Float Store	713660
UUFST	Unrounded, Unnormalized, Single-Precision Float Store	713670
DST	Double-Precision Float Store	713750
UNDST	Unnormalized, Double-Precision Float Store	713770
ILF	Single-Precision Integer Load and Float	714010
UNILF	Unnormalized, Single-Precision Integer Load and Float	714030
ELF	Extended Integer Load and Float	714110
UNELF	Unnormalized, Extended Integer Load and Float	714130
FLA	Float FMA	714210
UNFLA	Unnormalized Float FMA	714230
FLX	Single-Precision Float Load and Fix	714460
URFLX	Unrounded, Single-Precision Float Load and Fix	714470

Table 6-3 (Cont)
FP15 Instruction Summary

Mnemonic	Instruction Type	Octal Code
DLX	Double-Precision Float Load and Fix	714560
URDLX	Unrounded, Double-Precision Float Load and Fix	714570
FXA	Fix EPA, FMA	714660
URFXA	Unrounded, Fix EPA, FMA	714670
ILQ	Single-Precision Integer Load FMQ	715000
ELQ	Extended Integer Load FMQ	715100
FLQ	Single-Precision Float Load FMQ	715050
UNFLQ	Unnormalized, Single-Precision Float FMQ	715070
DLQ	Double-Precision Float Load FMQ	715150
UNDLQ	Unnormalized, Double-Precision Float Load FMQ	715170
SWQ	Swap FMA and FMQ	715250
UNSWQ	Unnormalized, Swap FMA and FMQ	715270
LJE	Load JEA Register	715400
SJE	Store JEA Register	715600
IAD	Single-Precision Integer Add	716000
EAD	Extended Integer Add	716100
FAD	Single-Precision Float Add	716040
URFAD	Unrounded, Single-Precision Float Add	716050
UNFAD	Unnormalized, Single-Precision Float Add	716060
UUFAD	Unrounded, Unnormalized, Single-Precision Float Add	716070
DAD	Double-Precision Float Add	716140
URDAD	Unrounded, Double-Precision Float Add	716150
UNDAD	Unnormalized, Double-Precision Float Add	716160
UUDAD	Unrounded, Unnormalized, Double-Precision Float Add	716170
BZA	Branch on 0 FMA	716601
BMA	Branch on Minus FMA	716602
BLE	Branch if FMA ≤ 0	716603
BPA	Branch on positive FMA	716604
BRU	Branch Unconditional	716606
BNA	Branch on non-zero FMA	716610
BAC	Branch if GUARD bit is Set	716620
FZR	Zero EPA (A SIGN) FMA	711200
FAB	Make A SIGN positive (Absolute Value)	713271
FNG	Make A SIGN negative	713272
FCM	Complement A SIGN	713273
FNM	Normalize EPA (A SIGN) FMA	713250
DMF	Diagnostic Mode Off	717200
DMN	Diagnostic Mode On	717300
DRR	Diagnostic Read Registers	710000
DSR	Diagnostic Step and Read Registers	710100 + n
DBK	Debreak	703304

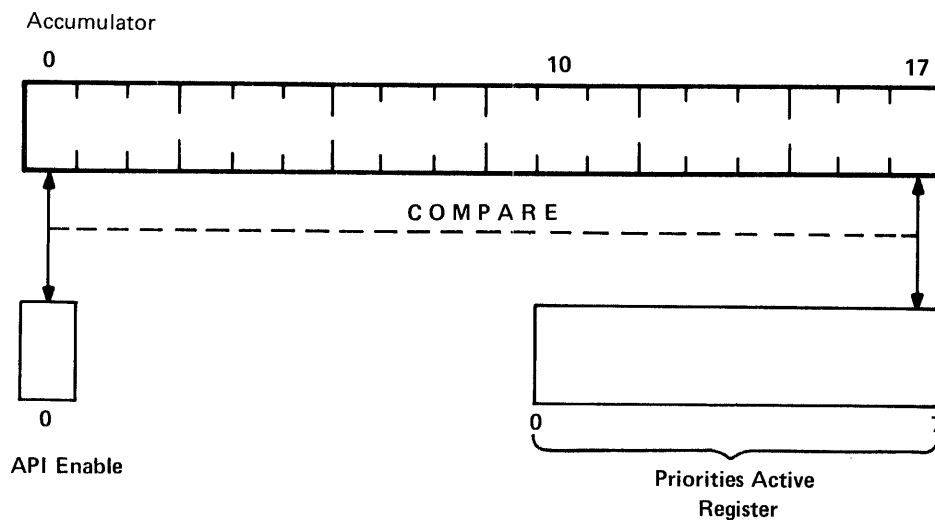
A complete description of the FP15 Floating-Point Processor instruction set is provided in the *FP15 Floating-Point Processor Reference Manual*, DEC-15-HQEA-D.

6.4 AUTOMATIC PRIORITY INTERRUPT INSTRUCTION SET



15-0954

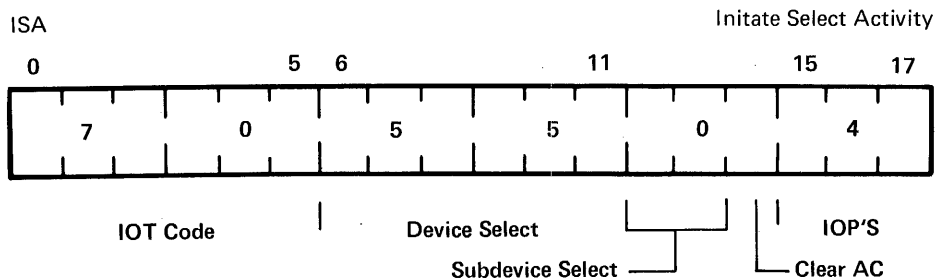
This instruction compares a condition code in the Accumulator with part of the ENABLE bit and Priorities Active register. If any bit of the condition code matches the corresponding bit of the ENABLE or Priority Active register and both are set, the next instruction is skipped. Otherwise the next instruction is executed. The corresponding bits are shown in Figure 6-20.



15-0955

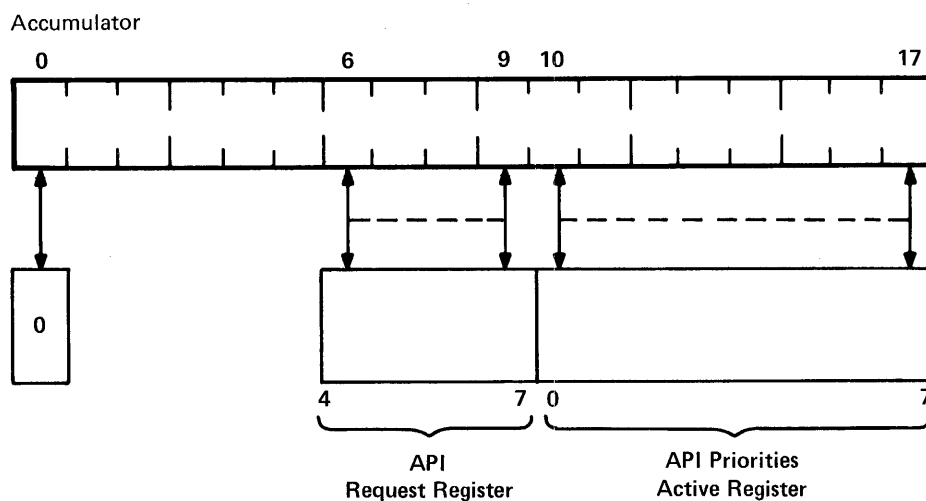
Figure 6-20 Skip on Priorities Inactive

INITIATE SELECT ACTIVITY



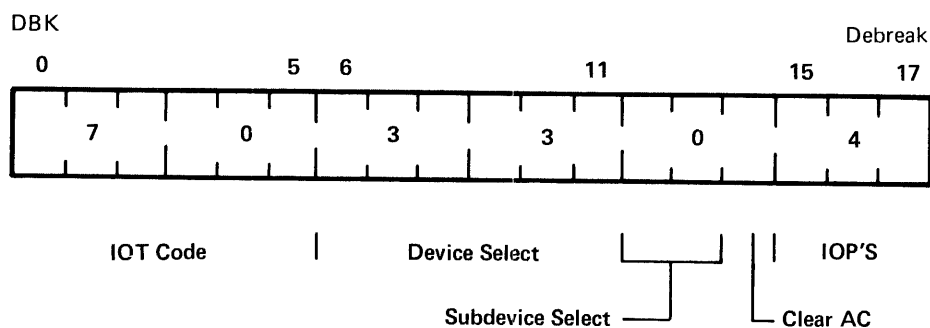
15-0956

The content of Accumulator bit 0 is placed into the ENABLE flip-flop; Accumulator bits 6 through 9 are ORed into bits 4 to 7 of the API request register, and Accumulator bits 10 through 17 are ORed into bits 0 through 7 of the API Priorities Active register.



15-0957

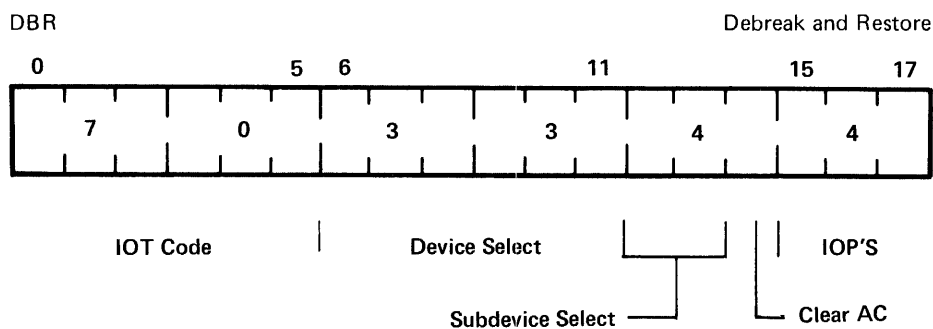
DEBREAK



15-0958

This instruction is used to release the highest active priority level. Its use is to return a subroutine's priority to the normal assignment after the requirement for an interim ISA-initiated raising of priority has been satisfied. DBK should not be used to terminate a subroutine as it does not provide for restoration of the PC, Link, etc.

DEBREAK AND RESTORE



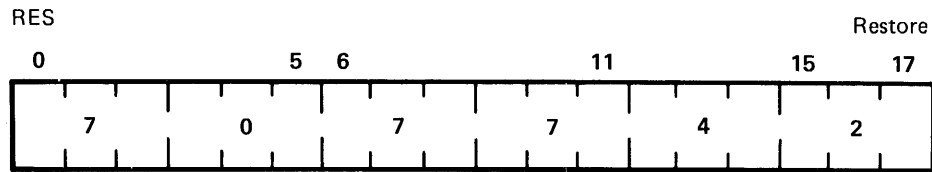
15-0959

This instruction zeroes the highest priority presently in the Priority Active register, thus clearing the way for future requests. It also primes the PDP-15 to restore the Link, the program counter, and User mode to their status at the time the API request was honored. The actual restoration occurs at the execution of any indirect instruction. However, a JMP indirect is usually used exiting the subroutine which must immediately follow the DBR instruction.

Programming Note

Normally, the SPI and ISA instructions are used sequentially to test first that the program segment currently in progress is not already at the requested priority level, and then if not, to initiate a raising of priority to the requested level. Hence, if a program segment cannot raise its priority, the segment must already be at the requested level or higher. The ISA instruction cannot be used to lower the priority level of an active program segment. The hardware will not recognize the priority change.

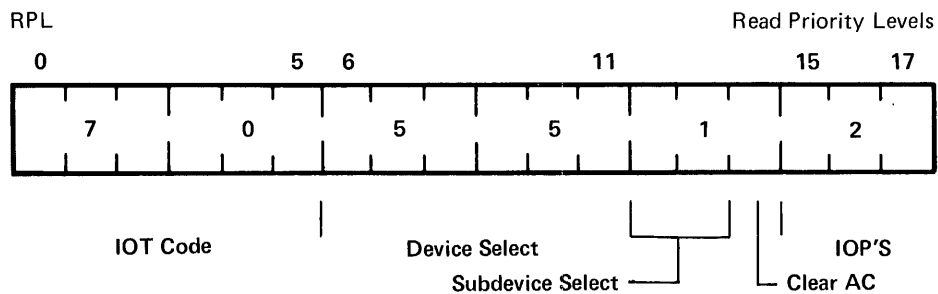
RESTORE



15-0960

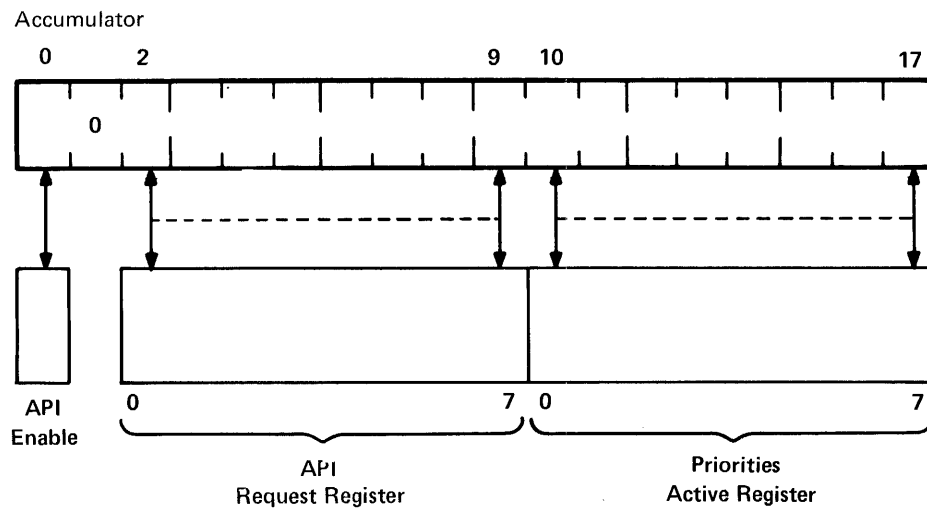
Restore the status of the Link, Bank mode, and User mode, at the first indirect instruction after it is executed. The RES does not, however, affect the API priority levels.

READ PRIORITY LEVELS



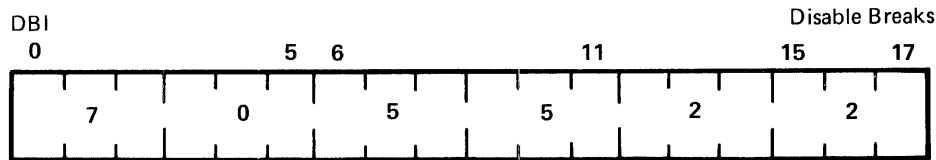
15-0961

The contents of the API ENABLE flip-flop is read into Accumulator bit 0, the content of the API Request register is read into Accumulator bits 2 through 9, and the content of the Priorities Active register is read into Accumulator bits 10 through 17, as shown in the following illustration.



15-0962

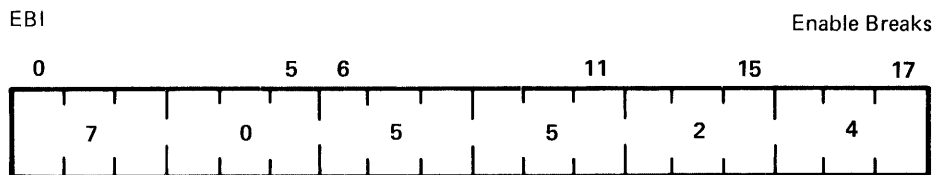
DISABLE BREAKS



15-0963

Inhibits API and PI. Incorporated to make re-entrant programming more convenient. When in Monitor mode, one free instruction will be granted after CAL, JMS, PI; two free instructions after NORM. "Free instructions" means executable instructions that are performed before the computer goes into the Interrupt mode. See example program.

ENABLE BREAKS



15-0964

Enable API or PI. See example program.

Example:

Each of the sequences listed is expected to be uninterruptable (except for data breaks).

	JMS A or JMS* (A)	/INTERRUPT FLAG OCCURS
A	0	
	LAC A	/INTERRUPT IS SERVICED
	JMS B or JMS* (B)	
B	0	
	DBI	
	LAC X	/INTERRUPT FLAG OCCURS
	DAC XX	
	LAC Y	
	EBI	
	DAC YY	/INTERRUPT WILL BE SERVICED

6.5 KW15 REAL-TIME CLOCK

The real-time clock, when enabled, counts in memory location 00007 the number of cycles completed by any one of three inputs:

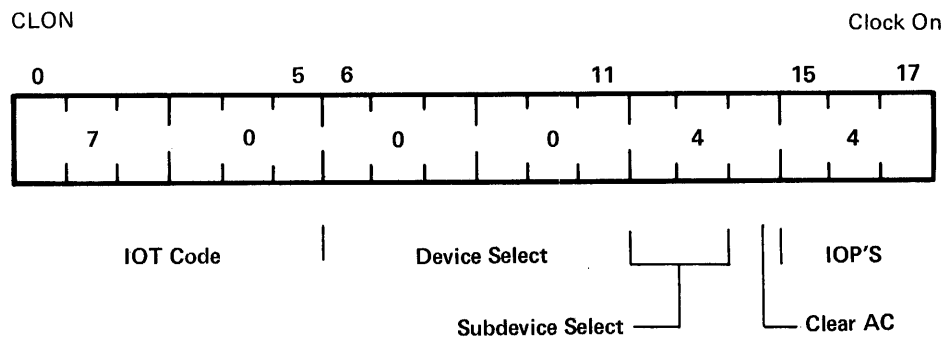
1. The line voltage (50 or 60 Hz).
2. An M401 R-C Clock (offered as standard) which can be set to any frequency from 0 to 10 kHz.
3. A user-supplied TTL compatible signal that is fed to a point on the XVM logic.

When location 00007 overflows, an interval program interrupt or API request, if available, is generated informing the monitor that its preset interval is over. The monitor must either disable the clock or reinitialize location 00007 to the 2's complement of the number of counts it needs to tally.

The incrementing of location 00007 during a real-time clock request occurs via the I/O Processor, using its increment-memory facility. A real-time clock request takes priority over API, PI and IOT requests.

The following IOT instructions are provided for use with the clock:

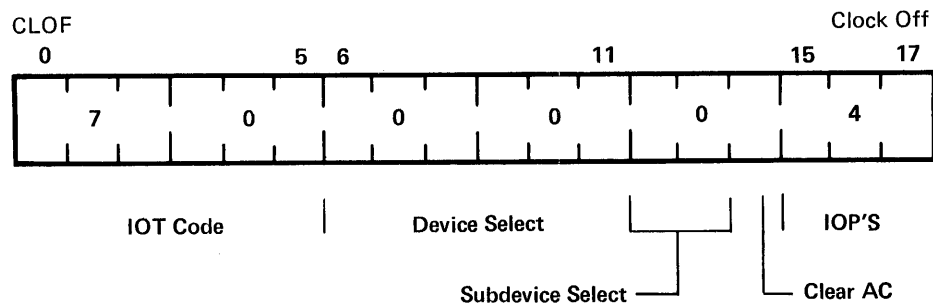
CLOCK ON



15-0965

The real-time clock is enabled to begin incrementing location 00007 and its flag is cleared.

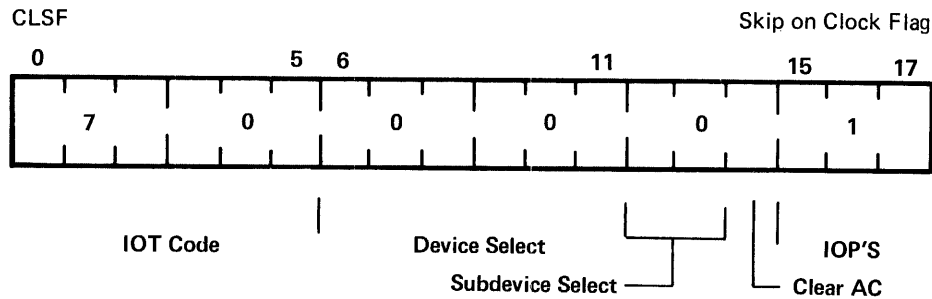
CLOCK OFF



15-0966

The real-time clock is disabled, preventing it from incrementing location 00007.

SKIP ON CLOCK FLAG



15-0967

The program counter is incremented and the next instruction skipped if the clock flag is set.

While the facility is enabled, requests for clock breaks have priority of acceptance over API and PI requests. The first clock break may occur at any time up to 17 ms after the facility has been enabled. The clock switch on the console can inhibit the clock from incrementing location 7.

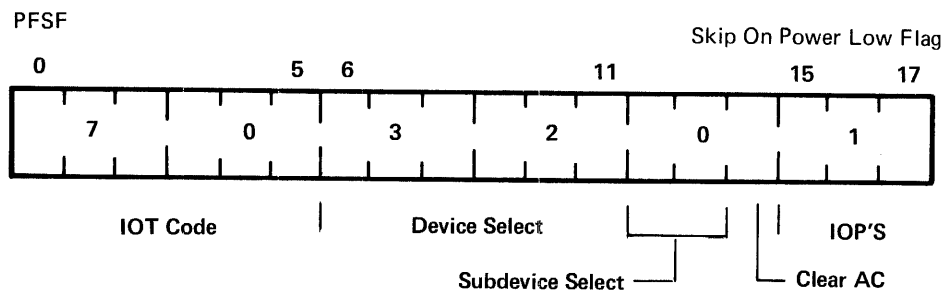
6.6 KF15 POWER FAIL

The XVM contains circuitry which provides optimum protection of programs during machine turn-on or turn-off, whether accidental or intended. The Power fail detection feature of the I/O Processor allows time to store active registers before the system stops during a power failure, a system restart, and the subsequent restoration of these registers when system power is reapplied.

The basic XVM is not affected by power interruptions of less than 10 ms duration. Active registers in the processor (AC, AR, PC, etc.) will lose their contents when interruptions of longer duration occur, but memory will not be disturbed. The power failure detection feature provides for saving the contents of active registers in the event of longer power interrupt and for automatic restart of the system when power is restored. The restart feature is switch-selected by the operator to be enabled or disabled. When enabled, the program in progress resumes execution at location 000000. The system must be operating with the program interrupt facility (or the API) enabled to sense the option's initiation of a program interrupt to save the register contents at the time of the line power failure. If API is enabled, power fail interrupts on its highest level and traps to memory address 52.

There is only one instruction associated with power fail. That is:

SKIP ON POWER LOW FLAG



15-0968

The state of the power low flag is tested, and if set, indicates that system line voltage has dropped and that this flag has posted an interrupt; then the reset instruction is skipped. The flag is cleared by the power clear signal when the power interruption is over.

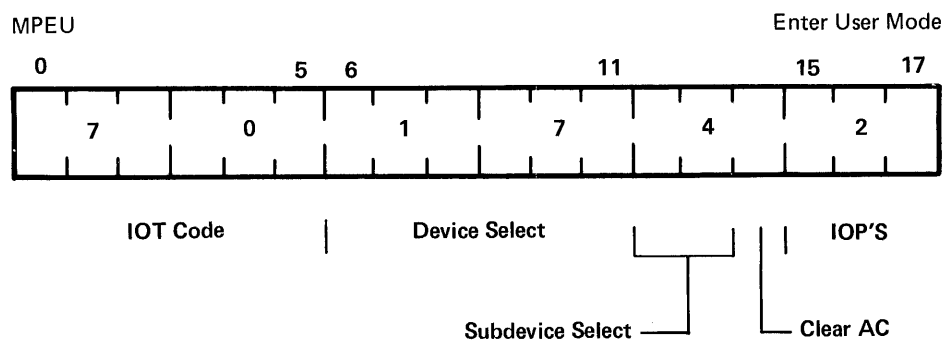
6.7 MEMORY MANAGEMENT

User mode may be enabled either by programmed instruction or by pressing the PROT switch on the console and pressing the START key. When enabled, the USER indicator lights.

The sole operator control is the PROT switch, which has an indicator above it. This indicator lights when in User mode. The PROT switch is used with the START key to establish the proper mode at the beginning of program execution. If the switch is up, then the program is started in User mode. The switch has no further effect.

The RESET key clears the violation and non-existent memory flags, and User mode (i.e., memory protect is turned off).

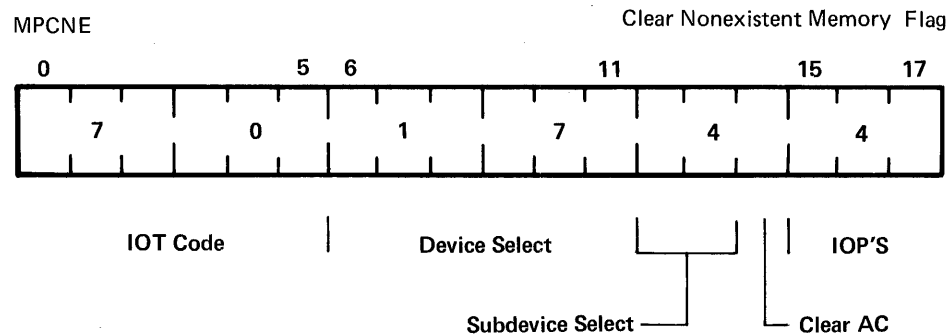
ENTER USER MODE



15-0969

User mode will be entered during the fetch cycle of the instruction following MPEU.

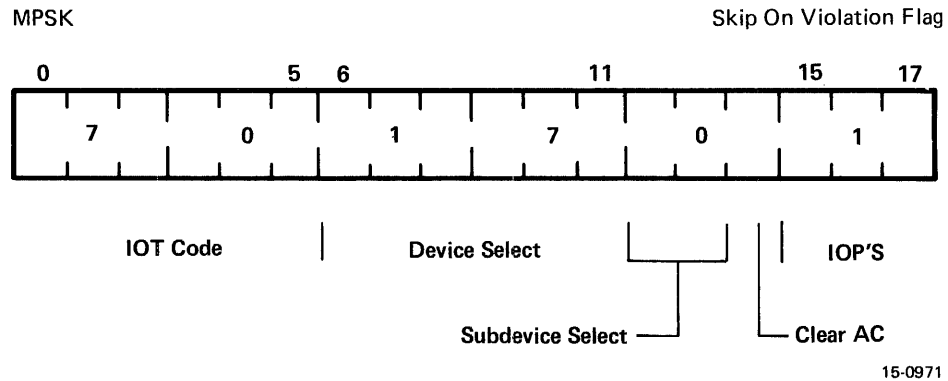
CLEAR NON-EXISTENT MEMORY



15-0970

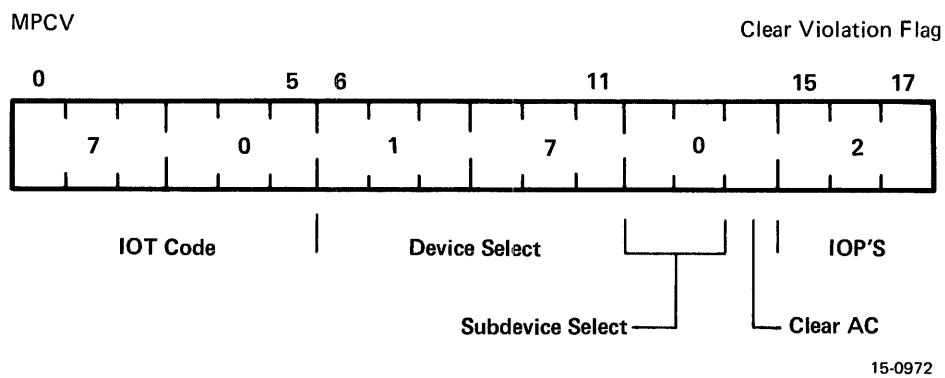
The nonexistent memory flag posted when nonexistent memory has been referenced, is cleared by the IOT.

SKIP ON VIOLATION FLAG



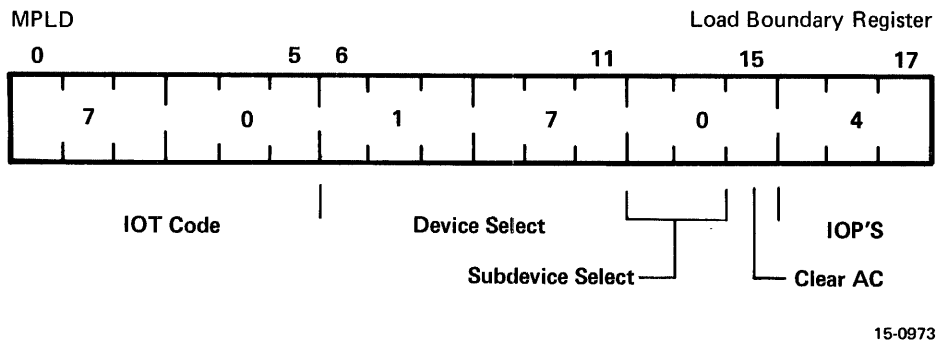
The Memory Protect Violation flag will be set whenever the execution of an instruction has violated the provision of memory protection (see above).

CLEAR VIOLATION FLAG



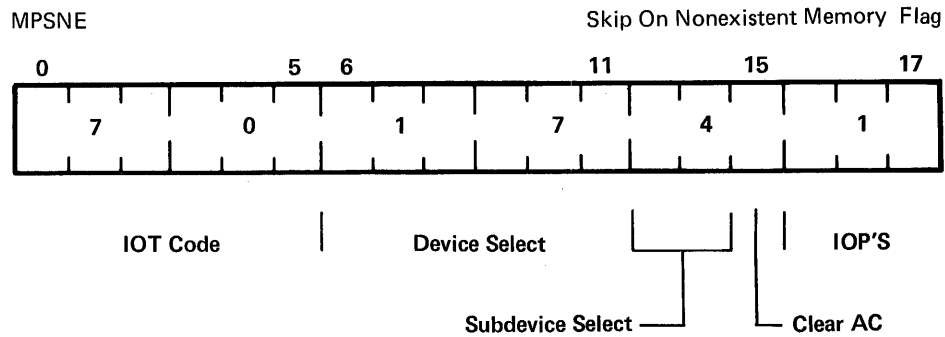
The Violation flag, set if the boundary has been violated or an illegal instruction attempted, is cleared by this IOT.

LOAD BOUNDARY REGISTER



Load the Memory Protection register with the contents of AC 1 through 9.

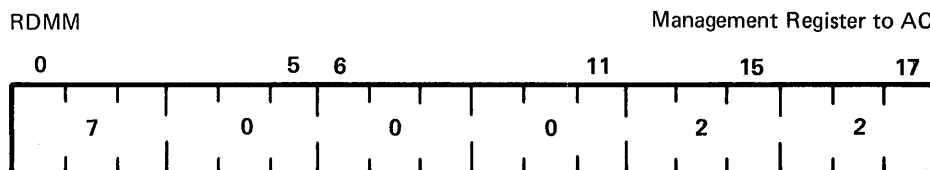
SKIP ON NON-EXISTENT MEMORY



15-0974

The Nonexistent Memory flag is set whenever the processor attempts to reference a nonexistent area of core.

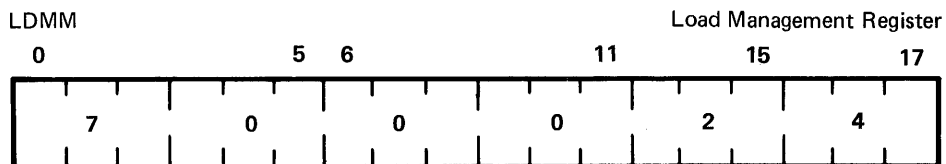
OR MANAGEMENT REGISTER TO AC



15-0976

This instruction will OR the contents of the Management register (00-17) into the AC.

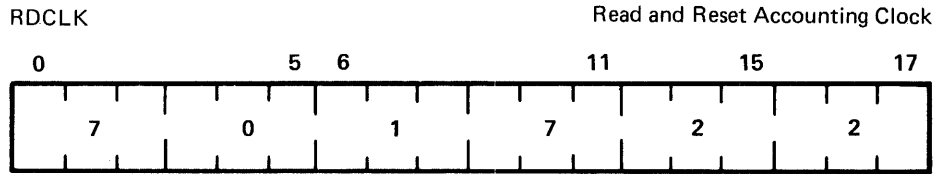
LOAD MANAGEMENT REGISTER



15-0977

This instruction will load the Memory Management register with the contents of the AC. The AC remains unchanged. Note that to clear the Memory Management register, the IOT 700034 should be used.

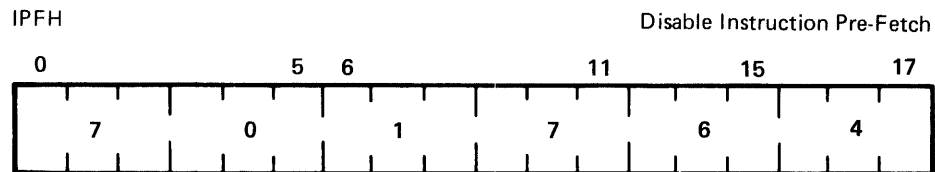
READ AND RESET ACCOUNTING CLOCK



15-0978

In the XVM Memory Processor there is a Task Accounting Clock. It is 18 bits in length and is incremented every 10 μ s. The counting is inhibited whenever an API level of 0-3 or a PI break is in progress.

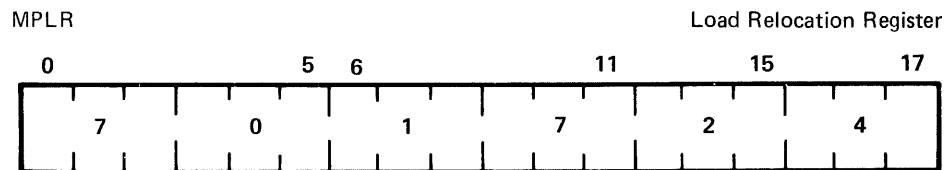
CONTROL INSTRUCTION PRE-FETCH



15-0979

When this instruction is executed with AC 17=1 the ABORT CLR flip-flop is set. This in turn prevents the IPF logic from synchronizing with a request from the XVM CPU. Normally, this is used in maintenance only. The ABORT CIR flip-flop may be reset (to enable the IPF) by a CAF instruction or the above instruction with AC17=0.

LOAD RELOCATION REGISTER



15-0975

Load the Relocation register with the contents of AC 00 through 09. The Relocation register will be set to the first address to which the user is to be relocated.

6.8 PERIPHERAL INSTRUCTION SET

Input/Output Transfer Instructions (IOTs)

Table 6-4 lists the IOTs for XVM peripheral devices.

Table 6-4
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
Program Interrupt		
IOF	700002	Interrupt off.
ION	700042	Interrupt on.
KW15 Real-Time Clock		
CLSF	700001	Skip the next instruction if the CLOCK flag is set to 1.
CLOF	700004	Clear the CLOCK flag and disable the clock.
CLON	700044	Clear the CLOCK flag and enable the clock.
PC15 High Speed Paper Tape Reader		
RSF	700101	Skip, if READER flag is a 1.
RCF	700102	Clear READER flag, then inclusively OR the contents of the reader buffer into the AC.
RRB	700112	Read reader buffer. Clear READER flag and AC, and then transfer content of the reader buffer into AC.
RSA	700104	Select reader in Alphanumeric mode. One 8-bit character is read into the reader buffer.
RSB	700144	Select reader in binary mode. Three 6-bit characters are read into the reader buffer.
PC15 High Speed Paper Tape Punch		
PSF	700201	Skip, if the PUNCH flag is set to 1.
PCF	700202	Clear the PUNCH flag.
PSA or PLS	700204 700206	Punch a line of tape in Alphanumeric mode.
PSB	700244	Punch a line of tape in Binary mode.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
I/O Equipment		
IORS	700314	Input/output read status. The content of given flags replaces the content of the assigned AC bits.
CAF	703302	Clear all flags.
SPCO	703341	Skip, if a PC15 is connected to the system.
SK15	707741	Skip, if processor is a PDP-15 or XVM.
SBA	707761	Skip, if processor is in Bank mode.
DBA	707762	Disable Bank Addressing (enter Page mode).
EBA	707764	Enable Bank Addressing
Console Device Keyboard		
KSF	700301	Skip, if the KEYBOARD flag is set to 1.
KRB	700312	Read the keyboard buffer. The content of the buffer is placed in AC10-17 and the KEYBOARD flag is cleared (half-duplex operation).
KRS	700332	Read keyboard buffer and select keyboard reader (full-duplex operation).
Console Device Printer		
TSF	700401	Skip, if the PRINTER flag is set.
TCF	700402	Clear the PRINTER flag.
TLS	700406	Load printer buffer. The content of AC00-17 is placed in the buffer and printed. The flag is cleared before transmission takes place and is set when the character has been printed.
VP15-A Storage Tube Display		
CXB	700502	Clear X-coordinate buffer.
CYB	700602	Clear Y-coordinate buffer.
LXB	700504	Load X-coordinate buffer from AC8-17.
LYB	700604	Load Y-coordinate buffer from AC8-17.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
VP15-A Storage Tube Display (Cont)		
EST	700724	Erase storage tube.
SDDF	700521	Skip on DISPLAY DONE flag.
CDDF	700722	Clear DISPLAY DONE flag.
LXBD	700564	Load X-coordinate buffer and display the point specified by XB and YB (Store mode).
LYBD	700664	Load Y-coordinate buffer and display the point specified by XB and YB (Store mode).
LXDNS	700544	Load the X-coordinate buffer and display the point specified by XB and YB (Nonstore mode).
LYDNS	700644	Load the Y-coordinate buffer and display the point specified by XB and YB (Nonstore mode).
VP15-B (RM503), BL (RM503 and Light Pen), C (VR12) and CL (VR12 and Light Pen)		
DXL	700504	Load the X-coordinate buffer from AC8-17.
DXS	700544	Load the X-coordinate buffer and display the point specified by the XB and YB.
DYL	700604	Load the Y-coordinate buffer from AC8A-17.
DYS	700644	Load the Y-coordinate buffer and display the point specified by the XB and YB.
DXC	700502	Clear the X-coordinate buffer.
DYC	700602	Clear the Y-coordinate buffer.
DLB	7000704	Load the Brightness register from bits 16-17 of the AC. This instruction clears the DISPLAY flag associated with the light pen.
DSF	700501	Skip, if DISPLAY (light pen) flag is a 1.
DCF	700702	Clear DISPLAY (light pen) flag.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
VP15-M Storage Tube Display Multiplexer		
LUDU	700764	Load Unit Designation register from AC10-17.
NP15 List-Mode P.H.A. Control		
SOWC	701101	Skip on Word Count overflow.
CLWO	701102	Clear WORD COUNT OVERFLOW flag.
SETM	701104	Set Mode register from AC13-17.
SOAL	701121	Skip on A live-time overflow.
CALO	701122	Clear A live-time overflow.
CBLO	701124	Clear B live-time overflow.
SOBL	701141	Skip on B live-time overflow.
Memory Management		
MPSK	701701	Skip on PROTECT VIOLATION flag.
MPCV	701702	Clear PROTECT VIOLATION flag.
MPLD	701704	Load Boundary register AC00-09.
MPRC	701722	Read accounting clock to AC.
MPLR	701724	Load Relocation register.
MPSNE	701741	Skip on nonexistent MEMORY flag.
MPEU	701742	Enter User mode.
MPCNE	701744	Clear nonexistent MEMORY flag.
RDMM	700022	OR Memory Management register to AC0-17.
LDMM	700024	Load Memory Management register from AC0-17.
RDCLK	701762	OR the Task Clock to AC0-17.
IPFH	701764	Inhibit IPF (Set Abort Clear).

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
VT15 Graphic Processor		
RS1	703002	Read status 1.
RS2	703022	Read status 2.
RS3	703142	Read status 3.
RYP	703042	Read Y register.
RPC	703062	Read program counter.
RXP	703102	Read X register.
SPSF	703001	Skip on STOP flag.
SPLP	703021	Skip on LIGHT PEN flag.
SPPB	703041	Skip on PUSHBUTTON flag.
SPEF	703061	Skip on EDGE flag.
SPDF	703101	Skip on any flag.
SPDI	703121	Skip on any interrupting flag.
SSLP	703141	Skip on SLAVE LIGHT PEN flag (Multiplexer with more than one VT04-370).
SPES	703161	Skip on external stop (Check STPD accomplished).
LSD	703004	Load and start display (Initializes VT15).
SIC	7030241	Set initial conditions.
STPD	703044	External stop display (XVM stops display).
RES	703064	Resume display after flag.
KF15 Power Fail Feature		
SPFAL	703201	Skip, if POWER-LOW flag is set.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
VW01 Writing Tablet Control		
WTCP	703221	Clear Pen Data flag.
WTRX	703222	Read X-coordinate.
WTSC	703224	Set tablet controls.
WTCD	703241	Clear Data Ready flag.
WTRY	703242	Read Y-coordinate.
WTMN	703244	Clear Set XY.
WTSK	703261	Skip on writing tablet flag.
WTRS	703262	Read tablet status.
WTSE	703264	Select tablet.
KA15 Automatic Priority Interrupt Feature		
DBK	703034	Debreak.
DBR	703344	Debreak and restore.
SPI	705501	Skip on priorities inactive.
RPL	705512	Read API status.
ISA	705504	Initiate selected activity.
ENB	705521	Enable breaks.
INH	705522	Disable breaks.
RES	707742	Restore.
RP15 Disk Pack Control		
DPSF	706301	Skip on DISK flag.
DPOSA	706302	OR the Status register A into AC.
DPRSA	706312	Read the Status register A into AC.
DPOU	706402	OR the Unit Cylinder Address register into the AC.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
RP15 Disk Pack Control (Cont)		
DPRU	706412	Read the Unit Cylinder Address register into the AC.
DPSA	706321	Skip on Attention flag.
DPOSB	706322	OR Status register B into the AC.
DPRSB	706332	Read Status register B into the AC.
DPLZ	706424	Load the accumulator zeros into Status register A bits 0 through 7 and execute.
DPLO	706444	Load the accumulator ones into Status register A bits 0 through 7 and execute.
DPCN	706454	Execute the Function register.
DPLF	706464	Load the Status register A and execute.
DPLA	706304	Load the cylinder, head, and Sector Address registers from the accumulator.
DPCA	706344	Load the Current Address register.
DPWC	706364	Load the Word Count register.
DPOA	706422	OR the cylinder, head, and Sector Address registers into the AC. AC bits 13 through 17 are ORed with the sector.
DPRA	706432	Read the cylinder, head, and Sector Address register into the AC.
DPOC	706442	OR the Current Address register into the AC.
DPRC	706452	Read the Current Address register into the AC.
DPOW	706462	OR the Word Count register into the AC.
DPRW	706472	Read the Word Count register into the AC.
DPCS	706324	Clear status.
DPCF	706404	Clear Function register.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
RP15 Maintenance IOTs		
DPSJ	706341	Skip, if the JOB DONE flag is set.
DPSE	706361	Skip, if an error condition is present.
DPOM	706342	OR the six-bit Maintenance register into AC.
DPRM	706352	Read the six-bit Maintenance register into AC.
DPEM	706401	Execute maintenance instruction.
DPLM	706411	Leave Maintenance mode. The AC is left cleared.
LP15 Line Printer Controls		
LPSF	706501	Causes a skip request, if done or error is set.
LPPM	706521	Initializes the control, sets header; sets multiline.
LPP1	706541	Initializes the control, sets header; does not set multiline.
LPRS	706542	Read status.
LPEI	706544	Sets the ENABLE INTERRUPT flip-flop.
LPDI	706561	Clears the ENABLE INTERRUPT flip-flop.
LPCD	706621	Clears DONE flag.
LPCF	706641	Clears STATUS and ERROR flag.
Line Printer Maintenance IOTs		
MRVFU	706502	Read VFU register.
MCVFU	706504	Clear VFU register.
MSM	706524	Set maintenance control.
MRDB1	706562	Read data buffer 00-17.
MCDB	706564	Clear data buffer.
MCM	706601	Clear maintenance control.
MRDB2	706602	Read data buffer 18-35.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
Line Printer Maintenance IOTs (Cont)		
MLDB1	706604	Load data buffer 0-17 from AC.
MRM1	706622	Read maintenance word 1.
MLDB2	706624	Load data buffer 18-35 from AC.
MRM2	706642	Read maintenance word 2.
MLS	706644	Load status.
CR15 Card Reader		
CRSKP	706701	Skip on ready or trouble conditions.
CRLD	706702	OR data buffer to AC6-17.
CRCON	706704	Load initial conditions from AC13-17.
CRLS	706722	OR status to AC4-17.
CRPC	706724	Clear status except End of Card.
RF15 DECdisk Control		
DSSF	707001	Skip on DISK flag.
DRBR	707002	OR the contents of the Buffer register with the AC.
DLBR	707004	Load the contents of the AC into the Buffer register.
DSCC	707021	Clear the disk control and disable the "freeze" status of the control.
DRAL	707022	OR the contents of the address pointer 0 (AP0) into the AC. Bits 0 through 6 contain the track address, and bits 7 through 17 contain the word address of the next word to be transferred.
DRAH	707062	OR the contents of the disk number (AP1) into the AC. Bits 15, 16, and 17 contain the disk number. Bit 14 is read back if a data transfer exceeded the capacity of the disk control. (Causes a NED error status.)
DLAL	707024	Load the contents of the AC into the AP0.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
Line Printer Maintenance IOTs (Cont)		
DLAH	707064	Load the contents of the AC (15, 16, 17) into the disk number (API).
DSCF	707041	Clear the Function register, interrupt mode.
DSFX	707042	XOR the contents of AC bits 15-17 into the Function register (FR).
DSCN	707044	Execute the condition held in the FR.
DLOK	707202	OR the contents of the 11-bit disk segment address (ADS) into the AC.
DGHS	707204	Generate simulated head signals.
DGSS	707224	Generate simulated disk signals.
DSCD	707242	Clear the Status register and DISK flag.
DSRS	707262	OR the contents of the Disk Status register with the AC.
Type TC59 Magnetic Tape Control IOT Instructions		
MTTR	707301	Skip on tape transport ready (TTR).
MTCR	707321	Skip on tape control ready (TCR).
MTSF	707341	Skip on ERROR flag or MAGNETIC TAPE flag (EF and MTF).
MTAF	707322	Clear Status and Command registers and EF and MTF in TCR.
LCM	707324	Inclusively OR content of AC0-11 into Command register.
MTLC	707326	Load content of AC0-11 into Command register.
MTCC	707356	Terminate write continuous mode.
	707342	Inclusively OR content of Status register into AC0-11.
MTRS	707352	Read content of Status register into AC0-11.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
Type TC59 Magnetic Tape Control IOT Instructions (Cont)		
MTRC	707312	Read Command register into AC0-11.
MTGO	707304	Set "go" bit to execute command in Command register.
TC15 DECtape Control		
DTCA	707541	Clear Status register A.
DTRA	707552	Read Status register A.
DTXA	707544	XOR Status register A.
DTLA	707545	Load Status register A.
DTEF	707561	Skip on ERROR flag.
DTRB	707572	Read status B.
DTDF	707601	Skip on DECtape flag.
AD15 Analog Subsystem		
ADCV	701304	Load Status register from accumulator, clear A/D done flag, and initiate conversion.
ADRB	701302	Read data buffer into accumulator and clear A/D done flag.
ADRS	701342	Read Status register into accumulator.
ADCF	701362	Clear all AD15 flags.
ADSF	701301	Skip on A/D flag.
WCSF	701341	Skip on word count overflow flag.
MSSF	701321	Skip on memory overflow flag.
UDC-15 Universal Digital Control		
UMOD	701001	Set UDC mode.
USINT*	702004	Interrupt Select.
ULA*	702024	Load address.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
UDC-15 Universal Digital Control (Cont)		
URA*	702012	Read deferred address.
URD*	702032	Read data in.
USCAN*	702021	Start interrupt scan.
USNB*	702041	Skip if not busy.
URCG	701072	Clear AC, read COS gates.
ULD	701064	Load data out.
ULPS	701044	Load previous status.
USI	701041	Skip on immediate flag.
USD	701061	Skip on deferred flag.
URAA	701052	Read immediate address.
AFC-15 Automatic Flying Capacitor		
FCMOD	701021	Set AFC mode.
FCEI*	702004	Enable AFC interrupt.
FCDI*	702001	Disable AFC interrupt.
FCLAG*	702024	Load address.
FCRB*	702032	Read A/D buffer.
FCSD*	702041	Skip on A/D done flag.
FCRA*	702012	Read AFC Address register.
BD-15 Maintenance		
MCLK	702044	Maintenance clock.
MSM	701004	Set Maintenance mode.
MCM	701022	Clear Maintenance mode.

*The UMOD IOT must be issued before these IOTs will be decoded as UDC-15 IOT instructions.

*The FCMOD IOT must be issued before these IOTs will be decoded as AFC-15 IOT instructions.

Table 6-4 (Cont)
Input/Output Transfer Instructions

Mnemonic Symbol	Octal Code	Operation Executed
BD-15 Maintenance (Cont)		
MLS	701024	Load Status register.
MRS	701012	Read Status register.
FCCV	702021	A/D convert.

Standard API Channel/Priority Assignments

Table 6-5 lists the channel number, priority level, and the address of options used on the XVM.

Table 6-5
Standard API Channel/Priority Assignments

Channel	Device	Option Number	Priority	Address
0	Software Priority	—	4	40
1	Software Priority	—	5	41
2	Software Priority	—	6	42
3	Software Priority	—	7	43
4	DECTape	TC15	1	44
5	Magtape	TC59	1	45
6	Graphics	VT15B	2	46
7	Not assigned		1	47
8	Paper Tape Reader	PC15	2	50
9	Clock Overflow	KW15	3	51
10	Power Fail	KF15	0	52
11	Not assigned			
12	Display	VT15A/VP15	2	54
13	Card Reader	CR15	2	55
14	Line Printer	LP15	2	56
15	A/D	AD15/ADF15	0	57
16	DB99A/DB98A	DB09A	3	60
17	Not assigned			
18	Dataphone	DP09A	2	62
19	Disk	RF15	1	63
20	Disk	RP15	1	64
21	Plotter	XY15	2	65
24	Terminal Control	DC01-ED No. 1	3	70
25	Terminal Control	DC01-ED No. 2	3	71
26	Terminal Control	DC01-ED No. 3	3	72
27	Writing Tablet	VW01-B	3	73
28	Terminal Keyboard	LT19/LT15A	3	74
29	Terminal Printer	LT19/LT15A	3	75
30	Terminal Control	DC01-ED No. 7	3	76
31	Dataphone	DP09*	2	77

*Channel allocated for systems with more than one of the above options.

IOT Device Selection Codes

Table 6-6 lists the IOT selection codes for devices used with the XVM.

Table 6-6
IOT Device Selection Codes

00 1 RT Clock 2 Prog Interrupt 4 RT Clock	10 AFC-15 UDC-15 BD-15	20 AFC-15 UDC-15 BD-15	30 VT15-A	40 LT19 Line 1,2,3,4 Printer or LT15A	50	60	70 RF15
01 PC15	11 NP02	21	31 VT15-A	41 Line 1,2,3,4 Keyboard or LT15A	51 AA15	61	71
02 PC15	12 NH14CR	22 DB09A	32 KF15 VW01	42 Line 5,6,7,8 Printer	52 CA15	62	72 RF15
03 1 Keyboard 2 Keyboard 4 IORS	13 AD15 ADF15	23	33 1 33 KSR Skip 2 Clear All Flags 4 DBR, DBK	43 Line 5,6,7,8 Keyboard	53 CA15	63 RP15	73 TC59
04 Console Printer	14	24 XY15	34 VT15-B	44 Line 9,10, 11,12 Printer	54 CA15	64 RP15	74
05 VP15A, B, BL, CL	15	25 DP09A	35 VT15-B	45 Line 9,10, 11,12 Keyboard	55 KA15	65 Line Printer LP15	75 TC15
06 VP15A, B, BL, CL	16	26 DP09A	36	46 Line 13,14, 15,16 Printer	56	66 Line Printer LP15	76 TC15
07 VP15A, B, BL, CL	17 Memory Management	27	37	47 Line 13,14, 15,16 Keyboard	57	67 CR15	77 61 Skip on Bank Mode 62 Disable Bank Mode 64 Enable Bank Mode

Reader's Comments

XVM SYSTEM MAINTENANCE MANUAL
EK-15XVM-OP-001

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