DEC-11-HR3A-D

MM11-E
CORE MEMORY MANUAL

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MM11-E CORE MEMORY MANUAL
DEC-11-HR3A-D

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INTRODUCTION

1.1 SCOPE

This manual provides the user with theory of operation and logic diagrams necessary to understand and maintain the MM11-E Read/Write Core Memory. The level of discussion assumes that the reader is familiar with basic digital computer theory. Both general and detailed descriptions of the core memory are included.

Although memory control signals and data pass through the Unibus®, it is beyond the scope of this manual to describe the operation of the Unibus itself. A detailed description of the Unibus is presented in the PDP-11 Unibus Interface Manual, DEC-11-HIAA-D.

A complete set of engineering logic drawings is shipped with each core memory. In addition, a set of reduced drawings is included in this manual. If there is any discrepancy between the drawings in this manual and the drawings supplied with the core memory, the drawings furnished with the memory take precedence because they reflect the specific unit delivered to the customer.

This manual is divided into three major sections:

a. Introduction
b. Theory of operation
c. Adjustment and maintenance procedures

1.2 INTRODUCTION

The MM11-E is a 16-bit, 4096-word (4K), read/write core memory designed for the PDP-11. The Unibus concept is used by the PDP-11 System; thus, the central processor does not contain an integral memory. The memory used by the system is an external device and is connected to the processor through the bus interface. The core memory functions as a true peripheral and is compatible with all PDP-11 Systems. It is normally used as the basic memory unit in any system that requires a large core memory.

1.3 MM11-E GENERAL DESCRIPTION

The standard PDP-11 core memory, designated MM11-E, is a random-access, coincident-current, magnetic read/write core memory; cycle time is 1.2 μs and access time is 500 ns. The memory comprises ferrite cores wired in a 3-D, 3-wire, planar configuration. The basic unit can store up to 4096 (4K) 16-bit words. The memory can be expanded up to 28K words in 4K increments. The hard-wired address that selects the memory for use as an external device is preselected by the user simply by moving appropriate jumpers on a logic card.

The Unibus concept of PDP-11 System requires that a master/slave relationship exist between the processor and an external device or between two different external devices. Although many devices can function as either master or slave, the core memory always functions as a slave, whether the controlling unit is the processor or another peripheral. The core memory can never function as bus master.

The basic functional components of the core memory are briefly described in the following paragraphs.

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1.3.1 Core Array

The ferrite core array consists of 16 core mats, each wired in a 64-by-64 matrix. This arrangement provides a total of 4096 16-bit words of data and/or program storage. The cores are connected by three wires. An X and a Y line are used for individual core selection. The third line is a shared sense/inhibit line. There is a separate sense/inhibit line for each mat. This single line can function as either a read or write line due to the method of wiring and the control logic circuits.

1.3.2 Memory Control

Memory control circuits acknowledge the requests of the master device, determine which of the four basic operations is to be performed, and set up the appropriate timing and logic sequences to perform the desired read or write operations. The memory control logic also transfers data to or from the Unibus as required.

1.3.3 Address Selection

The core memory receives an 18-bit address from the master device. The address is decoded to determine if the memory is the selected device and to determine the core location specifically addressed. If the operation is a byte operation, bus line A00 L indicates the byte to be used. The actual read or write operation is not selected by the address but is selected by the settings of the bus C lines.

The X and Y portion of the address is decoded through selection switches and a diode matrix to enable passage of read/write current through the selected X and Y drive lines of the memory. The coincidence of these currents selects the specific 16-bit core memory location desired.

1.3.4 Inhibit Drivers

The core memory is so designed that, unless inhibited, all bit locations of the selected memory cell are switched to a logical 1 during the write portion of the memory cycle. To prevent this occurrence, each bit has inhibit drivers that are used during write time to oppose the Y write current, thereby ensuring that, if logic 0 levels are stored in the data register, they are written in the corresponding bit location of the addressed memory cell.

1.3.5 Sense Amplifiers

During the read portion of a memory cycle, sense amplifiers detect analog signals induced in the sense/inhibit windings of the core array. These signals are shaped, amplified, and then time sampled by means of a strobe signal to set corresponding bits of the data register.

1.3.6 Data Register

The data register is a 16-bit, flip-flop register used to store the contents of a word after it is read out of the destructive memory; the same word can then be written back into memory (restored) when in the data in

(DATI) mode. The register is also used to shift data from the Unibus lines to accommodate the loading of incoming data into the core memory during the data out (DATO) or data out, byte (DATOB) cycles.

1.3.7 Switches and Drivers

The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

1.3.8 Current Generator

The current generator provides the current necessary to change the state of the magnetic cores. The linear rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

1.3.9 G103 Levels and Gates Module

The G103 Levels and Gates Module performs address gating functions for X and Y selection; generates the -6V and -5.2V threshold voltages which are derived from the -15V supply; and provides an ac termination for the X-Y switching matrices.

1.4 BASIC MEMORY OPERATIONS

The core memory has four basic modes of operation. The main function of the memory is simply to read or write data. Additional modes are provided, however, to allow for byte operation and to eliminate the restore cycle when it is not needed, thereby increasing overall system efficiency. The four basic memory operations are:

a. Read/restore (DATI)

b. Read only (DATIP)

c. Write (DATO)

d. Write byte (DATOB).

These four modes are briefly discussed in the following paragraphs.

NOTE

In the following discussions, all operations refer to the master (controlling) device. For example, the term data out indicates data flowing out of the master and into the memory.

1.4.1 Data In (DATI) Cycle

The DATI cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the Unibus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first part of the cycle, the memory loads the data into a register; at the same time, the memory applies the data to the Unibus. Then, during the second part of the cycle, the memory takes the data from the register and writes it back into the memory location.

1.4.2 Data In, Pause (DATIP) Cycle

Normally in reading memory, the information is destroyed in the particular location accessed, and the data must be restored. However, sometimes it is not actually necessary to restore the information after reading, because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The DATIP operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a DATIP must always be followed by a write cycle (either DATO or DATOB).

1.4.3 Data Out (DATO) Cycle

The DATO cycle is a write memory cycle used by the master device to transfer data into core memory. To ensure that proper data are stored, the memory unit must first be cleared by reading the cores (thereby setting them all to zero) before writing in the new data. During a normal DATO, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the bus into the selected core location. If a DATO follows a DATIP (rather than a DATI), the sequence is not the same. The DATIP clears core and generates a pause flag; thus, the memory skips the read cycle and immediately begins the write cycle. This process reduces the DATO cycle time by approximately 50 percent.

1.4.4 Data Out, Byte (DATOB) Cycle

The DATOB cycle is similar in function to the DATO cycle, except that during DATOB data are transferred into the core memory from the bus in byte form rather than as a full word. Actually, an entire word is loaded into the selected memory location: the selected byte which is new data from the bus and the non-selected byte, which is restored data from the word previously stored in that memory location. During the read cycle, the non-selected byte is saved by storing it in the data register while the selected byte is cleared. During the write cycle, only the selected byte portion of the word is loaded into the memory location from the bus. At the same time, the non-selected byte is restored from the data register into the memory location. In effect, the memory is first cleared and then simultaneously performs a restore cycle for the non-selected byte and a write cycle for the selected byte.

CHAPTER 2
THEORY OF OPERATION

2.1 INTRODUCTION

This chapter provides a detailed description of the MM11-E Core Memory. The first topic is the core array and overall memory operation. Subsequent paragraphs describe X- and Y- line selection and decoding, read/write operation, control and timing logic, read/write drivers and switches, and the current generator.

The information in this chapter is supported by a complete set of engineering drawings. All calibration and adjustment information is included in Chapter 3.

2.2 CORE ARRAY

The ferrite core memory consists of 16 memory mats, each mat containing 4096 ferrite cores arranged in a 64-by-64 array. Each mat represents a single bit position of a word; therefore, the memory is referred to as a planar memory. This planar configuration provides a total of 4096 16-bit word locations. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or a binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals. The ferrite cores themselves are 20-mil cores. The outside diameter of each core is 22 mils, and the inside diameter is approximately 16 mils. Each core is 5.5 mils thick.

Selection and switching of the cores is provided by only three wires traversing each core in a special selection technique. An X-axis read/write winding passes through all cores in each horizontal row for all 16 mats. A Y-axis read/write winding passes through all cores in each vertical row for all 16 mats. Through the use of selection circuits which control the current applied to specific X-Y windings, any one of the 4096 word locations can be addressed for writing data into memory or reading data out of memory. A third line passes through each core on a mat to provide the sense/inhibit functions. There is one sense/inhibit line per mat. This single sense/inhibit line, as well as the selection circuits, are discussed in subsequent paragraphs.

2.3 MEMORY OPERATION

Figure 2-1 illustrates a typical portion of the core memory. An X and Y winding pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field caused by the coincident current of both an X and a Y winding can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple winding arrangement to select one and only one memory core out of the possible 4096 contained on each mat. The current passing through either an X or Y winding is referred to as the half-select current.

A half-select current passing through the X3 winding (see Figure 2-1) from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 0 to 1 state. The flux produced by the current is, however, insufficient to complete the state transition in any core. Simultaneously passing a half-select current through the Y1 winding from top to bottom produces the same effect on all cores in that particular vertical row. Note, however, that both currents pass through only one core which is located at the intersection of the X3 and Y1 windings. This is the selected core and the combined current values are sufficient to change the state of the core.

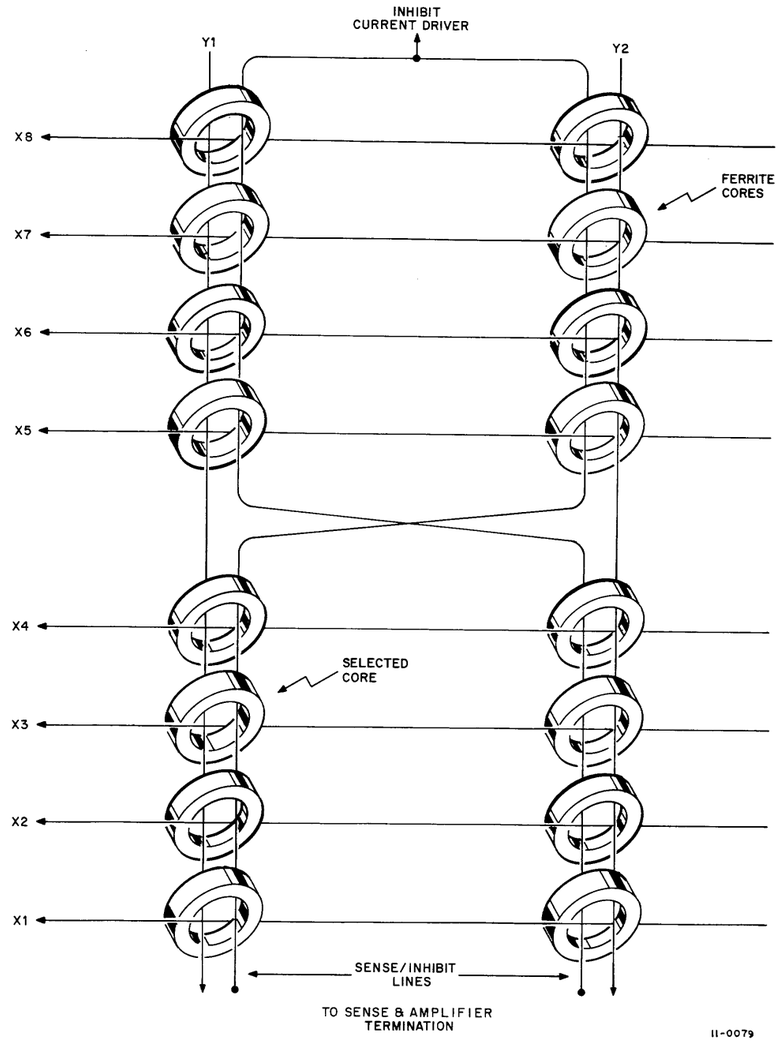


Figure 2-1 Three-Wire Memory Configuration

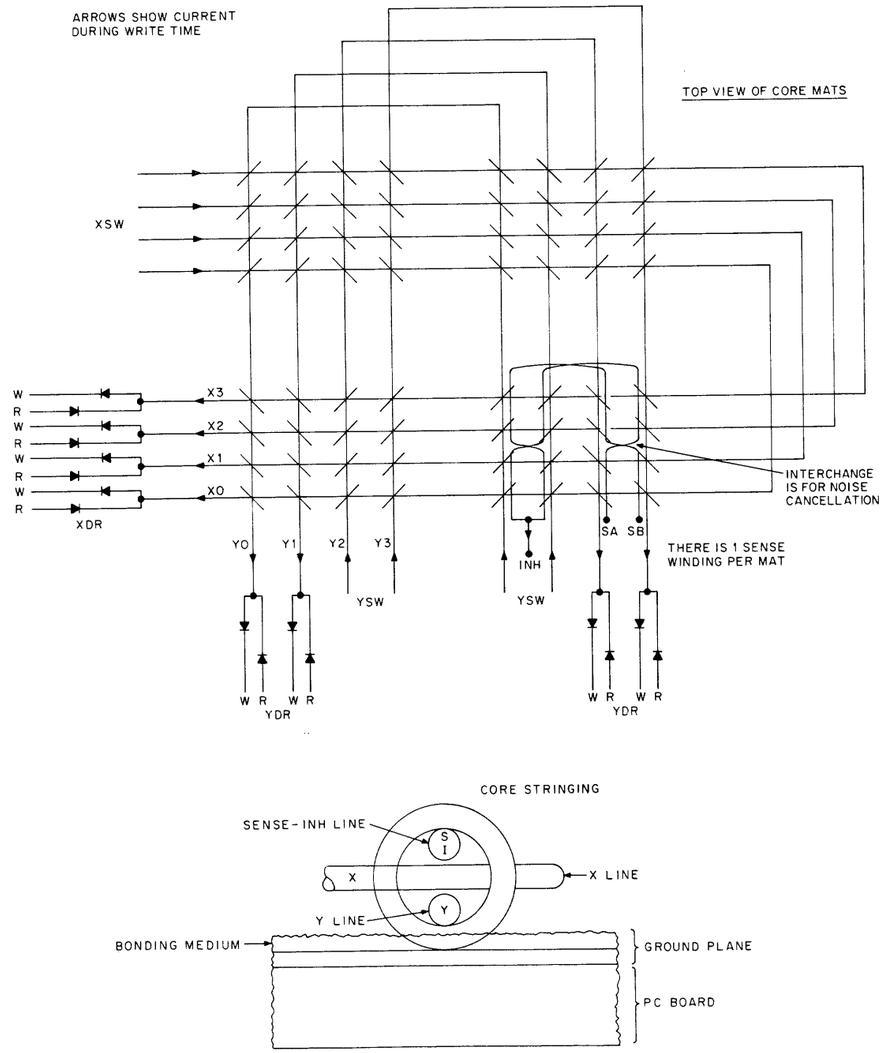


Figure 2-2a. Three-Wire 3D Memory, Four Mats Shown for a 16-Word – 4-Bit Memory

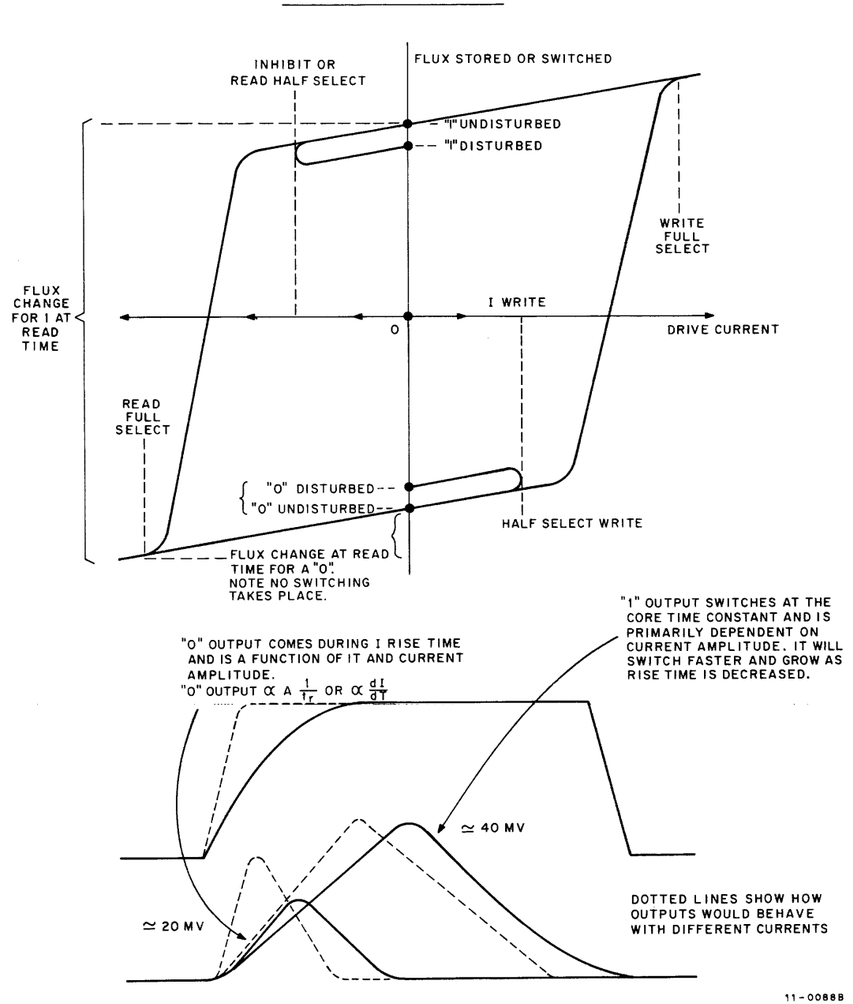


Figure 2-2b. Hysteresis Loop for Core

All X and Y windings are arranged in such a manner that whenever a half-select current is passed through each, the resultant magentic fields combine in the core at the point of intersection. This combined, full-select current ensures that the selected core is left in the binary 1 state. The currents used to select the core are referred to as write currents.

In the MM11-E Core Memory, the X3 windings in all 16 mats are connected in series as are the Y1 windings. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an identical core on the other 15 mats. The X3-Y1 cores on all mats switch to a binary 1, causing each of the 16 cores to become one bit of a 16-bit storage cell.

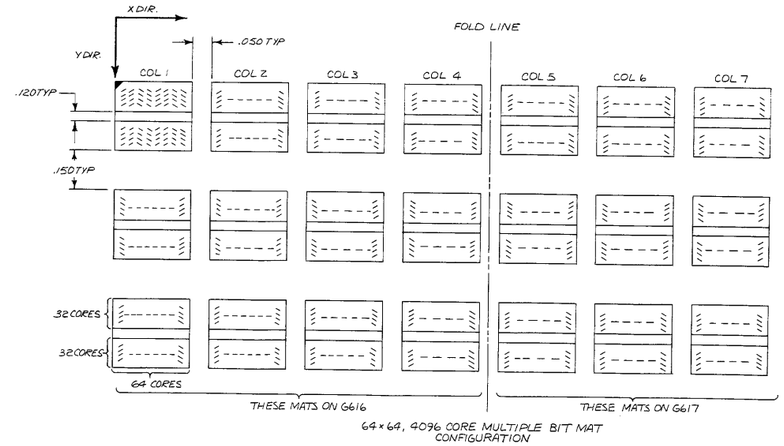
Because of the serial nature of the X-Y windings, a method must be employed to set certain cores to the 0 state; otherwise, every 16-bit word selected would be all 1s. The method used in the MM11-E Core Memory is to first clear all cores to the 0 state by reading and then, using an inhibit winding, inhibit cores on particular mats. The inhibited cores remain 0s even when identical cores on other mats are set to 1s.

In many memories, the inhibit line serves only the inhibiting function; however, in the MM11-E, this line serves as both an inhibit and sense line. As a result, only a three-wire memory is necessary, rather than a four-wire memory. Only the inhibit function is discussed at this point.

The half-select current for the inhibit lines is applied from an inhibit current driver, which is a switch and a resistor between the inhibit line and -15V. The current in the inhibit line flows in the opposite direction from the write current in that line and cancels out the write current. There is a separate inhibit driver for each memory mat, and each mat represents one bit position of a word; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. It must be remembered that the inhibit function is active only during write time.

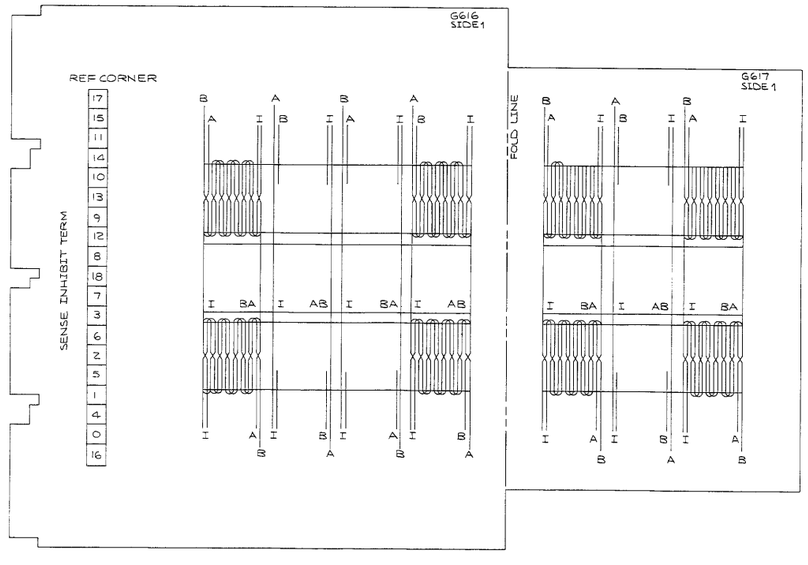
The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle with one notable exception: the X and Y currents are in the opposite direction. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not affected. Whenever the core changes from 1 to 0, the flux change induces a current in the sense winding of that mat. This current is detected and amplified by a sense amplifier. The amplifier strobes the signal into the data register for eventual transfer to the Unibus.

Figure 2-2 shows a 16-word by 4-bit planar memory. The MM11-E Core Memory functions in the same manner, except that it has 64 X-lines, 64 Y-lines, and 16 core mats. The core stringing is identical, and the sense windings are strung through all 4096 cores with the interchange between X31 and X32 instead of between X1 and X2. The actual configuration is shown in Figures 2-3 through 2-6. These figures show the core orientation, the sense inhibit windings, the X-Y lines, and word size variation.



NOTES:
1. DIMENSIONS SHOWN ARE CORNER, OR END, CORE TO CORE CENTER SPACING.
2. CORE CENTER TO CENTER SPACING ON 'Y' AXIS = .015" NOM.
3. CORE CENTER TO CENTER SPACING ON 'X' AXIS = .025" NOM.
4. CORE PATTERN TO BE "DOUBLE HERRINGBONE" PATTERN. THE LINES INSIDE THE MAT AREAS SHOW THE ORIENTATION OF THE PATTERN. NOTE THE MAT INVERSION ALONG THE 'Y' AXIS.
5. EACH MAT TO BE 64 X 64 WITH .120 SPACE TO ENABLE A SENSE WINDING INTERCHANGE.

Figure 2-3 Core Orientation



NOTES:
1. WINDINGS TO BE #40 INSULATED MAGNET WIRE
2. A AND B WIRES ARE TO BE TWISTED TOGETHER, A MINIMUM 10 TURNS PER INCH, BETWEEN MATS AND TERMINATIONS.
3. THE TWO WIRES MARKED 'I' WILL BE TWISTED AS IN NOTE 2.
4. SENSE INHIBIT WIRES WILL BE IMMOBILIZED AT 4 TO 2 INCH INTERVALS BY BEADS OF ADHESIVE OR SOME EQUIVALENT METHOD.
5. WINDINGS SHOULD BE UNIFORM WITH SMALL TURN AROUND LOOPS, BUT NOT SO TIGHT AS TO PULL THE CORES OUT OF ALIGNMENT.

Figure 2-4 Sense Inhibit Windings

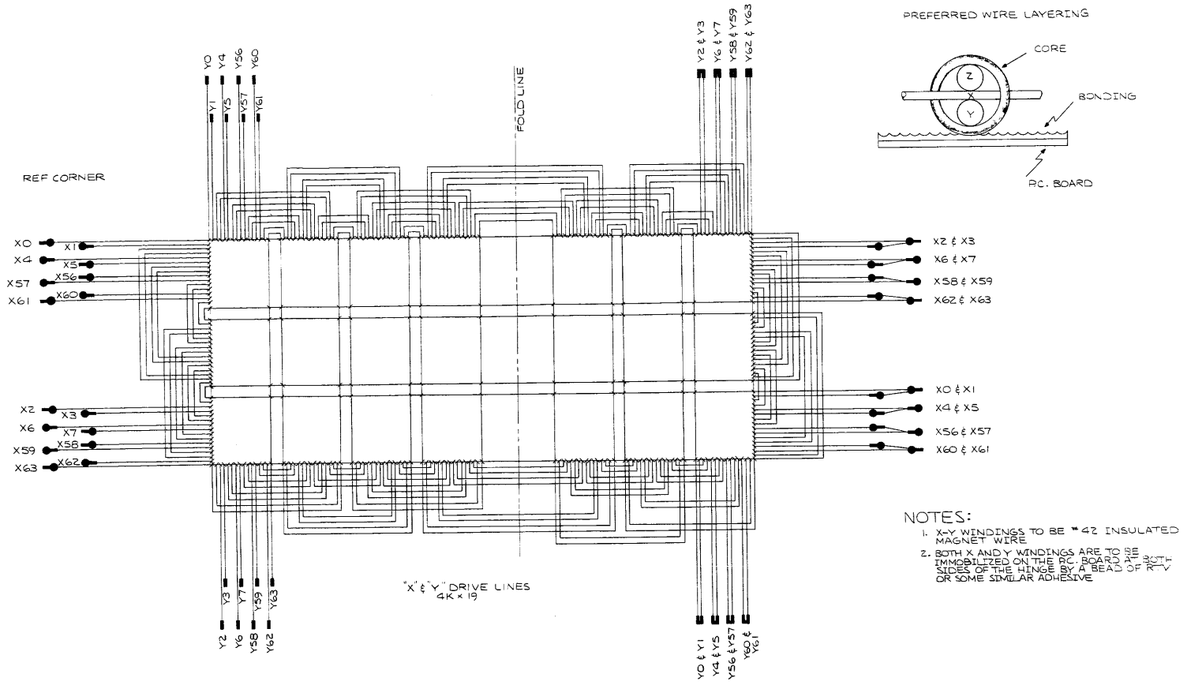


Figure 2-5 X-Y Windings

ASSY	BD1	BD2	TERM X AT	TERM Y AT	OMIT CORES IN MATS	# BITS	SPEC VAR
H203	G616	5508508	X1	Y1	B,G,H,J (G616)	8	-1
H204		5508508	X1	Y1	G,H,J (G616)	9	-2
H205		5508508	X1	Y2		12	-3
H206		G617	X2	Y3	B,K,L,M,D,E,F(G616+G617)	13	-4
H207		G617	X2	Y3	A,B,C,E,F (G616+G617)	16	-5
H208		G617	X2	Y3	A,D,E,F (G616+G617)	17	-6
H209		G617	X2	Y4	A,B,C (G616+G617)	2	-7
H210	G616	G617	X2	Y4	B,C (G616+G617)	19	-8

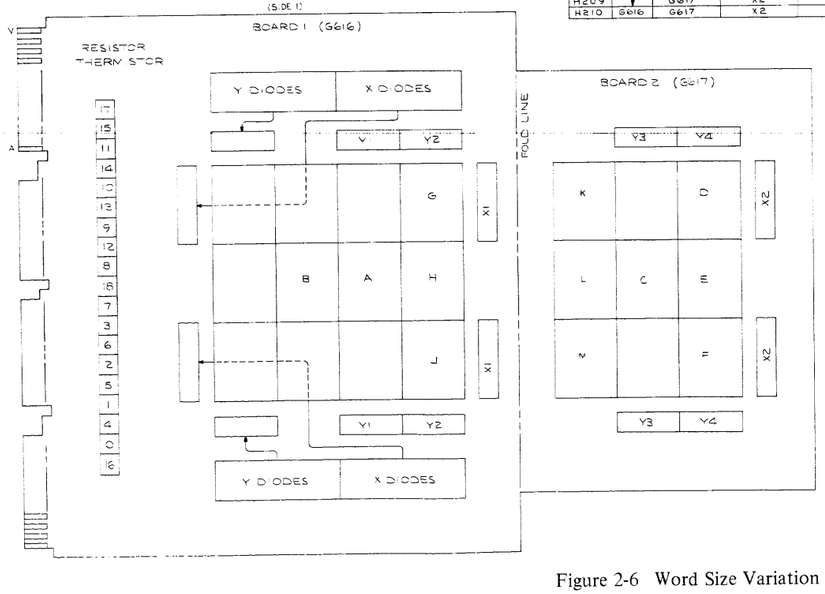


Figure 2-6 Word Size Variation

2.4 X- and Y-LINE SELECTION

Previous paragraphs have explained the method for selecting a specific core by passing half-select current values through specific X and Y windings. This paragraph is devoted to an explanation of the method used for selecting the specific X and Y lines.

An 8-by-8 decoding matrix is used to select 1 of the 64 X-lines. An identical matrix is used to select 1 out of the 64 Y-lines. For ease of presentation, only X-line decoding is discussed. Decoding of the Y lines is identical.

The 64 X-lines are represented by octal numbers 00 to 77. Figure 2-7 is a simplified schematic of the circuits used to decode the address that selects one of the octal lines. The most significant octal digit is selected by selection switch decoders A and B and the least significant octal digit is selected by driver decoders C and D. For example, the 4 output from the B decoder and the 6 output from the D decoder select line X46.

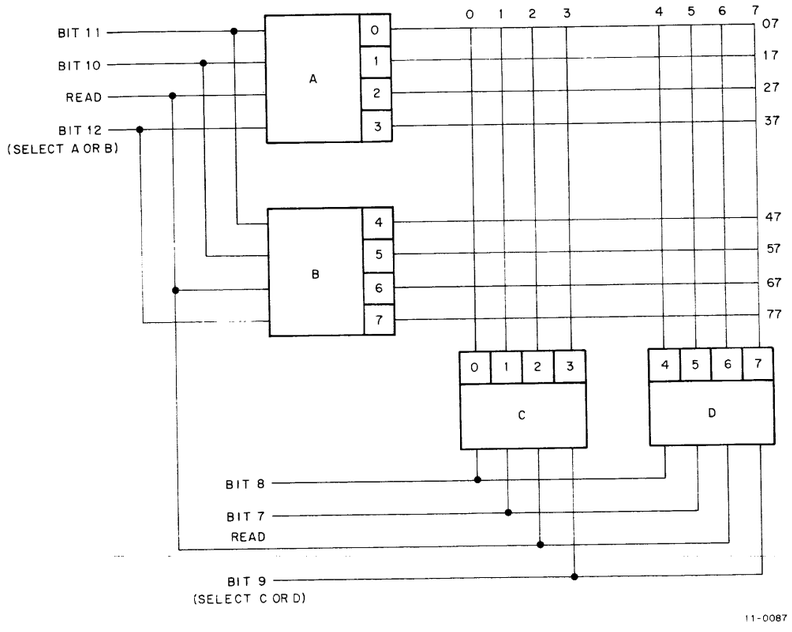


Figure 2-7 8-by-8 Address Selection, Simplified Schematic

The incoming address actually performs four separate functions; however, only X-line decoding is discussed at this point. The four functions and corresponding bit assignments of the address are listed in Table 2-1.

Table 2-1
Address Functions

Bit Assignment	Function
0	Select byte only during DATOB
1 thru 6	Y-line selection bits 1 thru 3 = positive, negative drivers 0 thru 7 bits 4 thru 6 = positive, negative switches 0 thru 7
7 thru 12	X-line selection bits 7 thru 9 = positive, negative drivers 0 thru 7 bits 10 thru 12 = positive, negative switches 0 thru 7
13 thru 17	Device selection

Figure 2-8a is a representation of one pair of decoders used to select the selection switch that corresponds to the most significant octal digit of the X line. As the method of decoding is slightly unorthodox, consider the A and B decoders as a single 4-line to 16-line decoder with 16 output pins. There are two pins for each switch: one for read operations and one for write operations. Figure 2-8b indicates the 16 possible outputs and the function of each. There are eight read switches and eight write switches.

In actuality, bit 12 of the incoming address effectively selects either the A or B decoder. If the bit is a binary 0, the A decoder is used; if the bit is binary 1, the B decoder is used. The read signal selects one half of the selected decoder. If the read signal is present, the output comes from the upper half of the decoder, and one of the four read outputs is used. If the read signal is absent, the lower half of the decoder provides one of the four write outputs. The remaining two bits, bits 10 and 11, select one of the four outputs (0 through 3) from the preselected part of the decoder.

As an example, assume that all bits are set and a read signal is present. Bit 12 set selects the B decoder. The read signal selects the upper half of the decoder. Bits 10 and 11 set represent a binary 3 so that output 7 from pin 3 is the selected read switch.

Assume now that only bit 11 is set and the read signal is not present. Bit 12 being 0 causes the A decoder to be used. The absence of a read signal effectively selects the lower (write) portion of the decoder. Bit 11 being set with bit 10 being 0 represents a binary 2. The third number (binary 2) in the write portion of the decoder is represented by pin 6. Therefore, the decoded octal digit output is write switch 2.

Decoders C and D function in an identical manner to select the read/write driver which corresponds to the other X octal digit.

The portion of the address used to select the Y lines is represented by bits 1 through 6. Therefore, bits 1 through 12 of the incoming address are used to select the X and Y lines that determine the specific core where a bit is to be read or written.

The X and Y selection logic is shown on drawing MM11-E-03, sheets 1 and 2. The decoder output numbers are not shown on the drawings in the same manner as described in this section. Figure 2-9 indicates the relationship between the output numbers shown on Figures 2-7 and 2-8, and the line number, function, and pin number shown on the MM11-E block schematics.

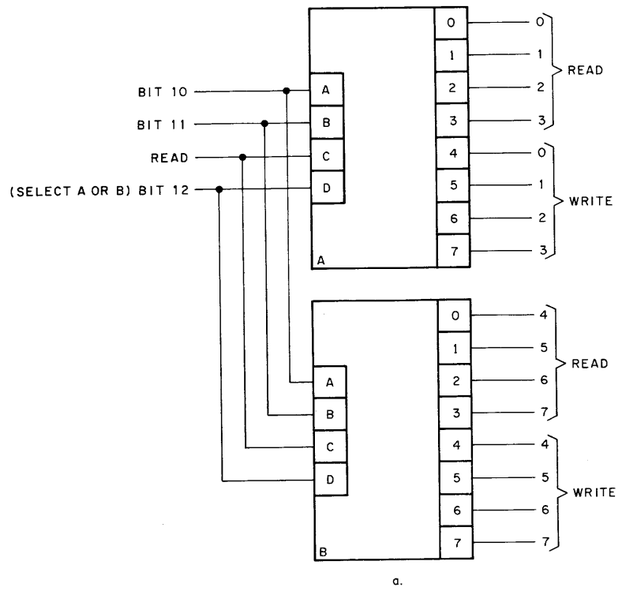


Figure 2-8 X-Line Decoding

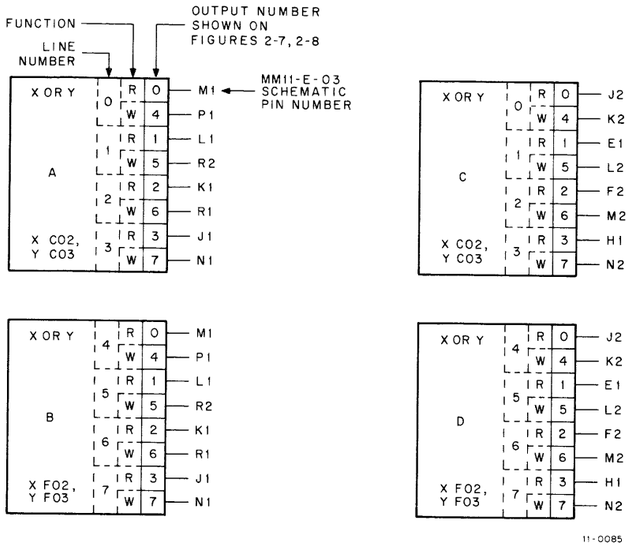


Figure 2-9 Pin Number Relationship

Figure 2-10 shows the switch or driver base drive circuit that is connected to the decoder. The timing and address inputs cause the 8251 decoder output to go to ground and current i_1 flows from the +5V supply, through the resistor, through the transformer primary, and into the decoder output. The value of the current is determined by the resistor and the voltage reflected into the transformer primary (approximately 1.0V). An equal current (i_2) is induced into the base emitter circuit connected to the transformer secondary. This current turns on the transistor. Note that all base current is provided from this circuit and the current from circuit i_3 equals the collector current.

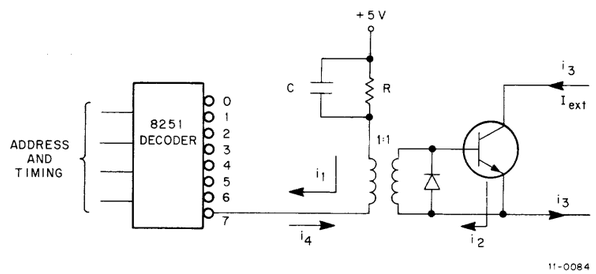


Figure 2-10 Switch or Driver Base Drive Circuit

When the decoder is turned off by the timing input, its pull-up transistor now tries to drive current in the opposite direction (i_4). The capacitor performs two functions: it speeds up the turn-on current i_1 and allows the decoder to pump reverse current i_4 into the transformer primary. The reverse current is necessary to remove the base emitter charge on the output transistor in the transformer secondary to turn it off. The base emitter diode prevents reverse breakdown of that junction during turnoff. Since this diode limits the transformer secondary voltage during turnoff, some of the circuits contain two diodes in series to allow faster transformer recovery. Note that the dc level of the output transistor is irrelevant. This transistor is saturated when on.

2.5 DRIVERS AND SWITCHES

Drivers and switches direct the flow of current through the cores to ensure proper polarity for the desired read or write function. A read driver and switch, as well as a write driver and switch, are provided for groups of eight X lines and groups of eight Y lines in the selection matrix, such that each axis has its 64 lines selected by an 8-by-8 matrix.

Figure 2-11 is a simplified diagram of the switches and drivers. The diagram represents one X line. Note that the flow of read current is shown by a solid line, and the write current path is shown by a broken line.

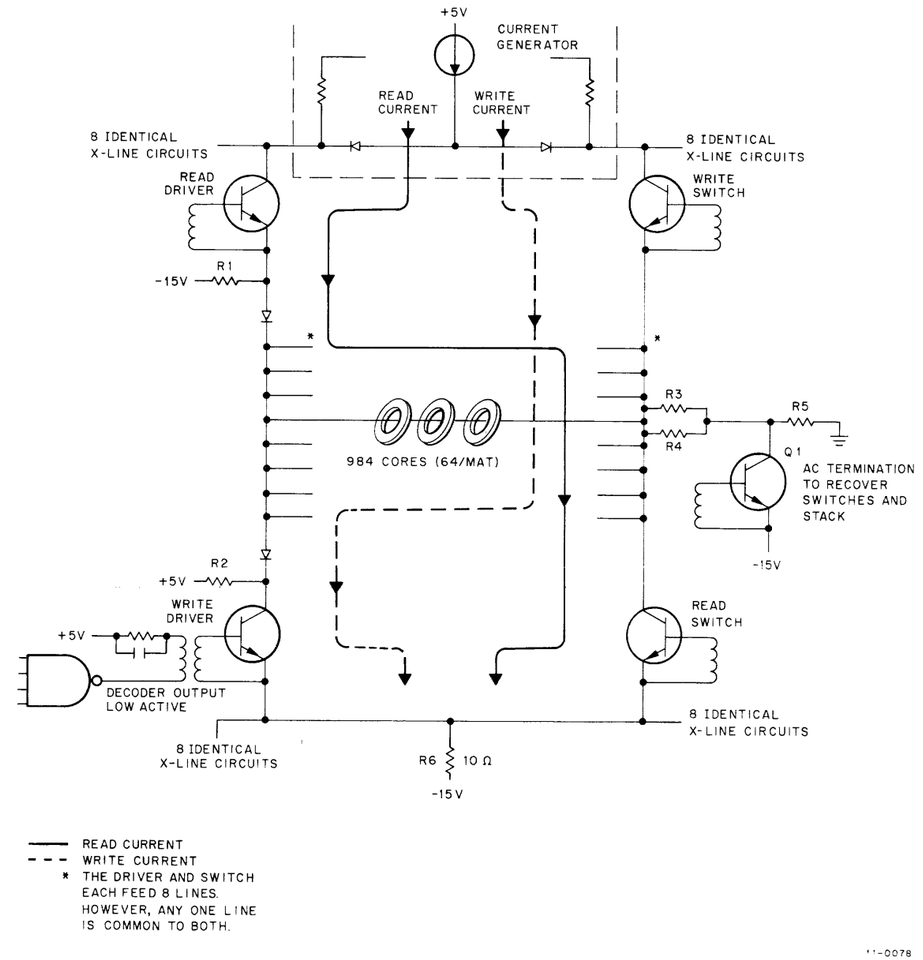


Figure 2-11 X-Line Drivers and Switches

When a read operation is selected, the read driver and read switch are turned on, and the write driver and write switch are turned off. The output current from the current generator flows through the read driver, through the cores on the associated X line, and through the read switch. When a write operation is selected, the write driver and switch are turned on, and the read driver and switch are turned off. In this case, current from the current generator flows through the write switch, through the cores (in the opposite direction from that during read), and through the write driver. The signals that select the read and write operations are given in Table 2-2. Each line has 64 x 16 (or 984) cores on it as it threads through all 16 mats.

Table 2-2
Read and Write Selection

Driver or Switch	Signals Required to Turn On
Read Driver	ADDRESS and TDR and READ H
Read Switch	ADDRESS and TSS and READ H
Write Driver	ADDRESS and TDR and WRITE H
Write Switch	ADDRESS and TSS and WRITE H

NOTE
READ H and WRITE H are both outputs of the same control flip-flop. When the READ flip-flop is set, the output is READ H; when it is cleared, the output is WRITE H.

Resistors R1 and R2 are provided as terminations to prevent unwanted currents from affecting the drivers and switches. The circuit that comprises transistor Q1 and resistor R5 is used to make the write current equal the read current and to assist the ferrite core stack in recovering. This method is much faster than allowing the stack to recover by itself. The decoder output and write driver transformer base drive are shown. All base drives are similar.

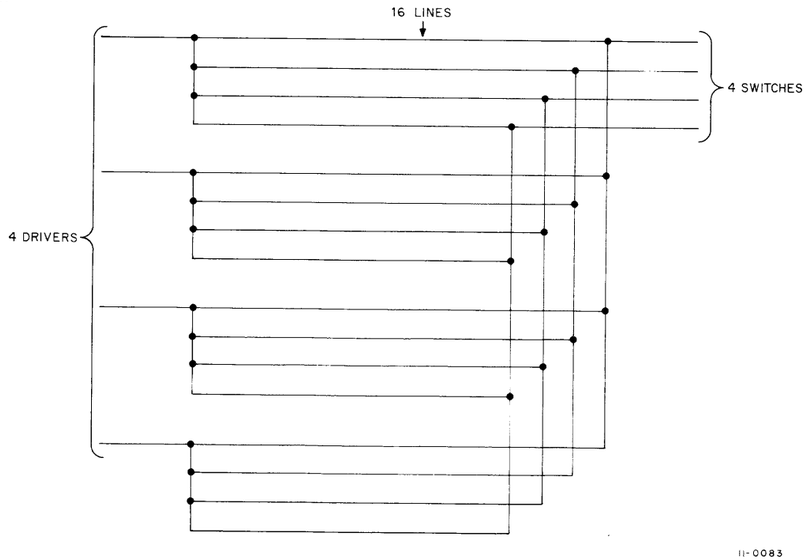


Figure 2-12 Simplified Interconnection Diagram

The drivers and switches in one line share a common line with drivers and switches in other lines. Figure 2-12 (representing 16 lines on a 4-by-4 matrix) shows the interconnection of four drivers and four switches on 16 lines to aid in understanding the interconnection of all 64 lines in the 8-by-8 matrix. Only one line is common between any driver and switch.

2.6 CURRENT GENERATOR

The current generator provides the current required to change states of the magnetic core. The design of the generator is such that the linear rise time and amplitude of the output current waveform ensure optimum switching of core states. Figure 2-13 is a simplified schematic of the current generator, and Figure 2-14 illustrates the test point and output waveforms.

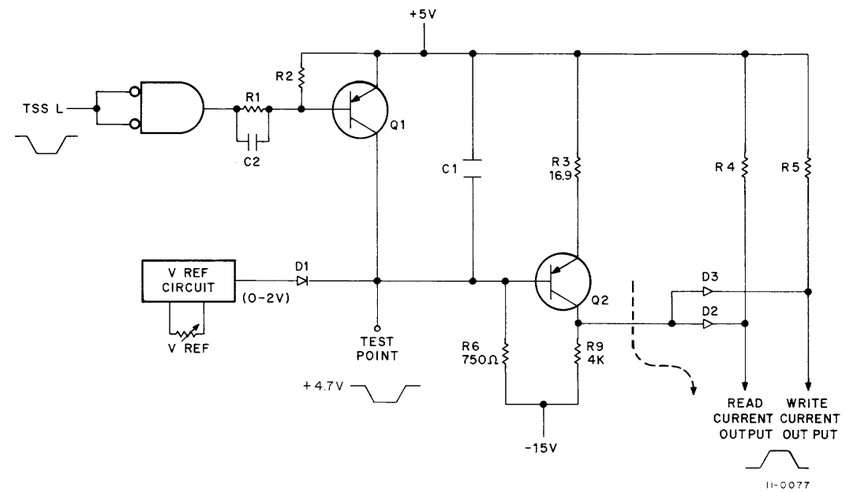


Figure 2-13 Current Generator, Simplified Schematic

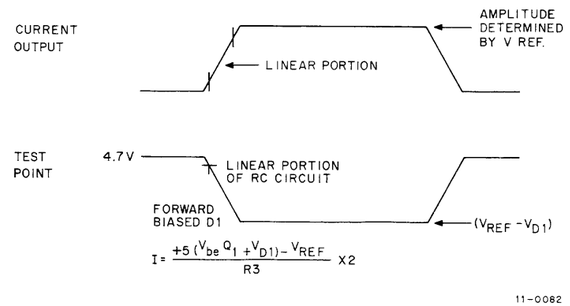


Figure 2-14 Current Generator Waveforms

When the current generator is in the quiescent state, transistor Q1 is saturated, thereby holding the voltage level at the test point to 4.7V. Diode D1 blocks any voltage from the voltage reference (V REF) circuit, and transistor Q2 is cut off. Therefore, the only output at this time is the current through R4 and R5, which is negligible.

Operation of the current generator is triggered by the negative-going TSS L signal from the memory control circuits. This signal is inverted by an AND gate and used to cut off transistor Q1. When Q1 cuts off, it allows the voltage at the test point to start going negative until it reaches the forward bias level of diode D1. This level is equal to the voltage reference minus the voltage drop across diode D1. The voltage reference circuit contains a trimpot to adjust the output between 0V and 2V. The adjustment procedure is given in Chapter 3.

At the same time that transistor Q1 cuts off, capacitor C1 begins charging. The time constant of C1 and resistor R6 determines the rise time as Q2 conducts to provide the read current. The write current is developed in the same manner. There are actually two circuits (R3 and Q2) in parallel.

The value of the output current is:

$$\frac{+5V\,(-V_{beQ2} + V_{beD1}) - V_{ref}}{R3}$$

This value is approximately 250 mA per circuit, or approximately 500 mA for the two circuits. The amplitude of the current output waveform is determined by the setting of the V REF trimpot. Resistors R4 and R5, and diodes D2 and D3 in the output lines are used to isolate the read switches from the write switches.

Although not shown on the schematic, a resistor and thermistor on the memory stack (see drawing MM11-E-03) are connected to the voltage reference portion of the current generator. These components automatically track the current amplitude with temperature to ensure that the amplitude remains within specified tolerances over the temperature range of 0° C to 50° C.

2.7 CONTROL AND TIMING LOGIC

The memory control and timing logic circuits perform three basic functions:

a. Decode the incoming address (bits 13 through 17) to determine if the memory has been selected to engage in a data transfer

b. Latch the address bits controlling the X and Y lines (bits A1 through A12) to ensure that the proper core location is selected

c. Perform the appropriate data transfer as requested by the master device by providing all internal memory timing.

The following paragraphs discuss device selection, X-Y address latching, and control and timing circuits for each of the four transfer operations (DATI, DATIP, DATO, and DATOB).

The control and timing circuits are shown on drawing MM11-E-05, Sheets 1 and 2. Sheet 2 contains the logic associated with the bus address and data lines, including the device selection logic. The remainder of the control and timing logic circuits are shown on Sheet 1. The timing diagram is on drawing MM11-E-08.

Details of the one-shot delays on the M729 Module are shown on Figure 2-15. This figure provides circuit drawings and waveforms for each of the three types of one-shots used on the M729 Module.

2.7.1 General

All memory operations are started by the generation of a memory select (MSEL) signal. This signal is initiated on receipt of a MSYN (master sync) signal from the controlling device, a device select (D SEL) signal from the memory address (A13 through A17) decoding circuits, and a DC OK signal. These signals indicate, respectively, that a master device has control of the Unibus, that the master device has selected the core memory as a slave device, and that the dc power level to the memory circuits is within specified tolerances. The three signals set the M SEL flip-flop to produce the memory select signal. This signal remains asserted until either the END·WRITE or END PAUSE signal clears the flip-flop to indicate that the selected memory operation is complete. The M SEL flip-flop also acts as a memory busy signal by prohibiting a new cycle from starting until M SEL is cleared.

The bus master places appropriate levels on the two bus C lines to select the type of memory operation to be performed. The data placed on these lines by the master to select a specific operation are shown in Table 2-3.

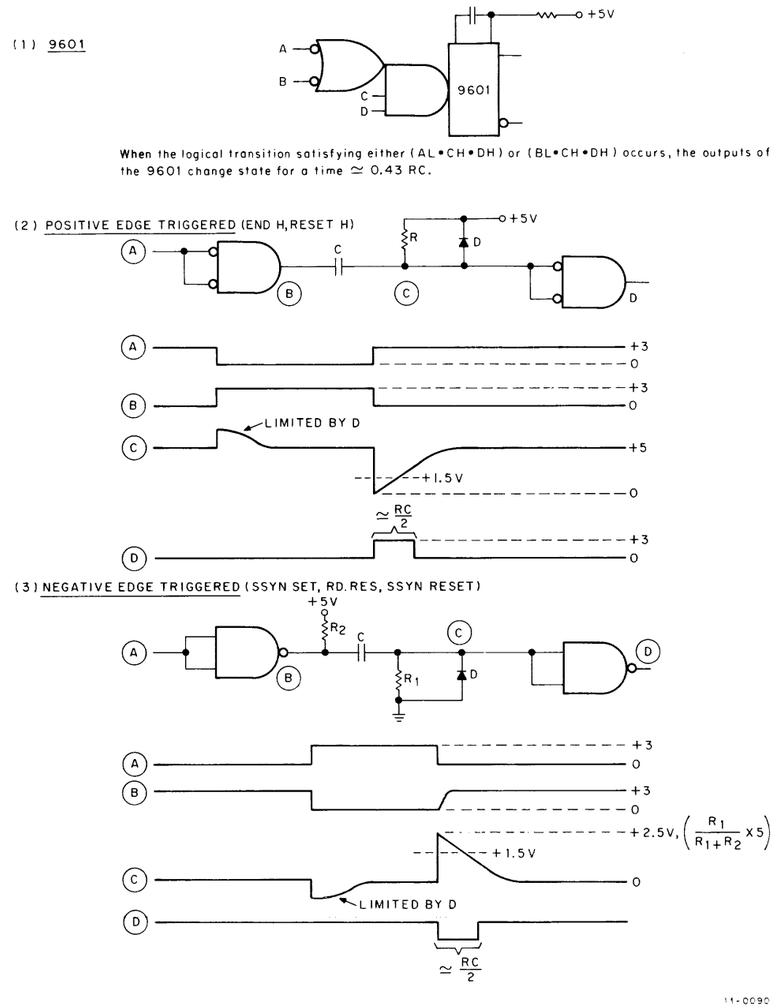


Figure 2-15 M729 One-Shot Delays

Table 2-3
Selection of Memory Operation

C Line State	Octal Equivalent	Selected Memory Operation
C0 H, C1 H	0	DATI
C0 L, C1 H	1	DATIP
C0 H, C1 L	2	DATO
C0 L, C1 L, A0 H	3	DATOB 0
C0 L, C1 L, A0 L		DATOB 1

2.7.2 Device Selection

Whenever a master device addresses another peripheral as a slave, the address is applied to all peripherals connected to the Unibus. Therefore, it is necessary for each peripheral to have a method of recognizing its own address and ignoring other addresses. The device selection circuits serve this purpose. The 18-bit address from the master device is used for both device selection and selection of the X-Y matrix. This paragraph covers the memory device selection circuits and Paragraph 2.7.3 covers the X-Y selection.

Bus address lines 13 through 17 are used for device selection. The selection logic is dependent upon jumpers connected to the input of a seven-input NAND gate, SP 314A. The device address is hard wired. If, for example, the desired bit is to be 0, a jumper is connected to the inverter output of the address buffer and ties this signal to the SP 314A gate. When a 0 is placed on the associated bus line, that leg of the SP 314A gate is qualified. It produces an output if all of the other four inputs to the gate are satisfied (three of the seven are always grounded). If the bus line has a binary 1, that device selection gate leg is not qualified and the SP 314A gate cannot be qualified. On the other hand, if a binary 1 is desired in the address code, a jumper is connected directly from the bus line to the input of the SP 314A gate, bypassing the inverter gate for that line. This causes the SP 314A gate to be qualified whenever a 1 is present on the bus line. In this manner, any combination of 1s and 0s can be preselected as the device address. When the proper signals are present on bus address lines 13 through 17, the SP 314A gate is qualified and produces a high output which is the device select (D SEL) signal. This signal indicates that the master device has selected the core memory as the slave device.

2.7.3 X-Y Address Latching

Bus address lines 1 through 12 are used for selection of the X and Y lines that select the desired core location (refer to Paragraph 2.4). Bits 1 through 6 select the Y lines, and bits 7 through 12 select the X lines.

When the bus master generates MSYN, the full 18-bit address appears at the memory control circuits. The five most significant bits are used by the device selection circuits (refer to Paragraph 2.7.2). The next 12 bits are gated into a flip-flop register. If the bit is low on the bus, it qualifies a gate that sets a corresponding flip-flop. If the bit is high on the bus, the gate is not qualified and the corresponding flip-flop remains cleared. The flip-flop is set low rather than high because of the negative logic used by the Unibus. The original X-Y address from the master device is now stored in the flip-flop register to be used by the decoding circuits during the selected memory operation. An asserted address bit is high (+3V) inside the memory.

Bus address line 0 is used for byte selection. The level on line 0 passes through a gate and is stored in a flip-flop in the same manner as the X-Y address lines. The output of the flip-flop represents either byte 1 when set or byte 0 when not set and is applied to the memory control circuits described in Paragraph 2.7.7.

2.7.4 Data In (DATI) Control Circuits

A DATI operation indicates that a selected location in memory is to be read and the information transferred through the Unibus into the master device. Because the core memory is a destructive readout device, the data must be restored to the selected location after the read operation. Therefore, a DATI is basically a read/restore (read/write) operation.

In the following discussion, assume that all flip-flops are initially in the RESET state. When the M SEL signal is generated, it qualifies an AND gate to produce a clock high (CLK H) pulse that latches the address. The M SEL flip-flop is set by CLK L. The CLK H pulse, together with the PAUSE L high pulse, sets the READ flip-flop which generates the READ H signal. The CLK H pulse is also gated through an OR gate to trigger two one-shots at the same time the READ signal is generated to produce the TDR H and TSS H signals. These two signals are gated into the address decoders to enable the current paths through the X and Y switches and drivers. This process enables the decoding matrix so that the selected core location receives read current.

The READ signal also triggers a strobe delay (STROBE DEL) one-shot to produce a delay of approximately 190 ns. This delay is used as a RESET L signal. This RESET L clears the data register flip-flops at the start of the read operation, before STROBE H comes high.

After the data register flip-flops have been reset, the current flowing through the selected cores produces an output at the sense amplifier for every bit position having a logical 1 (refer to Paragraph 2.8).

When the strobe delay is completed, a STROBE H pulse is generated and applied to the sense amplifier. Whenever an amplifier has an output exceeding the threshold level (during strobe time), it direct sets the associated flip-flop. The STROBE pulse is 70 ±10 ns wide. This width is fixed and cannot be changed. The STROBE DEL trimpot is factory adjusted so that the STROBE pulse occurs at the 10% point of read current +210 ns to make certain that core transitions are compared to the threshold level at the sense amplifiers at the proper time for best overall memory margins from 0° to 50° C.

When the STROBE pulse goes low, the slave sync (SSYN) flip-flop is set. The output of this flip-flop is gated with C1 L through an inverter gate to produce a DATA OUT H signal and also gates a bus driver to produce a BUS SSYN L signal. The DATA OUT H signal gates the outputs of the data register flip-flops onto the Unibus through the open collector bus drivers.

In effect, the memory places data from the selected core location on the Unibus data lines and asserts SSYN to inform the master device that it can now strobe in the data. After the master has strobed the data, it raises MSYN L which causes the memory control to produce a SSYN RESET signal. This action completes the read portion of the memory cycle. The memory then immediately enters the restore portion of the cycle.

Between the end of the read cycle and the beginning of the restore cycle, all signals go back to their initial conditions with the exception of the M SEL signal. Although MSYN is dropped, the M SEL flip-flop remains set, because it can only be cleared by an INIT L signal (which is not present) or the combination of WRITE H and READ H (which is not present at this time).

When the READ flip-flop is reset by RD RES and READ H pulses, a WRITE H level is generated. The RD RES and READ H pulses cause the TSS and TDR signals to be generated to enable the switches and drivers in the X- and Y-selection matrices. The WRITE H and TSS H pulses qualify an AND gate and two parallel OR gates to produce the inhibit pulses (INH H). These inhibit pulses function in the manner described in Paragraph 2-9. The current flowing through the X and Y switching circuits writes 1s into all cores not inhibited, and the memory location contents are restored to their original state. At this time, an END H pulse is generated, which is ANDed with WRITE H; the M SEL flip-flop is cleared; all other signals return to their original state; and the restore portion of the cycle is completed. The M SEL flip-flop performs the function of locking out MSYN L so that a new cycle cannot be started until the old cycle is completed.

2.7.5 Data In, Pause (DATIP) Control Circuits

A DATIP operation indicates that a selected location in memory is to be read out and the information transferred through the Unibus to the master device. Even though the memory is a destructive readout device, the restore cycle is not entered because a DATIP indicates that new data is to be stored in the memory location. Therefore, a DATIP skips the restore cycle and pauses until either a DATO or DATOB cycle is selected by the bus master device to write the new data into the memory location.

The read portion of a DATIP is identical to that of a DATI (as explained in Paragraph 2.7.4) until the SSYN signal is produced. At this point, the output of the SSYN flip-flop and the output of the DATIP gate (from bus line C1) are applied to the PAUSE flip-flop to set it. This action produces PAUSE L which is the pause flag. This pause flag prevents the READ flip-flop from being set, thus forcing the next cycle to be a DATO or DATOB. The PAUSE L and END H levels clear M SEL, and the memory control circuits revert to their original state with the exception of the pause flag which remains set. The restore (or write) portion of the memory cycle is inhibited. Regardless of which operation is defined, the next time memory is selected it performs a write only operation.

In normal memory operation, it is always necessary to read the memory before writing into it. This read operation magnetically changes all cores to zero, thereby clearing all cores before new data are written into them. In the case of a write operation (DATO, DATOB) that follows a DATIP, this read operation is not necessary because the cores have already been zeroed by the previous DATIP read operation. Note, however, that the DATO cycle following a DATIP is not identical to the DATO cycle that follows a DATI. In the former case, the pause flag is set; while in the latter, the pause flag is cleared. Discussion of a DATO with the pause flag cleared is covered in Paragraph 2.7.6.

The DATO operation associated with a DATIP begins when the master device asserts MSYN to provide a M SEL signal as before. The CLK H pulse is also generated as before, but because the pause flag is set, no READ signal is produced. The READ flip-flop remains cleared and produces a WRITE H output. Data from the bus master is applied to the D lines, which are connected to the data register D lines. A LOAD H is then generated and applied to the data register L lines. When the load pulse is generated, the data register flip-flops are set or remain clear corresponding to the 1s or 0s on the bus data lines. This loads the data from the bus into the data register.

Just after the LOAD 1 H signal is generated, the TSS and TDR signals are produced to enable the switches and drivers in the X and Y selection matrices. The inhibit (INH) signals are also produced as before. Write currents flow through the selected core locations. The current flowing through the selected cores writes 1s into all cores not inhibited. This causes the core memory location to contain the data stored in the data register. Data from the Unibus has been transferred into the selected core memory location. During a DATO or DATOB operation with the pause flag set, slave sync (SSYN) is generated as soon as the clock is generated. It is reset by the bus master dropping MSYN.

When the write operation is complete, and END H pulse is produced. The END H and WRITE H pulses qualify an AND gate, which clears the M SEL flip-flop and returns the memory control circuits to their original conditions.

2.7.6 Data Out (DATO) Control Circuits

A DATO operation indicates that the master device is to transfer data through the bus into the core memory for storage. In effect, the memory is to write data into the selected core location. It is necessary to clear the selected cores before writing into them; thus, the memory first performs a read cycle and then writes the new data into the location.

The read portion of a DATO is similar to the read portion of a DATI except no RESET 0 L, RESET 1 L, STROBE 0 H, or STROBE 1 H pulses are generated. When the master device asserts MSYN, it causes a M SEL, CLK H, and READ signal to be produced. The CLK H pulse triggers the address flip-flops to produce the enabling signals for the address matrix to establish the proper current return paths. After this sequence occurs, the selected cores receive read current and perform the 1 to 0 transition, thereby clearing the cores. This transition does not enter the data register, because no STROBE 0 H or STROBE 1 H signals are produced to gate them out of the sense amplifiers at the same time as CLK H.

The selected byte is controlled in just the opposite manner. Neither a RESET 0 or 1 L nor STROBE 0 or 1 H is generated, because it is not necessary to restore the byte. A LOAD 0 or 1 H pulse is provided, however, so that the data from the bus can be written into the selected byte location.

At the end of the DATOB operation, the selected byte has new information. The non-selected byte retains its previous data.

2.7.7 DATOB Control Circuits

A DATOB is the same as a DATO operation but a byte, rather than a full word, is transferred. In the case of a DATOB, a RESET 0 or 1 L and STROBE 0 or 1 H signal are produced for the non-selected byte. This process effectively strobes the byte into the data register for restoration during the write operation, because this byte has not been selected to receive new data. A LOAD 0 or 1 H pulse is not provided for the nonselected byte; therefore, any data on the bus have no effect on the nonselected byte.

The LOAD 0 H and LOAD 1 H signals, together with the data on the bus D lines, are applied to the data register, and the flip-flops are set in accordance with the data that is on the bus lines. This completes the read portion of the DATO cycle. All cores are in a zero state and the data that had been on the bus are now stored in the data register. When the READ signal drops (the pause flag is clear), a write cycle is initiated. The X- and Y-matrix enabling levels are supplied along with the inhibit signals to gate the data from the sense amplifier into the selected core location during the write cycle, as previously described.

2.8 READ OPERATION

This paragraph is devoted to an explanation of the read operation. The actual control signals that govern the read cycle are covered in Paragraph 2.7. This section covers read operation only from the standpoint of the core memory itself.

Whenever a word is to be read from memory, a read current passes through the address decoder and related X and Y switches and drivers to the selected core. The read current is a half-select current in both the X and Y windings. Since read current flows in the opposite direction of write current, all cores in the selected word previously set to the 1 state are switched to the 0 state; cores previously set to zero remain unchanged. To make read current opposite to write current, positive drivers and negative switches are used for reading, and negative drivers and positive switches are used for writing. A more detailed explanation of the switches and drivers is given in Paragraph 2.5.

A sense/inhibit termination circuit (referred to as Circuit 1 on logic drawing MM11-E-04) and sense amplifier are provided for each of the 16 mats in the memory. The input to each amplifier comes from a sense/inhibit winding which passes through every core on the associated mat. If, during the read operation, the addressed core in a mat makes the 1 to 0 transition, the flux change induces a current in the sense/inhibit winding of that mat. This current develops a voltage pulse at the input to the amplifier circuit. The input is amplified and (after strobed threshold detection) used to set a flip-flop in the data register when the strobe pulse is applied to the amplifier.

The threshold level (voltage slice) is a factory-set level of -5.2V. Whenever a core makes the 1 to 0 transition, the resultant induced voltage is sufficient to exceed the preset threshold level during strobe time and causes the amplifier to produce an output. Addressed cores which were already in the 0 state induce only a limited amount of current into the sense/inhibit windings when saturated by the full-select current. However, the voltage level produced by this noise is insufficient to reach the threshold level during strobe time and activate the amplifier. Therefore, the data flip-flop for that bit location remains cleared, indicating a logic 0 in that location.

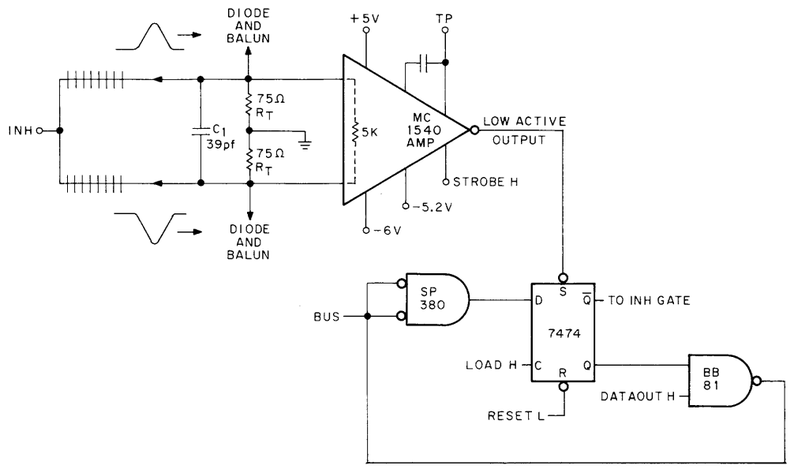
After the sense amplifier outputs have been strobed into the data register, the data register flip-flops are set for each bit position containing a 1. When the control logic generates a data out pulse, the high outputs (1s) from all of the flip-flops that are set in the data register are gated through drivers onto the data bus for transfer to the processor or master device. Note that the bus driver output is low for a logical 1 because the Unibus employs negative logic. Any 0 output from the data register is not gated, and a logical 0 remains on the bus for those bit positions.

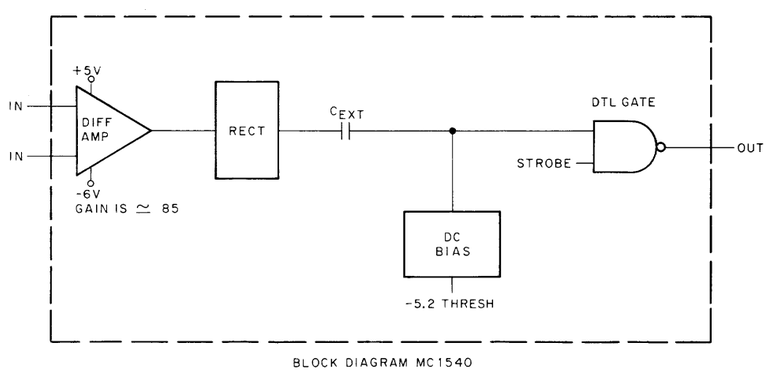
This type of readout destroys the contents of the addressed memory location (by switching all cores to zero); thus, the data stored in the data register must be put back into the cores to restore the memory location to its original contents. This is accomplished by immediately following the read cycle with a write (restore) cycle. Note, however, that this write cycle is delayed whenever a DATIP operation is performed, because it is not necessary to restore the contents of the memory. In effect, the memory pauses and waits for new data to be written into the core location. The restore cycle is the same as a normal write cycle as described in Paragraph 2.9.

Figure 2-16 is a circuit schematic of the sense amplifier detector circuit. At sense time, the effect of the inhibit drivers, isolation diodes, and Balun transformer can be ignored due to the high impedance of these components. The voltage signal is developed on the sense line and propagates through a twisted pair of wires to the sense amplifier module. The input to the MC 1540 Module is an impedance matching network used to terminate the sense line. The MC 1540 amplifies the difference signal approximately 85 times and rectifies it. The signal is ac-coupled through an external capacitor and superimposed upon a dc bias which is controlled by the threshold input. During strobe time, if the dc bias plus the coupled core signal exceeds the DTL gate threshold, its output goes to ground. This sets the 7474 flip-flop by means of a direct set gate. At the start of each read cycle, the 7474 flip-flop is reset by means of the direct reset gate. In a DATO operation, the data is shifted from the bus through the SP 380 inverter to the D input of the 7474 flip-flop and clocked into the flip-flop by a LOAD H pulse.

2.9 WRITE OPERATION

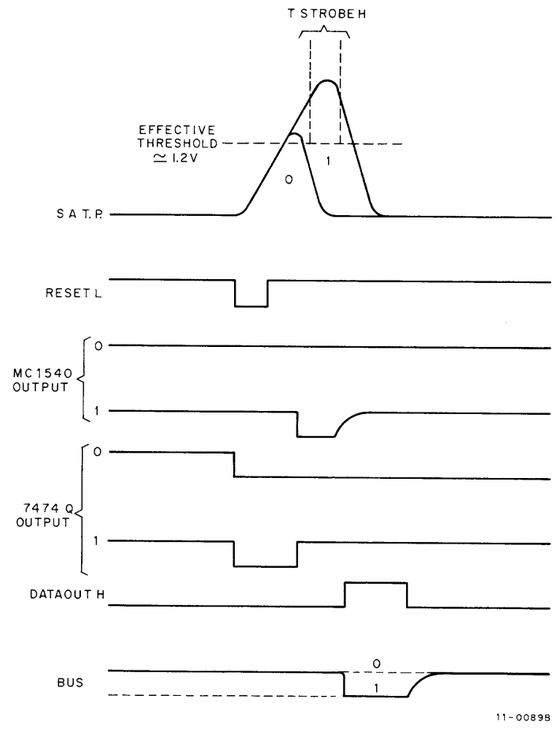
During a DATO operation, the word to be written into core memory is loaded into the data register flip-flops from the data lines when a load pulse is applied to each of the flip-flops in the register. Whenever the input from the data line is a 1, the load pulse (high) and the binary 1 set the flip-flop to the 1 state. If the input from the data line is 0, then the flip-flop remains cleared. The resultant states of the 16 flip-flops represent the word to be written into memory. During a write/restore cycle, the contents of the data register (from reading) is written.





BLOCK DIAGRAM MC1540

11-0089A



11-0089B

Figure 2-16 Sense Amplifier Detector Circuit

When the write cycle begins, an inhibit signal is applied to an inhibit driver (AND gate) for each line. If the gate is qualified (flip-flop set to 0), the gate enables an inhibit pulse. This inhibit pulse causes a current path through the core opposing the Y write current to prevent a core from being set into a 1 state. If the flip-flop is set, representing a 1, the gate is not qualified, no inhibit signal is generated, and the write currents set the selected core to the 1 state. Thus, the data word stored in the register is written into the appropriate core memory location.

Figure 2-17 is a schematic of the inhibit driver. When it is desired to write a zero and the inhibit current (I_{inh}) goes high, the 74H40 gate turns on and its output goes to ground. Current i_1 is determined by resistor R1 and the reflected base-emitter voltage (V_{be}) of output transistor Q1. Current i_2 equals i_1 and turns on transistor Q1. When Q1 turns on, current flows from ground, through the Balun transformer (which equalizes the two half currents), through the isolation diodes and the sense/inhibit winding, to the common inhibit terminal. Current then flows through resistor R2 and transistor Q1 to -15V.

$$I_{inh} = \frac{15V - V_{ce\ sat\ Q} - V_{be\ diodes}}{16.9 + mat^{\Omega}\ (\approx 2.0)}$$

$$= \frac{15 - 0.8 - 1.2}{16.9 + 2.0} = 690\ mA$$

Each winding sees nearly 345 mA. Capacitor C2 speeds up the rise time of the current. At turn-off time, the inductance of the stack winding would normally push the voltage at the switch (Q1) quite positive; however, the diode at the collector of Q1 clamps this voltage to ground. Capacitor C1 helps turn on Q1 faster and allows the 74H40 gate to provide reverse current to turn off Q1.

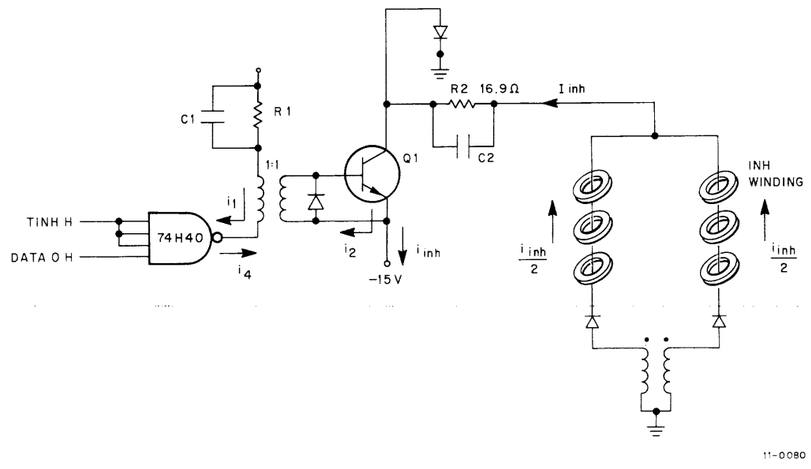


Figure 2-17 Inhibit Driver

CHAPTER 3
MAINTENANCE

3.1 INTRODUCTION

This chapter contains maintenance and adjustment procedures for the MM11-E Core Memory. Adjustment procedures are covered in Paragraph 3.2, and maintenance is covered in Paragraph 3.3.

3.2 ADJUSTMENTS

There are three adjustments that can be performed on the core memory: voltage reference (V REF), voltage slice (V SLICE), and strobe delay (STROBE DEL). It is usually not necessary to make any of these adjustments unless a module has been replaced. If, however, the memory is not functioning properly, check these adjustments before attempting to troubleshoot the memory.

The purpose of each of the three adjustments is given in Table 3-1. Specific adjustment procedures are given in subsequent paragraphs.

Table 3-1
Core Memory Adjustments

Adjustment	Location	Pin	Purpose
V REF	Trimpot on current generator Module G225	E1U2	Sets reference voltage for X-Y current.
V SLICE	Trimpot on V levels Module G103	D2F1	Sets threshold level of sense amplifier.
STROBE DELAY	STROBE DEL trimpot on control and timing Module M729	E1K1 E2S1	Sets delay time of strobe pulse used during read cycle.

3.2.1 Equipment Required

The following test equipments are used when checking or adjusting the MM11-E Core Memory.

a. Tektronix 453 or 547 oscilloscope with dual trace plug in, voltage probes

b. Honeywell 333R Digital Voltmeter (or equivalent 0.5% DVM)

NOTE
Although the digital voltmeter is not mandatory, it can be helpful when performing the procedures in this section.

3.2.2 Initial Procedures

Before attempting to check or adjust the core memory, perform the following steps:

NOTE
All tests and adjustments must be performed in an ambient temperature range of 20° C to 30° C (68° F to 86° F).

Step	Procedure
1.	Verify that all modules shown in the MUL print MM11-E-06 are properly installed in the backboard.
2.	Visually check for broken wires, connectors, modules, or other obvious defects.
3.	Verify that power buses are not shorted together.
4.	Turn primary power on and make certain that both -15V and +5V (±5%) power is present.
5.	Start the system. Memory should now cycle without errors. If not, check adjustments in Paragraphs 3.2.3, 3.2.4, and 3.2.5. If memory still does not function properly, a malfunction is indicated.

3.2.3 Voltage Reference (V REF) Adjustment

The voltage reference sets the amplitude of the X-Y current and is measured at pin E1U2 of the current generator Module G225. This voltage should be in the range of +0.70V to +1.90V at an ambient temperature of 30° C (86° F). The voltage fluctuates with temperature variations, going more positive as the temperature increases. If the reference voltage must be reset, perform the following adjustment procedure:

Step	Procedure
1.	Cycle the memory using a "worst-case" patterns program.
2.	Use the V REF trimpot on the current generator module to vary the reference voltage to the points where memory fails (both high voltage and low voltage). The system must have a margin of at least 0.80V, i.e., there must be an interval 0.80V wide in which the system functions properly.
3.	Set the reference voltage (V REF) at a point midway between the worst-case limits of operation. To effect this condition, adjust the trimpot on the current generator for a reference voltage that is midway between the lowest voltage causing the memory to fail at the high end and the highest voltage causing the memory to fail at the low end.

3.2.4 Voltage Slice (V SLICE) Adjustment

The V SLICE (voltage threshold) adjustment must be performed whenever a G103 Discharge Circuit Module is replaced. The adjustment procedure is as follows:

Step	Procedure
1.	Measure the slice voltage (V SLICE) at pin D2F1 of the sense amplifier with respect to ground.
2.	Verify that the measured voltage is -5.3V (±0.2V).
3.	If the voltage is not within the above tolerance, adjust V SLICE trimpot on the G103 Module until the voltage is within the specified tolerance.

3.2.5 Strobe (STROBE DEL) Adjustment

The STROBE DEL adjustment should be checked whenever an M729 Module (Control and Timing) or a G225 Module (current generator module) is replaced. If necessary, the strobe adjustment should be reset.

NOTE

The adjustment of the STROBE DEL trimpot on the M729 Module is critical. The setting should only be changed when absolutely necessary.

Figure 3-1 illustrates the proper setting of the strobe pulse. If required, adjust the STROBE DEL trimpot so that T STROBE is set to 210 ns ±5 ns.

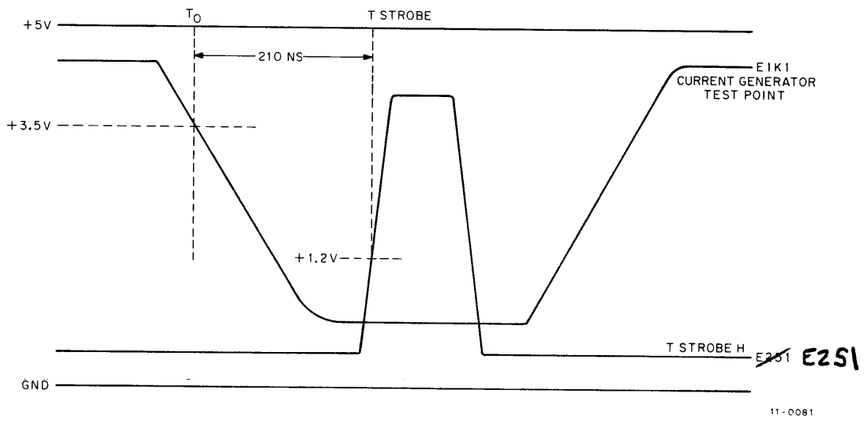


Figure 3-1 Strobe Pulse Waveform

3.3 MAINTENANCE

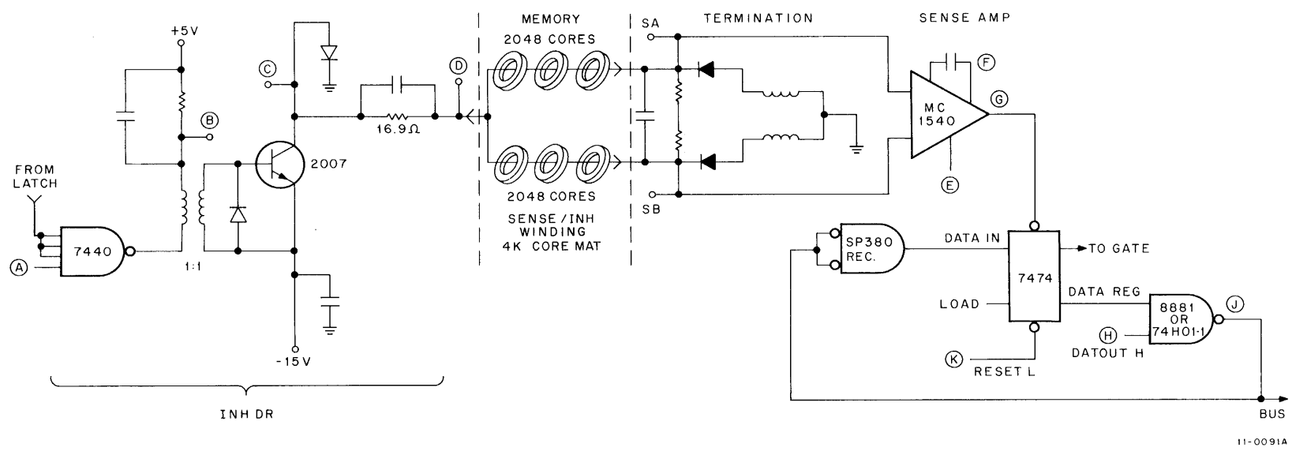
The basic maintenance philosophy of PDP-11 manuals presents information on normal system operation. The user can then utilize this information to analyze trouble symptoms and extrapolate necessary corrective action. This paragraph provides additional maintenance information to aid the user in isolating and correcting malfunctions.

Figure 3-2 illustrates the sense/inhibit waveforms; Figure 3-3 illustrates drive waveforms. Both figures include schematics to indicate the points in the circuit where the waveforms occur. In addition to the normal waveforms, dotted lines are used to indicate the waveform that appears if a component is faulty.

Table 3-2 is a troubleshooting chart that indicates possible malfunctions, probable causes, and corrective actions.

Table 3-2
MM11-E Troubleshooting Guide

Symptom	Affects	Possible Cause(s)	Corrective Action
Picks up bits	All bits	X-Y current too high	Check V REF and reset per set-up procedure.
	All bits	Strobe occurs too early	Reset STROBE DEL to 210 ns on M729 Module.
	All bits	-15V input low	Reset or repair H720 Power Supply.
	One bit	Inhibit driver inoperative; inhibit winding open	Repair G102 Module.
	All bits	Threshold too low (less than -5.2V)	Reset V SLICE to -5.2V on G103 Module.
	Some bits in one byte	Sense amplifier reset; inoperative for that byte	Repair M729 Module.
	8 or 16 bits	TINH H inoperative	Check M729, G225 Module
	All bits at high temp.	Stack thermistor or resistor	Check components and wiring to G225 Module.
Drops bits	All bits	X-Y current too low	Reset V REF or repair G225 Module.
	All bits	Strobe too early or too late	Reset STROBE DEL on M729 Module.
	All bits	Threshold too high	Reset V SLICE on G103 Module.
	All bits, 64 locations	Open line in memory	Ring out stack (read or write)
	All bits, 8 locations	Bad switch or driver	Troubleshoot and repair G226 module.
	One bit, all words	Bad sense line or sense chain (bus receiver, latch, sense amplifier, or bus driver)	Troubleshoot and repair G102 Module.
	Some bits, one byte	STROBE inoperative, LOAD inoperative for that byte	Troubleshoot and repair M729 Module.
	All bits at low temp.	Stack thermistor or resistor	Check components and wiring to G225 Module.
No response to MSYN L		No device select	Check M109 Module jumpers and gates.
		MSEL not reset on previous cycle	Check M729 Module circuits.
		SSYN not reset on previous cycle	Check M729 Module circuits.
		SSYN not setting	Check M729 Module circuits.
Memory always performs a DATIP	All bits	PROTECT L input to M729 Module grounded	Check and repair.



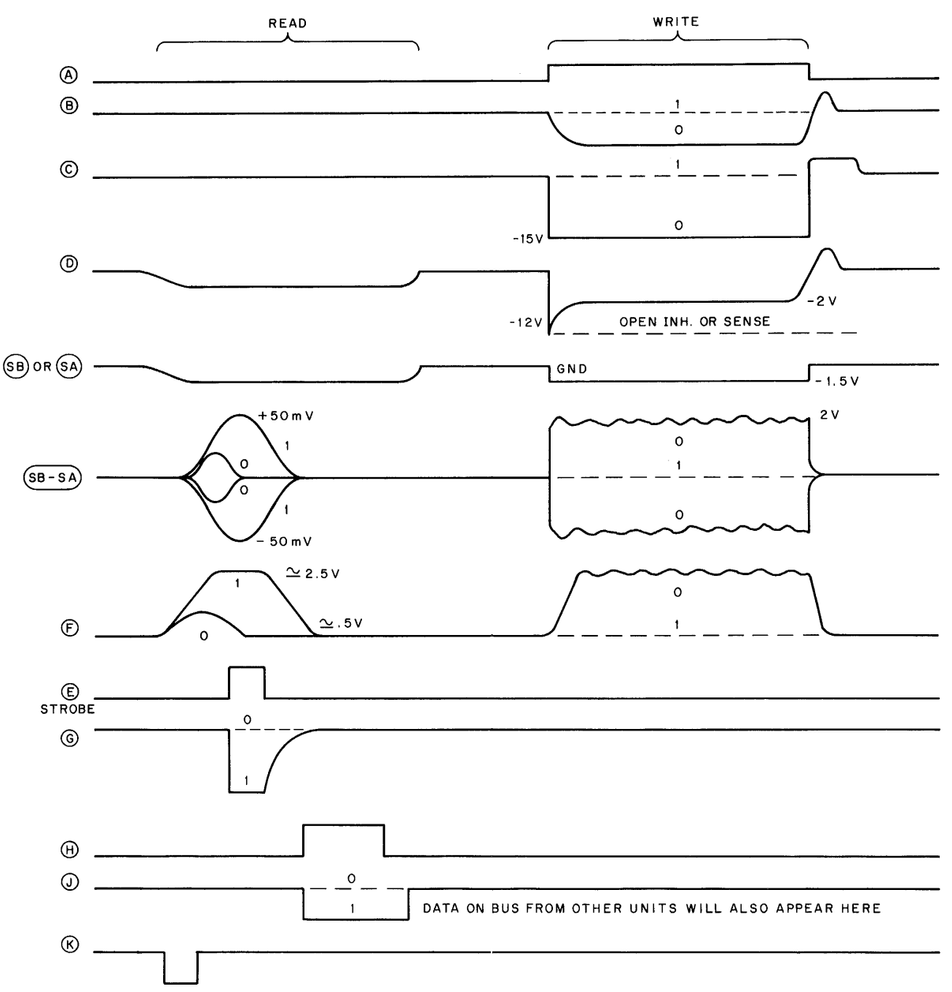


Figure 3-2 MM11-E Sense/Inhibit Waveforms

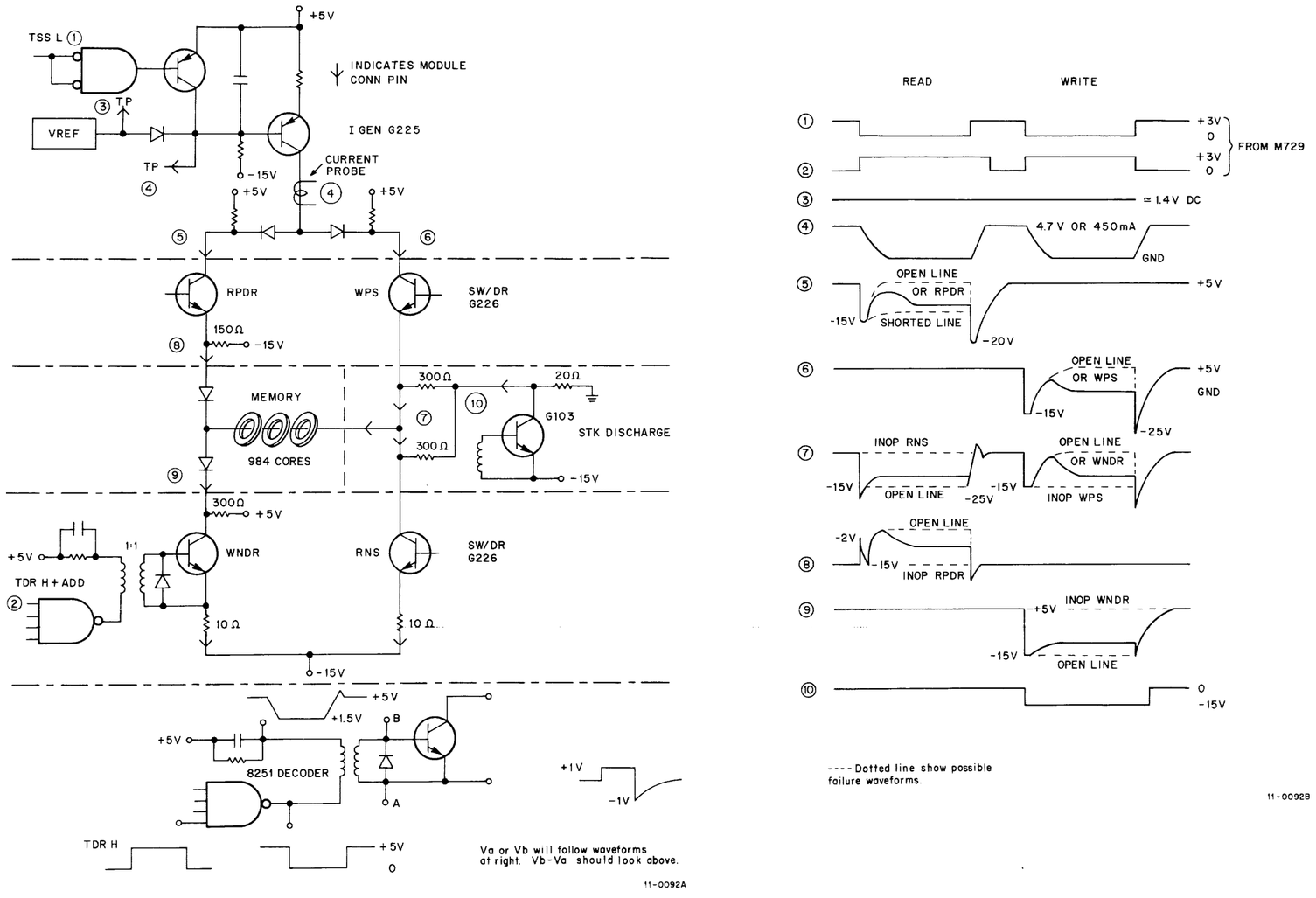
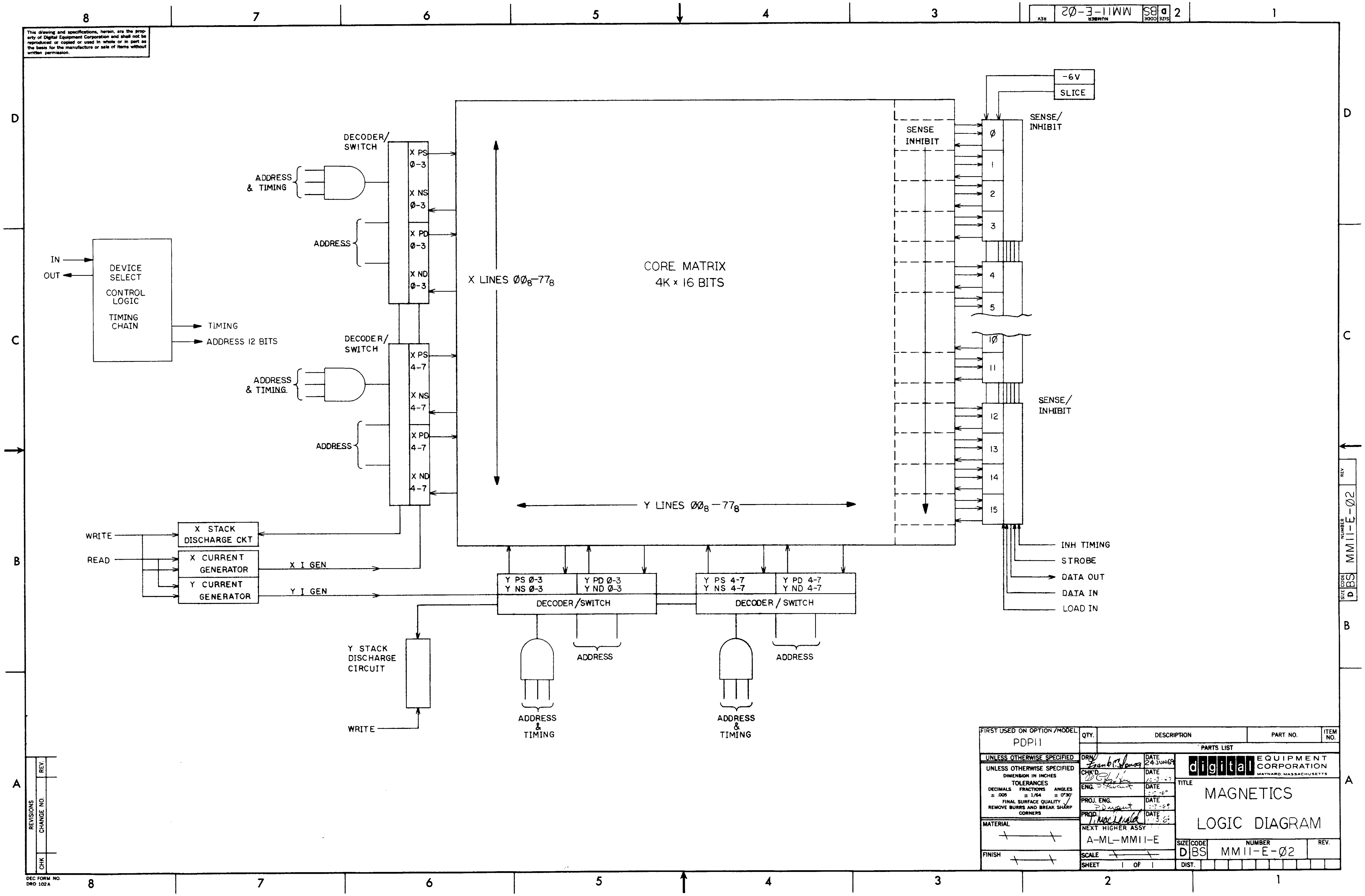


Figure 3-3 Drive Waveforms

CHAPTER 4
MM11–E ENGINEERING DRAWINGS

Table 4-1
MM11-E Engineering Drawing List

Dwg.	Title	Rev.	Pg.
D-BS-MM11-E-02	Magnetics, Logic Diagram		4-2
D-BS-MM11-E-03	Core Memory Stack (X Drive) (2 sheets)	A	4-3
D-BS-MM11-E-04	Core Memory Sense & Inhibit (4 sheets)	B	4-5
D-BS-MM11-E-05	Control & Timing (2 sheets)	A	4-9
D-IC-MM11-E-09	I/O Connectors		4-11
D-MU-MM11-E-06	Module Utilization	C	4-12
D-TD-MM11-E-08	Timing & Flow	A	4-13
C-CS-G103-0-1	Memory Levels and Gates, G103	D	4-14
C-CS-G616-0-1	Planar Stack Board 1, G616	C	4-14
D-CS-G226-0-1	X-Y Decoder Switch, G226	C	4-15
D-CS-G102-0-1	Sense Inhibit-Card, G102	C	4-16
B-CS-M109-0-1	Device Select Module, M109		4-17
D-CS-M729-0-1	MM11-E Control Logic, M729	A	4-18
C-CS-G225-0-1	X & Y Current Generator	B	4-19



DECODER/ SWITCH
ADDRESS & TIMING
X PS Ø-3
X NS Ø-3
ADDRESS
X PD Ø-3
X ND Ø-3
IN
OUT
DEVICE SELECT
CONTROL LOGIC
TIMING CHAIN
TIMING
ADDRESS 12 BITS
DECODER/ SWITCH
X PS 4-7
X NS 4-7
X PD 4-7
X ND 4-7
CORE MATRIX
4K × 16 BITS
X LINES $ØØ_8$–77_8
Y LINES $ØØ_8$ – 77_8
SENSE INHIBIT
-6V
SLICE
SENSE/ INHIBIT
Ø
1
2
3
4
5
1Ø
11
12
13
14
15
INH TIMING
STROBE
DATA OUT
DATA IN
LOAD IN
WRITE
READ
X STACK DISCHARGE CKT
X CURRENT GENERATOR
Y CURRENT GENERATOR
X I GEN
Y I GEN
Y PS Ø-3
Y NS Ø-3
Y PD Ø-3
Y ND Ø-3
DECODER/SWITCH
Y PS 4-7
Y NS 4-7
Y PD 4-7
Y ND 4-7
Y STACK DISCHARGE CIRCUIT
WRITE
ADDRESS & TIMING
FIRST USED ON OPTION/MODEL PDP11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES
MATERIAL
FINISH
NEXT HIGHER ASSY A-ML-MM11-E
SCALE
SHEET 1 OF 1
QTY. DESCRIPTION PART NO. ITEM NO.
PARTS LIST
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE MAGNETICS LOGIC DIAGRAM
SIZE D CODE BS NUMBER MM11-E-Ø2 REV.
DEC FORM NO. DRD 102A

THERMISTOR

G616 FØ4 J1 M2 +5V A1 A2 F1

E1 G225 EØ1 D1 TSSL

B1 CURRENT GENERATOR G225 EØ1 U2 V REF

F2 XWC G

N1

CURRENT LOOPS

E2 XRC G

L1

K1

VOLTAGE WAVEFORM OF CURRENT

T INH H E1 X DISCHARGE CIRCUIT GIØ3 FØ1 C1 X DISCH

DECODER/SWITCH G226 CØ2

TSS H P1
+3V P2
A12 L K1
G1Ø3 FØ1 K2 U2 XS(Ø-3)
A1Ø H U1
A11 H T2

XNSØ XPSØ XNS1 XPS1 XNS2 XPS2 XNS3 XPS3

G616 CØ4 D1 E1 H1 J1 U1 S1 R1 P1

DECODER/SWITCH G226 FØ2

TSS H (P1) (P2)
+3V R1
A12 H
G1Ø3 FØ1 R2 U2 XS(4-7)
A1Ø H U1
A11 H T2

XNS4 XPS4 XNS5 XPS5 XNS6 XPS6 XNS7 XPS7

G616 FØ4 P1 R1 S1 U1

Ø0 Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7

G616 CØ4 R1 K2 E2 S2 R2 K1 F1 T2

XPDØ XNDØ XPD1 XND1 XPD2 XND2 XPD3 XND3

J2 K2 E1 L2 F2 M2 H1 N2

H2 D1 F1 C1 DECODER/SWITCH G226 CØ2 Ø 1 2 3

E2 R1 A1 AØ7 H AØ8 H

STACK G 616 FØ4 D1 R2 N2 F2 D2 U2 P2 E2

XPD4 XND4 XPD5 XND5 XPD6 XND6 XPD7 XND7

J2 K2 E1 L2 F2 M2 H1 N2

H2 D1 F1 C1 DECODER/SWITCH G226 FØ2 4 5 6 7

E2 B1 A1 AØ7 H AØ8 H

+5V
-15V
READ H

TDR H V1
+3V (P2)
~AØ9 H F2
GIØ3 FØ1 H1 XDR(Ø-3)

TDR H (V1) (P2)
+3V
AØ9 H M1
GIØ3 FØ1 L1 XDR(4-7)

REVISIONS	REV.	CHANGE NO	CHK

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN Frank C. Lomma DATE 16 JUN69
CHK'D DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY A-ML-MM11-E
SCALE
SHEET 1 OF 2

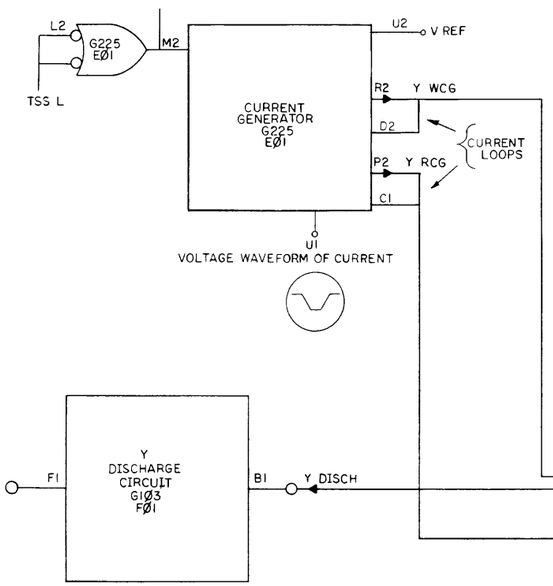
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

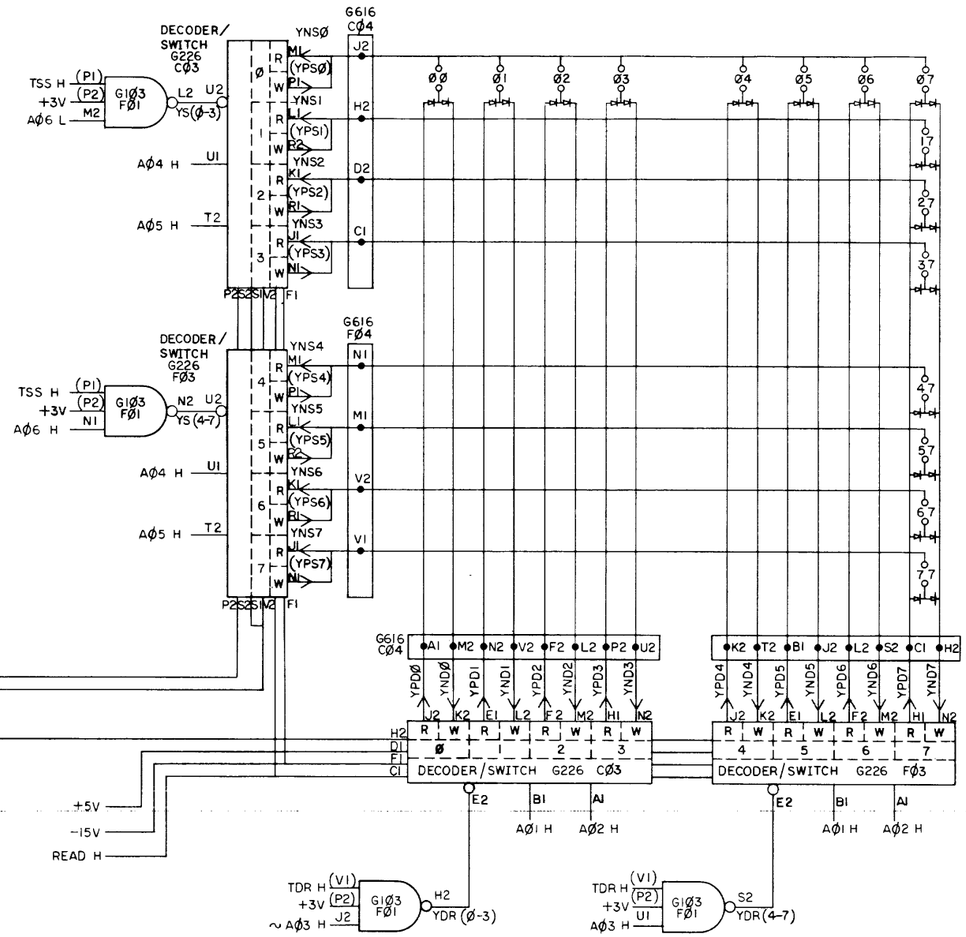
TITLE CORE, MEMORY STACK (X DRIVE)

SIZE	CODE	NUMBER	REV.
D	BS	MM11-E-Ø3	

DIST.

DEC FORM NO DRD 102A





FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
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UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN	Frank C. Sloma	DATE 16 JUN67
CHK'D	[illegible]	DATE 11-7-69
ENG	[illegible]	DATE 10-21-69
PROJ. ENG.	[illegible]	DATE 10-21-69
PROG	T. MacDonald	DATE 11/3/69

NEXT HIGHER ASSY
A-ML-MMII-E

SCALE

SHEET 2 OF 2

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

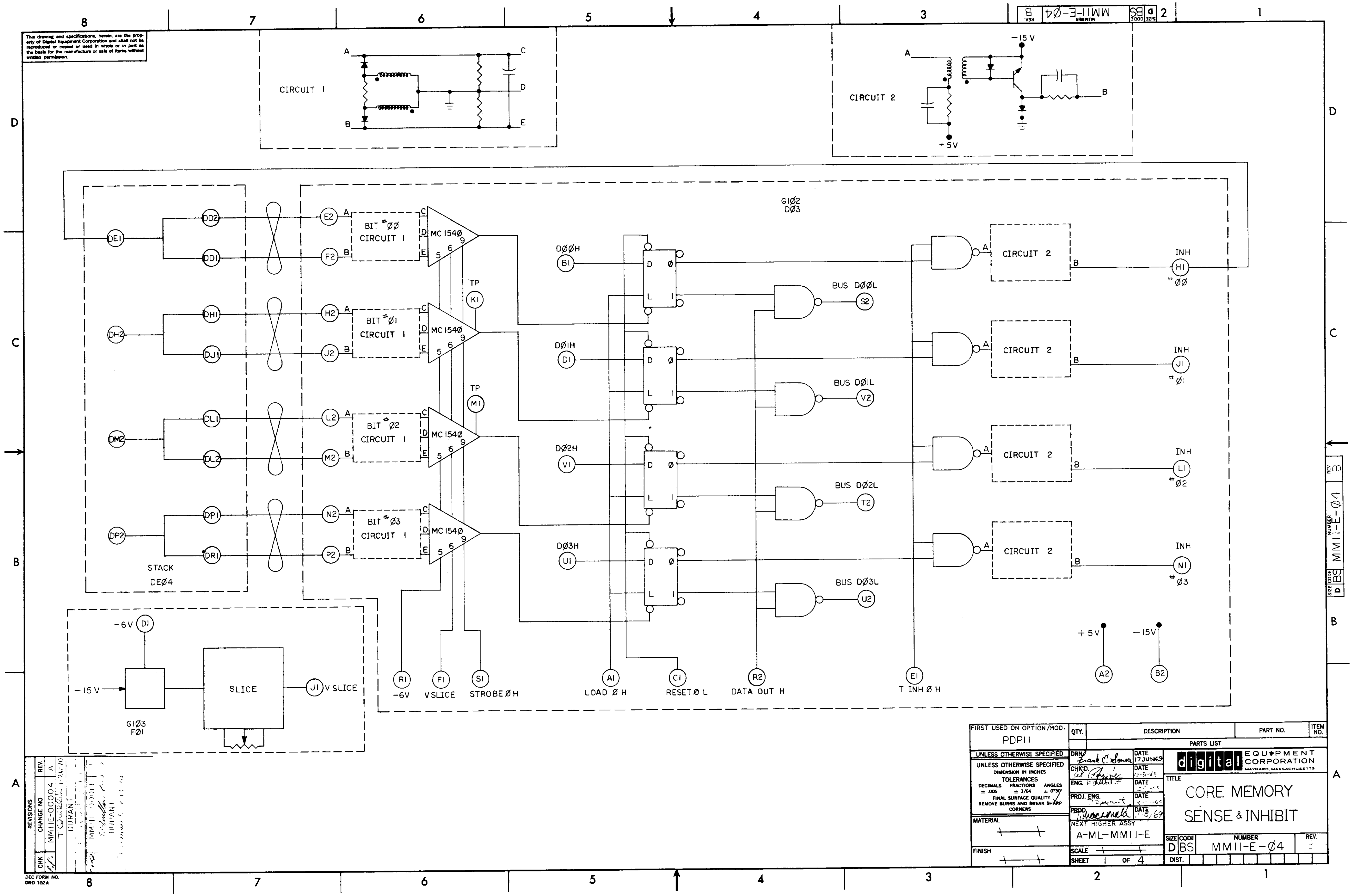
TITLE
CORE,
MEMORY STACK
(Y DRIVE)

SIZE D CODE BS NUMBER MMII-E-Ø3 REV A

DIST.

REVISIONS
REV.
CHANGE NO.
CHK

DEC FORM NO. DRD 102A


This drawing and specifications, herein, are the property of Digital Equipment Corporation and shall not be reproduced or copied or used in whole or in part as the basis for the manufacture or sale of items without written permission.
CIRCUIT 1
CIRCUIT 2
-15 V
+5 V
STACK
DE04
BIT #00 CIRCUIT 1
BIT #01 CIRCUIT 1
BIT #02 CIRCUIT 1
BIT #03 CIRCUIT 1
MC 1540
TP
G102
D03
D00H
D01H
D02H
D03H
BUS D00L
BUS D01L
BUS D02L
BUS D03L
INH
-6V
VSLICE
STROBE 0 H
LOAD 0 H
RESET 0 L
DATA OUT H
T INH 0 H
-15 V
SLICE
V SLICE
G103
F01
FIRST USED ON OPTION/MOD.
PDP11
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
MATERIAL
FINISH
QTY.
DESCRIPTION
PART NO.
ITEM NO.
PARTS LIST
DRN
CHK'D
ENG.
PROJ. ENG.
PROD.
DATE
17JUN69
NEXT HIGHER ASSY
A-ML-MM11-E
SCALE
SHEET 1 OF 4
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
TITLE
CORE MEMORY
SENSE & INHIBIT
SIZE D
CODE BS
NUMBER MM11-E-04
REV.
DIST.
REVISIONS
CHANGE NO.
MM11E-00004
DEC FORM NO. DRD 102A

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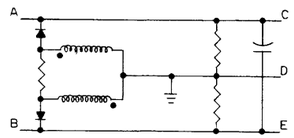

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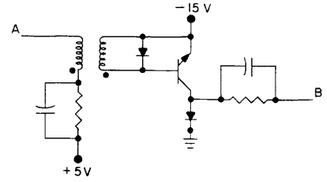

GIØ2
DØ2

DEI
DFI
DF2
E2
F2
BIT "Ø4 CIRCUIT 1
MC 1540
TP KI
DØ4H BI
BUS DØ4L S2
DKI
DK2
DJ2
H2
J2
BIT "Ø5 CIRCUIT 1
MC 1540
TP MI
DØ5H DI
BUS DØ5L V2
DMI
DN2
DNI
L2
M2
BIT "Ø6 CIRCUIT 1
MC 1540
DØ6H VI
BUS DØ6L T2
DSI
DT2
DS2
N2
P2
BIT "Ø7 CIRCUIT 1
MC 1540
DØ7H UI
BUS DØ7L U2
STACK DEØ4
CIRCUIT 2
INH HI Ø4
CIRCUIT 2
INH JI Ø5
CIRCUIT 2
INH LI Ø6
CIRCUIT 2
INH NI Ø7
+5V
−15V
A2
B2
RI −6V
FI V SLICE
SI STROBE Ø H
AI LOAD Ø H
CI RESET Ø L
R2 DATA OUT H
EI TINH Ø H

REVISIONS	REV.	CHANGE NO.	CHK

FIRST USED ON OPTION/MOD.	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
± .005 ± 1/64 ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN Frank C. Jones DATE 17JUN69
CHK'D DATE
ENG. DATE
PROJ. ENG. DATE
PROG. DATE
NEXT HIGHER ASSY A-ML-MMII-E
SCALE
SHEET 2 OF 4

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
CORE MEMORY
SENSE & INHIBIT

SIZE D | CODE BS | NUMBER MMII-E-Ø4 | REV

DIST.

DEC FORM NO. DRD 102A

REV E | NUMBER MMII-E-Ø4 | SIZE/CODE D BS

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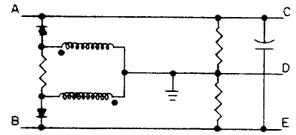

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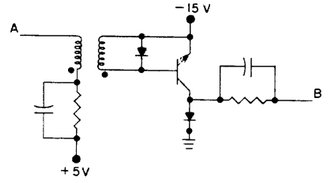


GIØ2
EØ3

EC1, EA1, EB1, E2, F2 — BIT #Ø8 CIRCUIT 1 — MC 154Ø 9 — TP K1
EH1, EE1, EF1, H2, J2 — BIT #Ø9 CIRCUIT 1 — MC 154Ø 9 — TP M1
EL1, EK2, EK1, L2, M2 — BIT #1Ø CIRCUIT 1 — MC 154Ø 9
ER1, EP2, EP1, N2, P2 — BIT #11 CIRCUIT 1 — MC 154Ø 9

STACK DEØ4

DØ8H B1 — D Ø / L 1 — BUS DØ8L S2
DØ9H D1 — D Ø / L 1 — BUS DØ9L V2
DIØH V1 — D Ø / L 1 — BUS DIØL T2
DI1H U1 — D Ø / L 1 — BUS DI1L U2

CIRCUIT 2 → INH H1 #Ø8
CIRCUIT 2 → INH J1 #Ø9
CIRCUIT 2 → INH L1 #1Ø
CIRCUIT 2 → INH N1 #11

+5V A2
-15V B2

R1 -6V
F1 VSLICE
S1 STROBE IH
A1 LOAD I H
C1 RESET I L
R2 DATA OUT H
E1 T INH I H

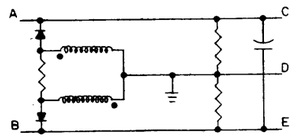
REVISIONS	REV.	CHANGE NO.	CHK

FIRST USED ON OPTION/MOD. PDP11	QTY.	DESCRIPTION	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED		PARTS LIST	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	DRN. Frank C. Lowe	DATE 17JUN69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
	CHK'D	DATE	
	ENG.	DATE	
	PROJ. ENG.	DATE	
	PROD.	DATE 9/16/69	
MATERIAL	NEXT HIGHER ASSY A-ML-MM11-E		TITLE CORE MEMORY SENSE & INHIBIT
FINISH	SCALE		SIZE D CODE BS NUMBER MM11-E-Ø4 REV B
	SHEET 3 OF 4		DIST.

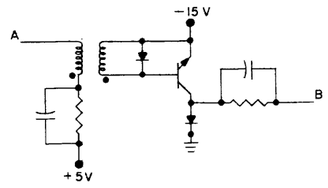
DEC FORM NO. DRD 102A

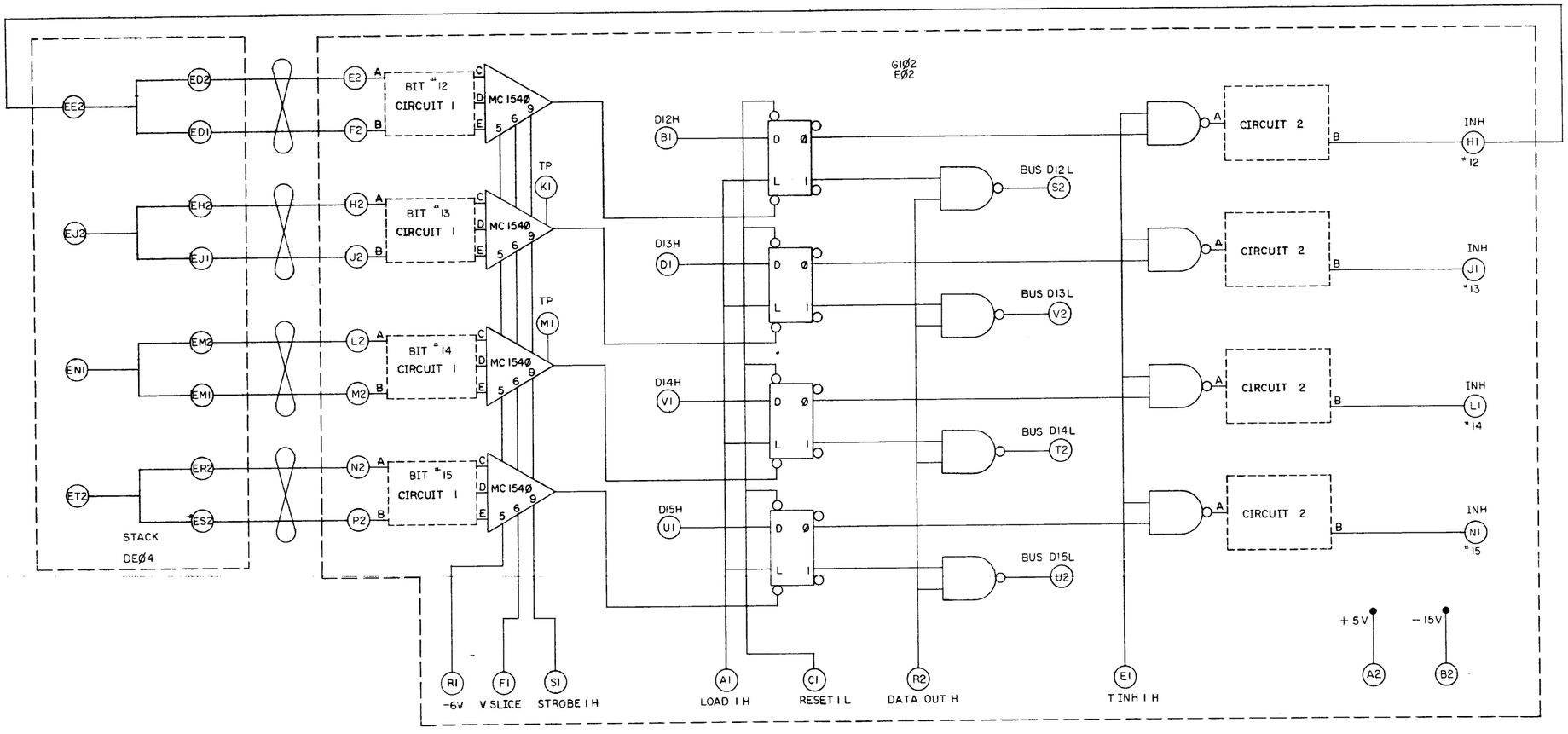
SIZE D CODE BS NUMBER MM11-E-Ø4 REV B

CIRCUIT 1



CIRCUIT 2





FIRST USED ON OPTION/MOD.	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN	Frank C. Lowe	DATE 17JUN69
CHK'D		DATE
ENG.		DATE
PROJ. ENG.		DATE
PROD.		DATE 7/31/69

NEXT HIGHER ASSY
A-ML-MM11-E

SCALE

SHEET 4 OF 4

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

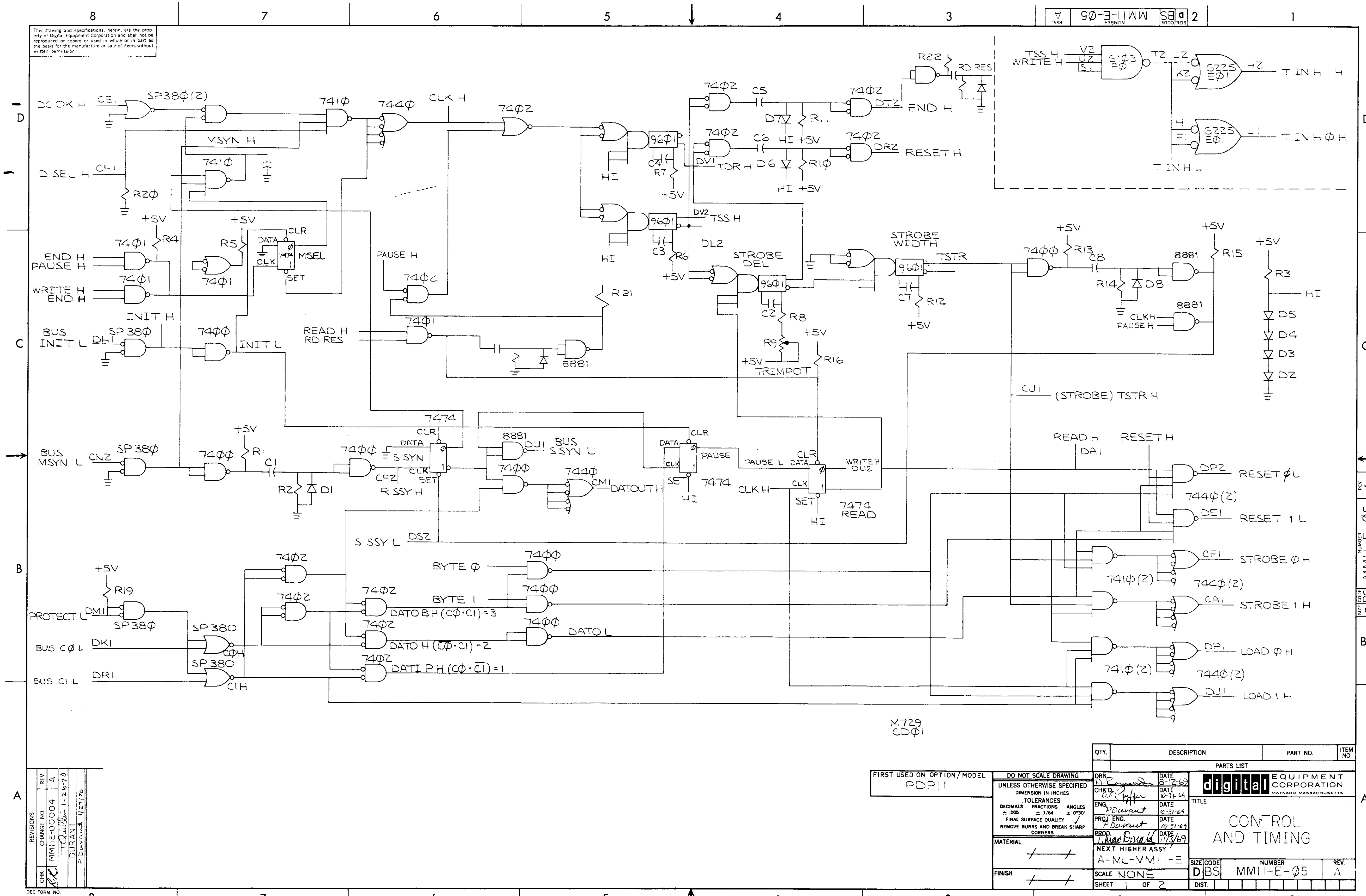
TITLE
CORE MEMORY
SENSE & INHIBIT

SIZE	CODE	NUMBER	REV.
D	BS	MM11-E-Ø4	E

DIST.

REVISIONS	REV.
CHANGE NO.	
CHK	

DEC FORM NO. DRD 102A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DC OK H
D SEL H
END H
PAUSE H
WRITE H
END H
BUS INIT L
INIT H
INIT L
MSYN H
MSEL
PAUSE H
READ H
RD RES
CLK H
TSS H
TDR H
STROBE DEL
STROBE WIDTH
TSTR
END H
RESET H
T IN H I H
T IN H Ø H
T IN H L
TRIMPOT
(STROBE) TSTR H
CLKH
PAUSE H
BUS MSYN L
BUS SSYN L
S SYN
R SSY H
S SSY L
DATOUT H
PAUSE L
WRITE H
CLK H
7474 READ
READ H
RESET H
RESET Ø L
RESET 1 L
STROBE Ø H
STROBE 1 H
LOAD Ø H
LOAD 1 H
BYTE Ø
BYTE 1
DATO B H (CØ·C1) = 3
DATO H (CØ·C1) = 2
DATI P H (CØ·C̄1) = 1
DATO L
PROTECT L
BUS CØ L
BUS C1 L
M729
CDØ1
FIRST USED ON OPTION/MODEL
PDP11
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
MATERIAL
FINISH
PARTS LIST
QTY. DESCRIPTION PART NO. ITEM NO.
DRN. DATE 8-13-69
CHK'D DATE 10-31-69
ENG. P. Durant DATE 10-31-69
PROJ. ENG. P. Durant DATE 10-31-69
PROD. DATE 11/3/69
NEXT HIGHER ASSY A-ML-MM11-E
SCALE NONE
SHEET 1 OF 2
digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
TITLE CONTROL AND TIMING
SIZE D CODE BS NUMBER MM11-E-Ø5 REV. A
REVISIONS
CHANGE NO. MM11E-00004
DEC FORM NO DRD 100

SP38Ø (13) 7474 (13)

BUS A2 L — CD1 — CJ2 — BAI2 H
CLCK H — CH2 — BAI2 L
BUS AI1 L — CD2 — CE2 — BAI1 H
BUS AIØ L — CL1 — CM2 — BAIØ H
BUS AØ9 L — CK1 — CL2 — BAØ9 H
CK2 — BAØ9 L
BUS AØ8 L — CS1 — CR2 — BAØ8 H
BUS AØ7 L — CR1 — CP2 — BAØ7 H
BUS AØ6 L — DD1 — CS2 — BAØ6 H
CT2 — BAØ6 L
BUS AØ5 L — DF1 — CU2 — BAØ5 H
BUS AØ4 L — DN1 — DF2 — BAØ4 H
BUS AØ3 L — DL1 — DE2 — BAØ3 H
DD2 — BAØ3 L
BUS AØ2 L — DM2 — DK2 — BAØ2 H
BUS AØ1 L — DS1 — DJ2 — BAØ1 H
BUS AØØ L — DN2 — BYTE 1
BYTE Ø
MSYN H

+5V — R18 — R17 — DH2 — LOG 1 L

M729 CDØ1

SP38Ø (11)

BUS DØØ L — R1 — P1 — DØØ H
BUS DØ1 L — M2 — L1 — DØ1 H
BUS DØ2 L — N1 — M1 — DØ2 H
BUS DØ3 L — S1 — R2 — DØ3 H
BUS DØ4 L — P2 — N2 — DØ4 H
BUS DØ5 L — H2 — F1 — DØ5 H
BUS DØ6 L — J1 — H1 — DØ6 H
BUS DØ7 L — K1 — K2 — DØ7 H
BUS DØ8 L — L2 — J2 — DØ8 H
BUS DØ9 L — D1 — A1 — DØ9 H
BUS DIØ L — C1 — B1 — DIØ H

SP38Ø (4)

BUS DI5 L — CC1 — CB1 — DI5 H
BUS DI4 L — CP1 — CN1 — DI4 H
BUS DI3 L — CU1 — CV1 — DI3 H
TSS H — DC1 — DB1 — TSS L

BUS AI7 L — V1 — Ø
BUS AI6 L — U1 — Ø
BUS AI5 L — U2 — Ø
BUS AI4 L — T2 — Ø
BUS AI3 L — V2 — Ø
C

JUMPERS

+5V — R1 — 1/W, 5P — S2 — D SEL H

SP 314A

M1Ø9 BØ2

BUS DI1 L — E1 — E2 — DI1 H
BUS DI2 L — F2 — D2 — DI2 H

FIRST USED ON OPTION/MODEL: PDP11	QTY.	DESCRIPTION	PART NO. / ITEM NO.
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL —
FINISH —

DRN. P. Hammond	DATE 8-2-69	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. [illegible]	DATE 10-31-69	
ENG. P.D Wescott	DATE 10-31-69	
PROJ. ENG. P. Divecchi	DATE 10-31-69	
PROD. Mike Dodd	DATE 11/3/69	

NEXT HIGHER ASSY: A-ML-MM11-E
SCALE NONE
SHEET 2 OF 2

TITLE: CONTROL AND TIMING

SIZE D | CODE BS | NUMBER MM11-E-Ø5 | REV. A
DIST.

REVISIONS | REV. | CHANGE NO. | CHK.

DEC FORM NO DRD 102A

NUMBER MM11-E-Ø5 REV A | SIZE D | CODE BS | 3001

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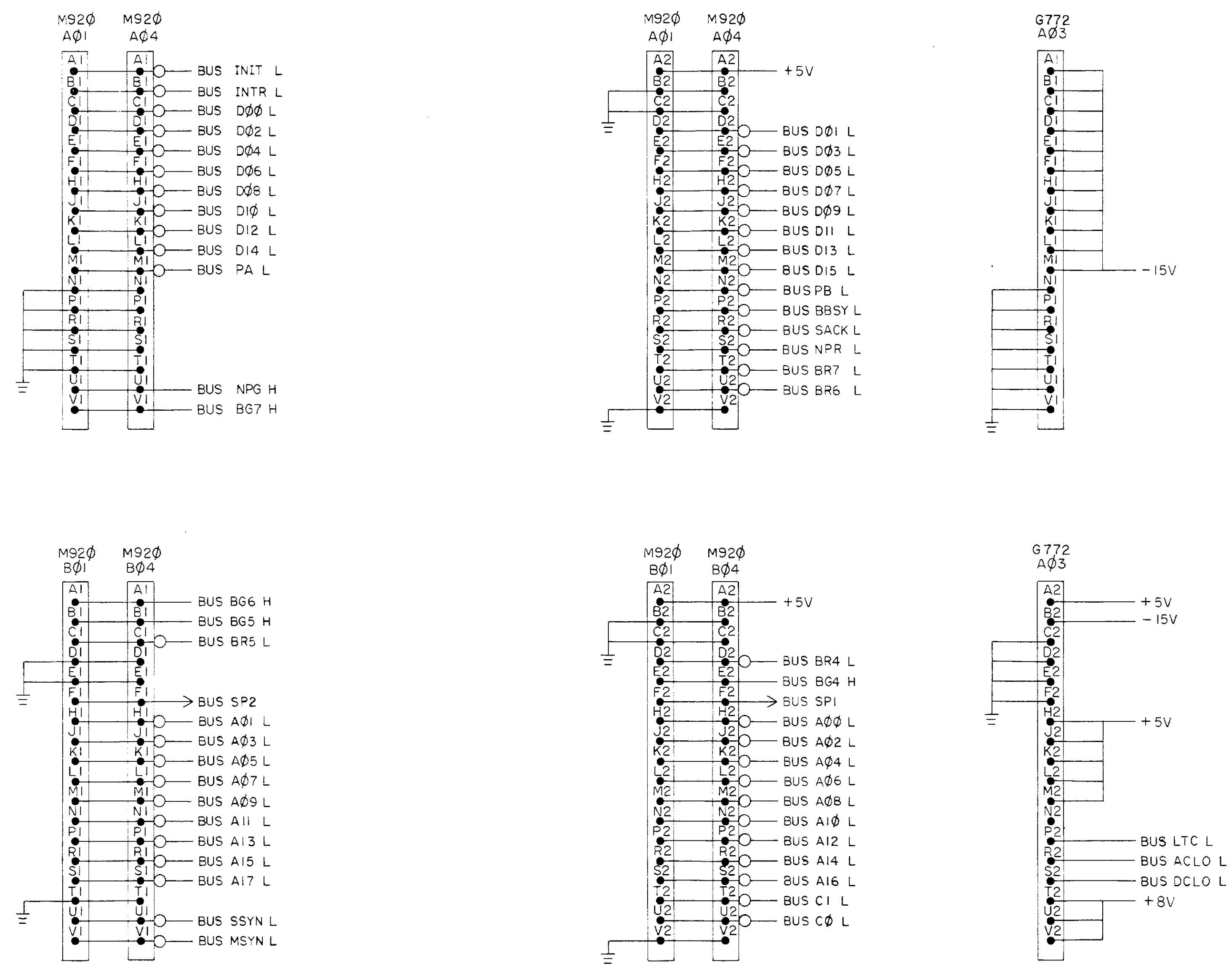

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP11

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ±.005 FRACTIONS ±1/64 ANGLES ±0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

DRN. R. Rainault DATE 9-8-69
CHK'D. DATE
ENG. DATE 10-31-69
PROJ. ENG. DATE
PROD. DATE 11/3/69

NEXT HIGHER ASS'Y A-ML-MMII-E

SCALE NONE
SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: I/O CONNECTORS

SIZE D CODE IC NUMBER MM11-E-Ø9 REV

REVISIONS | REV | CHANGE NO | CHK

DEC FORM NO DRD 102A

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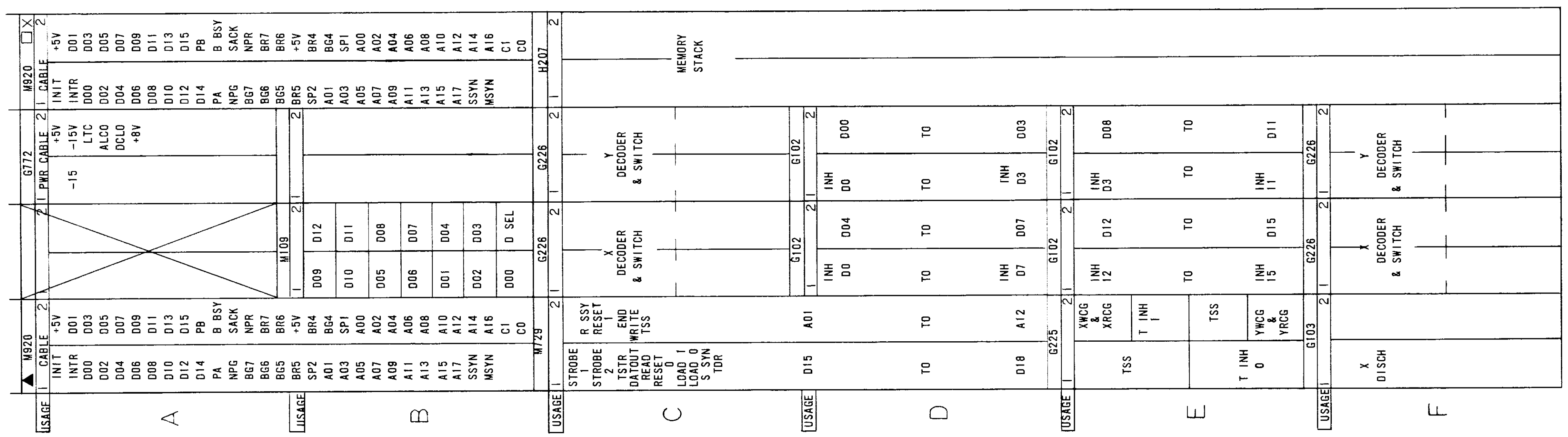


□ IF END OF BUS REPLACE M920 WITH M930.

X IF LAST UNIT IN BASIC BOX REPLACE M920 WITH BC11A CABLE END WHEN EXPANDING TO PERIPHERAL BOX.

▲ IF FIRST UNIT IN EXPANDER BOX REPLACE M920 WITH BC11A CABLE END.

CHK	CHANGE NO.	REV
	MM11E-00005 REDRAWN & REVISED T. Quellen 2.5.70 DURANT	A
	MM11E-00010 P. DURANT	B
	MM11E-00013 W. COATES	C

FIRST USED ON OPTION/MODEL: PDP11

DO NOT SCALE DRAWING. UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'. FINAL SURFACE QUALITY √. REMOVE BURRS AND BREAK SHARP CORNERS.

MATERIAL: —/—
FINISH: —/—

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN. RAIMONDI	DATE 7-21-69	
CHK'D. PFYFFER	DATE 10-31-69	
ENG. DURANT	DATE 10-31-69	
PROJ. ENG. DURANT	DATE 10-31-69	
PROD. MAC DONALD	DATE 11-6-69	

NEXT HIGHER ASSY: A-ML-MM11-E

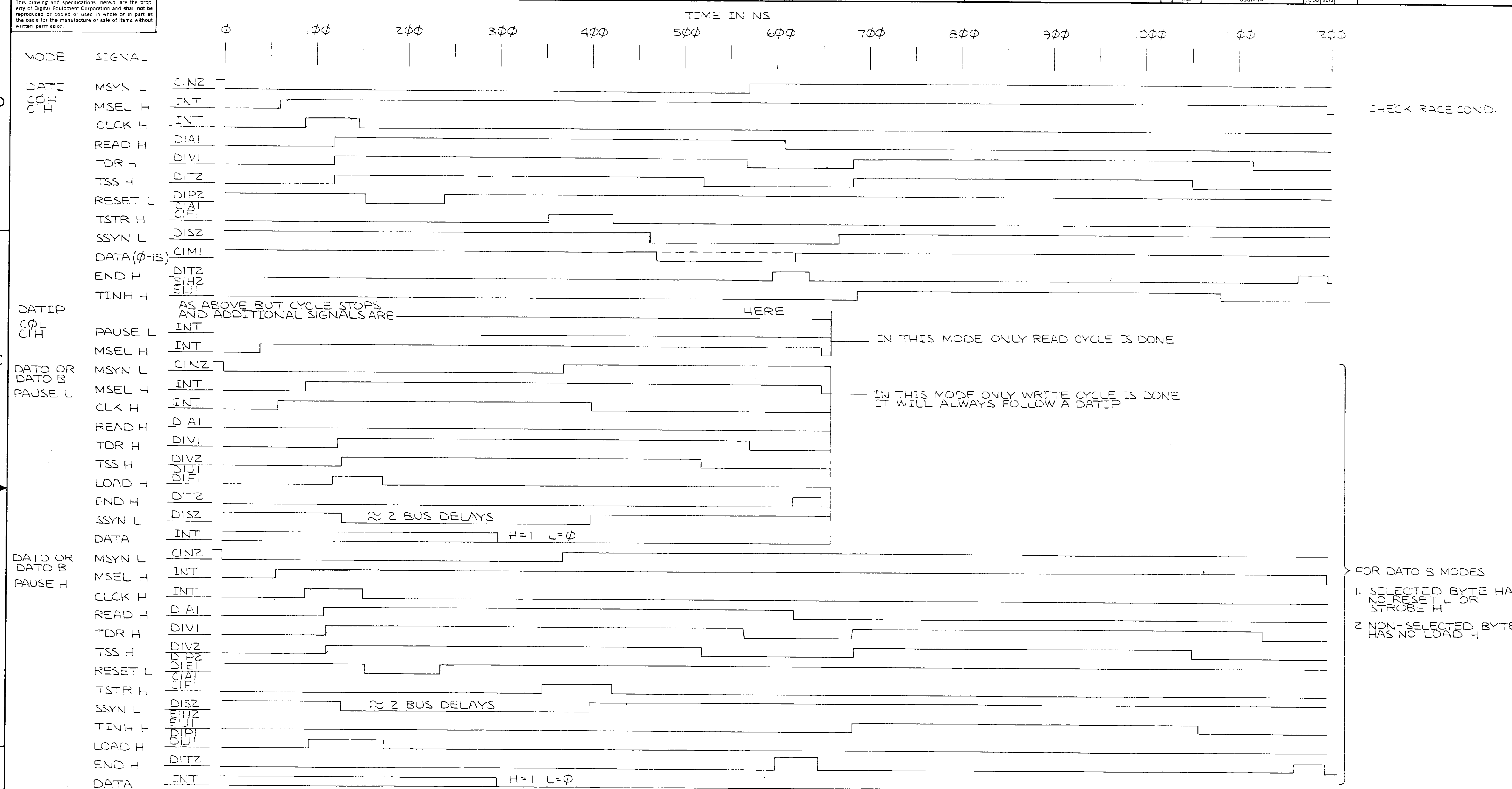
SCALE —/— SHEET 1 OF 1

DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

SIZE D | CODE MU | NUMBER MM11-E-Ø6 | REV. C

DEC FORM NO. DRD 100



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REVISIONS		
CHK	CHANGE NO	REV
	MM11-E-00004	A

FIRST USED ON OPTION/MODEL: PDP11

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS ±.005, FRACTIONS ±1/64, ANGLES ±0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL
FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

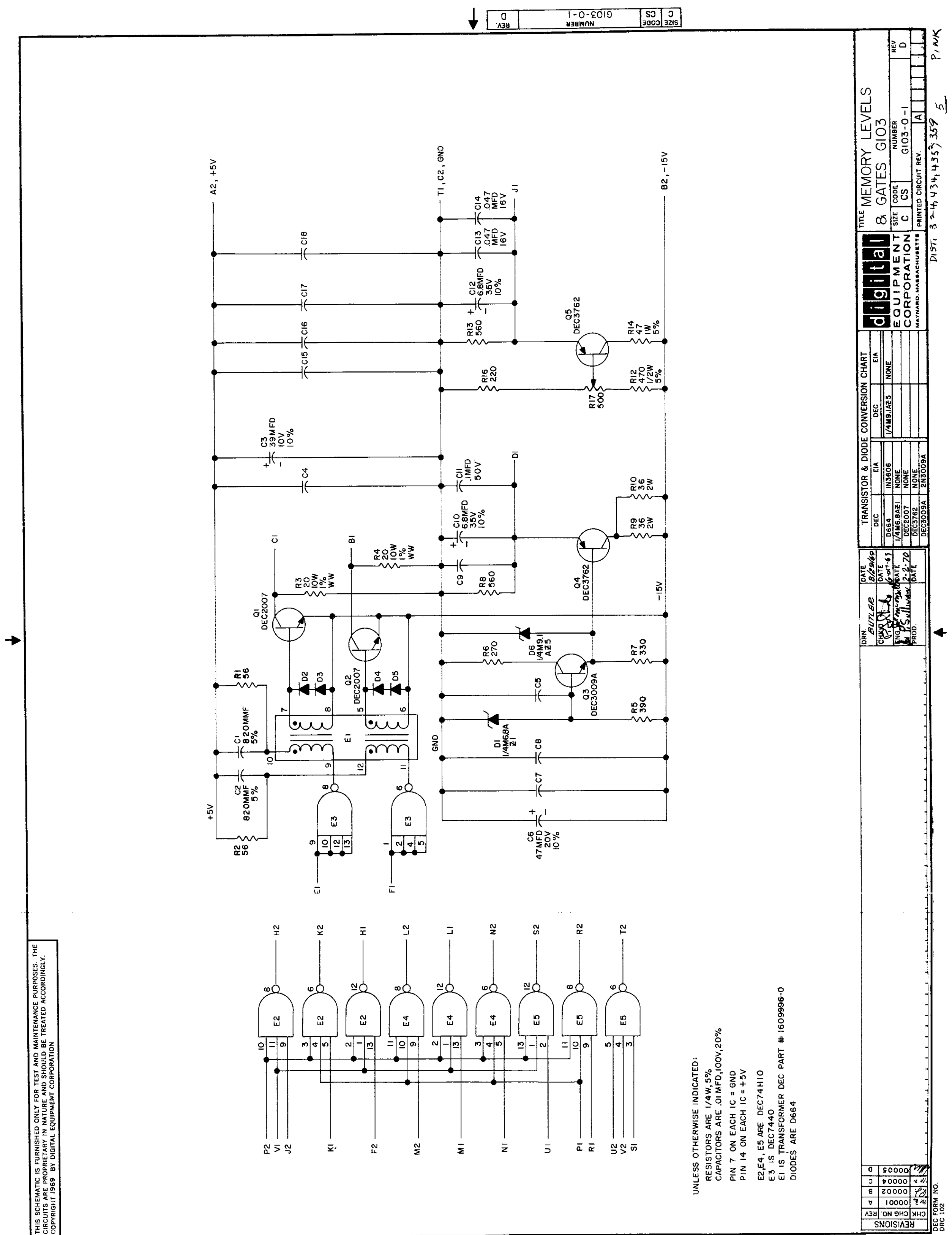
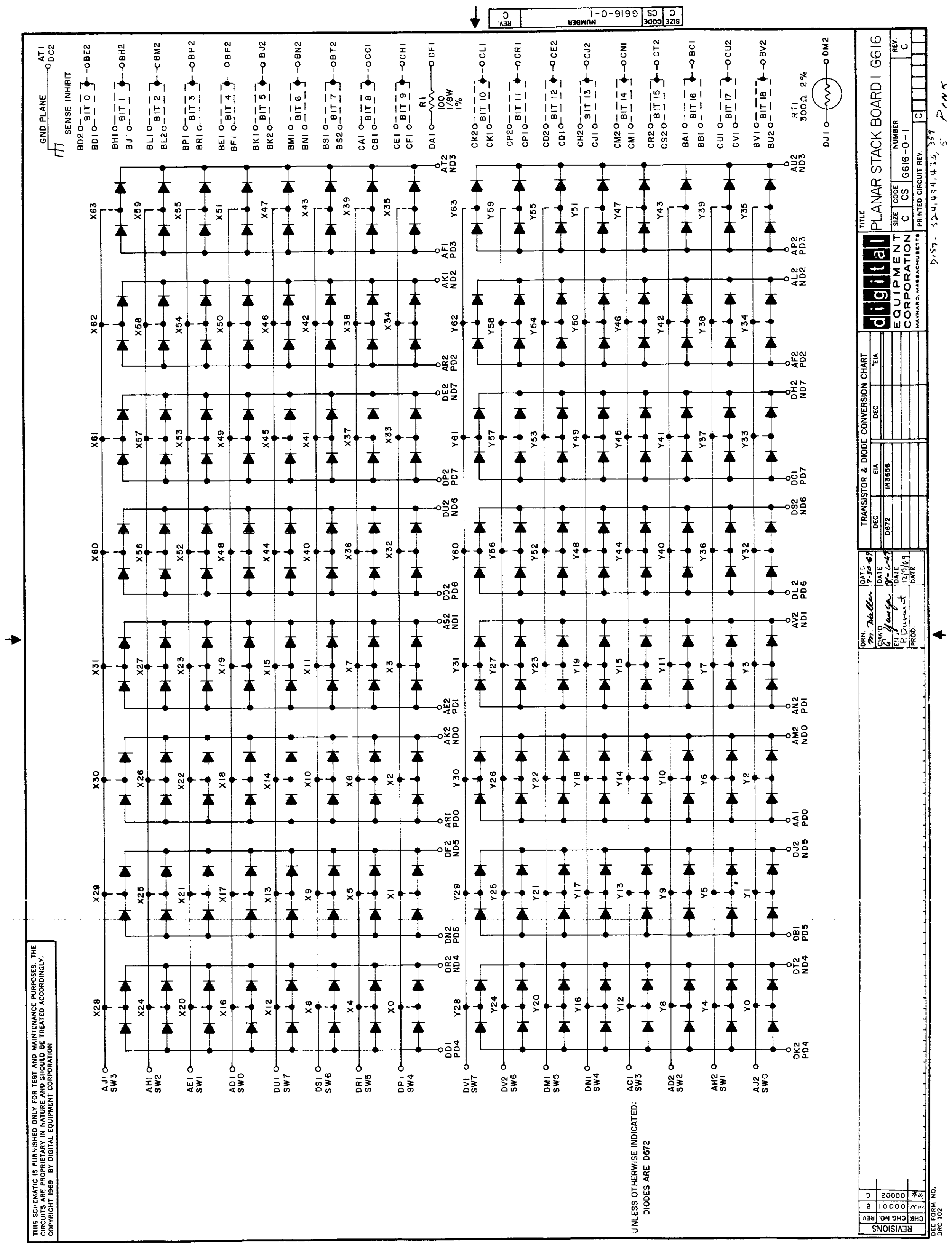
TITLE: TIMING & FLOW

NEXT HIGHER ASSY: A-VL-MM11-E

SCALE: NONE
SHEET 1 OF 1

SIZE: D | CODE: TD | NUMBER: MM11-E-Ø8 | REV: A

DEC FORM NO DRD 100


MEMORY LEVELS & GATES G103
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TRANSISTOR & DIODE CONVERSION CHART
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE .01MFD,100V,20%
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E2,E4, E5 ARE DEC74H10
E3 IS DEC7440
E1 IS TRANSFORMER DEC PART # 1609996-0
DIODES ARE D664
THIS SCHEMATIC IS FURNISHED ONLY FOR TEST AND MAINTENANCE PURPOSES. THE CIRCUITS ARE PROPRIETARY IN NATURE AND SHOULD BE TREATED ACCORDINGLY. COPYRIGHT 1969 BY DIGITAL EQUIPMENT CORPORATION

PLANAR STACK BOARD I G616
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TRANSISTOR & DIODE CONVERSION CHART
UNLESS OTHERWISE INDICATED:
DIODES ARE D672
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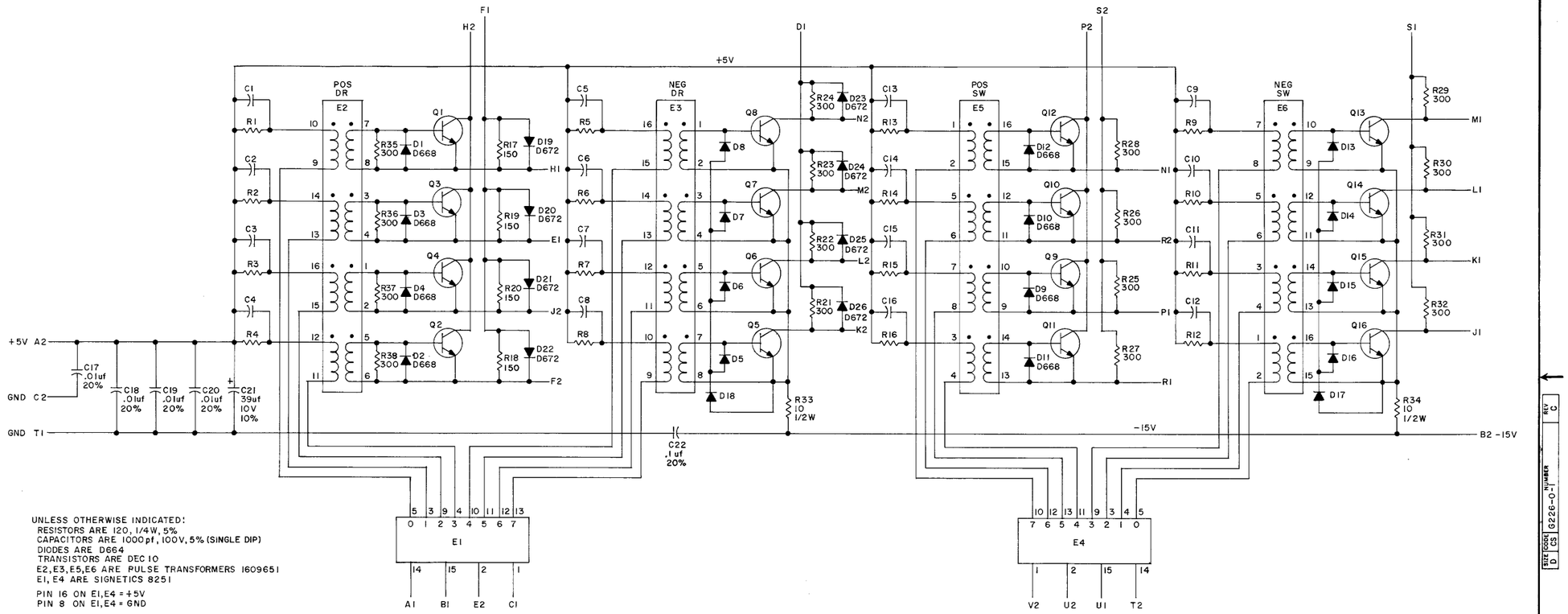


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 120, 1/4W, 5%
CAPACITORS ARE 1000 pf, 100V, 5% (SINGLE DIP)
DIODES ARE D664
TRANSISTORS ARE DEC 10
E2, E3, E5, E6 ARE PULSE TRANSFORMERS 1609651
E1, E4 ARE SIGNETICS 8251

PIN 16 ON E1, E4 = +5V
PIN 8 ON E1, E4 = GND

REVISIONS		
CHG	CHG NO.	REV.
Mod	00001	A
Mod	00002	B
Mod	00003	C

DRN	BUTLER	DATE 8-14-69
CHK'D	T. A. NALETTE	DATE 9-5-69
ENG	P. SULLIVAN	DATE 2-26-70
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		
DEC10	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

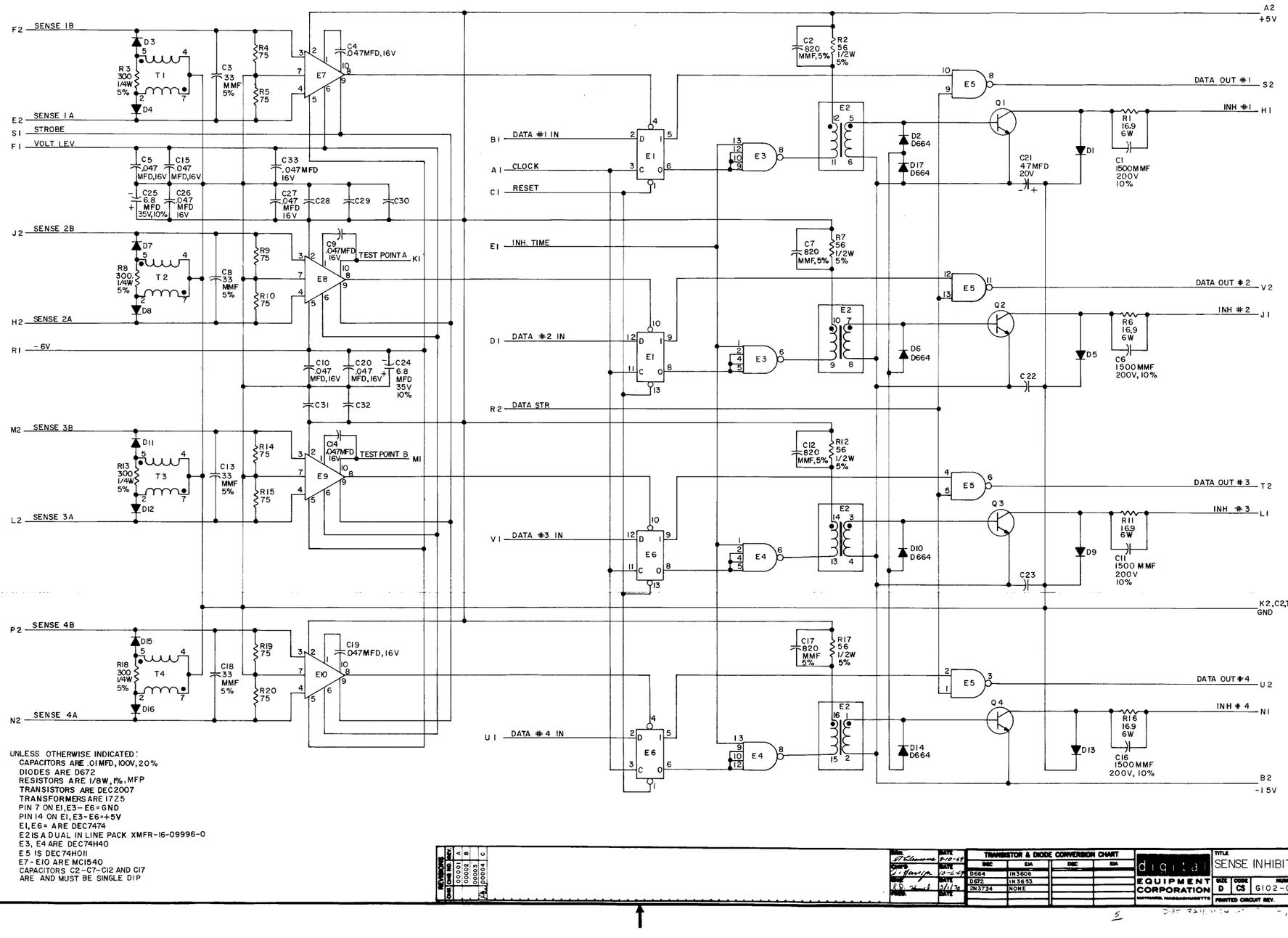
TITLE: X-Y DECODER SWITCH G226

SIZE	CODE	NUMBER	REV
D	CS	G226-0-1	C

PRINTED CIRCUIT REV. C

DEC FORM NO. DRD 116

REV C | SIZE D | CODE CS | NUMBER G226-0-1



UNLESS OTHERWISE INDICATED:
CAPACITORS ARE .01MFD, 100V, 20%
DIODES ARE D672
RESISTORS ARE 1/8W, 1%, MFP
TRANSISTORS ARE DEC2007
TRANSFORMERS ARE 17Z5
PIN 7 ON E1, E3-E6 = GND
PIN 14 ON E1, E3-E6 = +5V
E1, E6 = ARE DEC7474
E2 IS A DUAL IN LINE PACK XMFR-16-09996-0
E3, E4 ARE DEC74H40
E5 IS DEC74H011
E7-E10 ARE MC1540
CAPACITORS C2-C7-C12 AND C17 ARE AND MUST BE SINGLE DIP

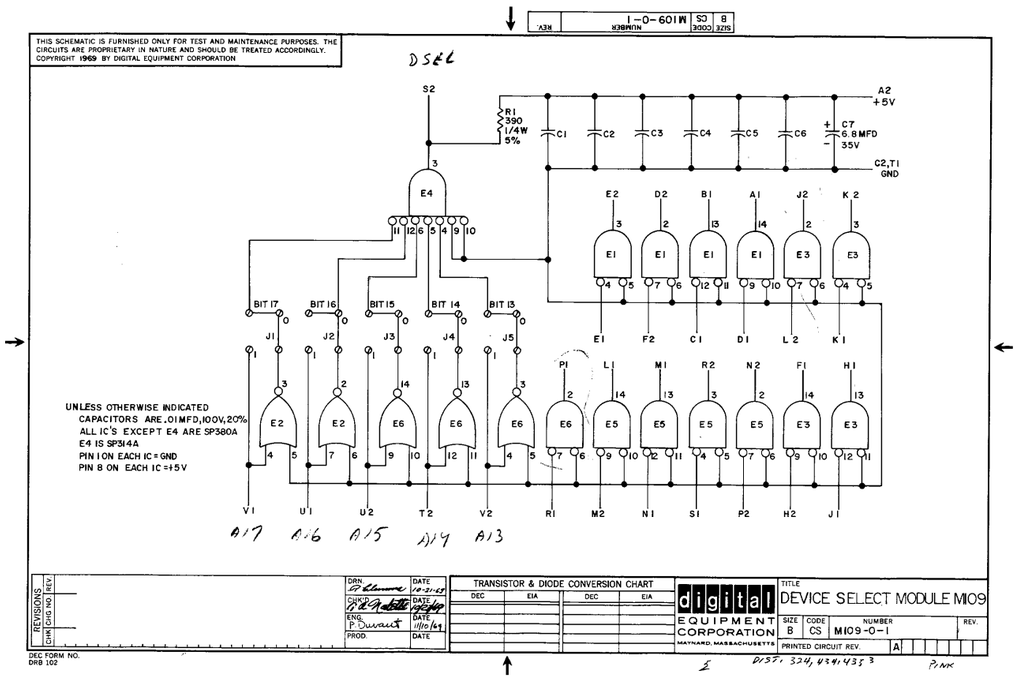
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606		
D672	IN3653		
2N3734	NONE		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: SENSE INHIBIT-CARD G102

SIZE D | CODE CS | NUMBER G102-0-1 | REV C

PRINTED CIRCUIT REV. D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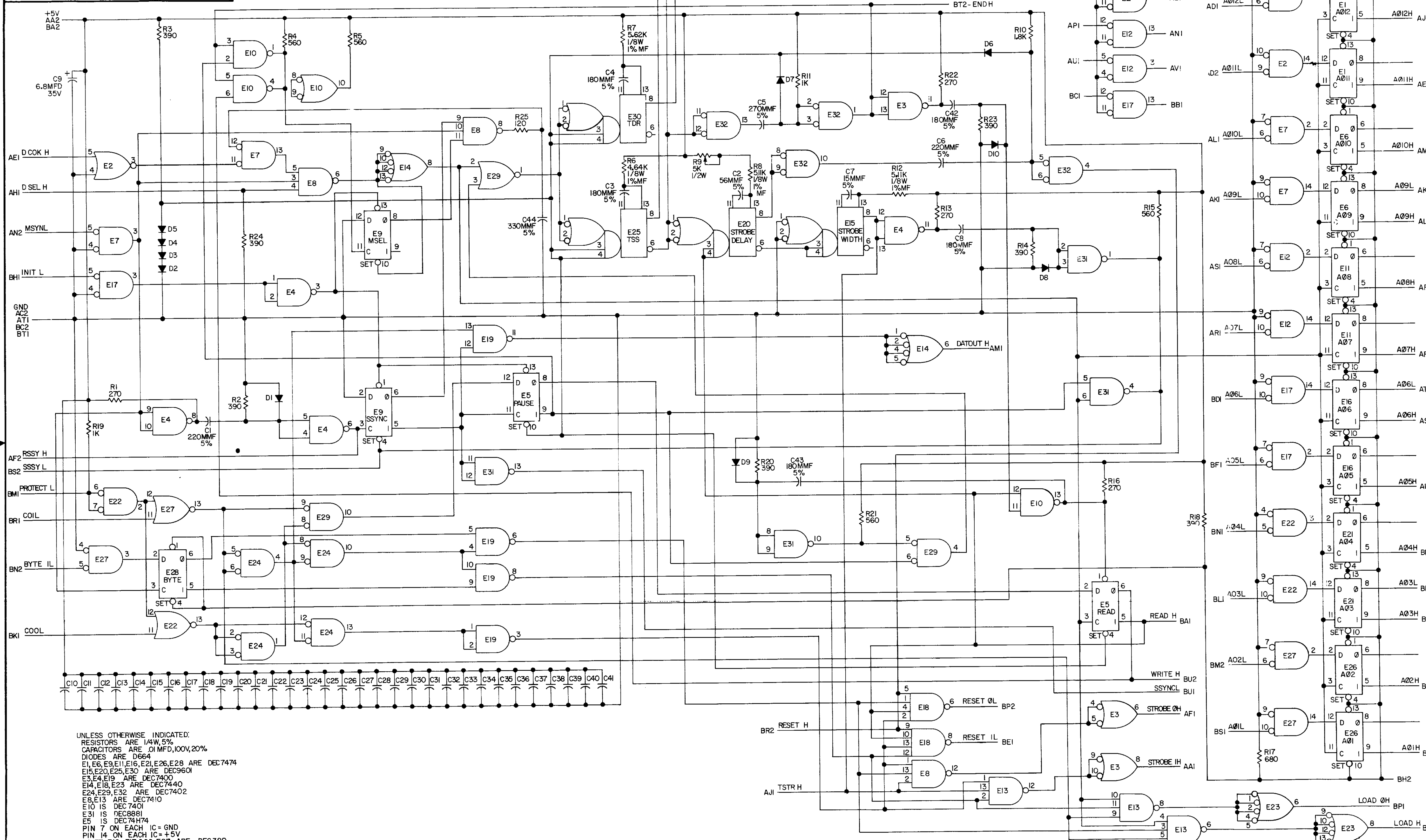
SIZE B CODE CS NUMBER M109-0-1 REV:
DSEL
S2
R1 390 1/4W 5%
C1 C2 C3 C4 C5 C6
C7 6.8MFD 35V
A2 +5V
C2,T1 GND
E4
E2 D2 B1 A1 J2 K2
E1 E1 E1 E1 E3 E3
BIT 17 BIT 16 BIT 15 BIT 14 BIT 13
J1 J2 J3 J4 J5
E2 E2 E6 E6 E6 E6
P1 L1 M1 R2 N2 F1 H1
E5 E5 E5 E5 E3 E3
V1 U1 U2 T2 V2 R1 M2 N1 S1 P2 H2 J1
A17 A16 A15 A14 A13
UNLESS OTHERWISE INDICATED
CAPACITORS ARE .01MFD,100V,20%
ALL IC'S EXCEPT E4 ARE SP380A
E4 IS SP314A
PIN 1 ON EACH IC = GND
PIN 8 ON EACH IC = +5V
REVISIONS
DRN. DATE
CHKD. DATE
ENG. P. Durant DATE 11/10/69
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA DEC EIA
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE DEVICE SELECT MODULE M109
SIZE B CODE CS NUMBER M109-0-1 REV.
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102
DIST. 324, 434, 435
PINK



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE .01 MFD, 100V, 20%
DIODES ARE D664
E1, E6, E9, E11, E16, E21, E26, E28 ARE DEC7474
E15, E20, E25, E30 ARE DEC9601
E3, E4, E19 ARE DEC7400
E14, E18, E23 ARE DEC7440
E24, E29, E32 ARE DEC7402
E8, E13 ARE DEC7410
E10 IS DEC7401
E31 IS DEC8881
E5 IS DEC74H74
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
E2, E7, E12, E17, E22, E27 ARE DEC380
PIN 1 ON DEC380 = GND
PIN 8 ON DEC380 = +5V

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	1N3606		

DRN. DATE 12-10-69
CHK'D DATE 1-13-70
ENG. P. Durant DATE 3/15/70
PROD. DATE

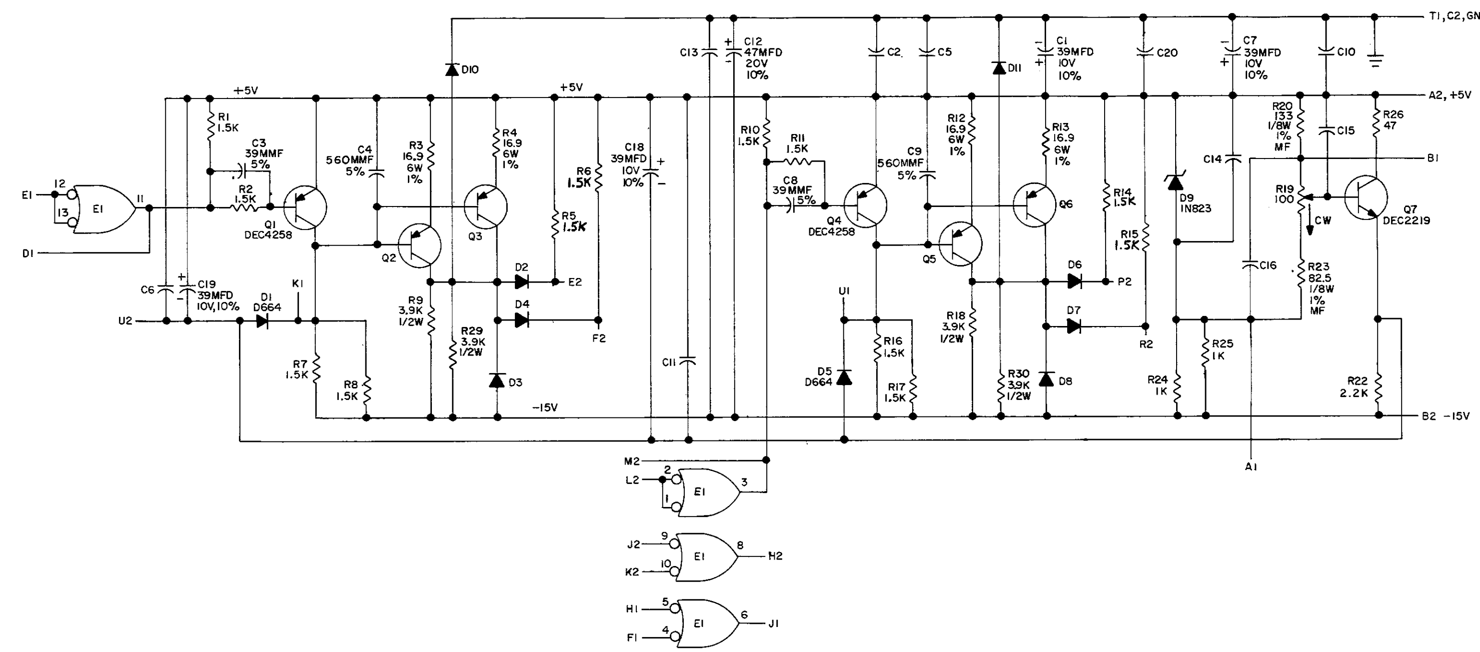
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE M MIIE CONTROL LOGIC M729

SIZE D CODE CS NUMBER M729-0-1 REV. A

PRINTED CIRCUIT REV. B

DIST. 324 434, 455 3   5 PINK



UNLESS OTHERWISE INDICATED:

PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
DIODES ARE D672
TRANSISTORS ARE DEC3762
RESISTORS ARE 1/4W,5%
CAPACITORS ARE .01MFD, 100V, 20%
E1 IS DEC74H00N

REVISIONS		
CHK	CHG NO	REV
	00001	A
	00003	B

DRN.	BUTLER	DATE 8-28-69
CHK'D	A. Younge	DATE 9-5-69
ENG.	for P. Sullivan	DATE 2-2-70
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
1N756A	SAME	DEC4258	2N4258
D664	1N3606		
D672	1N3653		
DEC2219	2N2219		
DEC3762	2N3762		

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE X & Y CURRENT GENERATOR G225

SIZE	CODE	NUMBER	REV.
C	CS	G225-0-1	B

PRINTED CIRCUIT REV. B

DEC FORM NO. DRC 102

5 DIST: 324, 434, 435, 357

READER'S COMMENTS

PDP-11 MM11E CORE MEMORY
DEC-11-HR3A-D

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