

11/24

11/24 ROM M9312
CJM9AA0

AH-T208A-MC
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JUL 1982
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IDENTIFICATION

PRODUCT CODE: AC-T207A-MC

PRODUCT NAME: CJM9AA0 11/24 ROM M9312

PRODUCT DATE: APRIL,1982

MAINTAINER: DIAGNOSTIC ENGINEERING

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SEQ 0002

50
51
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HISTORY

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1.0 GENERAL PROGRAM INFORMATION

1.1 ABSTRACT

THIS DIAGNOSTIC IS GO/NOGO VERIFICATION OF AN 11/24 SYSTEM WHICH TESTS:

1. ALL SINGLE AND DOUBLE OPERAND INSTRUCTIONS, INCLUDING EIS, UTILIZING ALL SOURCE AND DESTINATION ADDRESSING MODES.
2. ALL OF MEMORY, IN 4K PAGES, VIA MEMORY MANAGEMENT AND PRINT THE MEMORY SIZE (LAST MEMORY ADDRESS +2).
3. SLU1 VIA MAINTENANCE MODE (ALSO CHECKS CONSOLE PRINTER AND INTERFACE WHEN PRINTING MEMORY SIZE).
4. THE DIAGNOSTIC IS COMPATIBLE WITH M9312 DIAGNOSTIC ROM FORMAT REQUIREMENTS.

1.2 SYSTEM REQUIREMENTS

A. HARDWARE REQUIREMENTS

THIS DIAGNOSTIC IS DESIGNED TO RUN ON AN 11/24 WITH CONSOLE TERMINAL AND 4K OF MEMORY (MINIMUM). FURTHER, IT ASSUMES THE PRESENCE OF THE MEMORY MANAGEMENT UNIT (MMU) CHIP.

B. SOFTWARE REQUIREMENTS

NONE

1.3 RELATED DOCUMENTS AND STANDARDS

THE FOLLOWING DOCUMENTS WERE USED OR REFERENCED DURING THE CREATION OF THIS DIAGNOSTIC:

1. DIAGNOSTIC ENGINEERING STANDARDS AND CONVENTIONS PROGRAMMING PRACTICES (DOC. NO. 175-003-009-02).
2. PDP-11 SYSMAC PACKAGE (MAINDEC-11-DZQAC-C3).
3. REQUIRMENTS FOR NEW BOOT ROMS AND CPU ROMS USED IN THE M9312 (K-SP-M9312-0-8).

1.4 DIAGNOSTIC HIERARCHY PREREQUISITES

NGNE

1.5 ASSUMPTIONS

THE DIAGNOSTIC ASSUMES PROPER STEPUP OF THE DIP SWITCHPAK ON THE M9312 BOOTSTRAP MODULE (SEE M9312 USER'S MANUAL AND TABLE BELOW FOR THIS INFORMATION) AND PRESENCE OF A BOOT ROM IN THE M9312.

BOOTSTRAP:	DIAGNOSTICS	S1 (1-10)		
		FIRST DEVICE (ALL ROMS)	VIRTUAL ADDRESS	SWITCHPAK S1 SWITCHES ON
ODT	NO	2004	165004	1,9
	YES	2006	165006	1,9,10
DEVICE ROM #1	NO	0004	173004	9
	YES	0006	173006	9,10
DEVICE ROM #2	NO	0204	173204	4,9
	YES	0206	173206	4,9,10
DEVICE ROM #3	NO	0404	173404	3,9
	YES	0406	173406	3,9,10
DEVICE ROM #4	NO	0604	173604	3,4,9
	YES	0606	173606	3,4,9,10

2.0 OPERATING INSTRUCTION

2.1 LOADING AND STARTING PROCEDURE

IF DIAGNOSTIC IS SELECTED BY M9312 SWITCHPAK, IT WILL BE RUN ON POWER UP, BUT CAN ALSO SELECTED FROM MICRO-ODT BY COMMAND:

165000G

TO BOOT A DEVICE ROM DIRECTLY, USE THE VIRTUAL ADDRESS COLUMN OF THE ABOVE TABLE. FOR EXAMPLE, TO BOOT DEVICE ROM #3 WITH DIAGNOSTICS, USE 173406G (FROM MICRO-ODT).

2.2 PROGRAM OPTIONS

NONE

2.3 EXECUTION TIMES

A. FIRST PASS (QV)

A PASS OF THIS CODE TAKES APPROXIMATELY 6 SECONDS TO COMPLETE INCLUDING THE PRINTING OF THE MEMORY SIZE. THIS TIMING IS BASED ON A 11/24 CPU WITH 128K WORD OF MOS MEMORY.

B. LONGEST TEST

THE LONGEST SINGLE TEST IS THE MEMORY TEST WHICH TAKES APPROXIMATELY 5 SECONDS PER 128K WORDS OF MEMORY.

C. ADDITIONAL TIME FOR UNITS

APPROXIMATELY 5 SECONDS IS ADDED TO THE TEST TIME FOR EVERY ADDITIONAL 128K WORDS OF MEMORY. THIS TIMING IS BASED ON AN 11/24 WITH MOS MEMORY.

SAMPLE TEST TIMES BASED ON ABOVE FIGURES:

128KW=	6 SECONDS
256KW=	11 SECONDS
512KW=	21 SECONDS
1024KW=	41 SECONDS
1536KW=	61 SECONDS
1920KW=	76 SECONDS

D. FULL PASS TIME (ITERATIONS)

THIS PROGRAM DOES NOT DO ANY ITERATIONS ON ANY OF THE TESTS AND IN FACT ONLY MAKES ONE PASS THRU THE CODE FOR EACH START.

3.0 ERROR INFORMATION

3.1 ERROR REPORTING PROCEDURES

SINCE THIS DIAGNOSTIC IS A GO/NOGO, LOW-LEVEL TEST, NO ERROR REPORTING, AS SUCH, IS IMPLEMENTED; HOWEVER, IF THE MICRO-ODT AND CONSOLE TERMINAL ARE OPERATIONAL THE ERROR HALT ADDRESS+2 WILL BE TYPED FOR THE OPERATOR.

3.2 ERROR HALTS

BADADD = 165144	THIS ERROR IS CAUSED BY TRAPPING TO LOCATION 4 AT ANY TIME PRIOR TO EXECUTING THE MEMORY TEST ON THE FIRST 4K OF MEMORY. THE PROGRAM DOES ACCESSES TO SOME OF THE MEMORY MANAGEMENT REGISTERS DURING THIS TIME. IT MAY BE HELPFUL TO EXAMINE THE STACK BUT SINCE THE PROGRAM HAS NOT SET IT UP THE INFORMATION RECIEVED MAY NOT BE VALID.
CPUERR = 165146	THIS ERROR INDICATES A FAILURE WITH EITHER THE BASE INSTRUCTION SET OR THE EIS INSTRUCTION SET. FIRST SUSPECT THE DCF11-A HYBRID OR THE CPU BOARD.
MEMERR = 165550	THIS ERROR INDICATES A MEMORY SYSTEM FAILURE. FIRST SUSPECT THE MEMORY THEN THE KTF11-A. TO LOCATE THE FAILING BANK DIVIDE THE CONTENTS OF PAR0 (1772342) BY 200(8) THEN MULTIPLY BY 4.
SLUERR = 165702	THIS HALT INDICATES A DATA ERROR IN THE CONSOLE SLU. THE GOOD DATA IS IN R2.

4.0 PERFORMANCE AND PROGRESS REPORTS

4.1 PERFORMANCE REPORTS

NONE

4.2 PROGRESS REPORTS

THE PROGRAM REPORTS ITS PROGRESS USING TWO LEDS LOCATED ON THE 11/24 CPU BOARD. THEY ARE LOCATED ON THE HANDLE EDGE OF THE BOARD ALONG WITH THE RUN LIGHT. THEY ARE DRIVEN THROUGH BITS 0 AND 1 OF THE DISPLAY REGISTER WITH BIT 0 DRIVING THE LED FURTHEST FROM THE FRONT OF THE BOX AND BIT 1 DRIVING THE LED IN THE CENTER OF THE THREE LIGHTS. THE LIGHT CLOSEST TO THE FRONT OF THE BOX IS THE RUN LIGHT. THE PROGRAM FIRST WRITES AN OCTAL 3 TO THE REGISTER (TURNING BOTH LEDS ON) TO SIGNAL THE START OF THE CPU TEST. THE COUNT IS DECREMENTED BY ONE AT THE START OF EACH OF THE NEXT THREE TEST SECTIONS.

LIGHT COUNT

3
2
1
0

LAST TEST COMPLETED

NONE-SUCCESSFUL ENTRY TO PROGRAM
CPU TEST
MEMORY TEST
SLU TEST

5.0 DEVICE INFORMATION TABLES

POOL (LOC 165102) CONTAINS DATA USED BY DOUBLE OPERAND SECTION.

6.0 PROGRAM DESCRIPTION

6.1 PROGRAM EXECUTION CHARACTERISTICS

PROPER EXECUTION OF THE DIAGNOSTIC RESULTS IN PRINTOUT OF THE MEMORY SIZE AND BOOTING A PERIPHERAL OR ENTERING MICRO-ODT (DEPENDING ON M9312 SWITCH SETTINGS).

6.2 SUBTEST SUMMARIES

A. CPUTST - THIS SUBTEST VERIFIES THE PDP-11 INSTRUCTION SET, INCLUDING EIS, FOR BOTH WORD AND BYTE FORMATS. IT CONSISTS OF FIVE SECTIONS - SINGLE OPERAND (DESTINATION MODE 0), DOUBLE OPERAND (ALL SOURCE MODES, DESTINATION MODE 0), CONDITIONAL BRANCHES, BYTE INSTRUCTIONS (ALL DESTINATION MODES), AND JSR/RTS WITH EIS.

B. MEMTST - THIS SUBTEST CHECKS ALL OF MEMORY IN 4K PAGES USING THE MMU, DETERMINES MEMORY SIZE, AND CONSTRUCTS A PHYSICAL ADDRESS FROM THE VIRTUAL ADDRESS WHICH CAUSED A TIMEOUT TRAP. LOOPING THROUGH EACH 4K PAGE IS CONTROLLED BY THE 1\$ LOOP, AND; WITHIN THIS LOOP, THE 2\$ LOOP LOADS EACH LOCATION WITH ITS ADDRESS, THE 3\$ LOOP CHECKS THE DATA AND COMPLEMENTS IT, THE 4\$ LOOP ADDS THE CONTENTS OF EACH LOCATION TO ITS COMPLEMENT AND INCREMENTS THE RESULT TO PRODUCE ZERO. SECTION TIMEOUT TURNS OFF MEMORY MANAGEMENT AND BUILDS A PHYSICAL ADDRESS IN R0 AND R1.

NOTE: BECAUSE OF SPACE LIMITATIONS THERE IS A KNOWN FLAW IN THE MEMORY SIZING ROUTINE. IF MAXIMUM MEMORY IS CONFIGURED ON THE SYSTEM(1920KW) THE SIZING ROUTINE WILL REPORT A MEMORY SYSTEM SIZE OF 2044KW. THIS IS BECAUSE OF THE UNIBUS MAP WILL MAP THE LAST 124K OF VIRTUAL ADDRESS SPACE TO THE LOWER 124K OF MAIN MEMORY.

C. SLUTST - THIS SUBTEST PLACES SLU1 IN MAINTENANCE MODE (SERIAL OUT OF UART TIED TO SERIAL IN OF UART) AND TESTS THAT ALL 8-BIT PATTERNS CAN BE TRANSMITTED AND RECEIVED. SECTION PRINT PRINTS THE MEMORY SIZE CALCULATED BY MEMTST, AND TRANSFERS CONTROL BACK TO ODT OR THE APPLICABLE BOOT ROM.

6.3 SPECIAL SUBROUTINE DESCRIPTION

THE PRINT ROUTINE TYPES THE LAST 22-BIT MEMORY ADDRESS+2 FOUND BY THE MEMORY SIZE ROUTINE. THE 16 HIGH ORDER BITS ARE SAVED IN R0 AND THE 6 LOW ORDER BITS ARE SAVED IN R1.

7.0 LISTING

```
354      %
355
356      .TITLE  CJM9AA
357      .SBTTL  ROM AREA 165000-165776
358      .SBTTL  GO/NOGO MINIMUM DIAGNOSTIC
365      .TITLE  CJM9AA0 11/24 ROM M9312
(1)      ;*COPYRIGHT (C) APRIL, 1982
(1)      ;*DIGITAL EQUIPMENT CORP.
(1)      ;*MAYNARD, MASS. 01754
(1)      ;*
(1)      ;*PROGRAM BY D. SOBIK
(1)      ;*
(1)      ;*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
(1)      ;*PACKAGE (MAINDEC-11-DZQAC-C5), JAN, 1981.
(1)      ;*
(1)      000001 $TN=1
(1)      160000 $SWR=160000      ;;HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT
366
367      .SBTTL  REGISTER DEFINITIONS
368      177570      SWR=      177570      ;SWITCH REGISTER (DIAGNOSTIC LIGHTS)
369      177776      PS=      177776      ;PROCESSOR STATUS WORD
370      ;SLU1 REGISTERS
371      177560      RCSR=     177560      ;RECEIVER CSR
372      177562      RBUF=     177562      ;RECEIVER BUFFER
373      177564      XCSR=     177564      ;TRANSMITTER CSR
374      177566      XBUF=     177566      ;TRANSMITTER BUFFER
375
376      ;MMU REGISTERS
377      172340      PAR0=     172340      ;KERNAL PAGE ADDRESS REGISTERS
378      172342      PAR1=     172342
379      172356      PAR7=     172356
380      172300      PDR0=     172300      ;KERNAL PAGE DESCRIPTOR REGISTERS
381      172302      PDR1=     172302
382      172316      PDR7=     172316
383      177640      UPAR0=    177640      ;USER PAGE ADDRESS REGISTERS
384      177642      UPAR1=    177642
385      177572      SR0=      177572      ;STATUS REGISTER 0
386      172516      SR3=      172516      ;STATUS REGISTER 3 (22-BIT)
```

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388      165000 165000
389 165000 000177 006020      START: JMP    @173024      ;TRANSFER TO SELECTED BOOT ROM OR ODT
390 165004 000000              HALT          ;ENTRY POINT FOR ODT, NO DIAGNOSTICS
391                                     ;ENTRY POINT FOR ODT WITH DIAGNOSTICS
392 165006 012704 165002      MOV    #165002,R4      ;SET UP RETURN ADDRESS-2 IN R4
393
394      .SBTTL CPU TEST
395      ;*****
396
397      :      BASIC CPU TEST
398
399      ;*****
400 165012 012737 000003 177570 CPUTST: MOV    #3, @#SWR      ;LIGHTS = 3, INDICATING CPUTST
401 165020 012737 165144 000004      MOV    #BADADD,@#4      ;SET UP TIME OUT VECTOR INCASE OF TRAP
402 165026 005037 000006              CLR    @#6              ;CLEAR PRIORITY OF TRAP ROUTINE
403 165032 010037 177640              MOV    R0,    @#UPAR0      ;WE ARE USING THE UPAR'S HERE SIMPLY BECAUSE
404 165036 010137 177642              MOV    R1,    @#UPAR1      ;THEY ARE AVAILABLE UNUSED INTERNAL REGS.
405                                     ;WE ARE STORING PARAMETERS FROM THE BOOT ROM
406
407                                     ;R1 CONTENTS      N Z V C
408 165042 005001              CLR    R1              ;000000      0 1 0 0
409 165044 005201              INC    R1              ;1          0 0 0 0
410 165046 005101              COM    R1              ;177776      1 0 0 1
411 165050 006201              ASR    R1              ;177777      1 0 1 0
412 165052 006301              ASL    R1              ;177776      1 0 0 1
413 165054 006001              ROR    R1              ;177777      1 0 1 0
414 165056 005701              TST    R1              ;177777      1 0 0 0
415 165060 005401              NEG    R1              ;1          0 0 0 1
416 165062 005301              DEC    R1              ;0          0 1 0 1
417 165064 005601              SBC    R1              ;177777      1 0 0 1
418 165066 005501              ADC    R1              ;0          0 1 0 1
419 165070 001026              BNE    CPUERR          ;ERROR IF NOT ZERO
420
421      ; SECTION FOR DOUBLE OPERAND, ALL SOURCE MODES, DEST MODE 0
422
423 165072 012702 165126      MOV    #POOL, R2      ;SET UP ADDRESS OF DATA TABLE
424 165076 011201              MOV    (R2), R1      ;R1/POOL, SMODE 1
425 165100 022201              CMP    (R2)+, R1      ;DATA CORRECT? SMODE 2
426 165102 001021              BNE    CPUERR
427 165104 063201              ADD    @-(R2)+, R1      ;R1/POOL + 1, SMODE 3
428 165106 165201              SUB    @-(R2), R1      ;R1/POOL, SMODE 5
429 165110 044201              BIC    -(R2), R1      ;R1/0, SMODE 4
430 165112 056201 000004      BIS    4(R2), R1      ;R1/177777, SMODE 6
431 165116 037201 000006      BIT    @6(R2), R1      ;RESULT IS 177777, SMODE 7
432 165122 001411              BEQ    CPUERR
433 165124 000411              BR     CONT
434
435 165126 165126      POOL:  .WORD  POOL
436 165130 165136      .WORD  DATA1
437 165132 177777      DATA2: .WORD  177777
438 165134 165132      .WORD  DATA2
439 165136 000001      DATA1: .WORD  1
440 165140 000500      DOUBLE: .WORD  500
441 165142 000500      .WORD  500
442 165144 000000      BADADD: HALT
443 165146 000000      CPUERR: HALT

```

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445
446      :      CHECK CONDITIONAL BRANCHES
447
448      165150 000277      CONT:  SCC      :SET ALL CONDITION CODES
449      165152 001375      BNE      CPUERR  :BR IF Z=0
450      165154 100374      BPL      CPUERR  :.. .. N=0
451      165156 102373      BVC      CPUERR  :.. .. V=0
452      165160 103372      BCC      CPUERR  :.. .. C=0
453      165162 002771      BLT      CPUERR  :.. .. N XOR V=1
454      165164 003370      BGT      CPUERR  :.. .. Z OR (N XOR V)=0
455      165166 101367      BHI      CPUERR  :.. .. C OR Z=0
456      165170 000257      CCC      :CLR ALL CONDITION CODES
457      165172 001765      BEQ      CPUERR  :BR Z=1
458      165174 100764      BMI      CPUERR  :BR N=1
459      165176 102763      BVS      CPUERR  :BR V=1
460      165200 105762      BCS      CPUERR  :BR C=1
461      165202 003761      BLE      CPUERR  :BR Z OR (N XOR V)=1
462      165204 101760      BLOS     CPUERR  :BR C OR Z=1
463      165206 000270      SEN      :N=1
464      165210 002356      BGE      CPUERR  :BR N XOR V=0
465
466      :      CHECK BYTE INSTRUCTIONS, ALL DEST MODES
467
468
469
470      165212 105001      CLRB      R1      :177400      0 1 0 0
471      165214 105201      INCB      R1      :177401      0 0 0 0
472      165216 105101      COMB      R1      :177776      1 0 0 1
473      165220 106201      ASRB      R1      :177777      1 1 0 0
474      165222 106301      ASLB      R1      :177776      1 0 0 1
475      165224 106001      RORB      R1      :177777      1 0 1 0
476      165226 105401      NEGB      R1      :177401      0 0 0 1
477      165230 105301      DECB      R1      :177400      0 1 0 1
478      165232 105601      SBCB      R1      :177777      1 0 0 1
479      165234 106101      ROLB      R1      :177777      1 0 0 1
480      165236 105501      ADCB      R1      :177400      0 1 0 1
481      165240 000301      SWAB      R1      :000377      1 0 0 0
482      165242 012703 000500      MOV      #500, R3      :SETUP FOR DMODE TESTING
483      165246 105063 000001      CLRB      1(R3)      :CLR LOC 501, DMODE 6
484      165252 110113      MOVB      R1, (R3)      :500/000 377, DMODE 1
485      165254 120123      CMPB      R1, (R3)+      :SHOULD COMPARE, DMODE 2
486      165256 001333      BNE      CPUERR
487      165260 105143      COMB      -(R3)      :500/000 000, DMODE 4
488      165262 012703 165140      MOV      #DOUBLE, R3      :SETUP DEFERRED DMODES
489      165266 153733 165136      BISB      @DATA1, @2(R3)+      :500/1, DMODE 3
490      165272 143753 165132      BICB      @DATA2, @-(R3)      :500/0, DMODE 5
491      165276 130173 000002      BITB      R1, @2(R3)      :Z=1, DMODE 7
492      165302 001321      BNE      CPUERR

```

```

494
495
496
497 165304 012706 000500
498 165310 004767 000006
499 165314 000714
500 165316 000167 000042
501 165322 012701 000040
502 165326 070127 000010
503 165332 006700
504 165334 072127 000006
505 165340 073127 000071
506 165344 071027 000200
507 165350 005201
508 165352 074001
509 165354 001274
510 165356 062716 000002
511 165362 000207

; CHECK JSR/RTS AND EIS

MOV #500, SP ;SET UP STACK
JSR PC, EISTST
BR CPUERR
JMP MEMTST ;EXIT CPU TEST
EISTST: MOV #40, R1 ;R1/ 40
MUL #10, R1 ;R1/ 400
SXT R0 ;R0/ 0
ASH #6, R1 ;R1/ 40000
ASHC #71, R1 ;R1/ 200
DIV #200, R0 ;R0/1 R1/0
INC R1 ;R1/1
XOR R0, R1 ;R1/0
BNE CPUERR
ADD #2, (SP) ;FIX RETURN ADDRESS TO BYPASS ERROR BR
RTS PC ;EXIT TO MEMORY TEST

```

```

513      ;:*****
514
515      .SBTTL  MEMTST
516
517      ;:*****
518
519      ;+
520      :      THIS TEST SIZES MEMORY AND CHECKS MEMORY FROM LOC 1000 TO END OF
521      :      MEMORY BY WRITING IN EACH LOCATION THE ADDRESS OF THE LOCATION
522      :      AND COMPARING THE LOCATION AND ITS CONTENTS. THE PROCEDURE IS
523      :      REPEATED USING THE COMPLEMENTS OF THE ADDRESS IN EACH LOCATION.
524      :      MEMORY IS CLEARED ON EXIT FROM THIS TEST IN 4K BLOCKS; THAT IS,
525      :      IF 122K IS PRESENT, 120K GETS CLEARED, THE REST HAS THE ADDRESS
526      :      WRITTEN IN IT.
527      :-
528
529
530      ;:*****
531
532      165364 0' 2737 000002 177570 MEMTST: MOV    #2,    @#SWR    ;LIGHTS = 2, INDICATING MEMTST
533      165372 0J5037 172340          CLR    @#PAR0    ;MAP VECTOR SPACE TO PAR0
534      165376 012737 077406 172300          MOV    #77406, @#PDR0    ;4K PAGE R/W
535      165404 005037 172342          CLR    @#PAR1    ;PAR1 IS MOVABLE WINDOW INTO MEMORY
536      165410 012737 077406 172302          MOV    #77406, @#PDR1
537      165416 012737 177600 172356          MOV    #177600, @#PAR7    ;MAP PAR7 TO I/O PAGE
538      165424 012737 077406 172316          MOV    #77406, @#PDR7
539      165432 005037 177776          CLR    @#PS      ;ENSURE KERNEL MODE
540      165436 005237 177572          INC    @#SR0      ;TURN ON KT
541      165442 012737 000020 172516          MOV    #20,    @#SR3      ;SET UP FOR 22-BIT RELOCATION
542      165450 012702 000002          MOV    #2,    @#2      ;WORD INCREMENT
543      165454 012737 165552 000004 1$:      MOV    #TIMOUT, @#4      ;SETUP TIMEOUT VECTOR FOR MEMORY SIZE
544      165462 012703 020000          MOV    #20000, R3      ;START AT VIRTUAL ZERO
545      165466 012705 010000          MOV    #10000, R5      ;PAGE LENGTH = 4K
546      165472 010301          MOV    R3,    R1      ;WORKING COPY OF FIRST ADDRESS
547      165474 010500          MOV    R5,    R0      ;COPY PAGE LENGTH
548      165476 010111          MOV    R1,    (R1)      ;WRITE ADDRESS INTO LOCATION
549      165500 060201          ADD    R2,    R1      ;INCREMENT ADDRESS
550      165502 077003          SOB    R0,    2$      ;LOOP TILL PAGE DONE
551      165504 010301          MOV    R3,    R1      ;RESTORE INITIAL CONDITIONS FOR
552      165506 010500          MOV    R5,    R0      ;DATA CHECK AND COMPLEMENTING
553      165510 020111          CMP    R1,    (R1)      ;GOOD DATA?
554      165512 001014          BNE    MEMERR      ;NO, HALT
555      165514 005121          COM    (R1)+      ;COM DATA AND INC ADDRESS
556      165516 077004          SOB    R0,    3$      ;LOOP TILL PAGE DONE
557      165520 010301          MOV    R3,    R1      ;START AGAIN TO TEST COM DATA
558      165522 010500          MOV    R5,    R0
559      165524 060111          ADD    R1,    (R1)      ;RESULT SHOULD BE -1
560      165526 005221          INC    (R1)+      ;RESULT=0 AND SETUP NEXT ADDRESS
561      165530 001005          BNE    MEMERR
562      165532 077004          SC    R0,    4$      ;FINISH THE PAGE
563      165534 062737 000200 172342          ADD    #200,    @#PAR1    ;RELOC TO A NEW PAGE
564      165542 000744          BR    1$      ;CHECK OUT A NEW PAGE
565      165544 005037 177572          MEMERR: CLR    @#SR0      ;TURN OFF KT
566      165550 000000          HALT      ;BAD MEMORY
567      165552 005037 177572          TIMEOUT: CLR    @#SR0      ;TURN OFF KT
568      165556 005037 172516          CLR    @#SR3      ;RESTORE 18-BIT RELOCATION

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569 165562 000402          BR      1$          ;BRANCH AROUND ENTRY POINT
570 165564 000167 177222    JMP      CPUTST      ;BOOT ROM ENTRY POINT
571 165570 012737 000006 000004 1$: MOV      #6,      @#4      ;TIMEOUT TRAPCATCHER
572 165576 160301          SUB      R3,      R1      ;GET RID OF VIRTUAL OFFSET
573 165600 005000          CLR      R0          ;CLR HIGH HALF OF DOUBLEWORD
574 165602 073027 000012    ASHC     #12,      R0      ;LSH 10. TO BUILD PHYSICAL ADDRESS
575 165606 063700 172342    ADD      @#PAR1, R0      ;ADD PAGE BASE ADDRESS
576 165612 073027 177776    ASHC     #-2,      R0      ;ACCOUNT FOR 1-BIT MSD
577                          .SBTTL  SLU1 TEST
578
579                          ;:*****
580
581                          ;      CHECK SLU1 VIA MAINTENANCE MODE
582
583                          ;:*****
584
585 165616 012737 000001 177570 SLUTST: MOV      #1,      @#SWR      ;LIGHTS = 1, INDICATING SLUTST
586 165624 005002          CLR      R2          ;FIRST ASCII CODE TO BE CHECKED
587 165626 012737 000004 177564    MOV      #4,      @#XCSR      ;ENABLE MAINTENANCE MODE
588 165634 105737 177564    2$: TSTB     @#XCSR      ;TRANSMITTER READY?
589 165640 100375          BPL      2$          ;NO, WAIT FOR READY
590 165642 110237 177566    MOVB     R2,      @#XBUF      ;TRANSMIT CHAR
591 165646 105737 177560    3$: TSTB     @#RCSR      ;DATA RECEIVED?
592 165652 100375          BPL      3$          ;NO
593 165654 120237 177562    CMPB     R2,      @#RBUF      ;DID DATA LOOP AROUND CORRECTLY?
594 165660 001006          BNE      SLUERR      ;NO
595 165662 005202          INC      R2          ;SET UP NEXT PATTERN
596 165664 105702          TSTB     R2          ;DONE ALL PATTERNS?
597 165666 001362          BNE      2$          ;NO, CONTINUE
598 165670 005037 177564    CLR      @#XCSR      ;EXIT MAINTENANCE MODE
599 165674 000403          BR       PRINT      ;PRINT LAST ADDRESS
600 165676 005037 177564    SLUERR: CLR      @#XCSR      ;EXIT MAINT MODE
601 165702 000000          HALT

```

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609 165704 005037 177570
610 165710 012705 000010
611 165714 012703 000003
612 165720 005002
613 165722 073027 000001
614 165726 006102
615 165730 077304
616 165732 062702 000060
617 165736 105737 177564
618 165742 100375
619 165744 110237 177566
620 165750 077517
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628 165752 013700 177640
629 165756 013701 177642
630 165762 000164 000002
631 165766 015
632 165767 012
633 165770 000240
634 165772 000240
635 165774 042060
636 165776 113422
637
638 165000
  
```

```

;;*****
;      PRINT MEMORY SIZE (LAST ADDRESS + 2) AND EXIT
;;*****
PRINT: CLR      @#SWR      ;LIGHTS = 0, ALL TESTS PASSED
        MOV      #10,      R5 ;PRINT 8. DIGITS
1$:     MOV      #3,      R3 ;SHIFT COUNT FOR DIGIT ASSEMBLY
        CLR      R2        ;CLR DIGIT ASSEMBLY AREA
2$:     ASHC     #1,      R0 ;PUT BIT IN C-BIT
        ROL      R2        ;MOVE C-BIT TO R2
        SOB      R3,      2$ ;BUILD A DIGIT IN R2
        ADD      #'0,      R2 ;CNVRT TO ASCII
3$:     TSTB     @#XCSR     ;PRINTER READY?
        BPL      3$
        MOVB     R2,      @#XBUF ;PRINT IT
        SOB      R5,      1$ ;PRINT 8. DIGITS

;////////////////////////////////////
;      EXIT TO ODT OR TO BOOT ROM
;////////////////////////////////////
        MOV      @#UPAR0, R0 ;RESTORE BOOT ROM PARAMETERS
        MOV      @#UPAR1, R1
        JMP      2(R4)       ;RETURN TO BOOT ROM OR ODT
CRLF:   .BYTE    15
        .BYTE    12
        NOP
        NOP
CRC:    .ASCII   '0D'       ;#4 LPU ROM FOR M9312
        .WORD    113422     ;CRC CHECKWORD FOR ROM
        .END      START
  
```

[illegible]

E 2
CJM9AAO 11/24 ROM M9312 MACY11 30(1046) 08-APR-82 14:41 PAGE 11
CJM9AA.P11 08-APR-82 14:41 CROSS REFERENCE TABLE -- MACRO NAMES

SEQ 0017

SLASH	362#	622	626							
STARS	362#	395	399	513	517	530	579	583	603	607
.HEADE	362#	365								

. ABS. 166000 000

ERRORS DETECTED: 0

CJM9AA.BIN,CJM9AA.LST/CRF/NL:TOC=CJM9AA.P11
RUN-TIME: 1 1 .1 SECONDS
RUN-TIME RATIO: 44/2=15.2
CORE USED: 7K (14 PAGES)