CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

The AD01-D (without options) employs a single high-speed analog-to-digital converter, a gain-selectable amplifier, and an input multiplexer to provide fast multichannel scanning, scaling, and conversion capability. Interface logic compatible with the PDP-11 Computer System is also included in the AD01-D to facilitate direct computer control of the subsystem. This subsystem is intended for use in applications where sampling and processing of analog data from sensors or other external sources is desired. Block and simplified diagrams of the AD01-D are contained in this chapter; detailed block and circuit schematics are included in Chapter 6.

4.2 BLOCK DIAGRAM ANALYSIS

Figure 4-1 is a detailed block diagram of the AD01-D, showing the multiplexer, the gain-selectable amplifier, A/D converter, interface and control logic, and available options. The AD01-D, connected to the Unibus along with other PDP-11 devices, remains dormant unless it is addressed. Two device addresses have been assigned to the AD01-D: One address (766770_8) is used to gain access to the control and status register (CSR); the other address (766772_8) is used to gain access to the data buffer register (DBR). Address Selector M105 recognizes these addresses (A 17:01) and generates clock and gating signals to move data into and out of the AD01-D registers. The mode control bits (C 1:0) and the byte control bit (A 00) determine which of the following clock or gating signals is to be generated by the M105 Address Selector:

a. CLOCK ADCSR WORD
b. CLOCK ADCSR LOW BYTE
c. CLOCK ADCSR HIGH BYTE
d. GATE ADCSR (word)
e. GATE ADDBR (word)

An A/D conversion can be initiated in three different ways:

a. Setting the START bit (ST bit 00) of the CSR by incrementing the CSR word or low byte. This action initiates a conversion of the channel and gain setting that has been established by a previous instruction.

b. Loading a new multiplex channel address into the CSR with a move high byte or word instruction.

NOTE

When the external clock is enabled (EE bit 01 is set), conversions are not started by loading a new channel address or gain setting. The START bit must be set to start the conversion under program control. This feature makes it possible to change gain and multiplex address between external clock pulses.

c. By an external clock. When the external clock is enabled (EE bit 01 is set), a move word instruction cannot be used to enable the external clock and select channel and gain at the same time. This would set the error bit (ER 15).

When a conversion is initiated by setting the START bit, a timing train is generated by the timing generator (see Figure 4-1). The sequence of the timing train and the timing intervals are:

1.	Check error	0.5 μs
2.	Check read	0.6 μs
3.	Hold (CONV H)	5.5 μs
4.	Convert (CONV L)	6.0 μs

The multiplex channel (MC) and GAIN SELECT (GS) bits of the CSR are decoded by the gain and channel decoder to select the programmed channel and gain. The check error pulse produced by the timing generator initializes (clears) the A812 A/D Converter. The Check Error pulse also causes the ERROR bit (ER bit 15) in the CSR to be set if the data of the previous conversion has not been gated out of the DBR. Setting the ERROR bit initiates an interrupt and a trap vector if the interrupt logic is enabled. The second pulse in the timing train, the hold command, causes the A405 Sample and Hold Module to acquire and hold the input analog voltage.

Finally, the Convert pulse is produced to start the A/D converter and set the RD flip-flop. The converter produces 10 output bits, which correspond to the amplitude of the input voltage. The successive (serial) approximation technique is used by the converter. When 10 output bits have been determined, the converter produces an A/D Done pulse to release the A405 Sample and Hold Module so that it will start tracking again and to set the DONE bit (DN bit 07) of the CSR. Setting the DONE bit initiates an interrupt and a trap vector if the interrupt logic is enabled. When a conversion is done, the converter, which serves as the DBR, retains the data word until a new conversion is started. However, if the data is not read before a new conversion is started, an error results. This action is accomplished by the RD flip-flop. Data is read out of the AD01-D simply by programming a move DBR word instruction. This instruction is recognized by the M105 Address Selector, which then generates an ADDBR gate. This gate enables the DBR output drivers to transfer the data onto the Unibus. The gate also resets the RD flip-flop to prevent the error from occurring on the next conversion. Normally, the move DBR word instruction is issued by the processor in response to an interrupt signal from the AD01-D.

As noted before, an interrupt is generated by the M782 Interrupt Control (if enabled) when an error occurs and when the conversion is done. The M782 Module also issues a trap vector (address 000130_8) to inform the processor that the AD01-D issued the interrupt. The processor responds to the interrupt by testing the DONE and ERROR bits of the CSR.

Subject to the result of the test, the program jumps to the move DBR word instruction or an error routine.

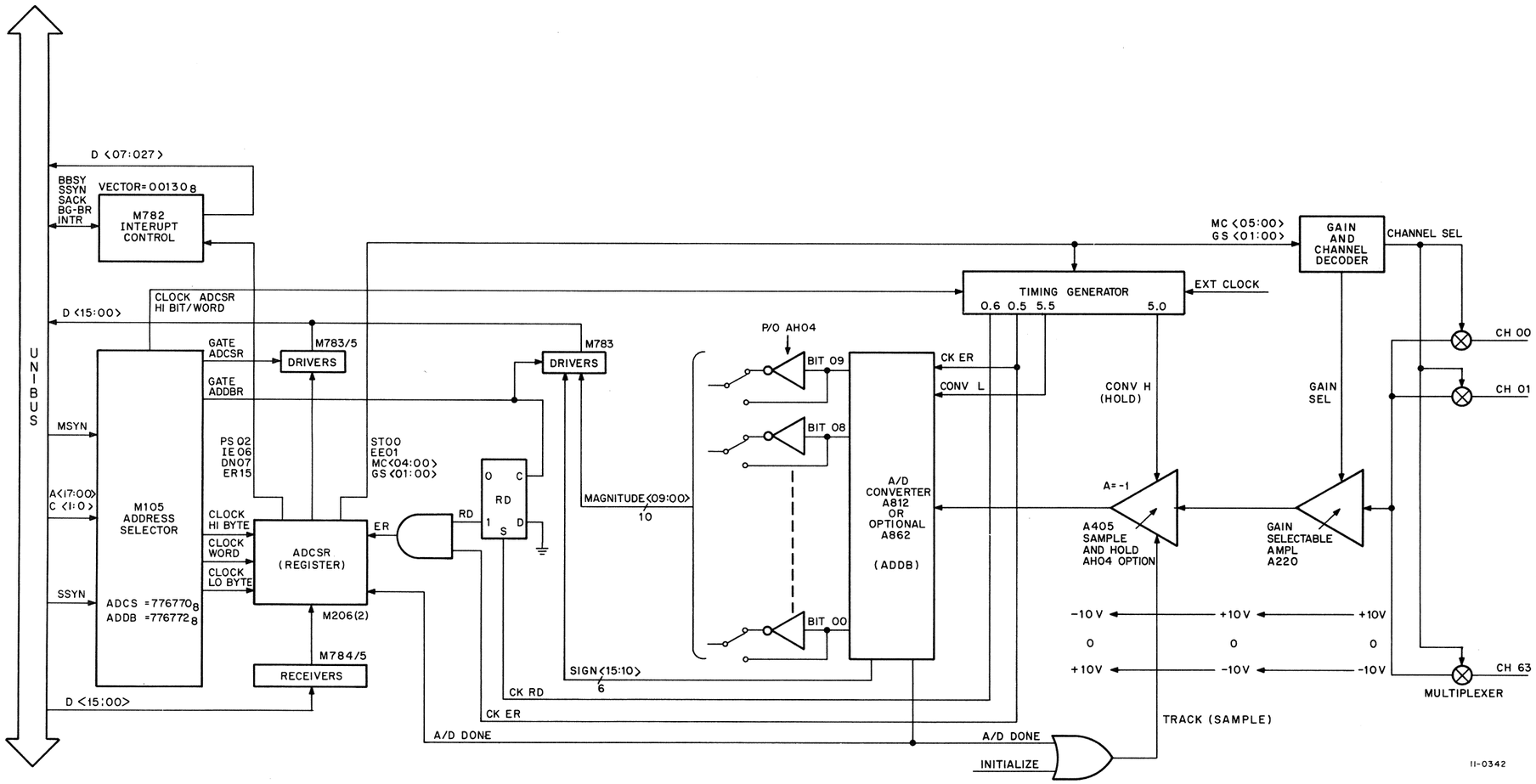

Figure 4-1 AD01-D Block Diagram

4.3 DETAILED CIRCUIT ANALYSIS

The two AD01-D options offer four unique configurations; the following description is organized to reflect these configurations. The order of presentation is as follows:

1. Multiplexer
2. Scaling Amplifier
3. A/D Conversion Configurations
4. Timing
5. Bus Interface

The four configurations accommodate unipolar or bipolar operation with a wide or narrow sampling aperture.

4.3.1 Multiplexer

The multiplexer (drawing D-BS-AD01-D-03) includes at least 4 channels and is expanded to 32 channels in 4-channel increments simply by adding additional A124 Multiplex Modules. The desired channel is selected by a binary decoder that decodes the 6-bit multiplex channel (MC) address received by the CSR. The three most significant bits of the address are decoded by the M161 Octal Decoder to select an A124 Multiplex Module and the two least significant bits of the address are decoded by logic in the multiplexer module itself to select one channel.

4.3.2 Scaling Amplifier

Scaling Amplifier A220 (drawing D-BS-AD01-D-05) provides the AD01-D with an extended dynamic range, the equivalent of up to 14 bits. The amplifier has program-selectable gains of X1, X2, X4, and X8 to achieve this range. The desired gain is selected by a binary decoder (in the associated A124 Module) that decodes the 2-bit gain code received by the CSR.

4.3.3 A/D Converter

The A/D conversion circuits may be configured four different ways using the AH05 Bipolar Option and the AH04 Sample and Hold Option (see Figure 2-1). The sample and hold option reduces the aperture of the AD01-D for skewless sampling applications.

4.3.3.1 **Unipolar with Wide Aperture** – This basic AD01-D configuration is capable of accurately converting unipolar analog voltages. The sampling aperture of this configuration is 17 μs. The configuration consists of the A812 A/D Converter Module and a specific jumper combination as described in Chapter 2. The operation of the A812 Converter is similar to the A811 A/D Converter described in the *Digital Logic Handbook.*

4.3.3.2 **Unipolar with Narrow Aperture** – A sampling aperture of 100 ns is obtained by installing AH04 Sample and Hold Option (see Figure 2-1). This configuration may be useful in analyzing frequency characteristics of unipolar signals or in signal averaging. Installation and calibration procedures are given in Chapter 2. The option consists of a single A405 Module, which is similar to the A404 Module described in the *Digital Logic Handbook.*

4.3.3.3 **Bipolar with Wide Aperture** – Bipolar Option AH05 provides the means for converting bipolar analog voltages. This option consists of a replacement A/D Converter Module (A862). The sampling aperture of this configuration is 24 μs. The converter has a 12-bit conversion capability, but only 11 bits, forming a 10-bit magnitude and 1-bit polarity, are used. The converter uses the successive approximation method in converting analog voltages. A detailed description of the A862 Converter is presented in the *Control Handbook.*

4.3.3.4 **Bipolar with Narrow Aperture** – The Sample and Hold Option (AH04) accommodates skewless sampling of bipolar analog voltages. The sample and hold option reduces the sampling aperture to 100 ns. Installation and calibration procedures are given in Chapter 2.

4.3.4 Timing

All timing pulses are produced by the timing generator circuits (see Figure 4-2) in response to the programmed control word or the external clock. The timing pulses that are produced by the timing generator circuits include the CK ER, CK RD, CONV H, and CONV L pulses. The function of each of these pulses in the A/D converter is described in Paragraph 4.2.

4.3.5 Bus Interface

The M105 Address Selector provides gating signals for up to four device registers. Only two device registers are used in the AD01-D; thus, only two of the select signals from the address selector are implemented. The address selector decodes the 18-bit bus address on A <17:00> to produce the gating signals for the device registers.

To deposit a whole control word into the CSR, both CLOCK ADSCR HIGH BYTE and CLOCK ADSCR LOW BYTE signals are generated at the same time. For more detailed description of the M105 Address Selector Module, refer to the *Digital Logic Handbook* or *PDP-11 Handbook.* The 16-bit CSR and DBR data words are carried on D <15:00> and are gated into and out of the AD01-D registers under control of the gating signals produced by the address selector output logic in response to the programmed instruction. A program-controlled conversion is started simply by depositing a control word or high byte into the CSR, or by incrementing the low byte which sets the START bit (ST00) of the CSR. If the external clock bit (EE01) is reset, all three specified operations activate the timing generator to initiate the conversion. When conversion is complete, the START bit (ST00) is reset and the DONE bit (DN07) is set by the A/D DONE signal. Before a new conversion can be initiated, the data must be read out of the DBR; otherwise, the CSR ERROR bit (ER15) will be set. The ERROR bit is set by the check error (CK RD) signal if the RD flip-flop is not reset by reading the data out of the DBR. The RD flip-flop is set by the CONV signal when the conversion is started, and the CK RD signal is produced each time a conversion is started. Therefore, if another conversion is started before the DBR is read, both RD and CK RD will be high, causing the ERROR bit of the CSR to be set.

The same principles discussed above apply to conversions initiated by an external clock. To effect conversions under external clock control, the external clock enable bit (EE01) of the CSR must be set.

Figure 4-3 illustrates the interrupt logic of the AD01-D. Most of the interrupt logic is contained in the M782 Interrupt Control Module. The interrupt logic allows the AD01-D to request and gain access to the Unibus on a priority basis. There are only two conditions for which the AD01-D may require use of the Unibus: in the event of an error (CSR bit ER15 is set), or when one conversion is done (CSR bit DN07 is set). Before the interrupt logic can request use of the Unibus, the CSR interrupt enable bit (bit IE06) must be set to enable the interrupt logic. Two levels of priority are available to the AD01-D: level 7 and level 4, 5, or 6 as established by Jumper Module G736. Either level can be selected under program control simply by changing the state of the priority select bit (CSR bit PS02). With bit PS02 reset, master control A of the M782 Module is enabled to issue a bus request of the highest priority (BR7). Master control B is enabled to issue a lower priority request (BR4, 5, or 6) when the bit PS02 is set. Setting the DONE or ERROR bits of the CSR activate the enabled master control to issue a bus request. Priority permitting, the processor relinquishes the bus to the AD01-D by issuing a bus grant (BG) signal.

In response to the bus grant signal, the interrupt control of the M782 issues an interrupt command. The vector address of the words in memory contain the address and status of the appropriate device service routine.

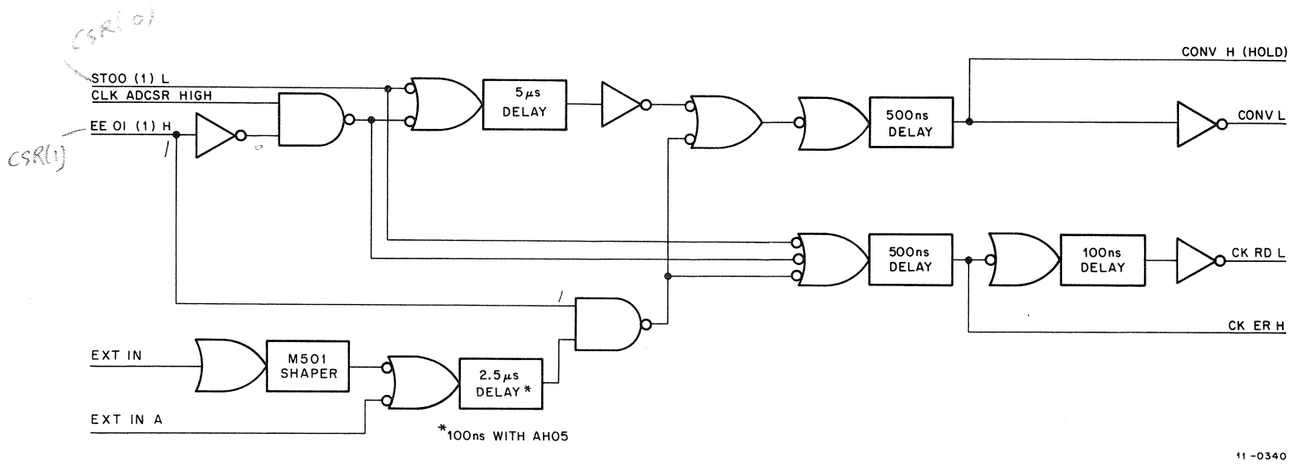

Figure 4-2 Timing Generator Circuit

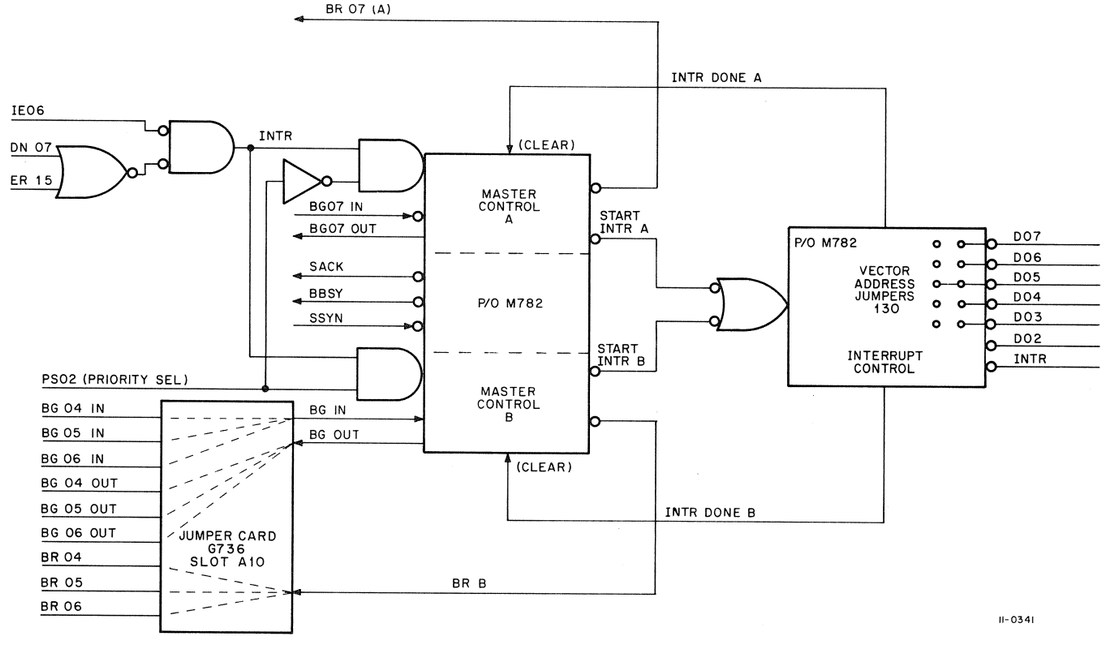

Figure 4-3 AD01-D Interrupt Logic

CHAPTER 5
MAINTENANCE

When operated under normal conditions, the AD01-D Analog Subsystem requires little maintenance (periodic performance of diagnostic programs, cleaning, and inspection). If preventive maintenance is required, follow the procedures outlined in this chapter to return the equipment to maximum operating efficiency.

If a module requires replacement, refer to the spare parts list outlined in this chapter. Do not replace a faulty component without first determining the cause of the failure. Refer to the block schematics associated with each module to determine the location of the components in question.

When conducting a maintenance analysis of the system, make certain that the input conditions required to produce a specified output are met; otherwise, erroneous output readings will result, indicating a nonexisting fault.

5.1 AD01-D MAINDEC-11-D6AB DIAGNOSTIC PROGRAM

The AD01-D diagnostic program is used to test the unique hardware features of the system that cannot be tested with existing MainDEC programs. The program is designed to facilitate troubleshooting by selectively exercising circuits in the AD01-D. Instructions and procedures for loading, operating, and interpreting the results of diagnostic tests are written in clear, concise language for beginning maintenance personnel.

The program tests are divided into the following nine separate tests.

a. **Normal Instruction Tests** – This test consists of 42 subtests that completely checkout the AD01-D logic. Each subtest may be looped 2048 times for reliability.

b. **Conversion Averaging** – This is done with 2 subroutines, CONAV and CONVRT, which together average 128 conversions. SW10=1 inhibits calling these subroutines.

c. **DSPLAY (Display Conversion)** – This routine reads the switch register for channel and gain, performs a corresponding conversion, and displays the result in the data indicators. Thus, calibration can be readily performed, and all channels and gain can be checked directly.

d. **EXTEST (External Conversion Test)** – This routine counts external conversions and prints out after every tenth conversion. It also allows checking for various error cases involving external conversions.

e. **EXFAST (Fast External Conversion Test)** – This routine enables external conversions and checks the error bit after each conversion. An error will occur when the external conversion signal occurs faster than the maximum possible throughput.

f. **FLY (Conversion Print Loop)** – This routine continuously prints the results of conversions at the gain and channel set in the switches. The average of 128 conversions is printed unless SW10 is set. If SW10 is set, the results of single conversions are printed.

g. **TESTX (Single Test Loop)** – This routine allows a single subtest to be run continuously for scope loop purposes. While a scope loop switch option exists, it requires that the user be within the test in which he wishes to loop; in some cases (such as with intermittent failures) that is not easy to do. This subroutine allows the user to load the address of any test from test 0 through test 40 at the halt and then go directly to that test.

h. **WAS-IS (Multiplexer Status, Selection, and Repeatability Test)** – This routine stores an initial conversion value for each channel in the initial table (ITABLE). This initial value is either the average of 128 conversions or the result of a single conversion, depending on the setting of SW10. A single conversion is then taken on each channel and stored in OTABLE (OLD TABLE). From that point, sets of one conversion for each channel are taken and stored in NTABLE (NEW TABLE). OTABLE and NTABLE are compared for ±1 LSB agreement (unless SW9 is set, in which case they must agree exactly; errors are printed out in a CHANNEL XX WAS YYYYYY, is ZZZZZZ format. After the comparison, OTABLE is updated with NTABLE and the process is repeated. If SW5 is set, eight comparisons are made on each channel before going to the following channel. Whenever SW6 is set, a comparison of ITABLE and NTABLE is printed out, which allows drift to be checked. If SW7 is set, NTABLE is compared with ITABLE instead of OTABLE. The bell is rung after every 4096 passes.

i. **SIGMA1 (Repeatability Specification Test)** – This routine tests repeatability to specifications on the channels desired at gains of 4 and 8. Ten thousand conversions are taken at each gain. The specifications have been interpreted to mean that 35 conversions out of the ten thousand may be outside of 2 states at a gain of 4, and the 35 conversions out of ten thousand may be outside of 3 states at a gain of 8.

At a gain of 4, the first 128 conversions are averaged. Then, ten thousand conversions are made, and each is compared to the average. If it is equal to the average, EQUAL is incremented. If it is one less than the average, UNDER is incremented. If it is farther from the average than one count, OUT is incremented. At the end of the ten thousand conversions, a check is made to determine the 2 allowed states (either equal and over or equal and under). The total for the other state (either over or under) is then added to the location OUT. If this total (OUT) is now greater than 35 (DECIMAL), the test fails. The distribution printed out with SW6 or SW7 up is this final setup – the number equal to the average, the number one less than the average, the number one greater than the average, and the total of those differing by more than one count plus those in the nonallowed state.

At a gain of 8, the first 128 conversions are averaged. Then, ten thousand conversions are made, and each is compared to the average. If it is within plus or minus one of the average, EQUAL is incremented. If not, OUT is incremented. At the end of ten thousand conversions, if more than 35 were outside of the 3 allowed states the test fails. The distribution printed out with SW6 or SW7 up is simply the number that were within the 3 states and the number outside of 3 states.

5.2 PREVENTIVE MAINTENANCE

A systematic preventive maintenance program is a useful tool to avert system failures. Proper application of a preventive maintenance program is an aid to both serviceman and user, because detection and prevention of probable failures substantially reduces maintenance and downtime.

Scheduling of computer usage should always include time for maintenance. Careful diagnostic testing can indicate problems that may only occur intermittently during on-line operation.

Weekly program checks and thorough preventive maintenance should be followed, based on the following criteria:

electrical:	1000 hours
mechanical:	500 hours

or at least quarterly.

5.2.1 Preventive Maintenance Tasks

Step	Procedure
1	Clean the exterior and interior of the equipment cabinet using a vacuum cleaner, air blower, or a brush with long soft bristles, and/or cloths moistened in nonflammable solvent. If an air hose is used for cleaning, do not disturb components or wiring.
2	Lubricate hinges, slide mechanisms, and casters, with a light machine oil. Wipe off excess oil.
3	Visually inspect equipment for general condition. Repaint any scratched area with DEC black paint or Krylon Glossy white no. 1501.
4	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
5	Inspect the following for mechanical security: keys, switches, control knobs, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
6	Inspect all module mounting panels to ensure that each module is securely seated in its connector. Remove and clean any module that may have collected dirt or dust due to improper air filter service.
7	Inspect power supply components for leaky capacitors, overheated resistor, etc. Replace any defective components.
8	Check the output voltages and ripple contents of the power supply as specified in Paragraph 2.6. Use a multimeter to make these measurements without disconnecting the load. Use an oscilloscope to measure p-p ripple on all dc outputs of the supply. The outputs of the supplies are adjustable; therefore, if any output voltages are not attainable, initiate power supply maintenance. Refer to the block schematic associated with the power supply in question. If ripple content is not within specifications, the power supply is considered defective, and corrective maintenance should be performed.
9	Run AD01-D programs to verify proper equipment operation.
10	Enter preventive maintenance results in a log book.
11	Vibrate the modules and wiring panels, while running the diagnostics.
12	Check all analog adjustments, while running the diagnostics.

5.3 CORRECTIVE MAINTENANCE

The AD01-D Analog Subsystem is constructed of highly reliable modules. The reliability of these circuits, in conjunction with performance of the preventive maintenance tasks, ensures relatively little equipment downtime due to failure. If a malfunction occurs, maintenance personnel should analyze the condition and correct as indicated in the following paragraphs.

The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the equipment. Persons responsible for maintenance should become thoroughly familiar with the system concept, the block schematics, the operation of specific module circuits, and the location of mechanical and electrical components. Diagnosis and remedial action for a faulty condition can be undertaken logically and systematically in the following phases:

a. Preliminary Investigation
b. System Troubleshooting
c. Logic Troubleshooting
d. Circuit Troubleshooting
e. Repair/Replacement
f. Validation Tests
g. Recording

5.3.1 Preliminary Investigation

Before commencing troubleshooting procedures, explore every possible source of information. Analyze the problem before attempting to troubleshoot the system. Gather all available information from users who have encountered the problem, and check the system log book for any previous references to the problem.

Do not attempt to troubleshoot using complex system programs alone. Run the AD01-D MainDEC-11-D6AB Diagnostic program and select the shortest, simplest program available that exhibits the error conditions.

5.3.2 System Troubleshooting

When the problem is understood and the proper program has been selected, the logic section of the system at fault should be determined. Obviously, the program that has been selected gives a reasonable idea of what section of the system is failing. However, faults in equipment that transmit or receive information, or improper connection of the system, frequently give fault indications similar to those caused by computer malfunctions.

5.3.3 Logic Troubleshooting

Before attempting to troubleshoot the logic, make certain that proper and calibrated test equipment is available. Always calibrate the vertical preamp and probes of an oscilloscope before using. Ensure that the oscilloscope has a good ac ground and keep the dc ground from the probe as short as possible. Use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep can be synchronized by control pulses or by level transitions that are available on individual module terminals at the wiring side of the logic.

CAUTION

When probing the logic, do not short between pins. Shorting of signal pins to power supply pins may result in damage to components.

5.3.4 Circuit Troubleshooting

Engineering schematic diagrams of each module used in the AD01-D are available; refer to these diagrams for detailed circuit information.

Visually inspect the module on the component side and the printed wiring side to check for overheated or broken components or etch. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

To avoid damaging components, do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested.

Measure the forward and reverse resistances of diodes; diodes should measure approximately 20Ω forward and more than 1000Ω reverse. If readings in each direction are the same and no parallel paths exist, replace the diode.

Measure the emitter-collector, collector-base, and emitter-base resistances of transistors in both directions. Short circuits between collector and emitter, or an open circuit in the base-emitter path, cause most failures. A good transistor indicates an open circuit in both directions between collector and emitter. Normally 50Ω to 100Ω resistance exists between the emitter and the base, or between the collector and the base in the forward direction, and an open circuit condition exists in the reverse direction. To determine forward and reverse directions, consider a transistor as two diodes connected back to back. In this analogy, PNP transistors would have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors, the base would be a common-anode connection, and both the emitter and collector, the cathode.

Multimeter polarity must be checked before measuring resistance, because many meters apply a positive voltage to the common lead when in the resistance mode.

Because integrated circuits (ICs) contain complex integrated circuits with only the input, output, and power terminals available, static multimeter testing is limited to continuity checks for shorts between terminals. IC checking is best accomplished under dynamic conditions using a module extender to make terminals readily accessible. Using AD01-D block schematics and module schematics, proceed as follows to locate an IC on a circuit board:

Step	Procedure
1	Hold the module with the handle in your left hand with the component side facing you.
2	ICs are numbered starting at the contact side of the board, upper right-hand corner.
3	The numbers increase toward the handle.
4	When a row is complete, the next IC is located in the next row at the contact end of the board (see Figure 5-1).
5	The pins on each IC are located as illustrated in Figure 5-2.

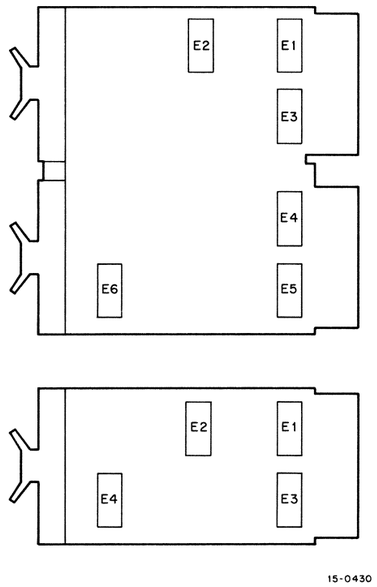

Figure 5-1 IC Location

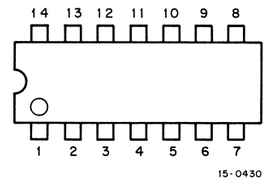

Figure 5-2 IC Pin Location

5.3.5 Validation Tests

Return repaired modules to the location from which they were removed. If a defective module is replaced by a new module while repairs are being made, tag the defective module and note the location from which it was taken and the nature of the failure. When repairs are completed, return the repaired module to its original location, and confirm that the repairs have resolved the problem by running all tests that originally exhibited the problem.

NOTE

If modules have been moved during the troubleshooting period, return all modules to their original positions before running the validation tests.

5.3.6 Recording

Maintain a log book (supplied) of AD01-D failures and corrective maintenance. All maintenance should be recorded in this book. Record all data indicating the symptoms of the fault, the method of fault detection, the component at fault, and any comments that would be helpful in maintaining the equipment in the future.

The log should be maintained on a daily basis, recording all operator usage and corrective maintenance results.

5.4 TEST EQUIPMENT

To service the AD01-D Analog Subsystem, the equipment listed in Table 5-1 is recommended. If recommended equipment is not available, alternate equipment with the same performance specifications should be used.

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
Voltage Standard (EDC)	Electronic Development Corporation	MV-100 (or equivalent)
10:1 Divider	DEC	No. 29-16810
Digital Voltmeter	Hewlett Packard	HP-3460 (or equivalent)
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453 (or equivalent)
Probe (2)	Tektronix	P6010
X10 Probe (2)	Tektronix	P6008
Module Extender (2)	DEC	W982
Multiplexer Checkout Module	DEC	G735

5.5 MODULE HANDLING AND REPAIR

To insert or extract modules, first turn off all power. To gain access to components on a module, remove the module by exerting a straight, even pull on the module handle to prevent twisting of the printed-wiring board. Insert a type W982 Flip-Chip Module extender into the vacated module mounting panel, then insert the module into the extender. Use two W982 Extender Modules for dual modules.

Do not attempt to repair, adjust, or calibrate the A862 and A812 Analog-to-Digital Converter modules except as noted in the Acceptance and Calibration procedure (A-SP-AD01-12 and 11).

NOTE

Failure to follow this rule may violate the warranty.

5.6 SPARE PARTS

The customer should maintain a spare parts inventory of those modules listed in Table 5-2.

Table 5-2
Spare Parts List

Type/Part No.	Name	Quantity
A124	Four-Input Multiplexer Switch	1
A124*	Four-Input Multiplexer	1
A220	Selectable Gain Buffer Amplifier	1
A862 (AH05)*	Bipolar A/D Converter	1
A405 (AH04)*	Sample and Hold	1
A708	Dual Voltage Regulator	1
A812	10-Bit A/D Converter	1
G736	Request Jumper	1
M105	Address Selector	1
M111	Inverter	1
M112	NOR Gate	1
M113	10 2-Input NAND Gates	1
M161	Binary to Octal/Decimal Decoder	1
M206	Six Flip-Flops	1
M302	Dual Delay Multivibrator	1
M501	Schmitt Trigger	1
M617	6 4-Input NOR Buffers	1
M782	Interrupt Control	1
M783	Unibus Drivers	1
M784	Unibus Receivers	1
M785	Unibus Transceivers	1
M908	Connector	1

*Denotes optional modules.

CHAPTER 6
ENGINEERING DRAWINGS

This chapter contains a listing of DEC block schematics and cabling diagrams which are referenced in other chapters of this maintenance manual and are contained in Volume II of this manual. These drawings provide detailed information about the logic and wiring of the AD01-D peripheral.

Table 6-1
AD01-D Subsystem

Drawing Number	Title
A-ML-AD01-DA	10 Bit ADC with Switch Gain (AD01-DA)
D-UA-AD01-0	10 Bit ADC with Switched Gain
A-PL-AD01-D-0	10 Bit ADC with Switched Gain (Parts List)
D-DI-AD01-D-1	Drawing Index List (AD01-D)
D-AD-7006919-0-0	Wired Assembly (AD01-D)
A-PL-7006919-0-0	Wired Assembly (Parts List) (AD01-D)
D-MU-AD01-D-02	Module Utilization (AD01-D)
A-PL-AD01-D-02	Module Utilization (Parts List) (AD01-D)
D-BS-AD01-D-03	Multiplexer
D-BS-AD01-D-04	Interface and CSR
D-BS-AD01-D-05	A/D Converter
D-IC-AD01-D-06	Analog Input Connectors
D-IC-AD01-D-09	Bus Connector
D-IC-AD01-D-15	Analog Input Connector (LAB-11)
K-WL-AD01-D-0 (Complete)	Wire List (AD01-D)
A-AL-AD01-D-8	Accessory List

Table 6-1 (Cont)
AD01-D Subsystem

Drawing Number	Title
A-SP-AD01-D-10	Engineering Specifications
A-SP-AD01-D-12	Acceptance Procedure
A-ML-AH04-0	Sample and Hold Option AH04
A-PL-AH04-0-0	Sample and Hold (Parts List)
C-CS-A405-0-1	Sample and Hold
A-ML-AH05-0	One Bit Extender for AD01
A-PL-AH05-0-0	One Bit Extender for AD01 (Parts List)
D-CS-A862-0-1	11 Bit A/D Converter with Sign
D-CS-A812-0-1	A/D Converter
C-UA-H727-A-0	H727-A Power Supply, 115V
C-UA-H727-B-0	H727-B Power Supply, 230V
D-UA-H716-B-0	H716-B Power Supply, 115V
D-UA-H716-D-0	H716-D Power Supply, 230V

APPENDIX A
10–BIT UNIPOLAR CALIBRATION CHART

Date:
Serial No:

AD91-D
10 Bit Unipolar
CALIBRATION CHART

Switching Point		Gain=1 ±10 mV ±12.5 mV W/AH04		Gain=2 ±5 mV ±6.25 mV W/AH04		Gain=3 ±2.5 mV ±3.12 mV W/AH04		Gain=4 ±1.25 mV ±1.56 mV W/AH04	
From	To	Theor. Voltage	Actual Voltage	Thoer. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage
000000	000001	0.0049		0.0029		0.0012		0.0006	
000001	000002	0.0146		0.0073		0.0036		0.0018	
000003	000004	0.0342		0.0171		0.0085		0.0043	
000004	000005	0.0439		0.0220		0.0110		0.0055	
000007	000010	0.0732		0.0366		0.0183		0.0091	
000010	000011	0.0829		0.0415		0.0207		0.0104	
000017	000020	0.1514		0.0757		0.0378		0.0189	
000020	000021	0.1611		0.0806		0.0403		0.0201	
000037	000040	0.3076		0.1538		0.0769		0.0385	
000040	000041	0.3173		0.1587		0.0793		0.0397	
000076	000077	0.6103		0.3051		0.1526		0.0763	
000077	000100	0.6201		0.3101		0.1550		0.0775	
000100	000101	0.6298		0.3149		0.1575		0.0787	
000176	000177	1.2353		0.6177		0.3088		0.1544	
000177	000200	1.2451		0.6226		0.3113		0.1556	
000200	000201	1.2549		0.6274		0.3137		0.1569	
000376	000377	2.4853		1.2427		0.6213		0.3107	
000377	000400	2.4951		1.2476		0.6238		0.3119	
000400	000401	2.5049		1.2524		0.6262		0.3131	
000776	000777	4.9853		2.4927		1.2463		0.6232	
000777	001000	4.9951		2.4976		1.2488		0.6244	
001000	001001	5.0049		2.5024		1.2512		0.6256	
001376	001377	7.4853		3.7427		1.8713		0.9357	
001377	001400	7.4951		3.7476		1.8738		0.9369	
001400	001401	7.5049		3.7524		1.8762		0.9381	
001576	001577	8.7353		4.3677		2.1838		1.0919	
001577	001600	8.7451		4.3726		2.1863		1.0931	
001600	001601	8.7549		4.3774		2.1887		1.0944	
001775	001776	9.9756		4.9878		2.4939		1.2470	
001776	001777	9.9853		4.9927		2.4963		1.2482	

APPENDIX B
11–BIT BIPOLAR CALIBRATION CHART

Date:
Serial No:

AD01-D
11 Bit Bipolar
CALIBRATION CHART

Switching Point		Gain=1 ±10 mV ±12.5 mV W/AH04		Gain=2 ±5 mV ±6.25 mV W/AH04		Gain=4 ±2.5 mV ±3.125 mV W/AH04		Gain=8 ±1.25 mV ±1.56 mV W/AH04	
From	To	Thoer. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage	Thoer. Voltage	Actual Voltage	Theor. Voltage	Actual Voltage
001777	001776	9.9853		4.9926		2.4963		1.2482	
001776	001775	9.9756		4.9878		2.4939		1.2470	
001001	001000	5.0049		2.5024		1.2512		0.6256	
001000	000777	4.9951		2.4976		1.2488		0.6244	
000777	000776	4.9853		2.4937		1.2463		0.6232	
000601	000600	3.7549		1.8774		0.9387		0.4694	
000600	000577	3.7451		1.8726		0.9363		0.4681	
000201	000200	1.2549		0.6274		0.3137		0.1569	
000200	000177	1.2451		0.6226		0.3113		0.1556	
000021	000020	0.1611		0.0806		0.0403		0.0201	
000020	000017	0.1514		0.0757		0.0378		0.0189	
000004	000003	0.0342		0.0171		0.0085		0.0043	
000003	000002	0.0244		0.0122		0.0061		0.0030	
000002	000001	0.0146		0.0073		0.0036		0.0018	
000001	000000	0.0049		0.0024		0.0012		0.0006	
000000	177777	–0.0049		–0.0024		–0.0012		–0.0006	
177777	177776	–0.0146		–0.0073		–0.0036		–0.0018	
177776	177775	–0.0244		–0.0122		–0.0061		–0.0030	
177775	177774	–0.0342		–0.0171		–0.0085		–0.0043	
177750	177747	–0.2393		–0.1196		–0.0598		–0.0299	
177747	177746	–0.2490		–0.1245		–0.0623		–0.0312	
177600	177577	–1.2549		–0.6274		–0.3137		–0.1569	
177577	177576	–1.2647		–0.6324		–0.3162		–0.1581	
177001	177000	–4.9951		–2.4976		–1.2488		–0.6244	
177000	176777	–5.0049		–2.5024		–1.2512		–0.6256	
176777	176776	–5.0147		–2.5074		–1.2537		–0.6269	
176300	176277	–8.1299		–4.0649		–2.0325		–1.0162	
176277	176276	–8.1396		–4.0698		–2.0349		–1.0175	
176003	176002	–9.9756		–4.9878		–2.4939		–1.2470	
176002	176001	–9.9853		–4.9926		–2.4963		–1.2482	