PIN	D1	D2	C1	C2	B1	B2	A1	A2
A		+15V		+5V		+5V		+5V
B		-15V		-15V		-15V		-15V
C	GND	GND	GND	GND	GND	GND	SP*GND	GND
D	MA8 L	IRØ L	IO PAUSE L	TP1 H	MA4 L	INT STB H	MAØ L	EMAØ L
E	MA9 L	IR1 L	CØ L	TP2 H	MA5 L	BRK PROG L	MA1 L	EMA1 L
F	GND	GND	GND	GND	GND	GND	GND	GND
H	MA1Ø L	IR2 L	C1 L	TP3 H	MA6 L	MA,MS LD L	MA2 L	EMA2 L
J	MA11 L	F L	C2 L	TP4 H	MA7 L	OVERFLOW L	MA3 L	MEM START L
K	MD8 L	D L	BUS STB L	TS1 L	MD4 L	BRK DA CT L	MDØ L	MD DIR L
L	MD9 L	E L	INT I/O L	TS2 L	MD5 L	BRK CYC L	MD1 L	SOURCE H
M	MD1Ø L	USR MD H	N L XFR L	TS3 L	MD6 L	LA EN. L	MD2 L	STROBE H
N	GND	GND	GND	GND	GND	GND	GND	GND
P	MD11 L	F SET L	INT RQST L	TS4 L	MD7 L	INT PROG H	MD3 L	INHIBIT H
R	DATA 8 L	PULSE LA H	INIT. H	LNK DATA L	DATA 4 L	RES 1 H	DATA Ø L	RETURN H
S	DATA 9 L	STOP L	SKIP L	LNK LOAD L	DATA 5 L	RES 2 H	DATA 1 L	WRITE H
T	GND	GND	GND	GND	GND	GND	GND	GND
U	DATA 1Ø L	KEY CTRL L	CPMA DIS L	IND 1 L	DATA 6 L	RUN L	DATA 2 L	ROM ADDR L
V	DATA 11 L	SW L	MS,IR DIS L	IND 2 L	DATA 7 L	POWER OK H	DATA 3 L	LINK L

Blank pins are not interconnected on the bus but may be test points on individual modules.

* This pin is connected to GND on the bus but serves as a logic signal within modules to facilitate testing.

OMNIBUS PIN ASSIGNMENTS

MODULE CONTACT DESIGNATORS