11/34 PARS

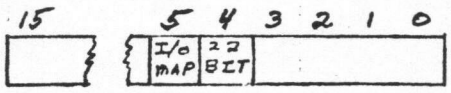
I/O ADDRESS	NAME	PRESET RANGE			
772356	KISAR7	124-128K	76 XXXX	I/O PAGE	
772354	KISAR6	120-124K	74 XXXX	KERNEL I SPACE	
772352	KISAR5	116-120K	72 XXXX		
772350	KISAR4	112-116K	70 XXXX		
772346	KISAR3	108-112K	66 XXXX		
772344	KISAR2	104-108K	64 XXXX		
772342	KISAR1	100-104K	62 XXXX		
772340	KISAR0	96-100K	60 XXXX		
777656	UISAR7	92-96K	56 XXXX	USER I SPACE	
777654	UISAR6	88-92K	54 XXXX		
777652	UISAR5	84-88K	52 XXXX		
777650	UISAR4	80-84K	50 XXXX		
777646	UISAR3	76-80K	46 XXXX		
777644	UISAR2	72-76K	44 XXXX		
777642	UISAR1	68-72K	42 XXXX		
777640	UISAR0	64-68K	40 XXXX		
		60-64K	36 XXXX		
		56-60K	34 XXXX		
		52-56K	32 XXXX		
		48-52K	30 XXXX		
		44-48K	26 XXXX		
		40-44K	24 XXXX		
		36-40K	22 XXXX		
		32-36K	20 XXXX		
		124-128K*			
		24-28K	14 XXXX	MMU OFF	
		20-24K	12 XXXX		
		16-20K	10 XXXX		
		12-16K	06 XXXX		
		8-12K	04 XXXX		
		4-8K	02 XXXX		
		0-4K	00 XXXX		

UNMAPPED

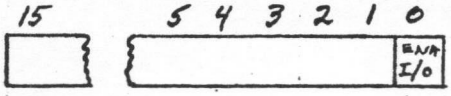
* APPEARS THE SAME AS MAPPED KERNEL PAR 7

ENABLE PARS

NAME	I/O ADDRESS
KISAR7'	763736
KISAR6'	763734
KISAR5'	763732
KISAR4'	763730
KISAR3'	763726
KISAR2'	763724
KISAR1'	763722
KISAR0'	763720
UISAR7'	763716
UISAR6'	763714
UISAR5'	763712
UISAR4'	763710
UISAR3'	763706
UISAR2'	763704
UISAR1'	763702
UISAR0'	763700
	763776
	763774
	763772
	763770
	763766
	763764
	763762
	763760
EPAR7	763756
EPAR6	763754
EPAR5	763752
EPAR4	763750
EPAR3	763746
EPAR2	763744
EPAR1	763742
EPAR0	763740



SR3' 763676



SR4 763674

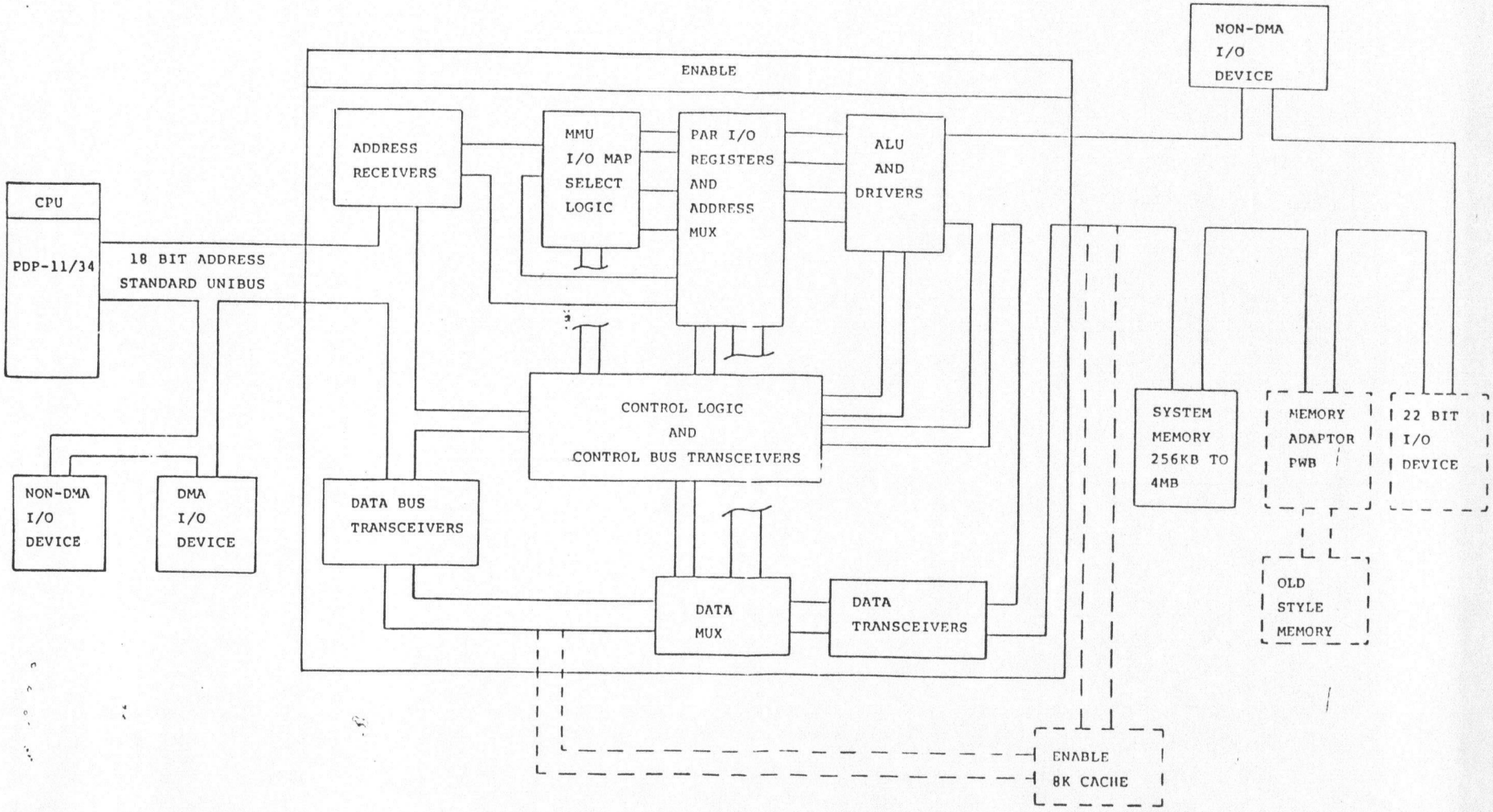


Figure 1: EnABLE Block Diagram

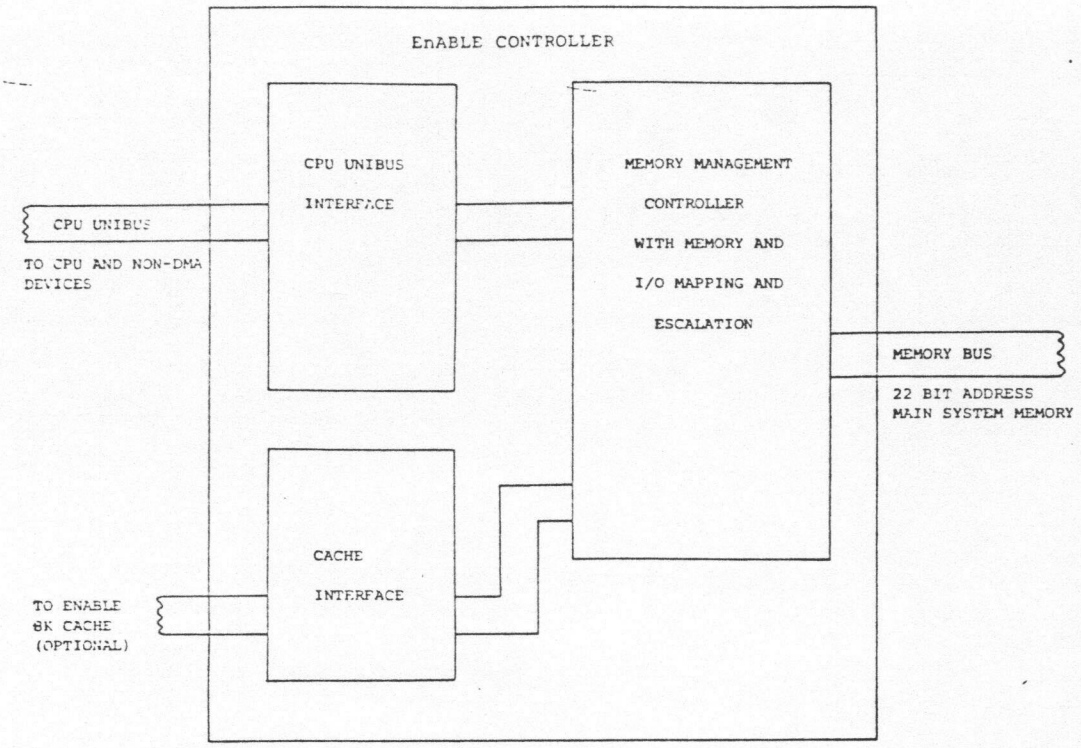


Figure 2: EnABLE Controller Block Diagram

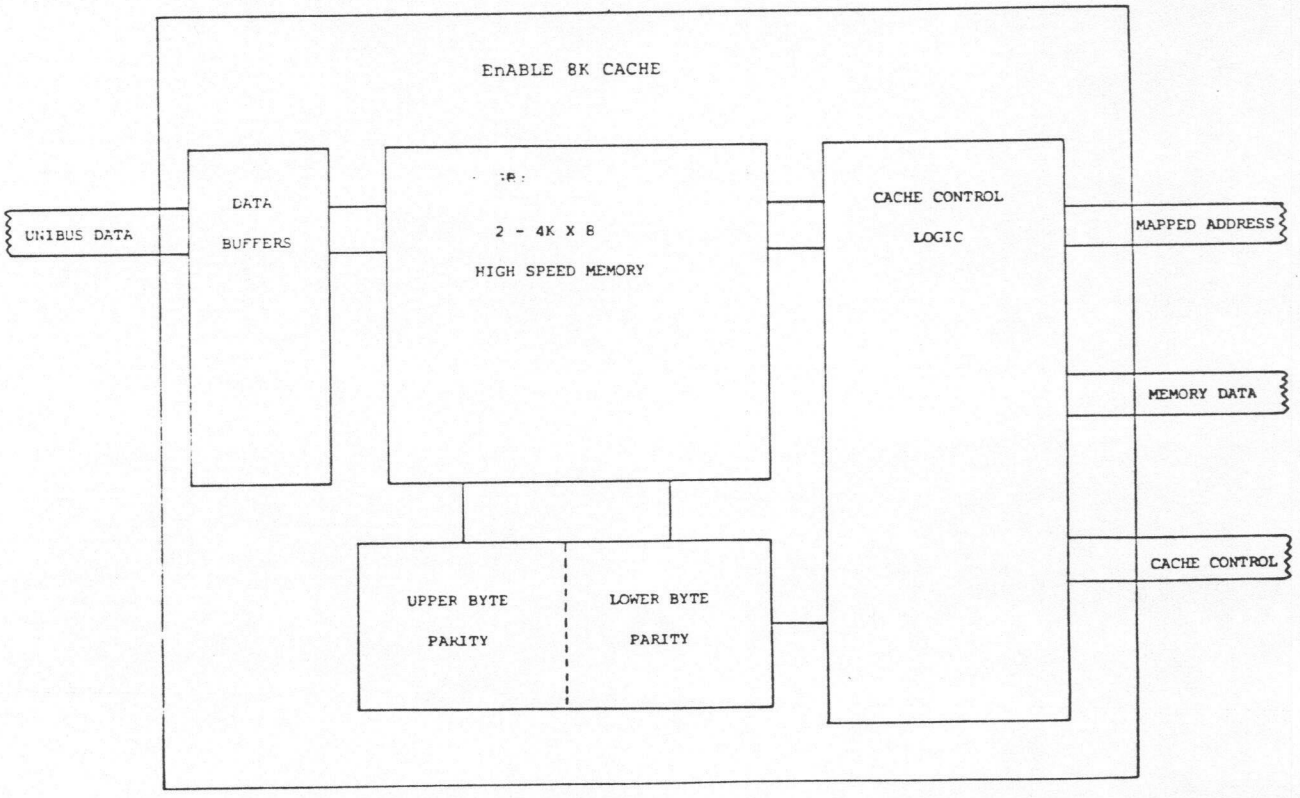


Figure 3: EnABLE 8K Cache Block Diagram

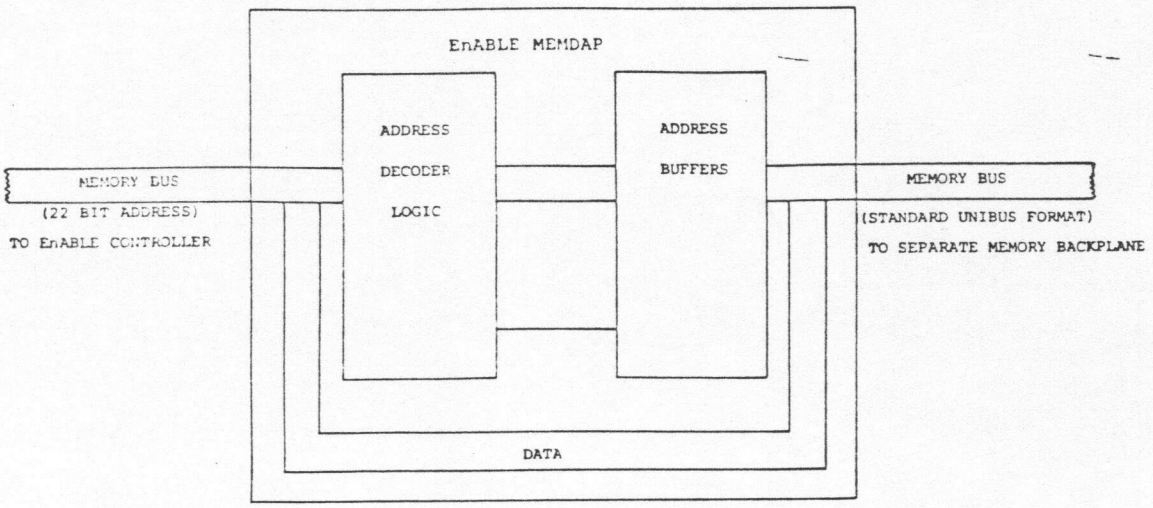


Figure 4: EnABLE Memdap Block Diagram

Features

- Increases direct memory addressing from the existing 256K bytes maximum to 4M bytes in increments of 256K bytes per PWB with on-board parity.
- Cache size is 8K bytes.
- Allows for the use of 128K bytes of existing memory and the associated parity modules.

Specifications

Controller board.

The controller requires 4.3 amps @ +5VDC ±0.25VDC. It derives the necessary power from the backplane into which it plugs. The controller appears to other devices equivalent to one bus load.

The EnABLE controller is configured on a modified hex-width board which plugs into the second slot of a dedicated, standard Unibus backplane. See Figure 5.

Timing: MSYN to mem MSYN: 92ns, typical; 110ns, maximum
Cache access: 110ns maximum

Switch Operation: The EnABLE controller PWB assembly is equipped with two toggle switches located in the upper left corner of the board. See Figure 5.

For diagnostic routines, the EnABLE disable switch disables the entire mapping function of EnABLE. When the handle is positioned towards the center of the board, the switch is in the "ON" position. (EnABLE is functional under software control. See SR3 description.) The switch is in the "OFF" position when the handle is towards the outside edge of the board, and all Unibus addressing (18 and 16 bit) passes unaltered through EnABLE to memory of other devices behind EnABLE.

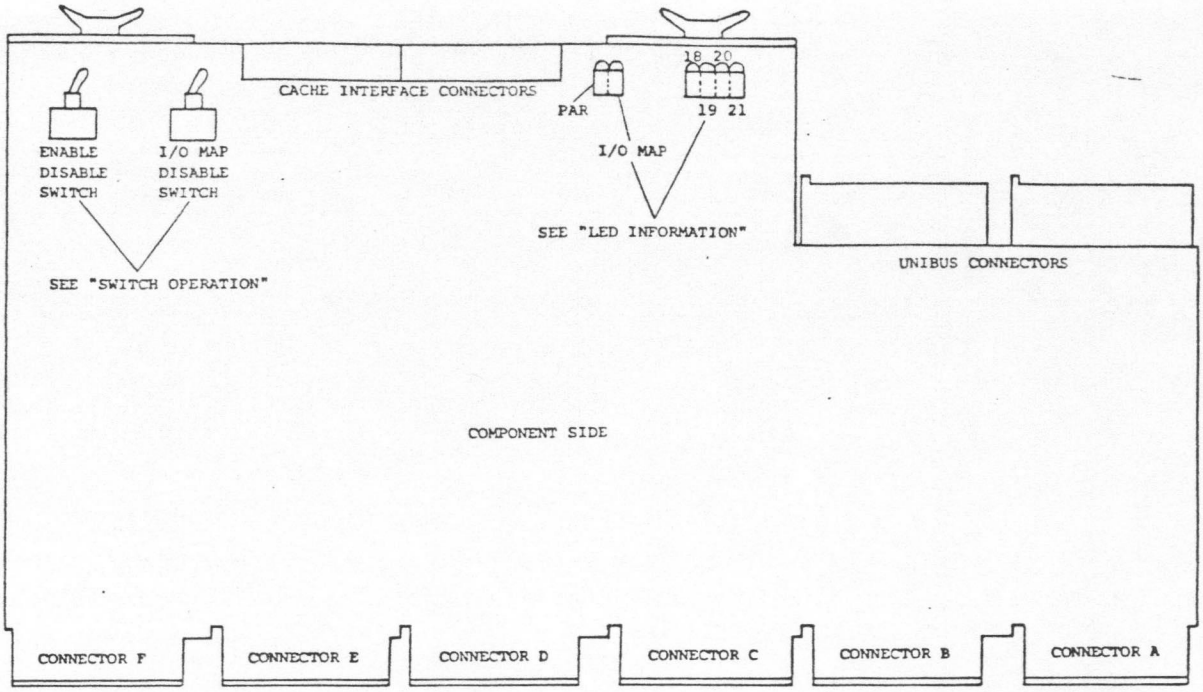


Figure 5: EnABLE Controller PWB Assembly

The I/O map disable switch allows the use of I/O devices located behind EnABLE on the 22 bit memory bus. A separate I/O map must be used when utilizing this system configuration. The switch is in the "ON" position when the handle is towards the center of the PWB. (EnABLE I/O map is functional under software control. See SR3 description.)

LED Information: The EnABLE controller board is equipped with 6 LED lamps which are located at the top of the PWB directly above the "C" connector. See Figure 5.

Two LED's located to the left of the extractor handle indicate access to either a page address register (PAR) or to an I/O map register.

Four LED's located to the right of the extractor handle indicate the logic level of the upper 4 address bits (of memory bus) during the preceding address cycle.

8K Cache Board.

Power requirements for the cache are 2.1 amps @+5VDC $\pm$0.25VDC. It derives power from the backplane into which it plugs. The cache does not provide additional bus loading.

The cache is contained on a quad-width board which plugs directly into the backplane containing the EnABLE controller. It is plugged into the C, D, E, and F connectors of the first slot. All necessary signals from the EnABLE controller are connected by two top-mounted ribbon cables. See Figure 6.

The Memory Adaptor PWB is equipped with a four position DIP switch assembly (SWI). The switch is used to set the beginning address for old style memory (18 bit address) located behind the memory adaptor board.

Starting addresses and the appropriate switch settings are shown in Table 1 below.

STARTING ADDRESS	SWI-A	SWI-B	SWI-C	SWI-D
0K	OFF	OFF	OFF	OFF
128K	ON	OFF	OFF	OFF
256K	OFF	ON	OFF	OFF
348K	ON	ON	OFF	OFF
512K	OFF	OFF	ON	OFF
640K	ON	OFF	ON	OFF
768K	OFF	ON	ON	OFF
896K	ON	ON	ON	OFF
1024K	OFF	OFF	OFF	ON
1152K	ON	OFF	OFF	ON
1280K	OFF	ON	OFF	ON
1408K	ON	ON	OFF	ON
1536K	OFF	OFF	ON	ON
1664K	ON	OFF	ON	ON
1792K	OFF	ON	ON	ON
1920K	ON	ON	ON	ON

Table 1: Memdap Switch Settings

Upon detection of the programmed address range, MSYN is passed to the bus enabling a response. All other bus signals are passed directly through with no modification.

System Configuration

All EnABLE boards are installed into a dedicated, standard Unibus backplane reserved for the EnABLE boards and 22 bit memory boards.

- EnABLE controller is plugged into the second slot of the dedicated backplane;
- EnABLE 8K cache is plugged into connectors C, D, E, and F of the first slot of the dedicated backplane;
- EnABLE Memdap is plugged into connectors A and B of the last slot (fourth or ninth depending on the size of backplane used) of the dedicated backplane;
- 22 bit memory PWB's are located in slot three of a four-slot backplane, or in slots three through eight of a nine-slot backplane.

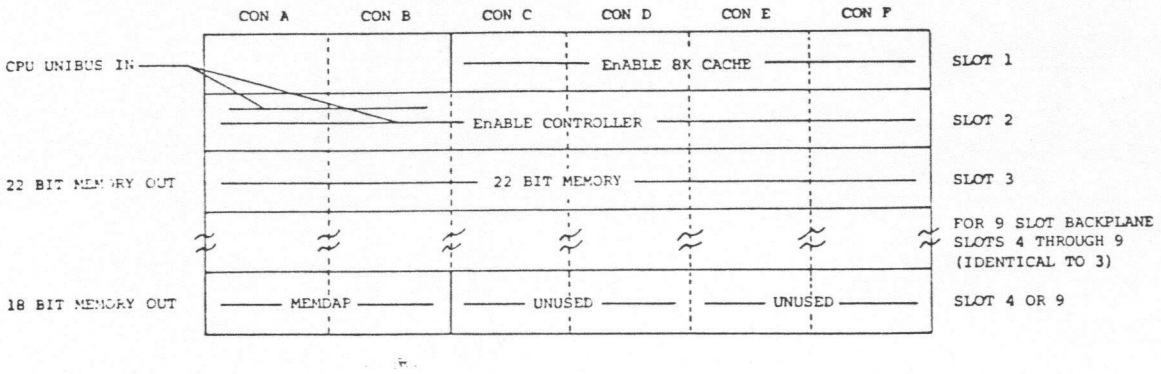


Figure 8: EnABLE Backplane Configuration

Backplane Connections

(1) The CPU Unibus is connected to EnABLE via a standard Unibus cable connected between connectors A and B of the last slot of the CPU backplane and connectors A and B atop the EnABLE controller PWB.

(2) The Memdap Memory Bus is connected to the EnABLE backplane via a standard Unibus cable connected between connectors A and B atop the Memdap PWB to connectors A and B of the first slot of the 18 bit memory backplane.

(3) For 22 bit memory expansion beyond the capacity of the EnABLE backplane, a special Unibus cable is used to connect from connectors A and B of the last MUD Bus slot of the EnABLE backplane (third or eighth depending on the backplane used) to connectors A and B of the first MUD Bus slot (second slot in all cases) of the memory expansion backplane.

See Figure 9.

PART 2 - PROGRAMMING INFORMATION

REGISTER DESCRIPTIONS

The EnABLE controller contains the following registers:

- 32 each Page Address Registers (PAR'S)
- 32 each I/O Map Registers
- 2 System Register (SR3)
  (SR4)
- 1 Memory System Error Register

PAR Registers.
Each PAR is arranged as a single 16-bit wide register. The contents of each register are user programmable via software control. Memory address offset is provided by the assigned contents as shown in Figure 10.

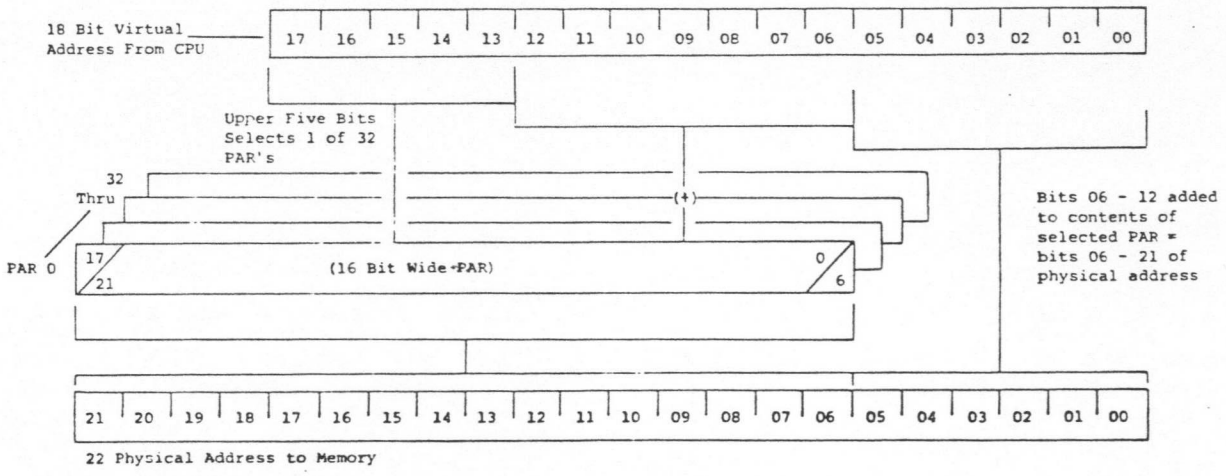


Figure 10: PAR Register

Table 2 contains PAR register addressing information.

DESCRIPTION	PHYSICAL ADDRESS (Octal)	PROGRAM CPU ADDRESS (Octal)
Kernel I Space PAR 0	763700	00XXXX
Kernel I Space PAR 1	763702	02XXXX
Kernel I Space PAR 2	763704	04XXXX
Kernel I Space PAR 3	763706	06XXXX
Kernel I Space PAR 4	763710	10XXXX
Kernel I Space PAR 5	763712	12XXXX
Kernel I Space PAR 6	763714	14XXXX
Kernel D Space PAR 7	763716	16XXXX
User I Space PAR 0	763720	20XXXX
User I Space PAR 1	763722	22XXXX
User I Space PAR 2	763724	24XXXX
User I Space PAR 3	763726	26XXXX
User I Space PAR 4	763730	30XXXX
User I Space PAR 5	763732	32XXXX
User I Space PAR 6	763734	34XXXX
User I Space PAR 7	763736	36XXXX
User D Space PAR 0	763740	40XXXX
User D Space PAR 1	763742	42XXXX
User D Space PAR 2	763744	44XXXX
User D Space PAR 3	763746	46XXXX
User D Space PAR 4	763750	50XXXX
User D Space PAR 5	763752	52XXXX
User D Space PAR 6	763754	54XXXX
User D Space PAR 7	763756	56XXXX
Kernel D Space PAR 0	763760	60XXXX
Kernel D Space PAR 1	763762	62XXXX
Kernel D Space PAR 2	763764	64XXXX
Kernel D Space PAR 3	763766	66XXXX
Kernel D Space PAR 4	763770	70XXXX
Kernel D Space PAR 5	763772	72XXXX
Kernel D Space PAR 6	763774	74XXXX
Kernel I Space PAR 7	763776	76XXXX

Table 2: PAR Register Addressing

I/O Map Registers.
Each I/O map register is arranged as a two word, 22-bit wide value.

The low order word contains the 16 least significant bits (0 through 15) while the high order word contains the 6 most significant bits (18 through 21).

The contents of each register are user programmable via software control. The assigned contents provide the direct memory access (DMA) address offset as shown in Figure 11 below.

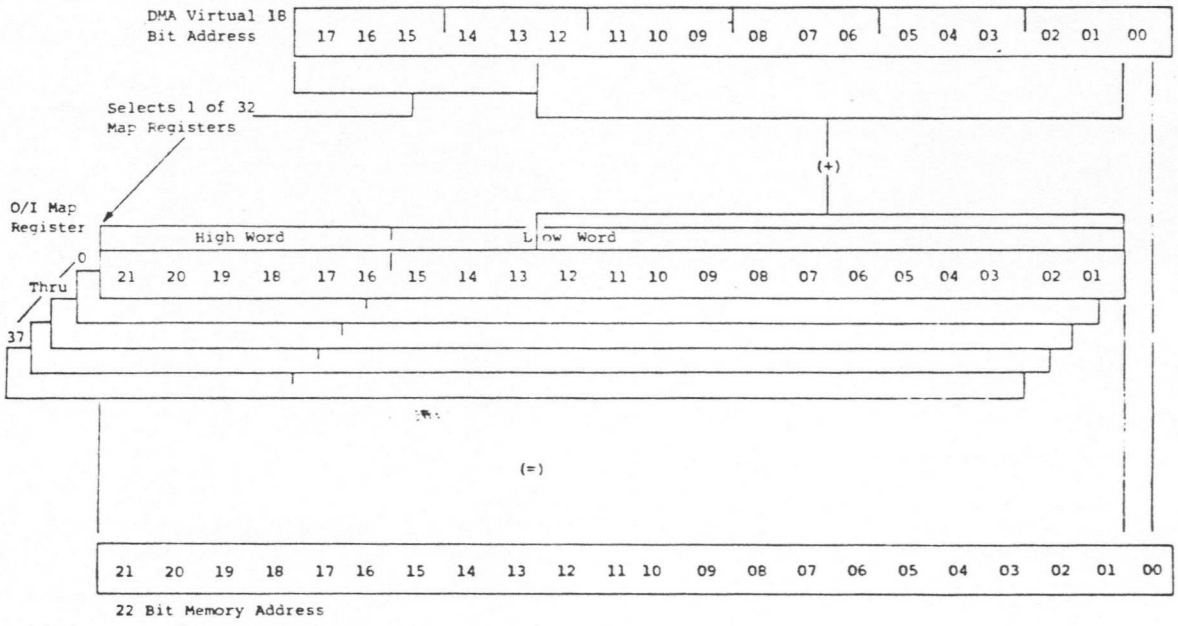


Figure 11: I/O Map Registers

Table 3 contains I/O map register addressing information.

DESCRIPTION		PHYSICAL ADDRESS	DEVICE ADDRESSING SELECTION
Map Register 0	Low Word	770200	00XXXX
	High Word	770202	
Map Register 1	Low Word	770204	02XXXX
	High Word	770206	
Map Register 2	Low Word	770210	04XXXX
	High Word	770212	
Map Register 3	Low Word	770214	06XXXX
	High Word	770216	
Map Register 4	Low Word	770220	10XXXX
	High Word	770222	
Map Register 5	Low Word	770224	12XXXX
	High Word	770226	
Map Register 6	Low Word	770230	14XXXX
	High Word	770232	
Map Register 7	Low Word	770234	16XXXX
	High Word	770236	
Map Register 10	Low Word	770240	20XXXX
	High Word	770242	
Map Register 11	Low Word	770244	22XXXX
	High Word	770246	
Map Register 12	Low Word	770250	24XXXX
	High Word	770252	
Map Register 13	Low Word	770254	26XXXX
	High Word	770256	
Map Register 14	Low Word	770260	30XXXX
	High Word	770262	
Map Register 15	Low Word	770264	32XXXX
	High Word	770266	
Map Register 16	Low Word	770270	34XXXX
	High Word	770272	
Map Register 17	Low Word	770274	36XXXX
	High Word	770276	
Map Register 20	Low Word	770300	40XXXX
	High Word	770302	
Map Register 21	Low Word	770304	42XXXX
	High Word	770306	
Map Register 22	Low Word	770310	44XXXX
	High Word	770312	
Map Register 23	Low Word	770314	46XXXX
	High Word	770316	
Map Register 24	Low Word	770320	50XXXX
	High Word	770322	
Map Register 25	Low Word	770324	52XXXX
	High Word	770326	
Map Register 26	Low Word	770330	54XXXX
	High Word	770332	
Map Register 27	Low Word	770334	56XXXX
	High Word	770336	

Table 3: I/O Map Register Addressing

DESCRIPTION		PHYSICAL ADDRESS	PHYSICAL ADDRESSING SELECTION
Map Register 30	Low Word	770340	60XXXX
	High Word	770342	
Map Register 31	Low Word	770344	62XXXX
	High Word	770346	
Map Register 32	Low Word	770350	64XXXX
	High Word	770352	
Map Register 33	Low Word	770354	66XXXX
	High Word	770356	
Map Register 34	Low Word	770360	70XXXX
	High Word	770362	
Map Register 35	Low Word	770364	72XXXX
	High Word	770366	
Map Register 36	Low Word	770370	74XXXX
	High Word	770372	
Map Register 37	Low Word	770374	76XXXX
	High Word	770376	

Table 3: I/O Map Register Addressing (Continued)

System Register 3 (SR3).
SR3 is a single word, 16 bit register located at physical address 763676 (octal).

Only three bits are used to set the EnABLE mode via software control.

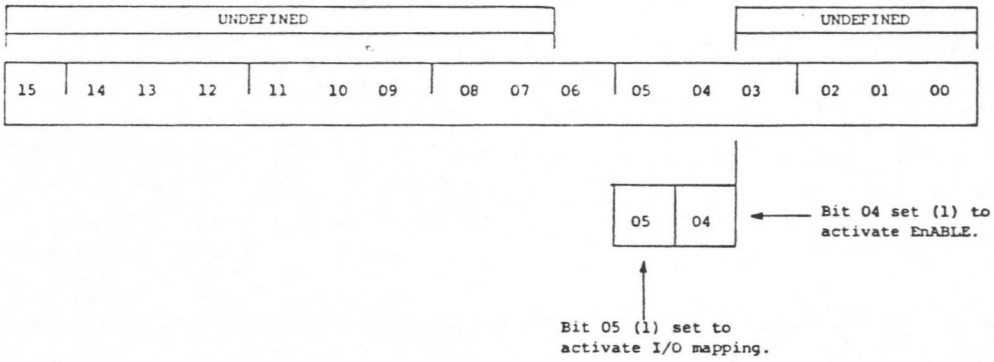


Figure 12: System Register 3

Note: The controller PWB assembly is also equipped with manual toggle switches to override SR3. These switches must be in the "ON" position for software control. For a complete description of switch functions see Section 1, Specifications.

Memory System Error Register
This register is a two word register located at physical address 777740 and 777742 (octal).

The Memory System Error Register contains the lowest 16 bits of the 22-bit address of the first error. All bits are read-only. See Figure 13.

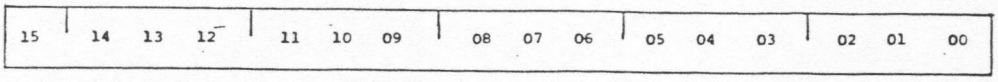


Figure 13: Low Error Address Register 777740

This register also contains the upper six bits of the 22-bit address of the first error, plus the cycle-type bits C0 and C1. All bits are read-only. See Figure 14.

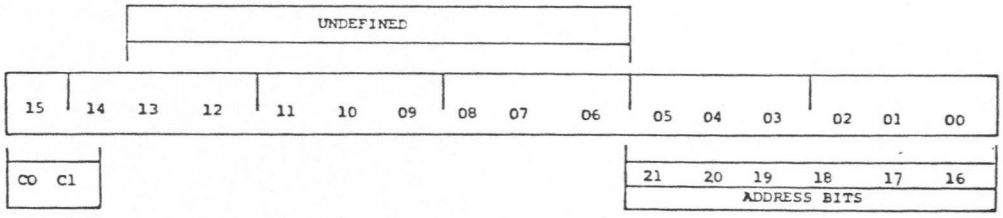


Figure 14: High Error Address Register 777742

System Register 4 (SR4).
SR4 is a single word 16 bit register located at physical address 763674 (octal).

Only 1 bit is used to activate the EnABLE and its on board I/O map registers via software control.

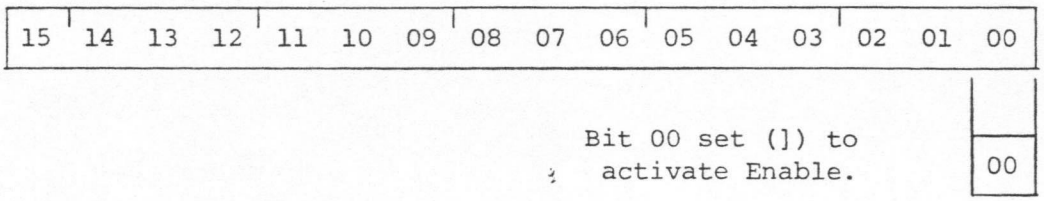


Figure 15: System Register 4