

MAINDEC-11-DZDAA-A
TABLE OF CONTENTS

BUS WINDOW LOGIC TEST

PAGE 2

CONTENTS

1. ABSTRACT
2. REQUIREMENTS
 - 2.1 EQUIPMENT
 - 2.2 STORAGE
 - 2.3 PRELIMINARY PROGRAMS
3. LOADING PROCEDURE
4. STARTING PROCEDURE
 - 4.1 CONTROL SWITCH SETTINGS
 - 4.2 STARTING ADDRESS
 - 4.3 PROGRAM AND/OR OPERATOR ACTION
5. OPERATING PROCEDURE
 - 5.1 OPERATIONAL SWITCH SETTINGS
 - 5.2 SUBROUTINE ABSTRACT
6. ERRORS
7. RESTRICTIONS
8. MISCELLANEOUS
 - 8.1 EXECUTION TIME
 - 8.2 STACK POINTER
 - 8.3 POWER FAIL
9. PROGRAM DESCRIPTION

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100

E01

MAINDEC-11-DZDAA-A
DZDAAA.P11

BUS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 5

146
147

THE PROGRAM CAN BE LOADED INTO EACH PROCESSOR BY USING THE
ABS LOADER THE PROGRAMS CAN THEN BE STARTED AT THE STARTING

MAINDEC-11-DZDAA-A
DESCRIPTION

BUS WINDOW LOGIC TEST

PAGE 4

ADDRESS SPECIFIED IN SECTION 4.2 . THE OTHER OPTION IS TO LOAD THE PROGRAM INTO ONE PROCESSOR USING THE ABS LOADER AND THEN HAVE THE WINDOW TRANSFER THE PROGRAM TO THE OTHER PROCESSOR AS DESCRIBED IN SECTION 4.3 . TO USE THIS METHOD THE WINDOW MUST BE WORKING, IT MUST HAVE A SIZE OF AT LEAST 4K, AND THE WINDOW CANNOT BE LOCATED AT 32K OR ABOVE.

4.1 CONTROL SWITCH SETTINGS

SEE 5.1.1 (ALL DOWN FOR WORST CASE TESTING)

4.2 STARTING ADDRESSES

SA 200 TWO BUS TEST
 SA 204 ONE BUS TEST
 SA 210 POWER FAIL TEST - HOST - FIRST TO GO DOWN
 SA 214 POWER FAIL TEST - NON HOST - SECOND TO GO DOWN
 SA 220 POWER FAIL TEST - NEITHER HOST - FIRST TO GO DOWN
 SA 224 POWER FAIL TEST - NEITHER HOST - SECOND TO GO DOWN
 SA 510 TRANSFERS 0 - 17476 TO OTHER MACHINE (IF > 4K WINDOW)

4.3 PROGRAM AND/OR OPERATOR ACTION

- 1) LOAD THE ABS LOADER IF NOT IN MEMORY
- 2) LOAD PROGRAM WITH ABS LOADER
- 3) LOAD OTHER PROCESSOR IF TWO PROCESSOR TEST.
 - A) IF THE WINDOW IS NOT WORKING, USE ABS LOADER ON OTHER PROCESSOR
 - OR
 - B) IF THE WINDOW IS UP:
 - 1) LOAD ADDRESS 510
 - 2) START
 - 3) LOAD ADDRESS *500 IN OTHER PROCESSOR.
(* = STARTING ADDRESS OF THE WINDOW)
 - 4) START
 - 5) BOTH PROCESSORS WILL SELF START IF SWITCH 7 IS CLEAR. THE HOST WILL DELAY FOR ABOUT 30 SECONDS BEFORE STARTING.
 - 6) THE DISPLAY ON THE 11/45 WILL SHOW THE ITERATION COUNT IN THE LEFT BYTE AND TEST NUMBER IN THE RIGHT. TO USE, SET THE DATA DISPLAY SWITCH TO THE DISPLAY POSITION.

5. OPERATING PROCEDURE

MAINDEC-11-DZDAA-A
DESCRIPTION

BUS WINDOW LOGIC TEST

PAGE 5

5.1 OPERATIONAL SWITCH SETTINGS

AT SA 200 .. ALL SWITCHES DOWN IS WORST CASE TESTING FOR THE 2 BUS TEST. THE BELL WILL RING UPON COMPLETION OF A PASS.

5.1.1 SWITCH SETTINGS ARE:

SW<15> = 1 HALT ON ERROR
SW<14> = 1 LOOP ON TEST
SW<13> = 1 INHIBIT PRINTOUT
SW<10> = 1 BELL ON ERROR
 0 BELL ON PASS COMPLETE
SW<08> = 1 TYPE THE TEST NUMBER BEING EXECUTED
SW<07> = 1 IF SET, PREVENTS THE PROGRAM FROM SELF
 STARTING WHEN THE PROGRAM IS LOADED THROUGH
 THE WINDOW.

5.2 SUBROUTINE ABSTRACTS

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUBTEST AS IT IS BEING ENTERED IN LOCATION "LAD". IF A SCOPE LOOP IS REQUESTED, THE CURRENT SUBTEST WILL BE LOOPED UPON. SW<11> ON A 1 INHIBITS ITERATION OF SUBTESTS. THE CONTENTS OF LAD MAY BE USED TO DETERMINE THE LAST SUBTEST SUCCESSFULLY COMPLETED.

5.2.2 HLT

THIS ROUTINE PRINTS OUT AN ERROR MESSAGE (SEE 6.1). TO INHIBIT TYPEOUTS, PUT SW<13> ON A 1.

5.2.3 TRAPCATCHER

A "+2" - "HALT" SEQUENCE IS REPEATED FROM 4 - 776 TO CATCH ANY UNEXPECTED TRAPS. THUS ANY UNEXPECTED TRAPS OR INTERRUPTS WILL HALT AT THE VECTOR + 2.

6. ERRORS

6.1 ERROR PRINTOUT

H01

MAINDEC-11-DZDAA-A
DZDAAA.P11

BUS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 8

258

THE FORMAT IS AS FOLLOWS:

MAINDEC-11-DZDAA-A
DESCRIPTION

BUS WINDOW LOGIC TEST

PAGE 6

259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313

ADR R0 R1

WHERE:

ADR = ADDRESS OF ERROR HLT
R0 = BAD DATA
R1 = GOOD DATA (OPTIONAL)

6.2 ERROR RECOVERY

ONE BUS TEST - RESTART AT 204

TWO BUS TEST - RESTART AT 200

7. RESTRICTIONS

WHEN RUNNING THE ONE BUS TEST, THE "B" SIDE OF THE WINDOW MUST HAVE ITS CSR REGISTER ADDRESS EXACTLY 20 GREATER THAN THE "A" SIDE CSR REGISTER. IF "A" SIDE CSR ADDRESS EQUALS 764000, THEN "B" SIDE CSR ADDRESS MUST BE 764020.

THE ONE BUS TEST IS PROVIDED FOR CONVENIENCE IN TROUBLE SHOOTING THE DA11-F MODULES. IT IS NOT USED IN THE NORMAL OPERATION OR MAINTENANCE OF A DUAL PROCESSOR SYSTEM. BEFORE USING THE ONE BUS TEST, REMOVE THE FOLLOWING WIRES FROM THE DA11-F WIRED ASSEMBLY BACKPLANE:

BUS A ACLO L: B01F1 TO B04F1

BUS A DCLO L: B01F2 TO B04F2

AFTER TROUBLESHOOTING AND REPAIRING THE MODULES, REPLACE BOTH OF THESE WIRES BEFORE CONNECTING THE DA11-F INTO THE NORMAL DUAL PROCESSOR CONFIGURATION.

8. MISCELLANEOUS

8.1 EXECUTION TIME

A BELL WILL RING WITHIN 1 MINUTE WITH ALL SWITCHES DOWN IN THE 2 BUS TEST.

8.2 STACK POINTER

STACK IS INITALLY SET TO 500

MAINDEC-11-DZDAA-A
DESCRIPTION

BUS WINDOW LOGIC TEST

PAGE 7

8.3 POWER FAIL

THERE ARE SPECIAL ENTRY POINTS FOR POWER FAIL:

SA = 210 HOST COMPUTER - FIRST TO POWER DOWN AND UP

SA = 214 OTHER COMPUTER IS HOST - SECOND TO POWER DOWN AND UP

SA = 220 NEITHER COMPUTER IS HOST - FIRST TO POWER DOWN AND UP

SA = 224 NEITHER COMPUTER IS HOST - SECOND TO POWER DOWN AND UP

TO TEST POWER FAIL, START EACH MACHINE AT ITS APPROPRIATE ADDRESS (SEE ABOVE). THEN TURN THE FIRST MACHINE OFF AND BACK ON. THEN TURN THE SECOND MACHINE OFF AND BACK ON. WHEN FINISHED BOTH MACHINES SHOULD HALT. IF NEITHER MACHINE IS HOST, A THIRD POWER DOWN AND UP IS REQUIRED. I.E., POWER DOWN AND UP THE WINDOW POWER SUPPLY. HOST IS THE SOURCE OF POWER FOR THE BUS WINDOW.

9. PROGRAM DESCRIPTION

THIS PROGRAM IS A TEST OF THE DA11-F BUS WINDOW. IT HAS 2 INDEPENDANT SECTIONS. THE FIRST IS THE 1 BUS TEST WHICH HAS 1 UNIBUS TIED INTO BOTH SIDES OF THE WINDOW. THE REGISTER ADDRESSES AND TRAP VECTORS MUST BE DIFFERENT IN THIS TEST AND TRANSFERS THROUGH THE WINDOW ARE NOT ALLOWED BECAUSE OF THE DATIP CYCLE WOULD CAUSE A TIMEOUT. THIS SHOULD ONLY BE USED FOR INITIAL BRING UP OF THE WINDOW. THE SECOND PART OF THE PROGRAM IS FOR 2 BUSES AND 2 PROCESSORS. IT USES HANDSHAKING TO CHECK OUT THE REGISTERS. THIS SECTION IS SYNCHRONOUS AND IS IN 2 SECTIONS. THESE SECTIONS ARE SELECTED DEPENDING UPON WHO GETS THE BUS FIRST AND THEY SWITCH EVERY PASS. IN THIS TEST, TRANSFERS THROUGH THE WINDOW ARE TRIED INCLUDING A SECTION WHICH EXECUTES CODE IN THE OTHER PROCESSOR'S MEMORY.

THE ONE BUS TEST IS PROVIDED FOR CONVENIENCE IN TROUBLESHOOTING THE DA11-F MODULES. IT IS NOT USED IN THE NORMAL OPERATION OR MAINTENANCE OF A DUAL PROCESSOR SYSTEM. BEFORE USING THE ONE BUS TEST, REMOVE THE FOLLOWING WIRES FROM THE DA11-F WIRED ASSEMBLY BACKPLANE:

BUS A ACLO L: B01F1 TO B04F1

BUS A DCLO L: B01F2 TO B04F2

AFTER TROUBLESHOOTING AND REPAIRING THE MODULES, REPLACE BOTH OF THESE WIRES BEFORE CONNECTING THE DA11-F INTO THE NORMAL DUAL PROCESSOR CONFIGURATION.

%

K01

MAINDEC-11-DZDAA-A
DZDAAA.F11

BUS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 11

.TITLE MAINDEC-11-DZDAA-A BUS WINDOW STATIC TEST
;COPYRIGHT 1972, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
;PROGRAM BY BOB BRAIN

370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407

100000
040000
020000
010000
004000
002000

001000
000400
000200

; SWITCH

SW15= 100000
SW14= 40000
SW13= 20000
SW12= 10000
SW11= 4000
SW10= 2000

SW9= 1000
SW8= 400
SW7= 200

USE

;HALT ON ERROR
;LOOP ON TEST
;INHIBIT ERROR TYPEOUTS

;INHIBIT ITERATIONS
;0 - BELL ON PASS COMPLETE
;1 - BELL ON ERROR
;

;HALT ON TRANSFER COMPLETE

; BIT ---	WCSRA -----	WCSRB -----
; 15	A ERROR	B ERROR
; 14	B TIME OUT	A TIME OUT
; 13	B ACLO	A ACLO
; 12	B NEW DATA	A NEW DATA
; 11	B DATA 3	A DATA 3
; 10	B DATA 2	A DATA 2
; 9	B DATA 1	A DATA 1
; 8	A TRANS ENABLE	B TRANS ENABLE
; 7	B TRANS ENABLE	A TRANS ENABLE
; 6	A I/E	B I/E
; 5	A DATA 3	B DATA 3
; 4	A DATA 2	B DATA 2
; 3	A DATA 1	B DATA 1
; 2	B WRITE ENABLE	A WRITE ENABLE
; 1	A WRITE ENABLE	B WRITE ENABLE
; 0	A NEW DATA	B NEW DATA

;LOADING PROCEDURE:

```

;1) LOAD THE ABS LOADER IF NOT IN MEMORY
;2) LOAD PROGRAM WITH ABS LOADER
;3) LOAD ADDRESS 510
;4) START
;5) LOAD ADDRESS *500 IN OTHER MACHINE (* = WINDOW ADDRESS)
;6) START

```

;TYPEOUTS:

;ADR RO R1

```

;ADR ADDRESS OF ERROR
;RO BAD DATA
;R1 GOOD DATA IF ANY (OPTIONAL)

```

```

000001
104400
104000
000004
177776
177570
177570
000007
000000
000001
000002
000003
000004
000005
000005
000006
000007

```

```

N= 1
SCOPE= TRAP
HLT= EMT
TYPE= IOT
PS= 177776
SWR= 177570
DISPLAY=SWR
BELL= 7
RO= %0
R1= %1
R2= %2
R3= %3
R4= %4
R5= %5
TTY= %5
SP= %6
PC= %7

```

MO1</

NO1

MAINDEC-11-DZDAA-A
DZDAAA.P11

BUS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 14
SETUP AND EQUATS

500 000740 000000

CHKADR: 0

;ADDRESS OF BIT

```

501
502      001000      . =      1000
503
504      001000      000000      ICNT:      0      ; LH = ITERATION COUNT ; RH = TEST NO.
505      001002      000000      ERRORS:      0      ; ERROR COUNT
506      001004      000000      000000      PCNT:      0,0      ; 2 WORD PASS COUNT
507      001010      000000      LAD:      0      ; LOOP ADDRESS FOR SCOPE
508      001012      000000      HLTADR:      0      ; LAST HLT INSTRUCTION ADD. EXECUTED
509
510      001014      012706      000500      ONEBUS:      MOV      #500,SP      ; SET SP ***** 500 *****
511      001020      004767      011604      JSR      PC,SETUP      ; SETUP THE VECTORS, ETC.
512      001024      012737      000340      177776      ONEB1:      MOV      #340,2#PS      ; SET PRIO=7
513
514      ;*****
515      ;TEST 1      CHECK R/W OF WCSRA
516      ;*****
517      001032      104400      TEST1:      SCOPE
518
519      001034      000005      RESET
520      001036      017700      013762      MOV      2WCSRA,RO      ; CLEAR THE WORLD
521      001042      022700      000000      CMP      #0,RO      ; GET THE DATA
522      001046      001401      BEQ      .+4      ; CHECK WCSRA FOR 0 ON RESET
523      001050      104000      HLT      ; SKIP IF OK
524      ; WCSRA DID NOT RESET TO 0
525
526      001052      012777      000573      013744      MOV      #573,2WCSRA      ; SET THE SETABLE BITS
527      001060      017700      013740      MOV      2WCSRA,RO      ; GET THE RESULT
528      001064      022700      000573      CMP      #573!0!1,RO      ; CHECK FOR PROPER BITS
529      001070      001401      BEQ      .+4      ; SKIP IF OK
530      001072      104000      HLT      ; WCSRA NOT 573!0
531
532      001074      012777      000452      013722      MOV      #452,2WCSRA      ; SET THE SETABLE BITS
533      001102      017700      013716      MOV      2WCSRA,RO      ; GET THE RESULT
534      001106      022700      000453      CMP      #452!0!1,RO      ; CHECK FOR PROPER BITS
535      001112      001401      BEQ      .+4      ; SKIP IF OK
536      001114      104000      HLT      ; WCSRA NOT 452!0
537
538      001116      012777      000121      013700      MOV      #121,2WCSRA      ; SET THE SETABLE BITS
539      001124      017700      013674      MOV      2WCSRA,RO      ; GET THE RESULT
540      001130      022700      000121      CMP      #121!0!1,RO      ; CHECK FOR PROPER BITS
541      001134      001401      BEQ      .+4      ; SKIP IF OK
542      001136      104000      HLT      ; WCSRA NOT 121!0
543
544      001140      005077      013660      CLR      2WCSRA      ; CLEAR ALL SETABLE BITS
545      001144      017700      013654      MOV      2WCSRA,RO      ; GET THE RESULT
546      001150      022700      000001      CMP      #0!1,RO      ; CHECK FOR PROPER BITS
547      001154      001401      BEQ      .+4      ; SKIP IF OK
548      001156      104000      HLT      ; WCSRA NOT 0

```

```

548 ;*****
549 ;TEST 2          CHECK R/W OF WCSR8
550 ;*****
551 001160 104400      TST2:  SCOPE
552
553 001162 000005      RESET
554 001164 017700 013662  MOV      2WCSR8,R0      ;CLEAR THE WORLD
555 001170 022700 000000  CMP      #0,R0      ;GET THE DATA
556 001174 001401      BEQ      .+4      ;CHECK WCSR8 FOR 0 ON RESET
557 001176 104000      HLT              ;SKIP IF OK
558                                     ;WCSR8 DID NOT RESET TO 0
559 001200 012777 000573 013644  MOV      #573,2WCSR8      ;SET THE SETABLE BITS
560 001206 017700 013640      MOV      2WCSR8,R0      ;GET THE RESULT
561 001212 022700 000573      CMP      #573!0!1,R0      ;CHECK FOR PROPER BITS
562 001216 001401      BEQ      .+4      ;SKIP IF OK
563 001220 104000      HLT              ;WCSR8 NOT 573!0
564
565 001222 012777 000452 013622  MOV      #452,2WCSR8      ;SET THE SETABLE BITS
566 001230 017700 013616      MOV      2WCSR8,R0      ;GET THE RESULT
567 001234 022700 000453      CMP      #452!0!1,R0      ;CHECK FOR PROPER BITS
568 001240 001401      BEQ      .+4      ;SKIP IF OK
569 001242 104000      HLT              ;WCSR8 NOT 452!0
570
571 001244 012777 000121 013600  MOV      #121,2WCSR8      ;SET THE SETABLE BITS
572 001252 017700 013574      MOV      2WCSR8,R0      ;GET THE RESULT
573 001256 022700 000121      CMP      #121!0!1,R0      ;CHECK FOR PROPER BITS
574 001262 001401      BEQ      .+4      ;SKIP IF OK
575 001264 104000      HLT              ;WCSR8 NOT 121!0
576
577 001266 005077 013560      CLR      2WCSR8      ;CLEAR ALL SETABLE BITS
578 001272 017700 013554      MOV      2WCSR8,R0      ;GET THE RESULT
579 001276 022700 000001      CMP      #0!1,R0      ;CHECK FOR PROPER BITS
580 001302 001401      BEQ      .+4      ;SKIP IF OK
581 001304 104000      HLT              ;WCSR8 NOT 0

```

```

582 :*****
583 :TEST 3          CHECK R/W OF WDBRA
584 :*****
585 TST3: SCOPE
586
587 001306 104400          RESET          ;CLEAR THE WORLD
588 001310 000005          MOV      @WDBRA,R0 ;GET THE DATA
589 001312 017700 013510  CMP      #0,R0    ;CHECK WDBRA FOR 0 ON RESET
590 001316 022700 000000  BEQ      .+4      ;SKIP IF OK
591 001322 001401          HLT              ;WDBRA DID NOT RESET TO 0
592 001324 104000
593
594 001326 012777 177777 013472 MOV      #-1,@WDBRA ;SET THE SETABLE BITS
595 001334 017700 013466  MOV      @WDBRA,R0 ;GET THE RESULT
596 001340 022700 177777  CMP      #-1!0,R0 ;CHECK FOR PROPER BITS
597 001344 001401          BEQ      .+4      ;SKIP IF OK
598 001346 104000          HLT              ;WDBRA NOT -1!0
599
600 001350 012777 125252 013450 MOV      #125252,@WDBRA ;SET THE SETABLE BITS
601 001356 017700 013444  MOV      @WDBRA,R0 ;GET THE RESULT
602 001362 022700 125252  CMP      #125252!0,R0 ;CHECK FOR PROPER BITS
603 001366 001401          BEQ      .+4      ;SKIP IF OK
604 001370 104000          HLT              ;WDBRA NOT 125252!0
605
606 001372 012777 052525 013426 MOV      #52525,@WDBRA ;SET THE SETABLE BITS
607 001400 017700 013422  MOV      @WDBRA,R0 ;GET THE RESULT
608 001404 022700 052525  CMP      #52525!0,R0 ;CHECK FOR PROPER BITS
609 001410 001401          BEQ      .+4      ;SKIP IF OK
610 001412 104000          HLT              ;WDBRA NOT 52525!0
611
612 001414 005077 013406  CLR      @WDBRA ;CLEAR ALL SETABLE BITS
613 001420 017700 013402  MOV      @WDBRA,R0 ;GET THE RESULT
614 001424 022700 000000  CMP      #0,R0    ;CHECK FOR PROPER BITS
615 001430 001401          BEQ      .+4      ;SKIP IF OK
616 001432 104000          HLT              ;WDBRA NOT 0

```

E02

 MAINDEC-11-DZDAA-A
 DZDAA.P11 TST4

 BUS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 18
 CHECK R/W OF WDBRBX

```

616                                     ;*****
617                                     ;TEST 4          CHECK R/W OF WDBRBX
618                                     ;*****
619 001434 104400                       TST4:  SCOPE
620
621 001436 000005                       RESET
622 001440 017700 013410                MOV    @WDBRBX,R0      ;CLEAR THE WORLD
623 001444 022700 000000                CMP    #0,R0          ;GET THE DATA
624 001450 001401                       BEQ     .+4             ;CHECK WDBRBX FOR 0 ON RESET
625 001452 104000                       HLT                     ;SKIP IF OK
626                                     ;WDBRBX DID NOT RESET TO 0
627 001454 012777 177777 013372         MOV    #-1,@WDBRBX    ;SET THE SETABLE BITS
628 001462 017700 013366                 MOV    @WDBRBX,R0      ;GET THE RESULT
629 001466 022700 177777                 CMP    #-1!0,R0        ;CHECK FOR PROPER BITS
630 001472 001401                       BEQ     .+4             ;SKIP IF OK
631 001474 104000                       HLT                     ;WDBRBX NOT -1!0
632
633 001476 012777 125252 013350         MOV    #125252,@WDBRBX ;SET THE SETABLE BITS
634 001504 017700 013344                 MOV    @WDBRBX,R0      ;GET THE RESULT
635 001510 022700 125252                 CMP    #125252!0,R0    ;CHECK FOR PROPER BITS
636 001514 001401                       BEQ     .+4             ;SKIP IF OK
637 001516 104000                       HLT                     ;WDBRBX NOT 125252!0
638
639 001520 012777 052525 013326         MOV    #52525,@WDBRBX  ;SET THE SETABLE BITS
640 001526 017700 013322                 MOV    @WDBRBX,R0      ;GET THE RESULT
641 001532 022700 052525                 CMP    #52525!0,R0    ;CHECK FOR PROPER BITS
642 001536 001401                       BEQ     .+4             ;SKIP IF OK
643 001540 104000                       HLT                     ;WDBRBX NOT 52525!0
644
645 001542 005077 013306                 CLR     @WDBRBX        ;CLEAR ALL SETABLE BITS
646 001546 017700 013302                 MOV    @WDBRBX,R0      ;GET THE RESULT
647 001552 022700 000000                 CMP    #0,R0          ;CHECK FOR PROPER BITS
648 001556 001401                       BEQ     .+4             ;SKIP IF OK
649 001560 104000                       HLT                     ;WDBRBX NOT 0

```

```

650                                     ;*****
651                                     ;TEST 5      CHECK WDBRA TO WDBRAX CROSS COMMUNICATION
652                                     ;*****
653 001562 104400                       TST5:  SCOPE
654
655 001564 000005                       RESET
656 001566 017700 013264                MOV    @WDBRAX,RO      ;CLEAR THE WORLD
657 001572 022700 000000                CMP    #0,RO        ;GET THE DATA
658 001576 001401                       BEQ    .+4             ;CHECK WDBRAX FOR 0 ON RESET
659 001600 104000                       HLT                     ;SKIP IF OK
660                                     ;WDBRAX DID NOT RESET TO 0
661 001602 012777 177777 013216         MOV    #-1,@WDBRA    ;SET THE SETABLE BITS
662 001610 017700 013242                MOV    @WDBRAX,RO    ;GET THE RESULT
663 001614 022700 177777                CMP    #-1!0,RO      ;CHECK FOR PROPER BITS
664 001620 001401                       BEQ    .+4             ;SKIP IF OK
665 001622 104000                       HLT                     ;WDBRAX NOT -1!0
666
667 001624 012777 125252 013174         MOV    #125252,@WDBRA ;SET THE SETABLE BITS
668 001632 017700 013220                MOV    @WDBRAX,RO    ;GET THE RESULT
669 001636 022700 125252                CMP    #125252!0,RO  ;CHECK FOR PROPER BITS
670 001642 001401                       BEQ    .+4             ;SKIP IF OK
671 001644 104000                       HLT                     ;WDBRAX NOT 125252!0
672
673 001646 012777 052525 013152         MOV    #52525,@WDBRA  ;SET THE SETABLE BITS
674 001654 017700 013176                MOV    @WDBRAX,RO    ;GET THE RESULT
675 001660 022700 052525                CMP    #52525!0,RO   ;CHECK FOR PROPER BITS
676 001664 001401                       BEQ    .+4             ;SKIP IF OK
677 001666 104000                       HLT                     ;WDBRAX NOT 52525!0
678
679 001670 005077 013132                CLR    @WDBRA        ;CLEAR ALL SETABLE BITS
680 001674 017700 013156                MOV    @WDBRAX,RO    ;GET THE RESULT
681 001700 022700 000000                CMP    #0,RO        ;CHECK FOR PROPER BITS
682 001704 001401                       BEQ    .+4             ;SKIP IF OK
683 001706 104000                       HLT                     ;WDBRAX NOT 0

```

```

684 :*****
685 :TEST 6 CHECK WDBRBX TO WDBRB CROSS COMMUNICATION
686 :*****
687 001710 104400 TST6: SCOPE
688
689 001712 000005 RESET ;CLEAR THE WORLD
690 001714 017700 013110 MOV @WDBRB,R0 ;GET THE DATA
691 001720 022700 000000 CMP #0,R0 ;CHECK WDBRB FOR 0 ON RESET
692 001724 001401 BEQ .+4 ;SKIP IF OK
693 001726 104000 HLT ;WDBRB DID NOT RESET TO 0
694
695 001730 012777 177777 013116 MOV #-1,@WDBRBX ;SET THE SETABLE BITS
696 001736 017700 013066 MOV @WDBRB,R0 ;GET THE RESULT
697 001742 022700 177777 CMP #-1!0,R0 ;CHECK FOR PROPER BITS
698 001746 001401 BEQ .+4 ;SKIP IF OK
699 001750 104000 HLT ;WDBRB NOT -1!0
700
701 001752 012777 125252 013074 MOV #125252,@WDBRBX ;SET THE SETABLE BITS
702 001760 017700 013044 MOV @WDBRB,R0 ;GET THE RESULT
703 001764 022700 125252 CMP #125252!0,R0 ;CHECK FOR PROPER BITS
704 001770 001401 BEQ .+4 ;SKIP IF OK
705 001772 104000 HLT ;WDBRB NOT 125252!0
706
707 001774 012777 052525 013052 MOV #52525,@WDBRBX ;SET THE SETABLE BITS
708 002002 017700 013022 MOV @WDBRB,R0 ;GET THE RESULT
709 002006 022700 052525 CMP #52525!0,R0 ;CHECK FOR PROPER BITS
710 002012 001401 BEQ .+4 ;SKIP IF OK
711 002014 104000 HLT ;WDBRB NOT 52525!0
712
713 002016 005077 013032 CLR @WDBRBX ;CLEAR ALL SETABLE BITS
714 002022 017700 013002 MOV @WDBRB,R0 ;GET THE RESULT
715 002026 022700 000000 CMP #0,R0 ;CHECK FOR PROPER BITS
716 002032 001401 BEQ .+4 ;SKIP IF OK
717 002034 104000 HLT ;WDBRB NOT 0

```


K04

MAINDEC-11-DZDAA-A BJS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 50
 DZDAAA.P11 TST214 CHECK INSTRUCTION EXECUTION

```

1882 ;*****
1883 ;TEST 214 CHECK INSTRUCTION EXECUTION
1884 ;*****
1885 010262 104400 TST214: SCOPE
1886
1887 010264 004767 004070 JSR PC,TIMO ;TIME THE RESPONCE .. 1 ..
1888
1889 010270 005077 004540 CLR QWRARA ;SET TO BANK 0
1890 010274 012777 000403 004522 MOV #402!1,QWCSRA ;SET 402 INTO QWCSRA
1891
1892 ;*****
1893 ;TEST 215 CHECK INTERUPTS
1894 ;*****
1895 010302 104400 TST215: SCOPE
1896
1897 010304 004767 004050 JSR PC,TIMO ;TIME THE RESPONCE .. 1 ..
1898 010310 012777 000001 004506 MOV #1!1,QWCSRA ;SET 1 INTO QWCSRA
1899
1900 010316 004767 004036 JSR PC,TIMO ;TIME THE RESPONCE .. 2 ..
1901 010322 012777 000001 004474 MOV #1!1,QWCSRA ;SET 1 INTO QWCSRA

```


M04

MAINDEC-11-DZDAA-A
DZDAAA.P11

BJS WINDOW STATIC TEST MACY11 27(732) 05-OCT-76 10:45 PAGE 52
TYPE ROUTINE

1958 010550 001000
1959 010552 000000
1960 010554 000000

FILCHR: 1000
.TYPE: 0
IOTIS: 0

;FILCHR=0 (CHAR) FILCHR+1=2 (COUNT)
;CHARACTER TYPE LOCATION

