

DMC11

HIGH SPD JUMP/FREE RUN
MD-11-DZDMH-A

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IDENTIFICATION

PRODUCT CODE: MAINDEC-11-DZDMH-A-D
PRODUCT NAME: DMC11 HIGH SPEED JUMP AND FREE RUNNING TESTS
DATE: JANUARY 1977
MAINTAINER: DIAGNOSTICS
AUTHOR: FAY BASHAW

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1. ABSTRACT

The function of the DMC11 diagnostics is to verify that the option operates according to specifications. The diagnostics verify that there are no malfunctions and the all operations of the DMC11 are correct in its environment.

Parameters must be set up to alert the diagnostics to the DMC11 configuration. These parameters are contained in the STATUS TABLE and are generated in two ways: 1) Manual Input - the operator answers questions. 2) Autosizing - the program determines the parameters automatically.

DZDMH tests the DMC11-AL micro-processor (M8200-YB) with high speed crom, or the KMC11 micro-processor (M8204). It performs jump tests on the micro-processor, verifies the control ROM of the M8200-YB, and tests the CRAM and other unique functions of the M8204. If a DMC11-AL (M8200-YB) and line unit (M8202-YA or M8202-YD) are present, free-running tests are performed. These tests are skipped if a KMC (M8204) or no line-unit is present. The best test is with a line-unit installed. DZDMH can be used as a Heat Test Diagnostic by Manufacturing.

Currently there are four off line diagnostics that are to be run in sequence to insure that if an error should occur it will be detected at an early stage.

NOTE: Additional diagnostics may be added in the future.

The four diagnostics are:

1. DZDMC [REV] Basic W/R and Micro-processor tests
2. DZDME [REV] DDCMP Line unit tests
3. DZDMF [REV] BITSTUFF Line unit tests
4. DZDMG [REV] Low speed jump and Free-running tests (Heat test tape) NOTE: DZDMG IS RUN ONLY ON A DMC11-AR (M8200-YA).
DZDMH [REV] High speed jump and Free-running tests (Heat test tape) NOTE: DZDMH IS RUN ONLY ON A DMC11-AL (M8200-YB).

2. REQUIREMENTS

2.1 EQUIPMENT

Any PDP11 family CPU (except an LSI-11) with minimum 8k memory
ASR 33 (or equivalent)
DMC11-AL (M8200-YB) or an KMC11-A (M8204) with a DMC11-MA or a DMC11-MD

2.2 STORAGE

Program will use all BK of memory except where ABL and BOOTSTRAP LOADER reside. Locations 1500 thru 1640; contain the "STATUS TABLE" information which is generated at start of diagnostics by manual input (questions) or automatically (auto-sizing). This area is an overlay area and should not be altered by the operator.

3. LOADING PROCEEDURE

3.1 METHOD

All programs are in absolute format and are loaded using the ABSOLUTE LOADER. NOTE: if the diagnostics are on a media such as DISK, MAGTAPE, DECTAPE, or CASSETTE; follow instructions for the monitor which has been provided on that specific media.

ABSOLUTE LOADER starting address *500

MEMORY * SIZE

4k	17
8k	37
12k	57
16k	77
20k	117
24k	137
28k	157

3.1.1 Place address of ABS loader into switch register.
(also place 'HALT' SW up)

3.1.2 Depress 'LOAD ADDRESS' key on console and release.

3.1.3 Depress 'START KEY' on console and release (program should now be loading into CPU)

4. STARTING PROCEEDURE

- a. Set switch register to 000200
- b. Depress 'LOAD ADDRESS' key and release
- c. Set SWR to zero for 'AUTO SIZING' or SWR bit0=1 for manual input (questions) or SWR bit7=1 to use existing parameters set up by a previous start or a previously run DMC11 diagnostic.
- d. Depress 'START KEY' and release. The program will type Maindec Name and program name (if this was the first start up of the program) and also the following:

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160010	145310	177777	000000
001510	160020	145320	177777	000000

The program will type 'R' and proceed to run the diagnostic. The above is only an example. This would indicate the status table starting at add. 1500 in the program. In this example the table contains the information and status of two DMC11'S. THE STATUS TABLE MUST BE VERIFIED BY THE USER IF AUTO SIZING IS DONE. For information of status table see section 8.4 for help.

If the diagnostic was started with SW00=1 indicating manual parameter input then the following shows an example of the questions asked and some example answers:

HOW MANY DMC11'S TO BE TESTED?1

D1
CSR ADDRESS?160010
VECTOR ADDRESS?310
BR PRIORITY LEVEL? (4,5,6,7)?5
DOES MICRO-PROCESSOR HAVE CRAM? (Y OR N)N
WHICH LINE UNIT? IF NONE TYPE "N", IF M8201 TYPE "1", IF M8202 TYPE "2"?1
IS THE LOOP BACK CONNECTOR ON?Y
SWITCH PAC#1 (DDCMP LINE#)?377
SWITCH PAC#2 (BMB73 BOOT ADD)?377

Following the questions the status map is printed out as described above, the information in the map reflects the answers to the questions. If the diagnostic was started with SW00=0 and SW07=0 (AUTO-SIZING) then no questions are asked and only the status-map is printed out. If AUTO-SIZING is used the status information must be verified to be correct (match the hardware). if it does not match the hardware the diagnostic must be restarted with SW00=1 and the questions answered.

4.1 CONTROL SWITCH SETTINGS

SW 15 Set: Halt on error
 SW 14 Set: Loop on current test
 SW 13 Set: Inhibit error print out
 SW 12 Set: Inhibit type out/abell on error.
 SW 11 Set: Inhibit iterations. (quick pass)
 SW 10 Set: Escape to next test on error
 SW 09 Set: Loop with current data
 SW 08 Set: Catch error and loop on it
 SW 07 Set: Use previous status table.
 SW 06 Set: Halt in ROMCLK routine before clocking
 micro-processor
 SW 05 Set: Reserved
 SW 04 Set: Reserved
 SW 03 Set: Reselect DMC11's desired active
 SW 02 Set: Lock on selected test
 SW 01 Set: Restart program at selected test
 SW 00 Set: Build new status table from questions. (If SW07=0
 and SW00=0 a new status table is built by
 auto-sizing)

Switch 06 and 08-15 are dynamic and can be changed as needed while the diagnostic is running. Switches 00-03 and switch 07 are static, and are used only on starting or restarting the diagnostic.

4.1.2 SWITCH REGISTER OPTIONS (at start up)

SW 01 RESTART PROGRAM AT SELECTED TEST. It is strongly suggested that at least one pass has been made before trying to select a test, the reason being is that the program has to clear areas and set up parameters. When this switch is used the diagnostic will ask TEST NO.? Answer by typing the number of the test desired and carriage return to begin execution at the selected test.

SW 02 LOCK ON SELECTED TEST. This switch when used with SW01 will cause the program to constantly loop on the selected test. Hitting any key on the console will let it advance to the next test and loop until a key is hit again. If SW02=0 when SW01 is used. The program will begin at the selected test and continue normal operations.

SW 03 RESELECT DMC11'S DESIRED ACTIVE. Please note that a message is typed out for setting the switch register equal to DMC11's active. this means if the system has four DMC11s; bits 00,01,02,03 will be set in loc 'DMACTV' from the switch register. Using this switch(SW00) alters that location; therefore if four DMC11s are in the system ***DO NOT*** set switches greater than SW 03 in the up position. this would be a fatal error. do not select more active DMC11s than there is information on in the status table.

METHOD: A: Load address 200
B: Start with SW 00=1
C: Program will type message
D: Set a switch for each DMC desired active.
EXAMPLE: If you have 4 DMC's but only want to run the first and the last set SWR bits 0 and 3 = 1. PRESS CONTINUE
E: Number (IF VALID) will be in data lights (excluding 11/05)
F: Set with any other switch settings desired. PRESS CONTINUE.

4.1.3 DYNAMIC SWITCHES

ERROR SWITCHES

1. SW 12 Delete print out/bell on error.
2. SW 13 Delete error printout.
3. SW 15 Halt on the error.
4. SW 08 Goto beginning of the test(on error).
5. SW 10 Goto next test(on error).

SCOPE SWITCHES

1. SW06 Halt in ROMCLK routine before clocking micro-processor instruction. This allows the operator to scope a micro-processor instruction in the static state before it is clocked. Hit continue to resume running.
2. SW09 (if enabled by 'SCOPI') on an error; If an '*' is printed in front of the test no. (ex. *TEST NO. 10) SW09 is incorporated in that test and therefore SW09 is usually the best switch for the scope loop (SW14=0, SW10=0, SW09=1, SW08=0). If SW09 is not enabled; and there is a HARD error (constant); SW08 is best. (SW14=1,0, SW10=0, SW09=0, SW08=1). for intermittent errors; SW14=1 will loop on test regardless of error or not error. (SW14=1, SW10=0, SW09=0, SW08=1,0)
3. SW11 Inhibit iterations.
4. SW14 Loop on current test.

4.2 STARTING ADDRESS

Starting address is at 000200 there are no other starting addresses for the DMC11 diagnostics. (See Section 4.0)

NOTE: If address 000042 is non-zero the program assumes it is under ACT11 or XXDP control and will act accordingly after all available DMC11's are tested the program will return to 'XXDP' or 'ACT-11'.

5. OPERATING PROCEDURE

When program is initially started messages as described in section 4.0 will be printed, and program will begin running the diagnostic

5.2 PROGRAM AND/OR OPERATOR ACTION

The typical approach should be

1. Halt on error (via SW 15=1) when ever an error occurs.
2. Clear SW 15.
3. Set SW 14: (loop on this test)
4. Set SW 13: (inhibit error print out)

The TEST NUMBER and PC will be typed out and possibly an error message (this depends on the test) to give the operator an idea as to the source of the problem. If it is necessary to know more information concerning the error report; LOOK IN THE LISTING for that TEST NUMBER which was typed out and then NOTE THE PC of the ERROR REPORT this way the EXACT FUNCTION of the test CAN BE DETERMINED.

6. ERRORS

As described previously there will always be a TEST NUMBER and PC typed out at the time of an error (providing SW 13=0 and SW 12=0). in most cases additional information will be supplied in the error message to give the operator an indication of the error.

6.2 ERROR RECOVERY

If for some reason the DMC11 should 'HANG THE BUS' (gain control of bus so that console manual functions are inhibited) an init or power down/up is necessary for operator to regain control of cpu. If this should happen; look in location 'TSTNO' (address 1226) for the number of the test that was running at the time of the catastrophic error. In this way the operator will have an idea as to what the DMC11 was doing at the time of the error.

7. RESTRICTIONS

7.1 STARTING RESTRICTIONS

See section 4. (PLEASE)
Status table should be verified regardless of how program was started. Also it is important to use this listing along with the information printed on the TTY to completely isolate problems.

7.2 OPERATING RESTRICTIONS

The first time a DMC11 diagnostic is loaded into core and run the STATUS TABLE must be set up. This is done by manual input (SW00=1) or by autosizing (SW00=0 and SW07=0). Thereafter however the status table need not be setup by subsequent restarts or even loading the next DMC diagnostic because the STATUS TABLE is overlayed. The current parameters in the STATUS TABLE are used when SW07=1 on start up.

7.3 HARDWARE CONFIGURATION RESTRICTIONS

DMC11(M8200)- Jumper W1 must be in, and switch 7 of E76 must be in the OFF position.

KMC(M8204)- Jumper W1 must be in.

LINE UNIT(M8201)- Jumpers W1, W2, and W4 must be IN. Jumpers W3 and W5 must be OUT. SW8 of E26 must be in the ON POSITION.

LINE UNIT (M8202)- Jumper W1 must be in. SW8 of E26 must be in the OFF position.

8. MISCELLANEOUS

8.1 EXECUTION TIME

All DMC11 device diagnostics will give an 'END PASS' message (providing no errors and sw12=0) within 4 mins. This is assuming SW11=1 (DELETE ITERATIONS) is set to give the fastest possible execution. The actual execution time depends greatly on the PDP11 CPU configuration and the amount of memory in the system.

8.2 PASS COMPLETE

NOTE: EVERY time the program is started; the tests will run as if SW11 (delete iterations) was up (=1). This is to 'VERIFY NO HARD ERRORS' as soon as possible. Therefore the first pass -EACH TIME PROGRAM IS STARTED- will be a 'QUICK PASS' until all DMC11's in system are tested. When the diagnostic has completed a pass the following is an example of the print out to be expected.

```
END PASS DZDMH CSR: 175000 VEC: 0300 PASSES: 000001
ERRORS: 000000
```

NOTE: The pass count and error counts are cumulative for each DMC11 that is running, and are set to zero only when the diagnostic is started. Therefore after an overnight run for example, the total passes and errors for each DMC11 since the diagnostic was started are reflected in PASSES: and ERRORS:.

8.4 KEY LOCATIONS

RETURN (1214) Contains the address where program will return when iteration count is reached or if loop on test is asserted.

NEXT (1216) Contains the address of the next test to be performed.

TSTNO (1226) Contains the number of the test now being performed.

RUN (1316) The bit in 'RUN' always points to the DMC11 currently being tested. EXAMPLE: (RUN) 1302/0000000001000000 Means that DMC11 no.06 is the DMC11 now running.

DMCROO-DMCR17
DMSTOO-DMST17
(1500)-(1640) These locations contain the information needed to test up to 16 (decimal) DMC11s sequentially. they contain the CSR, VECTOR and STATUS concerning the configuration of each DMC11.

DMACTV (1306) Each bit set in this location indicates that the associated DMC11 will be tested in turn. EXAMPLE: (DMACTV) 1276/0000000000011111 means that DMC11 no. 00,01,02,03,04 will be tested. EXAMPLE: (DMACTV) 1276/0000000000010001 Means that DMC11 no. 00,04 will be tested.

DMCSR (1404) Contains the CSR of the current DMC11 under test.

8.4A 'STATUS TABLE' (1500-1640)

The table is filled by AUTO SIZING or by the manual parameter input (questions) as described previously. Also if desired by user; the locations may be altered by hand (toggled in) to suit the specific configuration.

The example status map shown below contains information for two DMC11'S. the table can contain up to 16 DMC11'S. Following the map is a description of the bits for each map entry

MAP OF DMC11 STATUS

PC	CSR	STAT1	STAT2	STAT3
001500	160010	145310	177777	000000
001510	160020	016320	000000	000000

Each map entry contains 4 words which contain the status information for 1 DMC11. The PC shows where in core memory the first of the 4 words is. In the example above the first DMC'S status is in locations, 1500, 1502, 1504, and 1506. The second DMC status is located at 1510, 1512, 1514, and 1516. The information contained in each 4 word entry is defined as follows:

CSR: Contains DMC11 CSR address

STAT1: BITS 00-08 IS DMC11 VECTOR ADDRESS
 BIT15=1 MICRO-PROCESSOR HAS CROM
 BIT15=0 MICRO-PROCESSOR HAS CROM
 BIT14=1 TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS DMC11 BR PRIORITY LEVEL

STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)

STAT3: BIT0=1 PERFORM FREE RUNNING TESTS ON KMC
 (must be set manually. SEE TEST 50)

8.5 METHOD OF AUTO SIZING

8.5.1 FINDING THE CONTROL STATUS REGISTER.

The auto-sizing routine finds a DMC11 as follows: It starts at address 160000 and tests all address in increments of 10 up to and including address 167760. If the address does not time out, the following is done, the first CROM address is written to a 125252 then it is read back. If it contains a -1 or 125252 or 63220 a DMC11 or KMC11 has been found, if not, the address is updated by 10 and the search continues. A -1 indicates a DMC11 with no CROM, a 125252 indicates a KMC11 with CROM and a 63220 indicates a DMC11 with the DDCMP CROM. Further tests are performed at this point to determine which line unit, if any, is installed, if a loop-back connector is installed and various switch settings on the line unit. THIS IS WHY THE STATUS TABLE MUST BE VERIFIED BY THE USER AND IF ANY OF THE INFORMATION DOES NOT AGREE WITH THE HARDWARE THE DIAGNOSTIC MUST BE RESTARTED AND THE QUESTIONS MUST BE ANSWERED. All DMC11's in the system will be found by the auto-sizer. If it does not find a DMC11 the diagnostic must be restarted and the questions answered.

8.5.2 FINDING THE VECTOR AND BR LEVEL

The vector area (address 300-776) is filled with the instruction IOT and '+2' (next address). The processor status is started at 7 and the DMC is programmed to interrupt. The PS is lowered by 1 until the DMC interrupts, a delay is made and if no interrupt occurs at PS level 3 (because of a bad DMC11) the program assumes vector address 300 at BR level 5 and the problem should be fixed in the diagnostic. Once the problem is fixed; the program should be re-setup again to get correct vector. If an interrupt occurred; the address to which the DMC11 interrupted to is picked up and reported as the vector. NOTE: if the vector reported is not the vector set up by you; there is a problem and AUTO SIZING should not be done.

8.6 SOFTWARE SWITCH REGISTER

If the diagnostic is run on an 11/04 or other CPU without a switch register then a software switch register is used to allow user the same switch options as described previously. If the hardware switch register does not exist or if one does and it contains all ones (177777) this software switch register is used.

Control:

To obtain control at any allowable time during execution of the diagnostic the operator types a CTRL G on the console terminal keyboard. As soon as the CTRL G is recognized, by the diagnostic, the following message will be displayed:

SWR=XXXXXX NEW?

Where XXXXXX is the current contents of the software switch register in octal. The software control routine will then await operator action. At which time the operator is required to type one or more of the legal characters: 1) 0 - 7, 2) line feed(<LF>), 3) carriage return(<CR>), or 4) control-U (CTRL U). No check is made for legality. If the input character is not a <LF>, <CR>, or CTRL U it is assumed to be an octal digit.

To change the contents of the SSR the operator simply types the new desired value in octal - leading zeros need not be typed. And terminates the input string with a <CR> or <LF> depending on the program action desired as described below. The input value will be truncated to the last 6 digits typed. At least one digit must be typed on any given input string prior to the terminator before a change to the SSR will occur.

When the input string is terminated with a <CR> the diagnostic will continue execution from the point at which it was interrupted. If a <CR> is the only thing typed the program will continue without changing the SSR. The <LF> differs from the <CR> by restarting the program as if it were restarted at address 200.

If a CTRL U is typed at any point in the input string prior to the terminator the input value will be disregarded and the prompt displayed (SWR = XXXXXX NEW?).

To set the SSR for the starting switches, first load the diagnostic, then hit CTRL G, then start the diagnostic.

DZDMH LST

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DOCUMENT

DZDMH LST

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6 MAINDEC-11-DZDMH-A DMC11 LOCAL CROM, JUMP, AND FREE RUNNING TESTS
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1626 ***** TEST 1 *****
TEST OF BR RIGHT SHIFT
VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION
SHIFTS THE RESULTING BR DATA RIGHT ONCE.

1666 ***** TEST 2 *****
IOP CROM WRITE/READ TEST
FLOAT A 1 THROUGH EACH CROM LOCATION

1700 ***** TEST 3 *****
IOP CROM WRITE/READ TEST
FLOAT A 0 THROUGH EACH CROM LOCATION

1737 ***** TEST 4 *****
IOP CROM DUAL ADDRESSING TEST
WRITE EACH ADDRESS INTO ITSELF, READ EACH
ADDRESS TO VERIFY CORRECT ADDRESSING

1783 ***** TEST 5 *****
IOP CROM READ TEST
THIS TEST WRITES THE CROM WITH THE CROM MICRO-CODE MAP
THEN READS IT BACK AND COMPARES EACH ADDRESS WITH THE
DUPLICATE OF THE CROM MICRO-CODE.

1820 ***** TEST 6 *****
IOP MAIN MEMORY TEST
FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS

1866 ***** TEST 7 *****
IOP MAIN MEMORY TEST
FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS

1914 ***** TEST 10 *****
IOP MAIN MEMORY DUAL ADDRESSING TEST
LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS
READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING

1982 ***** TEST 11 *****
IOP MAR TEST
PERFORM DUAL ADDRESSING TEST
USING MAR AUTO-INC FEATURE

2022 ***** TEST 12 *****
IOP (CROM) ODT BITS TEST
LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS (2000 TIMES)
VERIFY THAT IBUS* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE
AND THAT IBUS* 10 BIT6 IS SET ON MAR OVERFLOW(2000)

2083 ***** TEST 13 *****
CROM READ TEST
THIS TEST READS EACH ROM LOCATION AND COMPARES

2086 IT TO A SOFTWARE DUPLICATE OF THE CROM. THIS TEST
ALSO TESTS THE JUMP(I) MICRO-PROCESSOR INSTRUCTION.

2132 ***** TEST 14 *****
CROM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
PERFORM THE JUMP INSTRUCTION
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2189 ***** TEST 15 *****
CROM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
PERFORM THE JUMP INSTRUCTION
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2242 ***** TEST 16 *****
CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
SET THE C BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2298 ***** TEST 17 *****
CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2354 ***** TEST 20 *****
CROM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2410 ***** TEST 21 *****
CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2466 ***** TEST 22 *****
CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2522 ***** TEST 23 *****
CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

2578 ***** TEST 24 *****
CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2635 ***** TEST 25 *****
CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2692 ***** TEST 26 *****
CROM TEST OF JUMP(I) ON BR0 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR0 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2749 ***** TEST 27 *****
CROM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2806 ***** TEST 30 *****
CROM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2863 ***** TEST 31 *****
CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THAT THE JUMP DID NOT OCCUR BY READING
THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

2920 ***** TEST 32 *****
CRAM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
PERFORM THE JUMP INSTRUCTION
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT

2926 THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

2982 ***** TEST 33 *****
CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
PERFORM THE JUMP INSTRUCTION
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3041 ***** TEST 34 *****
CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
SET THE C BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3103 ***** TEST 35 *****
CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
SET THE Z BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3165 ***** TEST 36 *****
CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3227 ***** TEST 37 *****
CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3289 ***** TEST 40 *****
CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3351 ***** TEST 41 *****
CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
THEN PORT4 WILL CONTAIN A 37

3413 ***** TEST 42 *****
CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3475 ***** TEST 43 *****
CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3537 ***** TEST 44 *****
CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE

3542 BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3599 ***** TEST 45 *****
CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3661 ***** TEST 46 *****
GRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE GRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE GRAM PC IS CORRECT, IF THE GRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3723 ***** TEST 47 *****
GRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,
VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
BR WITH THE LOWEST 8 BITS OF THE GRAM PC. AT THIS POINT
THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
THE GRAM PC IS CORRECT, IF THE GRAM PC IS NOT RIGHT,
THEN PORT4 CONTAINS A 37

3795 ***** TEST 50 *****
FREE RUNNING FLAG MODE DATA TEST
TRANSMIT A MESSAGE AND VERIFY THE RECEIVED DATA
IF NO TURNAROUND CONNECTOR IS ON LINE UNIT LOOP IS SET.
ALL FOLLOWING TESTS ARE FREE RUNNING AND ARE PERFORMED
ONLY ON DMC'S WITH LINE UNITS. IF YOU WISH TO PERFORM
THESE FREE RUNNING TESTS ON A KMC (NORMALLY THE FREE RUNNING TESTS
WILL FAIL ON A KMC, THE TIMER IS TOO FAST) THEN YOU MUST
MANUALLY SET BIT0 OF STAT3 IN THE STATUS MAP.

3960 ***** TEST 51 *****
OVERUN TEST
IN FREE RUNNING MODE SEND MESSAGE WITH NO RECEIVE
BUFFER AVAILABLE, VERIFY THAT AN OVERRUN ERROR OCCURS

4016 ***** TEST 52 *****
LOST DATA TEST
IN FREE RUNNING MODE SEND A MESSAGE LONGER THAN THE RECEIVE
BUFFER, VERIFY THAT A LOST DATA ERROR OCCURS.

4065 ***** TEST 53 *****
TRANSMIT NON-EXISTENT MEMORY TEST
IN FREE RUNNING MODE, LOAD A TRANSMIT BA THAT WILL TIME OUT
VERIFY THAT A NON-EXISTENT MEMORY ERROR OCCURS

4111 ***** TEST 54 *****
RECEIVE NON-EXISTENT MEMORY TEST
IN FREE RUNNING MODE, LOAD A RECEIVE BA THAT WILL TIME OUT
VERIFY THAT A NON-EXISTENT MEMORY ERROR OCCURS

4160 ***** TEST 55 *****
PROCESSOR ERROR TEST
IN FREE RUNNING MODE, DO A BASE TRANSFER REQUEST AFTER A
BASE HAS BEEN SET UP, VERIFY THAT A PROCESSOR ERROR OCCURS.

4204 ***** TEST 56 *****
PROCESSOR ERROR TEST
IN FREE RUNNING MODE DO A RQI WITH AN ILLEGAL IO CODE
VERIFY THAT A PROCESSOR ERROR OCCURS

4248 ***** TEST 57 *****
HALF DUPLEX TEST
IN FREE RUNNING MODE, SET HALF DUPLEX AND L U LOOP
SEND A MESSAGE AND VERIFY THAT THERE ARE NO DONES

4288 ***** TEST 60 *****
FREE RUNNING DATA TEST (INTERRUPT DRIVEN EXERCISER)
THIS TEST REPEATEDLY QUEUES UP 7 RECEIVE BUFFERS AND
7 TRANSMIT BUFFERS AND CHECKS DATA WHEN ALL 7 BUFFERS
ARE RECEIVED. TRANSMIT COUNTS RANGE FROM 1 TO 104, ALSO
ODD AND EVEN TRANSMIT AND RECEIVE BA'S ARE USED. DATA
IS A BINARY COUNT PATTERN. THE RESUME FUNCTION IS CHECKED IN THIS TEST

```

: *MAINDEC-11-DZDMH-A DMC11 LOCAL CROM, JUMP, AND FREE RUNNING TESTS
: *COPYRIGHT 1976, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
: *-----

```

```

: STARTING PROCEDURE
: LOAD PROGRAM
: LOAD ADDRESS 000200
: SWR=0 AUTOSIZE DMC11
: SW07=1 USE CURRENT DMC11 PARAMETERS
: SW00=1 INPUT NEW DMC11 PARAMETERS
: PRESS START
: PROGRAM WILL TYPE "MAINDEC-11-DZDMH-A DMC11 LOCAL CROM, JUMP, AND FREE RUNNIN
: PROGRAM WILL TYPE STATUS MAP
: PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
: AT THE END OF A PASS, PROGRAM WILL TYPE PASS COMPLETE MESSAGE
: AND THEN RESUME TESTING
: SUBSEQUENT RESTARTS WILL NOT TYPE PROGRAM TITLE

```

```

: SWITCH REGISTER OPTIONS
: -----

```

```

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

```

```

SW15=100000      :=1, HALT ON ERROR
SW14=40000        :=1, LOOP ON CURRENT TEST
SW13=20000        :=1, INHIBIT ERROR TIMEOUT
SW12=10000        :=1, DELETE TIMEOUT/BELL ON ERROR.
SW11=4000         :=1, INHIBIT ITERATIONS
SW10=2000         :=1, ESCAPE TO NEXT TEST ON ERROR
SW09=1000         :=1, LOOP WITH CURRENT DATA
SW08=400          :=1, LOOP ON ERROR
SW07=200          :=1, USE CURRENT DMC11 PARAMETERS, =0, AUTOSIZE DMC11
SW06=100          :=1, HALT BEFORE CLOCKING MICRO-PROCESSOR INSTRUCTION
SW05=40
SW04=20
SW03=10           := RESELECT DMC11'S TO BE TESTED (ACTIVE)
SW02=4            := LOCK ON TEST SELECT
SW01=2            := RESTART PROGRAM AT SELECTED TEST
SW00=1            := INPUT DMC11 PARAMETERS

```

K02

OZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 3
OZDMH.P11 09-DEC-76 14:59 GENERAL DEFINATIONS AND EQUIVALENCIES

PAGE: 0023

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92
93
94
95
96
97

```

;REGISTER DEFINITIONS
;-----
R0=%0      ;GENERAL REGISTER
R1=%1      ;GENERAL REGISTER
R2=%2      ;GENERAL REGISTER
R3=%3      ;GENERAL REGISTER
R4=%4      ;GENERAL REGISTER
R5=%5      ;GENERAL REGISTER
SP=%6      ;PROCESSOR STACK POINTER
PC=%7      ;PROGRAM COUNTER

;LOCATION EQUIVALENCIES
;-----
PS=177776  ;PROCESSOR STATUS WORD
STACK=1200  ;START OF PROCESSOR STACK

;INSTRUCTION DEFINITIONS
;-----
PUSH1SP=5746 ;DECREMENT PROCESSOR STACK 1 WORD
POP1SP=5726  ;INCREMENT PROCESSOR STACK 1 WORD
PUSHR0=10046 ;SAVE R0 ON STACK
POPR0=12600  ;RESTORE R0 FROM STACK
PUSH2SP=24646 ;DECREMENT STACK TWICE
POP2SP=22626 ;INCREMENT STACK TWICE
.EQUIV EMT,HLT ;BASIC DEFINITION OF ERROR CALL

;BIT DEFINITIONS
;-----
BIT15=100000
BIT14=40000
BIT13=20000
BIT12=10000
BIT11=4000
BIT10=2000
BIT9=1000
BIT8=400
BIT7=200
BIT6=100
BIT5=40
BIT4=20
BIT3=10
BIT2=4
BIT1=2
BIT0=1

```

000000
000001
000002
000003
000004
000005
000006
000007

177776
001200

005746
005726
010046
012600
024646
022626

100000
040000
020000
010000
004000
002000
001000
000400
000200
000100
000040
000020
000010
000004
000002
000001

R0=%0
R1=%1
R2=%2
R3=%3
R4=%4
R5=%5
SP=%6
PC=%7

PS=177776
STACK=1200

PUSH1SP=5746
POP1SP=5726
PUSHR0=10046
POPR0=12600
PUSH2SP=24646
POP2SP=22626
.EQUIV EMT,HLT

BIT15=100000
BIT14=40000
BIT13=20000
BIT12=10000
BIT11=4000
BIT10=2000
BIT9=1000
BIT8=400
BIT7=200
BIT6=100
BIT5=40
BIT4=20
BIT3=10
BIT2=4
BIT1=2
BIT0=1

L02

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 4
DZDMH.P11 09-DEC-76 14:59 TRAPCATCHER FOR UNEXPECTED INTERRUPTS

PAGE: 0024

```

98
99
100
101
102
103
104
105
106
107
108      000000
109
110
111
112      000024
113      000024 005240
114      000026 000340
115      000030 004656
116      000032 000340
117      000034 004624
118      000036 000340
119
120      000040 000000
121      000042 000000
122      000044 000000
123      000046 003432
124      000052 000052
125      000052 000000
126
127      000174
128      000174 000000
129      000176 000000
130
131      000200
132      000200 000137 002002
133
134
135      001000
136      001000 005377 040515 047111
137      (2) 001025 104 041515 030461
138      (2)
139      001200
140
141
142      001200 177570
143      001202 177570

```

```

:*****
:-----
:TRAPCATCAER FOR ILLEGAL INTERRUPTS
:THE STANDARD "TRAP CATCHER" IS PLACED
:BETWEEN ADDRESS 0 TO ADDRESS 776.
:IT LOOKS LIKE "PC+2 HALT".
:-----
:*****
:
:=0
:STANDARD INTERRUPT VECTORS
:-----
:=24
      .PFAIL      ;POWER FAIL HANDLER
      340          ;SERVICE AT LEVEL 7
      .HLT        ;ERROR HANDLER
      340          ;SERVICE AT LEVEL 7
      .TRPSRV     ;GENERAL HANDLER DISPATCH SERVICE
      340          ;SERVICE AT LEVEL 7
:=40
      0            ;SAVE FOR ACT-11 OR XXDP
      0            ;RETURN ADDRESS IF UNDER ACT-11 OR XXDP
      0            ;SAVE FOR ACT-11 OR XXDP
      $ENDAD      ;FOR USE WITH ACT-11 OR XXDP
:=52
      0            ;ACT-11 PROGRAM CHARACTERISTICS
:=174
DISPREG: 0          ;SOFTWARE DISPLAY REGISTER
SWREG: 0            ;SOFTWARE SWITCH REGISTER
:=200
      JMP .START   ;GO TO START OF PROGRAM
:=1000
MTITLE: .ASCII <377><12>/MAINDEC-11-DZDMH-A/<377>
        .ASCIIZ /DMC11 LOCAL CROM. JUMP, AND FREE RUNNING TESTS/<377>
:=1200
;INDIRECT POINTERS TO SWITCH REGISTER AND LIGHT DISPLAY
:-----
DISPLAY: 177570
SWR: 177570

```

M02

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 5
 DZDMH.P11 09-DEC-76 14:59

PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

PAGE: 0025

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144
145
146
147
149 001204 177560
149 001206 177562
150 001210 177564
151 001212 177566
152
153
154
155
156 001214 000000
157 001216 000000
158 001220 000000
159 001222 000003
160 001224 000000
161 001226 000000
162 001230 000000
163 001232 000000
164 001234 000000
165
166
167
168
169 001236 000000
170 001240 000000
171 001242 000000
172 001244 000000
173 001246 000000
174 001250 000000
175 001252 000000
176 001254 000000
177 001256 000000
178 001260 000000
179 001262 000000
180 001264 000000
181 001266 000000
182 001270 000000
183 001272 000000
184 001274 000000
185 001276 000000
186 001300 000000
187 001302 000001
188 001304 000000
189 001306 000001
190 001310 000001
191 001312 000001
192 001314 000001
193 001316 000000
194
195 001320 001472
196 001322 001676

```

```

;INDIRECT POINTERS TO TELETYPE VECTORS AND REGISTERS
;-----
TKCSR: 177560      ;TELETYPE KEYBOARD CONTROL REGISTER
TKDBR: 177562      ;TELETYPE KEYBOARD DATA BUFFER
TPCSR: 177564      ;TELEPRINTER CONTROL REGISTER
TPDBR: 177566      ;TELEPRINTER DATA BUFFER

;PROGRAM CONTROL PARAMETERS
;-----
RETURN: 0           ;SCOPE ADDRESS FOR LOOP ON TEST
NEXT: 0             ;ADDRESS OF NEXT TEST TO BE EXECUTED
LOCK: 0             ;ADDRESS FOR LOCK ON CURRENT DATA
ICOUNT: 3           ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE
LPCNT: 0            ;NUMBER OF ITERATIONS COMPLETED
TSTNO: 0            ;NUMBER OF TEST IN PROGRESS
PASCNT: 0           ;NUMBER OF PASSES COMPLETED
ERRCNT: 0           ;TOTAL NUMBER OF ERRORS
LSTERR: 0           ;PC OF LAST ERROR CALL

;PROGRAM VARIABLES
;-----
STRISW: 0           ;SWITCHES AT START OF PROGRAM
STAT: 0             ;DM STATUS WORD STORAGE
CLKX: 0
MASKX: 0
TEMP1: 0            ;TEMPORARY STORAGE
TEMP2: 0            ;TEMPORARY STORAGE
TEMP3: 0            ;TEMPORARY STORAGE
TEMP4: 0            ;TEMPORARY STORAGE
TEMP5: 0            ;TEMPORARY STORAGE
SAVR0: 0            ;R0 STORAGE
SAVR1: 0            ;R1 STORAGE
SAVR2: 0            ;R2 STORAGE
SAVR3: 0            ;R3 STORAGE
SAVR4: 0            ;R4 STORAGE
SAVR5: 0            ;R5 STORAGE
SAVSP: 0            ;STACK POINTER STORAGE
SAVPC: 0            ;PROGRAM COUNTER STORAGE
ZERO: 0
ONE: 1
MEMLIM: 0           ;HIGHEST LOCATION FOR NPR'S
DMACTV: .BLKW 1     ;DMC11'S SELECTED ACTIVE.
DMNUM: .BLKW 1       ;OCTAL NUMBER OF DMC11'S.
SAVACT: .BLKW 1      ;ORIGINAL ACTV DEVICES
SAVNUM: .BLKW 1      ;WORKABLE NUMBER
RUN: 0              ;POINTER TO RUNNING DEVICE.
.EVEN
CREAM: DM.MAP-6      ;TABLE POINTER.
MILK: CNT.MAP-4      ;TABLE POINTER

```

N02

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 6
 DZDMH.P11 09-DEC-76 14:59 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

PAGE: 0026

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238
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240
241
242
243
244
245
246
247

001324 000
001325 000
001326 000
001327 000

001330 104400
001330 003506
104401
001332 003644
104402
001334 003674
104403
001336 003756
104404
001340 004062
104405
001342 004102
104406
001344 004302
104407
001346 004342
104410
001350 004374
104411
001352 004400
104412
001354 005370
104413
001356 005340
104414
001360 005406
104415
001362 005454
104416
001364 005520

;PROGRAM CONTROL FLAGS

INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
 ERRFLG: .BYTE 0 ;ERROR OCCURED FLAG
 LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
 QV.FLG: .BYTE 0 ;QUICK VERIFY FLAG.
 ;ON FIRST PASS OF EACH DMC11 ITERATIONS WILL BE
 .EVEN

;DEFINITIONS FOR TRAP SUBROUTINE CALLS
 ;POINTERS TO SUBROUTINES CAN BE FOUND
 ;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS

;*****

TRPTAB:
 SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
 .SCOPE
 SCOP1=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
 .SCOP1
 TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
 .TYPE
 INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
 .INSTR
 INSTER=TRAP+4 ;CALL TO INPUT ERROR HANDLER
 .INSTER
 PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
 .PARAM
 SAVOS=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
 .SAVOS
 RESOS=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
 .RESOS
 CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
 .CONVRT
 CNVRT=TRAP+11 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF.
 .CNVRT
 MSTCLR=TRAP+12 ;CALL TO ISUE A MASTER CLEAR
 .MSTCLR
 DELAY=TRAP+13 ;CALL TO DELAY
 .DELAY
 ROMCLK=TRAP+14 ;CALL TO CLOCK ROM ONCE
 .ROMCLK
 DATACLK=TRAP+15 ;CALL TO CLK DATA
 .DATACLK
 TIMER=TRAP+16 ;CALL TO DELAY A CLOCK TICK
 .TIMER

;*****

```

248
249 ;DMC11 CONTROL INDICATORS FOR CURRENT DMC11 UNDER TEST
250 -----
251
252 001366 000000 STAT1: 0
253 001370 000000 STAT2: 0
254 001372 000000 STAT3: 0
255
256 ;DMC11 VECTOR AND REGISTER INDIRECT POINTERS
257 -----
258
259 001374 000000 DMRVEC: 0 ;POINTER TO DMC11 RECEIVER INTERRUPT VECTOR
260 001376 000000 DMRLVL: 0 ;POINTER TO DMC11 RECEIVER INTERRUPT SERVICE PS
261 001400 000000 DMTVEC: 0 ;POINTER TO DMC11 TRANSMITTER INTERRUPT VECTOR
262 001402 000000 DMTLVL: 0 ;POINTER TO DMC11 TRANSMITTER INTERRUPT SERVICE PS
263 001404 000000 DMCSR: 0 ;POINTER TO DMC11 CONTROL STATUS REGISTER
264 001406 000000 DMCSRH: 0 ;POINTER TO DMC11 CONTROL STATUS REGISTER HIGH BYTE.
265 001410 000000 DMCTL: 0 ;POINTER TO DMC11 CONTROL OUT REGISTER
266 001412 000000 DMP04: 0 ;POINTER TO DMC11 PORT REGISTER(SEL 4)
267 001414 000000 DMP06: 0 ;POINTER TO DMC11 PORT REGISTER(SEL 6)
268
269 ;TEMP STORAGE
270 -----
271
272 001416 000000 TEMP: 0
273 001460 .=. +40
274
275 ;DMC11 STATUS TABLE AND ADDRESS ASSIGNMENTS
276 -----
277
278 001500 . =1500
279 001500 000001 DM.MAP:
280 001500 000001 DMC00: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 00
281 001502 000001 DMS100: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 00
282 001504 000001 DMS200: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 00
283 001506 000001 DMS300: .BLKW 1 ;3RD STATUS WORD
284
285 001510 000001 DMC01: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 01
286 001512 000001 DMS101: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 01
287 001514 000001 DMS201: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 01
288 001516 000001 DMS301: .BLKW 1 ;3RD STATUS WORD
289
290 001520 000001 DMC02: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 02
291 001522 000001 DMS102: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 02
292 001524 000001 DMS202: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 02
293 001526 000001 DMS302: .BLKW 1 ;3RD STATUS WORD
294
295 001530 000001 DMC03: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 03
296 001532 000001 DMS103: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 03
297 001534 000001 DMS203: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 03
298 001536 000001 DMS303: .BLKW 1 ;3RD STATUS WORD
299
300 001540 000001 DMC04: .BLKW 1 ;CONTROL STATUS REGISTER FOR DMC11 NUMBER 04
301 001542 000001 DMS104: .BLKW 1 ;VECTOR FOR DMC11 NUMBER 04
302 001544 000001 DMS204: .BLKW 1 ;DDCMP LINE# FOR DMC11 NUMBER 04
303 001546 000001 DMS304: .BLKW 1 ;3RD STATUS WORD

```

304					
305	001550	000001	DMCR05:	.BLKW	1
306	001552	000001	DMS105:	.BLKW	1
307	001554	000001	DMS205:	.BLKW	1
308	001556	000001	DMS305:	.BLKW	1
309					
310	001560	000001	DMCR06:	.BLKW	1
311	001562	000001	DMS106:	.BLKW	1
312	001564	000001	DMS206:	.BLKW	1
313	001566	000001	DMS306:	.BLKW	1
314					
315	001570	000001	DMCR07:	.BLKW	1
316	001572	000001	DMS107:	.BLKW	1
317	001574	000001	DMS207:	.BLKW	1
318	001576	000001	DMS307:	.BLKW	1
319					
320	001600	000001	DMCR10:	.BLKW	1
321	001602	000001	DMS110:	.BLKW	1
322	001604	000001	DMS210:	.BLKW	1
323	001606	000001	DMS310:	.BLKW	1
324					
325	001610	000001	DMCR11:	.BLKW	1
326	001612	000001	DMS111:	.BLKW	1
327	001614	000001	DMS211:	.BLKW	1
328	001616	000001	DMS311:	.BLKW	1
329					
330	001620	000001	DMCR12:	.BLKW	1
331	001622	000001	DMS112:	.BLKW	1
332	001624	000001	DMS212:	.BLKW	1
333	001626	000001	DMS312:	.BLKW	1
334					
335	001630	000001	DMCR13:	.BLKW	1
336	001632	000001	DMS113:	.BLKW	1
337	001634	000001	DMS213:	.BLKW	1
338	001636	000001	DMS313:	.BLKW	1
339					
340	001640	000001	DMCR14:	.BLKW	1
341	001642	000001	DMS114:	.BLKW	1
342	001644	000001	DMS214:	.BLKW	1
343	001646	000001	DMS314:	.BLKW	1
344					
345	001650	000001	DMCR15:	.BLKW	1
346	001652	000001	DMS115:	.BLKW	1
347	001654	000001	DMS215:	.BLKW	1
348	001656	000001	DMS315:	.BLKW	1
349					
350	001660	000001	DMCR16:	.BLKW	1
351	001662	000001	DMS116:	.BLKW	1
352	001664	000001	DMS216:	.BLKW	1
353	001666	000001	DMS316:	.BLKW	1
354					
355	001670	000001	DMCR17:	.BLKW	1
356	001672	000001	DMS117:	.BLKW	1
357	001674	000001	DMS217:	.BLKW	1
358	001676	000001	DMS317:	.BLKW	1
359					

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 05
 ;VECTOR FOR DMC11 NUMBER 05
 ;DDCMP LINE# FOR DMC11 NUMBER 05
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 06
 ;VECTOR FOR DMC11 NUMBER 06
 ;DDCMP LINE# FOR DMC11 NUMBER 06
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 07
 ;VECTOR FOR DMC11 NUMBER 07
 ;DDCMP LINE# FOR DMC11 NUMBER 07
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 10
 ;VECTOR FOR DMC11 NUMBER 10
 ;DDCMP LINE# FOR DMC11 NUMBER 10
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 11
 ;VECTOR FOR DMC11 NUMBER 11
 ;DDCMP LINE# FOR DMC11 NUMBER 11
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 12
 ;VECTOR FOR DMC11 NUMBER 12
 ;DDCMP LINE# FOR DMC11 NUMBER 12
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 13
 ;VECTOR FOR DMC11 NUMBER 13
 ;DDCMP LINE# FOR DMC11 NUMBER 13
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 14
 ;VECTOR FOR DMC11 NUMBER 14
 ;DDCMP LINE# FOR DMC11 NUMBER 14
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 15
 ;VECTOR FOR DMC11 NUMBER 15
 ;DDCMP LINE# FOR DMC11 NUMBER 15
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 16
 ;VECTOR FOR DMC11 NUMBER 16
 ;DDCMP LINE# FOR DMC11 NUMBER 16
 ;3RD STATUS WORD

;CONTROL STATUS REGISTER FOR DMC11 NUMBER 17
 ;VECTOR FOR DMC11 NUMBER 17
 ;DDCMP LINE# FOR DMC11 NUMBER 17
 ;3RD STATUS WORD

D03

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 9
DZDMH.P11 09-DEC-76 14:59 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.
360 001700 000000 DM.END: 000000

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DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 10
 DZDMH.P11 09-DEC-76 14:59 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

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361
362                                     :DMC11 PASS COUNT AND ERROR COUNT TABLE
363                                     :-----
364
365 001702 CNT.MAP:
366 001702 000000 PACT00: 0 ;PASS COUNT FOR DMC11 NUMBER 00
367 001704 000000 ERCT00: 0 ;ERROR COUNT FOR DMC11 NUMBER 00
368
369 001706 000000 PACT01: 0 ;PASS COUNT FOR DMC11 NUMBER 01
370 001710 000000 ERCT01: 0 ;ERROR COUNT FOR DMC11 NUMBER 01
371
372 001712 000000 PACT02: 0 ;PASS COUNT FOR DMC11 NUMBER 02
373 001714 000000 ERCT02: 0 ;ERROR COUNT FOR DMC11 NUMBER 02
374
375 001716 000000 PACT03: 0 ;PASS COUNT FOR DMC11 NUMBER 03
376 001720 000000 ERCT03: 0 ;ERROR COUNT FOR DMC11 NUMBER 03
377
378 001722 000000 PACT04: 0 ;PASS COUNT FOR DMC11 NUMBER 04
379 001724 000000 ERCT04: 0 ;ERROR COUNT FOR DMC11 NUMBER 04
380
381 001726 000000 PACT05: 0 ;PASS COUNT FOR DMC11 NUMBER 05
382 001730 000000 ERCT05: 0 ;ERROR COUNT FOR DMC11 NUMBER 05
383
384 001732 000000 PACT06: 0 ;PASS COUNT FOR DMC11 NUMBER 06
385 001734 000000 ERCT06: 0 ;ERROR COUNT FOR DMC11 NUMBER 06
386
387 001736 000000 PACT07: 0 ;PASS COUNT FOR DMC11 NUMBER 07
388 001740 000000 ERCT07: 0 ;ERROR COUNT FOR DMC11 NUMBER 07
389
390 001742 000000 PACT10: 0 ;PASS COUNT FOR DMC11 NUMBER 10
391 001744 000000 ERCT10: 0 ;ERROR COUNT FOR DMC11 NUMBER 10
392
393 001746 000000 PACT11: 0 ;PASS COUNT FOR DMC11 NUMBER 11
394 001750 000000 ERCT11: 0 ;ERROR COUNT FOR DMC11 NUMBER 11
395
396 001752 000000 PACT12: 0 ;PASS COUNT FOR DMC11 NUMBER 12
397 001754 000000 ERCT12: 0 ;ERROR COUNT FOR DMC11 NUMBER 12
398
399 001756 000000 PACT13: 0 ;PASS COUNT FOR DMC11 NUMBER 13
400 001760 000000 ERCT13: 0 ;ERROR COUNT FOR DMC11 NUMBER 13
401
402 001762 000000 PACT14: 0 ;PASS COUNT FOR DMC11 NUMBER 14
403 001764 000000 ERCT14: 0 ;ERROR COUNT FOR DMC11 NUMBER 14
404
405 001766 000000 PACT15: 0 ;PASS COUNT FOR DMC11 NUMBER 15
406 001770 000000 ERCT15: 0 ;ERROR COUNT FOR DMC11 NUMBER 15
407
408 001772 000000 PACT16: 0 ;PASS COUNT FOR DMC11 NUMBER 16
409 001774 000000 ERCT16: 0 ;ERROR COUNT FOR DMC11 NUMBER 16
410
411 001776 000000 PACT17: 0 ;PASS COUNT FOR DMC11 NUMBER 17
412 002000 000000 ERCT17: 0 ;ERROR COUNT FOR DMC11 NUMBER 17
413

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F03

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 11
 DZDMH.P11 09-DEC-76 14:59 PROGRAM PARAMETERS, VARIABLES, AND TRAP CALLS.

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414
 415
 416
 417
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 419

FORMAT OF STATUS TABLE

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	CSR
I	C	O	N	T	R	O	L	I	R	E	G	I	S	T	E	R
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	*	I	*	I	*	I	*	I	*	I	*	I	*	I	*	STAT1
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	*	B	M	I	A	D	D	*	I	*	L	I	N	E	*	STAT2
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	*	STAT3
I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	I	

DEFINITION OF FORMAT

- CSR: CONTAINS DMC11 CSR ADDRESS
- STAT1: BITS 00-08 IS DMC11 VECTOR ADDRESS
 BIT15=1 MICRO-PROCESSOR HAS CROM
 BIT15=0 MICRO-PROCESSOR HAS CROM
 BIT14=1 ??? TURNAROUND CONNECTOR IS ON
 BIT14=0 NO TURNAROUND CONNECTOR
 BIT13=0 LINE UNIT IS AN M8201
 BIT13=1 LINE UNIT IS AN M8202
 BIT12=1 NO LINE UNIT
 BITS 09-11 IS DMC11 BR PRIORITY LEVEL
- STAT2: LOW BYTE IS SWITCH PAC#1 (DDCMP LINE NUMBER)
 HIGH BYTE IS SWITCH PAC#2 (BM873 BOOT ADD)
- STAT3: BIT0=1 DO FREE RUNNING TESTS ON KMC
 (MUST BE SET TO A ONE MANUALLY [PROGRAMS G AND H ONLY])

Address	Op Code	Op	Op2	Op3	Op4	Op5	Op6	Op7	Op8	Op9	Op10	Op11	Op12	Op13	Op14	Op15	Op16	Op17	Op18	Op19	Op20	Op21	Op22	Op23	Op24	Op25	Op26	Op27	Op28	Op29	Op30	Op31	Op32	Op33	Op34	Op35	Op36	Op37	Op38	Op39	Op40	Op41	Op42	Op43	Op44	Op45	Op46	Op47	Op48	Op49	Op50	Op51	Op52	Op53	Op54	Op55	Op56	Op57	Op58	Op59	Op60	Op61	Op62	Op63	Op64	Op65	Op66	Op67	Op68	Op69	Op70	Op71	Op72	Op73	Op74	Op75	Op76	Op77	Op78	Op79	Op80	Op81	Op82	Op83	Op84	Op85	Op86	Op87	Op88	Op89	Op90	Op91	Op92	Op93	Op94	Op95	Op96	Op97	Op98	Op99	Op100	Op101	Op102	Op103	Op104	Op105	Op106	Op107	Op108	Op109	Op110	Op111	Op112	Op113	Op114	Op115	Op116	Op117	Op118	Op119	Op120	Op121	Op122	Op123	Op124	Op125	Op126	Op127	Op128	Op129	Op130	Op131	Op132	Op133	Op134	Op135	Op136	Op137	Op138	Op139	Op140	Op141	Op142	Op143	Op144	Op145	Op146	Op147	Op148	Op149	Op150	Op151	Op152	Op153	Op154	Op155	Op156	Op157	Op158	Op159	Op160	Op161	Op162	Op163	Op164	Op165	Op166	Op167	Op168	Op169	Op170	Op171	Op172	Op173	Op174	Op175	Op176	Op177	Op178	Op179	Op180	Op181	Op182	Op183	Op184	Op185	Op186	Op187	Op188	Op189	Op190	Op191	Op192	Op193	Op194	Op195	Op196	Op197	Op198	Op199	Op200	Op201	Op202	Op203	Op204	Op205	Op206	Op207	Op208	Op209	Op210	Op211	Op212	Op213	Op214	Op215	Op216	Op217	Op218	Op219	Op220	Op221	Op222	Op223	Op224	Op225	Op226	Op227	Op228	Op229	Op230	Op231	Op232	Op233	Op234	Op235	Op236	Op237	Op238	Op239	Op240	Op241	Op242	Op243	Op244	Op245	Op246	Op247	Op248	Op249	Op250	Op251	Op252	Op253	Op254	Op255	Op256	Op257	Op258	Op259	Op260	Op261	Op262	Op263	Op264	Op265	Op266	Op267	Op268	Op269	Op270	Op271	Op272	Op273	Op274	Op275	Op276	Op277	Op278	Op279	Op280	Op281	Op282	Op283	Op284	Op285	Op286	Op287	Op288	Op289	Op290	Op291	Op292	Op293	Op294	Op295	Op296	Op297	Op298	Op299	Op300	Op301	Op302	Op303	Op304	Op305	Op306	Op307	Op308	Op309	Op310	Op311	Op312	Op313	Op314	Op315	Op316	Op317	Op318	Op319	Op320	Op321	Op322	Op323	Op324	Op325	Op326	Op327	Op328	Op329	Op330	Op331	Op332	Op333	Op334	Op335	Op336	Op337	Op338	Op339	Op340	Op341	Op342	Op343	Op344	Op345	Op346	Op347	Op348	Op349	Op350	Op351	Op352	Op353	Op354	Op355	Op356	Op357	Op358	Op359	Op360	Op361	Op362	Op363	Op364	Op365	Op366	Op367	Op368	Op369	Op370	Op371	Op372	Op373	Op374	Op375	Op376	Op377	Op378	Op379	Op380	Op381	Op382	Op383	Op384	Op385	Op386	Op387	Op388	Op389	Op390	Op391	Op392	Op393	Op394	Op395	Op396	Op397	Op398	Op399	Op400	Op401	Op402	Op403	Op404	Op405	Op406	Op407	Op408	Op409	Op410	Op411	Op412	Op413	Op414	Op415	Op416	Op417	Op418
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H03

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 13
 DZDMH.P11 09-DEC-76 14:59 PROGRAM INITIALIZATION AND START UP.

PAGE: 0033

526	002312	000000			HALT		: STOP THE SHOW
527	002314	000776			BR	.-2	: DISQUALIFY CONTINUE SWITCH
528	002316	004737	010252		17\$: JSR	PC,AUTO.SIZE	: GO DO THE AUTO SIZE
529	002322	105737	001324		16\$: TSTB	INIFLG	: FIRST TIME?
530	002326	001410			BEQ	21\$	: BR IF YES
531	002330	105737	001236		TSTB	STATSW	: IF USING SAME PARAMETERS DONT TYPE MAP
532	002334	100431			BMI	1\$	
533	002336	032737	000006	001236	BIT	#BIT1!BIT2,STATSW	: IS TEST NO. OR LOCK SELECTED
534	002344	001403			BEQ	24\$	: IF NO THEN TYPE STATUS
535	002346	000424			BR	1\$	: IF YES DO NOT TYPE STATUS
536	002350	005137	001324		21\$: COM	INIFLG	: SET FLAG
537	002354	104402	006126		24\$: TYPE	,XHEAD	: TYPE HEADER
538	002360	012704	001500		MOV	#DM.MAP,R4	: SET POINTER
539	002364	010437	001246		5\$: MOV	R4,TEMP1	: SET ADDRESS
540	002370	012437	001250		MOV	(R4)+,TEMP2	: SET CSR
541	002374	001411			BEQ	1\$	: ALL DONE IF ZERO
542	002376	012437	001252		MOV	(R4)+,TEMP3	: SET STAT1
543	002402	012437	001254		MOV	(R4)+,TEMP4	: SET STAT2
544	002406	012437	001256		MOV	(R4)+,TEMP5	: SET STAT3
545	002412	104410			CONVRT		: TYPE OUT STATUS MAP
546	002414	007230			XSTATQ		
547	002416	000762			BR	5\$	
548	002420	012700	001500		1\$: MOV	#DM.MAP,R0	: R0 POINTS TO STATUS TABLE
549							
550							
551							
552							
553							
554							
555							
556							
557							
558							
559							
560	002424	013746	000004		MOV	#4,-(SP)	: SAVE LOC 4
561	002430	013746	000006		MOV	#6,-(SP)	: SAVE LOC 6
562	002434	005037	000006		CLR	#6	: CLEAR VEC+2
563	002440	005037	001252		CLR	TEMP3	: CLEAR FLAG
564	002444	005005			CLR	R5	: R5=0=DMC, R5=-1=KMC
565	002446	011037	001404		AUSTR: MOV	(R0),DMCSR	: GET NEXT DMC CSR
566	002452	001530			BEQ	AUDONE	: BR IF DONE
567	002454	005705			TST	R5	: DMC OR KMC?
568	002456	001005			BNE	1\$	: BR IF KMC
569	002460	032760	100000	000002	BIT	#BIT15,2(R0)	: CHECK FOR DMC CSR
570	002466	001044			BNE	OK	: SKIP IF NOT DMC
571	002470	000404			BR	2\$	: ITS A DMC SO CONTINUE
572	002472	032760	100000	000002	1\$: BIT	#BIT15,2(R0)	: CHECK FOR KMC CSR
573	002500	001437			BEQ	OK	: SKIP IF NOT KMC
574	002502	012737	002606	000004	2\$: MOV	#NODEV,#4	: SET UP FOR TIMEOUT
575	002510	005705			TST	R5	: DMC OR KMC?
576	002512	001003			BNE	3\$	: BR IF KMC
577	002514	012703	000006		MOV	#6,R3	: R3 IS COUNT OF DEVICES BEFORE DMC
578	002520	000402			BR	4\$	: GO ON
579	002522	012703	000010		3\$: MOV	#10,R3	: R3 IS COUNT OF DEVICES BEFORE KMC
580	002526	012702	002722		4\$: MOV	#DEVTAB,R2	: R2 IS DEVICE TABLE POINTER
581	002532	012701	160010		MOV	#160010,R1	: START WITH ADDRESS 160010

582	002536	005711		FLOAT:	TST	(R1)	;CHECK ADDRESS IN R1
583	002540	111204			MOVB	(R2),R4	;IF NO TIMEOUT, GET NEXT ADDRESS
584	002542	060401			ADD	R4,R1	;IN R1
585	002544	005201			INC	R1	
586	002546	040401			BIC	R4,R1	
587	002550	005703			TST	R3	;ANY MORE DEVICES TO CHECK FOR?
588	002552	001371			BNE	FLOAT	;BR IF YES
589	002554	012737	002612 000004		MOV	#ERR,2#4	;OK ONLY DMC'S ARE LEFT. SET UP FOR TIMEOUT
590	002562	005711		FY:	TST	(R1)	;CHECK DMC ADDRESS
591	002564	020137	001404		CMP	R1,DMCSR	;DOES IT MATCH
592	002570	001403			BEQ	OK	;BR IF YES
593	002572	062701	000010		ADD	#10,R1	;GET NEXT DMC ADDRESS
594	002576	000771			BR	FY	;DO IT AGAIN
595	002600	062700	000010	OK:	ADD	#10,R0	;SKIP TO NEXT DMC CSR
596	002604	000720			BR	AJSTRT	;CONTINUE
597	002606	122243		NODEV:	CMPB	(R2)+,-(R3)	;ON TIMEOUT, INC R2. DEC R3
598	002610	000002			RTI		;RETURN
599	002612	005737	001252	ERR:	TST	TEMP3	;CHECK FLAG IF = 0 TYPE HEADER
600	002616	001014			BNE	1\$	;SKIP HEADER
601	002620	104402			TYPE		;TYPEOUT HEADER MESSAGE
602	002622	007125			CONERR		;CONFIGURATION ERROR!!!!
603	002624	012737	002612 001276		MOV	#ERR,SAVPC	;SAVE PC FOR TYPEOUT
604	002632	104411			CNVRT		;TYPE OUT ERROR PC
605	002634	002702			ERRPC		
606	002636	104402			TYPE		;TYPE REST OF HEADER
607	002640	007167			CNERR		
608	002642	012737	177777 001252		MOV	#-1,TEMP3	;SET FLAG SO IT ONLY GETS TYPED ONCE
609	002650	010137	001262	1\$:	MOV	R1,SAVR1	;SAVE R1 FOR TYPEOUT
610	002654	104410			CONVRT		
611	002656	002710			CONTAB		;TYPE CSR VALUES
612	002660	005705			TST	R5	;DMC OR KMC
613	002662	001003			BNE	3\$	;BR IF KMC
614	002664	104402			TYPE		
615	002666	007210			DMCM		
616	002670	000402			BR	4\$	;CONTINUE
617	002672	104402		3\$:	TYPE		
618	002674	007220			KMCM		
619	002676	022626		4\$:	CMP	(SP)+,(SP)+	;ADJUST STACK
620	002700	000737			BR	OK	;BR TO GET OUT
621	002702	000001		ERRPC:	1		
622	002704	006	002		.BYTE	6,2	
623	002706	001276			SAVPC		
624	002710	000002		CONTAB:	2		
625	002712	006	004		.BYTE	6,4	
626	002714	001262			SAVR1		
627	002716	006	002		.BYTE	6,2	
628	002720	001404			DMCSR		
629	002722	007		DEVTAB:	.BYTE	7	;DJ
630	002723	017			.BYTE	17	;DH
631	002724	007			.BYTE	7	;DQ
632	002725	007			.BYTE	7	;DU
633	002726	007			.BYTE	7	;DUP
634	002727	007			.BYTE	7	;LK
635	002730	007			.BYTE	7	;DMC
636	002731	007			.BYTE	7	;DZ
637	002732	007			.BYTE	7	;KMC

638		002734		.EVEN			
639	002734	005705		AUDONE:	TST	R5	:DMC?
640	002736	001005			BNE	1\$	:BR IF KMC AND ALL DONE
641	002740	012705	177777		MOV	#-1,R5	:SET R5 TO -1 (KMC)
642	002744	012700	001500		MOV	#DM.MAP,RO	:RESET RO TO START OF TABLE
643	002750	000636			BR	AUSTR	:GO DO KMC'S
644	002752	012637	000006	1\$:	MOV	(SP)+,2#6	:RESTORE LOC 6
645	002756	012637	000004		MOV	(SP)+,2#4	:RESTORE LOC 4
646	002762	032737	000010	001236	BIT	#SW03,STRSW	:SELECT SPECIFIC DEVICES??
647	002770	001422			BEQ	3\$	:BR IF NO.
648	002772	104402	006046		TYPE	MNEW	:TYPE THE MESSAGE.
649	002776	005000			CLR	RO	:ZERO DATA LIGHTS
650	003000	000000			HALT		:WAIT FOR USER TO TELL WHAT DEVICES TO RUN
651	003002	027737	176174	001312	CMP	2SWR.SAVACT	:IS THE NUMBER VALID?
652	003010	101404			BLOS	2\$	:BR IF NUMBER IS OK.
653	003012	104402	005707		TYPE	,MERR3	:TELL USER OF INVALID NUMBER.
654	003016	000000			HALT		:STOP EVERY THING.
655	003020	000776			BR	.-2	:RESTART THE PROGRAM AGAIN.
656	003022	017737	176154	001306	2\$:	MOV 2SWR.DMACTV	:GET NEW DEVICE PATTERN
657	003030	013700	001306		MOV	DMACTV,RO	:SHOW THE USER WHAT HE SELECTED.
658	003034	000000			HALT		:CONTINUE DYNAMIC SWITCHES.
659	003036	012700	000300		3\$:	MOV #300,RO	:PREPARE TO CLEAR THE FLOATING
660	003042	012701	000302		MOV	#302,R1	:VECTOR AREA. 300-776
661	003046	010120			4\$:	MOV R1,(RO)+	:START PUTTING "PC+2 - HALT"
662	003050	005021			CLR	(R1)+	:IN VECTOR AREA.
663	003052	022021			CMP	(RO)+,(R1)+	:POP POINTERS
664	003054	022700	001000		CMP	#1000,RO	:ALL DONE??
665	003060	001372			BNE	4\$	:BR IF NO.
666							
667							
668							
669							
670	003062	012706	001200		.BEGIN:	MOV #STACK,SP	:SET UP STACK
671	003066	013746	000006			MOV 2#6,-(SP)	:SAVE LOC 6
672	003072	013746	000004			MOV 2#4,-(SP)	:SAVE LOC 4
673	003076	005000				CLR RO	:START AT 0
674	003100	012737	003144	000004		MOV #2\$,2#4	:SET UP FOR TIME OUT
675	003106	005037	000006			CLR 2#6	:TO AUTOSIZE MEMORY
676	003112	005720			6\$:	TST (RO)+	:CHECK ADDRESS IN RO
677	003114	022700	157776			CMP #157776,RO	:IS IT AT LEAST 28K
678	003120	001374				BNE 6\$	:BR IF NO
679	003122	162700	007776			SUB #7776,RO	:SAVE 2K FOR MONITORS
680	003126	010037	001304		7\$:	MOV RO,MEMLIM	:STORE MEMORY LIMIT
681	003132	012637	000004			MOV (SP)+,2#4	:RESTORE LOC 4
682	003136	012637	000006			MOV (SP)+,2#6	:RESTORE LOC 6
683	003142	000413				BR 10\$	:CONTINUE
684	003144	022526			2\$:	CMP (SP)+,(SP)+	:ADJUST STACK
685	003146	162700	000004			SUB #4,RO	:GET LAST GOOD ADDRESS
686	003152	162700	00777			SUB #7776,RO	:SAVE 2K FOR MONITORS
687	003156	022700	030000			CMP #30000,RO	:IS IT 8K?
688	003162	001361				BNE 7\$	:BR IF NO
689	003164	012700	037400			MOV #37400,RO	:IF 8K DON'T SAVE 2K
690	003170	000756				BR 7\$	
691	003172	012737	000340	177776	10\$:	MOV #340,PS	:LOCK OUT INTERRUPTS
692	003200	032737	000004	001236		BIT #BIT2,STRSW	:CHECK FOR LOCK ON TEST
693	003206	001411				BEQ 1\$	:BR IF NO LOCK DESIRED.

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694	003210	104402	005745		TYPE	MLOCK	:TYPE LOCK SELECTED.
695	003214	012737	000240	003522	MOV	#NOP,TTST	:ADJUST SCOPE ROUTINE.
696	003222	012737	000240	003524	MOV	#NOP,TTST+2	:SET UP TO LOCK
697	003230	000406			BR	3\$	:CONTINUE ALONG.
698	003232	013737	003640	003522	1\$: MOV	BRW,TTST	:PREPARE NORMAL SCOPE ROUTINE
699	003240	013737	003642	003524	MOV	BRX,TTST+2	:LOCK NOT SELECTED, SET UP FOR NORMAL SCOPE LOOP
700	003246	012737	007620	001214	3\$: MOV	#CYCLE,RETURN	:START AT "CYCLE" FIND WHICH DEVICE TO TEST
701	003254	032737	000002	001236	4\$: BIT	#SW01,STRTSW	:IS TEST NO. SELECTED?
702	003262	001002			BNE	5\$	:BR IF YES
703	003264	104402	005657		TYPE	MR	:TYPE R
704	003270	000177	175720		5\$: JMP	\$RET*LRN	:START TESTING

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

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761	003514	032777	040000	175460		TTST:	BIT	#BIT14,2SWR	;"LOOP ON THIS TEST?"
762	003522	001407					BEQ	1\$	;BR IF NO. (IF LOCK SW01=1; THIS LOC =240)
763	003524	000437					BR	3\$	;GOTO 3\$ (IF LOCK SW01=1; THIS LOC =240)
764	003526	105777	175452				TSTB	2TKCSR	;KEYBOARD DONE?
765	003532	100034					BPL	3\$	;BR IF NO. (LOCK: HIT KEY TO GOTO NEXT TEST)
766	003534	017700	175446				MOV	2TKDBR,RO	;CLEAR DONE BIT
767	003540	000415					BR	2\$	;CONTINUE
768	003542	032777	004000	175432		1\$:	BIT	#SW11,2SWR	;DELETE ITERATION? (QUICK PASS)
769	003550	001011					BNE	2\$	;BR IF YES
770	003552	105737	001327				TSTB	QV.FLG	;HAVE PASSES BEEN COMPLETED?
771	003556	001406					BEQ	2\$	;BR IF QUICK PASS.
772	003560	005237	001224				INC	LPCNT	;UPDATE ITERATION COUNTER
773	003564	023737	001224	001222			CMP	LPCNT,ICOUNT	;ARE ALL ITERATIONS DONE?"
774	003572	101414					BLOS	3\$	;BR IF NOT YET
775	003574	105037	001325			2\$:	CLRB	ERRFLG	;PREPARE FOR NEW TEST
776	003600	005037	001224				CLR	LPCNT	;START ICOUNTER AT 0
777	003604	005037	001220				CLR	LOCK	
778	003610	012737	000020	001222			MOV	#20,ICOUNT	;RESET ITERATIONS
779	003616	013737	001216	001214			MOV	NEXT,RETURN	;GET NEXT TEST
780	003624	011600				3\$:	MOV	(SP),RO	;POP RO OFF OF THE STACK
781	003626	022626					POP2SP		;FAKE AN "RTI"
782	003630	013701	001404				MOV	DMCSR,R1	;R1 CONTAINS BASE DMC ADDRESS
783	003634	000177	175354				JMP	2RETURN	;GO DO THE TEST
784	003640	001407				BRW:	1407		
785	003642	000437				BRX:	437		
786									
787									
788									
789									
790	003644	004737	007362			.SCOPI:	JSR	PC,CKSWR	;CHECK FOR SOFT SWR
791	003650	032777	001000	175324			BIT	#SW09,2SWR	;IS SW09=1(SET)?
792	003656	001405					BEQ	1\$	;BR IF NOT SET.
793	003660	005737	001220				TST	LOCK	
794	003664	001402					BEQ	1\$	
795	003666	013716	001220				MOV	LOCK,(SP)	;GOTO THE ADDRESS IN LOCK.
796	003672	000002				1\$:	RTI		;GO BACK.
797									
798									
799									
800									
801	003674	010546				.TYPE:	MOV	R5,-(SP)	;SAVE R5 ON THE STACK.
802	003676	017605	000002				MOV	22(SP),R5	;GET ADDRESS OF MESSAGE.
803	003702	062766	000002	000002			ADD	#2,2(SP)	;POP OVER ADDRESS.
804	003710	005737	007556			4\$:	TST	SWFLG	;SOFT SWR MESSAGE?
805	003714	001004					BNE	1\$	;IF YES TYPE IT OUT REGARDLESS OF SW12
806	003716	032777	010000	175256			BIT	#SW12,2SWR	;INHIBIT ALL PRINT OUT?"
807	003724	001012					BNE	3\$	;BR IF NO PRINT OUT WANTED (SW12=1)
808	003726	105715				1\$:	TSTB	(R5)	;IS NUMBER MINUS? (MSB=1(BIT7))
809	003730	100002					BPL	2\$	;BR IF NUMBER IS PLUS
810	003732	104402	005574				TYPE	MCRLF	;TYPE A CR/LF!
811	003736	105777	175246			2\$:	TSTB	2TPCSR	;TTY READY?
812	003742	100375					BPL	2\$	;BR IF NO.
813	003744	112577	175242				MOV8	(R5)+,2TPDBR	;PRINT CURRENT CHAR.
814	003750	001357					BNE	4\$	;IF NOT ZERO KEEP PRINTING!
815	003752	012605				3\$:	MOV	(SP)+,R5	;END OF OUTPUT. RESTORE R5
816	003754	000002					RTI		;GO HOME

;CHECK FOR FREEZE ON CURRENT DATA

;TELETYPE OUTPUT ROUTINE

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

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817
818
819 003756 010346 .INSTR: MOV R3,-(SP) ;SAVE R3 ON STACK
820 003760 010446 MOV R4,-(SP) ;SAVE R4 ON STACK
821 003762 017637 000004 004000 MOV #4(SP),.MSG
822 003770 062766 000002 000004 ADD #2,4(SP)
823 003776 104402 .INST1: TYPE
824 004000 000000 .MSG: 0
825 004002 J12704 007256 MOV #INBUF,R4
826 004006 012703 000007 MOV #7,R3
827 004012 105777 175166 1S: TSTB @TKCSR
828 004016 100375 BPL 1S
829 004020 117714 175162 MOVB @TKDBR,(R4)
830 004024 142714 000200 BICB #200,(R4)
831 004030 122427 000015 CMPB (R4)+,#15
832 004034 001417 BEQ INSTR2
833 004036 105777 175146 2S: TSTB @TPCSR
834 004042 100375 BPL 2S
835 004044 017777 175136 175140 MOV @TKDBR,@TPDBR
836 004052 005303 DEC R3
837 004054 001356 BNE 1S
838 004056 012604 MOV (SP)+,R4
839 004060 012603 MOV (SP)+,R3
840 004062 104402 005570 .INSTE: TYPE MQM
841 004066 010346 MOV R3,-(SP)
842 004070 010446 MOV R4,-(SP)
843 004072 000741 BR .INST1
844 004074 012604 INSTR2: MOV (SP)+,R4 ;RESTORE R4
845 004076 012603 MOV (SP)+,R3 ;RESTORE R3
846 004100 000002 RTI
847
848 ;CONVERT ASCII STRING TO OCTAL
849
850
851 004102 010546 .PARAM: MOV R5,-(SP)
852 004104 010446 MOV R4,-(SP)
853 004106 016605 000004 MOV #4(SP),R5
854 004112 012537 004272 MOV (R5)+,LOLIM
855 004116 012537 004274 MOV (R5)+,HILIM
856 004122 012537 004276 MOV (R5)+,DEVADR
857 004126 112537 004300 MOVB (R5)+,LOBITS
858 004132 112537 004301 MOVB (R5)+,ADRCNT
859 004136 010566 000004 MOV R5,4(SP)
860 004142 005005 PARAM1: CLR R5
861 004144 012704 007256 MOV #INBUF,R4
862 004150 122714 000015 CMPB #15,(R4)
863 004154 001420 BEQ PARERR
864 004156 121427 000060 1S: CMPB (R4),#60
865 004162 002415 BLT PARERR
866 004164 121427 000067 CMPB (R4),#67
867 004170 003012 BGT PARERR
868 004172 142714 000060 BICB #60,(R4)
869 004176 152405 BISB (R4)+,R5
870 004200 122714 000015 CMPB #15,(R4)
871 004204 001406 BEQ LIMITS
872 004206 006305 ASL R5

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873	004210	006305		ASL	R5	
874	004212	006305		ASL	R5	
875	004214	000760		BR	1\$	
876	004216	104404		PARERR: INSTER		
877	004220	000750		BR	PARAM1	
878						
879						
880						
881						
882	004222	020537	004274	LIMITS: CMP	R5, HILIM	
883	004226	101373		BHI	PARERR	
884	004230	020537	004272	CMP	R5, LOLIM	
885	004234	103770		BLO	PARERR	
886	004236	133705	004300	BITB	LOBITS, R5	
887	004242	001365		BNE	PARERR	
888						
889						
890						
891	004244	013704	004276			
892	004250	010524		1\$: MOV	DEVADR, R4	
893	004252	062705	000002	MOV	R5, (R4)+	
894	004256	105337	004301	ADD	#2, R5	
895	004262	001372		DECB	ADRCNT	
896	004264	012604		BNE	1\$	
897	004266	012605		MOV	(SP)+, R4	
898	004270	000002		MOV	(SP)+, R5	
899	004272	000000		RTI		
900	004274	000000		LOLIM:	0	
901	004276	000000		HILIM:	0	
902	004300	000000		DEVADR:	0	
903		004301		LOBITS:	0	
904				ADRCNT=LOBITS+1		
905						
906						
907						
908	004302	016637	000004 001276	.SAV05: MOV	4(SP), SAVPC	;SAVE R7 (PC)
909						
910						
911						
912	004310	010537	001272	SV05: MOV	R5, SAVR5	;SAVE R5
913	004314	010437	001270	MOV	R4, SAVR4	;SAVE R4
914	004320	010337	001266	MOV	R3, SAVR3	;SAVE R3
915	004324	010237	001264	MOV	R2, SAVR2	;SAVE R2
916	004330	010137	001262	MOV	R1, SAVR1	;SAVE R1
917	004334	010037	001260	MOV	R0, SAVR0	;SAVE R0
918	004340	000002		RTI		;LEAVE.
919						
920						
921						
922	004342	013700	001260	.RES05: MOV	SAVR0, R0	;RESTORE R0
923	004346	013701	001262	MOV	SAVR1, R1	;RESTORE R1
924	004352	013702	001264	MOV	SAVR2, R2	;RESTORE R2
925	004356	013703	001266	MOV	SAVR3, R3	;RESTORE R3
926	004362	013704	001270	MOV	SAVR4, R4	;RESTORE R4
927	004366	013705	001272	MOV	SAVR5, R5	;RESTORE R5
928	004372	000002		RTI		;LEAVE

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929
930                                     ; CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
931                                     ;-----
932
933 004374 104402 005574 .CONVR: TYPE MCRLF
934 004400 010046 .CNVRT: MOV R0,-(SP)
935 004402 010146 MOV R1,-(SP)
936 004404 010346 MOV R3,-(SP)
937 004406 010446 MOV R4,-(SP)
938 004410 010546 MOV R5,-(SP)
939 004412 017601 000012 MOV @12(SP),R1
940 004416 062766 000002 000012 ADD #2,12(SP)
941 004424 012137 004616 MOV (R1)+,WRDCNT
942 004430 112137 004620 1$: MOV B (R1)+,CHRCNT
943 004434 112137 004621 MOV B (R1)+,SPACNT
944 004440 013137 004622 MOV @ (R1)+,BINWRD
945 004444 122737 000003 004620 CMP B #3,CHRCNT
946 004452 001003 BNE 2$
947 004454 042737 177400 004622 BIC #177400,BINWRD
948 004462 013704 004622 2$: MOV BINWRD,R4
949 004466 113705 004620 MOV B CHRCNT,R5
950 004472 012700 001416 MOV #TEMP,R0
951 004476 010403 3$: MOV R4,R3
952 004500 042703 177770 BIC #177770,R3
953 004504 062703 000060 ADD #060,R3
954 004510 110320 MOV B R3,(R0)+
955 004512 000241 CLC
956 004514 006004 ROR R4
957 004516 000241 CLC
958 004520 006004 ROR R4
959 004522 000241 CLC
960 004524 006004 ROR R4
961 004526 005305 DEC R5
962 004530 001362 BNE 3$
963 004532 012703 007320 MOV #MDATA,R3
964 004536 114023 4$: MOV B -(R0),(R3)+
965 004540 105337 004620 DECB CHRCNT
966 004544 001374 BNE 4$
967 004546 105737 004621 TST B SPACNT
968 004552 001405 BEQ 6$
969 004554 112723 000040 5$: MOV B #040,(R3)+
970 004560 105337 004621 DECB SPACNT
971 004564 001373 BNE 5$
972 004566 105013 6$: CLRB (R3)
973 004570 104402 007320 TYPE ,MDATA
974 004574 005337 004616 DEC WRDCNT
975 004600 001313 BNE 1$
976 004602 012605 MOV (SP)+,R5
977 004604 012604 MOV (SP)+,R4
978 004606 012603 MOV (SP)+,R3
979 004610 012601 MOV (SP)+,R1
980 004612 012600 MOV (SP)+,R0
981 004614 000002 RTI
982 004616 000000 WRDCNT: 0
983 004620 000000 CHRCNT: 0
984 004621 004621 SPACNT=CHRCNT+1

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985 004622 000000      BINWRD: 0
986
987
988      ;TRAP DISPATCH SERVICE
989      ;ARGUMENT OF TRAP IS EXTRACTED
990      ;AND USED AS OFFSET TO OBTAIN POINTER
991      ;TO SELECTED SUBROUTINE
992
993 004624 011646      .TRPSR: MOV      (SP), -(SP)      ;GET PC OF RETURN
994 004626 162716 000002 SUB      #2, (SP)      ;=PC OF TRAP
995 004632 017616 000000 MOV      @ (SP), (SP)      ;GET TRP
996 004636 006316      TRPOK: ASL      (SP)      ;MULTIPLY TRAP ARG BY 2
997 004640 042716 177001 BIC      #177001, (SP)      ;CLEAR UNWANTED BITS
998 004644 062716 001330 ADD      #.TRPTAB, (SP)      ;POINTER TO SUBROUTINE ADDRESS
999 004650 017616 000000 MOV      @ (SP), (SP)      ;SUBROUTINE ADDRESS
1000 004654 000136      JMP      @ (SP)+      ;GO TO SUBROUTINE
1001
1002      ;ERROR HANDLER
1003      ;-----
1004
1005 004656 004737 007362      .HLT: JSR      PC, CKSWR      ;CHECK FOR SOFT SWR
1006 004662 032777 010000 174312 BIT      #SW12, @SWR      ;BELL ON ERROR?
1007 004670 001406      BEQ      XBX      ;BR IF NO BELL
1008 004672 105777 174312 TSTB      @TPCSR      ;TTY READY.
1009 004676 100003      BPL      XBX      ;DON'T WAIT IF TTY NOT READY.
1010 004700 112777 000207 174304 MOVB      #207, @TPOBR      ;PUSH A BELL AT THE TTY.
1011 004706 032777 020000 174266 XBX: BIT      #SW13, @SWR      ;DELETE ERROR PRINT OUT?
1012 004714 001105      BNE      HALTS      ;BR IF NO PRINT OUT WANTED.
1013 004716 021637 001234 CMP      (SP), LSTERR      ;WAS THIS ERROR FOUND LAST TIME?
1014 004722 001404      BEQ      1$      ;BR IF YES
1015 004724 011637 001234 MOV      (SP), LSTERR      ;RECORD BEING HERE
1016 004730 105037 001325 CLRB      ERRFLG      ;PREPARE HEADER
1017 004734 104406      1$: SAVO5      ;SAVE ALL PROC REGISTERS
1018 004736 011605      MOV      (SP), R5      ;GET THE PC OF ERROR
1019 004740 162705 000002 SUB      #2, R5      ;GET ADDRESS OF TRAP CALL
1020 004744 011504      MOV      (R5), R4      ;GET HLT INSTRUCTION
1021 004746 006304      ASL      R4      ;MULT BY TWO
1022 004750 061504      ADD      (R5), R4      ;DOUBLE IT
1023 004752 006304      ASL      R4      ;MULT AGAIN
1024 004754 042704 177001 BIC      #177001, R4      ;CLEAR JUNK
1025 004760 062704 037270 ADD      #.ERRTAB, R4      ;GET POINTER
1026 004764 012437 005100 MOV      (R4)+, ERRMSG      ;GET ERROR MESSAGE
1027 004770 012437 005112 MOV      (R4)+, DATAHD      ;GET DATA HEADRER
1028 004774 011437 005124 MOV      (R4), DATABP      ;GET DATA TABLE
1029 005000 105737 001325 TSTB      ERRFLG      ;TYPE HEADREER
1030 005004 001403      BEQ      TYPMSG      ;BR IF YES
1031 005006 005737 005124 TST      DATABP      ;DOES DATA TABLE EXIST?
1032 005012 001040      BNE      TYPDAT      ;BR IF YES.
1033 005014 104402 005574 TYPMSG: TYPE      , MCRLF      ;
1034 005020 104402 005574 TYPE      , MCRLF      ;
1035 005024 005737 001220 TST      LOCK      ;
1036 005030 001402      BEQ      1$      ;
1037 005032 104402 006044 TYPE      , MASTEK      ;
1038 005036 104402 006032 TYPE      , MTSTN      ;
1039 005042 104411 005232 CNVRT      , XTSTN      ;SHOW IT
1040 005046 104402 006121 TYPE      , MERRPC      ;TYPE PC.

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1041	005052	104411	005224		CNVRT	,ERTABO	;SHOW IT
1042	005056	104402	005574		TYPE	,MCRLF	;GIVE A CR/LF
1043	005062	112737	177777	001325	MOVB	#-1,ERRFLG	;NO MORE HEADER UNLESS NO DATA TABLE.
1044	005070	005737	005100		TST	ERRMSG	;IS THERE AN ERROR MESSAGE?
1045	005074	001402			BEQ	WRK0.FM	;BR IF NO.
1046	005076	104402			TYPE		;TYPE
1047	005100	000000			ERRMSG: 0		ERROR MESSAGE
1048	005102				WRK0.FM:		
1049	005102	005737	005112		TST	DATAHD	;DATA HEADER?
1050	005106	001402			BEQ	TYPDAT	;BR IF NO
1051	005110	104402			TYPE		;TYPE
1052	005112	000000			DATAHD: 0		DATA HEADER
1053	005114	005737	005124		TYPDAT: TST	DATABP	;DATA TABLE?
1054	005120	001402			BEQ	RESREG	;BR IF NO.
1055	005122	104410			CONVRT		SHOW
1056	005124	000000			DATABP: 0		DATA TABLE
1057	005126	104407			RESREG: RES05		RESTORE PROC REGISTERS
1058	005130	022737	003432	000042	HALTS: CMP	#SENDAD,2*42	;IF ACT-11 AUTOMATIC MODE, HALT!!
1059	005136	001403			BEQ	1\$	
1060	005140	005777	174036		TST	2\$WR	;HALT ON ERROR?
1061	005144	100005			BPL	EXITER	;BR IF NO HALT ON ERROR
1062	005146	010046			1\$: PUSHRO		;SAVE R0
1063	005150	016600	000002		MOV	2(SP),R0	;SHOW ERROR PC IN DATA LIGHTS
1064	005154	000000			HALT		HALT
1065	005156	012600			POPPO		GET R0
1066	005160	005237	001232		EXITER: INC	ERRCNT	UPDATE ERROR COUNT
1067	005164	032777	000400	174010	BIT	#SW08,2\$WR	;GOTO TOP OF TEST?
1068	005172	001007			BNE	1\$	;BR IF YES
1069	005174	032777	002000	174000	BIT	#SW10,2\$WR	;GOTO NEXT TEST?
1070	005202	001407			BEQ	2\$	;BR IF NO
1071	005204	013737	001216	001214	MOV	NEXT,RETURN	;SET FOR NEXT TEST
1072	005212	012706	001200		1\$: MOV	#STACK,SP	;RESET SP
1073	005216	000177	173772		JMP	2\$RETURN	;GOTO SPECIFIED TEST
1074	005222	000002			2\$: RTI		;RETURN
1075	005224	000001			ERTABO: 1		
1076	005226	006	002		.BYTE	6,2	
1077	005230	001276			SAVPC		
1078	005232	000001			XTSTN: 1		
1079	005234	003	002		.BYTE	3,2	
1080	005236	001226			TSTNO		
1081							;ENTER HERE ON POWER FAILURE
1082							-----
1083							
1084							
1085	005240				.PFAIL:		
1086	005240	012737	005252	000024	MOV	#RESTART,24	;SET UP FOR POWER UP TRAP
1087	005246	000000			HALT		;HALT ON POWER DOWN NORMAL
1088	005250	000777			BR	.	
1089							
1090							;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
1091							
1092	005252				RESTAR:		
1093	005252	012737	005240	000024	MOV	#.PFAIL,24	;SET UP FOR POWER FAILURE
1094	005260	012706	001200		MOV	#STACK,SP	;RESET THE STACK POINTER
1095	005264	013701	001404		MOV	DMCSR,R1	;RESTORE R1
1096	005270	005037	001416		CLR	TEMP	;READY FOR TIMER

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1097 005274 005237 001416 INC TEMP ;PLUS ONE TO THE TIMER!
1098 005300 001375 BNE .-4 ;BR IF MORE TO GO
1099 005302 104402 005577 TYPE ,MPFAIL ;TYPE THE MESSAGE
1100 005306 104411 005332 CNVRT ,PFTAB ;TELL WHAT TEST TO RETURN TO.
1101 005312 105037 001325 CLRB ERRFLG ;START CLEAN
1102 005316 005037 001234 CLR LSTERR ;.....
1103 005322 005011 CLR (R1) ;CLEAR MAINT BITS
1104 005324 104412 MSTCLR ;START CLEAN UP OF DEVICE
1105 005326 000177 173662 JMP ;START DOING THAT TEST AGAIN.
1106 005332 000001 PFTAB: 1
1107 005334 003 002 .BYTE 3,2
1108 005336 001226 TSTNO
1109
1110 005340 .DELAY:
1111 005340 012777 000020 174044 MOV #20,DMPO4
1112 005346 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1113 005350 121111 121111 ;POKE CLOCK DELAY BIT
1114 005352
1115 005352 104414 1$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1116 005354 121224 121224 ;PORT4+IBUS*11
1117 005356 032777 000020 174026 BIT #BIT4,DMPO4 ;IS CLOCK BIT SET?
1118 005364 001772 BEQ 1$ ;BR IF NO
1119 005366 000002 RTI
1120
1121 005370 .MSTCLR:
1122 005370 152777 000100 174010 BISB #BIT6,DMCSRH ;SET MASTER CLEAR
1123 005376 142777 000300 174002 BICB #BIT6!BIT7,DMCSRH ;CLEAR MASTER CLEAR AND RUN
1124 005404 000002 RTI ;RETURN
1125
1126 005406 .ROMCLK:
1127 005406 152777 000002 173772 BISB #BIT1,DMCSRH ;SET ROMI
1128 005414 013677 173774 MOV #2,DMPO6 ;LOAD INSTRUCTION IN SEL6
1129 005420 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1130 005424 032777 000100 173550 BIT #SW06,DSWR ;HALT IF SW06 =1
1131 005432 001401 BEQ 1$ ;BR IF SW06 =0
1132 005434 000000 HALT ;HALT BEFORE CLOCKING INSTRUCTION
1133 005436 152777 000003 173742 1$: BISB #BIT1!BIT0,DMCSRH ;CLOCK INSTRUCTION
1134 005444 142777 000007 173734 BICB #BIT2!BIT1!BIT0,DMCSRH ;CLEAR ROM0, ROM1, STEP
1135 005452 000002 RTI
1136
1137 005454 .DATACLK:
1138 005454 013637 001416 MOV #2,DMPO6 ;PUT TICK COUNT IN TEMP
1139 005460 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1140 005464 152777 000020 173714 1$: BISB #BIT4,DMCSRH ;SET STEP LU
1141 005472 027777 173706 173704 CMP DMCSR,DMCSR ;WASTE TIME
1142 005500 142777 000020 173700 BICB #BIT4,DMCSRH ;CLEAR STEP LU
1143 005506 005337 001416 DEC TEMP ;DEC TICK COUNT
1144 005512 001364 BNE 1$ ;BR IF NOT DONE
1145 005514 000002 RTI ;RETURN
1146 005516 000001 3$: .BLKW 1
1147
1148 005520 .TIMER:
1149 005520 013637 001416 MOV #2,DMPO6 ;MOVE COUNT TO TEMP
1150 005524 062746 000002 ADD #2,-(SP) ;ADJUST STACK
1151 005530
1152 005530 104414 1$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

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1153 005532 021364
1154 005534 032777 000002 173650
1155 005542 001772
1156 005544
1157 005544 104414
1158 005546 021364
1159 005550 032777 000002 173634
1160 005556 001372
1161 005560 005337 001416
1162 005564 001361
1163 005566 000002
1164 005570 020040 000077
1165 005574 005015 000
1166 005577 377 053520 020122
1167 005635 377 047105 020104
1168 005657 377 000122
1169 005662 047377 020117 042504
1170 005707 377 047111 052523
1171 005733 377 042524 052123
1172 005745 377 047514 045503
1173 005774 051503 035122 000040
1174 006002 042526 035103 000040
1175 006010 040520 051523 051505
1176 006021 105 051122 051117
1177 006032 042524 052123 047040
1178 006044 000052
1179 006046 051777 052105 051440
1180 006121 120 035103 000040
1181 006126 020212 020040 020040
1182 006165 377 020040 020040
1183 006224 020212 050040 020103
1184 006276 026777 026455 026455
1185 006352 044377 053517 046440
1186 006412 041777 051123 040440
1187 006430 053377 041505 047524
1188 006451 377 051102 050040
1189 006510 044777 020106 046504
1190 006606 053777 044510 044103
1191 006720 051777 044527 041524
1192 006756 051777 044527 041524
1193 007016 044777 020123 044124
1194 007056 047377 020117 042504
1195 007107 377 051412 051127
1196 007117 116 053505 020077
1197 007125 377 042377 041515
1198 007167 377 054105 042520
1199 007210 024040 046504 024503
1200 007220 024040 046513 024503
1201 007230 000005
1202 007232 006 003
1203 007234 001246
1204 007236 006 003
1205 007240 001250
1206 007242 006 003

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021364
BIT #2,ADMP04 ;PORT4+IBUS* REG11
BEQ 1$ ;IS PGM CLOCK BIT CLEAR?
;BR IF YES
2$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
021364 ;PORT4+IBUS* REG11
BIT #2,ADMP04 ;IS PGM CLOCK BIT SET?
BNE 2$ ;BR IF YES
DEC TEMP ;DEC COUNT
BNE 1$ ;BR IF NOT DONE
RTI ;RETURN

MQM: .ASCIZ / ?/
MCRLF: .ASCIZ <15><12>
MPFAIL: .ASCIZ <377>/PWR FAILED. RESTART AT TEST /
MEPASS: .ASCIZ <377>/END PASS DZDMH /
MR: .ASCIZ <377>/R/
MERR2: .ASCIZ <377>/NO DEVICES PRESENT./
MERR3: .ASCIZ <377>/INSUFFICIENT DATA!/
MTSTPC: .ASCIZ <377>/TEST PC-/
MLOCK: .ASCIZ <377>/LOCK ON SELECTED TEST/
MCSRX: .ASCIZ /CSR: /
MVECX: .ASCIZ /VEC: /
MPASSX: .ASCIZ /PASSES: /
MERRX: .ASCIZ /ERRORS: /
MTSTN: .ASCIZ /TEST NO: /
MASTEK: .ASCIZ /*/
MNEW: .ASCIZ <377>/SET SWITCH REG TO DMC11'S DESIRED ACTIVE./
MERRPC: .ASCIZ /PC: /
XHEAD: .ASCII <212>/ MAP OF DMC11 STATUS/
      .ASCII <377>/-----/
      .ASCII <212>/ PC CSR STAT1 STAT2 STAT3/
      .ASCIZ <377>/-----/
NUM: .ASCIZ <377>/HOW MANY DMC11'S TO BE TESTED?/
CSR: .ASCIZ <377>/CSR ADDRESS?/
VEC: .ASCIZ <377>/VECTOR ADDRESS?/
PRIO: .ASCIZ <377>/BR PRIORITY LEVEL? (4,5,6,7)?/
CRAM: .ASCIZ <377>/IF DMC HAS CRAM (M8204) TYPE "Y", IF CROM (M8200) TYPE "N"
MODU: .ASCIZ <377>/WHICH LINE UNIT? IF NONE TYPE "N", IF M9201 TYPE "1", IF M
LINE: .ASCIZ <377>/SWITCH PAC#1 (DDCMP LINE #)?/
BM: .ASCIZ <377>/SWITCH PAC#2 (BM873 BOOT ADD)?/
CONN: .ASCIZ <377>/IS THE LOOP BACK CONNECTOR ON?/
NOACT: .ASCIZ <377>/NO DEVICES ARE SELECTED/
SWMES: .ASCIZ <377><12>/SWR= /
SWMES1: .ASCIZ /NEW? /
CONERR: .ASCIZ <377><377>/DMC11 CONFIGURATION ERROR PC: /
CNERR: .ASCIZ <377>/EXPECTED FOUND/
DMCM: .ASCIZ / (DMC) /
KMCM: .ASCIZ / (KMC) /
.EVEN
XSTATQ: 5
      .BYTE 6,3
      TEMP1
      .BYTE 6,3
      TEMP2
      .BYTE 6,3

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1171	007244	001252			TEMP3	
1172	007246	006	003		.BYTE	6,3
1173	007250	001254			TEMP4	
1174	007252	006	002		.BYTE	6,2
1175	007254	001256			TEMP5	
1176				.EVEN		
1177						
1178					;BUFFERS FOR INPUT-OUTPUT	
1179						
1180	007256	000000		INBUF:	0	
1181		007320		.+.40		
1182	007320	000000		MDATA:	0	
1183		007362		.+.40		
1184						
1185						
1186					;ROUTINE USED TO CHANGE SOFTWARE SWITCH	
1187					;REGISTER USING THE CONSOLE TERMINAL	
1188					-----	
1189						
1190	007362	022737	000176	001202	CKSWR:	CMP #SWREG,SWR ;IS THE SOFT SWR BEING USED?
1191	007370	001071			BNE CKSWR5 ;BR IF NO	
1192	007372	022777	000007	171606	CMP #7,@TKDBR ;WAS CTRL G TYPED? (7 BIT ASCII)	
1193	007400	001404			BEQ 1\$;BR IF YES	
1194	007402	022777	000207	171576	CMP #207,@TKDBR ;WAS CTRL G TYPED? (8 BIT ASCII)	
1195	007410	001061			BNE CKSWR5 ;BR IF NO	
1196	007412	010246			1\$: MOV R2,-(SP) ;STORE R2	
1197	007414	010346			MOV R3,-(SP) ;STORE R3	
1198	007416	010446			MOV R4,-(SP) ;STORE R4	
1199	007420	012737	177777	007556	MOV #-1,SWFLG ;SET SOFT TYPE OUT FLAG	
1200	007426	005002			CKSWR1: CLR R2 ;CLEAR NEW SWR CONTENTS	
1201	007430	012704	177777		MOV #-1,R4 ;SET FLAG TO ALL ONES	
1202	007434	104402	007107		TYPE ,SWMES ;TYPE "SWR="	
1203	007440	104411			CKSWR2: CNVRT ;TYPE OUT PRESENT CONTENTS	
1204	007442	007612			SOFTSW ;OF SOFT SWITCH REGISTER	
1205	007444	104402	007117		CKSWR3: TYPE ,SWMES1 ;TYPE "NEW?"	
1206	007450	004737	007560		CKSWR4: JSR PC,INCHAR ;GET RESPONSE	
1207	007454	022703	000015		CMP #15,R3 ;WAS IT A CR?	
1208	007460	001424			BEQ 5\$;BR IF YES	
1209	007462	022703	000012		CMP #12,R3 ;WAS IT A LF?	
1210	007466	001416			BEQ 4\$;BR IF YES	
1211	007470	022703	000025		CMP #25,R3 ;WAS IT CTRL U?	
1212	007474	001754			BEQ CKSWR1 ;BR IF YES(START OVER)	
1213	007476	022703	000007		CMP #7,R3 ;IF CNTRL G GET NEXT CHAR	
1214	007502	001762			BEQ CKSWR4	
1215	007504	005004			CLR R4 ;IT MUST BE A DIGIT SO CLR FLAG	
1216	007506	042703	177770		BIC #177770,R3 ;ONLY 0-7 ARE LEGAL SO MASK OFF BITS	
1217	007512	006302			ASL R2 ;SHIFT R2 3 TIMES	
1218	007514	006302			ASL R2	
1219	007516	006302			ASL R2	
1220	007520	050302			BIS R3,R2 ;ADD LAST DIGIT	
1221	007522	000752			BR CKSWR4 ;GET NEXT CHARACTER	
1222	007524	012766	002002	000006	4\$: MOV #-1,START,6(SP) ;LF WAS TYPED SO GO TO START	
1223	007532	005704			5\$: TST R4 ;IS FLAG CLEAR?	
1224	007534	001002			BNE 6\$;IF NOT DON'T CHANGE SOFT SWR	
1225	007536	010277	171440		MOV R2,@SWR ;IF YES THEN WRITE NEW CONTENTS TO SOFT SWR	
1226	007542	005037	007556		6\$: CLR SWFLG ;CLEAR TYPEOUT FLAG	

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1227	007546	012604		MOV	(SP)+,R4	:RESTORE R4
1228	007550	012603		MOV	(SP)+,R3	:RESTORE R3
1229	007552	012602		MOV	(SP)+,R2	:RESTORE R2
1230	007554	00C207		CKSWR5: RTS	PC	:RETURN
1231						
1232	007556	000000		SWFLG:	0	
1233						
1234	007560	105777	171420	INCHAR: TSTB	@TKCSR	
1235	007564	100375		BPL	.-4	
1236	007566	017703	171414	MOV	@TKDBR,R3	
1237	007572	105777	171412	TSTB	@TPCSR	
1238	007576	100375		BPL	.-4	
1239	007600	010377	171406	MOV	R3,@TPDBR	
1240	007604	042703	000200	BIC	#BIT7,R3	
1241	007610	000207		RTS	PC	
1242						
1243	007612	000001		SOFTSW:	1	
1244	007614	006	002	.BYTE	6,2	
1245	007616	000176		SWREG		

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

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1246
1247
1248
1249
1250
1251
1252
1253
1254
1255 007620 005737 001306 CYCLE: TST DMACTV ;ARE ANY DMC11'S TO BE TESTED?
1256 007624 001004 BNE 1$ ;BR IF OK.
1257 007626 104402 007056 TYPE ,NOACT ;NO DMC11'S SELECTED!!
1258 007632 000000 HALT ;STOP THE SHOW.
1259 007634 000776 BR -2 ;DISQUALIFY CONT. SW.
1260 007636 000241 1$: CLC ;CLEAR PROC. CARRY BIT.
1261 007640 006137 001316 ROL RUN ;UPDATE POINTER
1262 007644 005537 001316 ADC RUN ;CATCH CARRY FROM RUN
1263 007650 062737 000004 001322 ADD #4,MILK ;UPDATE POINTER
1264 007656 062737 000010 001320 ADD #10,CREAM ;UPDATE ADDRESS POINTER.
1265 007664 022737 001700 001320 CMP #DM.MAP+200,CREAM
1266 007672 001006 BNE 2$ ;KEEP GOING: NOT ALL TESTED FOR.
1267 007674 012737 001500 001320 MOV #DM.MAP,CREAM ;RESET ADDRESS POINTER.
1268 007702 012737 001702 001322 MOV #CNT.MAP,MILK ;RESET PASS COUNT POINTER
1269 007710 033737 001316 001306 2$: BIT RUN,DMACTV ;IS THIS ONE ACTIVE?
1270 007716 001747 BEQ 1$ ;BR IF NO
1271 007720 013700 001320 MOV CREAM,R0 ;GET ADDRESS POINTER
1272 007724 013702 001322 MOV MILK,R2 ;GET PASS COUNT POINTER
1273 007730 012037 001404 MOV (R0)+,DMCSR ;LOAD SYSTEM CTRL. REG
1274 007734 011037 001374 MOV (R0),DMRVEC ;LOAD VECTOR
1275 007740 042737 177000 001374 BIC #177000,DMRVEC ;CLEAR UNWANTED BITS
1276 007746 012037 001366 MOV (R0)+,STAT1 ;LOAD STAT1
1277 007752 012037 001370 MOV (R0)+,STAT2 ;LOAD STAT2
1278 007756 012037 001372 MOV (R0)+,STAT3 ;LOAD STAT3
1279 007762 012237 001230 MOV (R2)+,PASCNT ;LOAD PASS COUNT
1280 007766 012237 001232 MOV (R2)+,ERRCNT ;LOAD ERROR COUNT
1281 007772 012700 000002 MOV #2,R0 ;SAVE CORE THIS WAY!
1282 007776 013737 001404 001406 MOV DMCSR,DMCSRH
1283 010004 005237 001406 001410 INC DMCSRH
1284 010010 013737 001406 001410 MOV DMCSRH,DMCTL
1285 010016 005237 001410 001412 INC DMCTL
1286 010022 013737 001410 001412 MOV DMCTL,DMP04
1287 010030 060037 001412 001414 ADD R0,DMP04
1288 010034 013737 001412 001414 MOV DMP04,DMP06
1289 010042 060037 001414 001414 ADD R0,DMP06
1290
1291 010046 013737 001374 001376 MOV DMRVEC,DMRLVL ;PTY LVL
1292 010054 060037 001376 001400 ADD R0,DMRLVL ;TX VEC
1293 010060 013737 001376 001402 MOV DMRLVL,DMTVEC ;TX LVL
1294 010066 060037 001400 001402 ADD R0,DMTVEC
1295 010072 013737 001400 001402 MOV DMTVEC,DMTLVL
1296 010100 060037 001402 001402 ADD R0,DMTLVL
1297
1298 010104 032737 000002 001236 BIT #SW01,STATSW ;IS TEST NO. SELECTED
1299 010112 001450 4$: BEQ 7$ ;BR IF NO
1300 010114
1301 010114 005737 000042 TST #42 ;RUNNING IN AUTO MODE?

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1302	010120	001045			BNE	7\$		;BR IF YES
1303	010122	104402	005574		TYPE	,MCRLF		
1304	010126	104403			INSTR			;GET TEST NO.
1305	010130	006032			MTSTN			
1306	010132	104405			PARAM			
1307	010134	000001			1			
1308	010136	001000			1000			
1309	010140	001226			TSTNO			
1310	010142	000			0			
1311	010143	001			.BYTE			
1312	010144	012700	015766		.BYTE			
1313	010150	022710			5\$: MOV	#TST1,R0		
1314	010152	012737			CMP	(PC)+,(R0)		;CMP FIRST WORD TO 12737
1315	010154	001020			MOV	(PC)+,2(PC)+		
1316	010156	023760	001226	000002	BNE	6\$		;BR IF NOT SAME
1317	010164	001014			CMP	TSTNO,2(R0)		;DOES TSTNO MATCH?
1318	010166	022760	001226	000004	BNE	6\$		;BR IF NO
1319	010174	001010			CMP	#TSTNO,4(R0)		;IS LAST WORD OK?
1320	010176	010037	001214		BNE	6\$		;BR IF NO
1321	010202	104402	005657		MOV	R0,RETURN		;IT IS A LEGAL TEST SO DO IT
1322	010206	042737	000002	001236	TYPE	,MR		
1323	010214	000412			BIC	#SW01,STATSW		
1324	010216	005720			BR	8\$		
1325	010220	020027	031442		6\$: TST	(R0)+		;POP R0
1326	010224	001351			CMP	R0,#TLAST+10		;AT END YET?
1327	010226	104402	005570		BNE	5\$		;BR IF NO
1328	010232	000730			TYPE	,MQM		;YES ILLEGAL TEST NO.
1329					BR	4\$		;TRY AGAIN
1330	010234	012737	015766	001214	7\$: MOV	#TST1,RETURN		;PREPARE RETURN ADDRESS
1331	010242	013701	001404		8\$: MOV	DMCSR,R1		;R1 = BASE DMC11 ADDRESS
1332	010246	000177	170742		JMP	2RETURN		;GO START TESTING.
1333								
1334								
1335								
1336								
1337								
1338								
1339								
1340								
1341								
1342								
1343	010252							
1344	010252	000005			AUTO.SIZE:	RESET		;INSURE A BUS INIT.
1345	010254	012702	001500		CSRMAP:	MOV	#DM.MAP,R2	;LOAD MAP POINTER.
1346	010260	005022			1\$: CLR	(R2)+		;ZERO ENTIRE MAP
1347	010262	022702	001700		CMP	#DM.END,R2		;ALL DONE?
1348	010266	001374			BNE	1\$		;BR IF NO
1349	010270	005037	001310		CLR	DMNUM		;SET OCTAL NUMBER OF DMC11'S TO C
1350	010274	012702	001500		MOV	#DM.MAP,R2		;R2 POINTS TO DMC MAP
1351	010300	005037	001306		CLR	DMACTV		;CLEAR ACTIVE
1352	010304	032737	000001	001236	BIT	#SW00,STATSW		;QUESTIONS?
1353	010312	001002			BNE	+6		;BR IF YES
1354	010314	000137	010744		JMP	7\$		;IF NO SKIP QUESTIONS
1355	010320	012737	000001	001256	MOV	#1,TEMPS		;START WITH 1
1356	010326	104403			INSTR			
1357	010330	006352			NUM			

;ROUTINE USED TO "AUTO SIZE" THE DMC11
;CSR AND VECTOR.
;NOTE: THE CSR MAY BE ANY WHERE IN THE FLOATING
ADDRESS RANGE (160000:164000)
AND THE VECTOR MAY BE ANY WHERE IN THE
FLOATING VECTOR RANGE (300:770)

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1358	010332	104405			PARAM		
1359	010334	000001			1		
1360	010336	000020			16.		
1361	010340	001252			TEMP3		
1362	010342	000			.BYTE	0	
1363	010343	001			.BYTE	1	
1364	010344	013737	001252	001310	MOV	TEMP3,DMNUM	;DMNUM = HOW MANY
1365	010352	104402	005574		TYPE	,MCRLF	
1366	010356	104410			CONVRT		;TYPE WHICH DMC IS BEING DONE
1367	010360	011450			WHICH		;TEMPS IS WHICH DMC
1368	010362	005237	001256		INC	TEMPS	
1369	010366	104403			INSTR		
1370	010370	006412			CSR		
1371	010372	104405			PARAM		
1372	010374	160000			160000		
1373	010376	164000			164000		
1374	010400	001254			TEMP4		
1375	010402	000			.BYTE	0	
1376	010403	001			.BYTE	1	
1377	010404	013722	001254		MOV	TEMP4,(R2)+	;STORE CSR IN MAP
1378	010410	104403			INSTR		
1379	010412	006430			VEC		
1380	010414	104405			PARAM		
1381	010416	000000			0		
1382	010420	000776			776		
1383	010422	001254			TEMP4		
1384	010424	000			.BYTE	0	
1385	010425	001			.BYTE	1	
1386	010426	013712	001254		MOV	TEMP4,(R2)	;STORE VECTOR IN MAP
1387	010432	104402			TYPE		
1388	010434	006451			PRI0		;ASK WHAT BR LEVEL
1389	010436	004737	011734		JSR	PC,INTTY	;GET RESPONSE
1390	010442	022703	000024		CMP	#24,R3	
1391	010446	101014			BHI	50\$	;BR IF LESS THAN 4
1392	010450	022703	000027		CMP	#27,R3	
1393	010454	103411			BLO	50\$	;BR IF GREATER THAN 7
1394	010456	012704	000011		MOV	#11,R4	;R4 = NUMBER OF SHIFTS
1395	010462	006303			ASL	R3	;SHIFT R3 LEFT
1396	010464	005304			DEC	R4	;DEC SHIFT COUNT
1397	010466	001375			BNE	.-4	;BR IF NOT DONE
1398	010470	042703	170777		BIC	#170777,R3	;BIC UNWANTED BITS
1399	010474	050312			BIS	R3,(R2)	;PUT BR LEVEL IN STATUS MAP
1400	010476	000403			BR	8\$	;CONTINUE
1401	010500	104402			TYPE		
1402	010502	005570			MQM		;RESPONSE IS OUT OF LIMITS
1403	010504	000752			BR	10\$	;TRY AGAIN
1404	010506	104402			TYPE		
1405	010510	006510			CRAM		;DOES DMC HAVE CRAM?
1406	010512	004737	011734		JSR	PC,INTTY	;GET REPLY
1407	010516	022703	000131		CMP	#131,R3	
1408	010522	001406			BEQ	9\$	;YES
1409	010524	022703	000116		CMP	#116,R3	;NO
1410	010530	001405			BEQ	16\$	;NOT A Y OR N
1411	010532	104402			TYPE		
1412	010534	005570			MQM		;TYPE "?"
1413	010536	000763			BR	8\$	;ASK AGAIN

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1414	010540	052712	100000	9\$:	BIS	#BIT15,(R2)	;SET BIT 15 IF CRAM
1415	010544	104402		16\$:	TYPE		
1416	010546	006606			MODU		;ASK WHICH LINE UNIT
1417	010550	004737	011734		JSR	PC,INTTY	;GET REPLY
1418	010554	022703	000021		CMP	#21,R3	; "1"
1419	010560	001417			BEQ	30\$	
1420	010562	022703	000022		CMP	#22,R3	; "2"
1421	010566	001412			BEQ	31\$	
1422	010570	022703	000116		CMP	#116,R3	; "N"
1423	010574	001403			BEQ	32\$	
1424	010576	104402			TYPE		
1425	010600	005570			MQM		; IF NOT A 1,2 OR N TYPE "?"
1426	010602	000760			BR	16\$	;TRY AGAIN
1427	010604	052722	010000	32\$:	BIS	#BIT12,(R2)+	;SET BIT 12 IN STAT2 IF NO LU
1428	010610	022222			CMP	(R2)+,(R2)+	;POP OVER STAT2 AND STAT3
1429	010612	000447			BR	33\$	
1430	010614	052712	020000	31\$:	BIS	#BIT13,(R2)	;SET BIT 13 IN STAT2 IF M82C2
1431	010620	104402		30\$:	TYPE		
1432	010622	007016			CONN		;ASK IF LOOP-BACK IS ON
1433	010624	004737	011734		JSR	PC,INTTY	;GET REPLY
1434	010630	022703	000131		CMP	#131,R3	;Y
1435	010634	001406			BEQ	17\$	
1436	010636	022703	000116		CMP	#116,R3	;N
1437	010642	001406			BEQ	18\$	
1438	010644	104402			TYPE		
1439	010646	005570			MQM		; IF NOT Y OR N TYPE "?"
1440	010650	000763			BR	30\$	;TRY AGAIN
1441	010652	052722	040000	17\$:	BIS	#BIT14,(R2)+	;TURNAROUND IS CONNECTED
1442	010656	000402			BR	19\$	
1443	010660	042722	040000	18\$:	BIC	#BIT14,(R2)+	;NO TURNAROUND
1444	010664			19\$:			
1445	010664	104403			INSTR		
1446	010666	006720			LINE		
1447	010670	104405			PARAM		
1448	010672	000000			0		
1449	010674	000377			377		
1450	010676	001254			TEMP4		
1451	010700	000			.BYTE	0	
1452	010701	001			.BYTE	1	
1453	010702	113722	001254		MOVB	TEMP4,(R2)+	;STORE SWITCH PAC IN MAP
1454	010706	104403			INSTR		
1455	010710	006756			BM		
1456	010712	104405			PARAM		
1457	010714	000000			0		
1458	010716	000377			377		
1459	010720	001254			TEMP4		
1460	010722	000			.BYTE	0	
1461	010723	001			.BYTE	1	
1462	010724	113722	001254		MOVB	TEMP4,(R2)+	;STORE SWITCH PAC IN MAP
1463	010730	005722			TST	(R2)+	;POP OVER STAT3
1464	010732	005337	001252	33\$:	DEC	TEMP3	;DEC DMC COUNT
1465	010736	001205			BNE	12\$	;BR IF MORE TO DO
1466	010740	000137	011350		JMP	13\$	;CONTINUE
1467	010744	012701	160000	7\$:	MOV	#160000,R1	;SET FOR FIRST ADDRESS TO BE TESTED
1468	010750	012737	011442 000004		MOV	#6\$,\$#4	;SET FOR NON-EXISTANT DEVICE TIME OUT
1469	010756	005011		2\$:	CLR	(R1)	;CLEAR SELO

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GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

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1470	010760	005711		TST	(R1)	: IF DMC11 DMC SR S/B 0
1471	010762	001162		BNE	3\$	: IF NO DEV ; TRAP TO 4. IF NO BIT 8 THEN NO DMC1
1472	010764	005061	000006	CLR	6(R1)	: CLEAR SEL6
1473	010770	005761	000006	TST	6(R1)	: IF DMC11 THEN DMRIC S/B =0!
1474	010774	001155		BNE	3\$	: BR IF NOT DMC11
1475	010776	012711	002000	MOV	#BIT10,(R1)	: SET ROMO
1476	011002	005061	000004	CLR	4(R1)	: CLEAR SEL4
1477	011006	012761	125252 000006	MOV	#125252,6(R1)	: WRITE THIS TO SEL6
1478	011014	052711	020300	BIS	#BIT13,(R1)	: WRITE IT!
1479	011020	022761	125252 000004	CMP	#125252,4(R1)	: WAS IT WRITTEN?
1480	011026	001004		BNE	21\$	: IF NO IT IS NOT CROM
1481	011030	052762	100000 000002	BIS	#BIT15,2(R2)	: SET BIT15 IF CROM
1482	011036	000421		BR	22\$	
1483	011040	012711	001000	21\$: MOV	#BIT9,(R1)	: SET ROMI
1484	011044	012761	100400 000006	MOV	#100400,6(R1)	: PUT INSTRUCTION IN SEL6
1485	011052	012711	001400	MOV	#BIT9!BIT8,(R1)	: CLOCK INSTRUCTION (MICRO PROC PC TO 0)
1486	011056	012711	002000	MOV	#BIT10,(R1)	: SET ROMO
1487	011062	022761	063220 000006	CMP	#63220,6(R1)	: IS IT CROM
1488	011070	001404		BEQ	22\$	: BR IF YES
1489	011072	022761	177777 000006	CMP	#-1,6(R1)	: IF = -1 IT HAS NO CROM
1490	011100	001113		BNE	3\$	: BR IF NOT DMC11
1491				: AT THIS POINT IT IS ASSUMED THAT R1 HOLDS A DMC11 CSR ADDRESS.		
1492	011102	010122		22\$: MOV	R1,(R2)+	: STORE CSR IN CORE TABLE.
1493	011104	012711	001000	15\$: MOV	#BIT9,(R1)	: CLEAR LINE UNIT LOOP
1494	011110	005061	000004	CLR	4(R1)	: CLEAR PORT4
1495	011114	012761	122113 000006	MOV	#122113,6(R1)	: LOAD INSTRUCTION (CLR DTR)
1496	011122	052711	000400	BIS	#BIT8,(R1)	: CLOCK INSTRUCTION
1497	011126	012761	021264 000006	MOV	#021264,6(R1)	: LOAD INSTRUCTION
1498	011134	052711	000400	BIS	#BIT8,(R1)	: CLOCK INSTRUCTION
1499	011140	122761	000377 000004	CMPB	#377,4(R1)	: IS IT ALL ONES?
1500	011146	001003		BNE	+.10	: BR IF NO
1501	011150	052712	010000	BIS	#BIT12,(R2)	: IF YES, NO LINE UNIT, SET STATUS BIT
1502	011154	000436		BR	20\$	
1503	011156	032761	000002 000004	BIT	#BIT1,4(R1)	: IS SWITCH A ONE?
1504	011164	001403		BEQ	+.10	: BR IF M8201
1505	011166	052712	060000	BIS	#BIT13!BIT14,(R2)	: M8202 ASSUME CONNECTOR
1506	011172	000427		BR	20\$	: CONNECTOR ON)
1507	011174	032761	000010 000004	BIT	#BIT3,4(R1)	: IS MRDY SET
1508	011202	001023		BNE	20\$	: BR IF M8201 NO CONNECTOR (ON LINE)
1509	011204	012761	000100 000004	MOV	#BIT6,4(R1)	: LOAD PORT4
1510	011212	012761	122113 000006	MOV	#122113,6(R1)	: LOAD INSTRUCTION
1511	011220	052711	000400	BIS	#BIT8,(R1)	: CLOCK INSTRUCTION (SET DTR)
1512	011224	012761	021264 000006	MOV	#021264,6(R1)	: LOAD INSTRUCTION
1513	011232	052711	000400	BIS	#BIT8,(R1)	: CLOCK INSTRUCTION (READ MODEM REG)
1514	011236	032761	000010 000004	BIT	#BIT3,4(R1)	: IS MRDY SET NOW?
1515	011244	001402		BEQ	20\$	: BR IF NO CONNECTOR
1516	011246	052712	040000	BIS	#BIT14,(R2)	: SET STATUS BIT FOR CONNECTOR
1517	011252	005722		20\$: TST	(R2)+	: POP POINTER
1518	011254	012761	021324 000006	MOV	#021324,6(R1)	: PUT INSTRUCTION IN PORT6
1519	011262	012711	001400	MOV	#BIT9!BIT8,(R1)	: PORT4+LU 15
1520	011266	156122	000004	BISB	4(R1),(R2)+	: STORE DDCMP LINE # IN TABLE
1521	011272	012761	021344 000006	MOV	#021344,6(R1)	: PORT6+INSTRUCTION
1522	011300	012711	001400	MOV	#BIT8!BIT9,(R1)	: CLOCK INSTR.
1523	011304	156122	000004	BISB	4(R1),(R2)+	: STORE BM873 ADD IN TABLE
1524	011310	005722		TST	(R2)+	: POP OVER STAT3
1525	011312	005011		CLP	(R1)	: CLEAR ROMI

1526	011314	005237	001310		INC	DMNUM	;UPDATE DEVICE COUNTER
1527	011320	022737	000020	001310	CMP	#20,DMNUM	;ARE MAX. NO. OF DEV FOUND?
1528	011326	001410			BEQ	13\$	;YES DON'T LOOK FOR ANY MORE.
1529	011330	005011			3\$: CLR	(R1)	;CLEAR BIT 10
1530	011332	005061	000006		CLR	6(R1)	;CLEAR SEL 6
1531	011336	062701	000010		14\$: ADD	#10,R1	;UPDATE CSR POINTER ADDRESS
1532	011342	022701	164000		CMP	#164000,R1	
1533	011346	001203			BNE	2\$	;BR IF MORE ADDRESS TO CHECK.
1534	011350	005037	001306		13\$: CLR	DMACTV	
1535	011354	005737	001310		TST	DMNUM	;WERE ANY DMC11'S FOUND AT ALL?
1536	011360	001423			BEQ	5\$	;ERROR AUTO SIZER FOUND NO DMC11'S IN THIS SYS.
1537	011362	013701	001310		MOV	DMNUM,R1	
1538	011366	010137	001314		MOV	R1,SAVNUM	;SAVE NUMBER OF DEVICES
1539	011372	000241			4\$: CLC		
1540	011374	006137	001306		ROL	DMACTV	;GENERATE ACTIVE REGISTER OF DEVICES.
1541	011400	005237	001306		INC	DMACTV	;SET THE BIT
1542	011404	005301			DEC	R1	
1543	011406	001371			BNE	4\$	;BR IF MORE TO GENERATE
1544	011410	012737	000006	000004	MOV	#6,2#4	;RESTORE TRAP VECTOR
1545	011416	013737	001306	001312	MOV	DMACTV,SAVACT	;SAVE ACTIVE REGISTER
1546	011424	000137	011456		JMP	VECMAP	;GO FIND THE VECTOR NOW.
1547	011430	104402	005662		5\$: TYPE	MERR2	;NOTIFY OPR THAT NO DMC11'S FOUND.
1548	011434	005000			CLR	RO	;MAKE DATA LIGHTS ZERO
1549	011436	000000			HALT		;STOP THE SHOW
1550	011440	000776			BR	.-2	;DISABLE CONT. SW.
1551	011442	012716	011336		6\$: MOV	#14\$, (SP)	;ENTERED BY NON-EXISTANT TIME-OUT.
1552	011446	000002			RTI		;RETURN TO MAINSTREAM
1553							
1554	011450	000001			WHICH: 1		
1555	011452	002	002		.BYTE	2,2	
1556	011454	001256			TEMPS		
1557							
1558	011456	032737	000001	001236	VECMAP: BIT	#SW00,STRTSW	
1559	011464	001114			BNE	5\$	
1560	011466	012737	000340	000022	MOV	#340,2#22	;SET IOT TRAP PRIO TO 7
1561	011474	012737	011650	000020	MOV	#4\$,2#20	;SET IOT TRAP VECTOR
1562	011502	012702	001500		MOV	#DM.MAP,R2	;SET SOFTWARE POINTER
1563	011506	012700	000300		MOV	#300,RO	;FLOATING VECTORS START HERE.
1564	011512	012701	000302		MOV	#302,R1	;PC OF IOT INSTR.
1565	011516	010120			1\$: MOV	R1,(RO)+	;START FILLING VECTOR AREA
1566	011520	012721	000004		MOV	#4,(R1)+	;WITH .+2; IOT
1567	011524	022021			CMP	(RO)+(R1)+	;ADD 2 TO RO +R1
1568	011526	020127	001000		CMP	R1,#1000	
1569	011532	101771			BLOS	1\$	;BR IF MORE TO FILL
1570	011534	013737	001306	001246	MOV	DMACTV,TEMP1	;STORE TEMPORALLY
1571	011542	006037	001246		2\$: ROR	TEMP1	;BRING OUT A BIT
1572	011546	103063			BCC	5\$	;BR IF ALL DONE
1573	011550	012704	000012		MOV	#12,R4	;R4 IS INDEX REGISTER
1574	011554	016437	011720	177776	MOV	BRLVL(R4),PS	;SET PS TO 7
1575	011562	011201			MOV	(R2),R1	
1576	011564	012761	000200	000004	MOV	#200,4(R1)	
1577	011572	012711	001000		MOV	#BIT9,(R1)	;SET ROMI
1578	011576	012761	121111	000006	MOV	#121111,6(R1)	;PUT INSTRUCTION IN PORT6
1579	011604	012711	001400		MOV	#BIT9:BIT8,(R1)	;FORCE AN INTERRUPT
1580	011610	105200			7\$: INCB	RO	;STALL
1581	011612	001376			BNE	.-2	;FOR TIME TO INTERRUPT

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1582	011614	162704	000002		SUB	#2,R4	;GET NEXT LOWEST PS LEVEL
1583	011620	001404			BEQ	6\$	;BR IF R4 = 0
1584	011622	016437	011720	177776	MOV	BRLVL(R4),PS	;MOVE NEXT LOWER LEVEL IN PS
1585	011630	000767			BR	7\$	;BR TO DELAY
1586	011632	052762	005300	000002	6\$: BIS	#5300,2(R2)	;NO INTERRUPT ASSUME 300 AT LEVEL 5 AND FIX DMC11
1587	011640	005011			3\$: CLR	(R1)	;CLEAR ROMI
1588	011642	062702	000010		ADD	#10,R2	;POP SOFTWARE POINTER
1589	011646	000735			BR	2\$	;KEEP GOING
1590	011650	051662	000002		4\$: BIS	(SP),2(R2)	;GET VECTOR ADDRESS
1591	011654	042762	000007	000002	BIC	#7,2(R2)	;CLEAR JUNK
1592	011662	016405	011722		MOV	BRLVL+2(R4),R5	;GET BR LEVEL OF DMC11
1593	011666	006305			ASL	R5	;SHIFT LEVEL 4 PLACES
1594	011670	006305			ASL	R5	;TO THE LEFT FOR THE
1595	011672	006305			ASL	R5	;STATUS TABLE
1596	011674	006305			ASL	R5	
1597	011676	042705	170777		BIC	#170777,R5	;CLEAR UNWANTED BITS
1598	011702	050562	000002		BIS	R5,2(R2)	;PUT BR LEVEL IN STATUS TABLE
1599	011706	022626			CMP	(SP)+,(SP)+	;POP IOT JUNK OFF STACK
1600	011710	012716	011640		MOV	#3\$, (SP)	;SET FOR RETURN
1601	011714	000002			RTI		
1602	011716	000207			5\$: RTS	PC	;ALL DONE WITH "AUTO SIZING"
1603							
1604	011720	000000			BRLVL:	0	;LEVEL 0
1605	011722	000000				0	;LEVEL 0
1606	011724	000200				200	;LEVEL 4
1607	011726	000240				240	;LEVEL 5
1608	011730	000300				300	;LEVEL 6
1609	011732	000340				340	;LEVEL 7
1610							
1611							
1612	011734	105777	167244		INTTY: TSTB	@TKCSR	;WAIT FOR DONE
1613	011740	100375			BPL	-4	
1614	011742	017703	167240		MOV	@TKDBR,R3	;PUT CHAR IN R3
1615	011746	105777	167236		TSTB	@TPCSR	;WAIT UNTIL PRINTER IS READY
1616	011752	100375			BPL	-4	
1617	011754	010377	167232		MOV	R3,@TPDBR	;ECHO CHAR
1618	011760	042703	000240		BIC	#BIT7!BIT5,R3	;MASK OFF LOWER CASE
1619	011764	000207			RTS	PC	;RETURN
1620							
1621							
1622	011766						

15300
 15400 ROMMAP:

2	MACRO DEFINITIONS
4	REVISION 00
5	FEBRUARY 25, 1975
6	
7	REVISION 01
8	MARCH 18, 1975
9	NEW CSR BOARD CHANGES
10	
11	HARVEY M. SCHLESINGER
13	COPYRIGHT 1975 DIGITAL EQUIPMENT CORPORATION
65	MICRO INSTRUCTION DEFINITIONS
66	BRANCH INSTRUCTIONS
117	INDEXED BRANCH INSTRUCTIONS
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377	DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT
394	VERSION 00A FEBRUARY 26, 1975
385	
386	HARVEY M. SCHLESINGER
387	
388	COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION
389	
390	VERSION 00B MARCH 17, 1975
391	CSR AND MICROPROCESSOR CHANGES
392	
393	VERSION 00C NOVEMBER 6, 1975
394	RETRANSMISSION CHANGES
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396	VERSION 00D DECEMBER 3, 1975
397	TRANSMIT DONE CHANGES
398	
399	THE LATEST MODIFICATIONS WERE ADDED ON:
400	NOVEMBER 16, 1976
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467	SCRATCH PAD ASSIGNMENTS
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559	IDLE--PROGRAM IDLE LOOP
590	BASSRV----BASE SERVICE ROUTINE
627	NIDLE2---NO CSR ACTIVITY STATE
668	INWAIT---WAIT FOR RQI TO CLEAR
718	OUTINT---SET UP OUTPUT INTERRUPT [RDY0]
766	OUTWAI---WAIT FOR RDY0 TO GO AWAY
778	CTLSRV--CNTL I SERVICE
798	TBASRV--TRANSMITTER BUFFER ADDRESS SERVICE
818	RBASRV--RECEIVE BUFFER ADDRESS SERVICE
884	RCVA--ROUTINE TO HANDLE FIRST DDCMP CHARACTER
921	RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD
958	RCVC--ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINAL
979	RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES
1000	RCVE--ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE
1013	RCVF--ROUTINE TO IGNORE ADDRESS
1021	RCVG--ROUTINE TO IGNORE CRC1
1026	RCVH--ROUTINE TO HANDLE CRC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYPES
1091	RCVK01--ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
1103	RCVK0--PROCESS ODD CHARACTER

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
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1171		RCVI--STORE UNNUMBERED MESSAGE TYPE
1177		RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD, SELECT AND FINAL
1191		RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
1201		RCVQ--UNNUMBERED MESSAGE--NUMBER FIELD
1207		RCVL--PROCESS CRC3
1229		RCVM--PROCESS CRC4--END OF DATA MESSAGE
1251		EM2--PROCESS RLD MESSAGE
1271	NXMERR	---NON EXISTANT MEMORY HANDLER
1320		TMTDA--TRANSMITTER DISPATCH ROUTINE
1326		TMTA--FIRST CHARACTER OF HEADER
1397		TMTB--OUTPUT FIRST CHAR OF COUNT
1428		TMTC--OUTPUT SECOND CHAR OF COUNT
1452		TMTD--RESPONSE FIELD-NUMBERED MESSAGE
1462		TMTE--NUMBER FIELD--NUMBERED MESSAGE
1471		TMTF--NUMBERED MSG ADDRESS FIELD
1484		TF1-NUMBERED MSG HEADER EOM
1494		TMTH--ROUTINE TO OUTPUT DATA CHARACTERS
1551		TMTI--SEND UNNUMBERED TYPE FIELD
1557		TMTJ--SEND SUB-TYPE FIELD
1562		TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
1570		TMTL--UNNUMB MSG NUMBER FIELD
1589		TMTM--UNNUMB MSG--STATION ADDRESS
1604		TIMSRV--TIMEOUT ROUTINE--SENDS REP
1670		SNDACK--ROUTINE TO SEND AN ACK
1737		REP HANDLER
1746		START HANDLER
1759		STACK HANDLER

F05

DMC-11 MICROPROCESSOR INSTRUCTIONS
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G05

16 000000
17
18 000000
19 100000
20 020000
21 000000
22 040000
23 060000
24 060000
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26 060000
27 010000
28 014000
29 000400
30 001000
31 001400
32 002000
33 002400
34 003000
35 003400
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37 000200
38 000220
39 000240
40 000260
41 000300
42 000320
43 000340
44 000360
45 000000
46 000020
47 000040
48 000060
49 000100
50 000120
51 000140
52 000160
53
54 004000
55 010000
56 014000
57 001000
58 001400
59 000400
60 002000
61 002400
62 003000
63 003400

NEW=0
;MICROPROCESSOR INSTRUCTION WORD DEFINITIONS
MOVE=0 ;OPCODE MOVE
JUMP=100000 ;OPCODE JUMP
IBUS=20000 ;SOURCE IBUS
IMM=0 ;SOURCE IMMEDIATE
MEMX=40000 ;SOURCE MEMORY
BRX=60000 ;SOURCE BR
BR=60000 ;SOURCE BR

DP=60000 ;SOURCE BR
LDMAR=10000 ;MA-LOAD MAR LO
INCMAR=14000 ;MA-INCREMENT MAR
WRTEBR=400 ;DEST-WRITE BR
WROUTX=1000 ;DEST-EXTENDED IBUS
SHFTBR=1400 ;DEST-SHIFT BR LEFT
WROUT=2000 ;DEST-WRITE OUTPUT
WRMEM=2400 ;DEST-WRITE MEMORY
SPX=3000 ;DEST-WRITE SP
SPBRX=3400 ;DEST-WRITE SP AND BR

;FUNCTIONS
SELA=200 ;FUNCTION-SELECT A
SELB=220 ;FUNCTION-SELECT B
AORNB=240 ;FUNCTION-A OR NOT B
AANDB=260 ;FUNCTION A AND B
AORB=300 ;FUNCTION-A OR B
AXORB=320 ;FUNCTION A XOR B
SUB=340 ;SUBTRACT
SUBTC=360 ;FUNCTION- TWOS COMPLEMENT SUBTRACT
ADD=0 ;ADD A+B
ADDC=20 ;A+B+CARRY
SUBC=40 ;A-B-C
INCA=60 ;INCREMENT A
AC=100 ;A PLUS CARRY
AA=120 ;A PLUS A
AAC=140 ;A PLUS A PLUS C
DECA=160 ;DECREMENT A

;END FUNCTIONS
PAGE1=4000
PAGE2=10000
PAGE3=14000

CCOND=1000 ;CONDITION C
ZCOND=1400 ;CONDITION Z
ALCOND=400 ;ALWAYS
BROCON=2000 ;CONDITION BRO
BR1CON=2400 ;CONDITION BR1
BR4CON=3000 ;CONDITION BR4
BR7CON=3400 ;CONDITION BR7

H05

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100000

```
.SBTTL MICRO INSTRUCTION DEFINITIONS
.SBTTL BRANCH INSTRUCTIONS

: JUMP=100000 ;JUMP OP CODE
:
: .MACRO $ZERO
: MICPC=MICPC+1
: 000000
:
: .ENDM $ZERO
:
: .MACRO ALWAYS ADDRES ;JUMP ALWAYS
: MICPC=MICPC+1
: <JUMP!ALCOND!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO BRO ADDRES ;JUMP IF BRO SET
: MICPC=MICPC+1
: <JUMP!BROCON!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO BR1 ADDRES ;JUMP IF BR1 SET
: MICPC=MICPC+1
: <JUMP!BR1CON!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO BR4 ADDRES ;JUMP IF BR4 SET
: MICPC=MICPC+1
: <JUMP!BR4CON!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO BR7 ADDRES ;JUMP IF BR7 SET
: MICPC=MICPC+1
: <JUMP!BR7CON!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO Z ADDRES ;JUMP IF Z BIT SET
: MICPC=MICPC+1
: <JUMP!ZCOND!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
:
: .MACRO C ADDRES ;JUMP IF C BIT SET
: MICPC=MICPC+1
: <JUMP!CCOND!<ADDRES-INIT&3000*4>!<ADDRES-INIT&777/2>>
:
: .ENDM
: .SBTTL INDEXED BRANCH INSTRUCTIONS
:
: .MACRO .ALWAY SRC, FUNC, SPLOC ;INDEXED JUMP ALWAYS
: MICPC=MICPC+1
```

DMC-11 MICROPROCESSOR INSTRUCTIONS
DMCHGH.MAC 06-DEC-76 10:31

MACY11 27(1006) 14-DEC-76 16:44 PAGE 2-1
INDEXED BRANCH INSTRUCTIONS

PAGE: 0060

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<JUMP!ALCOND!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .BR0 SRC,FUNC,SPLOC ;INDEXED JUMP ON BR0 SET
MICPC=MICPC+1
<JUMP!BR0CON!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .BR1 SRC,FUNC,SPLOC ;INDEXED JUMP ON BR1 SET
MICPC=MICPC+1
<JUMP!BR1CON!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .BR4 SRC,FUNC,SPLOC ;INDEXED JUMP ON BR4 SET
MICPC=MICPC+1
<JUMP!BR4CON!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .BR7 SRC,FUNC,SPLOC ;INDEXED JUMP ON BR7 SET
MICPC=MICPC+1
<JUMP!BR7CON!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .Z SRC,FUNC,SPLOC ;INDEXED JUMP ON Z BIT SET
MICPC=MICPC+1
<JUMP!ZCOND!SRC!FUNC!SPLOC>
.ENDM
;
.MACRO .C SRC,FUNC,SPLOC ;INDEXED JUMP ON C BIT SET
MICPC=MICPC+1
<JUMP!CCOND!SRC!FUNC!SPLOC>
.ENDM
.SBTTL          MOVE INSTRUCTIONS
;
MOVE=0          ;MOVE OPCODE
;
.MACRO BRSHFT  ;BR SHIFT RIGHT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTBR!SELB>
.ENDM
;
.MACRO BSHFTB  ;BR ROTATE
MICPC=MICPC+1
<MOVE!SHFTBR!SELB!BR>
.ENDM
;
.MACRO SP SRC,FUNC,SPLOC ;LOAD SCRATCH-PAD

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232

```

MICPC=MICPC+1
<MOVE!SPX!SRC!FUNC!SPLOC>

.ENDM
;
.MACRO SPBR SRC,FUNC,SPLOC ;LOAD SP AND BR
MICPC=MICPC+1
<MOVE!SPBRX!SRC!FUNC!SPLOC>

.ENDM
;
.MACRO MEM SRC,DATA ;MOVE TO MEMORY
MICPC=MICPC+1
<MOVE!WRMEM!SRC!<DATA>>

.ENDM
;
.MACRO MEMADR ADDRES,FUNC ;WRITE ADDRESS TO MEMORY
MICPC=MICPC+1
.IF B FUNC
<MOVE!WRMEM!<ADDRES-INIT&777/2>>
.IFF
<MOVE!WRMEM!FUNC!<ADDRES-INIT&777/2>>
.ENDC
.ENDM
;
.MACRO MEMINC SRC,DATA ;MOVE TO MEM. INCR MAR
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!SRC!<DATA>>

.ENDM
;
.MACRO BRWRTE SRC,DATA ;MOVE TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!SRC!<DATA>>

.ENDM
;
.MACRO BRADDR ADDRES ;PUT RETURN ADDR (1 BYTE) IN BR
MICPC=MICPC+1
<MOVE!WRTEBR!<ADDRES-INIT&777/2>>

.ENDM
;
.MACRO OUTPUT SRC,DATA ;WRITE OUTPUT
MICPC=MICPC+1
<MOVE!WROUT!SRC!<DATA>>

.ENDM
;
.MACRO OUT SRC,DATA
MICPC=MICPC+1
<MOVE!WROUTX!SRC!<DATA>>

.ENDM
;

```

K05

DMC-11 MICROPROCESSOR INSTRUCTIONS
DMCHGH.MAC 06-DEC-76 10:31MACY11 27(1006) 14-DEC-76 16:44 PAGE 2-3
MOVE INSTRUCTIONS

PAGE: 0062

```

233      .MACRO LDMA SRC,DATA      ;LOAD MEMORY ADDRESS REG
234      MICPC=MICPC+1
235      .IF IDN SRC,IMM
236      <MOVE!LDMA!IMM!<DATA&377>>
237      .IFF
238      <MOVE!LDMA!SRC!<DATA>>
239      .ENDC
240
241      .ENDM
242
243      ;
244      .MACRO LDMAP SRC,DATA      ;LOAD MEMORY PAGE NUMBER
245      MICPC=MICPC+1
246      .IF IDN SRC,IMM
247      <MOVE!LDMAP!IMM!<DATA/400>>
248      .IFF
249      <MOVE!LDMAP!SRC!<DATA>>
250      .ENDC
251
252      .ENDM
253
254      ;
255      .MACRO LDADDR DATA      ;LOAD A LINE TABLE ADDRESS
256      BRWTE IMM,DATA
257      LDMA BR,<ADD!SP.RMD>
258      .ENDM
259
260      ;
261      .MACRO CMP SRC,SPADDR      ;COMPARE SOURCE AND SP
262      MICPC=MICPC+1
263      <SUBTC!SRC!SPADDR>
264
265      .ENDM
266
267      ;
268      .MACRO NOP SRC,FUNC,SPADDR ;NOP-SOURCE, FUNC, NO DEST
269      MICPC=MICPC+1
270      <SRC!FUNC!SPADDR>
271
272      .ENDM
273
274      .MACRO CALL REG,ADDRES      ;SUBROUTINE CALL
275      DISP=<MICPC+1>&377
276      BRWTE IMM,DISP+3
277      SP BR,SELB,REG
278      ALWAYS ADDRES
279      .ENDM
280
281      .MACRO RETURN REG,PAGE      ;SUBROUTINE RETURN
282      .ALWAY BR,SELA,<REG!PAGE>
283      .ENDM

```

282		.SBTTL INPUT/OUTPUT ASSIGNMENTS	
283		;IBUS ASSIGNMENTS	
284	100000	INCON=0+100000	;IN CONTROL CSR
285	100020	MAIN=20+100000	;MAINTENANCE REGISTER
286	100040	OCON=40+100000	;OUT CONTROL CSR
287	100060	UBADDR=60+100000	;UNUSED
288	100100	PORT1=100+100000	;CSR4
289	100120	PORT2=120+100000	;CSR5
290	100140	PORT3=140+100000	;CSR6
291	100160	PORT4=160+100000	;CSR7
292	100200	NPR=200+100000	;NPR CONTROL
293	100220	UBBR=220+100000	;BR (INTERRUPT) CONTROL
294	000000	INDAT1=0	;INPUT DATA LOW BYTE
295	000020	INDAT2=20	;INPUT DATA HIGH BYTE
296	000140	IOBA1=140	;OUTPUT BA LOW BYTE
297	000160	IOBA2=160	;OUTPUT BA HIGH BYTE
298	000100	IIBA1=100	;INPUT BA LOW BYTE
299	000120	IIBA2=120	;INPUT BA HIGH BYTE
300	000200	RCV DAT=200	;RECEIVE DATA
301	000220	TMTCON=220	;TMTR CONTROL
302	000240	RCVCON=240	;RCVR CONTROL
303	000260	MODEM=260	;MODEM CONTROL
304	000300	SYNREG=300	;SYN REGISTER
305	000320	LNOSW=320	;LINE NUMBER SWITCH
306	000340	BM873=340	;BM873 ADDRESS
307	000360	LUMAIN=360	;LINE UNIT MAINTENANCE
308		;OBUS ASSIGNMENTS	
309		;EXTENDED OBUS	
310	000000	OINCON=0	;IN CONTROL CSR
311	000001	OMAIN=1	;MAINT
312	000002	OCON=2	;OUT CONTROL CSR
313	000003	OUBADD=3	;UNUSED
314	000004	OPORT1=4	;CSR4
315	000005	OPORT2=5	;CSR5
316	000006	OPORT3=6	;CSR6
317	000007	OPORT4=7	;CSR7
318	000010	ONPR=10	;NPR CONTROL
319	000011	OBRR=11	;BR CONTROL
320		;UNEXTENDED OBUS	
321	000002	OUTDA1=2	;OUTPUT DATA LOW BYTE
322	000003	OUTDA2=3	;OUTPUT DATA HIGH BYTE
323	000006	OBA1=6	;OUTPUT BA LOW BYTE
324	000007	OBA2=7	;OUTPUT BA HIGH BYTE
325	000004	IBA1=4	;INPUT BA LOW BYTE
326	000005	IBA2=5	;INPUT BA HIGH BYTE
327	000010	TMTDAT=10	;TMTR DATA
328	000011	OTMTCO=11	;TMTR CONTROL
329	000012	ORCVCO=12	;RCVR CONTROL
330	000013	OMODEM=13	;MODEM CONTROL
331	000014	SYNC=14	;SYN REGISTER
332	000017	OLUMAN=17	;LINE UNIT MAINT.

M05

DMC-11 MICROPROCESSOR INSTRUCTIONS
DMCHGH.MAC 06-DEC-76 10:31

MACY11 27(1006) 14-DEC-76 16:44 PAGE 3-1
PROTOCOL DEPENDANT MACROS

PAGE: 0064

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334 .SBTTL PROTOCOL DEPENDANT MACROS
335 .MACRO RSTATE STATE ;UPDATE RECEIVE STATE POINTER
336 MICPC=MICPC+1
337 <MOVE!WRTEBR!IMM!<STATE-INIT&777/2>>
338 MICPC=MICPC+1
339 <MOVE!SPX!BR!SELB!SP3>
340 .ENDM
341 ;
342 .MACRO TSTATE STATE
343 MICPC=MICPC+1
344 <MOVE!WRTEBR!IMM!<STATE-INIT&777/2>>
345 MICPC=MICPC+1
346 <MOVE!SPX!BR!SELB!SP2>
347 .ENDM
348 ;
349 .MACRO STATE ADDR
350 MICPC=MICPC+1
351 <MOVE!WRTEBR!IMM!<ADDR-INIT&777/2>>
352 .ENDM
353 ;
354 .MACRO PSTATE STATE
355 MEM IMM,<<STATE-INIT&777/2>>
356 .ENDM
357 ;
358 .MACRO PSTATI STATE
359 MEMINC IMM,<<STATE-INIT&777/2>>
360 .ENDM
361 ;
362 .MACRO SYNMAC
363 SP BR,SELB,SP2 ;UPDATE STATE POINTER FROM BR
364 SYNOUT
365 ALWAYS IDLE
366 .ENDM
367 ;
368 .MACRO SYNOUT
369 LDMA IMM,UNMSG ;LOAD PTR TO UNNUMB MESSAGE SKELETON
370 OUTPUT <MEMX!INCMAR>,<SELB!OTMTCO> ;SOM TO TMTR CONTROL
371 OUTPUT <MEMX!INCMAR>,<SELB!TMDAT> ;SYNC TO TMTR SILO
372 .ENDM
373
374 177777 MICPC=177777 ;INIT MICRO PC
375

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N05

DMC-11 MICROPROCESSOR INSTRUCTIONS
HILOW.MAC 03-DEC-76 10:16

MACY11 27(1006) 14-DEC-76 16:44 PAGE 5
DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT

PAGE: 0065

377
378 000000

.SBTTL DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT
LOW=0

B06

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6
DMC11 DDCMP MICRO CODE ASSEMBLED FOR USE WITH THE M8201 LINE UNIT

PAGE: 0066

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.TITLE DMC11 DDCMP PROTOCOL IMPLEMENTATION
.SBTTL VERSION 00A FEBRUARY 26, 1975
.SBTTL
.SBTTL HARVEY M. SCHLESINGER
.SBTTL
.SBTTL COPYRIGHT 1975, DIGITAL EQUIPMENT CORPORATION
.SBTTL
.SBTTL VERSION 00B MARCH 17, 1975
.SBTTL CSR AND MICROPROCESSOR CHANGES
.SBTTL
.SBTTL VERSION 00C NOVEMBER 6, 1975
.SBTTL RETRANSMISSION CHANGES
.SBTTL
.SBTTL VERSION 00D DECEMBER 3, 1975
.SBTTL TRANSMIT DONE CHANGES
.SBTTL
.SBTTL THE LATEST MODIFICATIONS WERE ADDED ON:
.SBTTL NOVEMBER 16, 1976

C06

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402 .SBTTL MICROPROCESSOR MAIN MEMORY ASSIGNMENTS
403 ;ALLOCATION OF MICROPROCESSOR MAIN MEMORY
404 NAKSR=0 ;NAKS RECD--DYNAMIC
405 NAKST=NAKSR+1 ;NAKS TMTD--DYNAMIC
406 REPSR=NAKST+1 ;REPS RECD--DYNAMIC
407 REPST=REPSR+1 ;REPS TMTD--DYNAMIC
408 NP=REPST+3 ;CONSTANT 0
409 NTLR=NP+1 ;NAKS-MSG NO BUFFERS CUMUL.
410 NHDR=NTLR+1 ;NAKS-MSG HEADER BAD
411 NDATA=NHDR+1 ;NAKS-DATA BAD
412 NTLS=NDATA+1 ;NAK SENT --NO BUFFERS
413 NHDS=NTLS+1 ;NAK SENT BAD HEADER
414 NDATS=NHDS+1 ;NAK SENT BAD DATA
415 REPCS=NDATS+1 ;REPS SENT CUMUL
416 REPCR=REPCS+1 ;REPS RECD CUMUL
417 BASE=REPCR+1 ;CORE TABLE BASE ADDRESS
418 SRC=BASE+3 ;START OF INPUT CHAIN--NEXT RECV DONE
419 ERC=SRC+1 ;END OF INPUT CHAIN
420 RCL1=ERC+1 ;RECEIVE LINK #1
421 RCL2=RCL1+5 ;" " #2
422 RCL3=RCL2+5 ;" " #3
423 RCL4=RCL3+5
424 RCL5=RCL4+5
425 RCL6=RCL5+5
426 RCL7=RCL6+5
427 STC=RCL7+5 ;START OF OUTPUT CHAIN---NEXT TMT DONE
428 ETC=STC+1 ;END OF TRANSMIT CHAIN
429 TML1=ETC+1 ;TRANSMIT LINK #1
430 TML2=TML1+6 ;" " #2
431 TML3=TML2+6 ;" " #3
432 TML4=TML3+6
433 TML5=TML4+6
434 TML6=TML5+6
435 TML7=TML6+6
436 TML8=TML7+6
437 T=TML8+6 ;TYPE FIELD
438 ST=T+1 ;SUBTYPE FIELD
439 ISP17=ST+1 ;MSG ACKED IMAGE
440 IMG10=ISP17+1 ;IMAGE OF BIT 1 OF SP10
441 IMG11=IMG10+1 ;IMAGE OF SP11
442 IMG12=IMG11+1 ;IMAGE OF SP12
443 IMG14=IMG12+1 ;IMAGE OF SP14
444 IMG16=IMG14+1 ;IMAGE OF SP16
445 IMG17=IMG16+1 ;IMAGE OF SP17
446 TYPTAB=IMG17+1 ;TYPE TABLE---
447 ;72 TYPE TABLE REP
448 ;73 " " NAK
449 TYPSTT=TYPTAB+2 ;74 " " START
450 ;75 " " STACK
451
452
453 BC=TYPSTT+3 ;RECEIVE BYTE COUNT
454 ISP11=BC+2 ;SP11 IMAGE
455 ISP12=ISP11+1 ;SP12 IMAGE
456 INCONS=ISP12+1 ;IN CONTROL CSR IMAGE
457 RTHRS=INCONS+1 ;RECV THRESHOLD LINK

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006

SMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-2
MICROPROCESSOR MAIN MEMORY ASSIGNMENTS

PAGE: 0068

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000211
000240
000241
000242
000400

:ALL LOCATIONS FROM 200 ON ARE NOT WRITTEN OUT DURING A TABLE UPDATE

TABST=210 ;TABLE UPDATE STATE
PRTST=TABST+1 ;PORT STATE
NXTINT=240 ;NEXT INTERRUPT POSITION
NXTSP=NXTINT+1 ;END OF INTERRUPT CHAIN
INTSTK=NXTSP+1 ;STACK OF INTERRUPTS
MMEND=400 ;MAIN MEMORY END

E06

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DCCHGH.MAC 06-DEC-76 11:34MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-3
SCRATCH PAD ASSIGNMENTS

PAGE: 0069

467		.SBTTL	SCRATCH PAD ASSIGNMENTS
468	000000	SP0=0	;SP0---SCRATCH REGISTER
469	000001	SP1=1	;SP1---PORT STATUS WORD
470			;BIT ASSIGNMENTS
471			;BIT0---INIT MODE
472			;BIT1---SEC STATION SELECT(UNUSED)
473			;BIT2---NO BUFFER ASSIGNED IN BOOT MODE
474			;BIT3---DLE RECEIVED WHILE NOT IN MAINT MODE
475			;BIT4---INTERRUPT PENDING
476			;BIT6---DISCONNECT ERROR
477			;BIT7---BOOT MODE
478	000002	SP2=2	;SP2---TRANSMIT STATE POINTER
479	000003	SP3=3	;SP3---RECEIVE STATE POINTER
480	000004	SP4=4	;SP4---END RECV ADDRESS
481	000005	SP5=5	;SP5---END RECEIVE ADDRESS
482	000006	SP6=6	;SP6---END TRANSMIT ADDRESS
483	000007	SP7=7	;SP7---END TRANSMIT ADDRESS
484	000010	SP10=10	;SP10---LINE STATUS WORD
485			;BIT ASSIGNMENTS
486			;BIT0---UNNUMB PENDING
487			;BIT1---MESSAGE IN PROGRESS
488			;BIT2---LINE HAS GONE IDLE
489			;BIT3---START RECEIVED
490			;BIT4---CLEAR ACTIVE ON END
491			;BIT5---START MODE
492			;BIT6---HALF DUPLEX
493			;BIT7---OK TO SEND
494	000011	SP11=11	;SP11---R FIELD
495	000012	SP12=12	;SP12---N FIELD
496	000013	SP13=13	;SP13---TYPE
497	000014	SP14=14	;SP14---RECEIVE LINK IMAGE
498	000015	SP15=15	;SP15---TIMER ENTRY---NUMBER OF ONE SECOND TICKS
499	000016	SP16=16	;SP16---POINTER TO TMT LINK COPY IN MAIN MEM
500	000017	SP17=17	;SP17---LAST MESSAGE ACKNOWLEDGED

502			.SBTTL INIT--INITIALIZATION ROUTINE	
503			:ZEROS MAIN MEMORY	
504			:LOOPS WAITING FOR RECEIVE DATA(BOOT?)	
505			:OR FOR RQI TO BE SET	
506			:WILL ACCEPT ONLY BASE FORMAT. ALL OTHERS WILL RETURN A PROCEDURE ERROR	
507			:	
508			:AT INITIALIZATION --- THE HARDWARE CLEARS THE BR AND MAR	
509		011766	=11766	
510	011766		INIT: SP BR,SELB,SP0	;CLEAR SP0
(1)		000000	MICPC=MICPC+1	
(1)	011766	063220	<MOVE!SPX!BR!SELB!SP0>	
(1)				
511	011770		SP BR,SELB,SP3	;PAGE ONE TRANSFER ADDRESS
(1)		000001	MICPC=MICPC+1	
(1)	011770	063223	<MOVE!SPX!BR!SELB!SP3>	
(1)				
512	011772		SP BR,SELB,SP17	;CLEAR SP17
(1)		000002	MICPC=MICPC+1	
(1)	011772	063237	<MOVE!SPX!BR!SELB!SP17>	
(1)				
513	011774		OUT BR,<SELA!OINCON>	;ZERO THE IN CONTROL CSR
(1)		000003	MICPC=MICPC+1	
(1)	011774	061200	<MOVE!WROUTX!BR!<SELA!OINCON>>	
(1)				
514	011776		OUT BR,<SELA!OOCON>	;ZERO THE OUT CONTROL CSR
(1)		000004	MICPC=MICPC+1	
(1)	011776	061202	<MOVE!WROUTX!BR!<SELA!OOCON>>	
(1)				
515	012000		SP IMM,370,SP10	;WRITE 5 ONE BITS TO THE HIGH ORDER
(1)		000005	MICPC=MICPC+1	
(1)	012000	003370	<MOVE!SPX!IMM!370!SP10>	
(1)				
516				;BITS OF SP10
517	012002		SS: SP BR,AA,SP10	;SHIFT SP10 LEFT SETTING CARRY THE
(1)		000006	MICPC=MICPC+1	
(1)	012002	063130	<MOVE!SPX!BR!AA!SP10>	
(1)				
518				;FIRST 5 TIMES THRU THE LOOP
519	012004		MEMINC BR,ADDC!SP3	;WRITE A ONE TO THE FIRST 5 MEMORY
(1)		000007	MICPC=MICPC+1	
(1)	012004	076423	<MOVE!WRMEM!INCMAR!BR!<ADDC!SP3>>	
(1)				
520				;LOCATIONS AND ZERO THE REST
521	012006		SP BR,INCA,SP0	;INCREMENT COUNTER
(1)		000010	MICPC=MICPC+1	
(1)	012006	063060	<MOVE!SPX!BR!INCA!SP0>	
(1)				
522	012010		Z 105	;ALL DONE
(1)		000011	MICPC=MICPC+1	
(1)	012010	101413	<JUMP!ZCOND!<105-INIT&3000*4>!<105-INIT&777/2>>	
(1)				
523	012012		ALWAYS SS	;KEEP GOING
(1)		000012	MICPC=MICPC+1	
(1)	012012	10040E	<JUMP!ALCOND!<SS-INIT&3000*4>!<SS-INIT&777/2>>	
(1)				
524	012014		10\$: SPBR IMM,1,SP1	;WRITE A 1 TO THE BR AND SP1

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(1)      000013      MICPC=MICPC+1
(1) 012014 003401    <MOVE!SPBRX!IMM!1!SP1>

(1)
525 012016      SP      BR,SELB,SP11      ;WRITE A 1 TO SP11
(1)      000014      MICPC=MICPC+1
(1) 012016 063231    <MOVE!SPX!BR!SELB!SP11>

(1)
526 012020      SP      BR,SELB,SP12      ;WRITE A 1 TO SP12
(1)      000015      MICPC=MICPC+1
(1) 012020 063232    <MOVE!SPX!BR!SELB!SP12>

(1)
527 012022      LDMA     IMM,TYPTAB      ;POINT MAR TO TYPE TABLE
(1)      000016      MICPC=MICPC+1
(1)      001      .IF IDN IMM,IMM
(1) 012022 010162    <MOVE!LDMAR!IMM!<TYPTAB&377>>
(1)      .IFF
(1)      <MOVE!LDMAR!IMM!<TYPTAB>>
(1)      .ENDC
(1)      000

(1)
528 012024      BRWRT  IMM,226      ;WRITE SYNC TO MEMORY
(1)      000017      MICPC=MICPC+1
(1) 012024 000626    <MOVE!WRTEBR!IMM!<226>>

(1)
529 012026      OUTPUT  BR,SELB!SYNC    ;LOAD THE SYNC REGISTER
(1)      000020      MICPC=MICPC+1
(1) 012026 062234    <MOVE!WROUT!BR!<SELB!SYNC>>

(1)
530 012030      MEMINC  IMM,3      ;REP
(1)      000021      MICPC=MICPC+1
(1) 012030 016403    <MOVE!WRMEM!INCMAR!IMM!<3>>

(1)
531 012032      MEM     IMM,2      ;NAK
(1)      000022      MICPC=MICPC+1
(1) 012032 002402    <MOVE!WRMEM!IMM!<2>>

(1)
532 012034      SP      MEMX!INCMAR,SELB,SP15      ;SET STARTING COUNT
(1)      000023      MICPC=MICPC+1
(1) 012034 057235    <MOVE!SPX!MEMX!INCMAR!SELB!SP15>

(1)
533 012036      MEMINC  IMM,6      ;START
(1)      000024      MICPC=MICPC+1
(1) 012036 016406    <MOVE!WRMEM!INCMAR!IMM!<6>>

(1)
534 012040      MEMINC  IMM,7      ;STACK
(1)      000025      MICPC=MICPC+1
(1) 012040 016407    <MOVE!WRMEM!INCMAR!IMM!<7>>

(1)
535 012042      MEMINC  IMM,1      ;ACK
(1)      000026      MICPC=MICPC+1
(1) 012042 016401    <MOVE!WRMEM!INCMAR!IMM!<1>>

(1)
536 012044      LDMA     IMM,TABST      ;POINT TO TABLE UPDATE STATE
(1)      000027      MICPC=MICPC+1
(1)      001      .IF IDN IMM,IMM
(1) 012044 010210    <MOVE!LDMAR!IMM!<TABST&377>>
(1)      .IFF

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(1)                                <MOVE!LDMAR!IMM!<TABST>>
(1)                                .ENDC
(1)                                000
537 012046 PSTATI I3 ;INITIALIZE IT
(1) 012046 MEMINC IMM,<<I3-INIT&777/2>>
(2) 000030 MICPC=MICPC+1
(2) 012046 016460 <MOVE!WRMEM!INCMAR!IMM!<<I3-INIT&777/2>>>
(2)
538 012050 PSTATI NIDLE2 ;INITIALIZE PORT STATUS
(1) 012050 MEMINC IMM,<<NIDLE2-INIT&777/2>>
(2) 000031 MICPC=MICPC+1
(2) 012050 016533 <MOVE!WRMEM!INCMAR!IMM!<<NIDLE2-INIT&777/2>>>
(2)
539 012052 LDMA IMM,STC ;LOAD ADDRESS OF LAST TMT CHAIN
(1) 000032 MICPC=MICPC+1
(1) 001 .IF IDN IMM,IMM
(1) 012052 010067 <MOVE!LDMAR!IMM!<STC&377>>
(1) .IFF
(1) <MOVE!LDMAR!IMM!<STC>>
(1) .ENDC
(1) 000
540 012054 MEMINC IMM,TML1 ;STORE ADDRESS OF FIRST TMT LINK
(1) 000033 MICPC=MICPC+1
(1) 012054 016471 <MOVE!WRMEM!INCMAR!IMM!<TML1>>
(1)
541 012056 MEM IMM,TML1
(1) 000034 MICPC=MICPC+1
(1) 012056 002471 <MOVE!WRMEM!IMM!<TML1>>
(1)
542 012060 SP MEMX,SELB,SP16 ;INITIALIZE LAST XMIT POINTER
(1) 000035 MICPC=MICPC+1
(1) 012060 043236 <MOVE!SPX!MEMX!SELB!SP16>
(1)
543 012062 LDMA IMM,SRC ;LOAD ADDRESS OF LAST RECV CHAIN
(1) 000036 MICPC=MICPC+1
(1) 001 .IF IDN IMM,IMM
(1) 012062 010022 <MOVE!LDMAR!IMM!<SRC&377>>
(1) .IFF
(1) <MOVE!LDMAR!IMM!<SRC>>
(1) .ENDC
(1) 000
544 012064 MEMINC IMM,RCL1 ;SET UP ADDRESS OF FIRST RECV LINK
(1) 000037 MICPC=MICPC+1
(1) 012064 016424 <MOVE!WRMEM!INCMAR!IMM!<RCL1>>
(1)
545 012066 MEM IMM,RCL1
(1) 000040 MICPC=MICPC+1
(1) 012066 002424 <MOVE!WRMEM!IMM!<RCL1>>
(1)
546 012070 SP MEMX,SELB,SP14
(1) 000041 MICPC=MICPC+1
(1) 012070 043234 <MOVE!SPX!MEMX!SELB!SP14>
(1)
547 012072 LDMA IMM,NXTINT ;ADDRESS OF NEXT INTERRUPT POINTER TO MAR
(1) 000042 MICPC=MICPC+1
(1) 001 .IF IDN IMM,IMM

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(1) 012072 010240      <MOVE!LDMAR!IMM!<NXTINT&377>>
(1)                    .IFF
(1)                    <MOVE!LDMAR!IMM!<NXTINT>>
(1)                    .ENDC
(1)                    000
548 012074             MEMINC IMM,INTSTK          ;INITIALIZE NEXT INTERRUPT POINTER
(1)                    MICPC=MICPC+1
(1) 012074 016642      <MOVE!WRMEM!INCMAR!IMM!<INTSTK>>
(1)
549 012076             MEM IMM,INTSTK          ;INITIALIZE INSERTION POINTER
(1)                    MICPC=MICPC+1
(1) 012076 002642      <MOVE!WRMEM!IMM!<INTSTK>>
(1)
550 012100             BRWRT IMM,200            ;WRITE THE RUN BIT TO THE BR
(1)                    MICPC=MICPC+1
(1) 012100 000600      <MOVE!WRTEBR!IMM!<200>>
(1)
551 012102             OUT BR,<SELB!OMAIN>      ;WRITE THE RJN BIT TO MAINT CSR
(1)                    MICPC=MICPC+1
(1) 012102 061221      <MOVE!WROUTX!BR!<SELB!OMAIN>>
(1)
552                    ;FALL INTO IDLE LOOP
553                    001
554 012104             .IF NDF $LOW
(1)                    ALWAYS TEOM2
(1)                    MICPC=MICPC+1
(1) 012104 110740      <JUMP!ALCOND!<TEOM2-INIT&3000*4>!<TEOM2-INIT&777 2>>
(1)
555
556 012106             REXIT: SP BR,SELB,SP3
(1)                    MICPC=MICPC+1
(1) 012106 063223      <MOVE!SPX!BR!SELB!SP3>
(1)
557                    .ENDC

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559      .SBTTL IDLE--PROGRAM IDLE LOOP
560      ;PROGRAM IDLE LOOP
561      ;DISPATCHES TO APPROPRIATE SERVICE ROUTINES
562      ;USES STATE POINTERS FOR TMT,RCV,CSR ACTIVITY
563
564      IDLE: BRWRT BR,<SELA!SP10>          ;READ TRANSMIT STATUS WORD FROM SP10 TO BR
          MICPC=MICPC+1
          <MOVE!WRTEBR!BR!<SELA!SP10>>
          BR1 TMTDA                      ;IF DATA TO SEND-- BRANCH
          MICPC=MICPC+1
          <JUMP!BR1CON!<TMTDA-INIT&3000*4>!<TMTDA-INIT&777/2>>
          BR0 TMTDA                      ;IF DATA TO SEND-- BRANCH
          MICPC=MICPC+1
          <JUMP!BR0CON!<TMTDA-INIT&3000*4>!<TMTDA-INIT&777/2>>
          .IF DF SLOW
          ALWAYS I1
          XEXIT: SP BR,SELB,SP2
          .ENDC
          I1: BRWRT IBUS,RCVCON          ;READ LINE UNIT RECEIVE CONTROL WORD
          MICPC=MICPC+1
          <MOVE!WRTEBR!IBUS!<RCVCON>>
          .BR4 BR,SELA,SP3!PAGE1        ;BRANCH BASED UPON RCV STATE
          MICPC=MICPC+1
          <JUMP!BR4CON!BR!SELA!SP3!PAGE1>
          I2: LDMA IMM,TABST             ;POINT TO TABLE UPDATE STATE
          MICPC=MICPC+1
          .IF IDN IMM,IMM
          <MOVE!LDMA!IMM!<TABST&377>>
          .IFF
          <MOVE!LDMA!IMM!<TABST>>
          .ENDC
          .ALWAY MEMX,SELB,0
          MICPC=MICPC+1
          <JUMP!ALCOND!MEMX!SELB!0>
          I3: .IF NDF SLOW
          STATE TMTA+2                  ;GET IDLE TRANSMIT STATE + 1
          MICPC=MICPC+1
          <MOVE!WRTEBR!IMM!<TMTA+2-INIT&777/2>>
          NOP BR,SUB,SP2                ;SUBTRACT FROM CURRENT STATE
          MICPC=MICPC+1
          <BR!SUB!SP2>
          C TMTDA                      ;NON-IDLE STATE
          MICPC=MICPC+1
          <JUMP!CCOND!<TMTDA-INIT&3000*4>!<TMTDA-INIT&777/2>>
          .ENDC
567      001
568
569
570
571      000
572      012116 000054
          (1) 012116 020640
          (1)
573      012120 000055
          (1) 012120 167203
          (1)
574      012122 000056
          (1) 012122 010210
          (1) 001
          (1) 000
          (1)
575      012124 000057
          (1) 012124 140620
          (1)
576      012126 001
577
578      012126 000060
          (1) 012126 000404
          (1)
579      012130 000061
          (1) 012130 060342
          (1)
580      012132 000062
          (1) 012132 111000
          (1)
581      000

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582 012134 000063
(1) 012134 123620
(1)
583 012136 000064
(1) 012136 113255
(1)
584 012140 000065
(1) 012140 023240
(1)
585 012142 000066
(1) 012142 060520
(1)
586 012144 000067
(1) 012144 103454
(1)
587 012146 000070
(1) 001
(1) 012146 010211
(1)
(1) 000
(1)
588 012150 000071
(1) 012150 140620
(1)

IDLE0: SPBR IBUS,UBBR,SPO ;TIMER EXPIRES?
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!UBBR!SPO>

BR4 TIMSRV
MICPC=MICPC+1
<JUMP!BR4CON!<TIMSRV-INIT&3000*4>!<TIMSRV-INIT&777/2>>

SP IBUS,RCVCON,SPO ;READ THE RECEIVE CONTROL REGISTER
MICPC=MICPC+1
<MOVE!SPX!IBUS!RCVCON!SPO>

BRWRT BR,AA!SPO ;SHIFT IT LEFT
MICPC=MICPC+1
<MOVE!WRTBR!BR!<AA!SPO>>

BR7 I1 ;RECEIVE ACTIVE. DON'T DO PORT STATUS
MICPC=MICPC+1
<JUMP!BR7CON!<I1-INIT&3000*4>!<I1-INIT&777/2>>

LDMA IMM,PRTST ;ADDRESS PORT STATE
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMA!IMM!<PRTST&377>>
.IFF
<MOVE!LDMA!IMM!<PRTST>>
.ENDC

.ALWAY MEMX,SELB,0 ;INDEX
MICPC=MICPC+1
<JUMP!ALCOND!MEMX!SELB!0>

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590			.SBTTL BASSRV---- BASE SERVICE ROUTINE	
591	012152		BASSRV: PSTATE NIDLE2	
(1)	012152		MEM IMM,<<NIDLE2-INIT&777/2>>	
(2)		000072	MICPC=MICPC+1	
(2)	012152	002533	<MOVE!WRMEM!IMM!<<NIDLE2-INIT&777/2>>>	
(2)				
592	012154		LDMA IMM,BASE	;CLEAR TO MAR SO IT PCINTS TO BASE POINT
(1)		000073	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	012154	010017	<MOVE!LDMAR!IMM!<BASE&377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<BASE>>	
(1)		000	.ENDC	
(1)				
593	012156		MEMINC IBUS,PORT1	;READ CSR4
(1)		000074	MICPC=MICPC+1	
(1)	012156	136500	<MOVE!WRMEM!INCMAR!IBUS!<PORT1>>	
(1)				
594	012160		MEMINC IBUS,PORT2	;READ CSR5
(1)		000075	MICPC=MICPC+1	
(1)	012160	136520	<MOVE!WRMEM!INCMAR!IBUS!<PORT2>>	
(1)				
595	012162		MEM IBUS,PORT4	
(1)		000076	MICPC=MICPC+1	
(1)	012162	122560	<MOVE!WRMEM!IBUS!<PORT4>>	
(1)				
596	012164		SP IBUS,INCON,SPO	;READ INPUT CONTROL CSR
(1)		000077	MICPC=MICPC+1	
(1)	012164	123000	<MOVE!SPX!IBUS!INCON!SPO>	
(1)				
597	012166		BRWRT IMM,100	;CLEAR THE BR
(1)		000100	MICPC=MICPC+1	
(1)	012166	000500	<MOVE!WRTEBR!IMM!<100>>	
(1)				
598	012170		OUT BR,<AANDB!0INCON>	;CLEAR THE INCONTROL CSR
(1)		000101	MICPC=MICPC+1	
(1)	012170	061260	<MOVE!WROUTX!BR!<AANDB!0INCON>>	
(1)				
599	012172		OUTPUT IMM,<120!0MODEM>	;MASK FOR HDX AND DTR
(1)		000102	MICPC=MICPC+1	
(1)	012172	002133	<MOVE!WROUT!IMM!<120!0MODEM>>	
(1)				
600	012174		BRWRT MEMX,SELB	;READ SEL6
(1)		000103	MICPC=MICPC+1	
(1)	012174	040620	<MOVE!WRTEBR!MEMX!<SELB>>	
(1)				
601	012176		BR4 RESUME	;IF SET RESUME
(1)		000104	MICPC=MICPC+1	
(1)	012176	103113	<JUMP!BR4CON!<RESUME-INIT&3000*4>!<RESUME-INIT&777/2>>	
(1)				
602	012200		LDMA IMM,T	;LOAD ADDRESS OF TYPE FIELD
(1)		000105	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	012200	010151	<MOVE!LDMAR!IMM!<T&377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<T>>	

M06

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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BASSRV---- BASE SERVICE ROUTINE

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(1)          000          .ENDC
(1)
603 012202      000106      MEMINC IMM,6          ;WRITE START TYPE TO MEMORY
(1)          016406      MICPC=MICPC+1
(1)          012202      <MOVE!WRMEM!INCMAR!IMM!<6>>
(1)
604 012204      000107      MEM IMM,300          ;WRITE SELECT AND FINAL TO MEMORY
(1)          002700      MICPC=MICPC+1
(1)          012204      <MOVE!WRMEM!IMM!<300>>
(1)
605 012206      000110      SP BR,DECA,SP1          ;TURN OFF INIT MODE
(1)          063161      MICPC=MICPC+1
(1)          012206      <MOVE!SPX!BR!DECA!SP1>
(1)
606 012210      000111      BS1: BRWRTE IMM,241          ;SET OK TO SEND,STARTMODE AND UNNUM PENDING
(1)          000641      MICPC=MICPC+1
(1)          012210      <MOVE!WRTEBR!IMM!<241>>
(1)
607 012212      000112      ALWAYS SA3
(1)          110737      MICPC=MICPC+1
(1)          012212      <JUMP!ALCOND!<SA3-INIT&3000*4>!<SA3-INIT&777/2>>
(1)
608 012214      000113      RESUME: SP IMM,SP4,4          ;SET UP SP4 FOR COUNTING NPRS
(1)          003004      MICPC=MICPC+1
(1)          012214      <MOVE!SPX!IMM!SP4!4>
(1)
609 012216      000114      SP BR,INCA,SP10          ;SET UNNUMB MESSAGE PENDING TO
(1)          063070      MICPC=MICPC+1
(1)          012216      <MOVE!SPX!BR!INCA!SP10>
(1)
610          000115      ;TRICK TRANSMITTER CODE
611 012220      001          ;ADDRESS BASE TABLE ADDRESS
(1)          010017      LDMA IMM,BASE
(1)          001          MICPC=MICPC+1
(1)          012220      .IF IDN IMM,IMM
(1)          010017      <MOVE!LDMAR!IMM!<BASE&377>>
(1)          000          .IFF
(1)          000          <MOVE!LDMAR!IMM!<BASE>>
(1)          000          .ENDC
(1)
612 012222      000116      STATE FUDGE          ;SET TMTR STATE TO ENTER TABLE UPDATE
(1)          000743      MICPC=MICPC+1
(1)          012222      <MOVE!WRTEBR!IMM!<FUDGE-INIT&777/2>>
613 012224      000117      ALWAYS TBO          ;GO SET UP MXT BITS AND ADRESS OF BASE FOR NPRS
(1)          110455      MICPC=MICPC+1
(1)          012224      <JUMP!ALCOND!<TBO-INIT&3000*4>!<TBO-INIT&777/2>>
(1)
614 012226      000120      BS2: LDMA IMM,IMG10
(1)          001          MICPC=MICPC+1
(1)          012226      .IF IDN IMM,IMM
(1)          010154      <MOVE!LDMAR!IMM!<IMG10&377>>
(1)          000          .IFF
(1)          000          <MOVE!LDMAR!IMM!<IMG10>>
(1)          000          .ENDC
(1)
615 012230      000121      SP MEMX!INCMAR,AORB,SP10          ;RESTORE BIT 1 OF SP10
(1)          000121      MICPC=MICPC+1

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N06

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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(1) 012230 057310      <MOVE!SPX!MEMX!INCMAR!AORB!SP10>
(1)
616 012232      SP      MEMX!INCMAR,SELB,SP11      ;RESTORE SP11
(1)      MICPC=MICPC+1
(1) 012232 057231      <MOVE!SPX!MEMX!INCMAR!SELB!SP11>
(1)
617 012234      SP      MEMX!INCMAR,SELB,SP12      ;RESTORE SP12
(1)      MICPC=MICPC+1
(1) 012234 057232      <MOVE!SPX!MEMX!INCMAR!SELB!SP12>
(1)
618 012236      SP      MEMX!INCMAR,SELB,SP14      ;RESTORE SP14
(1)      MICPC=MICPC+1
(1) 012236 057234      <MOVE!SPX!MEMX!INCMAR!SELB!SP14>
(1)
619 012240      SP      MEMX!INCMAR,SELB,SP16      ;RESTORE SP16
(1)      MICPC=MICPC+1
(1) 012240 057236      <MOVE!SPX!MEMX!INCMAR!SELB!SP16>
(1)
620 012242      SP      MEMX,SELB,SP17      ;RESTORE      SP17
(1)      MICPC=MICPC+1
(1) 012242 043237      <MOVE!SPX!MEMX!SELB!SP17>
(1)
621 012244      SP      BR,DECA,SP10      ;TURN OFF UNNUM MESSAGE PENDING AND
(1)      MICPC=MICPC+1
(1) 012244 063170      <MOVE!SPX!BR!DECA!SP10>
(1)
622      ;ZERO THE BRG
623 012246      SP      BR,DECA,SP1      ;CLEAR INIT MODE
(1)      MICPC=MICPC+1
(1) 012246 063161      <MOVE!SPX!BR!DECA!SP1>
(1)
624 012250      BRWRT IMM,200      ;SET OK TO SEND
(1)      MICPC=MICPC+1
(1) 012250 000600      <MOVE!WRTBR!IMM!<200>>
(1)
625 012252      ALWAYS SA3
(1)      MICPC=MICPC+1
(1) 012252 110737      <JUMP!ALCOND!<SA3-INIT&3000*4>!<SA3-INIT&777/2>>
(1)

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B07

627
628 012254 000133
(1) 012254 060601
(1)
629 001
630 012256 000134
(1) 012256 103141
(1)
631 000
632 001
633
634 000
635 012260 000135
(1) 012260 123400
(1)
636 012262 000136
(1) 012262 001620
(1)
637 012264 000137
(1) 012264 103146
(1)
638
639
640 001
641 012266 000140
(1) 012266 100451
(1)
642 000
643 012270 001
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662 000
663 001
664 012270

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.SBTTL NIDLE2---NO CSR ACTIVITY STATE
NIDLE2: BRWRT BR, SELA!SP1 ;READ PORT STATUS WORD
        MICPC=MICPC+1
        <MOVE!WRTBR!BR!<SELA!SP1>>

        .IF NDF $LOW
        BR4 NIDLE5 ;INTERRUPT PENDING?---BRANCH
        MICPC=MICPC+1
        <JUMP!BR4CON!<NIDLE5-INIT&3000*4>!<NIDLE5-INIT&777/2>>

        .ENDC
        .IF DF $LOW
        BR4 OUTINT
        .ENDC
        SPBR IBUS, INCON, SPO ;READ INPUT CONTROL CSR
        MICPC=MICPC+1
        <MOVE!SPBRX!IBUS!INCON!SPO>

        BRSHFT ;SHIFT IT RIGHT
        MICPC=MICPC+1
        <MOVE!SHFTBR!WRTBR!SELB>

        BR4 INWAT1 ;IF RQI SET -- BRANCH
        MICPC=MICPC+1
        <JUMP!BR4CON!<INWAT1-INIT&3000*4>!<INWAT1-INIT&777/2>>

        ;TO RE-READ THE IN CNTRL REGISTER TO AVOID
        ;A RACE IN MICRO-P READ/UNIBUS WRITE

        .IF NDF $LOW
        ALWAYS IDLE
        MICPC=MICPC+1
        <JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

        .ENDC
NIDLE6:
10$: .IF DF $LOW
        SPBR IBUS, MODEM, SPO ;READ MODEM CONTROL CSR
        BRWRT BR, AA!SPO ;SHIFT IT LEFT
        BR4 SETDSR ;IF DSR SET, CLEAR FLAG
        BRWRT BR, SELA!SP10 ;READ LINE STATUS WORD
        BRSHFT
        BR4 IDLE ;START MODE
        BRWRT BR, AA!SP1 ;READ PORT STATUS WORD
        BR1 IDLE ;INIT MODE
        BR7 IDLE ;DISCONNECT ERROR ALREADY SENT
        SPBR IBUS, MAIN, SPO ;READ THE MAINT REGISTER
        BRWRT BR, ADD!SPO ;SHIFT LEFT
        BR4 IDLE ;LU LOOP -- EXIT
        BRWRT IMM, 100 ;WRITE DISCONNECT ERROR
        SP BR, AORB, SP1 ;FLAG ERROR RECORDED
        ALWAYS ERAXX ;MAKE A CONTROL OUT
        SETDSR: BRWRT IMM, 277 ;CLEAR DISCONNECT ERROR FLAG
        ALWAYS CLRIDL
        .ENDC
        .IF NDF $LOW
        NIDLE5: PSTATE OUTINT ;SET STATE FOR INTERRUPT PROCESSING
```

C07

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NIDLE2---NO CSR ACTIVITY STATE

PAGE: 008C

(1) 012270
(2) 000141
(2) 012270 002614
(2)
665 012272
(1) 000142
(1) 012272 100451
(1)
666 000

MEM IMM,<<OUTINT-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<OUTINT-INIT&777/2>>>

ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

.ENDC

007

668
669 012274 000143
(1) 012274 123400
(1)
(1)
670 012276 000144
(1) 012276 060520
(1)
(1)
671 012300 000145
(1) 012300 103550
(1)
(1)
672
673 012302 000146
(1) 012302 123400
(1)
(1)
674 012304 000147
(1) 012304 103557
(1)
(1)
675 012306
(1) 012306
(2) 000150
(2) 012306 002546
(2)
676 012310 000151
(1) 012310 060520
(1)
(1)
677 012312 000152
(1) 012312 117460
(1)
(1)
678 012314
(1) 012314
(2) 000153
(2) 012314 002543
(2)
679 012316 000154
(1) 012316 000600
(1)
(1)
680 012320 000155
(1) 012320 061300
(1)
(1)
681 012322 000156
(1) 012322 100451
(1)
(1)
682
683 012324 000157
(1) 012324 001620
(1)

.SBTTL INWAIT---WAIT FOR RQI TO CLEAR
INWAIT: SPBR IBUS,INCON,SPO ;READ INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!INCON!SPO>

BRWRT BR,AA!SPO ;SHIFT IT LEFT
MICPC=MICPC+1
<MOVE!WRTBR!BR!<AA!SPO>>

BR7 NIDLE3 ;INTERRUPT ENABLE HAS BEEN SET
MICPC=MICPC+1
<JUMP!BR7CON!<NIDLE3-INIT&3000*4>!<NIDLE3-INIT&777/2>>

INWAT1: SPBR IBUS,INCON,SPO ;READ THE INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!INCON!SPO>

BR7 INWAT2 ;READY IN STILL SET
MICPC=MICPC+1
<JUMP!BR7CON!<INWAT2-INIT&3000*4>!<INWAT2-INIT&777/2>>

NIDLE3: PSTATE INWAT1 ;UPDATE STATE TO INPUT
MEM IMM,<<INWAT1-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<INWAT1-INIT&777/2>>>

BRWRT BR,AA!SPO ;SHIFT CSR LEFT
MICPC=MICPC+1
<MOVE!WRTBR!BR!<AA!SPO>>

BR7 ININT
MICPC=MICPC+1
<JUMP!BR7CON!<ININT-INIT&3000*4>!<ININT-INIT&777/2>>

PSTATE INWAIT ;UPDATE STATE POINTER TO NO INTERRUPT GENERATED
MEM IMM,<<INWAIT-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<INWAIT-INIT&777/2>>>

NIDLE4: BRWRT IMM,200
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<200>>

OUT BR,AORB!OINCON ;SET THE RDY!
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AORB!OINCON>>

ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

INWAT2: BRSHFT ;SHIFT THE BR RIGHT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTBR!SELB>

(1)	684	001	.IF DF \$LOW	
(1)	685		BR4 NIDLE6	;RQI SET--- GO AWAY
(1)	686	000	.ENDC	
(1)	687	001	.IF NDF \$LOW	
(1)	688	012326	BR4 IDLE	
(1)		000160	MICPC=MICPC+1	
(1)		103051	<JUMP!BR4CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)	689	012330	PSTATE INSRV	;SET NEXT STATE TO INPUT SERVICE
(1)		012330	MEM IMM,<<INSRV-INIT&777/2>>	
(2)		000161	MICPC=MICPC+1	
(2)		002563	<MOVE!WRMEM!IMM!<<INSRV-INIT&777/2>>>	
(2)	690	012332	ALWAYS IDLE	
(1)		000162	MICPC=MICPC+1	
(1)		100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)	691	000	.ENDC	
(1)	692	012334	INSRV: SPBR IBUS INCON, SPO	;READ THE INPUT CONTROL CSR
(1)		000163	MICPC=MICPC+1	
(1)		123400	<MOVE!SPBRX!IBUS!INCON!SPO>	
(1)	693	012336	BR1 30\$	--SENSE OR BASE
(1)		000164	MICPC=MICPC+1	
(1)		102600	<JUMP!BR1CON!<30\$-INIT&3000*4>!<30\$-INIT&777/2>>	
(1)	694	012340	BRO 10\$	;CNTL I
(1)		000165	MICPC=MICPC+1	
(1)		102172	<JUMP!BROCON!<10\$-INIT&3000*4>!<10\$-INIT&777/2>>	
(1)	695	012342	BRSHFT	;MUST BE BA/CC-SHIFT FOR IN OR OUT
(1)		000166	MICPC=MICPC+1	
(1)		001620	<MOVE!SHFTBR!WRTEBR!SELB>	
(1)	696	012344	BR1 15\$	
(1)		000167	MICPC=MICPC+1	
(1)		102574	<JUMP!BR1CON!<15\$-INIT&3000*4>!<15\$-INIT&777/2>>	
(1)	697	012346	PSTATE TBASRV	;TRANSMITTER
(1)		012346	MEM IMM,<<TBASRV-INIT&777/2>>	
(2)		000170	MICPC=MICPC+1	
(2)		002700	<MOVE!WRMEM!IMM!<<TBASRV-INIT&777/2>>>	
(2)	698	012350	ALWAYS 20\$	
(1)		000171	MICPC=MICPC+1	
(1)		100575	<JUMP!ALCOND!<20\$-INIT&3000*4>!<20\$-INIT&777/2>>	
(1)	699	012352	10\$: PSTATE CTLSRV	
(1)		012352	MEM IMM,<<CTLSRV-INIT&777/2>>	
(2)		000172	MICPC=MICPC+1	
(2)		002657	<MOVE!WRMEM!IMM!<<CTLSRV-INIT&777/2>>>	
(2)	700	012354	ALWAYS 20\$	
(1)		000173	MICPC=MICPC+1	
(1)		100575	<JUMP!ALCOND!<20\$-INIT&3000*4>!<20\$-INIT&777/2>>	

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```

(1)
701 012356
(1) 012356
(2) 000174
(2) 012356 002721
(2)
702 012360
(1) 000175
(1) 012360 060601
(1)
703 012362
(1) 000176
(1) 012362 102201
(1)
704 012364
(1) 000177
(1) 012364 100451
(1)
705 012366
(1) 000200
(1) 012366 102211
(1)
706 012370
(1) 012370
(2) 000201
(2) 012370 002533
(2)
707 012372
(1) 000202
(1) 012372 000500
(1)
708 012374
(1) 000203
(1) 012374 061260
(1)
709 012376
(1) 000204
(1) 001
(1) 012376 010177
(1)
(1)
(1) 000
(1)
710 012400
(1) 000205
(1) 012400 016402
(1)
711 012402
(1) 000206
(1) 012402 002400
(1)
712 012404
(1) 000207
(1) 012404 042233
(1)
713 012406

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15$: PSTATE RBASRV
MEM IMM,<<RBASRV-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<RBASRV-INIT&777/2>>>

20$: BRWRT BR,SELA!SP1 ;INIT MODE
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELA!SP1>>

BRO PROCER ;IF INIT MODE--ERROR
MICPC=MICPC+1
<JUMP!BROCON!<PROCER-INIT&3000*4>!<PROCER-INIT&777/2>>

ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

30$: BRO INSRV1 ;IF BASE---PROCESS
MICPC=MICPC+1
<JUMP!BROCON!<INSRV1-INIT&3000*4>!<INSRV1-INIT&777/2>>

PROCER: PSTATE NIDLE2 ;RESET PORT STATUS
MEM IMM,<<NIDLE2-INIT&777/2>>
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<<NIDLE2-INIT&777/2>>>

BRWRT IMM,100 ;CLEAR INPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<100>>

OUT BR,AANDB!OINCON ;;
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AANDB!OINCON>>

LDMA IMM,<<RTHRS+3>> ;ADDRESS ERROR LINK
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMA!IMM!<<RTHRS+3>>3377>>
.IFF
<MOVE!LDMA!IMM!<<RTHRS+3>>>
.ENDC

MEMINC IMM,2
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<2>>

MEM IMM,0
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<0>>

OUTPUT MEMX,SELB!OMODEM ;CLEAR DATA TERMINAL READY
MICPC=MICPC+1
<MOVE!WROUT!MEMX!<SELB!OMODEM>>

ALWAYS PCEXX ;POST THE ERROR - FATAL

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INWAIT---WAIT FOR RQI TO CLEAR

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G07

(1) 012406 000210
(1) 114524
(1)
714 012410
(1) 000211
(1) 012410 060601
(1)
715 012412
(1) 000212
(1) 012412 102072
(1)
716 012414
(1) 000213
(1) 012414 100601
(1)

MICPC=MICPC+1
<JUMP!ALCOND!<RCEXX-INIT&3000*4>!<RCEXX-INIT&777/2>>
INSRV1: BRWRT BR,SELA!SP1 ;INIT MODE?
MICPC=MICPC+1
<MOVE!WRTBR!BR!<SELA!SP1>>
BRO BASSRV
MICPC=MICPC+1
<JUMP!BROCON!<BASSRV-INIT&3000*4>!<BASSRV-INIT&777/2>>
ALWAYS PROCER ;NO - PROCEDURE ERROR
MICPC=MICPC+1
<JUMP!ALCOND!<PROCER-INIT&3000*4>!<PROCER-INIT&777/2>>

718			.SBTTL OUTINT---SET UP OUTPUT INTERRUPT [RDY0]
719	012416		OUTINT:
720		001	.IF NDF \$LOW
721	012416		PSTATE PINT2
(1)	012416		MEM IMM,<<PINT2-INIT&777/2>>
(2)		000214	MICPC=MICPC+1
(2)	012416	002631	<MOVE!WRMEM!IMM!<<PINT2-INIT&777/2>>>
(2)			
722		000	.ENDC
723		001	.IF DF \$LOW
724			PSTATE OUTWAIT ;PORT STATUS TO WAITING FOR OUT
725		000	.ENDC
726			;COMPLETION
727	012420		LDMA IMM,NXTINT ;ADDRESS OF NEXT INTERRUPT POINTER
(1)		000215	MICPC=MICPC+1
(1)		001	.IF IDN IMM,IMM
(1)	012420	010240	<MOVE!LDMA!IMM!<NXTINT&377>>
(1)			.IFF
(1)			<MOVE!LDMA!IMM!<NXTINT>>
(1)		000	.ENDC
(1)			
729	012422		LDMA MEMX,SELB ;NEXT INTERRUPT
(1)		000216	MICPC=MICPC+1
(1)		001	.IF IDN MEMX,IMM
(1)			<MOVE!LDMA!IMM!<SELB&377>>
(1)			.IFF
(1)	012422	050220	<MOVE!LDMA!MEMX!<SELB>>
(1)		000	.ENDC
(1)			
729	012424		SP IBUS,OCON,SPD ;READ THE OUTPUT CONTROL CSR
(1)		000217	MICPC=MICPC+1
(1)	012424	123040	<MOVE!SPX!IBUS!OCON!SPD>
(1)			
730	012426		OUT <MEMX!INCMAR>,<AORB!OCON> ;WRITE THE OUT CONTROL CSR
(1)		000220	MICPC=MICPC+1
(1)	012426	055302	<MOVE!WROUTX!MEMX!INCMAR!<AORB!OCON>>
(1)			
731	012430		LDMA MEMX,SELB ;ADDRESS LINK
(1)		000221	MICPC=MICPC+1
(1)		001	.IF IDN MEMX,IMM
(1)			<MOVE!LDMA!IMM!<SELB&377>>
(1)			.IFF
(1)	012430	050220	<MOVE!LDMA!MEMX!<SELB>>
(1)		000	.ENDC
(1)			
732	012432		BRWRT <BR!INCMAR>,<AA!SPD> ;KICK PAST LINK STATUS BYTE
(1)		000222	MICPC=MICPC+1
(1)	012432	074520	<MOVE!WRTBR!BR!INCMAR!<AA!SPD>>
(1)			
733			;SHIFT CSRD IMAGE LEFT
734			;***DO NOT CHANGE BR UNTIL BR7***
735	012434		OUT <MEMX!INCMAR>,<SELB!OPORT1> ;WRITE LOW BYTE OF BA TO CSR
(1)		000223	MICPC=MICPC+1
(1)	012434	055224	<MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT1>>
(1)			
736	012436		OUT <MEMX!INCMAR>,<SELB!OPORT2> ;WRITE HIGH BYTE OF BA TO CSR

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(1)      000224      MICPC=MICPC+1
(1) 012436 055225    <MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT2>>
(1)
737 012440      000225      OUT      <MEMX!INCMAR>,<SELB!OPORT4>      ;WRITE HIGH BYTE OF COUNT TO CSR
(1)      000225      MICPC=MICPC+1
(1) 012440 055227    <MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT4>>
(1)
738 012442      000226      OUT      <MEMX!INCMAR>,<SELB!OPORT3>      ;WRITE THE LOW BYTE OF COUNT
(1)      000226      MICPC=MICPC+1
(1) 012442 055226    <MOVE!WROUTX!MEMX!INCMAR!<SELB!OPORT3>>
(1)
739                                     ;***HERE IS BR7***
740 012444                                     ;INTERPUPT ENABLE IS SET
(1)      000227      BR7      PE1
(1) 012444 103757    MICPC=MICPC+1
(1)                                     <JUMP!BR7CON!<PE1-INIT&3000*4>!<PE1-INIT&777/2>>
(1)
741                                     ;GENERATE AN INTERRUPT
742      001
743 012446      000230      .IF NDF $LOW
(1)      000230      ALWAYS IDLE
(1) 012446 100451    MICPC=MICPC+1
(1)                                     <JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
(1)
744 012450      000231      PINT2: PSTATE OUTWAIT
(1) 012450      002652      MEM      IMM,<<OUTWAIT-INIT&777/2>>
(2)      000231      MICPC=MICPC+1
(2) 012450 002652    <MOVE!WRMEM!IMM!<<OUTWAIT-INIT&777/2>>>
(2)
745      000
746      001
747
748      000
749 012452      000232      .ENDC
(1)      000232      LDMA      IMM,NXTINT      ;ADDRESS NEXT INTERRUPT QUEUE
(1)      001      MICPC=MICPC+1
(1) 012452 010240    .IF IDN IMM,IMM
(1)                                     <MOVE!LDMA!IMM!<NXTINT&377>>
(1)      000      .IFF
(1)                                     <MOVE!LDMA!IMM!<NXTINT>>
(1)      000      .ENDC
(1)
750 012454      000233      SP      MEMX,SELB,SPO      ;COPY ADDRESS FOR NEXT INT TO SPO
(1)      043220      MICPC=MICPC+1
(1)                                     <MOVE!SPX!MEMX!SELB!SPO>
(1)
751 012456      000234      MEM      IMM,INTSTK      ;ASSUME WRAP AROUND CASE
(1)      002642      MICPC=MICPC+1
(1)                                     <MOVE!WRMEM!IMM!<INTSTK>>
(1)
752 012460      000235      BRWRT IMM,<<MMEND-2>>      ;ADDRESS OF LAST INT IN STACK
(1)      000776      MICPC=MICPC+1
(1)                                     <MOVE!WRTBR!IMM!<<MMEND-2>>>
(1)
753 012462      000236      CMP      BR,SPO      ;SHOULD WE WRAP
(1)      060360      MICPC=MICPC+1
(1)                                     <SUBTC!BR!SPO>
(1)
754 012464      Z      SS      ;YES--BRANCH

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OUTINT---SET UP OUTPUT INTERRUPT [RDY0]

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(1)		000237	MICPC=MICPC+1	
(1)	012464	101642	<JUMP!ZCOND!<5\$-INIT&3000*4>!<5\$-INIT&777/2>>	
(1)				
755	012466		BRWRT IMM,2	;OFFSET FOR NEXT POINTER
(1)		000240	MICPC=MICPC+1	
(1)	012466	000402	<MOVE!WRTEBR!IMM!<2>>	
(1)				
756	012470		MEM BR,ADD!SP0	;UPDATE POINTER
(1)		000241	MICPC=MICPC+1	
(1)	012470	062400	<MOVE!WRMEM!BR!<ADD!SP0>>	
(1)				
757	012472		5\$: SP MEMX,SELB,SP0	;COPY POINTER TO SP0
(1)		000242	MICPC=MICPC+1	
(1)	012472	043220	<MOVE!SPX!MEMX!SELB!SP0>	
(1)				
758	012474		LDMA IMM,NXTSP	;PICK UP START OF IN QUEUE
(1)		000243	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	012474	010241	<MOVE!LDMA!IMM!<NXTSP&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<NXTSP>>	
(1)		000	.ENDC	
(1)				
759	012476		CMP MEMX,SP0	;COMPARE TO END
(1)		000244	MICPC=MICPC+1	
(1)	012476	040360	<SUBTC!MEMX!SP0>	
(1)				
760	012500		Z 10\$	;IF EQUAL--CLEAR INT PENDING
(1)		000245	MICPC=MICPC+1	
(1)	012500	101647	<JUMP!ZCOND!<10\$-INIT&3000*4>!<10\$-INIT&777/2>>	
(1)				
761	012502		ALWAYS IDLE	
(1)		000246	MICPC=MICPC+1	
(1)	012502	100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				
762	012504		10\$: BRWRT IMM,357	;MASK TO CLEAR INT PENDING
(1)		000247	MICPC=MICPC+1	
(1)	012504	000757	<MOVE!WRTEBR!IMM!<357>>	
(1)				
763	012506		CLRIDL: SP BR,AANDB,SP1	
(1)		000250	MICPC=MICPC+1	
(1)	012506	063261	<MOVE!SPX!BR!AANDB!SP1>	
(1)				
764	012510		ALWAYS IDLE	
(1)		000251	MICPC=MICPC+1	
(1)	012510	100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				

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OUTWAI--WAIT FOR RDYO TO GO AWAY

PAGE: 0088

766
767 012512 000252
(1) 012512 123440
(1)
(1)
768 001
769
770 000
771 001
772 012514 000253
(1) 012514 103451
(1)
(1)
773 000
774 012516 000254
(1) 012516 000500
(1)
(1)
775 012520 000255
(1) 012520 061262
(1)
(1)
776 012522 000256
(1) 012522 100671
(1)

.SBTTL OUTWAI--WAIT FOR RDYO TO GO AWAY
OUTWAI: SPBR IBUS,OCON,SPO ;READ OUTPUT CONTROL CSR
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!OCON!SPO>

.IF DF SLOW
BR7 NIDLE6 ;RDYO SET --GET OUT
.ENDC
.IF NDF SLOW
BR7 IDLE
MICPC=MICPC+1
<JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

.ENDC
BRWTE IMM,100 ;CLEAR CONTROL BITS
MICPC=MICPC+1
<MOVE!WTEBR!IMM!<100>>

OUT BR,OCON!AANDB
MICPC=MICPC+1
<MOVE!WROUTX!BR!<OCON!AANDB>>

ALWAYS INS13
MICPC=MICPC+1
<JUMP!ALCOND!<INS13-INIT&3000*4>!<INS13-INIT&777/2>>

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CTLSRV--CNTL I SERVICE

PAGE: 0089

778			.SBTTL CTLSRV--CNTL I SERVICE	
779	012524		CTLSRV: SPBR IBUS,PORT4,SPO	;TO SPO
(1)		000257	MICPC=MICPC+1	
(1)	012524	123560	<MOVE!SPBRX!IBUS!PORT4!SPO>	
(1)				
780	012526		BRSFT	
(1)		000260	MICPC=MICPC+1	
(1)	012526	001620	<MOVE!SHFTBR!WRTEBR!SELB>	
(1)				
781	012530		BR1 HDSEL	;IF SET IS HALF DUPLEX
(1)		000261	MICPC=MICPC+1	
(1)	012530	102754	<JUMP!BR1CON!<HDSEL-INIT&3000*4>!<HDSEL-INIT&777/2>>	
(1)				
782	012532		OUTPUT IMM,<100!OMODEM>	;MASK DTR, TURN OFF HDX
(1)		000262	MICPC=MICPC+1	
(1)	012532	002113	<MOVE!WROUT!IMM!<100!OMODEM>>	
(1)				
793	012534		INS11: BRWRTE DP,<SELA!SPO>	;RESTORE THE CNTL WORD
(1)		000263	MICPC=MICPC+1	
(1)	012534	060600	<MOVE!WRTEBR!DP!<SELA!SPO>>	
(1)				
784	012536		BR0 CBOOT	;IF SET IS BOOT
(1)		000264	MICPC=MICPC+1	
(1)	012536	102273	<JUMP!BR0CON!<CBOOT-INIT&3000*4>!<CBOOT-INIT&777/2>>	
(1)				
785	012540		INS12: SP IBUS,INCON,SPO	;READ THE INPUT CONTROL CSR
(1)		000265	MICPC=MICPC+1	
(1)	012540	123000	<MOVE!SPX!IBUS!INCON!SPO>	
(1)				
786	012542		BRWRTE IMM,100	;ZERO THE BR REGISTER EXCEPT INT ENABLE
(1)		000266	MICPC=MICPC+1	
(1)	012542	000500	<MOVE!WRTEBR!IMM!<100>>	
(1)				
787	012544		OUT BR,<AANDB!0INCON>	;CLEAR IN CONTROL CSR
(1)		000267	MICPC=MICPC+1	
(1)	012544	061260	<MOVE!WROUTX!BR!<AANDB!0INCON>>	
(1)				
788	012546		LDMA IMM,PRST	;ADDRESS PORT STATE
(1)		000270	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	012546	010211	<MOVE!LDMA!IMM!<PRST&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<PRST>>	
(1)		000	.ENDC	
(1)				
789	012550		INS13: PSTATE NIDLE2	
(1)	012550		MEM IMM,<<NIDLE2-INIT&777/2>>	
(2)		000271	MICPC=MICPC+1	
(2)	012550	002533	<MOVE!WRMEM!IMM!<<NIDLE2-INIT&777/2>>>	
(2)				
790	012552		ALWAYS IDLE	
(1)		000272	MICPC=MICPC+1	
(1)	012552	100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				
791				
792	012554		CB00T: BRWRTE IMM,200	;MASK FOR BOOT MODE

M07

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-24
CTLSRV--CNTL I SERVICE

PAGE: 0090

(1)		000273	MICPC=MICPC+1	
(1)	012554	000600	<MOVE!WRTEBR!IMM!<200>>	
(1)				
793	012556		SP BR,AORB,SP1	;IN PORT STATUS WORD
(1)		000274	MICPC=MICPC+1	
(1)	012556	063301	<MOVE!SPX!BR!AORB!SP1>	
(1)				
794	012560		BRWRT IMM,204	;MASK FOR OK TO SEND AND LINE IDLE
(1)		000275	MICPC=MICPC+1	
(1)	012560	000604	<MOVE!WRTEBR!IMM!<204>>	
(1)				
795	012562		SP BR,SELB,SP10	;IN LINE STATUS
(1)		000276	MICPC=MICPC+1	
(1)	012562	063230	<MOVE!SPX!BR!SELB!SP10>	
(1)				
796	012564		ALWAYS INS12	
(1)		000277	MICPC=MICPC+1	
(1)	012564	100665	<JUMP!ALCOND!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>	
(1)				

NO7

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-25
TBASRV--TRANSMITTER BUFFER ADDRESS SERVICE

PAGE: 0091

798			.SBTTL TBASRV--TRANSMITTER BUFFER ADDRESS SERVICE	
799	012566	000300	TBASRV: LDMA IMM,ETC	;GET POINTER TO END OF TMT CHAIN
(1)		001	MICPC=MICPC+1	
(1)	012566	010070	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<ETC&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<ETC>>	
(1)		000	.ENDC	
800	012570	000301	LDMA MEMX,<SELB!SPX!SPO>	;FIND THE LINK
(1)		001	MICPC=MICPC+1	
(1)			.IF IDN MEMX,IMM	
(1)			<MOVE!LDMA!IMM!<SELB!SPX!SPO&377>>	
(1)			.IFF	
(1)	012570	053220	<MOVE!LDMA!MEMX!<SELB!SPX!SPO>>	
(1)		000	.ENDC	
801	012572	000302	MEMINC IMM,1	;BUFFER ASSIGNED IN IN LINK FLAGS
(1)		016401	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IMM!<1>>	
802	012574	000303	BRWRT <IMM!INCMAR>,TMLB	;POINT PAST NUMBER FIELD
(1)		014543	MICPC=MICPC+1	
(1)			<MOVE!WRTEBR!IMM!INCMAR!<TMLB>>	
803				;SET BR FOR ADDITION TO SPO
804	012576	000304	MEMINC IBUS,PORT1	
(1)		136500	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT1>>	
805	012600	000305	MEMINC IBUS,PORT2	
(1)		136520	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT2>>	
806	012602	000306	MEMINC IBUS,PORT4	
(1)		136560	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT4>>	
807	012604	000307	MEMINC IBUS,PORT3	
(1)		136540	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT3>>	
808	012606	000310	LDMA IMM,ETC	
(1)		001	MICPC=MICPC+1	
(1)	012606	010070	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<ETC&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<ETC>>	
(1)		000	.ENDC	
809	012610	000311	MEM IMM,TML1	;ASSUME QUEUE WRAP AROUND
(1)		002471	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!IMM!<TML1>>	
810	012612	000312	CMP BR,SPO	;END OF CHAIN
(1)			MICPC=MICPC+1	

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(1) 012612 060360      <SUBTC!BR!SPO>
(1)
811 012614      Z      10$      :IF YES--BRANCH
(1)      MICPC=MICPC+1
(1) 012614 000313      <JUMP!ZCOND!<10$-INIT&3000*4>!<10$-INIT&777/2>>
(1) 012614 101716
(1)
812 012616      BRWRT IMM,6      ;QUEUE ENTRY LENGTH
(1)      MICPC=MICPC+1
(1) 012616 000314      <MOVE!WRTEBR!IMM!<6>>
(1) 012616 000406
(1)
813 012620      MEM      BR,ADD!SPO      ;UPDATE THE END POINTER IN MEMORY
(1)      MICPC=MICPC+1
(1) 012620 000315      <MOVE!WRMEM!BR!<ADD!SPO>>
(1) 012620 062400
(1)
814 012622      10$: BRWRT IMM,2      ;NUMBERED MSG PENDING MASK
(1)      MICPC=MICPC+1
(1) 012622 000316      <MOVE!WRTEBR!IMM!<2>>
(1) 012622 000402
(1)
815 012624      SP      BR,AORB,SP10      ;UPDATE LINE STATUS
(1)      MICPC=MICPC+1
(1) 012624 000317      <MOVE!SPX!BR!AORB!SP10>
(1) 012624 063310
(1)
816 012626      ALWAYS INS12
(1)      MICPC=MICPC+1
(1) 012626 000320      <JUMP!ALCOND!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>
(1) 012626 100665
(1)

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818			.SBTTL RBASRV--RECEIVE BUFFER ADDRESS SERVICE	
819	012630	000321	RBASRV: LDMA IMM,ERC	;ADDRES END OF RECEIVE CHAIN
(1)		001	MICPC=MICPC+1	
(1)	012630	010023	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<ERC&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<ERC>>	
(1)		000	.ENDC	
820	012632	000322	LDMA MEMX,<SELB!SPX!SP0>	;GET THE POINTER TO LINK
(1)		001	MICPC=MICPC+1	
(1)			.IF IDN MEMX,IMM	
(1)			<MOVE!LDMA!IMM!<SELB!SPX!SP0&377>>	
(1)			.IFF	
(1)	012632	053220	<MOVE!LDMA!MEMX!<SELB!SPX!SP0>>	
(1)		000	.ENDC	
821	012634	000323	MEMINC IMM,1	
(1)		016401	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IMM!<1>>	
822	012636	000324	MEMINC IBUS,PORT1	
(1)		136500	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT1>>	
823	012640	000325	MEMINC IBUS,PORT2	
(1)		136520	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT2>>	
824	012642	000326	MEMINC IBUS,PORT4	
(1)		136560	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT4>>	
825	012644	000327	MEMINC IBUS,PORT3	
(1)		136540	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IBUS!<PORT3>>	
826			;;;NOTE INVERTED ORDER OF PORT 3 AND PORT4	
827	012646	000330	LDMA IMM,ERC	
(1)		001	MICPC=MICPC+1	
(1)	012646	010023	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<ERC&377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<ERC>>	
(1)		000	.ENDC	
828	012650	000331	MEM IMM,RCL1	;ASSUME WRAP AROUND CASE
(1)		002424	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!IMM!<RCL1>>	
829	012652	000332	BWRITE IMM,RCL7	;GET ADDRESS OF END OF CAHIN AREA
(1)		000462	MICPC=MICPC+1	
(1)			<MOVE!WRITEBR!IMM!<RCL7>>	
830	012654	000333	CMP BR,SP0	;CHECK FOR END
(1)			MICPC=MICPC+1	

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(1) 012654 060360      <SUBTC!BR!SP0>
(1)
831 012656             Z      INS12                ;IF EQUAL BRANCH
(1) 012656 000334      MICPC=MICPC+1
(1) 012656 101665      <JUMP!ZCOND!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>
(1)
832 012660             BRWRT IMM,5                ;CALCULATE ADDRESS OF NEXT LINK
(1) 012660 000335      MICPC=MICPC+1
(1) 012660 000405      <MOVE!WRTBR!IMM!<5>>
(1)
833 012662             MEM      BR,ADD!SP0          ;...
(1) 012662 000336      MICPC=MICPC+1
(1) 012662 062400      <MOVE!WRMEM!BR!<ADD!SP0>>
(1)
834 012664             ALWAYS INS12                ;EXIT
(1) 012664 000337      MICPC=MICPC+1
(1) 012664 100665      <JUMP!ALCOND!<INS12-INIT&3000*4>!<INS12-INIT&777/2>>
(1)
835 012666             RA1:  BRWRT IMM,317          ;MASK TO CLEAR START MODE AND CLR ACTIVE
(1) 012666 000340      MICPC=MICPC+1
(1) 012666 000717      <MOVE!WRTBR!IMM!<317>>
(1)
836 012670             SPBR      BR,AANDB,SP10      ;CLEAR BIT IN LINE STATUS WORD
(1) 012670 000341      MICPC=MICPC+1
(1) 012670 063670      <MOVE!SPBRX!BR!AANDB!SP10>
(1)
837 012672             RA3:  BRWRT IMM,0            ;CLEAR BR
(1) 012672 000342      MICPC=MICPC+1
(1) 012672 000400      <MOVE!WRTBR!IMM!<0>>
(1)
838 012674             SP      BR,SELB,SP13         ;SET NUMB MESSAGE TYPE IN SP13
(1) 012674 000343      MICPC=MICPC+1
(1) 012674 063233      <MOVE!SPX!BR!SELB!SP13>
(1)
839 012676             STATE  RCVB                ;CHANGE RECEIVE STATE POINTER TO STATE 3
(1) 012676 000344      MICPC=MICPC+1
(1) 012676 000424      <MOVE!WRTBR!IMM!<RCVB-INIT&777/2>>
840 012700             ALWAYS REXIT
(1) 012700 000345      MICPC=MICPC+1
(1) 012700 100450      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
(1)
841
842             001
843 012702             ACK:  .IF NDF $LOW
(1) 012702 000346      BRWRT BR,AA!SP10            ;READ LINE STATUS SHIFTING LEFT
(1) 012702 060530      MICPC=MICPC+1
(1)                                <MOVE!WRTBR!BR!<AA!SP10>>
(1)
844 012704             BR4      $S                ;IF START RECD--CLEAR START MODE
(1) 012704 000347      MICPC=MICPC+1
(1) 012704 103351      <JUMP!BR4CON!<$S-INIT&3000*4>!<$S-INIT&777/2>>
(1)
845 012706             ALWAYS IDLE
(1) 012706 000350      MICPC=MICPC+1
(1) 012706 100451      <JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE INIT&777/2>>
(1)
846 012710             $S:  BRWRT IMM,327          ;CLEAR START MODE

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E08

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-29
RBASRV--RECEIVE BUFFER ADDRESS SERVICE

PAGE: 0095

(1) 000351
(1) 012710 000727
(1) 947 012712
(1) 000352
(1) 012712 063270
(1) 948 012714
(1) 000353
(1) 012714 104507
(1) 949 000

MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<327>>

SP BR,AANDB,SP10 ;IN LINE STATUS
MICPC=MICPC+1
<MOVE!SPX!BR!AANDB!SP10>

ALWAYS RDS
MICPC=MICPC+1
<JUMP!ALCOND!<RDS-INIT&3000*4>!<RDS-INIT&777/2>>

.ENDC

```

851 012716      000354
(1) 012716      000500
(1)
(1)
952 012720      000355
(1) 012720      063310
(1)
(1)
853 012722      000356
(1) 012722      100663
(1)
(1)
854
855 012724      000357
(1) 012724      000700
(1)
(1)
956 012726      000360
(1) 012726      123220
(1)
(1)
857 012730      000361
(1) 012730      061311
(1)
(1)
958          001
859 012732      000362
(1) 012732      100451
(1)
(1)
860          000
861          001
862          000
863          000
864
865 012734      000363
(1)          001
(1) 012734      002722
(1)
(1)
(1)          000
966
867 012736      000364
(1) 012736      000402
(1)
(1)
868 012740      000365
(1) 012740      061231
(1)
(1)
869 012742      000366
(1) 012742      120620
(1)
(1)
870 012744

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HDSEL: BRWRT IMM,100          ;HD MASK TO BR
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<100>>

      SP      BR,AORB,SP10    ;UPDATE PORT STATUS WORD
      MICPC=MICPC+1
      <MOVE!SPX!BR!AORB!SP10>

      ALWAYS INS11
      MICPC=MICPC+1
      <JUMP!ALCOND!<INS11-INIT&3000*4>!<INS11-INIT&777/2>>

PE1:  BRWRT IMM,300          ;MASK FOR INTERRUPT AND VECTOR THROUGH X04
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<300>>

      SP      IBUS,UBBR,SPO    ;READ BR CONTROL REG
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!UBBR!SPO>

      OUT     BR,<AORB!OBR>    ;INTERRUPT
      MICPC=MICPC+1
      <MOVE!WROUTX!BR!<AORB!OBR>>

      .IF NDF $LOW
      ALWAYS IDLE
      MICPC=MICPC+1
      <JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

      .ENDC
      .IF DF $LOW
      ALWAYS PINT2
      .ENDC

HALTED: MEMADR EM6
      MICPC=MICPC+1
      .IF B
      <MOVE!WRMEM!<EM6-INIT&777/2>>
      .IFF
      <MOVE!WRMEM!!<EM6-INIT&777/2>>
      .ENDC

ACLOW: BRWRT IMM,2          ;FALL INTO ACLOW
      MICPC=MICPC+1          ;CAUSE AN AC LOW
      <MOVE!WRTBR!IMM!<2>>

      OUT     BR,<SELB!OBR>
      MICPC=MICPC+1
      <MOVE!WROUTX!BR!<SELB!OBR>>

SS:   BRWRT IBUS,UBBR        ;WAIT FOR IT TO COMPLETE
      MICPC=MICPC+1
      <MOVE!WRTBR!IBUS!<UBBR>>

BR1   SS

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G08

JMC:1 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-31
RBASRV--RECEIVE BUFFER ADDRESS SERVICE

PAGE: 0097

(1) 000367
(1) 012744 102766
(1)
871 012746 000370
(1) 012746 154620
(1)
872 012750 000371
(1) 012750 120620
(1)
873 012752 000372
(1) 012752 103363
(1)
874 012754 000373
(1) 012754 114725
(1)
875
876 012756 000374
(1) 012756 120600
(1)
877 012760 000375
(1) 012760 102051
(1)
878 012762 000376
(1) 012762 114752
(1)
879 012764 000377
(1) 012764 000000
(1)
880

MICPC=MICPC+1
<JUMP!BR1CON!<SS-INIT&3000*4>!<SS-INIT&777/2>>

ALWAY MEMX,SELB,PAGE3
MICPC=MICPC+1
<JUMP!ALCOND!MEMX!SELB!PAGE3>

CKTIME: BRWRT IBUS,UBBR :READ BR CONTROL REG
MICPC=MICPC+1
<MOVE!WRTBR!IBUS!<UBBR>>

BR4 HALTED
MICPC=MICPC+1
<JUMP!BR4CON!<HALTED-INIT&3000*4>!<HALTED-INIT&777/2>>

ALWAYS EM1
MICPC=MICPC+1
<JUMP!ALCOND!<EM1-INIT&3000*4>!<EM1-INIT&777/2>>

IBU1: BRWRT IBUS,NPR
MICPC=MICPC+1
<MOVE!WRTBR!IBUS!<NPR>>

BR0 IDLE
MICPC=MICPC+1
<JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

ALWAYS EC2
MICPC=MICPC+1
<JUMP!ALCOND!<EC2-INIT&3000*4>!<EC2-INIT&777/2>>

\$ZERO
MICPC=MICPC+1
000000

882	012766		.=INIT+1000	
883	000377		MICPC=377	
884			.SBTTL RCVA--ROUTINE TO HANDLE FIRST DDCMP CHARACTER	
885			; ENTERED FROM IDLE LOOP	
886			; DETERMINES IF MESSAGE TYPE IS NUMBERED, UNNUMBERED OR BOOT	
887			; SETS UP APPROPRIATE STATES FOR REST OF MESSAGE.	
888	012766		RCVA: SP IBUS,RCVDAT,SPD ; READ RECEIVE CHARACTER TO SPD	
(1)		000400	MICPC=MICPC+1	
(1)	012766	02320C	<MOVE!SP!IBUS!RCVDAT!SPD>	
(1)				
889	012770		BRWRT BR,SELA!SP1 ; READ PORT STATUS WORD	
(1)		000401	MICPC=MICPC+1	
(1)	012770	060601	<MOVE!WRTBR!BR!SELA!SP1>	
(1)				
890	012772		BR0 55 ; IF INIT MODE---ONLY BOOT OK	
(1)		000402	MICPC=MICPC+1	
(1)	012772	106012	<JUMP!BR0CON!<55-INIT&3000*4>!<55-INIT&777/2>>	
(1)				
891	012774		BR7 55 ; IF BOOT MODE---ONLY BOOT OK	
(1)		000403	MICPC=MICPC+1	
(1)	012774	107412	<JUMP!BR7CON!<55-INIT&3000*4>!<55-INIT&777/2>>	
(1)				
892	012776		BRWRT IMM,201 ; SOH TO BR	
(1)		000404	MICPC=MICPC+1	
(1)	012776	000601	<MOVE!WRTBR!IMM!<201>>	
(1)				
893	013000		CMP BR,SPD ; COMPARE BR TO SPD	
(1)		000405	MICPC=MICPC+1	
(1)	013000	060360	<SUBTC!BR!SPD>	
(1)				
894	013002		Z RA1 ; IF EQUAL-IS NUMBERED MESSAGE	
(1)		000406	MICPC=MICPC+1	
(1)	013002	101740	<JUMP!ZCOND!<RA1-INIT&3000*4>!<RA1-INIT&777/2>>	
(1)				
895	013004		BRWRT IMM,5 ; ENG TO BR	
(1)		000407	MICPC=MICPC+1	
(1)	013004	000405	<MOVE!WRTBR!IMM!<5>>	
(1)				
896	013006		CMP BR,SPD ; COMPARE ENG TO SPD	
(1)		000410	MICPC=MICPC+1	
(1)	013006	060360	<SUBTC!BR!SPD>	
(1)				
897	013010		Z RA2 ; IF EQUAL-IS UNNUMBERED MESSAGE	
(1)		000411	MICPC=MICPC+1	
(1)	013010	105422	<JUMP!ZCOND!<RA2-INIT&3000*4>!<RA2-INIT&777/2>>	
(1)				
898	013012		55: BRWRT IMM,220 ; DLE TO BR	
(1)		000412	MICPC=MICPC+1	
(1)	013012	000620	<MOVE!WRTBR!IMM!<220>>	
(1)				
899	013014		CMP BR,SPD ; COMPARE DLE TO SPD	
(1)		000413	MICPC=MICPC+1	
(1)	013014	060360	<SUBTC!BR!SPD>	
(1)				
900	013016		Z BOOT ; IF EQUAL IS BOOT	
(1)		000414	MICPC=MICPC+1	

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<JUMP!ZCOND!<BOOT-INIT&3000*4>!<BOOT-INIT&777/2>>
FLUSH:  OUTPUT IMM,<200!ORCVCO>          ;FLUSH INPUT SILO
        MICPC=MICPC+1
        <MOVE!WROUT!IMM!<200!ORCVCO>>

        ;(LOW ORDER BITS READ ONLY)
        BRWRT IMM,357                    ;MASK TO CLEAR--CLEAR ACTIVE
        MICPC=MICPC+1
        <MOVE!WRTBR!IMM!<357>>

        SP      BR,AANDB,SP10            ;IN LINE STATUS WORD
        MICPC=MICPC+1
        <MOVE!SPX!BR!AANDB!SP10>

        .IF DF $LOW
        ALWAYS RM1                      ;SET STATE TO RCVA AND RETURN TO IDLE
        .ENDC
RM1:    .IF NDF $LOW
        STATE   RCVA
        MICPC=MICPC+1
        <MOVE!WRTBR!IMM!<RCVA-INIT&777/2>>
        ALWAYS REXIT
        MICPC=MICPC+1
        <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

        .ENDC
RA2:    STATE   RCVI                    ;CHANGE RECEIVE STATE TO I
        MICPC=MICPC+1
        <MOVE!WRTBR!IMM!<RCVI-INIT&777/2>>
        .IF NDF $LOW
        ALWAYS REXIT
        MICPC=MICPC+1
        <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

        .ENDC
REXIT:  .IF DF $LOW
        SP      BR,SELB,SP3
        ALWAYS  IDLE
        .ENDC

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J08

DMC11 CDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-34
RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD

PAGE: 0100

921			.SBTTL RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD
922			;ENTERED FROM IDLE LOOP
923			;STORES COUNT FIELD AND SETS UP RCVB AS NEXT STATE
924			:
925	013036		RCVB: SP IBUS,RCVDAT,SP4 ;READ CHARACTER TO SP4
926	013036		MICPC=MICPC+1
(1)		000424	<MOVE!SPX!IBUS!RCVDAT!SP4>
(1)	013036	023204	
(1)			
927	013040		LDMA BR,<SELA!SP14> ;LOAD MAR WITH ADDRESS OF CURRENT BA
(1)		000425	MICPC=MICPC+1
(1)		001	.IF IDN BR,IMM
(1)			<MOVE!LDMAR!IMM!<SELA!SP14&377>>
(1)			.IFF
(1)	013040	070214	<MOVE!LDMAR!BR!<SELA!SP14>>
(1)		000	.ENDC
(1)			
928	013042		BRWRT MEMX,INCMAR!SELB ;READ FLAGS BYTE
(1)		000426	MICPC=MICPC+1
(1)	013042	054620	<MOVE!WRTBR!MEMX!<INCMAR!SELB>>
(1)			
929	013044		BRO RB1 ;RECV BUFFER ASSIGNED---CONTINUE
(1)		000427	MICPC=MICPC+1
(1)	013044	106041	<JUMP!BROCON!<RB1-INIT&3000*4>!<RB1-INIT&777/2>>
(1)			
930	013046		BRWRT BR,SELA!SP1 ;READ STATUS BYTE
(1)		000430	MICPC=MICPC+1
(1)	013046	060601	<MOVE!WRTBR!BR!<SELA!SP1>>
(1)			
931	013050		BR7 RB3 ;MAINT MODE
(1)		000431	MICPC=MICPC+1
(1)	013050	107437	<JUMP!BR7CON!<RB3-INIT&3000*4>!<RB3-INIT&777/2>>
(1)			
932	013052		LDMA IMM,T ;ERROR--LOAD TYPE FIELD ADDRESS IN MAR
(1)		000432	MICPC=MICPC+1
(1)		001	.IF IDN IMM,IMM
(1)	013052	010151	<MOVE!LDMAR!IMM!<T&377>>
(1)			.IFF
(1)			<MOVE!LDMAR!IMM!<T>>
(1)		000	.ENDC
(1)			
933	013054		MEMINC IMM,2 ;LOAD NAK TYPE
(1)		000433	MICPC=MICPC+1
(1)	013054	016402	<MOVE!WRMEM!INCMAR!IMM!<2>>
(1)			
934	013056		MEM IMM,310 ;LOAD SUB-TYPE NO BUFFERS
(1)		000434	MICPC=MICPC+1
(1)	013056	002710	<MOVE!WRMEM!IMM!<310>>
(1)			
935	013060		LDMA IMM,NTLS
(1)		000435	MICPC=MICPC+1
(1)		001	.IF IDN IMM,IMM
(1)	013060	010012	<MOVE!LDMAR!IMM!<NTLS&377>>
(1)			.IFF
(1)			<MOVE!LDMAR!IMM!<NTLS>>
(1)		000	.ENDC

K08

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD

PAGE: 0101

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(1)
936 013062          ALWAYS RNS                      ;BRANCH TO SEND NAK ROUTINE
(1)          000436
(1) 013062 104552   MICPC=MICPC+1
(1)          104552   <JUMP!ALCOND!<RHS-INIT&3000*4>!<RHS-INIT&777/2>>
(1)
937 013064          RB3: BRWRT IMM,4                  ;MASK FOR NO BUFFER AVAILABLE
(1)          000437   MICPC=MICPC+1
(1) 013064 000404   <MOVE!WRTBR!IMM!<4>>
(1)
938 013066          SP BR,AORB,SP1                    ;SET THE FLAG
(1)          000440   MICPC=MICPC+1
(1) 013066 063301   <MOVE!SPX!BR!AORB!SP1>
(1)
939 013070          RB1: STATE RCVC
(1)          000441   MICPC=MICPC+1
(1) 013070 000461   <MOVE!WRTBR!IMM!<RCVC-INIT&777/2>>
940 013072          RB0: SP BR,SELB,SP3
(1)          000442   MICPC=MICPC+1
(1) 013072 063223   <MOVE!SPX!BR!SELB!SP3>
(1)
941 013074          OUTPUT <MEMX!INCMAR>,<SELB!OBA1>    ;OUTPUT LOW ORDER BYTE OF ADDRESS
(1)          000443   MICPC=MICPC+1
(1) 013074 056226   <MOVE!WROUT!MEMX!INCMAR!<SELB!OBA1>>
(1)
942 013076          OUTPUT MEMX!INCMAR,<SELB!OBA2>    ;OUTPUT HIGH BYTE OF ADDRESS
(1)          000444   MICPC=MICPC+1
(1) 013076 056227   <MOVE!WROUT!MEMX!INCMAR!<SELB!OBA2>>
(1)
943 013100          SP IBUS,UBBR,SP0                  ;READ THE BLS REQ REGISTER
(1)          000445   MICPC=MICPC+1
(1) 013100 123220   <MOVE!SPX!IBUS!UBBR!SP0>
(1)
944 013102          BRWRT IMM,101                      ;MASK OFF ALL BUT NXM AND VEC4 BITS
(1)          000446   MICPC=MICPC+1
(1) 013102 000501   <MOVE!WRTBR!IMM!<101>>
(1)
945 013104          SP BR,AANDB,SP0                    ;AND SAVE IN SP0
(1)          000447   MICPC=MICPC+1
(1) 013104 063260   <MOVE!SPX!BR!AANDB!SP0>
(1)
946 013106          SP IMM,300,SP5                     ;MASK TO ISOLATE EX. MEM BITS
(1)          000450   MICPC=MICPC+1
(1) 013106 003305   <MOVE!SPX!IMM!300!SP5>
(1)
947          ;NOTE THIS REALLY WRITES A 305 BUT THE
948          ;5 GETS SHIFTED OUT
949 013110          BRWRT MEMX,AANDB!SP5               ;MASK ALL BUT EX. MEM BITS
(1)          000451   MICPC=MICPC+1
(1) 013110 040665   <MOVE!WRTBR!MEMX!<AANDB!SP5>>
(1)
950 013112          BRSHFT                               ;SHIFT THEM INTO THE CORRECT POSITION
(1)          000452   MICPC=MICPC+1
(1) 013112 003520   <MOVE!SHFTBR!WRTBR!SELB>
(1)
951 013114          BRSHFT
(1)          000453   MICPC=MICPC+1

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LOS

CMC11 DDCMP PROTOCOL IMPLEMENTATION
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RCVB--ROUTINE TO HANDLE FIRST CHARACTER OF COUNT FIELD

PAGE: 0102

(1)	013114	001620	<MOVE!SHFTBR!WRTEBR!SELB>	
(1)				
952	013116		BRSHT	
(1)		000454	MICPC=MICPC+1	
(1)	013116	001620	<MOVE!SHFTBR!WRTEBR!SELB>	
(1)				
953	013120		BRSHT	
(1)		000455	MICPC=MICPC+1	
(1)	013120	001620	<MOVE!SHFTBR!WRTEBR!SELB>	
(1)				
954	013122		OUT BR,AORB!OBR	;WRITE EX MEM BITS OUT
(1)		000456	MICPC=MICPC+1	
(1)	013122	061311	<MOVE!WROUTX!BR!<AORB!OBR>>	
(1)				
955	013124		ALWAYS IDLE	
(1)		000457	MICPC=MICPC+1	
(1)	013124	100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				
956	013126		RB2: ALWAYS I2	
(1)		000460	MICPC=MICPC+1	
(1)	013126	100456	<JUMP!ALCOND!<I2-INIT&3000*4>!<I2-INIT&777/2>>	
(1)				

958
959
960
961
962
963 013130
964 001
965
966 000
967 001
968 013130
(1) 000461
(1) 013130 023205
(1)
969 013132
(1) 000462
(1) 013132 000600
(1)
970 013134
(1) 000463
(1) 013134 060665
(1)
971 013136
(1) 000464
(1) 013136 063310
(1)
972 013140
(1) 000465
(1) 002
(1) 013140 010167
(1)
(1)
(1) 001
(1)
973 013142
(1) 000466
(1) 013142 076604
(1)
974 013144
(1) 000467
(1) 013144 076605
(1)
975 000
976 013146
(1) 000470
(1) 013146 000472
977 013150
(1) 000471
(1) 013150 100450
(1)

.SBTTL RCVC--ROUTINE TO HANDLE SECOND CHARACTER OF COUNT FIELD, SELECT AND FINA
;ENTERED FROM IDLE LOOP
;INTERPRETS SELECT AND FINAL
;CHECKS FOR COUNT TOO LARGE
;
RCVC:
.IF DF \$LOW
ALWAYS SELQSY ;"CALL" SELECT/QSYNC SUBROUTINE
.ENDC
.IF NDF \$LOW
SP IBUS,RCVDAT,SP5 ;GET CHARACTER
MICPC=MICPC+1
<MOVE!SPX!IBUS!RCVDAT!SP5>

BRWRT IMM,200 ;SEPARATE SELECT BIT FROM COUNT
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<200>>

BRWRT BR,AANDB!SP5
MICPC=MICPC+1
<MOVE!WRTBR!BR!<AANDB!SP5>>

SP BR,AORB,SP10
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>

LDMA IMM,BC ;LOAD MAR TO BYTE COUNT
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMAR!IMM!<BC&377>>
.IFF
<MOVE!LDMAR!IMM!<BC>>
.ENDC

MEMINC BR,SELA!SP4 ;SAVE LOW BYTE
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!BR!<SELA!SP4>>

MEMINC BR,SELA!SP5 ;AND NOW HIGH BYTE
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!BR!<SELA!SP5>>

.ENDC
RCS: STATE RCVD ;SET NEXT STATE TO D
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RCVD-INIT&777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

979
980
981 013152 000472
(1) 013152 000513
982 013154 000473
(1) 013154 063223
(1)
983 013156 000474
(1) 013156 023600
(1)
984 013160 000475
(1) 013160 060757
(1)
985 013162 000476
(1) 013162 107500
(1)
986 013164 000477
(1) 013164 100451
(1)
987 013166 000500
(1) 013166 060601
(1)
988 013170 000501
(1) 013170 103451
(1)
989 013172 000502
(1) 013172 060610
(1)
990 013174 000503
(1) 013174 001620
(1)
991 013176 000504
(1) 013176 103051
(1)
992 013200 000505
(1) 001
(1) 013200 010153
(1)
(1)
(1) 000
(1)
993 013202 000506
(1) 013202 062600

.SBTTL RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES
RCVD: STATE RCVE
MICPC=MICPC+1
<MOVE!WTEBR!IMM!<RCVE-INIT&777/2>>
RD2: SP BR,SELB,SP3 ;SAVE THE STATE
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP3>
SPBR IBUS,RCVDAT,SPO ;INPUT THE CHARACTER
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!RCVDAT!SPO>
BRWTE BR,SUB!SP17 ;COMPARE NEW R TO LAST R
MICPC=MICPC+1
<MOVE!WTEBR!BR!<SUB!SP17>>
BR7 10\$;IF NEW IS GREATER---PROCESS
MICPC=MICPC+1
<JUMP!BR7CON!<10\$-INIT&3000*4>!<10\$-INIT&777/2>>
ALWAYS IDLE
MICPC=MICPC+1
<JUM?!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
10\$: BRWTE BR,SELA!SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVE!WTEBR!BR!<SELA!SP1>>
BR7 IDLE ;MAINT. MODE - GET OUT
MICPC=MICPC+1
<JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
BRWTE BR,SELA!SP10
MICPC=MICPC+1
<MOVE!WTEBR!BR!<SELA!SP10>>
BRSHFT
MICPC=MICPC+1
<MOVE!SHFTBR!WTEBR!SELB>
BR4 IDLE
MICPC=MICPC+1
<JUMP!BR4CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
LDMA IMM,ISP17 ;ADDRESS LAST ACKED IMAGE
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMAR!IMM!<ISP17&377>>
.IFF
<MOVE!LDMAR!IMM!<ISP17>>
.ENDC
MEM BR,SELA!SPO ;COPY THE CHAR
MICPC=MICPC+1
<MOVE!WRMEM!BR!<SELA!SPO>>

B09

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RCVD--ROUTINE TO HANDLE RESPONSE FIELD FOR NUMBERED MESSAGES

PAGE: 0105

(1)				
994	013204		RDS:	BW RTE IMM! LDMAR, REPST ; SET UP COUNT FOR TIMER
(1)		000507		MICPC=MICPC+1
(1)	013204	010403		<MOVE! W RTE BR! IMM! LDMAR! <REPST>>
(1)				
995				; ****DEPENDENT ON REPST = 2
996	013206		MEM IMM, 1	; RESET REP THRESHOLD
(1)		000510	MICPC=MICPC+1	
(1)	013206	002401	<MOVE! WR MEM! IMM! <1>>	
(1)				
997	013210		SP BR, SELB, SP15	: RESET THE COUNT
(1)		000511	MICPC=MICPC+1	
(1)	013210	063235	<MOVE! SPX! BR! SELB! SP15>	
(1)				
998	013212		ALWAYS IDLE	
(1)		000512	MICPC=MICPC+1	
(1)	013212	100451	<JUMP! AL COND! <IDLE-INIT&3000*4>! <IDLE-INIT&777/2>>	
(1)				

```

1000
1001
1002 013214 000513
      (1) 013214 060601
      (1)
1003 013216 000514
      (1) 013216 107703
      (1)
1004 013220 000515
      (1) 013220 020600
      (1)
1005 013222 000516
      (1) 013222 060371
      (1)
1006 013224 000517
      (1) 013224 105522
      (1)
1007 013226 000520
      (1) 013226 063173
      (1)
1008 013230 000521
      (1) 013230 104523
      (1)
1009 013232 000522
      (1) 013232 063071
      (1)
1010 013234 000523
      (1) 013234 000525
1011 013236 000524
      (1) 013236 100450
      (1)

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.SP TL RCVE--ROUTINE TO HANDLE N FIELD OF NUMBERED MESSAGE
RCVE: BRWRT BR SELA!SP1 ;READ THE STATUS BYTE
      MICPC=MICPC+1
      <MOVE!WRTBR!BR!<SELA!SP1>>

      BR7 RCVQ
      MICPC=MICPC+1
      <JUMP!BR7CON!<RCVQ-INIT&3000*4>!<RCVQ-INIT&777/2>>

      BRWRT IBUS,RCVDAT ;INPUT THE CHARACTER
      MICPC=MICPC+1
      <MOVE!WRTBR!IBUS!<RCVDAT>>

      CMP BR,SP11
      MICPC=MICPC+1
      <SUBTC!BR!SP11>

      Z SS
      MICPC=MICPC+1
      <JUMP!ZCOND!<SS-INIT&3000*4>!<SS-INIT&777/2>>

      SP BR,DECA,SP13 ;FORCE MSG TYPE TO -1
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP13>

      ALWAYS RE2
      MICPC=MICPC+1
      <JUMP!ALCOND!<RE2-INIT&3000*4>!<RE2-INIT&777/2>>

SS: SP BR,INCA,SP11 ;UPDATE R FIELD
     MICPC=MICPC+1
     <MOVE!SPX!BR!INCA!SP11>

RE2: STATE RCVF ;NEXT RECEIVE STATE IS F
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<RCVF-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

```

1013
1014 013240 000525
(1) 013240 063164
(1)
(1)
1015 013242 000526
(1) 013242 105130
(1)
(1)
1016 013244 000527
(1) 013244 063165
(1)
(1)
1017 013246 000530
(1) 013246 000533
(1)
1018 013250 000531
(1) 013250 020200
(1)
(1)
1019 013252 000532
(1) 013252 100450
(1)
(1)
1020
1021
1022
1023 013254 000533
(1) 013254 000535
(1)
1024 013256 000534
(1) 013256 104531
(1)
(1)

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.SBTTL RCVF--ROUTINE TO IGNORE ADDRESS
RCVF:  SP      BR,DECA,SP4          ;DECREMENTLOW BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP4>

      C      RCVF0          ;NO OVERFLOW
      MICPC=MICPC+1
      <TUMP!CCOND!<RCVF0-INIT&3000*4>!<RCVF0-INIT&777/2>>

      SP      BR,DECA,SP5          ;OVERFLOW - DECREMENT HIGH BYTE
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP5>

RCVF0:  STATE  RCVG
      MICPC=MICPC+1
      <MOVE!WTEBR!IMM!<RCVG-INIT&777/2>>

RCVF1:  NOP      IBUS,RCVDAT,0          ;INPUT CHARACTER - AND DISCARD
      MICPC=MICPC+1
      <IBUS!RCVDAT!0>

      ALWAYS  REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

;
.SBTTL RCVG--ROUTINE TO IGNORE CRC1
RCVG:  STATE  RCVH          ;NEXT STATE IS RCVH
      MICPC=MICPC+1
      <MOVE!WTEBR!IMM!<RCVH-INIT&777/2>>
      ALWAYS  RCVF1
      MICPC=MICPC+1
      <JUMP!ALCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>

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1026      .SBTTL RCVH--ROUTINE TO HANDLE CRC2 AND TO DISPATCH NUMBERED AND UNNUMBERED TYP
1027      ;
1028      RCVH:  SP      IBUS,RCVDAT,SPD      ;GET CHAR IN SPD
1029      MICPC=MICPC+1
1030      <MOVE!SPX!IBUS!RCVDAT!SPD>
1031      BRWRT  IBUS,RCVCON      ;READ RECVR CONTROL REGISTER
1032      MICPC=MICPC+1
1033      <MOVE!WRTBR!IBUS!<RCVCON>>
1034      BR0     TDON1      ;IF BCC MATCH SET CRC IS GOOD
1035      MICPC=MICPC+1
1036      <JUMP!BROCON!<TDON1-INIT&3000*4>!<TDON1-INIT&777/2>>
1037      BRWRT  BR,SELA!SP1      ;READ STATUS BYTE
1038      MICPC=MICPC+1
1039      <MOVE!WRTBR!BR!<SELA!SP1>>
1040      BR7     RHX      ;MAINT MODE
1041      MICPC=MICPC+1
1042      <JUMP!BR7CON!<RHX-INIT&3000*4>!<RHX-INIT&777/2>>
1043      BRWRT  DP,<SELA!SP10>      ;READ PORT STATUS WORD TO BR
1044      MICPC=MICPC+1
1045      <MOVE!WRTBR!DP!<SELA!SP10>>
1046      BRSHFT
1047      MICPC=MICPC+1
1048      <MOVE!SHFTBR!WRTBR!SELB>
1049      BR4     SNAK1      ;IF START MODE--PROCEED TO RESEND START
1050      MICPC=MICPC+1
1051      <JUMP!BR4CON!<SNAK1-INIT&3000*4>!<SNAK1-INIT&777/2>>
1052      LDMA    IMM,T      ;ELSE BCC ERROR--LOAD ADDRESS OF TYPE FI
1053      MICPC=MICPC+1
1054      .IF IDN IMM,IMM
1055      <MOVE!LDMA!IMM!<T&377>>
1056      .IFF
1057      <MOVE!LDMA!IMM!<T>>
1058      .ENDC
1059      MEMINC  IMM,2      ;WRITE NAK TYPE
1060      MICPC=MICPC+1
1061      <MOVE!WRMEM!INCMAR!IMM!<2>>
1062      MEMINC  IMM,301      ;WRITE HEADER BCC ERROR SUBTYPE
1063      MICPC=MICPC+1
1064      <MOVE!WRMEM!INCMAR!IMM!<301>>
1065      MEM     BR,SELA!SP17      ;RESTORE LAST ACKED IMAGE
1066      MICPC=MICPC+1
1067      <MOVE!WRMEM!BR!<SELA!SP17>>
1068      LDMA    IMM,NHDS      ;ADDRESS CUM ERROR COUNTER

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(1)		000551	MICPC=MICPC+1	
(1)		001	.IF IDN IMM IMM	
(1)	013310	010013	<MOVE!LDMAR!IMM!<NHDS\$377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<NHDS>>	
(1)		000	.ENDC	
1042	013312		RH5: SP MEMX SELB SPO	;WRITE IT TO SPO
(1)		000552	MICPC=MICPC+1	
(1)	013312	043220	<MOVE!SPX!MEMX!SELB!SPO>	
(1)				
1043	013314		MEM BR INCA!SPO	;INCREMENT IT
(1)		000553	MICPC=MICPC+1	
(1)	013314	062460	<MOVE!WRMEM!BR!<INCA!SPO>>	
(1)				
1044	013316		LDMA IMM NAKST	;ADDRESS NAKS TMED DYNAMIC
(1)		000554	MICPC=MICPC+1	
(1)		001	.IF IDN IMM IMM	
(1)	013316	010001	<MOVE!LDMAR!IMM!<NAKST\$377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<NAKST>>	
(1)		000	.ENDC	
1045	013320		BRWRT MEMX SELB	;WRITE IT TO BR
(1)		000555	MICPC=MICPC+1	
(1)	013320	040620	<MOVE!WRTEBR!MEMX!<SELB>>	
(1)				
1046	013322		BSHFTB	;SHIFT IT RIGHT
(1)		000556	MICPC=MICPC+1	
(1)	013322	061620	<MOVE!SHFTBR!SELB!BR>	
(1)				
1047	013324		MEM BR SELB	;UPDATE IT
(1)		000557	MICPC=MICPC+1	
(1)	013324	062620	<MOVE!WRMEM!BR!<SELB>>	
(1)				
1048	013326		BRO NTHRES	;BRANCH IF THRESHOLD EXCEEDED
(1)		000560	MICPC=MICPC+1	
(1)	013326	116256	<JUMP!BROCON!<NTHRES-INIT\$3000*4>!<NTHRES-INIT\$777/2>>	
(1)				
1049	013330		ALWAYS SNAK	
(1)		000561	MICPC=MICPC+1	
(1)	013330	114704	<JUMP!ALCOND!<SNAK-INIT\$3000*4>!<SNAK-INIT\$777/2>>	
(1)				
1050	013332		RH3: BRWRT DP <DECA!SP13>	;LOAD TYPE RECEIVED--DECREMENTING
(1)		000562	MICPC=MICPC+1	
(1)	013332	060573	<MOVE!WRTEBR!DP!<DECA!SP13>>	
(1)				
1051	013334		Z RH1	;IF ALJOUT IS ALL ONES IS NUMBERED MSG
(1)		000563	MICPC=MICPC+1	
(1)	013334	115467	<JUMP!ZCOND!<RH1-INIT\$3000*4>!<RH1-INIT\$777/2>>	
(1)				
1052	013336		RSTATE RCVA	
(1)		000564	MICPC=MICPC+1	
(1)	013336	000400	<MOVE!WRTEBR!IMM!<RCVA-INIT\$777/2>>	
(1)		000565	MICPC=MICPC+1	
(1)	013340	063223	<MOVE!SPX!BR!SELB!SP3>	

```

1053 013342 000566
(1) 013342 060610
(1)
(1) 001
1054
1055
1056
1057 000
1058 001
1059 013344 000567
(1) 013344 002212
(1)
1060 000
1061 013346 000570
(1) 013346 001620
(1)
1062 013350 000571
(1) 013350 107177
(1)
1063 013352 000572
(1) 001
(1) 013352 010162
(1)
(1) 000
(1)
1064 013354 000573
(1) 013354 054373
(1)
1065 013356 000574
(1) 013356 115411
(1)
1066 013360 000575
(1) 013360 054373
(1)
1067 013362 000576
(1) 013362 115445
(1)
1068 013364 000577
(1) 001
(1) 013364 010164
(1)
(1) 000
(1)
1069 013366 000600
(1)

```

```

BRWRT DP, <SELA!SP10> ;LOAD LINE STATUS WORD IN BR
MICPC=MICPC+1
<MOVE!WRTEBR!DP!<SELA!SP10>>

IF DF SLOW
BR4 FLUSH1

CG1: .ENDC
IF NDF SLOW
OUTPUT IMM, <200!ORCVCC>
MICPC=MICPC+1
<MOVE!WROUT!IMM!<200!ORCVCC>>

.ENDC
BRSHFT ;SHIFT RIGHT
MICPC=MICPC+1
<MOVE!SHFTBR!WRTEBR!SELB>

BR4 10$
MICPC=MICPC+1
<JUMP!BR4CON!<10$-INIT&3000*4>!<10$-INIT&777/2>>

LDMA IMM, TYPTAB ;ADDRESS TYPE TABLE
MICPC=MICPC+1
IF IDN IMM, IMM
<MOVE!LDMAR!IMM!<TYPTAB&377>>
IF
<MOVE!LDMAR!IMM!<TYPTAB>>
.ENDC

CMP <MEMX!INCMAR>, SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>

Z REP
MICPC=MICPC+1
<JUMP!ZCOND!<REP-INIT&3000*4>!<REP-INIT&777/2>>

CMP <MEMX!INCMAR>, SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>

Z NAK
MICPC=MICPC+1
<JUMP!ZCOND!<NAK-INIT&3000*4>!<NAK-INIT&777/2>>

10$: LDMA IMM, TYPSTT ;SET POINTER TO START TYPE
MICPC=MICPC+1
IF IDN IMM, IMM
<MOVE!LDMAR!IMM!<TYPSTT&377>>
IF
<MOVE!LDMAR!IMM!<TYPSTT>>
.ENDC

CMP <MEMX!INCMAR>, SP13
MICPC=MICPC+1

```

(1) 013366 054373
(1) 013370 000601
(1) 013370 115420
(1) 013372 000602
(1) 013372 054373
(1) 013374 000603
(1) 013374 115422
(1) 013376 000604
(1) 013376 054373
(1) 013400 000605
(1) 013400 101746
(1) 013402 000606
(1) 013402 100451
(1) 001
(1) 005

<SUBTC!MEMX!INCMAR!SP13>
Z START
MICPC=MICPC+1
<JUMP!ZCOND!<START-INIT&3000*4>!<START-INIT&777/2>>
;STACK TYPE
CMP <MEMX!INCMAR>,SP13
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>
Z STACK
MICPC=MICPC+1
<JUMP!ZCOND!<STACK-INIT&3000*4>!<STACK-INIT&777/2>>
CMP <MEMX!INCMAR>,SP13 ;ACK TYPE
MICPC=MICPC+1
<SUBTC!MEMX!INCMAR!SP13>
Z ACK
MICPC=MICPC+1
<JUMP!ZCOND!<ACK-INIT&3000*4>!<ACK-INIT&777/2>>
ALWAYS IDLE ;OTHERWISE IGNORE--MUST BE CDS MSG
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

RCVCK: .IF DF SLOW
SPBR IBUS,RCVCON.SPD ;READ RCVR CONTROL CSR
BRWRT BR,ADD!SPD ;SHIFT LEFT
BR7 I1
ALWAYS TAI
ACK: BRWRT BR,AA!SP1D ;READ LINE STATUS-SHIFTING LEFT
BR4 SS ;IF START RECD -- CLEAR START MODE
ALWAYS IDLE
SS: BRWRT IMM,327 ;CLEAR START MODE
SP BR,AND8.SP1D ;IN LINE STATUS
ALWAYS RDS
.ENDC

1090
1091
1092 013404 000607
(1) 013404 123600
(1)
1093 013406 000610
(1) 013406 102051
(1)
1094 013410 000611
(1) 013410 000600
(1)
1095 001
1096 013412 000612
(1) 013412 063300
(1)
1097 000
1098 001
1099
1100 000
1101 013414 000613
(1) 013414 000653
(1)
1102 013416 000614
(1) 013416 104620
(1)
1103
1104 013420 000615
(1) 013420 123600
(1)
1105 001
1106 013422 000616
(1) 013422 106247
(1)
1107 000
1108 001
1109
1110 000
1111 013424 000617
(1) 013424 000625
(1)
1112 013426 000620
(1) 013426 063223
(1)
1113 013430 000621
(1) 013430 022203
(1)
1114 013432

*****TIME CRITICAL CODE-- CHANGE WITH GREAT CARE*****
RCVK01: SBTTL RCVK01--ROUTINE TO HANDLE FIRST BYTE ODD RECEIVE
SPBR IBUS,NPR,SPO ;READ NPR REGISTER
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!NPR!SPO>

BRO IDLE
MICPC=MICPC+1
<JUMP!BROCON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

BRWRT IMM,200 ;MASK FOR CO(BYTE TRANSFER)
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<200>>

.IF NDF \$LOW
SP BR,AORB,SPO
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SPO>

.ENDC
.IF DF \$LOW
OUT BR,<AORB!ONPR> ;TURN ON CO
.ENDC
STATE RKE1
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RKE1-INIT&777/2>>
ALWAYS RCVK02
MICPC=MICPC+1
<JUMP!ALCOND!<RCVK02-INIT&3000*4>!<RCVK02-INIT&777/2>>

RCVK0: SBTTL RCVK0--PROCESS ODD CHARACTER
SPBR IBUS,NPR,SPO ;IS AN NPR GOING
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!NPR!SPO>

.IF NDF \$LOW
BRO RK66 ;IF SO, REITERATE ODD AND EXIT
MICPC=MICPC+1
<JUMP!BROCON!<RK66-INIT&3000*4>!<RK66-INIT&777/2>>

.ENDC
.IF DF \$LOW
BRO IDLE ;IF SO, GO BACK TO IDLE LOOP
.ENDC
STATE RCVKE
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RCVKE-INIT&777/2>>

RCVK02: SP BR,SELB,SP3 ;SET STATE
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP3>

OUTPUT IBUS,RCVDAT!OUTDA2 ;OUTPUT A CHAR
MICPC=MICPC+1
<MOVE!WROUT!IBUS!<RCVDAT!OUTDA2>>

RK8: BRWRT IMM,21 ;SET OUT NPR (C1) AND NPR REG

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RCVKO--PROCESS ODD CHARACTER

PAGE: 0113

(1) 000622
(1) 013432 000421
(1)
1115 001
1116
1117 000
1118 013434
(1) 000623
(1) 013434 061310
(1)
1119 013436
(1) 000624
(1) 013436 100451
(1)

MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<21>>

.IF DF SLOW
SP IBUS,NPR,SPO ;READ NPR REGISTER
.ENDC
RK7: OUT BR,<AORB!ONPR> ;WRITE NPR REGISTER
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AORB!ONPR>>

ALWAYS IDLE
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>;

```

1121
1122 013440 000625
(1) 013440 120600
(1)
1123 001
1124 013442 000626
(1) 013442 107251
(1)
1125 000
1126 001
1127
1128 000
1129 013444 000627
(1) 013444 023140
(1)
1130 013446 000630
(1) 013446 062066
(1)
1131 013450 000631
(1) 013450 063164
(1)
1132 013452 000632
(1) 013452 105235
(1)
1133 013454 000633
(1) 013454 063165
(1)
1134 013456 000634
(1) 013456 105711
(1)
1135 013460 000635
(1) 013460 022202
(1)
1136 013462 000636
(1) 013462 023140
(1)
1137 013464 000637
(1) 013464 062066
(1)
1138 013466 000640
(1) 013466 115035
(1)
1139 013470 000641
(1)

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RCVKE: SBTTL RCVKE--HANDLE EVEN BYTES
        BRWRT IBUS,NPR ;READ NPR CONTROL REGISTER
        MICPC=MICPC+1
        <MOVE!WRTBR!IBUS!<NPR>>

        .IF NDF $LOW
        BR4 RK4 ;IF RECV NPR--BRANCH
        MICPC=MICPC+1
        <JUMP!BR4CON!<RK4-INIT&3000*4>!<RK4-INIT&777/2>>

        .ENDC
        .IF DF $LOW
        BRO IDLE
        .ENDC
RK5: SP IBUS,IOBA1,SP0 ;READ LOW BYTE OF BA TO SP
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IOBA1!SP0>

      OUTPUT DP,<INCA!OBA1> ;WRITE INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!DP!<INCA!OBA1>>

RK50: SP BR,DECA,SP4 ;DECREMENT CHARACTER CCUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP4>

C 10$ ;NO OVERFLOW
MICPC=MICPC+1
<JUMP!CCOND!<10$-INIT&3000*4>!<10$-INIT&777/2>>

SP BR,DECA,SP5 ;OVERFLOW - DECREMENT HIGH BYTE
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP5>

Z RL3 ;BYTE COUNT ZERO
MICPC=MICPC+1
<JUMP!ZCOND!<RL3-INIT&3000*4>!<RL3-INIT&777/2>>

10$: OUTPUT IBUS,<RCVDAT!OUTDA1> ;READ CHARACTER AND WRITE IT
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<RCVDAT!OUTDA1>>

SP IBUS,IOBA1,SP0 ;READ INCREMENTED BA
MICPC=MICPC+1
<MOVE!SPX!IBUS!IOBA1!SP0>

OUTPUT DP,<INCA!OBA1> ;WRITE INCREMENTED BA
MICPC=MICPC+1
<MOVE!WROUT!DP!<INCA!OBA1>>

C ICBA22 ;IF CARRY INC BA HIGH
MICPC=MICPC+1
<JUMP!CCOND!<ICBA22-INIT&3000*4>!<ICBA22-INIT&777/2>>

RK3: SP BR,DECA,SP4 ;DECREMENT THE COUNT OF BYTES
      MICPC=MICPC+1

```

(1)	013470	063164	<MOVE!SPX!BR!DECA!SP4>	
(1)				
1140	013472		C RK6	;NO OVERFLOW
(1)		000642	MICPC=MICPC+1	
(1)	013472	105245	<JUMP!CCOND!<RK6-INIT&3000*4>!<RK6-INIT&777/2>>	
(1)				
1141	013474		SP BR,DECA,SP5	;DECREMENT HIGH BYTE OF COUNT
(1)		000643	MICPC=MICPC+1	
(1)	013474	063165	<MOVE!SPX!BR!DECA!SP5>	
(1)				
1142	013476		Z RL4	;BYTE COUNT ZERO
(1)		000644	MICPC=MICPC+1	
(1)	013476	111772	<JUMP!ZCOND!<RL4-INIT&3000*4>!<RL4-INIT&777/2>>	
(1)				
1143		001	.IF NDF \$LOW	
1144	013500		RK6: BRWRT IBUS,RCVCON	;READ RECEIVER CONTROL REGISTER
(1)		000645	MICPC=MICPC+1	
(1)	013500	020640	<MOVE!WRTBR!IBUS!<RCVCON>>	
(1)				
1145	013502		BR4 RCVK0	;IF ANOTHER CHARACTER--PROCESS
(1)		000646	MICPC=MICPC+1	
(1)	013502	107215	<JUMP!BR4CON!<RCVK0-INIT&3000*4>!<RCVK0-INIT&777/2>>	
(1)				
1146	013504		RK66: STATE RCVK0	
(1)		000647	MICPC=MICPC+1	
(1)	013504	000615	<MOVE!WRTBR!IMM!<RCVK0-INIT&777/2>>	
1147	013506		ALWAYS REXIT	
(1)		000650	MICPC=MICPC+1	
(1)	013506	100450	<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>	
(1)				
1148	013510		RK4: BR0 IDLE	
(1)		000651	MICPC=MICPC+1	
(1)	013510	102051	<JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				
1149	013512		ALWAYS RK5	;IF NO NPR --PROCESS
(1)		000652	MICPC=MICPC+1	
(1)	013512	104627	<JUMP!ALCOND!<RK5-INIT&3000*4>!<RK5-INIT&777/2>>	
(1)				
1150		000	.ENDC	
1151		001	.IF DF \$LOW	
1152			RK6: STATE RCVK0	
1153			ALWAYS REXIT	
1154		000	.ENDC	
1155				
1156	013514		RKE1: SP IBUS,NPR,SPO	;READ NPR REGISTER
(1)		000653	MICPC=MICPC+1	
(1)	013514	123200	<MOVE!SPX!IBUS!NPR!SPO>	
(1)				
1157		001	.IF NDF \$LOW	
1158	013516		BR0 IDLE	;NPR STILL IN PROGRESS
(1)		000654	MICPC=MICPC+1	
(1)	013516	102051	<JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>	
(1)				
1159		000	.ENDC	
1160	013520		BRWRT IMM,177	;MASK FOR ALL BUT CO
(1)		000655	MICPC=MICPC+1	

M09

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RCVKE--HANDLE EVEN BYTES

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(1) 013520 000577      <MOVE!WRTEBR!IMM!<177>>
(1)
1161 013522      OUT      BR,<AANDB!ONPR>      ;TURN OFF ALL BUT CO
(1) 000656      MICPC=MICPC+1
(1) 013522 061270      <MOVE!WROUTX!BR!<AANDB!ONPR>>
(1)
1162 013524      ALWAYS  RK50
(1) 000657      MICPC=MICPC+1
(1) 013524 104631      <JUMP!ALCOND!<RK50-INIT&3000*4>!<RK50-INIT&777/2>>
(1)
1163      ;*****END OF TIME CRITICAL PATH*****
1164
1165 013526      RCVKEO: SP      IBUS,RCVDAT,SPO      ;READ CHARACTER AND SAVE IN SPO
(1) 000660      MICPC=MICPC+1
(1) 013526 023200      <MOVE!SPX!IBUS!RCVDAT!SPO>
(1)
1166 013530      OUTPUT  BR,<SELA!OUTDA1>      ;SEND NONSENSE CHARACTER
(1) 000661      MICPC=MICPC+1
(1) 013530 062202      <MOVE!WROUT!BR!<SELA!OUTDA1>>
(1)
1167 013532      BRWRT  BR,SELA!SP1      ;READ STATUS BYTE
(1) 000662      MICPC=MICPC+1
(1) 013532 060601      <MOVE!WRTEBR!BR!<SELA!SP1>>
(1)
1168 013534      BR7      PASWRD      ;MAINT MODE - SEE IF RLD MESSAGE
(1) 000663      MICPC=MICPC+1
(1) 013534 117576      <JUMP!BR7CON!<PASWRD-INIT&3000*4>!<PASWRD-INIT&777/2>>
(1)
1169 013536      ALWAYS  RK3      ;OTHERWISE PROCESS NORMALLY
(1) 000664      MICPC=MICPC+1
(1) 013536 104641      <JUMP!ALCOND!<RK3-INIT&3000*4>!<RK3-INIT&777/2>>
(1)

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N09

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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RCVI--STORE UNNUMBERED MESSAGE TYPE

PAGE: 0117

1171
1172 013540
(1) 000665
(1) 013540 023213
(1)
1173 013542
(1) 000666
(1) 013542 000670
1174 013544
(1) 000667
(1) 013544 100450
(1)
1175

RCVI: .SBTTL RCVI--STORE UNNUMBERED MESSAGE TYPE
SP IBUS,RCVDAT,SP13 ;STORE UNNUMBERED TYPE
MICPC=MICPC+1
<MOVE!SPX!IBUS!RCVDAT!SP13>

STATE RCVJ ;NEXT STATE IS J
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RCVJ-INIT&777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

;

1177
1178 013546
1179 001
1180
1181 000
1182 001
1183 013546
(1) 000670
(1) 013546 023205
(1)
1184 013550
(1) 000671
(1) 013550 000600
(1)
1185 013552
(1) 000672
(1) 013552 060665
(1)
1186 013554
(1) 000673
(1) 013554 063310
(1)
1187 000
1188 013556
(1) 000674
(1) 013556 000676
1189 013560
(1) 000675
(1) 013560 100450
(1)

RCVJ: .SBTTL RCVJ--ROUTINE TO HANDLE SUBTYPE FIELD, SELECT AND FINAL
.IF DF \$LOW
ALWAYS SELQSY ;"CALL" SELECT AND QSYNC SUBROUTINE
.ENDC
.IF NOF \$LOW
SP IBUS, RCV DAT, SP5 ;GET CHARACTER
MICPC=MICPC+1
<MOVE!SPX!IBUS!RCV DAT!SP5>

BRWRT IMM, 200 ;CONDITIONALLY SET BIT
MICPC=MICPC+1
<MOVE!WRT EBR!IMM!<200>>

BRWRT BR, AANDB!SP5
MICPC=MICPC+1
<MOVE!WRT EBR!BR!<AANDB!SP5>>

SP BR, AORB, SP10
MICPC=MICPC+1
<MOVE!SPX!BR!AORB!SP10>

.ENDC
STATE RCVR ;NEXT STATE IS N
MICPC=MICPC+1
<MOVE!WRT EBR!IMM!<RCVR-INIT&777/2>>
ALWAYS REXIT
MICPC=MICPC+1
<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

C10

```

1191 .SBTTL RCVR--UNNUMBERED MESSAGE RESPONSE FIELD
1192 ;ENTERED FROM IDLE LOOP
1193
1194 RCVR: BRWRT IMM,3 ;REP MESSAGE TYPE TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<3>>
      (1) 013562 000676
      (1) 013562 000403
      (1)
1195 NOP BR,SUB,SP13 ;IS TYPE ACK OR NAK
      MICPC=MICPC+1
      <BR!SUB!SP13>
      (1) 013564 000677
      (1) 013564 060353
      (1)
1196 STATE RCVQ ;NEXT STATE IS RCVQ
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<RCVQ-INIT&777/2>>
      (1) 013566 000700
      (1) 013566 000703
1197 ;***NOTE THIS INSTR DOES NOT CLOCK "C"
1198 C RCVF1 ;IF NOT IGNORE
      MICPC=MICPC+1
      <JUMP!CCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>
      (1) 013570 000701
      (1) 013570 105131
      (1)
1199 ALWAYS RD2 ;DO RANGE CHECKS
      MICPC=MICPC+1
      <JUMP!ALCOND!<RD2-INIT&3000*4>!<RD2-INIT&777/2>>
      (1) 013572 000702
      (1) 013572 104473
      (1)

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D10

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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RCVQ--UNNUMBERED MESSAGE--NUMBER FIELD

PAGE: 0120

1201
1202
1203
1204 013574 000703
(1) 013574 000525
1205 013576 000704
(1) 013576 104531
(1)
(1)

.SBTTL RCVQ--UNNUMBERED MESSAGE--NUMBER FIELD
:ENTER FROM IDLE
RCVQ: STATE RCVF ;NEXT STATE IS ADDRESS
MICPC=MICPC+1
<MOVE!WRITEBR!IMM!<RCVF-INIT&777/2>>
ALWAYS RCVF1
MICPC=MICPC+1
<JUMP!ALCOND!<RCVF1-INIT&3000*4>!<RCVF1-INIT&777/2>>

1207		
1208		
1209	013600	
(1)		000705
(1)	013600	123600
(1)		
1210		001
1211	013602	
(1)		000705
(1)	013602	107314
(1)		
1212		000
1213		001
1214		
1215		000
1216	013604	
(1)		000707
(1)	013604	000576
(1)		
1217	013606	
(1)		000710
(1)	013606	061270
(1)		
1218		
1219	013610	
(1)		000711
(1)	013610	020200
(1)		
1220	013612	
(1)		000712
(1)	013612	000715
1221	013614	
(1)		000713
(1)	013614	100450
(1)		
1222		
1223		001
1224	013616	
(1)		000714
(1)	013616	102051
(1)		
1225	013620	
(1)		000715
(1)	013620	104707
(1)		
1226		000
1227		

```

.SBTTL  RCVL--PROCESS CRC3
;ENTERED FROM  IDLE LOOP
RCVL:  SPBR      IBUS,NPR,SPO                ;READ NPR CONTROL
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!NPR!SPO>

      .IF NDF $LOW
BR4      RL1                                ;RCV NPR BRANCH
MICPC=MICPC+1
<JUMP!BR4CON!<RL1-INIT&3000*4>!<RL1-INIT&777/2>>

      .ENDC
      .IF DF  $LOW
BR0      IDLE
      .ENDC
RL2:  BRWRT  IMM 176                        ;MASK TO TURN OFF CO
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<176>>

      OUT      BR,AANDB!ONPR
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AANDB!ONPR>>

RL3:  ;
NOP      IBUS,RCV DAT,0                    ;INPUT CHARACTER AND DISCARD
MICPC=MICPC+1
<IBUS!RCV DAT!0>

STATE  RCVM
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<RCVM-INIT&777/2>>
ALWAYS  REXIT
MICPC=MICPC+1
<JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

      ;
RL1:  .IF NDF $LOW
BR0      IDLE                            ;NPR GOING --GET OUT
MICPC=MICPC+1
<JUMP!BR0CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

ALWAYS  RL2
MICPC=MICPC+1
<JUMP!ALCOND!<RL2-INIT&3000*4>!<RL2-INIT&777/2>>

      .ENDC
      ;

```

1229			SBTTL RCVM--PROCESS CRC4--END OF DATA MESSAGE	
1230			;ENTERED FROM IDLE LOOP	
1231			;IF CRC CORRECT -- QUEUE INTERRUPT AND UPDATE RESPONSE	
1232			;IF CRC WRONG SEND NAK	
1233			RCVM: BRWRT IBUS,UBBR	;READ UNIBUS BR REGISTER
1234	013622	000716	MICPC=MICPC+1	
(1)	013622	120620	<MOVE!WRTBR!IBUS!<UBBR>>	
(1)				
1235	013624	000717	BR0 NXMERR	;NON-EXISTANT MEMCR
(1)	013624	136351	MICPC=MICPC+1	
(1)			<JUMP!BR0CON!<NXMERR-INIT\$3000*4>!<NXMERR-INIT\$777/2>>	
(1)				
1236	013626	000720	SP IBUS,RCVDAT,SP0	;READ CRC CHARACTER
(1)	013626	023200	MICPC=MICPC+1	
(1)			<MOVE!SPX!IBUS!RCVDAT!SP0>	
(1)				
1237	013630	000721	BRWRT IBUS,RCVCON	;READ RECEIVER CONTROL REGISTER
(1)	013630	020640	MICPC=MICPC+1	
(1)			<MOVE!WRTBR!IBUS!<RCVCON>>	
(1)				
1238	013632	000722	BR0 RCVM1	;IF CRC GOOD -- PROCESS
(1)	013632	116214	MICPC=MICPC+1	
(1)			<JUMP!BR0CON!<RCVM1-INIT\$3000*4>!<RCVM1-INIT\$777/2>>	
(1)				
1239	013634	000723	BRWRT BR,SELA!SP1	;READ STATUS BYTE
(1)	013634	060601	MICPC=MICPC+1	
(1)			<MOVE!WRTBR!BR!<SELA!SP1>>	
(1)				
1240	013636	000724	BR7 RHX	;CRC ERROR IN BOOT MODE - FLUSH
(1)	013636	107740	MICPC=MICPC+1	
(1)			<JUMP!BR7CON!<RHX-INIT\$3000*4>!<RHX-INIT\$777/2>>	
(1)				
1241	013640	000725	LDMA IMM,T	;ELSE SEND NAK --DATA ERROR
(1)		001	MICPC=MICPC+1	
(1)	013640	010151	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<T\$377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<T>>	
(1)		000	.ENDC	
(1)				
1242	013642	000726	MEMINC IMM,2	;NAK TYPE
(1)	013642	016402	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IMM!<2>>	
(1)				
1243	013644	000727	MEMINC IMM,302	;DATA ERROR SUBTYPE
(1)	013644	016702	MICPC=MICPC+1	
(1)			<MOVE!WRMEM!INCMAR!IMM!<302>>	
(1)				
1244	013646	000730	LDMA IMM,NDATS	
(1)		001	MICPC=MICPC+1	
(1)	013646	010014	.IF IDN IMM,IMM	
(1)			<MOVE!LDMA!IMM!<NDATS\$377>>	
(1)			.IFF	
(1)			<MOVE!LDMA!IMM!<NDATS>>	
(1)		000	.ENDC	

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JMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-57
RCVM--PROCESS CRC4--END OF DATA MESSAGE

PAGE: 0123

(1)	1245	013650		ALWAYS RHS	;SEND NAK
(1)			000731	MICPC=MICPC+1	
(1)		013650	104552	<JUMP!ALCOND!<RHS-INIT\$3000*4>!<RHS-INIT\$777/2>>	
(1)					
(1)	1246				
(1)	1247	013652		RCVMO: LDMA IMM,<<RTHRS+3>>	;POINT TO ERROR WORD
(1)			000732	MICPC=MICPC+1	
(1)			001	.IF IDN IMM IMM	
(1)		013652	010177	<MOVE!LDMAR!IMM!<<RTHRS+3>>\$377>>	
(1)				.IFF	
(1)				<MOVE!LDMAR!IMM!<<RTHRS+3>>>	
(1)			000	.ENDC	
(1)					
(1)	1248	013654		BRWRT IMM,10	;MAINT MESSAGE ERROR
(1)			000733	MICPC=MICPC+1	
(1)		013654	000410	<MOVE!WRTBR!IMM!<10>>	
(1)					
(1)	1249	013656		ALWAYS RCEXY	;GIVE FATAL ERROR
(1)			000734	MICPC=MICPC+1	
(1)		013656	114522	<JUMP!ALCOND!<RCEXY-INIT\$3000*4>!<RCEXY-INIT\$777/2>>	
(1)					

1251			.SBTTL EM2--PROCESS RLD MESSAGE
1252			;ENTERED FROM IDLE LOOP
1253			;IF RLD PASSWORD CHECKS TRIGGER THE BCOT ROM
1254			
1255	013660		EM2: BRWRT IBUS,RCVDAT ;READ THE CHAR
(1)		000735	MICPC=MICPC+1
(1)	013660	020600	<MOVE!WRTBR!IBUS!<RCVDAT>>
(1)			
1256	013662		CMP BR,SP13 ;IS IT A MATCH
(1)		000736	MICPC=MICPC+1
(1)	013662	060373	<SUBTC!BR!SP13>
(1)			
1257	013664		Z EM3
(1)		000737	MICPC=MICPC+1
(1)	013664	105746	<JUMP!ZCOND!<EM3-INIT&3000*4>!<EM3-INIT&777/2>>
(1)			
1258			
1259	013666		RHX: BRWRT BR,AA!SP1 ;FALL INTO RHX
(1)		000740	MICPC=MICPC+1 ;READ STATUS BYTE SHIFTED LEFT
(1)	013666	060521	<MOVE!WRTBR!BR!<AA!SP1>>
(1)			
1260	013670		BR4 10\$;DLE RECEIVED IN NORMAL MODE
(1)		000741	MICPC=MICPC+1
(1)	013670	107343	<JUMP!BR4CON!<10\$-INIT&3000*4>!<10\$-INIT&777/2>>
(1)			
1261	013672		ALWAYS FLUSH ;ALREADY IN MAINT MODE
(1)		000742	MICPC=MICPC+1
(1)	013672	104415	<JUMP!ALCOND!<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>
(1)			
1262	013674		10\$: BRWRT IMM,163 ;MASK TO CLEAR ALL MAINT RELATED BITS
(1)		000743	MICPC=MICPC+1
(1)	013674	000563	<MOVE!WRTBR!IMM!<163>>
(1)			
1263	013676		SP BR,AANDB,SP1 ;CLEAR THEM
(1)		000744	MICPC=MICPC+1
(1)	013676	063261	<MOVE!SPX!BR!AANDB!SP1>
(1)			
1264	013700		ALWAYS FLUSH
(1)		000745	MICPC=MICPC+1
(1)	013700	104415	<JUMP!ALCOND!<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>
(1)			
1265			
1266	013702		EM3: SP BR,DECA,SP4 ;DECREMENT CHARACTER COUNT BY ONE
(1)		000746	MICPC=MICPC+1
(1)	013702	063164	<MOVE!SPX!BR!DECA!SP4>
(1)			
1267	013704		Z EMTRIG ;TRIGGER AC LOW
(1)		000747	MICPC=MICPC+1
(1)	013704	115712	<JUMP!ZCOND!<EMTRIG-INIT&3000*4>!<EMTRIG-INIT&777/2>>
(1)			
1268	013706		ALWAYS IDLE
(1)		000750	MICPC=MICPC+1
(1)	013706	100451	<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
(1)			

I10

1270 001
1271
1272 013710 000751
(1) 002
(1) 013710 010177
(1)
(1)
(1) 001
(1)
1273 013712 000752
(1) 016401
(1)
1274 013714 000753
(1) 002400
(1)
1275 013716 000754
(1) 043230
(1)
1276 013720 000755
(1) 114524
(1)

```
.IF NDF $LOW
.SBTTL NXMERR ---NON EXISTANT MEMORY HANDLER
NXMERR: LDMA IMM,<<RTHRS+3>> ;ADDRESS ERROR LINK
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMA!IMM!<<RTHRS+3>>377>>
.IFF
<MOVE!LDMA!IMM!<<RTHRS+3>>>
.ENDC

MEMINC IMM,1
MICPC=MICPC+1
<MOVE!WRMEM!INCMAR!IMM!<1>>

MEM IMM,0 ;NXM ERROR BIT
MICPC=MICPC+1
<MOVE!WRMEM!IMM!<0>>

SP MEMX,SELB,SP10 ;CLEAR STATUS
MICPC=MICPC+1
<MOVE!SPX!MEMX!SELB!SP10>

ALWAYS RCXX
MICPC=MICPC+1
<JUMP!ALCOND!<RCXX-INIT$3000*4 !RCXX-INIT$777.2>>
```

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1278          00C
1279          001
1280
1281          .ENDC
1282          .IF OF SLOW
1283          .SBTTL SELQSY--ROUTINETOCHECK SELECT AND QSYNC AND DIDDLE LINE STATUS WORD
1284          .USES SP5, ALWAYS CALLED BY FIRST INSTR IN A RSTATE
1285          SELQSY: SPBR IBUS,RCV DAT,SP5 ;READ CHARACTER INTO SP5 AND THE BR
1286          BR7 15$ ;SELECT SET?--BRANCH
1287          5$: BRWRT BR,AA!SP5 ;SHIFTBR LEFT
1288          BR7 20$ ;FINAL SET?
1289          10$: BRWRT IMM,77 ;MASK TO BR
1290          SP BR,ANDB,SP5 ;TURN OFF SELECTANDFINAL
1291          .ALWAY BR,INCA,SP3!PAGE1
1292
1293          15$: BRWRT IMM,200 ;SET OK TO SEND
1294          SP BR,AORB,SP10 ;IN LINE STATUS WORD
1295          ALWAYS 5$
1296          20$: BRWRT IMM,20 ;SETCLEARACTIVE
1297          SP BR,AORB,SP10 ;IN LINE STATUS WORD
1298          ALWAYS 10$
1299          .PAGE
1300          .ENDC
1301          000
1302          013722 000756
1303          (1) 013722 060601
1304          (1)
1305          013724 BR7 RA3 ;BRANCH IF SO AND TREAT DLE LIKE NUM. MSG.
1306          (1) MICPC=MICPC+1
1307          (1) 013724 103742 <JUMP!BR7CON!<RA3-INIT&3000*4>!<RA3-INIT&777/2>>
1308          (1)
1309          013726 BRWRT IMM,210 ;MASK TO SET MAINT MODE AND DLE RECV'D
1310          (1) MICPC=MICPC+1
1311          (1) 013726 000760 <MOVE!WRTBR!IMM!<210>>
1312          (1)
1313          013730 SP BR,AORB,SP1 ;SET THE BITS
1314          (1) MICPC=MICPC+1
1315          (1) 013730 063301 <MOVE!SPX!BR!AORB!SP1>
1316          (1)
1317          013732 ALWAYS RA3 ;TREAT LIKE NUMBERED MESSAGE
1318          (1) MICPC=MICPC+1
1319          (1) 013732 100742 <JUMP!ALCOND!<RA3-INIT&3000*4>!<RA3-INIT&777/2>>
1320          (1)
1321          013734 RESEXT: BRWRT IMM,4 ;ADD TO MXT BITS
1322          (1) MICPC=MICPC+1
1323          (1) 013734 000404 <MOVE!WRTBR!IMM!<4>>
1324          (1)
1325          013736 SP BR,ADD,SP0
1326          (1) MICPC=MICPC+1
1327          (1) 013736 063000 <MOVE!SPX!BR!ADD!SP0>
1328          (1)
1329          013740 ALWAYS TH3X
1330          (1) MICPC=MICPC+1
1331          (1) 013740 110601 <JUMP!ALCOND!<TH3X-INIT&3000*4>!<TH3X-INIT&777/2>>
1332          (1)
1333          013742 TABMXT: BRWRT IMM,4 ;INCREMENT MXT
1334          (1) MICPC=MICPC+1
1335          (1) 013742 000404 <MOVE!WRTBR!IMM!<4>>

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-61
NXMERR ---NON EXISTANT MEMORY HANDLER

PAGE: 0127

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(1)
1308 013744      SP      IBUS,UBBR,SPO      ;READ BR CONTROL
(1)              MICPC=MICPC+1
(1) 013744      123220      <MOVE!SPX!IBUS!UBBR!SPO>
(1)
1309 013746      OUT      BR,ADD!OBR
(1)              MICPC=MICPC+1
(1) 013746      061011      <MOVE!WROUTX!BR!<ADD!OBR>>
(1)
1310 013750      ALWAYS   ECX
(1)              MICPC=MICPC+1
(1) 013750      114761      <JUMP!ALCOND!<ECX-INIT&3000*4>!<ECX-INIT&777/2>>
(1)
1311
1312 013752      ;ATHRES: BRWRT IMM,2
(1)              MICPC=MICPC+1
(1) 013752      000772      <MOVE!WRTEBR!IMM!<2>>
(1) 013752      000402
(1)
1313 013754      ALWAYS   ERRXX
(1)              MICPC=MICPC+1
(1) 013754      114663      <JUMP!ALCOND!<ERRXX-INIT&3000*4>!<ERRXX-INIT&777/2>>
(1)
1314              000004      .REPT      4
1315              $ZERO
1316              .ENDR
(1) 013756      $ZERO
(2)              MICPC=MICPC+1
(2) 013756      000000      000000
(2)
(1) 013760      $ZERO
(2)              MICPC=MICPC+1
(2) 013760      000775      000000
(2)
(1) 013762      $ZERO
(2)              MICPC=MICPC+1
(2) 013762      000776      000000
(2)
(1) 013764      $ZERO
(2)              MICPC=MICPC+1
(2) 013764      000777      000000
(2)

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DMC11 CDCMP PROTOCOL IMPLEMENTATION
DCCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-62
NXMERR ---NON EXISTANT MEMORY HANDLER

PAGE: 0128

1318 013766
1319 000777
1320
1321
1322 013766 001000
(1) 013766 020620
(1)
(1)
1323 013770 001001
(1) 013770 173202
(1)
(1)
1324 013772 001002
(1) 013772 100454
(1)
(1)

. = INIT+2000
MICPC=777
.SBTTL TMTDA--TRANSMITTER DISPATCH ROUTINE
:
TMTDA: BRWRT IBUS,TMTCON ;READ TRANSMITTER CONTROL REGISTER
MICPC=MICPC+1
<MOVE!WRTBR!IBUS!<TMTCON>>

.BR4 DP,SELA,<2!PAGE2> ;IF READY PROCEED
MICPC=MICPC+1
<JUMP! BR4CON!DP!SELA!2!PAGE2>

ALWAYS I1 ;ELSE IDLE
MICPC=MICPC+1
<JUMP!ALCOND! (I1-INIT&3000*4)!<I1-INIT&777/2>>

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-63
TMTA--FIRST CHARACTER OF HEADER

PAGE: 0129

1326			.SBTTL TMTA--FIRST CHARACTER OF HEADER
1327			;
1328	013774		TMTA:
1329		001	.IF DF \$LOW
1330			BRWRT BR,AA!SP10 ;SHIFT LEFT
1331			BR7 RCVCK
1332			TA1:
1333		000	.ENDC
1334	013774		BRWRT BR,SELA!SP10 ;REREAD STATUS
(1)		001003	MICPC=MICPC+1
(1)	013774	060610	<MOVE!WRTBR!BR!<SELA!SP10>>
(1)			
1335	013776		BR0 NUMSYN ;IF UNNUMBPENDING -- SEND IT
(1)		001004	MICPC=MICPC+1
(1)	013776	112007	<JUMP!BR0CON!<NUMSYN-INIT&3000*4>!<NUMSYN-INIT&777/2>>
(1)			
1336	014000		BRSHFT
(1)		001005	MICPC=MICPC+1
(1)	014000	001620	<MOVE!SHFTBR!WRTBR!SELB>
(1)			
1337	014002		BR4 IDLE0 ;IF START MODE--EXIT
(1)		001006	MICPC=MICPC+1
(1)	014002	103063	<JUMP!BR4CON!<IDLE0-INIT&3000*4>!<IDLE0-INIT&777/2>>
(1)			
1338		001	.IF DF \$LOW
1339			BR1 NUMSYN ;IF LINE HAS GONE IDLE SEND SYN
1340			;ELSE--START TO SEND MESSAGE
1341		000	.ENDC
1342		001	.IF NDF \$LOW
1343	014004		NUMSYN: BRWRT BR,<SELA!SP10> ;READ LINE STATUS WORD
(1)		001007	MICPC=MICPC+1
(1)	014004	060610	<MOVE!WRTBR!BR!<SELA!SP10>>
(1)			
1344	014006		BR7 5\$;IF OK TO SEND--PROCEED
(1)		001010	MICPC=MICPC+1
(1)	014006	113412	<JUMP!BR7CON!<5\$-INIT&3000*4>!<5\$-INIT&777/2>>
(1)			
1345	014010		ALWAYS I1 ;ELSE--IDLE
(1)		001011	MICPC=MICPC+1
(1)	014010	100454	<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
(1)			
1346	014012		5\$: BRWRT IBUS,MODEM ;ARE WE STILL SENDING?
(1)		001012	MICPC=MICPC+1
(1)	014012	020660	<MOVE!WRTBR!IBUS!<MODEM>>
(1)			
1347	014014		BRSHFT
(1)		001013	MICPC=MICPC+1
(1)	014014	001620	<MOVE!SHFTBR!WRTBR!SELB>
(1)			
1348	014016		BR4 I1 ;RTS SET? IF SO WE ARE--STALL
(1)		001014	MICPC=MICPC+1
(1)	014016	103054	<JUMP!BR4CON!<I1-INIT&3000*4>!<I1-INIT&777/2>>
(1)			
1349	014020		BRWRT IMM,373 ;MASK TO TURN OFFLINE IDLE
(1)		001015	MICPC=MICPC+1
(1)	014020	000773	<MOVE!WRTBR!IMM!<373>>

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 6-64
TMTA--FIRST CHARACTER OF HEADER

PAGE: 0130

(1)	1350	014022	001016	SP BR, AANDB, SP10	; IN LINE STATUS WORD
(1)	(1)	014022	063270	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!SPX!BP!AANDB!SP10>	
(1)	1351	014024	001017	TSTATE TMTA1	
(1)	(1)	014024	000424	MICPC=MICPC+1	
(1)	(1)	(1)	001020	<MOVE!WRTEBR!IMM!<TMTA1-INIT&777/2>>	
(1)	(1)	014026	063222	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!SPX!BR!SELB!SP2>	
(1)	1352	014030	001021	BRWRT IMM, 12	
(1)	(1)	014030	000412	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!WRTEBR!IMM!<12>>	
(1)	1353	014032	001022	SP BR, SELB, SP6	; STORE IN SP6
(1)	(1)	014032	063226	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!SPX!BR!SELB!SP6>	
(1)	1354	014034	001023	ALWAYS I1	; BACK TO IDLE LOOP
(1)	(1)	014034	100454	MICPC=MICPC+1	
(1)	(1)	(1)		<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>	
(1)	1355	014036	001024	TMTA1: SP BR, DECA, SP6	; DECREMENT SYN COUNT
(1)	(1)	014036	063166	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!SPX!BR!DECA!SP6>	
(1)	1356	014040	001025	Z TMTTEXT	
(1)	(1)	014040	111432	MICPC=MICPC+1	
(1)	(1)	(1)		<JUMP!ZCOND!<TMTTEXT-INIT&3000*4>!<TMTTEXT-INIT&777/2>>	
(1)	1357	014042	001026	OUTPUT IMM, <1!OTMTCO>	; WRITE SOM TO TMTR CNTRL
(1)	(1)	014042	002011	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!WROUT!IMM!<1!OTMTCO>>	
(1)	1358	014044	001027	BRWRT IMM, 226	; SYNC CHAR
(1)	(1)	014044	000626	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!WRTEBR!IMM!<226>>	
(1)	1359	014046	001030	OUTPUT BR, <SELB!TMTDAT>	; SEND THE CHARACTER
(1)	(1)	014046	062230	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!WROUT!BR!<SELB!TMTDAT>>	
(1)	1360	014050	001031	ALWAYS I1	
(1)	(1)	014050	100454	MICPC=MICPC+1	
(1)	(1)	(1)		<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>	
(1)	1361		000	.ENDC	
(1)	1362	014052	001032	TMTTEXT: BRWRT BR, <SELA!SP10>	; UNNUMB MESSGE?
(1)	(1)	014052	060610	MICPC=MICPC+1	
(1)	(1)	(1)		<MOVE!WRTEBR!BR!<SELA!SP10>>	
(1)	1363	014054	001033	BRO TMTUN	; IF SO --BRANCH
(1)	(1)	014054	112043	MICPC=MICPC+1	
(1)	(1)	(1)		<JUMP!BROCON!<TMTUN-INIT&3000*4>!<TMTUN-INIT&777/2>>	
(1)	1364	014056		TSTATE TMTB	

B11

(1) 001034
(1) 014056 000451
(1) 001035
(1) 014060 063222
1365 014062 001036
(1) 060601
(1) 014062 060601
(1) 014064 001037
(1) 113447
(1) 014066 001040
(1) 000601
(1) 014070 001041
(1) 062230
(1) 014072 001042
(1) 100454
(1) 014074 001043
(1) 000610
(1) 001044
(1) 014076 063222
1371 014100 001045
(1) 000405
(1) 014102 001046
(1) 110441
(1) 014104 001047
(1) 000620
(1) 014106 001050
(1) 110441
(1) 001
1375
1376
1377
1378
1379
1380
1381

MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTB-INIT&777/2>>
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>
BRWRT BR SELA!SP1 ;ARE WE IN BOOT MODE
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<SELA!SP1>>

BR7 TMTBT ;IF SO SEND DLE
MICPC=MICPC+1
<JUMP!BR7CON!<TMTBT-INIT&3000*4>!<TMTBT-INIT&777/2>>

BRWRT IMM,201 ;ELSE STORE SOH
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<201>>

TMTAS: OUTPUT BR,<SELB!TMTDAT> ;IN TMT SILO
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!TMTDAT>>

ALWAYS I1
MICPC=MICPC+1
<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>

TMTUN: TSTATE TMTI
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTI-INIT&777/2>>
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>
BRWRT IMM,5 ;END TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<5>>

ALWAYS TMTAS
MICPC=MICPC+1
<JUMP!ALCOND!<TMTAS-INIT&3000*4>!<TMTAS-INIT&777/2>>

TMTBT: BRWRT IMM,220 ;WRITE A DLE TO BR
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<220>>

ALWAYS TMTAS ;SEND IT
MICPC=MICPC+1
<JUMP!ALCOND!<TMTAS-INIT&3000*4>!<TMTAS-INIT&777/2>>

.IF DF \$LOW

NUMSYN: BRWRT BR,<SELA!SP10> ;READ LINE STATUS WORD
BR7 \$S ;IF OK TO SEND--PROCEED
ALWAYS I1 ;ELSE--IDLE
\$S: BRWRT IBUS,MODEM ;ARE WE STILL SENDING?
BRSHFT

C11

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

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TMTA--FIRST CHARACTER OF HEADER

PAGE: 0132

1383
1384
1385
1386
1387

BR4 I1
BRWRT IMM,373
SP BR, AANDB, SP10
TSTATE TMTA1
BRWRT IMM,10

;RTS SET? IF SO WE ARE--STALL
;MASK TO TURN OFFLINE IDLE
;IN LINE STATUS WORD

DMC11 DDCMP PROTOCOL IMPLEMENTATION
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D11

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8
TMTA--FIRST CHARACTER OF HEADER

PAGE: 0133

1389
1390
1391
1392
1393
1394
1395

000

TMTA1: SP BR,SELB,SP6
SP BR,DECA,SP6
Z TMTEXT
OUTPUT IMM,<1!OTMTCO>
BRWRT IMM,226
ALWAYS TMTA5
.ENDC

;STORE IN SP6
;DECREMENT SYN COUNT
;WRITE SOM TO TMTR CONTRL
;SYNC CHAR

```

1397
1398
1399 014110 001051
      (1)    001
      (1)
      (1)
      (1)
      (1)
      (1) 014110 070216
      (1)    000
      (1)
1400 014112 001052
      (1)    016403
      (1)
1401 014114 001053
      (1)    076612
      (1)
1402 014116 001054
      (1)    000476
      (1) 014116 000476
1403 014120 001055
      (1)    063222
      (1)
1404 014122 001056
      (1)    056224
      (1)
1405 014124 001057
      (1)    056225
      (1)
1406 014126 001060
      (1)    043227
      (1)
1407
1408 014130 001061
      (1)    123200
      (1)
1409 014132 001062
      (1)    000620
      (1)
1410 014134 001063
      (1)    063260
      (1)
1411 014136 001064
      (1)    003306
      (1)
1412 014140 001065
      (1)

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      .SBTTL TMTB--OUTPUT FIRST CHAR OF COUNT
TMTB:  LDMA BR, SELA!SP16 ;GETPOINTER TO NEXT TMT LINK
      MICPC=MICPC+1
      .IF IDN BR, IMM
      <MOVE!LDMAR!IMM!<SELA!SP16$377>>
      .IFF
      <MOVE!LDMAR!BR!<SELA!SP16>>
      .ENDC

      MEMINC IMM, 3 ;WRITE MSG TMTD TO FLAGS
      MICPC=MICPC+1
      <MOVE!WRMEM!INCMAR!IMM!<3>>

      MEMINC BR, SELA!SP12 ;PICK UP MSGNO
      MICPC=MICPC+1
      <MOVE!WRMEM!INCMAR!BR!<SELA!SP12>>

      STATE TMTC ;ADDRESS TMTR STATE
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TMTC-INIT$777/2>>
TBO:  SP BR, SELB, SP2 ;UPDATE IT
      MICPC=MICPC+1
      <MOVE!SPX!BR!SELB!SP2>

      OUTPUT <MEMX!INCMAR>, SELB!IBA1 ;WRITE LOW BYTE OF ADDRESS
      MICPC=MICPC+1
      <MOVE!WROUT!MEMX!INCMAR!<SELB!IBA1>>

      OUTPUT <MEMX!INCMAR>, SELB!IBA2 ;WRITE HIGH BYTE OF ADDRESS
      MICPC=MICPC+1
      <MOVE!WROUT!MEMX!INCMAR!<SELB!IBA2>>

      SP MEMX, SELB, SP7 ;HIGH BYTE OF COUNT TO SP7
      MICPC=MICPC+1
      <MOVE!SPX!MEMX!SELB!SP7>

      ;WAIT TO MASK OFF MEM EXT. BITS
      SP IBUS, NPR, SP0
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!NPR!SP0>

      BRWRT IMM, 220
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<220>>

      SP BR, AANDB, SP0
      MICPC=MICPC+1
      <MOVE!SPX!BR!AANDB!SP0>

      SP IMM, 300, SP6 ;MASK FOR MXT
      MICPC=MICPC+1
      <MOVE!SPX!IMM!300!SP6>

      BRWRT MEMX!INCMAR, AANDB!SP6 ;TURN OFF CC2
      MICPC=MICPC+1

```

```

(1) 014140 054666      <MOVE!WRTEBR!MEMX!INCMAR!<AANDB!SP6>>
(1)
1413 014142      OUTPUT MEMX,SELB!TMTDAT      :ALSO WRITE COUNT TO TMTR SILC
(1) 001066      MICPC=MICPC+1
(1) 014142 042230      <MOVE!WROUT!MEMX!<SELB!TMTDAT>>
(1)
1414 014144      BRSHFT      :SHIFT BITS INTO CORRECT POSITION
(1) 001067      MICPC=MICPC+1
(1) 014144 001620      <MOVE!SHFTBR!WRTEBR!SELB>
(1)
1415 014146      BRSHFT
(1) 001070      MICPC=MICPC+1
(1) 014146 001620      <MOVE!SHFTBR!WRTEBR!SELB>
(1)
1416 014150      BRSHFT
(1) 001071      MICPC=MICPC+1
(1) 014150 001620      <MOVE!SHFTBR!WRTEBR!SELB>
(1)
1417 014152      BRSHFT
(1) 001072      MICPC=MICPC+1
(1) 014152 001620      <MOVE!SHFTBR!WRTEBR!SELB>
(1)
1418 014154      OUT      BR,AORB!ONPR
(1) 001073      MICPC=MICPC+1
(1) 014154 061310      <MOVE!WROUTX!BR!<AORB!ONPR>>
(1)
1419 014156      SPBR      MEMX,SELB,SP6      :LOWBYTE OF COUNT TO SP6
(1) 001074      MICPC=MICPC+1
(1) 014156 043626      <MOVE!SPBRX!MEMX!SELB!SP6>
(1)
1420      001      .IF DF $LOW      ;*****10/21/76
1421      ALWAYS IDLE
1422      000      .ENDC
1423      001      .IF NDF $LOW      ;*****10/21/76
1424 014160      ALWAYS I1
(1) 001075      MICPC=MICPC+1
(1) 014160 100454      <JUMP!ALCOND!<I1-INIT33000*4>!<I1-INIT3777*2>>
(1)
1425      000      .ENDC
1426      :

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1428
1429
1430 014162 001076
1431 014162 000477
1432 014164 001077
1433 014164 063667
1434 014166 001100
1435 014166 062230
1436 014170 001101
1437 014170 000543
1438 014172 001102
1439 014172 060376
1440 014174 001103
1441 014174 111511
1442 014176 001104
1443 014176 000406
1444 014200 001105
1445 014200 063016
1446 014202 001
1447 014202 000
1448 014202 001
1449 014202 001106
1450 014202 000514
1451 014202 001107
1452 014204 063222
1453 014206 001110
1454 014206 100454
1455 014210 000
1456 014210 001111
1457 014210 000471
1458 014212 001112

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.SBTTL TMTD--OUTPUT SECOND CHAR OF COUNT
TMTD: BRWRT IMM,77 ;MASK TO CLEAR MXT BITS
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<77>>

      SPBR BR,AANDB,SP7 ;CLEAR THEM
      MICPC=MICPC+1
      <MOVE!SPBRX!BR!AANDB!SP7>

      OUTPUT DP,<SELB!TMTDAT> ;WRITE TO TMT SILO
      MICPC=MICPC+1
      <MOVE!WROUT!DP!<SELB!TMTDAT>>

      BRWRT IMM,TML8 ;GET WRAPAROUND ADDRESS
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<TML8>>

      CMP BR,SP16 ;WRAPAROUND
      MICPC=MICPC+1
      <SUBTC!BR!SP16>

      Z 105
      MICPC=MICPC+1
      <JUMP!ZCOND!<105-INIT$3000*4>!<105-INIT$777/2>>

      BRWRT IMM,6 ;OFFSET TO NEXT LINK
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<6>>

      SP BR,ADD,SP16 ;UPDATE THE POINTER
      MICPC=MICPC+1
      <MOVE!SPX!BR!ADD!SP16>

SS: .IF DF SLOW
     STATE TMTD
     ALWAYS XEXIT
     .ENDC
     .IF NDF SLOW
     TSTATE TMTD
     MICPC=MICPC+1
     <MOVE!WRTBR!IMM!<TMTD-INIT$777/2>>
     MICPC=MICPC+1
     <MOVE!SPX!BR!SELB!SP2>
     ALWAYS I1 ;***OCTOBER 29, 1976
     MICPC=MICPC+1
     <JUMP!ALCOND!<I1-INIT$3000*4>!<I1-INIT$777/2>>

     .ENDC
105: BRWRT IMM,TML1 ;GO BACK TO FIRST LINK
     MICPC=MICPC+1
     <MOVE!WRTBR!IMM!<TML1>>

     SP BR,SELB,SP16
     MICPC=MICPC+1

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H11

SMC:1 DDMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

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TMTG--OUTPUT SECOND CHAR OF COUNT

PAGE: 0137

(1) 014212 063236
(2) 014214
(3) 001113
(4) 014214 1:0506
(5) 1450

<MOVE!SPX!BR!SELB!SP16>

ALWAYS SS
MICPC=MICPC+1
<JUMP!ALCOND!<SS-INIT\$3000*4>!<SS-INIT\$777/2>>

:

1452
1453 014216 001114
(1) 014216 000524
1454 014220 001115
(1) 014220 063166
(1)
1455 014222
(1) 014222 001116
(1) 014222 111120
(1)
1456 014224
(1) 014224 001117
(1) 014224 063167
(1)
1457 014226
(1) 014226 001120
(1) 014226 001
(1) 014226 010171
(1)
(1) 000
(1)
1458 014230
(1) 014230 001121
(1) 014230 042230
(1)
1459 014232
(1) 014232 001122
(1) 014232 063222
(1)
1460 014234
(1) 014234 001123
(1) 014234 100454
(1)

TMTD: .SBTTL TMTD--RESPONSE FIELD-NUMBERED MESSAGE
STATE TMTE
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTE-INIT&777/2>>
SP BR,DECA,SP6 ;ADJUST COUNT FOR TWO'S COMPLEMENT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP6>
C TD2 ;NO OVERFLOW
MICPC=MICPC+1
<JUMP!CCOND!<TD2-INIT&3000*4>!<TD2-INIT&777/2>>
SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP7>
TD2: LDMA IMM,ISP11 ;RESP FIELD ADDR TO MAR
MICPC=MICPC+1
.IF IDN IMM,IMM
<MOVE!LDMA!IMM!<ISP11&377>>
.IFF
<MOVE!LDMA!IMM!<ISP11>>
.ENDC
TD3: OUTPUT MEMX,SELB!TMTDAT ;WRITE IT TO SILO
MICPC=MICPC+1
<MOVE!WROUT!MEMX!<SELB!TMTDAT>>
XEXIT2: SP BR,SELB,SP2
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>
ALWAYS I1
MICPC=MICPC+1
<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>

1462
 1463 014236
 1464 014236
 (1) 001124
 (1) 014236 123600
 (1)
 1465 014240
 (1) 001125
 (1) 014240 102054
 (1)
 1466 014242
 (1) 001126
 (1) 014242 060612
 (1)
 1467 014244
 (1) 001127
 (1) 014244 062230
 (1)
 1468 014246
 (1) 001130
 (1) 014246 000532
 1469 014250
 (1) 001131
 (1) 014250 110600
 (1)

.SBTTL TMTE--NUMBER FIELD--NUMBERED MESSAGE
 TMTE: SPBR IBUS,NPR,SPO ;READ NPR CONTROL REGISTER
 MICPC=MICPC+1
 <MOVE!SPBRX!IBUS!NPR!SPO>
 BR0 I1 ;BUSY - GET OUT
 MICPC=MICPC+1
 <JUMP!BROCON!<I1-INIT&3000*4>!<I1-INIT&777/2>>
 BRWRT BR,SELA!SP12
 MICPC=MICPC+1
 <MOVE!WRTBR!BR!<SELA!SP12>>
 OUTPUT BR,<SELB!TMTDAT> ;WRITE IT TO THE SILO
 MICPC=MICPC+1
 <MOVE!WROUT!BR!<SELB!TMTDAT>>
 STATE TMTF
 MICPC=MICPC+1
 <MOVE!WRTBR!IMM!<TMTF-INIT&777/2>>
 ALWAYS TH3
 MICPC=MICPC+1
 <JUMP!ALCOND!<TH3-INIT&3000*4>!<TH3-INIT&777/2>>

K11

DMC11 DDMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-7
TMTF--NUMBERED MSG ADDRESS FIELD

PAGE: 0140

1471
1472
1473 014252 001132
(1) 014252 000537
1474 014254 001133
(1) 014254 063222
(1)
1475 014256 001134
(1) 014256 000401
(1)
1476 001
1477 014260 001135
(1) 014260 062230
(1)
1478 014262 001136
(1) 014262 100454
(1)
1479 000
1480 001
1481
1482 000

.SBTTL TMTF--NUMBERED MSG ADDRESS FIELD
TMTF: STATE TF1
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TF1-INIT&777/2>>
TF2: SP BR SELB,SP2
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>

BRWRT IMM,1 ;LOAD ADDRESS
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<1>>

TF3: .IF NDF SLOW
OUTPUT BR,<SELB!TMTDAT>
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!TMTDAT>>

ALWAYS I1
MICPC=MICPC+1
<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>

.ENDC
.IF DF SLOW
ALWAYS TMTAS
.ENDC

L11

1484			.SBTTL TF1-NUMBERED MSG HEADER EOM	
1485	014264		TF1: BRWRT IMM,2	;EOM MASK TO BR
(1)		001137	MICPC=MICPC+1	
(1)	014264	000402	<MOVE!WRTEBR!IMM!<2>>	
(1)				
1486	014266		OUTPUT BR,<SELB!OTMTCO>	;UPDATE TMTR CONTROL REGISTER
(1)		001140	MICPC=MICPC+1	
(1)	014266	062231	<MOVE!WROUT!BR!<SELB!OTMTCO>>	
(1)				
1487	014270		OUTPUT BR,<SELB!TMTDAT>	;OUTPUT A GARBAGE CHAR
(1)		001141	MICPC=MICPC+1	
(1)	014270	062230	<MOVE!WROUT!BR!<SELB!TMTDAT>>	
(1)				
1488	014272		BRWRT IBUS,IIBA1	;READ LOW ORDER FROM INBA
(1)		001142	MICPC=MICPC+1	
(1)	014272	020500	<MOVE!WRTEBR!IBUS!<IIBA1>>	
(1)				
1489	014274		BRO TMTF1	;IF ODD BYTE--BRANCH
(1)		001143	MICPC=MICPC+1	
(1)	014274	112162	<JUMP!BROCON!<TMTF1-INIT&3000*4>!<TMTF1-INIT&777/2>>	
(1)				
1490	014276		STATE TMTH	
(1)		001144	MICPC=MICPC+1	
(1)	014276	000546	<MOVE!WRTEBR!IMM!<TMTH-INIT&777/2>>	
1491	014300		ALWAYS XEXIT	
(1)		001145	MICPC=MICPC+1	
(1)	014300	110563	<JUMP!ALCONC!<XEXIT-INIT&3000*4>!<XEXIT-INIT&777/2>>	
(1)				

M11

1493
1494
1495
1496 014302 001146
(1) 014302 123600
(1)
1497 001
1498 014304 001147
(1) 014304 113151
(1)
1499 000
1500 014306 001150
(1) 014306 102054
(1)
1501 014310 001151
(1) 014310 022010
(1)
1502 014312 001152
(1) 014312 023100
(1)
1503 014314 001153
(1) 014314 062064
(1)
1504 014316 001154
(1) 014316 063166
(1)
1505 014320 001155
(1) 014320 111160
(1)
1506 014322 001156
(1) 014322 063167
(1)
1507 014324 001157
(1) 014324 115407
(1)
1508 014326 001
1509 001
1510 014326 001160
(1) 014326 020620
(1)
1511 014330 001161
(1) 014330 113165
(1)
1512 000

```

:*****TIME CRITICAL PATH--MODIFY WITH GREAT CARE
.SBTTL TMTH--ROUTINE TO OUTPUT DATA CHARACTERS
TMTH: SPBR IBUS,NPR,SP0 ;READ NPR CONTROL
      MICPC=MICPC+1
      <MOVE!SPBRX!IBUS!NPR!SP0>

      .IF NDF $LOW
      BR4 5$ ;IF RECV NPR --PROCESS
      MICPC=MICPC+1
      <JUMP!BR4CON!<5$-INIT&3000*4>!<5$-INIT&777/2>>

      .ENDC
      BRO I1 ;IF NPR IN PROGRESS --BRANCH
      MICPC=MICPC+1
      <JUMP!BROCON!<I1-INIT&3000*4>!<I1-INIT&777/2>>

5$: OUTPUT IBUS,<INDAT1!TMTDAT> ;WRITE THE EVEN CHAR TO TMT SILO
      MICPC=MICPC+1
      <MOVE!WROUT!IBUS!<INDAT1!TMTDAT>>

      SP IBUS,IIBA1,SP0 ;READ LOW BYTE OF BA TO SP
      MICPC=MICPC+1
      <MOVE!SPX!IBUS!IIBA1!SP0>

      OUTPUT BR,<INCA!IBA1> ;OUTPUT INCREMENTED BA
      MICPC=MICPC+1
      <MOVE!WROUT!BR!<INCA!IBA1>>

      SP BR,DECA,SP6 ;DECREMENT CHARACTER COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP6>

      C TH6 ;NO OVERFLOW
      MICPC=MICPC+1
      <JUMP!CCOND!<TH6-INIT&3000*4>!<TH6-INIT&777/2>>

      SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
      MICPC=MICPC+1
      <MOVE!SPX!BR!DECA!SP7>

      Z HEH1 ;BYTE COUNT ZERO
      MICPC=MICPC+1
      <JUMP!ZCOND!<HEH1-INIT&3000*4>!<HEH1-INIT&777/2>>

TH6: .IF NDF $LOW
      BRWRT IBUS,TMTCON ;READ TMTR CONTROL CSR
      MICPC=MICPC+1
      <MOVE!WRTBR!IBUS!<TMTCON>>

      BR4 TH9 ;IF MORE ROOM IN SILO--BRANCH
      MICPC=MICPC+1
      <JUMP!BR4CON!<TH9-INIT&3000*4>!<TH9-INIT&777/2>>

      .ENDC

```

N11

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-10
TMTH--ROUTINE TO OUTPUT DATA CHARACTERS

PAGE: 0143

1513 014332 001162
(1)
(1) 014332 000565
1514 001
1515 000
1516 001
1517 001
1518 014334 001163
(1)
(1) 014334 063222
(1)
1519 014336 001164
(1)
(1) 014336 100454
(1)
1520 000
1521 014340 001
1522 001
1523 000
1524 000
1525 000
1526 014340 001165
(1)
(1) 014340 022030
(1)
1527 014342 001166
(1)
(1) 014342 023100
(1)
1528 014344 001167
(1)
(1) 014344 062064
(1)
1529 014346 001170
(1)
(1) 014346 111377
(1)
1530 014350 001171
(1)
(1) 014350 063166
(1)
1531 014352 001172
(1)
(1) 014352 111175
(1)
1532 014354 001173
(1)
(1) 014354 063167
(1)
1533 014356 001174
(1)
(1) 014356 115407
(1)
1534 014360 001175
(1)
(1) 014360 123600

TMTF1: STATE TMTH0
MICPC=MICPC+1
<MOVE!WRTEBR!IMM!<TMTH0-INIT&777/2>>
.IF DF \$LOW
ALWAYS XEXIT
.ENDC
.IF NDF \$LOW
XEXIT: SP BR,SELB,SP2 ;STORE NEW TRANSMIT STATE
MICPC=MICPC+1
<MOVE!SPX!BR!SELB!SP2>

ALWAYS I1
MICPC=MICPC+1
<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
.ENDC
TMTH0: .IF DF \$LOW
SPBR IBUS,NPR,SPO ;NPR BUSY
BRO I1
.ENDC
TH9: OUTPUT IBUS,<INDAT2!TMTDAT> ;ODD CHAR TO SILO
MICPC=MICPC+1
<MOVE!WROUT!IBUS!<INDAT2!TMTDAT>>

SP IBUS,IIBA1,SPO ;READ LOW BYTE TO BA
MICPC=MICPC+1
<MOVE!SPX!IBUS!IIBA1!SPO>

OUTPUT BR,<INCA!IBA1> ;OUTPUT THE INCREMENTED BA
MICPC=MICPC+1
<MOVE!WROUT!BR!<INCA!IBA1>>

C HOINCH
MICPC=MICPC+1
<JUMP!CCOND!<HOINCH-INIT&3000*4>!<HOINCH-INIT&777/2>>
TH8: SP BR,DECA,SP6 ;DECREMENT CHARACTERCOUNT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP6>

C TH7 ;NO OVERFLOW
MICPC=MICPC+1
<JUMP!CCOND!<TH7-INIT&3000*4>!<TH7-INIT&777/2>>
1532: SP BR,DECA,SP7 ;DECREMENT HIGH BYTE OF COUNT
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP7>

Z HEH1 ;BYTE COUNT ZERO
MICPC=MICPC+1
<JUMP!ZCOND!<HEH1-INIT&3000*4>!<HEH1-INIT&777/2>>
TH7: SPBR IBUS,NPR,SPO ;READ NPR REGISTER
MICPC=MICPC+1
<MOVE!SPBRX!IBUS!NPR!SPO>

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(1)
1535          001          .IF NDF $LOW
1536 014362    001176      BRO      TH2          ;IF NPR BUSY WAIT TO GO
(1)          001176      MICPC=MICPC+1
(1) 014362    112205      <JUMP!BROCON!<TH2-INIT&3000*4>!<TH2-INIT&777/2>>
(1)
1537          000          .ENDC
1538 014364    001177      STATE    TMTH
(1)          001177      MICPC=MICPC+1
(1) 014364    000546      <MOVE!WTEBR!IMM!<TMTH-INIT&777/2>>
1539 014366    001200      TH3:    SP      BR,SELB,SP2          ;SAVE TSTATE
(1)          001200      MICPC=MICPC+1
(1) 014366    063222      <MOVE!SPX!BR!SELB!SP2>
(1)
1540 014370    001201      TH3X:   BRWRT  IMM,156          ;CLEAR CO AND C1
(1)          001201      MICPC=MICPC+1
(1) 014370    000556      <MOVE!WTEBR!IMM!<156>>
(1)
1541 014372    001202      SP      BR,AANDB,SP0          ;CLEAR THE BITS
(1)          001202      MICPC=MICPC+1
(1) 014372    063260      <MOVE!SPX!BR!AANDB!SP0>
(1)
1542 014374    001203      OUT      BR,<INCA!ONPR>
(1)          001203      MICPC=MICPC+1
(1) 014374    061070      <MOVE!WROUTX!BR!<INCA!ONPR>>
(1)
1543 014376    001204      ALWAYS  I1
(1)          001204      MICPC=MICPC+1
(1) 014376    100454      <JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
(1)
1544          001          .IF NDF $LOW
1545 014400    001205      TH2:    TSTATE TH7
(1)          001205      MICPC=MICPC+1
(1) 014400    000575      <MOVE!WTEBR!IMM!<TH7-INIT&777/2>>
(1)          001206      MICPC=MICPC+1
(1) 014402    063222      <MOVE!SPX!BR!SELB!SP2>
1546 014404    001207      ALWAYS  I1
(1)          001207      MICPC=MICPC+1
(1) 014404    100454      <JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
(1)
1547          000          .ENDC
1548          ;*****END TIME CRITICAL PATH*****
1549          ;

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```

1551
1552 014406 001210
      (1) 001
      (1) 014406 010151
      (1)
      (1) 000
      (1)
1553 014410
      (1) 001211
      (1) 014410 043226
      (1)
1554 014412
      (1) 001212
      (1) 014412 000614
1555 014414
      (1) 001213
      (1) 014414 110521
      (1)
1556
1557
1558 014416
      (1) 001214
      (1) 001
      (1) 014416 010152
      (1)
      (1) 000
      (1)
1559 014420
      (1) 001215
      (1) 014420 000617
1560 014422
      (1) 001216
      (1) 014422 110521
      (1)

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TMTI: .SBTTL TMTI--SEND UNNUMBERED TYPE FIELD
      LDMA IMM,T ;ADDRESS OF TYPE FIELD TO MAR
      MICPC=MICPC+1
      .IF IDN IMM,IMM
      <MOVE!LDMAR!IMM!<T&377>>
      .IFF
      <MOVE!LDMAR!IMM!<T>>
      .ENDC

      SP MEMX,SELB,SP6 ;COPY IT TO SP6
      MICPC=MICPC+1
      <MOVE!SPX!MEMX!SELB!SP6>

      STATE TMTJ
      MICPC=MICPC+1
      <MOVE!WRITEBR!IMM!<TMTJ-INIT&777/2>>
      ALWAYS TD3
      MICPC=MICPC+1
      <JUMP!ALCOND!<TD3-INIT&3000*4>!<TD3-INIT&777/2>>

TMTJ: .SBTTL TMTJ--SEND SUB-TYPE FIELD
      LDMA IMM,ST ;ADDRESS OF SUB-TYPE FIELD TO MAR
      MICPC=MICPC+1
      .IF IDN IMM,IMM
      <MOVE!LDMAR!IMM!<ST&377>>
      .IFF
      <MOVE!LDMAR!IMM!<ST>>
      .ENDC

      STATE TMTK
      MICPC=MICPC+1
      <MOVE!WRITEBR!IMM!<TMTK-INIT&777/2>>
      ALWAYS TD3
      MICPC=MICPC+1
      <JUMP!ALCOND!<TD3-INIT&3000*4>!<TD3-INIT&777/2>>

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1562			.SBTTL TMTK--OUTPUT RESPONSE FIELD (UNNUMB MSG)
1563			
1564	014424		TMTK: BRWRT IMM,3 ;WRITE A 3 TO BR
(1)		001217	MICPC=MICPC+1
(1)	014424	000403	<MOVE!WRTEBR!IMM!<3>>
(1)			
1565	014426		NOP BR,SUB,SP6 ;IF TYPE LESS THAN 3
(1)		001220	MICPC=MICPC+1
(1)	014426	060346	<BR!SUB!SP6>
(1)			
1566	014430		TSTATE TMTL
(1)		001221	MICPC=MICPC+1
(1)	014430	000625	<MOVE!WRTEBR!IMM!<TMTL-INIT&777/2>>
(1)		001222	MICPC=MICPC+1
(1)	014432	063222	<MOVE!SPX!BR!SELB!SP2>
1567	014434		C TMTLO
(1)		001223	MICPC=MICPC+1
(1)	014434	111232	<JUMP!CCOND!<TMTLO-INIT&3000*4>!<TMTLO-INIT&777/2>>
(1)			
1568	014436		ALWAYS TD2
(1)		001224	MICPC=MICPC+1
(1)	014436	110520	<JUMP!ALCOND!<TD2-INIT&3000*4>!<TD2-INIT&777/2>>
(1)			
1569			
1570			.SBTTL TMTL--UNNUMB MSG NUMBER FIELD
1571	014440		TMTL: TSTATE TMTM
(1)		001225	MICPC=MICPC+1
(1)	014440	000637	<MOVE!WRTEBR!IMM!<TMTM-INIT&777/2>>
(1)		001226	MICPC=MICPC+1
(1)	014442	063222	<MOVE!SPX!BR!SELB!SP2>
1572	014444		BRWRT IMM,3
(1)		001227	MICPC=MICPC+1
(1)	014444	000403	<MOVE!WRTEBR!IMM!<3>>
(1)			
1573	014446		CMP BR,SP6 ;IS MESSAGE REP
(1)		001230	MICPC=MICPC+1
(1)	014446	060366	<SUBTC!BR!SP6>
(1)			
1574	014450		Z TMTL1 ;YES
(1)		001231	MICPC=MICPC+1
(1)	014450	111635	<JUMP!ZCOND!<TMTL1-INIT&3000*4>!<TMTL1-INIT&777/2>>
(1)			
1575	014452		TMTLO: BRWRT IMM,0 ;ADDRESS CONTNAT OF ZERO
(1)		001232	MICPC=MICPC+1
(1)	014452	000400	<MOVE!WRTEBR!IMM!<0>>
(1)			
1576		001	.IF DF SLOW
1577			ALWAYS TMTAS
1578		000	.ENDC
1579		001	.IF NDF SLOW
1580	014454		OUTPUT BR,<SELB!TMTDAT> ;SEND IT OUT
(1)		001233	MICPC=MICPC+1
(1)	014454	062230	<MOVE!WROUT!BR!<SELB!TMTDAT>>
(1)			
1581	014456		ALWAYS I1 ;BACK TO IDLE LOOP
(1)		001234	MICPC=MICPC+1

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-75 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-14
TMTL--UNNUMB MSG NUMBER FIELD

PAGE: 0147

(1) 014456 100454
(1)
1582 000
1583
1594 014460
(1) 001235
(1) 014460 060572
(1)
1585 014462
(1) 001236
(1) 014462 110441
(1)
1596

<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>
.ENDC
TMTL1: BRWRTE BR,DECA!SP12 ;WRITE A RESPONSE
MICPC=MICPC+1
<MOVE!WRTEBR!BR!<DECA!SP12>>
ALWAYS TMTAS
MICPC=MICPC+1
<JUMP!ALCOND!<TMTAS-INIT&3000*4>!<TMTAS-INIT&777/2>>
:

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1588
1589 014464 001237
      (1) 014464 000641
1590 014466 001240
      (1) 014466 110533
      (1)
1591 014470 001241
      (1) 014470 000402
      (1)
1592 014472 001242
      (1) 014472 062231
      (1)
1593 014474 001243
      (1) 014474 062230
      (1)
1594 014476 001244
      (1) 014476 000404
      (1)
1595 014500 001245
      (1) 014500 063710
      (1)
1596 014502 001246
      (1) 014502 060530
      (1)
1597 014504 001247
      (1) 014504 113653
      (1)
1598 014506 001250
      (1) 014506 000775
      (1)
1599 014510 001251
      (1) 014510 063270
      (1)
1600 014512 001252
      (1) 014512 110740
      (1)
1601 014514 001253
      (1) 014514 000576
      (1)
1602 014516 001254
      (1) 014516 110651
      (1)

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TMTM: .SBTTL TMTM--UNNUMB MSG--STATION ADDRESS
      STATE TNEOM
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<TNEOM-INIT&777/2>>
      ALWAYS TF2
      MICPC=MICPC+1
      <JUMP!ALCOND!<TF2-INIT&3000*4>!<TF2-INIT&777/2>>

TNEOM: BRWRT IMM,2 ;END OF MESSAGE TO BR
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<2>>

      OUTPUT BR,<SELB!OTMTCO>
      MICPC=MICPC+1
      <MOVE!WROUT!BR!<SELB!OTMTCO>>

      OUTPUT BR,<SELB!TMDAT> ;OUTPUT A GARBAGE CHARACTER
      MICPC=MICPC+1
      <MOVE!WROUT!BR!<SELB!TMDAT>>

      BRWRT IMM,4 ;SET UP LINE HAS GONE IDLE MASK
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<4>>

      SPBR BR,AORB,SP10 ;UPDATE LINE STATUS WORD
      MICPC=MICPC+1
      <MOVE!SPBRX!BR!AORB!SP10>

      BRWRT BR,AA!SP10 ;SHIFT STATUS LEFT
      MICPC=MICPC+1
      <MOVE!WRTEBR!BR!<AA!SP10>>

      BR7 10$ ;IF HDX SET---BRANCH TO CLEAR OK TO SEND
      MICPC=MICPC+1
      <JUMP!BR7CON!<10$-INIT&3000*4>!<10$-INIT&777/2>>

      BRWRT IMM,376 ;MASK TO TURN OFF UNNUMB PENDING
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<376>>

5$: SP BR,AANDB,SP10 ;MASK TO LINE STATUS WORD
      MICPC=MICPC+1
      <MOVE!SPX!BR!AANDB!SP10>

      ALWAYS TEOM2
      MICPC=MICPC+1
      <JUMP!ALCOND!<TEOM2-INIT&3000*4>!<TEOM2-INIT&777/2>>

10$: BRWRT IMM,176 ;CLEAR OK TO SEND AND UNNUMB PENDING
      MICPC=MICPC+1
      <MOVE!WRTEBR!IMM!<176>>

      ALWAYS 5$
      MICPC=MICPC+1
      <JUMP!ALCOND!<5$-INIT&3000*4>!<5$-INIT&777/2>>

```

G12

1604
1605
1606
1607 014520 001255
(1) 014520 000577
(1)
1608
1609
1610
1611
1612 014522 001256
(1) 014522 061271
(1)
1613 014524 001257
(1) 014524 060601
(1)
1614 014526 001260
(1) 014526 102051
(1)
1615 014530 001261
(1) 014530 103451
(1)
1616 014532 001262
(1) 014532 063175
(1)
1617 014534 001263
(1) 014534 111670
(1)
1618 014536 001264
(1) 014536 060610
(1)
1619 014540 001265
(1) 014540 116731
(1)
1620 014542 001266
(1) 014542 116331
(1)
1621 014544 001267
(1) 014544 100451
(1)
1622 014546 001270
1623 014546 000402
(1)
(1)

```
.SBTTL TIMSRV--TIMEOUT ROUTINE--SENDS REP
;
;ENABLE LSB
TIMSRV: BRWRT IMM,177 ;MASK OFF BR REG
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<177>>

;RESET TIMER---SLICK MOVE
;SINCE TIMER IS RESET BY WRITING
;A 1 AND THE EXPIRATION LOCKS
;LIKE 1---VOILA
;AND THE BIT ON
OUT BR,<AANDB!OBR>
MICPC=MICPC+1
<MOVE!WROUTX!BR!<AANDB!OBR>>

BRWRT BR,SELA!SP1 ;READ STATUS BYTE
MICPC=MICPC+1
<MOVE!WRTBR!BR!<SELA!SP1>>

BRO IDLE
MICPC=MICPC+1
<JUMP!BROCON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

BR7 IDLE ;IF IN MAINT. MODE DISABLE TIMER
MICPC=MICPC+1
<JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

SP BR,DECA,SP15 ;DECREMENT THE COUNTER
MICPC=MICPC+1
<MOVE!SPX!BR!DECA!SP15>

Z 20$ ;IF ALL ONES HAS EXPIRED
MICPC=MICPC+1
<JUMP!ZCOND!<20$-INIT&3000*4>!<20$-INIT&777/2>>

10$: BRWRT BR,SELA!SP10 ;READ LINE STATUS
MICPC=MICPC+1
<MOVE!WRTBR!BR!<SELA!SP10>>

BR1 TABUPD ;NUMBERED MESSAGE IN PROGRESS
MICPC=MICPC+1
<JUMP!BR1CON!<TABUPD-INIT&3000*4>!<TABUPD-INIT&777/2>>

BRO TABUPD ;UNNUMBMSGIN PROGRES=
MICPC=MICPC+1
<JUMP!BROCON!<TABUPD-INIT&3000*4>!<TABUPD-INIT&777/2>>

ALWAYS IDLE ;ELSE BACK TO IDLE LOOP
MICPC=MICPC+1
<JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>

TIME1:
20$: BRWRT IMM,2
MICPC=MICPC+1
<MOVE!WRTBR!IMM!<2>>
```

H12

1624	014550	001271	SP BR,SELB,SP15	:RESET THE TIMER TICK COUNT
(1)		063235	MICPC=MICPC+1	
(1)	014550		<MOVE!SPX!BR!SELB!SP15>	
1625		001	.IF NDF SLOW	
1626	014552	001272	BRWRT IMM,201	:SET OK TO SEND AND
(1)		000601	MICPC=MICPC+1	
(1)	014552		<MOVE!WRTBR!IMM!<201>>	
1627	014554	001273	SPBR BR,AORB,SP10	:UNNUM MSG PENDING
(1)		063710	MICPC=MICPC+1	
(1)	014554		<MOVE!SPBRX!BR!AORB!SP10>	
1629		000	.ENDC	
1629		001	.IF DF SLOW	
1630			BRWRT DP,<SELA!SP10>	:READ LINE STATUS WORD
1631		000	.ENDC	
1632	014556	001274	BRSHFT	
(1)		001620	MICPC=MICPC+1	
(1)	014556		<MOVE!SHFTBR!WRTBR!SELB>	
1633	014560	001275	BR4 BS1	:IF IN START MODE--BRAN
(1)		103111	MICPC=MICPC+1	
(1)	014560		<JUMP!BR4CON!<BS1-INIT&3000*4>!<BS1-INIT&777/2>>	
1634	014562	001276	BRWRT BR,DECA!SP12	:GET LAST NUMBER SENT
(1)		060572	MICPC=MICPC+1	
(1)	014562		<MOVE!WRTBR!BR!<DECA!SP12>>	
1635	014564	001277	CMP BR,SP17	:COMPARE TO LAST ACKED
(1)		060377	MICPC=MICPC+1	
(1)	014564		<SUBTC!BR!SP17>	
1636	014566	001300	Z SNDACK	:IF EQ --SEND ACK
(1)		111733	MICPC=MICPC+1	
(1)	014566		<JUMP!ZCONC!<SNDACK-INIT&3000*4>!<SNDACK-INIT&777/2>>	
1637	014570	001301	TIME2: LDMA IMM,T	:LOAD ADDRESS OF TYPE FIELD IN UNNUMB SX
(1)		001	MICPC=MICPC+1	
(1)	014570	010151	.IF IDN IMM,IMM	
(1)			<MOVE!LDMAR!IMM!<T&377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<T>>	
(1)		000	.ENDC	
1638	014572	001302	MEMINC IMM,3	:LOAD REP TYPE
(1)		016403	MICPC=MICPC+1	
(1)	014572		<MOVE!WRMEM!INCMAR!IMM!<3>>	
1639	014574	001303	MEMINC IMM,300	:ZERO THE SUB-TYPE
(1)		016700	MICPC=MICPC+1	
(1)	014574		<MOVE!WRMEM!INCMAR!IMM!<300>>	
1640	014576	001304	LDMA IMM,REPCS	:CUMULATIVE REPS RECD
(1)		001	MICPC=MICPC+1	
(1)			.IF IDN IMM,IMM	

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(1) 014576 010015      <MOVE!LDMAR!IMM!<REPCS&377>>
(1)                      .IFF
(1)                      <MOVE!LDMAR!IMM!<REPCS>>
(1)                      .ENDC
(1)                      000
1641 014600      SP      MEMX,SELB,SPD      ;COPY IT TO SPD
(1)                      MICPC=MICPC+1
(1) 014600 001305      <MOVE!SPX!MEMX!SELB!SPD>
(1)                      043220
1642 014602      MEM      BR,INCA!SPD      ;INCREMENT IT
(1)                      MICPC=MICPC+1
(1) 014602 001306      <MOVE!WRMEM!BR!<INCA!SPD>>
(1)                      062460
1643 014604      LDMA      IMM,REPST      ;ADDRESS DYNAMIC REP COUNTER
(1)                      MICPC=MICPC+1
(1)                      .IF IDN IMM,IMM
(1) 014604 001307      <MOVE!LDMAR!IMM!<REPST&377>>
(1)                      001
(1) 014604 010003      <MOVE!LDMAR!IMM!<REPST>>
(1)                      .IFF
(1)                      <MOVE!LDMAR!IMM!<REPST>>
(1)                      .ENDC
(1)                      000
1644 014606      BRWRT      MEMX,SELB      ;COPY IT TO THE BR
(1)                      MICPC=MICPC+1
(1) 014606 001310      <MOVE!WRTBR!MEMX!<SELB>>
(1)                      040620
1645 014610      BSHFTB
(1)                      MICPC=MICPC+1
(1) 014610 001311      <MOVE!SHFTBR!SELB!BR>
(1)                      061620
1646 014612      MEM      BR,SELB
(1)                      MICPC=MICPC+1
(1) 014612 001312      <MOVE!WRMEM!BR!<SELB>>
(1)                      062620
1647 014614      BRO      RTHRES
(1)                      MICPC=MICPC+1
(1) 014614 001313      <JUMP!BROCON!<RTHRES-INIT&3000*4>!<RTHRES-INIT&777/2>>
(1)                      106372
1648                      001
1649                      .IF DF $LOW
1650                      BRWRT      IMM,201      ;MASK FOR OK TO SEND
1651                      SP      BR,AORB,SP10      ;OR IT IN
1652                      .ENDC
1652 014616      ALWAYS      IDLE
(1)                      MICPC=MICPC+1
(1) 014616 001314      <JUMP!ALCOND!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
(1)                      100451
1653                      .DSABLE LSB
1654                      :

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1656 014620 001315
(1) 014620 120620
(1)
1657 014622 001316
(1) 014622 106351
(1)
1658 014624 001317
(1) 014624 000402
(1)
1659 014626 001320
(1) 014626 062231
(1)
1660 014630 001321
(1) 014630 062230
(1)
1661 014632 001322
(1) 014632 060601
(1)
1662 014634 001323
(1) 014634 113762
(1)
1663 014636 001324
(1) 014636 063072
(1)
1664 014640 001325
(1) 001
(1)
(1)
(1) 014640 070216
(1) 000
(1)
1665 014642 001326
(1) 014642 040620
(1)
1666 014644 001327
(1) 014644 112340
(1)
1667 014646 001330
(1) 014646 000775
(1)
1668 014650 001331
(1) 014650 063670
(1)

TEOM: BRWRITE IBUS,UBBR
MICPC=MICPC+1
<MOVE!WRITEBR!IBUS!<UBBR>>

BRO NXMERR ;NON-EXISTANT MEMORY
MICPC=MICPC+1
<JUMP!BROCON!<NXMERR-INIT&3000*4>!<NXMERR-INIT&777/2>>

BRWRITE IMM,2 ;EOM TO BR
MICPC=MICPC+1
<MOVE!WRITEBR!IMM!<2>>

OUTPUT BR,<SELB!OTMTCO> ;WRITE TMTR CONTROL
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!OTMTCO>>

OUTPUT BR,<SELB!TMTDAT> ;WRITE GARBAGE DATA
MICPC=MICPC+1
<MOVE!WROUT!BR!<SELB!TMTDAT>>

BRWRITE BR,SELH!SP1 ;CHECK FOR BOOT MODE
MICPC=MICPC+1
<MOVE!WRITEBR!BR!<SELH!SP1>>

BR7 BTEOM ;---IF SET IS MAINT MSG
MICPC=MICPC+1
<JUMP!BR7CON!<BTEOM-INIT&3000*4>!<BTEOM-INIT&777/2>>

SP BR,INCA,SP12 ;INCREMENT THE MESSAGE NUMBER
MICPC=MICPC+1
<MOVE!SPX!BR!INCA!SP12>

TEOM1: LDMA BR,SEL4!SP16 ;ADDRESS LAST TMT LINK
MICPC=MICPC+1
.IF IDN BR,IMM
<MOVE!LDMA!BR!IMM!<SEL4!SP15&377>>
.IFF
<MOVE!LDMA!BR!<SEL4!SP16>>
.ENDC

BRWRITE MEMX,SELB
MICPC=MICPC+1
<MOVE!WRITEBR!MEMX!<SELB>>

BRO TEOM2
MICPC=MICPC+1
<JUMP!BROCON!<TEOM2-INIT&3000*4>!<TEOM2-INIT&777/2>>

TEOM3: BRWRITE IMM,375 ;TURN OFF MESSAGE PENDING
MICPC=MICPC+1
<MOVE!WRITEBR!IMM!<375>>

SPBR BR,AANDB,SP10 ;
MICPC=MICPC+1
<MOVE!SPBRX!BR!AANDB!SP10>

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-20
TIMSRV--TIMEOUT ROUTINE--SENDS REP

PAGE: 0153

1669	014652		BRO	TEOM2		;IF UNNUMB PENDING--GO AWAY
(1)		001332	MICPC=MICPC+1			
(1)	014652	112340	<JUMP!BROCON!<TEOM2-INIT&3000*4>!<TEOM2-INIT&777/2>>			
(1)						
1670			.SBTTL	SNDACK--ROUTINE TO SEND AN ACK		
1671	014654		SNDACK: LDMA	IMM,1		
(1)		001333	MICPC=MICPC+1			
(1)		001	.IF IDN IMM,IMM			
(1)	014654	010151	<MOVE!LDMA!IMM!<T&377>>			
(1)			.IFF			
(1)			<MOVE!LDMA!IMM!<T>>			
(1)		000	.ENDC			
(1)						
1672	014656		MEMINC	IMM,1		
(1)		001334	MICPC=MICPC+1			
(1)	014656	016401	<MOVE!WRMEM!INCMAR!IMM!<1>>			
(1)						
1673	014660		BRWRT	IMM,5		
(1)		001335	MICPC=MICPC+1			
(1)	014660	000405	<MOVE!WRTEBR!IMM!<5>>			
(1)						
1674	014662		SA2:	MEMINC	IMM,300	
(1)		001336	MICPC=MICPC+1			
(1)	014662	016700	<MOVE!WRMEM!INCMAR!IMM!<300>>			
(1)						
1675	014664		SA3:	SP	BR,AORB,SP10	
(1)		001337	MICPC=MICPC+1			
(1)	014664	063310	<MOVE!SPX!BR!AORB!SP10>			
(1)						
1676						
1677		001	TEOM2:	.IF DF	\$LOW	
1678			STATE	TMTA		
1679			ALWAYS	XEXIT		
1680		000	.ENDC			
1681		001	TEOM2:	.IF NDF	\$LOW	
1682	014666		TSTATE	TMTA		
(1)		001340	MICPC=MICPC+1			
(1)	014666	000403	<MOVE!WRTEBR!IMM!<TMTA-INIT&777/2>>			
(1)		001341	MICPC=MICPC+1			
(1)	014670	063222	<MOVE!SPX!BR!SELB!SP2>			
1683	014672		ALWAYS	I1		
(1)		001342	MICPC=MICPC+1			
(1)	014672	100454	<JUMP!ALCOND!<I1-INIT&3000*4>!<I1-INIT&777/2>>			
(1)						
1684		000	FJDGE:	.ENDC		
1685	014674		BRWRT	IBUS,NPR		;READ NPR CONTROL
(1)		001343	MICPC=MICPC+1			
(1)	014674	120600	<MOVE!WRTEBR!IBUS!<NPR>>			
(1)						
1686	014676		BRO	IDLE		;IF NPR GOING---LEAVE
(1)		001344	MICPC=MICPC+1			
(1)	014676	102051	<JUMP!BROCON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>			
(1)						
1687	014700		BRWRT	BR!LDMA,SELA!SP4		;LOAD THE MAR
(1)		001345	MICPC=MICPC+1			
(1)	014700	070604	<MOVE!WRTEBR!BR!LDMA!<SELA!SP4>>			

```

(1)
1688 014702 001346 BR7 BS2 ;IF SET - READ BACK ALL 200
(1) 014702 103520 MICPC=MICPC+1
(1) <JUMP!BR7CON!<BS2-INIT&3000*4>!<BS2-INIT&777/2>>
1689 014704 001347 MEMINC IBUS,INDAT1 ;OTHERWISE RESTORE TWO BYTES
(1) 014704 036400 MICPC=MICPC+1
(1) <MOVE!WRMEM!INCMAR!IBUS!<INDAT1>>
1690 014706 001350 MEMINC IBUS,INDAT2 ;..
(1) 014706 036420 MICPC=MICPC+1
(1) <MOVE!WRMEM!INCMAR!IBUS!<INDAT2>>
1691 014710 001351 BRWRT IMM,2 ;UPDATE---UNIBUS ADDRESS
(1) 014710 000402 MICPC=MICPC+1
(1) <MOVE!WRTEBR!IMM!<2>>
1692 014712 001352 SP BR,ADD,SP4 ;UPDATE NPR COUNTER
(1) 014712 063004 MICPC=MICPC+1
(1) <MOVE!SPX!BR!ADD!SP4>
1693 014714 001353 SP IBUS,IIBA1,SP0 ;UPDATE ADDRESS LOW
(1) 014714 023100 MICPC=MICPC+1
(1) <MOVE!SPX!IBUS!IIBA1!SP0>
1694 014716 001354 OUTPUT BR,ADD!IBA1
(1) 014716 062004 MICPC=MICPC+1
(1) <MOVE!WROUT!BR!<ADD!IBA1>>
1695 014720 001355 SP IBUS,IIBA2,SP0 ;READ HIGH ADDRESS
(1) 014720 023120 MICPC=MICPC+1
(1) <MOVE!SPX!IBUS!IIBA2!SP0>
1696 014722 001356 OUTPUT BR,AC!IBA2 ;UPDATE HIGH
(1) 014722 062105 MICPC=MICPC+1
(1) <MOVE!WROUT!BR!<AC!IBA2>>
1697 014724 001357 SP IBUS,NPR,SP0 ;READ NPR REGISTER
(1) 014724 123200 MICPC=MICPC+1
(1) <MOVE!SPX!IBUS!NPR!SP0>
1698 014726 001360 C RESEXT ;IF CARRY---UPDATE MXT
(1) 014726 105363 MICPC=MICPC+1
(1) <JUMP!CCOND!<RESEXT-INIT&3000*4>!<RESEXT-INIT&777/2>>
1699 014730 001361 ALWAYS TH3X ;GO DO ANOTHER NPR
(1) 014730 110601 MICPC=MICPC+1
(1) <JUMP!ALCOND!<TH3X-INIT&3000*4>!<TH3X-INIT&777/2>>
1700 014732 001362 BTEOM: BRWRT IMM,374 ;MASK FOR CLEAR MSG PENDING
(1) 014732 000774 MICPC=MICPC+1
(1) <MOVE!WRTEBR!IMM!<374>>
1701 014734 001363 SP BR,AANDB,SP10 ;TURN THEM OFF IN LINE STATUS WORD
(1) 014734 063270 MICPC=MICPC+1
(1) <MOVE!SPX!BR!AANDB!SP10>

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(1)
1702 014736 001364 SP BR,SELB,SP13 ;STORE UNRECOGNIZABLE VALUE INTO SP13
(1) 014736 063233 MICPC=MICPC+1
(1) <MOVE!SPX!BR!SELB!SP13>
(1)
1703 ;SO "RH3" WILL EXIT BACK TO IDLE LOOP
1704 014740 LDMA IMM,STC ;ADDRESS START OF TMT CHAIN
(1) 001365 MICPC=MICPC+1
(1) 001 .IF IDN IMM,IMM
(1) 014740 010067 <MOVE!LDMA!IMM!<STC&377>>
(1) .IFF
(1) <MOVE!LDMA!IMM!<STC>>
(1) .ENDC
(1) 000
(1)
1705 014742 SP MEMX,SELB,SPO ;COPY LINK ADDRESS
(1) 001366 MICPC=MICPC+1
(1) 014742 043220 <MOVE!SPX!MEMX!SELB!SPO>
(1)
1706 001 .IF DF SLOW
1707 TSTATE NUMSYN ;CHANGE XMIT STATE TO LINE IS IDLE
1708 .ENDC
1709 001 .IF NDF SLOW
1710 014744 TSTATE TMTA ;CHANGE XMIT STATE TO LINE IS IDLE
(1) 001367 MICPC=MICPC+1
(1) 014744 000403 <MOVE!WTEBR!IMM!<TMTA-INIT&777/2>>
(1) 001370 MICPC=MICPC+1
(1) 014746 063222 <MOVE!SPX!BR!SELB!SP2>
1711 000 .ENDC
1712 014750 ALWAYS TDON2 ;POST A DONE
(1) 001371 MICPC=MICPC+1
(1) 014750 114532 <JUMP!ALCOND!<TDON2-INIT&3000*4>!<TDON2-INIT&777/2>>
(1)
1713 014752 RL4: RSTATE RCVL
(1) 001372 MICPC=MICPC+1
(1) 014752 000705 <MOVE!WTEBR!IMM!<RCVL-INIT&777/2>>
(1) 001373 MICPC=MICPC+1
(1) 014754 063223 <MOVE!SPX!BR!SELB!SP3>
1714 014756 SP IBUS,NPR,SPO ;READ NPR CONTROL REGISTER
(1) 001374 MICPC=MICPC+1
(1) 014756 123200 <MOVE!SPX!IBUS!NPR!SPO>
(1)
1715 014760 BRWTE IMM,221
(1) 001375 MICPC=MICPC+1
(1) 014760 000621 <MOVE!WTEBR!IMM!<221>>
(1)
1716 014762 ALWAYS RK7
(1) 001376 MICPC=MICPC+1
(1) 014762 104623 <JUMP!ALCOND!<RK7-INIT&3000*4>!<RK7-INIT&777/2>>
(1)
1717 014764 HOINCH: SP IBUS,IIBA2,SPO
(1) 001377 MICPC=MICPC+1
(1) 014764 023120 <MOVE!SPX!IBUS!IIBA2!SPO>
(1)
1718 014766 OUTPUT BR,INCA,IIBA2 ;OUTPUT INCREMENTED BA
(1) 001400 MICPC=MICPC+1
(1) 014766 062065 <MOVE!WROUT!BR!<INCA!IIBA2>>

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DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-23
SNDACK--ROUTINE TO SEND AN ACK

PAGE: 0156

(1)	1719	014770		C	SS		; INCREMENT BYTEW COUNT
(1)			001401				
(1)		014770	115003				
(1)							
(1)	1720	014772		ALWAYS	TH8		
(1)			001402				
(1)		014772	110571				
(1)							
(1)	1721						
(1)	1722	014774		SS:			
(1)			001403				
(1)		014774	123200				
(1)							
(1)	1723	014776					
(1)			001404				
(1)		014776	000404				
(1)							
(1)	1724	015000					
(1)			001405				
(1)		015000	061010				
(1)							
(1)	1725	015002					
(1)			001406				
(1)		015002	110571				
(1)							
(1)	1726						
(1)	1727		001				
(1)	1728	015004		HEH1:			
(1)			001407				
(1)		015004	000715				
(1)	1729	015006					
(1)			001410				
(1)		015006	110563				
(1)							
(1)	1730		000				
(1)	1731						
(1)	1732		001				
(1)	1733			HEH1:			
(1)	1734						
(1)	1735		000				

1737
1738 015010 001411
(1) 001
(1) 015010 010016
(1)
(1)
(1) 000
(1)
1739 015012
(1) 001412
(1) 015012 043220
(1)
1740 015014
(1) 001413
(1) 015014 062460
(1)
1741 015016
(1) 001414
(1) 001
(1) 015016 010151
(1)
(1) 000
(1)
1742 015020
(1) 001415
(1) 015020 016402
(1)
1743 015022
(1) 001416
(1) 015022 016703
(1)
1744 015024
(1) 001417
(1) 015024 114704
(1)
1745
1746
1747 015026
(1) 001420
(1) 015026 060610
(1)
1748 015030
(1) 001421
(1) 015030 001620
(1)
1749 015032
(1) 001422
(1) 015032 117026
(1)
1750
1751 015034
(1) 001423
(1) 001
(1) 015034 010177

```

REP:  .SBTTL  REP HANDLER
      LDMA   IMM, REPCR          ;LOAD MAR ADDRESS WITH POINTER TO REPS RECD
      MICPC=MICPC+1
      .IF IDN IMM, IMM
      <MOVE!LDMAR!IMM!<REPCR&377>>
      .IFF
      <MOVE!LDMAR!IMM!<REPCR>>
      .ENDC

      SP      MEMX, SELB, SPO      ;READ NUMBER OF REPS RECD
      MICPC=MICPC+1
      <MOVE!SPX!MEMX!SELB!SPO>

      MEM     DP, <INCA!SPO>      ;INCREMNT REPS RECD
      MICPC=MICPC+1
      <MOVE!WRMEM!DP!<INCA!SPO>>

      LDMA   IMM, T              ;LOAD ADDRESS OF TYPE FIELD
      MICPC=MICPC+1
      .IF IDN IMM, IMM
      <MOVE!LDMAR!IMM!<T&377>>
      .IFF
      <MOVE!LDMAR!IMM!<T>>
      .ENDC

      MEMINC  IMM, 2              ; LOAD NAK TYPE
      MICPC=MICPC+1
      <MOVE!WRMEM!INCMAR!IMM!<2>>

      MEMINC  IMM, 303            ;LOAD REP RESPONSE SUB-TYPE
      MICPC=MICPC+1
      <MOVE!WRMEM!INCMAR!IMM!<303>>

      ALWAYS  SNAK                ;SEND AN UNNUMB MSG
      MICPC=MICPC+1
      <JUMP!ALCOND!<SNAK-INIT&3000*4>!<SNAK-INIT&777/2>>

START: .SBTTL  START HANDLER
      BRWRT  DP, <SELA!SP10>      ;READ LINE STATUS WORD
      MICPC=MICPC+1
      <MOVE!WRTBR!DP!<SELA!SP10>>

      BRSHFT                                ;GET START MODE BIT IN TESTABLE POSITION
      MICPC=MICPC+1
      <MOVE!SHFTBR!WRTBR!SELB>

      BR4    10$                  ;IF IN START MODE SET STACK
      MICPC=MICPC+1
      <JUMP!BR4CON!<10$-INIT&3000*4>!<10$-INIT&777/2>>

                                           ;ELSE SET UP START ERROR
      LDMA   IMM, <<RTHRS+3>>
      MICPC=MICPC+1
      .IF IDN IMM, IMM
      <MOVE!LDMAR!IMM!<<RTHRS+3>&377>>

```

```

(1)
(1)
(1)      000
(1)
1752 015036      001424      BRWRT IMM,200
(1)      015036      000600      MICPC=MICPC+1
(1)      015036      000600      <MOVE!WRTBR!IMM!<200>>
(1)
1753 015040      001425      ALWAYS RCEXY
(1)      015040      114522      MICPC=MICPC+1
(1)      015040      114522      <JUMP!ALCOND!<RCEXY-INIT&3000*4>!<RCEXY-INIT&777/2>>
(1)
1754 015042      001426      10$: LDMA IMM,T ;SET UP ADDRESS OF TYPE FIELD
(1)      015042      001426      MICPC=MICPC+1
(1)      015042      001426      .IF IDN IMM,IMM
(1)      015042      010151      <MOVE!LDMA!IMM!<T&377>>
(1)      015042      010151      .IFF
(1)      015042      010151      <MOVE!LDMA!IMM!<T>>
(1)      015042      010151      .ENDC
(1)      015042      010151      000
(1)
1755 015044      001427      MEMINC IMM,7 ;WRITE STACK TYPE
(1)      015044      001427      MICPC=MICPC+1
(1)      015044      016407      <MOVE!WRMEM!INCMAR!IMM!<7>>
(1)
1756 015046      001430      BRWRT IMM,11 ;SET START RECD AND UNNUMB PENDING
(1)      015046      001430      MICPC=MICPC+1
(1)      015046      000411      <MOVE!WRTBR!IMM!<11>>
(1)
1757 015050      001431      ALWAYS SA2 ;SEND THE UNNUMBERED MESSAGE
(1)      015050      001431      MICPC=MICPC+1
(1)      015050      110736      <JUMP!ALCOND!<SA2-INIT&3000*4>!<SA2-INIT&777/2>>
(1)
1758
1759 ; SBTTL STACK HANDLER
1760 015052      001432      STACK: BRWRT IMM,327 ;MASK TO CLEAR START MODE
(1)      015052      001432      MICPC=MICPC+1
(1)      015052      000727      <MOVE!WRTBR!IMM!<327>>
(1)
1761 015054      001433      SP BR,AANDB,SP10 ;CLEAR START MODE
(1)      015054      001433      MICPC=MICPC+1
(1)      015054      063270      <MOVE!SPX!BR!AANDB!SP10>
(1)
1762 015056      001434      ALWAYS TIME1 ;RESET TIMER AND IDLE
(1)      015056      001434      MICPC=MICPC+1
(1)      015056      110670      <JUMP!ALCOND!<TIME1-INIT&3000*4>!<TIME1-INIT&777/2>>
(1)

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```

1764 015060 001435
(1) 015060 023160
(1)
1765 015062 001436
(1) 015062 062067
(1)
1766 015064 001437
(1) 015064 115041
(1)
1767 015066 001440
(1) 015066 104641
(1)
1768
1769 015070 001441
(1) 015070 123220
(1)
1770 015072 001442
(1) 015072 000404
(1)
1771 015074 001443
(1) 015074 061011
(1)
1772 015076 001444
(1) 015076 104641
(1)
1773 001
1774
1775 000
1776 000
1777 015100 001445
(1) 015100 001
(1) 015100 010011
(1)
(1) 000
(1)
1778 015102 001446
(1) 015102 043220
(1)
1779 015104 001447
(1) 015104 042460
(1)
1780 015106 001450
(1) 001

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ICBA22: SP      IBUS,IOBA2,SPO      ;READTHEHIGH ORDERBITS OF BA TO SPC
        MICPC=MICPC+1
        <MOVE!SPX!IBUS!IOBA2!SPO>

        OUTPUT DP,<INCA!OBA2>      ;OUTPUT THE INCREMENTED COUNT
        MICPC=MICPC+1
        <MOVE!WROUT!DP!<INCA!OBA2>>

        C      SS      ;IF CARRY SET INCREMENT THE MXTBITS
        MICPC=MICPC+1
        <JUMP!CCOND!<SS-INIT&3000*4>!<SS-INIT&777/2>>

        ALWAYS RK3
        MICPC=MICPC+1
        <JUMP!ALCOND!<RK3-INIT&3000*4>!<RK3-INIT&777/2>>

SS:      SP      IBUS,UBBR,SPO
        MICPC=MICPC+1
        <MOVE!SPX!IBUS!UBBR!SPO>

        BRWRT IMM,4
        MICPC=MICPC+1
        <MOVE!WRTEBR!IMM!<4>>

        OUT      BR,<ADD!OBR>
        MICPC=MICPC+1
        <MOVE!WROUTX!BR!<ADD!OBR>>

        ALWAYS RK3
        MICPC=MICPC+1
        <JUMP!ALCOND!<RK3-INIT&3000*4>!<RK3-INIT&777/2>>

FLUSH1: .IF DF SLOW
        OUTPUT IMM,<200!ORCVCO>      ;FLUSH THE RECVR
        ALWAYS CG1
        .ENDC

NAK:     LDMA     IMM,NDATR      ;CUMMULATIVE NAK COUNTER
        MICPC=MICPC+1
        .IF IDN IMM,IMM
        <MOVE!LDMA!IMM!<NDATR&377>>
        .IFF
        <MOVE!LDMA!IMM!<NDATR>>
        .ENDC

        SP      MEMX,SELB,SPO      ;READ IT
        MICPC=MICPC+1
        <MOVE!SPX!MEMX!SELB!SPO>

        MEM      MEMX,INCA!SPO      ;INCREMENT THE COUNTER
        MICPC=MICPC+1
        <MOVE!WRMEM!MEMX!<INCA!SPO>>

        LDMA     IMM,STC      ;ADDRESS START OF TMT CHAIN
        MICPC=MICPC+1
        .IF IDN IMM,IMM

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(1) 015106 010067      <MOVE!LDMAR!IMM!<STC&377>>
(1)                      .IFF
(1)                      <MOVE!LDMAR!IMM!<STC>>
(1)                      .ENDC
(1)                      000
1781 015110 001451      SP      MEMX,SELB,SP16      ;COPY START OF CHAIN TO LAST XMIT PCINTER
(1)                      MICPC=MICPC+1
(1) 015110 043236      <MOVE!SPX!MEMX!SELB!SP16>
(1)
1782 015112 001452      BRWRT  BR,INCA!SP17      ;GETLASTMESSAGE ACKED
(1)                      MICPC=MICPC+1
(1) 015112 060477      <MOVE!WRTBR!BR!<INCA!SP17>>
(1)
1783 015114 001453      SP      BR,SELB,SP12      ;COPY TO CURRENT NUMBER
(1)                      MICPC=MICPC+1
(1) 015114 063232      <MOVE!SPX!BR!SELB!SP12>
(1)
1784 015116 001454      BRWRT  IMM,6      ;WRITE NUMBERED MSG PENDING
(1)                      MICPC=MICPC+1
(1) 015116 000406      <MOVE!WRTBR!IMM!<6>>
(1)
1785
1786 015120 001455      SP      BR,AORB,SP10      ; AND LINE HAS GONE IDLE
(1)                      MICPC=MICPC+1      ;SET IT IN LINE STATUS WORD
(1) 015120 063310      <MOVE!SPX!BR!AORB!SP10>
(1)
1787 015122 001456      SP      BR,SELB,SP15      ;RESET TIMER COUNT
(1)                      MICPC=MICPC+1
(1) 015122 063235      <MOVE!SPX!BR!SELB!SP15>
(1)
1788 015124 001457      ALWAYS TEOM1
(1)                      MICPC=MICPC+1
(1) 015124 110725      <JUMP!ALCOND!<TEOM1-INIT&3000*4>!<TEOM1-INIT&777/2>>
(1)
1789 015126 001460      ININT: BRWRT  IMM,15      ;MASK FOR TURN OFF ALL BUT EXT MEM BITS + NXM
(1)                      MICPC=MICPC+1
(1) 015126 000415      <MOVE!WRTBR!IMM!<15>>
(1)
1790 015130 001461      SP      IBUS,UBBR,SPO      ;READ BR CONTROL REGISTER
(1)                      MICPC=MICPC+1
(1) 015130 123220      <MOVE!SPX!IBUS!UBBR!SPO>
(1)
1791 015132 001462      SP      BR,AANDB,SPO      ;MASK OFF VECTOR TO X04
(1)                      MICPC=MICPC+1
(1) 015132 063260      <MOVE!SPX!BR!~<1>!SPO>
(1)
1792 015134 001463      BRWRT  IMM,200      ;MASK FOR INTERRUPT
(1)                      MICPC=MICPC+1
(1) 015134 000600      <MOVE!WRTBR!IMM!<200>>
(1)
1793 015136 001464      OUT      BR,AORB!OBR      ;INTERRUPT
(1)                      MICPC=MICPC+1
(1) 015136 061311      <MOVE!WROUTX!BR!<AORB!OBR>>
(1)
1794 015140 001465      SP      IBUS,INCON,SPO      ;RESTORE INPUT CONTROL CSR
(1)                      MICPC=MICPC+1

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F13

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHSH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-29
STACK HANDLER

PAGE: 015:

(1) 015140 123000
(1)
1795 015142
(1) 001466
(1) 015142 120554
(1)
1796

<MOVE!SPX!IBUS!INCON!SPD>

ALWAYS NIDLE4

MICPC=MICPC+1

<JUMP!ALCOND!<NIDLE4-INIT&3000*4>!<NIDLE4-INIT&777/2>>

:

1798		001	.IF DF SLOW	
1799			.SBTTL NXMERR ---NON EXISTANT MEMORY HANDLER	
1800			NXMERR: LDMA IMM,<<RTHRS+3>>	:ADDRESS ERROR LINK
1801			MEMINC IMM,1	
1802			MEM IMM,0	:NXM ERROR BIT
1803			SP MEMX,SELB,SP10	:CLEAR STATUS
1804			ALWAYS RCEXX	
1805			.PAGE	
1806		000	.ENDC	
1807			.FUGITIVE RECEIVE ROUTINES---DON'T FIT IN PAGE	
1808	015144		RH1: BRWRT IMM,77	
(1)		001467	MICPC=MICPC+1	
(1)	015144	000477	<MOVE!WRTBR!IMM!<77>>	
(1)				
1809	015146		SP BR,AANDB,SP5	
(1)		001470	MICPC=MICPC+1	
(1)	015146	063265	<MOVE!SPX!BR!AANDB!SP5>	
(1)				
1810	015150		LDMA BR,<INCA!SP14>	:LOAD ADDRESS OF CURRENT COUNT
(1)		001471	MICPC=MICPC+1	
(1)		001	.IF IDN BR,IMM	
(1)			<MOVE!LDMA!IMM!<INCA!SP14!377>>	
(1)			.IFF	
(1)	015150	070074	<MOVE!LDMA!BR!<INCA!SP14>>	
(1)		000	.ENDC	
(1)				
1811	015152		SP BR!INCMAR,SELB,SP0	:SAVE MASK
(1)		001472	MICPC=MICPC+1	
(1)	015152	077220	<MOVE!SPX!BR!INCMAR!SELB!SP0>	
(1)				
1812	015154		BRWRT BR!INCMAR,SELA!SP1	:READ STATUS BYTE
(1)		001473	MICPC=MICPC+1	
(1)	015154	074601	<MOVE!WRTBR!BR!INCMAR!<SELA!SP1>>	
(1)				
1813	015156		BRSHFT	:SHIFT IT RIGHT
(1)		001474	MICPC=MICPC+1	
(1)	015156	001620	<MOVE!SHFTBR!WRTBR!SELB>	
(1)				
1814	015160		BR1 RH2	:NO BUFFER ASSIGNED IN MAINT MODE
(1)		001475	MICPC=MICPC+1	
(1)	015160	116502	<JUMP!BR1CON!<RH2-INIT!3000*4>!<RH2-INIT!777/2>>	
(1)				
1815	015162		BRWRT MEMX!INCMAR,AANDB!SP0	:GET HIGH BYTE COUNT BITS
(1)		001476	MICPC=MICPC+1	
(1)	015162	054660	<MOVE!WRTBR!MEMX!INCMAR!<AANDB!SP0>>	
(1)				
1816	015164		CMP BR,SP5	:COMPARE HIGH ORDER BITS OF COUNT
(1)		001477	MICPC=MICPC+1	
(1)	015164	060365	<SUBTC!BR!SP5>	
(1)				
1817	015166		C RCFATL	:IF CARRY--TOO BIG ERROR
(1)		001500	MICPC=MICPC+1	
(1)	015166	115113	<JUMP!CCOND!<RCFATL-INIT!3000*4>!<RCFATL-INIT!777/2>>	
(1)				
1818	015170		Z RCLW	:IF EQUAL COMPARE LOW ORDER BITS OF COUNT
(1)		001501	MICPC=MICPC+1	

H13

DMC11 CDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-30
STACK HANDLER

PAGE: 0163

```
(1) 015170 11551C
(1)
1919 015172
(1) 001502
(1) 015172 020540
(1)
1920 015174
(1) 001503
(1) 015174 11510E
(1)
1921
(1) 001
1922
1923
1924 000
1925 015176
(1) 001504
(1) 015176 000660
1926 015200
(1) 001505
(1) 015200 100450
(1)
1927
1928 015202
(1) 001506
(1) 015202 000607
1929 015204
(1) 001507
(1) 015204 100450
(1)
1930
1931 015206
(1) 001510
(1) 015206 040364
(1)
1932 015210
(1) 001511
(1) 015210 115113
(1)
1933 015212
(1) 001512
(1) 015212 114502
(1)
1934 015214
(1) 001513
(1) 001
(1) 015214 010151
(1)
(1) 000
(1)
1935 015216
(1) 001514
(1) 015216 016432
(1)
1936 015220
(1) 001515
```

```
<JUMP!ZCOND!<RCLOW-INIT&3000*4>!<RCLOW-INIT&777/2>>

RH2: BRWRT IBUS,IOBA1 ;READ LOW BYTE OF IN BA
      MICPC=MICPC+1
      <MOVE!WRTBR!IBUS!<IOBA1>>

      BRO RCVODD ;IF SET IS ODD TRANSFER
      MICPC=MICPC+1
      <JUMP!BROCON!<RCVODD-INIT&3000*4>!<RCVODD-INIT&777/2>>

      .IF NDF LOW
      BRWRT IBUS,RCVCON ;IS THE RECEIVER READY?
      BR4 RCVKED ;YES--GO PROCESS
      .ENDC
      STATE RCVKED
      MICPC=MICPC+1
      <MOVE!WRTBR!IMM!<RCVKED-INIT&777/2>>
      ALWAYS REXIT
      MICPC=MICPC+1
      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

RCVODD: STATE RCVK01
        MICPC=MICPC+1
        <MOVE!WRTBR!IMM!<RCVK01-INIT&777/2>>
        ALWAYS REXIT
        MICPC=MICPC+1
        <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>

RCLOW: CMP MEMX,SP4 ;COMPARE LOW ORDER BITS OF COUNT
        MICPC=MICPC+1
        <SUBTC!MEMX!SP4>

        C RCFATL ;CARRY--TOC BIG
        MICPC=MICPC+1
        <JUMP!CCOND!<RCFATL-INIT&3000*4>!<RCFATL-INIT&777/2>>

        ALWAYS RH2 ;ELSE CONTINUE
        MICPC=MICPC+1
        <JUMP!ALCOND!<RH2-INIT&3000*4>!<RH2-INIT&777/2>>

RCFATL: LDMA IMM,T
        MICPC=MICPC+1
        .IF IDN IMM,IMM
        <MOVE!LDMAR!IMM!<T&377>>
        .IFF
        <MOVE!LDMAR!IMM!<T>>
        .ENDC

        MEMINC IMM,2
        MICPC=MICPC+1
        <MOVE!WRMEM!INCMAR!IMM!<2>>

        MEM IMM,311
        MICPC=MICPC+1
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(1) 015220 002711          <MOVE!WRMEM!IMM!<311>>
(1)
1837 015222          LDMA IMM,<<RTHRS+1>>          ;ADDRESS ERROR LINK
(1)          001516          MICPC=MICPC+1
(1)          001          .IF IDN IMM,IMM
(1) 015222 010175          <MOVE!LDMA!IMM!<<RTHRS+1>>377>>
(1)          .IFF
(1)          <MOVE!LDMA!IMM!<<RTHRS+1>>>
(1)          .ENDC
(1)          000
1838 015224          MEMINC IBUS,IOBA1
(1)          001517          MICPC=MICPC+1
(1) 015224 036540          <MOVE!WRMEM!INCMAR!IBUS!<IOBA1>>
(1)
1839 015226          MEMINC IBUS,IOBA2
(1)          001520          MICPC=MICPC+1
(1) 015226 036560          <MOVE!WRMEM!INCMAR!IBUS! IOBA2>>
(1)
1840 015230          BRWRT IMM,20
(1)          001521          MICPC=MICPC+1
(1) 015230 000420          <MOVE!WRTEBR!IMM!<20>>
(1)
1841 015232          RCEXY: MEMINC IMM,0
(1)          001522          MICPC=MICPC+1
(1) 015232 016400          <MOVE!WRMEM!INCMAR!IMM!<0>>
(1)
1842 015234          MEM BR,SELB
(1)          001523          MICPC=MICPC+1
(1) 015234 062620          <MOVE!WRMEM!BR!<SELB>>
(1)
1843 015236          RCEXX: OUTPUT IMM,<200!ORCVCO>          ;FLUSH INPUT SILC
(1)          001524          MICPC=MICPC+1
(1) 015236 002212          <MOVE!WROUT!IMM!<200!ORCVCO>>
(1)
1844 015240          SP IMM,SP2,2          ;INHIBIT FURTHER TRANSMISSIONS
(1)          001525          MICPC=MICPC+1
(1) 015240 003002          <MOVE!SPX!IMM!SP2!2>
(1)
1845 015242          SP IMM,1,SP1          ;SET INIT MODE IN PORT STATUS WORD
(1)          001526          MICPC=MICPC+1
(1) 015242 003001          <MOVE!SPX!IMM!1!SP1>
(1)
1846 015244          ALWAYS NTRS1
(1)          001527          MICPC=MICPC+1
(1) 015244 114666          <JUMP!ALCOND!<NTRS1-INIT$3000*4>!<NTRS1-INIT$777/2>>
(1)
1847 015246          TDON3: BRWRT MEMX,SUB!SP17          ;COMPARE RESPONSE TO MSG NO
(1)          001530          MICPC=MICPC+1
(1) 015246 040757          <MOVE!WRTEBR!MEMX!<SUB!SP17>>
(1)
1848 015250          BR7 RH3          ;IF NEGATIVE EXIT
(1)          001531          MICPC=MICPC+1
(1) 015250 107562          <JUMP!BR7CON!<RH3-INIT$3000*4>!<RH3-INIT$777/2>>
(1)
1849 015252          TDON2: LDMA BR,SELA!SPO          ;ADDRESS THE TRANSMITLINK
(1)          001532          MICPC=MICPC+1

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(1)          001          .IF IDN BR,IMM
(1)          .MOVE!LDMAR!IMM!<SELB!SP0&377>
(1)          .IFF
(1) 015252 07C200      .MOVE!LDMAR!BR!<SELB!SP0>
(1)          000          .ENDC
(1)
1850 015254          MEM      IMM,0          ;TURN OF ASSIGNEDAND TMED BITS IN FLAG
(1)          001533      MICPC=MICPC+1
(1) 015254 002400      <MOVE!WRMEM!IMM!<0>>
(1)
1851 015256          LDMA      IMM,STC
(1)          001534      MICPC=MICPC+1
(1)          001          .IF IDN IMM,IMM
(1) 015256 010067      <MOVE!LDMAR!IMM!<STC&377>
(1)          .IFF
(1)          <MOVE!LDMAR!IMM!<STC>>
(1)          000          .ENDC
(1)
1852 015260          MEM      IMM,TML1          ;ASSUME WRAPAROUND
(1)          001535      MICPC=MICPC+1
(1) 015260 002471      <MOVE!WRMEM!IMM!<TML1>>
(1)
1853 015262          BRWRT     IMM,TML8          ;WRAPAROUND?
(1)          001536      MICPC=MICPC+1
(1) 015262 000543      <MOVE!WRTEBR!IMM!<TML8>>
(1)
1854 015264          CMP      BR,SP0
(1)          001537      MICPC=MICPC+1
(1) 015264 060360      <SUBTC!BR!SP0>
(1)
1855 015266          Z      TDON4          ;YES
(1)          001540      MICPC=MICPC+1
(1) 015266 115543      <JUMP!ZCOND!<TDON4-INIT&3000*4>!<TDON4-INIT&777/2>>
(1)
1856 015270          BRWRT     IMM,6          ;OFFSET FOR NEXT TM? LINK
(1)          001541      MICPC=MICPC+1
(1) 015270 000406      <MOVE!WRTEBR!IMM!<6>>
(1)
1857 015272          MEM      BR,ADD!SP0          ;UPDATE THE POINTER
(1)          001542      MICPC=MICPC+1
(1) 015272 062400      <MOVE!WRMEM!BR!<ADD!SP0>>
(1)
1858 015274          TDON4: LDMA      IMM,NXTSP          ;ADDRESS DONE LINK
(1)          001543      MICPC=MICPC+1
(1)          001          .IF IDN IMM,IMM
(1) 015274 010241      <MOVE!LDMAR!IMM!<NXTSP&377>>
(1)          .IFF
(1)          <MOVE!LDMAR!IMM!<NXTSP>>
(1)          000          .ENDC
(1)
1859 015276          LDMA      MEMX,SELB!SPX!SP3          ;ADDRESS THE LINK,COPYING
(1)          001544      MICPC=MICPC+1
(1)          001          .IF IDN MEMX,IMM
(1)          <MOVE!LDMAR!IMM!<SELB!SPX!SP3&377>>
(1)          .IFF
(1) 015276 053223      <MOVE!LDMAR!MEMX!<SELB!SPX!SP3>>

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(1)          000          .ENDC
(1)
1860          :ITS ADDRESS TO SPO
1861 015300      MEMINC IMM,200      :WRITE THE INTERRUPT TYPE
(1)          MICPC=MICPC+1
(1) 015300      001545      <MOVE!WRMEM!INCMAR!IMM!<200>>
(1)          016600
(1)
1862 015302      MEM      BR,INCA!SPO      :COPY ACTUAL LINK ADDRESS
(1)          MICPC=MICPC+1
(1) 015302      001546      <MOVE!WRMEM!BR!<INCA!SPO>>
(1)          062460
(1)
1863 015304      LDMA      IMM,NXTSP      :ADDRESS PTR INT STACK
(1)          MICPC=MICPC+1
(1)          .IF IDN IMM,IMM
(1) 015304      001547      <MOVE!LDMAR!IMM!<NXTSP&377>>
(1)          001      .IFF
(1)          010241      <MOVE!LDMAR!IMM!<NXTSP>>
(1)          .ENDC
(1)          000
(1)
1864 015306      MEM      IMM,INTSTK      ;ASSUME WRAP AROUND
(1)          MICPC=MICPC+1
(1) 015306      001550      <MOVE!WRMEM!IMM!<INTSTK>>
(1)          002642
(1)
1865 015310      BRWRT IMM,<<MMEND-2>>      :ADDRESS ENDOFINT STACK
(1)          MICPC=MICPC+1
(1) 015310      001551      <MOVE!WRTBR!IMM!<<MMEND-2>>>
(1)          000776
(1)
1866 015312      CMP      BR,SP3      ;WRAPAROUND?
(1)          MICPC=MICPC+1
(1) 015312      001552      <SUBTC!BR!SP3>
(1)          060363
(1)
1867 015314      Z      TDON40      ;YES---BRANCH
(1)          MICPC=MICPC+1
(1) 015314      001553      <JUMP!ZCOND!<TDON40-INIT&3000*4>!<TDON40-INIT&777/2>>
(1)          115556
(1)
1868 015316      BRWRT IMM,2      :OFFSET TO NEXT PAIR
(1)          MICPC=MICPC+1
(1) 015316      001554      <MOVE!WRTBR!IMM!<2>>
(1)          000402
(1)
1869 015320      MEM      BR,ADD!SP3      :UPDATE POINTER
(1)          MICPC=MICPC+1
(1) 015320      001555      <MOVE!WRMEM!BR!<ADD!SP3>>
(1)          062403
(1)
1870 015322      TDON40: BRWRT IMM,20      ;WRITE INTERRUPT PENDING
(1)          MICPC=MICPC+1
(1) 015322      001556      <MOVE!WRTBR!IMM!<20>>
(1)          000420
(1)
1871 015324      SP      BR,AORB,SP1      :IN PORT STATUS WORD
(1)          MICPC=MICPC+1
(1) 015324      001557      <MOVE!SPX!BR!AORB!SP1>
(1)          063301
(1)
1872 015326      LDMA      IMM,ETC      :ADDRESS NEXT EMPTY PTR
(1)          MICPC=MICPC+1
(1)          .IF IDN IMM,IMM
(1) 015326      001560      <MOVE!LDMAR!IMM!<ETC&377>>
(1)          001      .IFF
(1)          010070

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(1)
(1)          000
(1)
(1)
1973 015330      SP      MEMX,SELB,SPO          ;COPY IT TO SPO
(1)          001561      MICPC=MICPC+1
(1) 015330      043220      <MOVE!SPX!MEMX!SELB!SPO>
(1)
1974 015332      LDMA     IMM,STC              ;GET NEXT DONE PTR
(1)          001562      MICPC=MICPC+1
(1)          001      .IF IDN IMM,IMM
(1) 015332      010067      <MOVE!LDMA!IMM!<STC&377>>
(1)          .IFF
(1)          <MOVE!LDMA!IMM!<STC>>
(1)          000      .ENDC
(1)
1975 015334      CMP      MEMX,SPO              ;IDENTICAL?
(1)          001563      MICPC=MICPC+1
(1) 015334      040360      <SUBTC!MEMX!SPO>
(1)
1976 015336      Z      RH3                      ;FINISH PROCESSING HEADER
(1)          001564      MICPC=MICPC+1
(1) 015336      105562      <JUMP!ZCOND!<RH3-INIT&3000*4>!<RH3-INIT&777/2>>
(1)
1977
1978 015340      TDON1: LDMA     IMM,ISP17          ;GET LAST ACKED
(1)          001565      MICPC=MICPC+1
(1)          001      .IF IDN IMM,IMM
(1) 015340      010153      <MOVE!LDMA!IMM!<ISP17&377>>
(1)          .IFF
(1)          <MOVE!LDMA!IMM!<ISP17>>
(1)          000      .ENDC
(1)
1979 015342      SP      MEMX,SELB,SP17          ;STORE IT IN SP17
(1)          001566      MICPC=MICPC+1
(1) 015342      043237      <MOVE!SPX!MEMX!SELB!SP17>
(1)
1980 015344      LDMA     IMM,STC              ;GET START OF TMT CHAIN
(1)          001567      MICPC=MICPC+1
(1)          001      .IF IDN IMM,IMM
(1) 015344      010067      <MOVE!LDMA!IMM!<STC&377>>
(1)          .IFF
(1)          <MOVE!LDMA!IMM!<STC>>
(1)          000      .ENDC
(1)
1981 015346      LDMA     MEMX,SELB!SPBRX!SPO      ;ADDRESS THE LINK
(1)          001570      MICPC=MICPC+1
(1)          001      .IF IDN MEMX,IMM
(1)          <MOVE!LDMA!IMM!<SELB!SPBRX!SPO&377>>
(1)          .IFF
(1) 015346      053620      <MOVE!LDMA!MEMX!<SELB!SPBRX!SPO>>
(1)          000      .ENDC
(1)
1982 015350      BRWRT  MEMX!INCMAR,SELB          ;GET THE FLAGS
(1)          001571      MICPC=MICPC+1
(1) 015350      054620      <MOVE!WRTBR!MEMX!INCMAR!<SELB>>
(1)

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1883 015352          BR1      TDON3                      ;IF BUFFER ASSIGNED PROCEED
      (1)            001572
      (1) 015352    116530          MICPC=MICPC+1
      (1)                                <JUMP!BR!CON!<TDON3-INIT&3000*4>!<TDON3-INIT&777/2>>
1884 015354          ALWAYS  RH3                      ;ELSE---EXIT
      (1)            001573          MICPC=MICPC+1
      (1) 015354    104562          <JUMP!ALCOND!<RH3-INIT&3000*4>!<RH3-INIT&777/2>>
      (1)
1885
1886 015356          OVRUN:  BRWRT  IMM,4
      (1)            001574          MICPC=MICPC+1
      (1) 015356    000404          <MOVE!WRTBR!IMM!<4>>
      (1)
1887 015360          ALWAYS  NTRSO
      (1)            001575          MICPC=MICPC+1
      (1) 015360    114663          <JUMP!ALCOND!<NTRSO-INIT&3000*4>!<NTRSO-INIT&777/2>>
      (1)
1888
1889
1890
1891
1892 015362          PASWRD: SP      IBUS, LNOSW, SP13      ;READ PASSWD SWITCH
      (1)            001576          MICPC=MICPC+1
      (1) 015362    023333          <MOVE!SPX!IBUS!LNOSW!SP13>
      (1)
1893 015364          Z      10$                      ;IF ALL ONES NO RLD ENABLED
      (1)            001577          MICPC=MICPC+1
      (1) 015364    115603          <JUMP!ZCOND!<10$-INIT&3000*4>!<10$-INIT&777/2>>
      (1)
1894 015366          BRWRT  IMM,6                      ;CHECK FOR ENTER MOP MODE
      (1)            001600          MICPC=MICPC+1
      (1) 015366    000406          <MOVE!WRTBR!IMM!<6>>
      (1)
1895 015370          CMP      BR, SPO
      (1)            001601          MICPC=MICPC+1
      (1) 015370    060360          <SUBTC!BR!SPO>
      (1)
1896 015372          Z      20$                      ;IF EQUAL ENTER MOP
      (1)            001602          MICPC=MICPC+1
      (1) 015372    115611          <JUMP!ZCOND!<20$-INIT&3000*4>!<20$-INIT&777/2>>
      (1)
1897 015374          10$:  BRWRT  BR, SELA!SP1          ;READ STATUS BYTE
      (1)            001603          MICPC=MICPC+1
      (1) 015374    060601          <MOVE!WRTBR!BR!<SELA!SP1>>
      (1)
1898 015376          BRSHFT
      (1)            001604          MICPC=MICPC+1          ;SHIFT IT RIGHT
      (1) 015376    001620          <MOVE!SHFTBR!WRTBR!SELB>
      (1)
1899 015400          BR1      RHX                      ;MESSAGE WITH NO BUFFER ASSIGNED
      (1)            001605          MICPC=MICPC+1
      (1) 015400    106740          <JUMP!BR!CON!<RHX-INIT&3000*4>!<RHX-INIT&777/2>>
      (1)
1900 015402          BRSHFT
      (1)            001606          MICPC=MICPC+1          ;SHIFT RIGHT AGAIN
      (1) 015402    001620          <MOVE!SHFTBR!WRTBR!SELB>

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(1)
1901 015404          BR1      RCVMD                      ;DLE RECEIVED IN NORMAL MODE
(1)          001607      MICPC=MICPC+1
(1) 015404 106732      <JUMP!BR1CON!<RCVMD-INIT&3000*4>!<RCVMD-INIT&777/2>>
(1)
1902 015406          ALWAYS  RK3                      ;HANDLE MAINT MODE MESSAGE
(1)          001610      MICPC=MICPC+1
(1) 015406 104641      <JUMP!ALCOND:<RK3-INIT&3000*4>!<RK3-INIT&777/2>>
(1)
1903 015410          20$:  SP      BR,DECA,SP4          ;COUNT FOR NUMB OF COMPARES
(1)          001611      MICPC=MICPC+1
(1) 015410 063164      <MOVE!SPX!BR!DECA!SP4>
(1)
1904 015412          STATE   EM2
(1)          001612      MICPC=MICPC+1
(1) 015412 000735      <MOVE!WRITEBR!IMM!<EM2-INIT&777/2>>
1905 015414          ALWAYS  REXIT
(1)          001613      MICPC=MICPC+1
(1) 015414 100450      <JUMP!ALCOND!<REXIT-INIT&3000*4>!<REXIT-INIT&777/2>>
(1)
1906
1907
1908
1909 015416          ;
(1)          001614      .ENABL  LSB
(1)          001          RCVMD1: LDMA      IMM,NAKST          ;RESET NAKS SENT
(1) 015416 010001      MICPC=MICPC+1
(1)          001          .IF  IDN IMM,IMM
(1)          001          <MOVE!LDMAR!IMM!<NAKST&377>>
(1)          001          .IFF
(1)          001          <MOVE!LDMAR!IMM!<NAKST>>
(1)          000          .ENDC
(1)
1910 015420          MEM      IMM,1                      ;...
(1)          001615      MICPC=MICPC+1
(1) 015420 002401      <MOVE!WRMEM!IMM!<1>>
(1)
1911 015422          LDMA      IMM,BC                      ;ADDRESS ORIGINAL RECV BYTE COUNT
(1)          001616      MICPC=MICPC+1
(1)          001          .IF  IDN IMM,IMM
(1) 015422 010167      <MOVE!LDMAR!IMM!<BC&377>>
(1)          001          .IFF
(1)          001          <MOVE!LDMAR!IMM!<BC>>
(1)          000          .ENDC
(1)
1912 015424          SP      MEMX!INCMAR,SELB,SP4        ;MOVE BYTE COUNT TO SP4
(1)          001617      MICPC=MICPC+1
(1) 015424 057224      <MOVE!SPX!MEMX!INCMAR!SELB!SP4>
(1)
1913 015426          SP      MEMX!INCMAR,SELB,SP5        ;AND SP5
(1)          001620      MICPC=MICPC+1
(1) 015426 057225      <MOVE!SPX!MEMX!INCMAR!SELB!SP5>
(1)
1914 015430          MEM      BR,DECA!SP11              ;COPY SP11 FROM MEMORY
(1)          001621      MICPC=MICPC+1
(1) 015430 062571      <MOVE!WRMEM!BR!<DECA!SP11>>
(1)
1915 015432          LDMA      IMM,NXTSP

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(1)		001622	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	015432	010241	<MOVE!LDMAR!IMM!<NXTSP&377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<NXTSP>>	
(1)		000	.ENDC	
1916	015434		SP MEMX!LDMAR,SELB,SP3	:COPY TO SP3
(1)		001623	MICPC=MICPC+1	
(1)	015434	053223	<MOVE!SPX!MEMX!LDMAR!SELB!SP3>	
1917	015436		MEMINC IMM,204	:RECEIVE DONE IMAGE
(1)		001624	MICPC=MICPC+1	
(1)	015436	016604	<MOVE!WRMEM!INCMAR!IMM!<204>>	
1918	015440		MEM BR!LDMAR,SELA!SP14	:COPY LINK ADDRESS TO NEXT INTER
(1)		001625	MICPC=MICPC+1	
(1)	015440	072614	<MOVE!WRMEM!BR!LDMAR!<SELA!SP14>>	
1919	015442		MEMINC IMM,0	:ZERO THE FLAGS
(1)		001626	MICPC=MICPC+1	
(1)	015442	016400	<MOVE!WRMEM!INCMAR!IMM!<0>>	
1920	015444		SP IMM!INCMAR,SPO,300	:WRITE A 300 TO SPO
(1)		001627	MICPC=MICPC+1	
(1)	015444	017300	<MOVE!SPX!IMM!INCMAR!SPO!300>	
1921	015446		BRWRT IMM!INCMAR,2	:PREPARE TO ADDRESS NEXT
(1)		001630	MICPC=MICPC+1	
(1)	015446	014402	<MOVE!WRTBR!IMM!INCMAR!<2>>	
1922				:INTERRUPT STACK AND INCREMENT
1923				:THE MAR
1924	015450		MEM MEMX,AANDB!SPO	:MASK OFF ORIGINAL HIGH BYTE
(1)		001631	MICPC=MICPC+1	
(1)	015450	042660	<MOVE!WRMEM!MEMX!<AANDB!SPO>>	
1925				:OF COUNT SAVING EXTENDED MEM BITS
1926	015452		MEMINC MEMX,AORB!SP5	:COPY TO MEMORY LINK
(1)		001632	MICPC=MICPC+1	
(1)	015452	056705	<MOVE!WRMEM!INCMAR!MEMX!<AORB!SP5>>	
1927	015454		MEMINC BR,SELA!SP4	
(1)		001633	MICPC=MICPC+1	
(1)	015454	076604	<MOVE!WRMEM!INCMAR!BR!<SELA!SP4>>	
1928	015456		LDMAR IMM,NXTSP	:ADDRESS NEXT INT STACK
(1)		001634	MICPC=MICPC+1	
(1)		001	.IF IDN IMM,IMM	
(1)	015456	010241	<MOVE!LDMAR!IMM!<NXTSP&377>>	
(1)			.IFF	
(1)			<MOVE!LDMAR!IMM!<NXTSP>>	
(1)		000	.ENDC	
1929	015460		MEM BR,ADD!SP3	
(1)		001635	MICPC=MICPC+1	

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(1) 015460 062403      <MOVE!WRMEM!BR!<ADD!SP3>>
(1)
1930 015462      BRWRT IMM,<<MMEND-2>>      :ADDRESSEND OF INT STACK
(1)      MICPC=MICPC+1
(1) 015462 001636      <MOVE!WRTEBR!IMM!<<MMEND-2>>>
(1)      000776
1931 015464      CMP      BR,SP3      ;WRAP AROUND
(1)      MICPC=MICPC+1
(1) 015464 060363      <SUBTC!BR!SP3>
(1)
1932 015466      Z      40$      ;IF YES-- BRANCH
(1)      MICPC=MICPC+1
(1) 015466 115651      <JUMP!ZCOND!<40$-INIT&3000*4>!<40$-INIT&777/2>>
(1)
1933 015470      20$:      BRWRT IMM,5      :INDEX TO NEXT BUFFER
1934 015470      MICPC=MICPC+1
(1) 015470 001641      <MOVE!WRTEBR!IMM!<5>>
(1)      000405
1935 015472      SP      BR,ADD,SP14      ;UPDATE COPY OF POINTER
(1)      MICPC=MICPC+1
(1) 015472 063014      <MOVE!SPX!BR!ADD!SP14>
(1)
1936 015474      BRWRT IMM,STC      :ADDRESS OF WRAP AROUND POINT
(1)      MICPC=MICPC+1
(1) 015474 001643      <MOVE!WRTEBR!IMM!<STC>>
(1)      000467
1937 015476      CMP      BR,SP14      ;WRAPAROUND?
(1)      MICPC=MICPC+1
(1) 015476 060374      <SUBTC!BR!SP14>
(1)
1938 015500      Z      50$      ;IF YES---BRANCH
(1)      MICPC=MICPC+1
(1) 015500 115653      <JUMP!ZCOND!<50$-INIT&3000*4>!<50$-INIT&777/2>>
(1)
1939 015502      30$:      BRWRT IMM,20      ;MASK FOR INTERRUPT PENDING
(1)      MICPC=MICPC+1
(1) 015502 001646      <MOVE!WRTEBR!IMM!<20>>
(1)      000420
1940 015504      SP      DP,AORB,SP1      ;UPDATE PORT STATUS WORD
(1)      MICPC=MICPC+1
(1) 015504 063301      <MOVE!SPX!DP!AORB!SP1>
(1)
1941      001
1942      .IF DF SLOW
1943      BRWRT DP,<SELA!SP10>      :READ LINE STATUS WORD
1944      BR4      FLUSH      :IF CLEAR ACTIVE SET---FLUSH
1945      STATE      RCVA
1946      ALWAYS      REXIT
1947      .ENDC
1948      .IF NDF SLOW
1949      ALWAYS      FLUSH
(1)      MICPC=MICPC+1
(1) 015506 104415      <JUMP!ALCOND!<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>
(1)
1949      .ENDC
1950 015510      40$:      MEM      IMM,INTSTK      ;POINT TO START OF INTERRUPT STACK

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(1) 015510 001651 MICPC=MICPC+1
(1) 015510 002642 <MOVE!WRMEM!IMM!<INTSTK>>
(1) 1951 015512 ALWAYS 20$
(1) 015512 001652 MICPC=MICPC+1
(1) 015512 114641 <JUMP!ALCOND!<20$-INIT&3000*4>!<20$-INIT&777/2>>
(1) 1952 015514 SOS: BRWRT IMM,RCL1 ;POINT TO START OF RECEIVE QUEUE
(1) 015514 001653 MICPC=MICPC+1
(1) 015514 000424 <MOVE!WRTEBR!IMM!<RCL1>>
(1) 1953 015516 SP BR,SELB,SP14
(1) 015516 001654 MICPC=MICPC+1
(1) 015516 063234 <MOVE!SPX!BR!SELB!SP14>
(1) 1954 015520 ALWAYS 30$
(1) 015520 001655 MICPC=MICPC+1
(1) 015520 114646 <JUMP!ALCOND!<30$-INIT&3000*4>!<30$-INIT&777/2>>
(1) 1955 015522 NTHRES: .DSABL LSB
(1) 015522 001656 LDMA IMM,ST
(1) 001 MICPC=MICPC+1
(1) 015522 010152 .IF IDN IMM,IMM
(1) <MOVE!LDMA!IMM!<ST&377>>
(1) .IFF
(1) <MOVE!LDMA!IMM!<ST>>
(1) .ENDC
(1) 000
(1) 1957 015524 SPBR MEMX,SELB,SP0
(1) 015524 001657 MICPC=MICPC+1
(1) 015524 043620 <MOVE!SPBRX!MEMX!SELB!SP0>
(1) 1958 015526 BRWRT BR,ADD!SP0 ;SHIFT LEFT
(1) 015526 001660 MICPC=MICPC+1
(1) 015526 060400 <MOVE!WRTEBR!BR!<ADD!SP0>>
(1) 1959 015530 BR4 OVRUN
(1) 015530 001661 MICPC=MICPC+1
(1) 015530 117174 <JUMP!BR4CON!<OVRUN-INIT&3000*4>!<OVRUN-INIT&777/2>>
(1) 1960 015532 BRWRT IMM,1
(1) 015532 001662 MICPC=MICPC+1
(1) 015532 000401 <MOVE!WRTEBR!IMM!<1>>
(1) 1961 015534 ERRXX:
(1) 1962 015534 NTRSO: LDMA IMM,<<RTHRS+3>>
(1) 001 MICPC=MICPC+1
(1) 015534 010177 .IF IDN IMM,IMM
(1) <MOVE!LDMA!IMM!<<RTHRS+3>&377>>
(1) .IFF
(1) <MOVE!LDMA!IMM!<<RTHRS+3>>>
(1) .ENDC
(1) 000
(1) 1963 015536 MEMINC IMM,0
(1) 015536 001664 MICPC=MICPC+1
(1) 015536 016400 <MOVE!WRMEM!INCMAR!IMM!<0>>

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(1)	1964	015540		MEM BR,SELB	
(1)			001665	MICPC=MICPC+1	
(1)		015540	062620	<MOVE!WRMEM!BR!<SELB>>	
(1)	1965	015542		NTRS1: LDMA IMM,NXTSP	
(1)			001666	MICPC=MICPC+1	
(1)			001	.IF IDN IMM,IMM	
(1)		015542	010241	<MOVE!LDMAR!IMM!<NXTSP&377>>	
(1)				.IFF	
(1)				<MOVE!LDMAR!IMM!<NXTSP>>	
(1)			000	.ENDC	
(1)	1966	015544		LDMA MEMX,SELB!SPX!SP0	
(1)			001667	MICPC=MICPC+1	
(1)			001	.IF IDN MEMX,IMM	
(1)				<MOVE!LDMAR!IMM!<SELB!SPX!SP0&377>>	
(1)				.IFF	
(1)		015544	053220	<MOVE!LDMAR!MEMX!<SELB!SPX!SP0>>	
(1)			000	.ENDC	
(1)	1967	015546		MEMINC IMM,201	
(1)			001670	MICPC=MICPC+1	
(1)		015546	016601	<MOVE!WRMEM!INCMAR!IMM!<201>>	
(1)	1968	015550		MEM IMM,<<RTHRS>>	
(1)			001671	MICPC=MICPC+1	
(1)		015550	002574	<MOVE!WRMEM!IMM!<<RTHRS>>>	
(1)	1969	015552		LDMA IMM,NXTSP	
(1)			001672	MICPC=MICPC+1	
(1)			001	.IF IDN IMM,IMM	
(1)		015552	010241	<MOVE!LDMAR!IMM!<NXTSP&377>>	
(1)				.IFF	
(1)				<MOVE!LDMAR!IMM!<NXTSP>>	
(1)			000	.ENDC	
(1)	1970	015554		MEM IMM,INTSTK	:ASSUME QUEUE WRAP AROUND
(1)			001673	MICPC=MICPC+1	
(1)		015554	002642	<MOVE!WRMEM!IMM!<INTSTK>>	
(1)	1971	015556		BRWRT IMM,<<MMEND-2>>	
(1)			001674	MICPC=MICPC+1	
(1)		015556	001676	<MOVE!WRTEBR!IMM!<<MMEND-2>>	
(1)	1972	015560		CMP BR,SP0	
(1)			001675	MICPC=MICPC+1	
(1)		015560	060360	<SUBTC!BR!SP0>	
(1)	1973	015562		Z NTRS2	:IT DID WRAP AROUND
(1)			001676	MICPC=MICPC+1	
(1)		015562	115701	<JUMP!ZCOND!<NTRS2-INIT&3000*4>!<NTRS2-INIT&377/2>>	
(1)	1974	015564		BRWRT IMM,2	:OFFSET TO NEXT PAIR
(1)			001677	MICPC=MICPC+1	
(1)		015564	000402	<MOVE!WRTEBR!IMM!<2>>	

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(1)
1975 015566 001700 MEM BR,ADD!SP0 ;UPDATE QUEUE POINTER
(1) 015566 062400 MICPC=MICPC+1
(1) <MOVE!WRMEM!BR!<ADD!SP0>>
1976 015570 NTRS2: BRWRT IMM,20
(1) 001701 MICPC=MICPC+1
(1) 000420 <MOVE!WRTEBR!IMM!<20>>
1977 015572 SPBR BR,AORB,SP1
(1) 001702 MICPC=MICPC+1
(1) 063701 <MOVE!SPBRX!BR!AORB!SP1>
1978 015574 BRO TAB1 ;FLAGGED BY ERROR TYPE
(1) 001703 MICPC=MICPC+1
(1) 116334 <JUMP!BROCON!<TAB1-INIT&3000*4>!<TAB1-INIT&777/2>>
1979 015576 SNAK: LDMA IMM,ISP11
(1) 001704 MICPC=MICPC+1
(1) 001 .IF IDN IMM,IMM
(1) 015576 010171 <MOVE!LDMA!IMM!<ISP11&377>>
(1) .IFF
(1) <MOVE!LDMA!IMM!<ISP11>>
(1) .ENDC
(1) 000
1980 015600 SP MEMX,SELB,SP11
(1) 001705 MICPC=MICPC+1
(1) 043231 <MOVE!SPX!MEMX!SELB!SP11>
1981 015602 SP BR,INCA,SP11 ;INCREMENT MSG EXPECTED
(1) 001706 MICPC=MICPC+1
(1) 063071 <MOVE!SPX!BR!INCA!SP11>
1982 015604 SNAK1: BRWRT IMM,1 ;UNNUMB PENING BIT TO BR
(1) 001707 MICPC=MICPC+1
(1) 000401 <MOVE!WRTEBR!IMM!<1>>
1983 015606 SNAK2: SP BR,AORB,SP10 ;UPDATE LINE STATUS WORD
(1) 001710 MICPC=MICPC+1
(1) 063310 <MOVE!SPX!BR!AORB!SP10>
1984 015610 ALWAYS FLUSH
(1) 001711 MICPC=MICPC+1
(1) 104415 <JUMP!ALCOND!<FLUSH-INIT&3000*4>!<FLUSH-INIT&777/2>>
1985
1986 015612 EMTRIG: BRWRT IMM,24
(1) 001712 MICPC=MICPC+1
(1) 000424 <MOVE!WRTEBR!IMM!<24>>
1987 015614 OUTPUT BR,<SELB!OBA1>
(1) 001713 MICPC=MICPC+1
(1) 062226 <MOVE!WROUT!BR!<SELB!OBA1>>
1988 015616 BRWRT IMM,0
(1) 001714 MICPC=MICPC+1

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(1) 015616 000400          <MOVE!WRTEBR!IMM!<0>>
(1)
1989 015620          OUTPUT BR,<SELB!OBA2>
(1) 001715          MICPC=MICPC+1
(1) 015620 062227          <MOVE!WROUT!BR!<SELB!OBA2>>
(1)
1990 015622          SPBR IBUS,BM873,SP0          :READ BM873 ADDRESS---
(1) 001716          MICPC=MICPC+1
(1) 015622 023740          <MOVE!SPBRX!IBUS!BM873!SP0>
(1)
1991 015624          OUTPUT BR,SELB!OUTDA1          :SET UP LOW BYTE OF ADDRESS
(1) 001717          MICPC=MICPC+1
(1) 015624 062222          <MOVE!WROUT!BR!<SELB!OUTDA1>>
(1)
1992 015626          BRWRT IMM,366          :HIGH BYTE BASE FOR ROM BOOT
(1) 001720          MICPC=MICPC+1
(1) 015626 000766          <MOVE!WRTEBR!IMM!<366>>
(1)
1993 015630          OUTPUT BR,SELB!OUTDA2          :
(1) 001721          MICPC=MICPC+1
(1) 015630 062223          <MOVE!WROUT!BR!<SELB!OUTDA2>>
(1)
1994 015632          EM6: BRWRT IMM,21          ;MASK FOR TIMER AND ALSO TO START NPR
(1) 001722          MICPC=MICPC+1
(1) 015632 000421          <MOVE!WRTEBR!IMM!<21>>
(1)
1995 015634          OUT BR,<SELB!OBR>
(1) 001723          MICPC=MICPC+1
(1) 015634 061231          <MOVE!WROUTX!BR!<SELB!OBR>>
(1)
1996 015636          OUT BR,<SELB!ONPR>
(1) 001724          MICPC=MICPC+1
(1) 015636 061230          <MOVE!WROUTX!BR!<SELB!ONPR>>
(1)
1997 015640          EM1: BRWRT IBUS,NPR          :READ NPR CONTROL
(1) 001725          MICPC=MICPC+1
(1) 015640 120600          <MOVE!WRTEBR!IBUS!<NPR>>
(1)
1998 015642          BRO CKTIME
(1) 001726          MICPC=MICPC+1
(1) 015642 132371          <JUMP!BROCON!<CKTIME-INIT$3000*4>!<CKTIME-INIT$777/2>>
(1)
1999 015644          MEMADR RM1          :IF NPR DONE
(1) 001727          MICPC=MICPC+1
(1) 001          .IF B
(1) 015644 002420          <MOVE!WRMEM!<RM1-INIT$777/2>>
(1)          .IFF
(1)          <MOVE!WRMEM!!<RM1-INIT$777/2>>
(1)          .ENDC
2000 015646          ALWAYS ACLOW
(1) 001730          MICPC=MICPC+1
(1) 015646 100764          <JUMP!ALCOND!<ACLOW-INIT$3000*4>!<ACLOW-INIT$777/2>>
(1)
2001 015650          TABUPD: SPBR IBUS,RCVCON,SP0          :READ RECEIVER CONTROL REG
(1) 001731          MICPC=MICPC+1
(1) 015650 023640          <MOVE!SPBRX!IBUS!RCVCON!SP0>

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(1)
2002 015652      001732      BRWRT  BR,ADD!SP0      :SHIFT LEFT
(1)      015652      060400      MICPC=MICPC+1
(1)      015652      060400      <MOVE!WRTBR!BR!<ADD!SP0>>
(1)
2003 015654      001733      BR7      IDLE      :RECEIVE ACTIVE--IDLE
(1)      015654      103451      MICPC=MICPC+1
(1)      015654      103451      <JUMP!BR7CON!<IDLE-INIT&3000*4>!<IDLE-INIT&777/2>>
(1)
2004 015656      001734      TAB1:  LDMA      IMM,IMG10
(1)      015656      001734      MICPC=MICPC+1
(1)      015656      010154      .IF IDN IMM,IMM
(1)      015656      010154      <MOVE!LDMA!IMM!<IMG10&377>>
(1)      015656      010154      .IFF
(1)      015656      010154      <MOVE!LDMA!IMM!<IMG10>>
(1)      015656      010154      .ENDC
(1)      015656      000
(1)
2005 015660      001735      BRWRT  IMM,2
(1)      015660      000402      MICPC=MICPC+1
(1)      015660      000402      <MOVE!WRTBR!IMM!<2>>
(1)
2006 015662      001736      MEMINC  BR,AANDB!SP10      :SAVE BIT 1 OF SP10
(1)      015662      076670      MICPC=MICPC+1
(1)      015662      076670      <MOVE!WRMEM!INCMAR!BR!<AANDB!SP10>>
(1)
2007 015664      001737      MEMINC  BR,SELA!SP11      :SAVE SP11
(1)      015664      076611      MICPC=MICPC+1
(1)      015664      076611      <MOVE!WRMEM!INCMAR!BR!<SELA!SP11>>
(1)
2008 015666      001740      MEMINC  BR,SELA!SP12      :SAVE SP12
(1)      015666      076612      MICPC=MICPC+1
(1)      015666      076612      <MOVE!WRMEM!INCMAR!BR!<SELA!SP12>>
(1)
2009 015670      001741      MEMINC  BR,SELA!SP14      :SAVE SP14
(1)      015670      076614      MICPC=MICPC+1
(1)      015670      076614      <MOVE!WRMEM!INCMAR!BR!<SELA!SP14>>
(1)
2010 015672      001742      MEMINC  BR,SELA!SP16      :SAVE SP16
(1)      015672      076616      MICPC=MICPC+1
(1)      015672      076616      <MOVE!WRMEM!INCMAR!BR!<SELA!SP16>>
(1)
2011 015674      001743      MEMINC  BR,SELA!SP17      :SAVE SP17
(1)      015674      076617      MICPC=MICPC+1
(1)      015674      076617      <MOVE!WRMEM!INCMAR!BR!<SELA!SP17>>
(1)
2012 015676      001744      STATE  RB2      :MAR NOW POINTS TO BASE
2013 015676      000460      MICPC=MICPC+1      ;DO NOT CHANGE BR UNTIL RBO
(1)      015676      000460      <MOVE!WRTBR!IMM!<RB2-INIT&777/2>>
(1)      015700      001745      LDMA      IMM,TABST      :POINT TO TABLE UPDATE STATE
(1)      015700      001745      MICPC=MICPC+1
(1)      015700      001745      .IF IDN IMM,IMM
(1)      015700      010210      <MOVE!LDMA!IMM!<TABST&377>>
(1)      015700      010210      .IFF
(1)      015700      010210      <MOVE!LDMA!IMM!<TABST>>
(1)      015700      010210      .ENDC
(1)

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(1) 2015 015702 PSTATE TBUI ;NEW PORT STATE ADDRESS
(1) 015702 MEM IMM,<<TBUI-INIT&777/2>>
(1) 001746 MICPC=MICPC+1
(1) 015702 002774 <MOVE!WRMEM!IMM!<<TBUI-INIT&777/2>>>
(1)
2016 015704 SP IMM,4,SP4 ;INITIALIZE COUNT
(1) 001747 MICPC=MICPC+1
(1) 015704 003004 <MOVE!SPX!IMM!4!SP4>
(1)
2017 ;NOTE: FIRST 6 RAM LOCATIONS ARE NOT WRITTEN
2018 ;TO CORE TABLE.
2019 015706 LDMA IMM,BASE
(1) 001750 MICPC=MICPC+1
(1) 001 IF IDN IMM,IMM
(1) 015706 010017 <MOVE!LDMA!IMM!<BASE&377>>
(1) .IFF
(1) <MOVE!LDMA!IMM!<BASE>>
(1) .ENDC
(1) 000
2020 015710 ALWAYS RBO
(1) 001751 MICPC=MICPC+1
(1) 015710 104442 <JUM:ALCOND!<RBO-INIT&3000*4>!<RBO-INIT&777/2>>
(1)
2021 015712 EC2: BRWRT IMM,2 ;INCREMENT COUNT/TEST
(1) 001752 MICPC=MICPC+1
(1) 015712 000402 <MOVE!WRTEBR!IMM!<2>>
(1)
2022 015714 SP BR,ADD,SP4
(1) 001753 MICPC=MICPC+1
(1) 015714 063004 <MOVE!SPX!BR!ADD!SP4>
(1)
2023 015716 SP IBUS IOBA1,SP0 ;POINT TO NEXT ADDRESS
(1) 001754 MICPC=MICPC+1
(1) 015716 023140 <MOVE!SPX!IBUS!IOBA1!SP0>
(1)
2024 015720 OUTPUT BR,ADD!OBA1
(1) 001755 MICPC=MICPC+1
(1) 015720 062006 <MOVE!WROUT!BR!<ADD!OBA1>>
(1)
2025 015722 SP IBUS IOBA2,SP0
(1) 001756 MICPC=MICPC+1
(1) 015722 023160 <MOVE!SPX!IBUS!IOBA2!SP0>
(1)
2026 015724 OUTPUT BR,AC!OBA2
(1) 001757 MICPC=MICPC+1
(1) 015724 062107 <MOVE!WROUT!BR!<AC!OBA2>>
(1)
2027 015726 C TABMXT
(1) 001760 MICPC=MICPC+1
(1) 015726 105366 <JUMP!CCOND!<TABMXT-INIT&3000*4>!<TABMXT-INIT&777/2>>
(1)
2028 015730 ECX: BRWRT BR,SELA!SP1 ;READ PORT STATUS
(1) 001761 MICPC=MICPC+1
(1) 015730 060601 <MOVE!WRTEBR!BR!<SELA!SP1>>

```

2029	015732		BRO 30\$	: INIT MODE, WRITE OUT 200 BYTES
(1)		001762	MICPC=MICPC+1	
(1)	015732	116374	<JUMP! BROCON! <30\$-INIT&3000*4>! <30\$-INIT&777/2>>	
2030				: OTHERWISE ONLY WRITE OUT ERROR COUNTERS
2031	015734		BRWRITE BR! LDMA, SELA! SP4	: READ COUNTER
(1)		001763	MICPC=MICPC+1	
(1)	015734	070604	<MOVE! WRTEBR! BR! LDMA! <SELA! SP4>>	
2032	015736		BR4 JS	: ALL DONE
(1)		001764	MICPC=MICPC+1	
(1)	015736	117371	<JUMP! BR4CON! <20\$-INIT&3000*4>! <20\$-INIT&777/2>>	
2033	015740		10\$: OUTPUT MEMX! INCMAR, SELB! OUTDA1	: STORE COUNTS OF ERRORS
(1)		001765	MICPC=MICPC+1	
(1)	015740	056222	<MOVE! WROUT! MEMX! INCMAR! <SELB! OUTDA1>>	
2034	015742		OUTPUT MEMX! INCMAR, SELB! OUTDA2	
(1)		001766	MICPC=MICPC+1	
(1)	015742	056223	<MOVE! WROUT! MEMX! INCMAR! <SELB! OUTDA2>>	
2035		001	.IF NDF \$LOW	
2036	015744		SP IBUS, NPR, SPO	
(1)		001767	MICPC=MICPC+1	
(1)	015744	123200	<MOVE! SPX! IBUS! NPR! SPO>	
2037		000	.ENDC	
2038	015746		ALWAYS RK8	
(1)		001770	MICPC=MICPC+1	
(1)	015746	104622	<JUMP! ALCOND! <RK8-INIT&3000*4>! <RK8-INIT&777/2>>	
2039	015750		20\$: LDMA IMM, TABS	
(1)		001771	MICPC=MICPC+1	
(1)		001	.IF IDN IMM, IMM	
(1)	015750	010210	<MOVE! LDMA! IMM! <TABST&377>>	
(1)			.IFF	
(1)			<MOVE! LDMA! IMM! <TABST>>	
(1)		000	.ENDC	
2040	015752		PSTATE I3	
(1)	015752		MEM IMM, <<I3-INIT&777/2>>	
(2)		001772	MICPC=MICPC+1	
(2)	015752	002460	<MOVE! WRMEM! IMM! <<I3-INIT&777/2>>>	
2041	015754		ALWAYS RM1	
(1)		001773	MICPC=MICPC+1	
(1)	015754	104420	<JUMP! ALCOND! <RM1-INIT&3000*4>! <RM1-INIT&777/2>>	
2042	015756		30\$: BRWRITE BR! LDMA, SELA! SP4	: READ COUNTER
(1)		001774	MICPC=MICPC+1	
(1)	015756	070604	<MOVE! WRTEBR! BR! LDMA! <SELA! SP4>>	
2043	015760		BR7 20\$	: ALL DONE
(1)		001775	MICPC=MICPC+1	
(1)	015760	117771	<JUMP! BR7CON! <20\$-INIT&3000*4>! <20\$-INIT&777/2>>	

K14

DMC11 DDCMP PROTOCOL IMPLEMENTATION
DDCHGH.MAC 06-DEC-76 11:34

MACY11 27(1006) 14-DEC-76 16:44 PAGE 8-46
STACK HANDLER

PAGE: 0179

2044	015762		ALWAYS 10\$	;KEEP GOING
(1)		001776	MICPC=MICPC+1	
(1)	015762	114765	<JUMP!ALCOND!<10\$-INIT&3000*4>!<10\$-INIT&777/2>>	
(1)				
2045	015764		\$ZERO	
(1)		001777	MICPC=MICPC+1	
(1)	015764	000000	000000	
(1)				
2046			:	
2047		000001	.END	

.ABS. 015766 000

ERRORS DETECTED: 0
DEFAULT GLOBALS GENERATED: 0

DDCMP/CRF/DS:CRF+DMCHGH,HILOW,DDCHGH
RUN-TIME: 16 31 .1 SECONDS
RUN-TIME RATIO: 189/48=3.8
CORE USED: 7K (13 PAGES)

1623				00200
1624				
1625				
1626				
1627				
1628				
1629				
1630				
1631				
1632				
1633				
1634	015766	012737	000001	001226
1635	015774	012737	016100	001216
1636				
1637	016002	104412		

```

***** TEST 1 *****
;*TEST OF BR RIGHT SHIFT
;*VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION
;*SHIFTS THE RESULTING BR DATA RIGHT ONCE.
*****

; TEST 1
-----
TST1: MOV     #1,TSTNO
      MOV     #TST2,NEXT
      MSTCLR
;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11

```

L14

DZCMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 35
DZCMH.P11 09-DEC-76 14:59 GENERAL UTILITIES (TYPEOUT, ERROR, SCOPE, ETC)

PAGE: 0180

1638	016004	013701	001404		MOV	DMCSR,R1	;R1 = DMC BASE ADDRESS
1639	016010	005011			CLR	(R1)	;CLEAR SEL0
1640	016012	012705	052525		MOV	#52525,R5	;START WITH 125
1641	016016	010561	000004		MOV	R5,4(R1)	;PORT4+125
1642	016022	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1643	016024	120500			120500		;BR + PORT4
1644	016026	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1645	016030	061620			061620		;BR RSH+BR, SHIFT BR RIGHT
1646	016032	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1647	016034	061225			061225		;PORT5+BR
1648	016036	006005			ROR	R5	;R5 = "EXPECTED"
1649	016040	116104	000005		MOVB	5(R1),R4	;R4 = "FOUND"
1650	016044	120504			CMPB	R5,R4	;DID BR SHIFT RIGHT ONCE?
1651	016046	001401			BEQ	1\$	;BR IF YES
1652	016050	104012			HLT	12	;BR RIGHT SHIFT ERROR
1653	016052			1\$:			
1654	016052	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1655	016054	061620			061620		;BR RSH+BR, SHFT BR RIGHT AGAIN
1656	016056	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1657	016060	061225			061225		;PORT5+BR
1658	016062	006005			ROR	R5	;R5 = "EXPECTED"
1659	016064	116104	000005		MOVB	5(R1),R4	;R4 = "FOUND"
1660	016070	120504			CMPB	R5,R4	;DID BR SHIFT RIGHT?
1661	016072	001401			BEQ	2\$	;BR IF YES
1662	016074	104012			HLT	12	;BR RIGHT SHIFT ERROR
1663	016076	104400		2\$:	SCOPE		;SCOPE THIS TEST
1664							
1665							
1666							
1667							
1668							
1669							
1670							
1671							
1672							
1673	016100	012737	000002	001226	TST2:	MOV	#2,TSTNO
1674	016106	012737	016214	001216		MOV	#TST3,NEXT
1675	016114	012737	016140	001220		MOV	#3\$,LOCK
1676							
1677	016122	032737	100000	001366		BIT	#BIT15,STAT1
1678	016130	001430				BEQ	5\$
1679	016132	005000				CLR	R0
1680	016134	012702	000001		1\$:	MOV	#1,R2
1681	016140				2\$:		
1682	016140	012711	002008		3\$:	MOV	#BIT10,(R1)
1683	016144	010061	000004			MOV	R0,4(R1)
1684	016150	010261	000006			MOV	R2,6(R1)
1685	016154	052711	020000			BIS	#BIT13,(R1)
1686	016160	016104	000004			MOV	4(R1),R4
1687	016164	020204				CMP	R2,R4
1688	016166	001401				BEQ	4\$
1689	016170	104001				HLT	1
1690	016172	104401			4\$:	SCOP1	
1691	016174	000241				CLC	
1692	016176	006102				ROL	R2
1693	016200	001357				BNE	2\$

***** TEST 2 *****
;IOP CRAM WRITE/READ TEST
;FLOAT A 1 THROUGH EACH CRAM LOCATION

; TEST 2

;R1 CONTAINS BASE DMC11 ADDRESS
;DOES DMC HAVE CRAM?
;SKIP TEST IF NO CRAM
;R0 = CRAM ADDRESS
;R2 = WRITE DATA
;SET ROM0
;WRITE ADDRESS TO SEL4
;LOAD SEL6 WITH WRITE DATA
;WRITE SEL6 INTO CRAM
;READ CRAM INTO "FOUND"
;IS DATA CORRECT?
;BR IF OK
;ERROR
;CLEAR CARRY
;SHIFT WRITE DATA
;BR IF NOT DONE THIS ADDRESS

M14

DZDMH MACY11 27(1006) 14-DEC-76 16:32 PAGE 36
 DZDMH.P11 09-DEC-76 14:59 CRAM WRITE/READ TESTS

PAGE: 0181

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1694 016202 005200      INC      R0      ;BUMP TO NEXT CRAM ADDRESS
1695 016204 022700 002000  CMP      #2000,R0      ;DONE YET?
1696 016210 001351      BNE      1$      ;BR IF NO
1697 016212 104400      5$:      SCOPE      ;SCOPE THIS TEST
1698
1699
1700      ;***** TEST 3 *****
1701      ;*IOP CRAM WRITE/READ TEST
1702      ;*FLOAT A 0 THROUGH EACH CRAM LOCATION
1703      ;*****
1704
1705      ; TEST 3
1706      ;-----
1707 016214 012737 000003 001226  TST3:  MOV      #3,TSTNO
1708 016222 012737 016336 001216      MOV      #TST4,NEXT
1709 016230 012737 016260 001220      MOV      #3$,LOCK
1710
1711 016236 104412      MSTCLR      ;R1 CONTAINS BASE DMC11 ADDRESS
1712 016240 032737 100000 001366      BIT      #BIT15,STAT1 ;MASTER CLEAR DMC11
1713 016246 001432      BEQ      5$      ;YES DMC HAVE CRAM?
1714 016250 005000      CLR      R0      ;SKIP TEST IF NO CRAM
1715 016252 012702 000001      1$:  MOV      #1,R2      ;R0 = CRAM ADDRESS
1716 016256      2$:      ;R2 = WRITE DATA
1717 016256 005102      COM      R2      ;MAKE IT A FLOATING ZERO
1718 016260 012711 002000      3$:  MOV      #BIT10,(R1) ;SET ROM0
1719 016264 010061 000004      MOV      R0,4(R1) ;WRITE ADDRESS TO SEL4
1720 016270 010261 000006      MOV      R2,6(R1) ;LOAD SEL6 WITH WRITE DATA
1721 016274 052711 020000      BIS      #BIT13,(R1) ;WRITE SEL6 INTO CRAM
1722 016300 016104 000004      MOV      4(R1),R4 ;READ CRAM INTO "FOUND"
1723 016304 020204      CMP      R2,R4      ;IS DATA CORRECT?
1724 016306 001401      BEQ      4$      ;BR IF OK
1725 016310 104001      HLT      1      ;ERROR
1726 016312 104401      4$:  SCOP1
1727 016314 005102      COM      R2      ;BACK TO FLOATING ONE
1728 016316 000241      CLC      ;CLEAR CARRY
1729 016320 006102      ROL      R2      ;SHIFT WRITE DATA
1730 016322 001355      BNE      2$      ;BR IF NOT DONE THIS ADDRESS
1731 016324 005200      INC      R0      ;BUMP TO NEXT CRAM ADDRESS
1732 016326 022700 002000      CMP      #2000,R0      ;DONE YET?
1733 016332 001347      BNE      1$      ;BR IF NO
1734 016334 104400      5$:  SCOPE      ;SCOPE THIS TEST
1735
1736
1737      ;***** TEST 4 *****
1738      ;*IOP CRAM DUAL ADDRESSING TEST
1739      ;*WRITE EACH ADDRESS INTO ITSELF,READ EACH
1740      ;*ADDRESS TO VERIFY CORRECT ADDRESSING
1741      ;*****
1742
1743      ; TEST 4
1744      ;-----
1745 016336 012737 000004 001226  TST4:  MOV      #4,TSTNO
1746 016344 012737 016516 001216      MOV      #TST5,NEXT
1747 016352 012737 016374 001220      MOV      #1$,LOCK
1748
1749 016360 104412      MSTCLR      ;R1 CONTAINS BASE DMC11 ADDRESS
      ;MASTER CLEAR DMC11

```

1750	016362	032737	100000	001366
1751	016370	001451		
1752	016372	005000		
1753	016374	010002		
1754	016376	012711	002000	
1755	016402	010061	000004	
1756	016406	010061	000006	
1757	016412	052711	020000	
1758	016416	005061	000006	
1759	016422	016104	000006	
1760	016426	020004		
1761	016430	001401		
1762	016432	104001		
1763	016434	104401		
1764	016436	005200		
1765	016440	022700	002000	
1766	016444	001353		
1767	016446	005000		
1768	016450	012737	016456	001220
1769	016456	010002		
1770	016460	012711	002000	
1771	016464	010061	000004	
1772	016470	016104	000006	
1773	016474	020004		
1774	016476	001401		
1775	016500	104002		
1776	016502	104401		
1777	016504	005200		
1778	016506	022700	002000	
1779	016512	001361		
1780	016514	104400		

```

BIT      #BIT15,STAT1
BEQ      $S
CLR      R0
1$:      MOV      R0,R2
          MOV      #BIT10,(R1)
          MOV      R0,4(R1)
          MOV      R0,6(R1)
          BIS      #BIT13,(R1)
          CLR      6(R1)
          MOV      6(R1),R4
          CMP      R0,R4
          BEQ      2$
          HLT      1
2$:      SCOP1
          INC      R0
          CMP      #2000,R0
          BNE      1$
          CLR      R0
          MOV      #3$,LOCK
3$:      MOV      R0,R2
          MOV      #BIT10,(R1)
          MOV      R0,4(R1)
          MOV      6(R1),R4
          CMP      R0,R4
          BEQ      4$
          HLT      2
4$:      SCOP1
          INC      R0
          CMP      #2000,R0
          BNE      3$
5$:      SCOPE

```

```

;DOES DMC HAVE CRAM?
;SKIP TEST IF NO CRAM
;R0 =CRAM ADDRESS
;SAVE R2 FOR TYPEOUT
;SET ROMO
;WRITE ADDRESS TO SEL4
;LOAD SEL6 WITH WRITE DATA
;WRITE CRAM
;CLEAR SEL 6
;SHOULD READ BACK OWN ADDRESS
;IS DATA CORRECT?
;BR IF YES
;DATA ERROR
;LOOP TO 1$ IF SW09=1
;BUMP TO NEXT ADDRESS
;DONE WRITING YET?
;BR IF NO
;RESTART AT ADDRESS 0
;NEW SCOPI
;SAVE R2 FOR TYPEOUT
;SET ROMO
;SEL4 = CRAM ADDRESS
;READ CRAM INTO "FOUND"
;IS DATA CORRECT?
;BR IF YES
;DUAL ADDRESSING ERROR
;LOOP TO 3$ IF SW09=1
;BUMP TO NEXT ADDRESS
;DONE WRITING YET?
;BR IF NO
;SCOPE THIS TEST

```

1781				
1782				
1783				
1784				
1785				
1786				
1787				
1788				
1789				
1790				
1791				
1792	016516	012737	000005	001226
1793	016524	012737	016636	001216
1794	016532	012737	016566	001220
1795				
1796	016540	104412		
1797	016542	032737	100000	001366
1798	016550	001431		
1799	016552	005011		
1800	016554	004737	035602	
1801	016560	012700	011766	
1802	016564	005002		
1803	016566	010261	000004	
1804	016572	012711	002000	
1805	016576	011005		

```

***** TEST 5 *****
;IOP CROM READ TEST
;THIS TEST WRITES THE CROM WITH THE CROM MICRO-CODE MAP
;THEN READS IT BACK AND COMPARES EACH ADDRESS WITH THE
;DUPLICATE OF THE CROM MICRO-CODE.
*****

; TEST 5
-----
TST5: MOV      #5,TSTNO
      MOV      #TST6,NEXT
      MOV      #1$,LOCK

      MSTCLR
      BIT      #BIT15,STAT1
      BEQ      3$
      CLR      (R1)
      JSR      PC,WROM
      MOV      #ROMMAP,R0
      CLR      R2
1$:   MOV      R2,4(R1)
      MOV      #BIT10,(R1)
      MOV      (R0),R5

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS IT RAM OR ROM
;SKIP TEST IF CROM
;CLEAR RUN
;WRITE CROM WITH MAP
;SOFTWARE POINTER TO CROM DUPLICATE
;R2 = CROM ADDRESS
;WRITE CROM ADDRESS TO SEL4
;SET CROMO
;PUT "EXPECTED" IN R5

```

Address	Hex	Dec	Label	Op	Op2	Op3	Op4	Op5	Op6	Op7	Op8	Op9	Op10	Op11	Op12	Op13	Op14	Op15	Op16	Op17	Op18	Op19	Op20	Op21	Op22	Op23	Op24	Op25	Op26	Op27	Op28	Op29	Op30	Op31	Op32	Op33	Op34	Op35	Op36	Op37	Op38	Op39	Op40	Op41	Op42	Op43	Op44	Op45	Op46	Op47	Op48	Op49	Op50	Op51	Op52	Op53	Op54	Op55	Op56	Op57	Op58	Op59	Op60	Op61	Op62	Op63	Op64	Op65	Op66	Op67	Op68	Op69	Op70	Op71	Op72	Op73	Op74	Op75	Op76	Op77	Op78	Op79	Op80	Op81	Op82	Op83	Op84	Op85	Op86	Op87	Op88	Op89	Op90	Op91	Op92	Op93	Op94	Op95	Op96	Op97	Op98	Op99	Op100	Op101	Op102	Op103	Op104	Op105	Op106	Op107	Op108	Op109	Op110	Op111	Op112	Op113	Op114	Op115	Op116	Op117	Op118	Op119	Op120	Op121	Op122	Op123	Op124	Op125	Op126	Op127	Op128	Op129	Op130	Op131	Op132	Op133	Op134	Op135	Op136	Op137	Op138	Op139	Op140	Op141	Op142	Op143	Op144	Op145	Op146	Op147	Op148	Op149	Op150	Op151	Op152	Op153	Op154	Op155	Op156	Op157	Op158	Op159	Op160	Op161	Op162	Op163	Op164	Op165	Op166	Op167	Op168	Op169	Op170	Op171	Op172	Op173	Op174	Op175	Op176	Op177	Op178	Op179	Op180	Op181	Op182	Op183	Op184	Op185	Op186	Op187	Op188	Op189	Op190	Op191	Op192	Op193	Op194	Op195	Op196	Op197	Op198	Op199	Op200	Op201	Op202	Op203	Op204	Op205	Op206	Op207	Op208	Op209	Op210	Op211	Op212	Op213	Op214	Op215	Op216	Op217	Op218	Op219	Op220	Op221	Op222	Op223	Op224	Op225	Op226	Op227	Op228	Op229	Op230	Op231	Op232	Op233	Op234	Op235	Op236	Op237	Op238	Op239	Op240	Op241	Op242	Op243	Op244	Op245	Op246	Op247	Op248	Op249	Op250	Op251	Op252	Op253	Op254	Op255	Op256	Op257	Op258	Op259	Op260	Op261	Op262	Op263	Op264	Op265	Op266	Op267	Op268	Op269	Op270	Op271	Op272	Op273	Op274	Op275	Op276	Op277	Op278	Op279	Op280	Op281	Op282	Op283	Op284	Op285	Op286	Op287	Op288	Op289	Op290	Op291	Op292	Op293	Op294	Op295	Op296	Op297	Op298	Op299	Op300	Op301	Op302	Op303	Op304	Op305	Op306	Op307	Op308	Op309	Op310	Op311	Op312	Op313	Op314	Op315	Op316	Op317	Op318	Op319	Op320	Op321	Op322	Op323	Op324	Op325	Op326	Op327	Op328	Op329	Op330	Op331	Op332	Op333	Op334	Op335	Op336	Op337	Op338	Op339	Op340	Op341	Op342	Op343	Op344	Op345	Op346	Op347	Op348	Op349	Op350	Op351	Op352	Op353	Op354	Op355	Op356	Op357	Op358	Op359	Op360	Op361	Op362	Op363	Op364	Op365	Op366	Op367	Op368	Op369	Op370	Op371	Op372	Op373	Op374	Op375	Op376	Op377	Op378	Op379	Op380	Op381	Op382	Op383	Op384	Op385	Op386	Op387	Op388	Op389	Op390	Op391	Op392	Op393	Op394	Op395	Op396	Op397	Op398	Op399	Op400	Op401	Op402	Op403	Op404	Op405	Op406	Op407	Op408	Op409	Op410	Op411	Op412	Op413	Op414	Op415	Op416	Op41
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1862 017020 001326
1863 017022 104400
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873 017024 012737 000007 001226
1874 017032 012737 017216 001216
1875 017040 012737 017072 001220
1876
1877 017046 104412
1878 017050 032737 100000 001366
1879 017056 001456
1880 017060 005037 034704
1881 017064 012700 000001
1882 017070 005100
1883 017072 042737 000377 017124
1884 017100 042737 000003 017130
1885 017106 153737 034704 017124
1886 017114 153737 034705 017130
1887 017122 104414
1888 017124 010000
1889 017126 104414
1890 017130 004000
1891 017132 010061 000004
1892 017136 104414
1893 017140 122500
1894 017142 104414
1895 017144 040620
1896 017146 104414
1897 017150 061225
1898 017152 010005
1899 017154 116104 000005
1900 017160 120504
1901 017162 001401
1902 017164 104010
1903 017166 104401
1904 017170 005100
1905 017172 000241
1906 017174 106100
1907 017176 001334
1908 017200 005237 034704
1909 017204 022737 002003 034704
1910 017212 001324
1911 017214 104400
1912
1913
1914
1915
1916
1917

2$: BNE 1$ ;BR IF NO
SCOPE ;SCOPE THIS TEST

;***** TEST 7 *****
;IOP MAIN MEMORY TEST
;FLOAT A G THROUGH ALL MAIN MEMORY LOCATIONS
;*****

; TEST 7
-----
TST7: MOV #7,TSTNO
MOV #TSTNO, NEXT
MOV #65$, LOCK

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS THIS AN IOP?
;SKIP TEST IF NO
;START WITH ADDRESS 0
;START WITH BIT 0
;CHANGE TO FLOATING 0
;CLEAR ADDRESS FIELD OF INSTRUCTION
;CLEAR ADDRESS FIELD OF INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;ADD ADDRESS TO INSTRUCTION
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR LO WITH ADDRESS IN FLAG
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR HI
;WRITE PATTERN IN PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE PORT4 TO MEMORY
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE MEMORY TO BR
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE BR TO PORT5
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;DATA ERROR
;SWD9=1?
;CHANGE TO FLOATING 1
;CLEAR CARRY
;SHIFT BIT IN R0
;DONE IF R0=0
;NEXT ADDRESS
;LAST ADDRESS?
;BR IF NO
;SCOPE THIS TEST

1$: MOV #1,R0
64$: COM R0
65$: BIC #377,66$
BIC #3,68$
BISB FLAG,66$
BISB FLAG+1,68$
ROMCLK
66$: 010000
ROMCLK
68$: 004000
MOV R0,4(R1)
ROMCLK
122500
ROMCLK
040620
ROMCLK
61225
MOV R0,R5
MOV R5,(R1),R4
CMPB R5,R4
BEQ 67$
HLT 10
67$: SCOP1
COM R0
CLC
ROLB R0
BNE 64$
INC FLAG
CMP #2000,FLAG
BNE 1$
SCOPE

;***** TEST 10 *****
;IOP MAIN MEMORY DUAL ADDRESSING TEST
;LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS
;READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING

```

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1918
1919
1920
1921
1922 017216 012737 000010 001226 TST10: MOV #10,TSTNO
1923 017224 012737 017516 001216 MOV #TST11,NEXT
1924 017232 012737 017256 001220 MOV #1$,LOCK
1925
1926 017240 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
1927 017242 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
1928 017250 001521 BEQ 9$ ;IS THIS AN IOP?
1929 017252 005037 034704 CLR FLAG ;SKIP TEST IF NO
1930 017256 013702 034704 1$: MOV FLAG,R2 ;START AT ADDRESS 0
1931 017262 042737 000377 017314 BIC #377,2$ ;PUT DATA IN R2
1932 017270 042737 000003 017320 BIC #3,7$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
1933 017276 153737 034704 017314 BISB FLAG,2$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
1934 017304 153737 034705 017320 BISB FLAG+1,7$ ;ADD ADDRESS TO INSTRUCTION
1935 017312 104414 ROMCLK ;ADD ADDRESS TO INSTRUCTION
1936 017314 010000 2$: 010000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1937 017316 104414 ROMCLK ;LOAD MAR LO
1938 017320 004000 7$: 004000 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1939 017322 010261 000004 MOV R2,4(R1) ;LOAD MAR HI
1940 017326 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1941 017330 122500 122500 ;MOVE PORT4 TO MEMORY
1942 017332 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1943 017334 040620 040620 ;MOVE MEMORY TO THE BR
1944 017336 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1945 017340 061225 61225 ;MOV BR TO PORT5
1946 017342 010205 MOV R2,R5 ;PUT "EXPECTED" IN R5
1947 017344 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
1948 017350 120504 CMPB R5,R4 ;DATA CORRECT?
1949 017352 001401 BEQ 3$ ;BR IF YES
1950 017354 104010 HLT 10 ;DATA ERROR
1951 017356 104401 3$: SCOP1 ;SW09=1?
1952 017360 005237 034704 INC FLAG ;NEXT ADDRESS
1953 017364 022737 002000 034704 CMP #2000,FLAG ;LAST ADDRESS
1954 017372 001331 BNE 1$ ;BR IF NO
1955 017374 012737 017406 001220 MOV #4$,LOCK ;NEW SCOPE 1
1956 017402 005037 034704 CLR FLAG ;RESTART AT ADDRESS 0
1957 017406 013702 034704 4$: MOV FLAG,R2 ;PUT DATA IN R2
1958 017412 042737 000377 017444 BIC #377,5$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
1959 017420 042737 000003 017450 BIC #3,8$ ;CLEAR ADDRESS FIELD OF INSTRUCTION
1960 017426 153737 034704 017444 BISB FLAG,5$ ;ADD ADDRESS TO INSTRUCTION
1961 017434 153737 034705 017450 BISB FLAG+1,8$ ;ADD ADDRESS TO INSTRUCTION
1962 017442 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1963 017444 010000 5$: 010000 ;LOAD THE MAR LO
1964 017446 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1965 017450 004000 8$: 004000 ;LOAD MAR HI
1966 017452 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1967 017454 040620 040620 ;MOVE MEMORY TO THE BR
1968 017456 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
1969 017460 061225 61225 ;MOV BR TO PORT5
1970 017462 010205 MOV R2,R5 ;PUT "EXPECTED" IN R5
1971 017464 116104 000005 MOVB 5(R1),R4 ;PUT "FOUND" IN R4
1972 017470 120504 CMPB R5,R4 ;DATA CORRECT?
1973 017472 001401 BEQ 6$ ;BR IF YES

```

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 DZCMH.P11 09-DEC-76 14:59 IOP TEST

PAGE: 0196

1974	017474	104010			6\$:	HLT	10		: ADDRESSING ERROR
1975	017476	104401				SCOPI			: SW09=1?
1976	017500	005237	034704			INC	FLAG		: NEXT ADDRESS
1977	017504	022737	002000	034704		CMP	#2000,FLAG		: IS IT THE LAST
1979	017512	001335				BNE	4\$		: BR IF NO
1979	017514	104400			9\$:	SCOPE			: SCOPE THIS TEST
1980									
1981									
1982									
1983									
1984									
1985									
1986									
1987									
1988									
1989									
1990	017516	012737	000011	001226					
1991	017524	012737	017532	001216					
1992									
1993	017532	104412							
1994	017534	032737	100000	001366					
1995	017542	001432							
1996	017544	005002							
1997	017546	104414							
1998	017550	010000							
1999	017552	010261	000004		1\$:				
2000	017556	104414							
2001	017560	136500							
2002	017562	005202							
2003	017564	022702	002000						
2004	017570	001370							
2005	017572	005002							
2006	017574	104414							
2007	017576	010000							
2008	017600				2\$:				
2009	017600	104414							
2010	017602	055224							
2011	017604	010205							
2012	017606	016104	000004						
2013	017612	120504							
2014	017614	001401							
2015	017616	104011							
2016	017620	005202			3\$:				
2017	017622	022702	002000						
2018	017626	001364							
2019	017630	104400			4\$:				
2020									
2021									
2022									
2023									
2024									
2025									
2026									
2027									
2028									
2029									


```

;***** TEST 11 *****
;IOP MAR TEST
;PERFORM DUAL ADDRESSING TEST
;USING MAR AUTO-INC FEATURE
;*****

; TEST 11
;-----
TST11: MOV #11,TSTNO
      MOV #TST12,NEXT
      MSTCLR
      BIT #BIT15,STAT1
      BEQ 4$
      CLR R2
      ROMCLK
      010000
      1$: MOV R2,4(R1)
      ROMCLK
      136500
      INC R2
      CMP #2000,R2
      BNE 1$
      CLR R2
      ROMCLK
      010000
      2$: ROMCLK
      055224
      MOV R2,R5
      MOV 4(R1),R4
      CMPB R5,R4
      BEQ 3$
      HLT 11
      3$: INC R2
      CMP #2000,R2
      BNE 2$
      4$: SCOPE

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS THIS AN IOP?
;SKIP TEST IF NO
;START WITH A ZERO
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR WITH A ZERO
;WRITE DATA TO PORT4
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MEM+PORT4, AUTO-INC MAR
;INCREMENT DATA
;DONE YET?
;BR IF NO
;RESTART WITH A ZERO
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;LOAD MAR WITH A ZERO
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;MOVE MEM TO PORT4
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;DATA CORRECT?
;BR IF YES
;MAR ERROR
;NEXT ADDRESS
;DONE YET?
;BR IF NO
;SCOPE THIS TEST

```



```

;***** TEST 12 *****
;IOP (GRAM) ODT BITS TEST
;LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS (2000 TIMES)
;VERIFY THAT IBUS* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE
;AND THAT IBUS* 10 BITS IS SET ON MAR OVERFLOW(2000)
;*****

; TEST 12

```

SCOPE

```
;R5="EXPECTED"  
;R4="FOUND"  
;CLEAR UNWANTED BITS  
;BITS 5&6 SHOULD BE CLEAR  
;BR IF OK  
;ERROR 5&6 NOT BOTH CLEAR  
;SCOPE THIS TEST
```

```

;***** TEST 13 *****
;*CROM READ TEST
;*THIS TEST READS EACH ROM LOCATION AND COMPARES

```

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PAGE: 0182

```

2086
2087
2088
2089
2090
2091
2092 020040 012737 000013 001226
2093 020046 012737 020230 001216
2094 020054 012737 020106 001220
2095
2096 020062 104412
2097 020064 032737 100000 001366
2098 020072 001055
2099 020074 005011
2100 020076 012700 011766
2101 020102 005002
2102 020104 005003
2103 020106 042737 014377 020126
2104 020114 050237 020126
2105 020120 050337 020126
2106 020124 104414
2107 020126 100400
2108 020130 012711 002000
2109 020134 011005
2110 020136 016104 000006
2111 020142 020504
2112 020144 001414
2113 020146 010337 001252
2114 020152 000241
2115 020154 006037 001252
2116 020160 006037 001252
2117 020164 006037 001252
2118 020170 050237 001252
2119 020174 104004
2120 020176 104401
2121 020200 005720
2122 020202 005202
2123 020204 022702 000400
2124 020210 001336
2125 020212 005002
2126 020214 062703 004000
2127 020220 022703 020000
2128 020224 001330
2129 020226 104400
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141 020230 012737 000014 001226

; *IT TO A SOFTWARE DUPLICATE OF THE CROM. THIS TEST
; *ALSO TESTS THE JUMP(I) MICRO-PROCESSOR INSTRUCTION.
; *****
; TEST 13
; -----
TST13: MOV #13,TSTNO
MOV #TST14,NEXT
MOV #13,LOCK

MSTCLR
BIT #BIT15,STAT1
BNE 4$
CLR (R1)
MOV #ROMMAP,R0
CLR R2
CLR R3
1$: BIC #14377,2$
BIS R2,2$
BIS R3,2$
ROMCLK
2$: 100400
MOV #BIT10,(R1)
MOV (R0),R5
MOV 6(R1),R4
CMP R5,R4
BEQ 3$
MOV R3,TEMP3
CLC
ROR TEMP3
ROR TEMP3
ROR TEMP3
BIS R2,TEMP3
HLT 4
3$: SCOP1
TST (R0)+
INC R2
CMP #400,R2
BNE 1$
CLR R2
ADD #4000,R3
CMP #20000,R3
BNE 1$
4$: SCOPE

; R1 CONTAINS BASE DMC11 ADDRESS
; MASTER CLEAR DMC11
; IS IT RAM OR ROM
; SKIP TEST IF CROM
; CLEAR RUN
; R0 POINTS TO SOFTWARE ROM MAP
; R2 CONTAINS ROM ADDRESS BITS 0-7
; R3 CONTAINS ROM ADDRESS BITS 8&9 IN BITS 11&12
; CLEAR ADDRESS FIELDS OF INSTRUCTION
; ADD BITS 0-7 TO INSTRUCTION
; ADD BITS 11&12 TO INSTRUCTION
; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
; JUMP(I) TO ROM ADDRESS IN R2 & R3
; SET ROMO
; PUT "EXPECTED" IN R5
; PUT "FOUND" IN R4
; COMPARE ROM CONTENTS TO SOFT DUP
; BR IF OK
; PUT ROM ADDRESS IN TEMP3
; FOR ERROR TYPEOUT

; TEMP3 NOW CONTAINS CORRECT ADDRESS
; ROM READ ERROR
; LOOP TO 1$ IF SW09=1
; BUMP SOFT POINTER
; BUMP ROM ADDRESS
; IS R2 TO MAX YET?
; BR IF NO
; YES. RESET R2 TO 0
; INC TO NEXT PAGE OF ROM
; DONE YET?
; BR IF NO
; SCOPE THIS TEST

; ***** TEST 14 *****
; *CROM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
; *PERFORM THE JUMP INSTRUCTION
; *VERIFY THAT THE JUMP DID NOT OCCUR BY READING
; *THE CONTENTS OF THE NEW ROM PC.IT SHOULD INCREMENT BY ONE).
; *****
; TEST 14
; -----
TST14: MOV #14,TSTNO

```

H15

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PAGE: 3189

2142	020236	012737	020420	001216	MOV	#TST15,NEXT	
2143	020244	012737	020264	001220	MOV	#15,LOCK	
2144							;R1 CONTAINS BASE DMC11 ADDRESS
2145	020252	104412			MSTCLR		;MASTER CLEAR DMC11
2146	020254	032737	100000	001366	BIT	#BIT15,STAT1	;IS IT CROM?
2147	020262	001055			BNE	6\$+2	;SKIP TEST IF YES
2148	020264						
2149	020264	004737	035430		15:	JSR	PC,CLRALL
2150	020270	104414			ROMCLK		;CLEAR ALL CONDITIONS
2151	020272	100400			100400		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2152	020274	104414			ROMCLK		;START AT ROM PC=0
2153	020276	114377			114377! <400*0>		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2154	020300	004737	035522		JSR	PC,ROMDAT	;JUMP TO ROM PC OF 1777
2155	020304	000002			2		;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2156	020306	020504			CMP	R5,R4	;INDEX
2157	020310	001401			BEQ	2\$	;ARE NEW PC CONTENTS CORRECT?
2158	020312	104006			HLT	6	;BR IF YES
2159	020314	104401			2\$:	SCOP1	;ERROR, CROM PC IS WRONG
2160	020316	012737	020324	001220	MOV	#3\$,LOCK	;LOOP TO 1\$ IF SW09=1
2161	020324				3\$:		;NEW SCOP1
2162	020324	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2163	020330	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2164	020332	100403			100403		;START AT ROM PC=3
2165	020334	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2166	020336	100000			100000! <400*0>		;JUMP TO ROM PC OF 0
2167	020340	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2168	020344	000010			10		;INDEX
2169	020346	020504			CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2170	020350	001401			BEQ	4\$	;BR IF YES
2171	020352	104006			HLT	6	;ERROR, CROM PC IS WRONG
2172	020354	104401			4\$:	SCOP1	;LOOP TO 3\$ IF SW09=1
2173	020356	012737	020364	001220	MOV	#5\$,LOCK	;NEW SCOP1
2174	020364				5\$:		
2175	020364	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2176	020370	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2177	020372	100406			100406		;START AT ROM PC=6
2178	020374	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2179	020376	104125			104125! <400*0>		;JUMP TO ROM PC OF 525
2180	020400	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2181	020404	000016			16		;INDEX
2182	020406	020504			CMP	R5,R4	;ARE NEW ROM PC CONTENTS CORRECT?
2183	020410	001401			BEQ	6\$	;BR IF YES
2184	020412	104006			HLT	6	;ERROR, CROM PC IS WRONG
2185	020414	104401			6\$:	SCOP1	;LOOP TO 5\$ IF SW59=1
2186	020416	104400			SCOPE		;SCOPE THIS TEST
2187							
2188							
2189							
2190							
2191							
2192							
2193							
2194							
2195							
2196							
2197	020420	012737	000015	001226	TST15:	MOV	#15,*STNO

***** TEST 15 *****
 *CROM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
 *PERFORM THE JUMP INSTRUCTION
 *VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC

 : TEST 15
 :-----

2198	020426	012737	020574	001216
2199	020434	012737	020454	001220
2200				
2201	020442	104412		
2202	020444	032737	100000	001366
2203	020452	001047		
2204	020454			
2205	020454	104414		
2206	020456	100400		
2207	020460	104414		
2208	020462	114777		
2209	020464	004737	035522	
2210	020470	003776		
2211	020472	020504		
2212	020474	001401		
2213	020476	104006		
2214	020500	104401		
2215	020502	012737	020510	001220
2216	020510			
2217	020510	104414		
2218	020512	100403		
2219	020514	104414		
2220	020516	100400		
2221	020520	004737	035522	
2222	020524	000000		
2223	020526	020504		
2224	020530	001401		
2225	020532	104006		
2226	020534	104401		
2227	020536	012737	020544	001220
2228	020544			
2229	020544	104414		
2230	020546	100406		
2231	020550	104414		
2232	020552	104525		
2233	020554	004737	035522	
2234	020560	001252		
2235	020562	020504		
2236	020564	001401		
2237	020566	104006		
2238	020570	104401		
2239	020572	104400		
2240				
2241				
2242				
2243				
2244				
2245				
2246				
2247				
2248				
2249				
2250	020574	012737	000016	001226
2251	020602	012737	020764	001216
2252	020610	012737	020630	001220
2253				

```

MOV      #TST16,NEXT
MOV      #1$,LOCK
;R1 CONTAINS BASE DMC11 ADDRESS
MSTCLR   ;MASTER CLEAR DMC11
BIT      #BIT15,STAT1
BNE      6$+2
;IS IT CRAM?
;SKIP TEST IF YES

ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400   ;START AT ROM PC=0
ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377!<400*1> ;JUMP TO ROM PC OF 1777
JSR      PC,ROMDAT
3776     ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
CMP      R5,R4
BEQ      2$
HLT      6
SCOPI    ;ERROR, CROM PC IS WRONG
MOV      #3$,LOCK
;LOOP TO 1$ IF SW09=1
;NEW SCOPI

ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100403   ;START AT ROM PC=3
ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000!<400*1> ;JUMP TO ROM PC OF 0
JSR      PC,ROMDAT
0        ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
CMP      R5,R4
BEQ      4$
HLT      6
SCOPI    ;ERROR, CROM PC IS WRONG
MOV      #5$,LOCK
;LOOP TO 3$ IF SW09=1
;NEW SCOPI

ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100406   ;START AT ROM PC=6
ROMCLK   ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
104125!<400*1> ;JUMP TO ROM PC OF 525
JSR      PC,ROMDAT
1252     ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
CMP      R5,R4
BEQ      6$
HLT      6
SCOPI    ;ERROR, CROM PC IS WRONG
SCOPE    ;LOOP TO 5$ IF SW59=1
;SCOPE THIS TEST

```

```

***** TEST 16 *****
;*CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
;*SET THE C BIT, PERFORM THE JUMP INSTRUCTION.
;*VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
;*****

```

: TEST 16

```
TST16:  MOV     #16,TSTNO
        MOV     #TST17,NEXT
        MOV     #15,LOCK
```

:R1 CONTAINS BASE DMC11 ADDRESS

J15

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PAGE: 0191

2254	020616	104412			MSTCLR		:MASTER CLEAR DMC11
2255	020620	032737	100000	001366	BIT	#BIT15,STAT1	:IS IT CROM?
2256	020626	001055			BNE	6\$+2	:SKIP TEST IF YES
2257	020630						
2258	020630	004737	035476		1\$: JSR	PC,SETC	:SET THE C BIT'
2259	020634	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2260	020636	100400			100400		:START AT ROM PC=0
2261	020640	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2262	020642	115377			114377!<400*2>		:JUMP TO ROM PC OF 1777
2263	020644	004737	035522		JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2264	020650	003776			3776		:INDEX
2265	020652	020504			CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2266	020654	001401			BEQ	2\$	:BR IF YES
2267	020656	104006			HLT	6	:ERROR, CROM PC IS WRONG
2268	020660	104401			2\$: SCOP1		:LOOP TO 1\$ IF SW09=1
2269	020662	012737	020670	001220	MOV	#3\$,LOCK	:NEW SCOP1
2270	020670				3\$: JSR	PC,SETC	:SET THE C BIT'
2271	020670	004737	035476		ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2272	020674	104414			100403		:START AT ROM PC=3
2273	020676	100403			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2274	020700	104414			100000!<400*2>		:JUMP TO ROM PC OF 0
2275	020702	101000			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2276	020704	004737	035522		0		:INDEX
2277	020710	000000			CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2278	020712	020504			BEQ	4\$	:BR IF YES
2279	020714	001401			HLT	6	:ERROR, CROM PC IS WRONG
2280	020716	104006			4\$: SCOP1		:LOOP TO 3\$ IF SW09=1
2281	020720	104401			MOV	#5\$,LOCK	:NEW SCOP1
2282	020722	012737	020730	001220	5\$: JSR	PC,SETC	:SET THE C BIT'
2283	020730				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2284	020730	004737	035476		100406		:START AT ROM PC=6
2285	020734	104414			ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2286	020736	100406			104125!<400*2>		:JUMP TO ROM PC OF 525
2287	020740	104414			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2288	020742	105125			1252		:INDEX
2289	020744	004737	035522		CMP	R5,R4	:ARE NEW ROM PC CONTENTS CORRECT?
2290	020750	001252			BEQ	6\$	:BR IF YES
2291	020752	020504			HLT	6	:ERROR, CROM PC IS WRONG
2292	020754	001401			6\$: SCOP1		:LOOP TO 5\$ IF SW59=1
2293	020756	104006			SCOPE		:SCOPE THIS TEST
2294	020760	104401					
2295	020762	104400					
2296							
2297							
2298							
2299							
2300							
2301							
2302							
2303							
2304							
2305							
2306	020764	012737	000017	001226	TST17: MOV	#17,TSTNO	
2307	020772	012737	021154	001216	MOV	#TST20,NEXT	
2308	021000	012737	021020	001220	MOV	#1\$,LOCK	
2309							

:R1 CONTAINS BASE DMC11 ADDRESS

K15

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PAGE: 0192

2310	021006	104412				MSTCLR		:MASTER CLEAR DMC11
2311	021010	032737	100000	001366		BIT	#BIT15,STAT1	:IS IT CROM?
2312	021016	001055				BNE	6\$+2	:SKIP TEST IF YES
2313	021020				1\$:			
2314	021020	004737	035514			JSR	PC,SETZ	:SET THE Z BIT'
2315	021024	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2316	021026	100400				100400		:START AT ROM PC=0
2317	021030	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2318	021032	115777				114377! <400*3>		:JUMP TO ROM PC OF 1777
2319	021034	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2320	021040	003776				3776		:INDEX
2321	021042	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2322	021044	001401				BEQ	2\$	:BR IF YES
2323	021046	104006				HLT	6	:ERROR, CROM PC IS WRONG
2324	021050	104401			2\$:	SCOPI		:LOOP TO 1\$ IF SW09=1
2325	021052	012737	021060	001220		MOV	#3\$,LOCK	:NEW SCOPI
2326	021060				3\$:			
2327	021060	004737	035514			JS	PC,SETZ	:SET THE Z BIT'
2328	021064	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2329	021066	100403				100403		:START AT ROM PC=3
2330	021070	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2331	021072	101400				100000! <400*3>		:JUMP TO ROM PC OF 0
2332	021074	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2333	021100	000000				0		:INDEX
2334	021102	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2335	021104	001401				BEQ	4\$	:BR IF YES
2336	021106	104006				HLT	6	:ERROR, CROM PC IS WRONG
2337	021110	104401			4\$:	SCOPI		:LOOP TO 3\$ IF SW09=1
2338	021112	012737	021120	001220		MOV	#5\$,LOCK	:NEW SCOPI
2339	021120				5\$:			
2340	021120	004737	035514			JSR	PC,SETZ	:SET THE Z BIT'
2341	021124	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2342	021126	100406				100406		:START AT ROM PC=6
2343	021130	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2344	021132	105525				104125! <400*3>		:JUMP TO ROM PC OF 525
2345	021134	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2346	021140	001252				1252		:INDEX
2347	021142	020504				CMP	R5,R4	:ARE NEW ROM PC CONTENTS CORRECT?
2348	021144	001401				BEQ	6\$	:BR IF YES
2349	021146	104006				HLT	6	:ERROR, CROM PC IS WRONG
2350	021150	104401			6\$:	SCOPI		:LOOP TO 5\$ IF SW59=1
2351	021152	104400				SCOPE		:SCOPE THIS TEST
2352								
2353								
2354								
2355								
2356								
2357								
2358								
2359								
2360								
2361								
2362	021154	012737	000020	001226	TST20:	MOV	#20,TSTNO	
2363	021162	012737	021344	001216		MOV	#TST21,NEXT	
2364	021170	012737	021210	001220		MOV	#1\$,LOCK	
2365								

:R1 CONTAINS BASE DMC11 ADDRESS

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PAGE: 0193

2366	021176	104412				MSTCLR		;MASTER CLEAR DMC11
2367	021200	032737	100000	001366		BIT	#BIT15,STAT1	;IS IT CROM?
2368	021206	001055				BNE	6\$+2	;SKIP TEST IF YES
2369	021210				1\$:			
2370	021210	004737	035446			JSR	PC,SETBRO	;SET THE BRO BIT
2371	021214	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2372	021216	100400				100400		;START AT ROM PC=0
2373	021220	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2374	021222	116377				114377! <400*4>		;JUMP TO ROM PC OF 1777
2375	021224	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2376	021230	003776				3776		;INDEX
2377	021232	020504				CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2378	021234	001401				BEQ	2\$	;BR IF YES
2379	021236	104006				HLT	6	;ERROR, CROM PC IS WRONG
2380	021240	104401			2\$:	SCOPI		;LOOP TO 1\$ IF SW09=1
2381	021242	012737	021250	001220		MOV	#3\$,LOCK	;NEW SCOPI
2382	021250				3\$:			
2383	021250	004737	035446			JSR	PC,SETBRO	;SET THE BRO BIT
2384	021254	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2385	021256	100403				100403		;START AT ROM PC=3
2386	021260	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2387	021262	102000				100000! <400*4>	;JUMP TO	ROM PC OF 0
2388	021264	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2389	021270	000000				0		;INDEX
2390	021272	020504				CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2391	021274	001401				BEQ	4\$	;BR IF YES
2392	021276	104006				HLT	6	;ERROR, CROM PC IS WRONG
2393	021300	104401			4\$:	SCOPI		;LOOP TO 3\$ IF SW09=1
2394	021302	012737	021310	001220		MOV	#5\$,LOCK	;NEW SCOPI
2395	021310				5\$:			
2396	021310	004737	035446			JSR	PC,SETBRO	;SET THE BRO BIT
2397	021314	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2398	021316	100406				100406		;START AT ROM PC=6
2399	021320	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2400	021322	106125				104125! <400*4>		;JUMP TO ROM PC OF 525
2401	021324	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2402	021330	0C1252				1252		;INDEX
2403	021332	020504				CMP	R5,R4	;ARE NEW ROM PC CONTENTS CORRECT?
2404	021334	001401				BEQ	6\$	;BR IF YES
2405	021336	104006				HLT	6	;ERROR, CROM PC IS WRONG
2406	021340	104401			6\$:	SCOPI		;LOOP TO 5\$ IF SW59=1
2407	021342	104400				SCOPE		;SCOPE THIS TEST
2408								
2409								
2410								
2411								
2412								
2413								
2414								
2415								
2416								
2417								
2418	021344	012737	000021	001226				
2419	021352	012737	021534	001216				
2420	021360	012737	021400	001220				
2421								

***** TEST 21 *****
 ;CROM TEST OF JUMP(I) ON BRI SET MICRO-PROCESSOR INSTRUCTION.
 ;SET THE BRI BIT. PERFORM THE JUMP INSTRUCTION.
 ;VERIFY THE JUMP BY READING THE CONTENTS OF THE NEW ROM PC
 ;*****

TEST 21

 TST21: MOV #21,TSTNO
 MOV #TST22,NEXT
 MOV #1\$,LOCK

;R1 CONTAINS BASE DMC11 ADDRESS

M15

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PAGE: 0194

2422	021366	104412				MSTCLR		:MASTER CLEAR DMC11
2423	021373	032737	100000	001366		BIT	#BIT15,STAT1	:IS IT CROM?
2424	021376	001055				BNE	6\$+2	:SKIP TEST IF YES
2425	021400				1\$:			
2426	021400	004737	035454			JSR	PC,SETBR1	:SET THE BR1 BIT'
2427	021404	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2428	021406	100400				100400		:START AT ROM PC=0
2429	021410	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2430	021412	116777				114377! <400*5>		:JUMP TO ROM PC OF 1777
2431	021414	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2432	021420	003776				3776		:INDEX
2433	021422	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2434	021424	001401				BEQ	2\$	:BR IF YES
2435	021426	104006				HLT	6	:ERROR, CROM PC IS WRONG
2436	021430	104401			2\$:	SCOPI		:LOOP TO 1\$ IF SW09=1
2437	021432	012737	021440	001220		MOV	#3\$,LOCK	:NEW SCOPI
2438	021440				3\$:			
2439	021440	004737	035454			JSR	PC,SETBR1	:SET THE BR1 BIT'
2440	021444	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2441	021446	100403				100403		:START AT ROM PC=3
2442	021450	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2443	021452	102400				100000! <400*5>	:JUMP TO	:ROM PC OF 0
2444	021454	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2445	021460	000000				0		:INDEX
2446	021462	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2447	021464	001401				BEQ	4\$	:BR IF YES
2448	021466	104006				HLT	6	:ERROR, CROM PC IS WRONG
2449	021470	104401			4\$:	SCOPI		:LOOP TO 3\$ IF SW09=1
2450	021472	012737	021500	001220		MOV	#5\$,LOCK	:NEW SCOPI
2451	021500				5\$:			
2452	021500	004737	035454			JSR	PC,SETBR1	:SET THE BR1 BIT'
2453	021504	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2454	021506	100406				100406		:START AT ROM PC=6
2455	021510	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2456	021512	106525				104125! <400*5>		:JUMP TO ROM PC OF 525
2457	021514	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2458	021520	001252				1252		:INDEX
2459	021522	020504				CMP	R5,R4	:ARE NEW ROM PC CONTENTS CORRECT?
2460	021524	001401				BEQ	6\$	:BR IF YES
2461	021526	104006				HLT	6	:ERROR, CROM PC IS WRONG
2462	021530	104401			6\$:	SCOPI		:LOOP TO 5\$ IF SW59=1
2463	021532	104400				SCOPE		:SCOPE THIS TEST
2464								
2465								
2466								
2467								
2468								
2469								
2470								
2471								
2472								
2473								
2474	021534	012737	000022	001226	TST22:	MOV	#22,TSTNO	
2475	021542	012737	021724	001216		MOV	#TST23,NEXT	
2476	021550	012737	021570	001220		MOV	#1\$,LOCK	
2477								

:R1 CONTAINS BASE DMC11 ADDRESS

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PAGE: 0195

2478	021556	104412				MSTCLR		;MASTER CLEAR DMC11
2479	021560	032737	100000	001366		BIT	#BIT15,STAT1	;IS IT CROM?
2480	021566	001055				BNE	6\$+2	;SKIP TEST IF YES
2481	021570				1\$:			
2482	021570	004737	035462			JSR	PC,SETBR4	;SET THE BR4 BIT'
2483	021574	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2484	021576	100400				100400		;START AT ROM PC=0
2485	021600	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2486	021602	117377				114377! <400*6>		;JUMP TO ROM PC OF 1777
2487	021604	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2488	021610	003776				3776		;INDEX
2489	021612	020504				CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2490	021614	001401				BEQ	2\$	;BR IF YES
2491	021616	104006				HLT	6	;ERROR, CROM PC IS WRONG
2492	021620	104401			2\$:	SCOP1		;LOOP TO 1\$ IF SW09=1
2493	021622	012737	021630	001220		MOV	#3\$,LOCK	;NEW SCOP1
2494	021630				3\$:			
2495	021630	004737	035462			JSR	PC,SETBR4	;SET THE BR4 BIT'
2496	021634	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2497	021636	100403				100403		;START AT ROM PC=3
2498	021640	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2499	021642	103000				100000! <400*6>	JUMP TO	;ROM PC OF 0
2500	021644	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2501	021650	000000				0		;INDEX
2502	021652	020504				CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2503	021654	001401				BEQ	4\$	;BR IF YES
2504	021656	104006				HLT	6	;ERROR, CROM PC IS WRONG
2505	021660	104401			4\$:	SCOP1		;LOOP TO 3\$ IF SW09=1
2506	021662	012737	021670	001220		MOV	#5\$,LOCK	;NEW SCOP1
2507	021670				5\$:			
2508	021670	004737	035462			JSR	PC,SETBR4	;SET THE BR4 BIT'
2509	021674	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2510	021676	100406				100406		;START AT ROM PC=6
2511	021700	104414				ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2512	021702	107125				104125! <400*6>		;JUMP TO ROM PC OF 525
2513	021704	004737	035522			JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2514	021710	001252				1252		;INDEX
2515	021712	020504				CMP	R5,R4	;ARE NEW ROM PC CONTENTS CORRECT?
2516	021714	001401				BEQ	6\$	;BR IF YES
2517	021716	104006				HLT	6	;ERROR, CROM PC IS WRONG
2518	021720	104401			6\$:	SCOP1		;LOOP TO 5\$ IF SW59=1
2519	021722	104400				SCOPE		;SCOPE THIS TEST
2520								
2521								
2522								
2523								
2524								
2525								
2526								
2527								
2528								
2529								
2530	021724	012737	000023	001226	TST23:	MOV	#23,TSTNO	
2531	021732	012737	022114	001216		MOV	#TST24,NEXT	
2532	021740	012737	021760	001220		MOV	#1\$,LOCK	
2533								

;R1 CONTAINS BASE DMC11 ADDRESS

B16

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PAGE: 0176

2534	021746	104412				MSTCLR		:MASTER CLEAR DMC11
2535	021750	032737	100000	001366		BIT	#BIT15,STAT1	:IS IT CRAM?
2536	021756	001055				BNE	6\$+2	:SKIP TEST IF YES
2537	021760				1\$:			
2538	021760	004737	035470			JSR	PC,SETBR7	:SET THE BR7 BIT'
2539	021764	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2540	021766	100400				100400		:START AT ROM PC=0
2541	021770	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2542	021772	117777				114377!<400*7>		:JUMP TO ROM PC OF 1777
2543	021774	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2544	022000	003776				3776		:INDEX
2545	022002	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2546	022004	001401				BEQ	2\$	:BR IF YES
2547	022006	104006				HLT	6	:ERROR, CROM PC IS WRONG
2548	022010	104401			2\$:	SCOP1		:LOOP TO 1\$ IF SW09=1
2549	022012	012737	022020	001220		MOV	#3\$,LOCK	:NEW SCOP1
2550	022020				3\$:			
2551	022020	004737	035470			JSR	PC,SETBR7	:SET THE BR7 BIT'
2552	022024	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2553	022026	100403				100403		:START AT ROM PC=3
2554	022030	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2555	022032	103400				100000!<400*7>	:JUMP TO	:ROM PC OF 0
2556	022034	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2557	022040	000000				0		:INDEX
2558	022042	020504				CMP	R5,R4	:ARE NEW PC CONTENTS CORRECT?
2559	022044	001401				BEQ	4\$	:BR IF YES
2560	022046	104006				HLT	6	:ERROR, CROM PC IS WRONG
2561	022050	104401			4\$:	SCOP1		:LOOP TO 3\$ IF SW09=1
2562	022052	012737	022060	001220		MOV	#5\$,LOCK	:NEW SCOP1
2563	022060				5\$:			
2564	022060	004737	035470			JSR	PC,SETBR7	:SET THE BR7 BIT'
2565	022064	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2566	022066	100406				100406		:START AT ROM PC=6
2567	022070	104414				ROMCLK		:NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2568	022072	107525				104125!<400*7>		:JUMP TO ROM PC OF 525
2569	022074	004737	035522			JSR	PC,ROMDAT	:R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2570	022100	001252				1252		:INDEX
2571	022102	020504				CMP	R5,R4	:ARE NEW ROM PC CONTENTS CORRECT?
2572	022104	001401				BEQ	6\$	:BR IF YES
2573	022106	104006				HLT	6	:ERROR, CROM PC IS WRONG
2574	022110	104401			6\$:	SCOP1		:LOOP TO 5\$ IF SW59=1
2575	022112	104400				SCOPE		:SCOPE THIS TEST
2576								
2577								
2578								
2579								
2580								
2581								
2582								
2583								
2584								
2585								
2586								
2587	022114	012737	000024	001226	TST24:	MOV	#24,TSTNO	
2588	022122	012737	022304	001216		MOV	#TST25,NEXT	
2589	022130	012737	022150	001220		MOV	#1\$,LOCK	

***** TEST 24 *****
 *CROM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
 *CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION.
 *VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 *THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

TEST 24

```

2590
2591 022136 104412
2592 022140 032737 100000 001366
2593 022146 001055
2594 022150
2595 022150 004737 035430
2596 022154 104414
2597 022156 100400
2598 022160 104414
2599 022162 115377
2600 022164 004737 035522
2601 022170 000002
2602 022172 020504
2603 022174 001401
2604 022176 104006
2605 022200 104401
2606 022202 012737 022210 001220
2607 022210
2608 022210 004737 035430
2609 022214 104414
2610 022216 100403
2611 022220 104414
2612 022222 101090
2613 022224 004737 035522
2614 022230 000010
2615 022232 020504
2616 022234 001401
2617 022236 104006
2618 022240 104401
2619 022242 012737 022250 001220
2620 022250
2621 022250 004737 035430
2622 022254 104414
2623 022256 100406
2624 022260 104414
2625 022262 105125
2626 022264 004737 035522
2627 022270 000016
2628 022272 020504
2629 022274 001401
2630 022276 104006
2631 022300 104401
2632 022302 104400
2633
2634
2635
2636
2637
2638
2639
2640
2641
2642
2643
2644 022304 012737 000025 001226
2645 022312 012737 022474 001216

MSTCLR
BIT #BIT15,STAT1
BNE 6$+2
1$: JSR PC,CLRALL
ROMCLK
100400
ROMCLK
114377! <400*2>
JSR PC,ROMDAT
2
CMP R5,R4
BEQ 2$
HLT 6
2$: SCOP1
MOV #3$,LOCK
3$: JSR PC,CLRALL
ROMCLK
100403
ROMCLK
100000! <400*2> JUMP TO
JSR PC,ROMDAT
10
CMP R5,R4
BEQ 4$
HLT 6
4$: SCOP1
MOV #5$,LOCK
5$: JSR PC,CLRALL
ROMCLK
100406
ROMCLK
104125! <400*2>
JSR PC,ROMDAT
16
CMP R5,R4
BEQ 6$
HLT 6
6$: SCOP1
SCOPE

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS IT CRAM?
;SKIP TEST IF YES
;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=0
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 1777
;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
;ARE NEW PC CONTENTS CORRECT?
;BR IF YES
;ERROR, CROM PC IS WRONG
;LOOP TO 1$ IF SW09=1
;NEW SCOP1
;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=3
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 0
;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
;ARE NEW PC CONTENTS CORRECT?
;BR IF YES
;ERROR, CROM PC IS WRONG
;LOOP TO 3$ IF SW09=1
;NEW SCOP1
;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=6
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 525
;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
;INDEX
;ARE NEW ROM PC CONTENTS CORRECT?
;BR IF YES
;ERROR, CROM PC IS WRONG
;LOOP TO 5$ IF SW59=1
;SCOPE THIS TEST

;***** TEST 25 *****
;*CROM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
;*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
;*VERIFY THAT THE JUMP DID NOT OCCUR BY READING
;*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
;*****

; TEST 25
;-----
TST25: MOV #25,TSTNO
MOV #TST26,NEXT

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D16

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PAGE: 0198

2646	022320	012737	022340	001220	MOV	#1\$,LOCK	
2647							;R1 CONTAINS BASE DMC11 ADDRESS
2649	022326	104412			MSTCLR		;MASTER CLEAR DMC11
2649	022330	032737	100000	001366	BIT	#BIT15,STAT1	;IS IT CROM?
2650	022336	001055			BNE	6\$+2	;SKIP TEST IF YES
2651	022340				1\$:		
2652	022340	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2653	022344	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2654	022346	100400			100400		;START AT ROM PC=0
2655	022350	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2656	022352	115777			114377! <400*3>		;JUMP TO ROM PC OF 1777
2657	022354	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2658	022360	000002			2		;INDEX
2659	022362	020504			CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2660	022364	001401			BEQ	2\$	;BR IF YES
2661	022366	104006			HLT	6	;ERROR, CROM PC IS WRONG
2662	022370	104401			2\$:	SCOPI	;LOOP TO 1\$ IF SW09=1
2663	022372	012737	022400	001220	MOV	#3\$,LOCK	;NEW SCOPI
2664	022400				3\$:		
2665	022400	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2666	022404	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2667	022406	100403			100403		;START AT ROM PC=3
2668	022410	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2669	022412	101400			100000! <400*3>	JUMP TO	;JUMP TO ROM PC OF 0
2670	022414	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2671	022420	000010			10		;INDEX
2672	022422	020504			CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2673	022424	001401			BEQ	4\$	;BR IF YES
2674	022426	104006			HLT	6	;ERROR, CROM PC IS WRONG
2675	022430	104401			4\$:	SCOPI	;LOOP TO 3\$ IF SW09=1
2676	022432	012737	022440	001220	MOV	#5\$,LOCK	;NEW SCOPI
2677	022440				5\$:		
2678	022440	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2679	022444	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2680	022446	100406			100406		;START AT ROM PC=6
2681	022450	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2682	022452	105525			104125! <400*3>		;JUMP TO ROM PC OF 525
2683	022454	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2684	022460	000016			16		;INDEX
2685	022462	020504			CMP	R5,R4	;ARE NEW ROM PC CONTENTS CORRECT?
2686	022464	001401			BEQ	6\$	;BR IF YES
2687	022466	104006			HLT	6	;ERROR, CROM PC IS WRONG
2688	022470	104401			6\$:	SCOPI	;LOOP TO 5\$ IF SW59=1
2689	022472	104400			SCOPE		;SCOPE THIS TEST
2690							
2691							
2692							
2693							
2694							
2695							
2696							
2697							
2698							
2699							
2700							
2701	022474	012737	000026	001226	TEST26:	MOV	#26,TESTNO

***** TEST 26 *****
 *CROM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
 *CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION,
 *VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 *THE CONTENTS OF THE NEW ROM PC (IT SHOULD INCREMENT BY ONE).

 : TEST 26
 :-----
 : TEST 26

E16

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 CZCMM.P11 09-DEC-76 14:59 CROM JUMP TESTS

PAGE: 0199

2702	022502	012737	022664	001216	MOV	#TST27,NEXT	
2703	022510	012737	022530	001220	MOV	#1\$,LOCK	
2704							;R1 CONTAINS BASE DMC11 ADDRESS
2705	022516	104412			MSTCLR		;MASTER CLEAR DMC11
2706	022520	032737	100000	001366	BIT	#BIT15,STAT1	;IS IT CROM?
2707	022526	001055			BNE	6\$+2	;SKIP TEST IF YES
2708	022530				1\$:		
2709	022530	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2710	022534	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2711	022536	100400			100400		;START AT ROM PC=0
2712	022540	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2713	022542	116377			114377!(400*4)		;JUMP TO ROM PC OF 1777
2714	022544	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2715	022550	000002			2		;INDEX
2716	022552	020504			CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2717	022554	001401			BEQ	2\$	;BR IF YES
2718	022556	104006			HLT	6	;ERROR, CROM PC IS WRONG
2719	022560	104401			2\$:		;LOOP TO 1\$ IF SW09=1
2720	022562	012737	022570	001220	MOV	#3\$,LOCK	;NEW SCOPI
2721	022570				3\$:		
2722	022570	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2723	022574	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2724	022576	100403			100403		;START AT ROM PC=3
2725	022600	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2726	022602	102000			100000!(400*4)		;JUMP TO ROM PC OF 0
2727	022604	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2728	022610	000010			10		;INDEX
2729	022612	020504			CMP	R5,R4	;ARE NEW PC CONTENTS CORRECT?
2730	022614	001401			BEQ	4\$	;BR IF YES
2731	022616	104006			HLT	6	;ERROR, CROM PC IS WRONG
2732	022620	104401			4\$:		;LOOP TO 3\$ IF SW09=1
2733	022622	012737	022630	001220	MOV	#5\$,LOCK	;NEW SCOPI
2734	022630				5\$:		
2735	022630	004737	035430		JSR	PC,CLRALL	;CLEAR ALL CONDITIONS
2736	022634	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2737	022636	100406			100406		;START AT ROM PC=6
2738	022640	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2739	022642	106125			104125!(400*4)		;JUMP TO ROM PC OF 525
2740	022644	004737	035522		JSR	PC,ROMDAT	;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2741	022650	000016			16		;INDEX
2742	022652	020504			CMP	R5,R4	;ARE NEW ROM PC CONTENTS CORRECT?
2743	022654	001401			BEQ	6\$	;BR IF YES
2744	022656	104006			HLT	6	;ERROR, CROM PC IS WRONG
2745	022660	104401			6\$:		;LOOP TO 5\$ IF SW59=1
2746	022662	104400			SCOPI		;SCOPE THIS TEST
2747					SCOPE		
2748							
2749							
2750							
2751							
2752							
2753							
2754							
2755							
2756							
2757							

***** TEST 27 *****
 ;CROM TEST OF JUMP(I) ON BRI SET MICRO-PROCESSOR INSTRUCTION.
 ;CLEAR THE BRI BIT, PERFORM THE JUMP INSTRUCTION.
 ;VERIFY THAT THE JUMP DID NOT OCCUR BY READING
 ;THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).
 :*****
 : TEST 27
 :-----

F16

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020MH.P11 09-DEC-76 14:59 CROM JUMP TESTS

PAGE: 0200

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2758 022664 012737 000027 001226 TST27: MOV #27,TSTNO
2759 022672 012737 023054 001216 MOV #TST30,NEXT
2760 022700 012737 022720 001220 MOV #1$,LOCK
2761
2762 022706 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2763 022710 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
2764 022716 001055 BNE 6$+2 ;IS IT CROM?
2765 022720 1$: JSR PC,CLRALL ;SKIP TEST IF YES
2766 022720 004737 035430 ROMCLK ;CLEAR ALL CONDITIONS
2767 022724 104414 100400 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2768 022726 100400 100400 ;START AT ROM PC=0
2769 022730 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2770 022732 116777 114377! <400*5> ;JUMP TO ROM PC OF 1777
2771 022734 004737 035522 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2772 022740 000002 2 ;INDEX
2773 022742 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2774 022744 001401 BEQ 2$ ;BR IF YES
2775 022746 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2776 022750 104401 2$: SCOP1 ;LOOP TO 1$ IF SW09=1
2777 022752 012737 022760 001220 MOV #3$,LOCK ;NEW SCOP1
2778 022760 3$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2779 022760 004737 035430 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2780 022764 104414 100403 ;START AT ROM PC=3
2781 022766 100403 100403 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2782 022770 104414 100000! <400*5> ;JUMP TO ROM PC OF 0
2783 022772 102400 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2784 022774 004737 035522 10 ;INDEX
2785 023000 000010 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2786 023002 020504 BEQ 4$ ;BR IF YES
2787 023004 001401 HLT 6 ;ERROR, CROM PC IS WRONG
2788 023006 104006 4$: SCOP1 ;LOOP TO 3$ IF SW09=1
2789 023010 104401 MOV #5$,LOCK ;NEW SCOP1
2790 023012 012737 023020 001220 5$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2791 023020 004737 035430 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2792 023020 004737 035430 100405 ;START AT ROM PC=6
2793 023024 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2794 023026 100406 104125! <400*5> ;JUMP TO ROM PC OF 525
2795 023030 104414 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2796 023032 106525 16 ;INDEX
2797 023034 004737 035522 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2798 023040 000016 BEQ 6$ ;BR IF YES
2799 023042 020504 HLT 6 ;ERROR, CROM PC IS WRONG
2800 023044 001401 6$: SCOP1 ;LOOP TO 5$ IF SW59=1
2801 023046 104006 SCOPE ;SCOPE THIS TEST
2802 023050 104401
2803 023052 104401
2804
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G16

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PAGE: 0201

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2814
2815 023054 012737 000030 001226 TST30: MOV #30,TSTNO
2816 023062 012737 023244 001216 MOV #TST31,NEXT
2817 023070 012737 023110 001220 MOV #1$,LOCK
2818
2819
2820 023076 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
2821 023100 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
2822 023110 001055 BNE 6$+2 ;IS IT CROM?
2823 023110 004737 035430 1$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2824 023114 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2825 023116 100400 100400 ;START AT ROM PC=0
2826 023120 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2827 023122 117377 114377! <400*6> ;JUMP TO ROM PC OF 1777
2828 023124 004737 035522 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2829 023130 000002 2 INDEX
2830 023132 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2831 023134 001401 BEQ 2$ ;BR IF YES
2832 023136 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2833 023140 104401 2$: SCOP1 ;LOOP TO 1$ IF SW09=1
2834 023142 012737 023150 001220 MOV #3$,LOCK ;NEW SCOP1
2835 023150 3$:
2836 023150 004737 035430 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2837 023154 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2838 023156 100403 100403 ;START AT ROM PC=3
2839 023160 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2840 023162 103000 100000! <400*6> ;JUMP TO ROM PC OF 0
2841 023164 004737 035522 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2842 023170 000010 10 INDEX
2843 023172 020504 CMP R5,R4 ;ARE NEW PC CONTENTS CORRECT?
2844 023174 001401 BEQ 4$ ;BR IF YES
2845 023176 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2846 023200 104401 4$: SCOP1 ;LOOP TO 3$ IF SW09=1
2847 023202 012737 023210 001220 MOV #5$,LOCK ;NEW SCOP1
2848 023210 5$:
2849 023210 004737 035430 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
2850 023214 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2851 023216 100406 100406 ;START AT ROM PC=6
2852 023220 104414 ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2853 023222 107125 104125! <400*6> ;JUMP TO ROM PC OF 525
2854 023224 004737 035522 JSR PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2855 023230 000016 16 INDEX
2856 023232 020504 CMP R5,R4 ;ARE NEW ROM PC CONTENTS CORRECT?
2857 023234 001401 BEQ 6$ ;BR IF YES
2858 023236 104006 HLT 6 ;ERROR, CROM PC IS WRONG
2859 023240 104401 6$: SCOP1 ;LOOP TO 5$ IF SW59=1
2860 023242 104401 SCOPE ;SCOPE THIS TEST
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***** TEST 31 *****

*CROM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.

*CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION,

*VERIFY THAT THE JUMP DID NOT OCCUR BY READING

*THE CONTENTS OF THE NEW ROM PC(IT SHOULD INCREMENT BY ONE).

H16

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PAGE: 0202

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2870      : TEST 31
2871      :-----
2872 023244 012737 000031 001226      TST31: MOV     #31,TSTNO
2873 023252 012737 023434 001216      MOV     #TST32,NEXT
2874 023260 012737 023300 001220      MOV     #15,LOCK
2875      ;R1 CONTAINS BASE DMC11 ADDRESS
2876 023266 104412      MSTCLR      ;MASTER CLEAR DMC11
2877 023270 032737 100000 001366      BIT     #BIT15,STAT1
2878 023276 001055      BNE     6$+2      ;IS IT CROM?
2879      ;SKIP TEST IF YES
2880 023300      1$:      JSR     PC,CLRALL      ;CLEAR ALL CONDITIONS
2881 023304 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2882 023306 100400      100400      ;START AT ROM PC=0
2883 023310 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2884 023312 117777      114377!<400*7> ;JUMP TO ROM PC OF 1777
2885 023314 004737 035522      JSR     PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2886 023320 000002      2      ;INDEX
2887 023322 020504      CMP     R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2888 023324 001401      BEQ     2$      ;BR IF YES
2889 023326 104006      HLT     6      ;ERROR, CROM PC IS WRONG
2890 023330 104401      2$:      SCOP1      ;LOOP TO 1$ IF SW09=1
2891 023332 012737 023340 001220      MOV     #3$,LOCK ;NEW SCOP1
2892 023340      3$:
2893 023340 004737 035430      JSR     PC,CLRALL      ;CLEAR ALL CONDITIONS
2894 023344 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2895 023346 100403      100403      ;START AT ROM PC=3
2896 023350 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2897 023352 103400      100000!<400*7> ;JUMP TO ROM PC OF 0
2898 023354 004737 035522      JSR     PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2899 023360 000010      10      ;INDEX
2900 023362 020504      CMP     R5,R4      ;ARE NEW PC CONTENTS CORRECT?
2901 023364 001401      BEQ     4$      ;BR IF YES
2902 023366 104006      HLT     6      ;ERROR, CROM PC IS WRONG
2903 023370 104401      4$:      SCOP1      ;LOOP TO 3$ IF SW09=1
2904 023372 012737 023400 001220      MOV     #5$,LOCK ;NEW SCOP1
2905 023400      5$:
2906 023400 004737 035430      JSR     PC,CLRALL      ;CLEAR ALL CONDITIONS
2907 023404 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2908 023406 100406      100406      ;START AT ROM PC=6
2909 023410 104414      ROMCLK      ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
2910 023412 107525      104125!<400*7> ;JUMP TO ROM PC OF 525
2911 023414 004737 035522      JSR     PC,ROMDAT ;R5=EXPECTED ROM DATA,R4=ACTUAL ROM DATA
2912 023420 000016      16      ;INDEX
2913 023422 020504      CMP     R5,R4      ;ARE NEW ROM PC CONTENTS CORRECT?
2914 023424 001401      BEQ     6$      ;BR IF YES
2915 023426 104006      HLT     6      ;ERROR, CROM PC IS WRONG
2916 023430 104401      6$:      SCOP1      ;LOOP TO 5$ IF SW59=1
2917 023432 104400      SCOPE      ;SCOPE THIS TEST
2918
2919
2920
2921 ***** TEST 32 *****
2922 *CROM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
2923 *PERFORM THE JUMP INSTRUCTION
2924 *VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
2925 *IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
2926 *BR WITH THE LOWEST 9 BITS OF THE CROM PC. AT THIS POINT

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2926      ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
2927      ;*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT.
2928      ;*THEN PORT4 CONTAINS A 37
2929      ;*****
2930
2931      ; TEST 32
2932      ;-----
2933      *ST32: MOV      #32,TSTNO
2934             MOV      #TST33,NEXT
2935             MOV      #1$,LOCK
2936
2937             MSTCLR
2938             BIT      #BIT15,STAT1
2939             BEQ      6$+2
2940             JSR      PC,MEMSET
2941
2942             1$: JSR      PC,CLRALL
2943                 ROMCLK
2944                 100400
2945                 ROMCLK
2946                 114377! <400*0>
2947                 JSR      PC,RAMDAT
2948                 1
2949                 CMPB     R5,R4
2950                 BEQ      2$
2951                 HLT      5
2952                 2$: SCOP1
2953                     MOV      #3$,LOCK
2954
2955                 3$: JSR      PC,CLRALL
2956                     ROMCLK
2957                     100403
2958                     ROMCLK
2959                     100000! <400*0> JUMP TO ROM PC OF 0
2960                     JSR      PC,RAMDAT
2961                     4
2962                     CMPB     R5,R4
2963                     BEQ      4$
2964                     HLT      5
2965                     4$: SCOP1
2966                         MOV      #5$,LOCK
2967
2968                     5$: JSR      PC,CLRALL
2969                         ROMCLK
2970                         100406
2971                         ROMCLK
2972                         104125! <400*0>
2973                         JSR      PC,RAMDAT
2974                         7
2975                         CMPB     R5,R4
2976                         BEQ      6$
2977                         HLT      5
2978                         6$: SCOP1
2979                             SCOPE
2980
2981

```

;R1 CONTAINS BASE DMC11 ADDRESS
 ;MASTER CLEAR DMC11
 ;IS IT CRAM?
 ;SKIP TEST IF NO
 ;SET MEM AND RAM
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=0
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 1777
 ;R4=CRAM PC (LSB 8 BITS)
 ;EXPECTED DATA
 ;IS ROM PC CORRECT?
 ;BR IF YES
 ;ERROR, CRAM PC IS WRONG
 ;LOOP TO 1\$ IF SW09=1
 ;NEW SCOPI
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=3
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 0
 ;R4=CRAM PC (LSB 8 BITS)
 ;EXPECTED DATA
 ;IS ROM PC CORRECT?
 ;BR IF YES
 ;ERROR, CRAM PC IS WRONG
 ;LOOP TO 3\$ IF SW09=1
 ;NEW SCOPI
 ;CLEAR ALL CONDITIONS
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=6
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 525
 ;R4=CRAM PC (LSB 8 BITS)
 ;EXPECTED DATA
 ;IS ROM PC CORRECT?
 ;BR IF YES
 ;ERROR, CRAM PC IS WRONG
 ;LOOP TO 5\$ IF SW59=1
 ;SCOPE THIS TEST

J16

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PAGE: 0204

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2995 023630 012737 000033 001226
2996 023636 012737 024010 001216
2997 023644 012737 023670 001220
2998
2999 023652 104412
3000 023654 032737 100000 001366
3001 023662 001451
3002 023664 004737 035654
3003 023670
3004 023670 104414
3005 023672 100400
3006 023674 104414
3007 023676 114777
3008 023700 004737 035550
3009 023704 000377
3010 023706 120504
3011 023710 001401
3012 023712 104005
3013 023714 104401
3014 023716 012737 023724 001220
3015 023724
3016 023724 104414
3017 023726 100403
3018 023730 104414
3019 023732 100400
3020 023734 004737 035550
3021 023740 000000
3022 023742 120504
3023 023744 001401
3024 023746 104005
3025 023750 104401
3026 023752 012737 023760 001220
3027 023760
3028 023760 104414
3029 023762 100406
3030 023764 104414
3031 023766 104525
3032 023770 004737 035550
3033 023774 000125
3034 023776 120504
3035 024000 001401
3036 024002 104005
3037 024004 104401

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***** TEST 33 *****
*CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
*PERFORM THE JUMP INSTRUCTION
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
*****

: TEST 33
-----
TS*33: MOV #33,ISTNO
MOV #TS*34,NEXT
MOV #1$,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
BEQ 6$+2 ;IS IT CRAM?
JSR PC,MEMSET ;SKIP TEST IF NO
;SET MEM AND RAM

1$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400 ;START AT ROM PC=0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377! <400*1> ;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
377 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 2$ ;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
2$: SCOP1 ;LOOP TO 1$ IF SW09=1
MOV #3$,LOCK ;NEW SCOP1

3$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100403 ;START AT ROM PC=3
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000! <400*1> ;JUMP TO ROM PC OF 0
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
0 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 4$ ;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
4$: SCOP1 ;LOOP TO 3$ IF SW09=1
MOV #5$,LOCK ;NEW SCOP1

5$: ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100406 ;START AT ROM PC=6
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
104125! <400*1> ;JUMP TO ROM PC OF 525
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
125 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 6$ ;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
6$: SCOP1 ;LOOP TO 5$ IF SW59=1

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K16

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PAGE: 0205

3038 024006 104400

SCOPE

:SCOPE THIS TEST

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024010 012737 000034 001226
024016 012737 024204 001216
024024 012737 024050 001220

024032 104412
024034 032737 100000 001366
024042 001457
024044 004737 035654
024050
024050 004737 035476
024054 104414
024056 100400
024060 104414
024062 115377
024064 004737 035550
024070 000377
024072 120504
024074 001401
024076 104005
024100 104401
024102 012737 024110 001220
024110
024110 004737 035476
024114 104414
024116 100403
024120 104414
024122 101000
024124 004737 035550
024130 000000
024132 120504
024134 001401
024136 104005
024140 104401
024142 012737 024150 001220
024150
024150 004737 035476
024154 104414
024156 100406
024160 104414
024162 105125

TST34:

1\$:

2\$:

3\$:

4\$:

5\$:

***** TEST 34 *****
*CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
*SET THE C BIT, PERFORM THE JUMP INSTRUCTION,
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37

: TEST 34

MOV #34,TSTNO
MOV #TST35,NEXT
MOV #1\$,LOCK

MSTCLR
BIT #BIT15,STAT1
BEQ 6\$+2
JSR PC,MEMSET

JSR PC,SETC ;SET THE C BIT'

ROMCLK
100400
ROMCLK
114377! <400*2>
JSR PC,RAMDAT
377

CMPB R5,R4
BEQ 2\$
HLT 5

SCOP1
MOV #3\$,LOCK

JSR PC,SETC ;SET THE C BIT'

ROMCLK
100403
ROMCLK
100000! <400*2>
JSR PC,RAMDAT
0

CMPB R5,R4
BEQ 4\$
HLT 5

SCOP1
MOV #5\$,LOCK

JSR PC,SETC ;SET THE C BIT'

ROMCLK
100406
ROMCLK
104125! <400*2>

;R1 CONTAINS BASE DMC11 ADDRESS

;MASTER CLEAR DMC11

;IS IT CRAM?

;SKIP TEST IF NO

;SET MEM AND RAM

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;START AT ROM PC=0

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;JUMP TO ROM PC OF 1777

;R4=CRAM PC (LSB 8 BITS)

;EXPECTED DATA

;IS ROM PC CORRECT?

;BR IF YES

;ERROR, CRAM PC IS WRONG

;LOOP TO 1\$ IF SW09=1

;NEW SCOP1

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;START AT ROM PC=3

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;JUMP TO ROM PC OF 0

;R4=CRAM PC (LSB 8 BITS)

;EXPECTED DATA

;IS ROM PC CORRECT?

;BR IF YES

;ERROR, CRAM PC IS WRONG

;LOOP TO 3\$ IF SW09=1

;NEW SCOP1

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;START AT ROM PC=6

;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304

;JUMP TO ROM PC OF 525

L16

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PAGE: 0206

3094 024164 004737 035550
3095 024170 000125
3096 024172 120504
3097 024174 001401
3098 024176 104005
3099 024200 104401
3100 024202 104400

6\$:

JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
125 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 6\$;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
SCOPI ;LOOP TO 5\$ IF SW59=1
SCOPE ;SCOPE THIS TEST

***** TEST 35 *****
*CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
*SET THE Z BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL. IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37

: TEST 35

3116 024204 012737 000035 001226
3117 024212 012737 024400 001216
3118 024220 012737 024244 001220
3119
3120 024226 104412
3121 024230 032737 100000 001366
3122 024236 001457
3123 024240 004737 035654
3124 024244
3125 024244 004737 035514
3126 024250 104414
3127 024252 100400
3128 024254 104414
3129 024256 115777
3130 024260 004737 035550
3131 024264 000377
3132 024266 120504
3133 024270 001401
3134 024272 104005
3135 024274 104401
3136 024276 012737 024304 001220
3137 024304
3138 024304 004737 035514
3139 024310 104414
3140 024312 100403
3141 024314 104414
3142 024316 101400
3143 024320 004737 035550
3144 024324 000000
3145 024326 120504
3146 024330 001401
3147 024332 104005
3148 024334 104401
3149 024336 012737 024344 001220

TST35:

1\$:

2\$:

3\$:

4\$:

MOV #35,TSTNO
MOV #TST36,NEXT
MOV #1\$,LOCK
MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
BEQ 6\$+2 ;IS IT CRAM?
JSR PC,MEMSET ;SKIP TEST IF NO
;SET MEM AND RAM
JSR PC,SETZ ;SET THE Z BIT'
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400 ;START AT ROM PC=0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377! <400*3> ;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
377 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 2\$;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
SCOPI ;LOOP TO 1\$ IF SW09=1
MOV #3\$,LOCK ;NEW SCOPI
JSR PC,SETZ ;SET THE Z BIT'
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100403 ;START AT ROM PC=3
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000! <400*3> ;JUMP TO ROM PC OF 0
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
0 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 4\$;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
SCOPI ;LOOP TO 3\$ IF SW09=1
MOV #5\$,LOCK ;NEW SCOPI

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 DZDMH.P11 09-DEC-76 14:59 CRAM JUMP TESTS

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3150 024344          5$:
3151 024344 004737 035514      JSR      PC,SETZ ;SET THE Z BIT'
3152 024350 104414          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3153 024352 100406          100406    ;START AT ROM PC=6
3154 024354 104414          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3155 024356 105525          104125! <400*3> ;JUMP TO ROM PC OF 525
3156 024360 004737 035550      JSR      PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3157 024364 000125          125        ;EXPECTED DATA
3158 024366 120504          CMPB      R5,R4 ;IS ROM PC CORRECT?
3159 024370 001401          BEQ       6$    ;BR IF YES
3160 024372 104005          HLT       5     ;ERROR, CRAM PC IS WRONG
3161 024374 104401          6$:         ;LOOP TO 5$ IF SW59=1
3162 024376 104400          SCOP1      ;SCOPE THIS TEST
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3177
3178 024400 012737 000036 001226      ;***** TEST 36 *****
3179 024406 012737 024574 001216      ;*CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
3180 024414 012737 024440 001220      ;*SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION.
3181
3182 024422 104412          ;*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
3183 024424 032737 100000 001366      ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
3184 024432 001457          ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3185 024434 004737 035654          ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
3186 024440          ;*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
3187 024440 004737 035446          ;*THEN PORT4 WILL CONTAIN A 37
3188 024444 104414          ;*****
3189 024446 100400          : TEST 36
3190 024450 104414          :-----
3191 024452 116377          TST36: MOV     #36,TSTNO
3192 024454 004737 035550      MOV     #TST37,NEXT
3193 024460 000377          MOV     #1$,LOCK
3194 024462 120504          MSTCLR          ;R1 CONTAINS BASE DMC11 ADDRESS
3195 024464 001401          BIT      #BIT15,STAT1 ;MASTER CLEAR DMC11
3196 024466 104005          BEQ      6$+2    ;IS IT CRAM?
3197 024470 104401          JSR      PC,MEMSET ;SKIP TEST IF NO
3198 024472 012737 024500 001220      ;SET MEM AND RAM
3199 024500          1$: JSR      PC,SETBRO ;SET THE BRO BIT'
3200 024500 004737 035446      ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3201 024504 104414          100400    ;START AT ROM PC=0
3202 024506 100403          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3203 024510 104414          114377! <400*4> ;JUMP TO ROM PC OF 1777
3204 024512 102000          JSR      PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3205 024514 004737 035550      377      ;EXPECTED DATA
          CMPB      R5,R4 ;IS ROM PC CORRECT?
          BEQ      2$     ;BR IF YES
          HLT      5     ;ERROR, CRAM PC IS WRONG
          SCOP1      ;LOOP TO 1$ IF SW09=1
          MOV      #3$,LOCK ;NEW SCOPE
          2$: JSR      PC,SETBRO ;SET THE BRO BIT'
          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
          100403    ;START AT ROM PC=3
          ROMCLK    ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
          100000! <400*4> ;JUMP TO ROM PC OF 0
          JSR      PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)

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Address	Hex	Hex	Hex	Hex	Label	Assembly	Comments
3206	024520	000000				0	; EXPECTED DATA
3207	024522	120504				CMPB R5,R4	; IS ROM PC CORRECT?
3208	024524	001401				BEQ 4\$	; BR IF YES
3209	024526	104005				HLT 5	; ERROR, CRAM PC IS WRONG
3210	024530	104401			4\$:	SCOP1	; LOOP TO 3\$ IF SW09=1
3211	024532	012737	024540	001220		MOV #5\$,LOCK	; NEW SCOP1
3212	024540				5\$:		
3213	024540	004737	035446			JSR PC,SETBR0	; SET THE BR0 BIT
3214	024544	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3215	024546	100406				100406	; START AT ROM PC=6
3216	024550	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3217	024552	106125				104125! <400*4>	; JUMP TO ROM PC OF 525
3218	024554	004737	035550			JSR PC,RAMDAT	; R4=CRAM PC (LSB 8 BITS)
3219	024560	000125				125	; EXPECTED DATA
3220	024562	120504				CMPB R5,R4	; IS ROM PC CORRECT?
3221	024564	001401				BEQ 6\$	; BR IF YES
3222	024566	104005				HLT 5	; ERROR, CRAM PC IS WRONG
3223	024570	104401			6\$:	SCOP1	; LOOP TO 5\$ IF SW59=1
3224	024572	104400				SCOPE	; SCOPE THIS TEST
3225							
3226							
3227							
3228							***** TEST 37 *****
3229							*CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
3230							*SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
3231							*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
3232							*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
3233							*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3234							*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
3235							*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
3236							*THEN PORT4 WILL CONTAIN A 37
3237							: *****
3238							
3239							: TEST 37
3240	024574	012737	000037	001226	TST37:	MOV #37,TSTNO	
3241	024602	012737	024770	001216		MOV #TST40,NEXT	
3242	024610	012737	024634	001220		MOV #1\$,LOCK	
3243							
3244	024616	104412				MSTCLR	; R1 CONTAINS BASE DMC11 ADDRESS
3245	024620	032737	100000	001366		BIT #BIT15,STAT1	; MASTER CLEAR DMC11
3246	024626	001457				BEQ 6\$+2	; IS IT CRAM?
3247	024630	004737	035654			JSR PC,MEMSET	; SKIP TEST IF NO
3248	024634				1\$:		; SET MEM AND RAM
3249	024634	004737	035454			JSR PC,SETBR1	; SET THE BR1 BIT
3250	024640	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3251	024642	100400				100400	; START AT ROM PC=0
3252	024644	104414				ROMCLK	; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3253	024646	116777				114377! <400*5>	; JUMP TO ROM PC OF 1777
3254	024650	004737	035550			JSR PC,RAMDAT	; R4=CRAM PC (LSB 8 BITS)
3255	024654	000377				377	; EXPECTED DATA
3256	024656	120504				CMPB R5,R4	; IS ROM PC CORRECT?
3257	024660	001401				BEQ 2\$	; BR IF YES
3258	024662	104005				HLT 5	; ERROR, CRAM PC IS WRONG
3259							

C01

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PAGE: 0209

3262	024674	004737	035454		JSR	PC,SETBR1	;SET THE BR1 BIT'
3263	024700	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3264	024702	100403			100403		;START AT ROM PC=3
3265	024704	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3266	024706	102400			100000!	<400*5>	JUMP TO ROM PC OF 0
3267	024710	004737	035550		JSR	PC,RAMDAT	R4=CRAM PC (LSB 8 BITS)
3268	024714	000000			0		EXPECTED DATA
3269	024716	120504			CMPB	R5,R4	IS ROM PC CORRECT?
3270	024720	001401			BEQ	4\$	BR IF YES
3271	024722	104005			HLT	5	ERROR, CRAM PC IS WRONG
3272	024724	104401			SCOPI		LOOP TO 3\$ IF SW09=1
3273	024726	012737	024734	001220	MOV	#5\$,LOCK	NEW SCOPI
3274	024734						
3275	024734	004737	035454		JSR	PC,SETBR1	;SET THE BR1 BIT'
3276	024740	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3277	024742	100406			100406		;START AT ROM PC=6
3278	024744	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3279	024746	106525			104125!	<400*5>	JUMP TO ROM PC OF 525
3280	024750	004737	035550		JSR	PC,RAMDAT	R4=CRAM PC (LSB 8 BITS)
3281	024754	000125			125		EXPECTED DATA
3282	024756	120504			CMPB	R5,R4	IS ROM PC CORRECT?
3283	024760	001401			BEQ	6\$	BR IF YES
3284	024762	104005			HLT	5	ERROR, CRAM PC IS WRONG
3285	024764	104401			SCOPI		LOOP TO 5\$ IF SW59=1
3286	024766	104400			SCOPE		SCOPE THIS TEST
3287							
3288							
3289							
3290							
3291							
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3299							
3300							
3301							
3302	024770	012737	000040	001226	TST40:	MOV	#40,TSTNO
3303	024776	012737	025164	001216		MOV	#TST41,NEXT
3304	025004	012737	025030	001220		MOV	#1\$,LOCK
3305							
3306	025012	104412			MSTCLR		R1 CONTAINS BASE DMC11 ADDRESS
3307	025014	032737	100000	001366	BIT	#BIT15,STAT1	MASTER CLEAR DMC11
3308	025022	001457			BEQ	6\$+2	IS IT CRAM?
3309	025024	004737	035654		JSR	PC,MEMSET	SKIP TEST IF NO
3310	025030						SET MEM AND RAM
3311	025030	004737	035462		JSR	PC,SETBR4	;SET THE BR4 BIT'
3312	025034	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3313	025036	100400			100400		;START AT ROM PC=0
3314	025040	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3315	025042	117377			114377!	<400*6>	JUMP TO ROM PC OF 1777
3316	025044	004737	035550		JSR	PC,RAMDAT	R4=CRAM PC (LSB 8 BITS)
3317	025050	000377			377		EXPECTED DATA

***** TEST 40 *****
 ;CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
 ;SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.
 ;VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
 ;IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
 ;BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
 ;THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
 ;THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
 ;THEN PORT4 WILL CONTAIN A 37
 ;*****

; TEST 40

TST40: MOV #40,TSTNO
 MOV #TST41,NEXT
 MOV #1\$,LOCK

1\$:

MSTCLR
 BIT #BIT15,STAT1
 BEQ 6\$+2
 JSR PC,MEMSET

JSR PC,SETBR4
 ROMCLK
 100400
 ROMCLK
 114377!<400*6>
 JSR PC,RAMDAT
 377

R1 CONTAINS BASE DMC11 ADDRESS
 MASTER CLEAR DMC11
 IS IT CRAM?
 SKIP TEST IF NO
 SET MEM AND RAM

;SET THE BR4 BIT'
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;START AT ROM PC=0
 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
 ;JUMP TO ROM PC OF 1777
 ;R4=CRAM PC (LSB 8 BITS)
 ;EXPECTED DATA

001

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PAGE: 0210

3318	025052	120504				CMPB	R5,R4	; IS ROM PC CORRECT?
3319	025054	001401				BEQ	2\$	; BR IF YES
3320	025056	104005				HLT	5	; ERROR, CRAM PC IS WRONG
3321	025060	104401			2\$:	SCOP1		; LOOP TO 1\$ IF SW09=1
3322	025062	012737	025070	001220		MOV	#3\$,LOCK	; NEW SCOP1
3323	025070				3\$:			
3324	025070	004737	035462			JSR	PC,SETBR4	; SET THE BR4 BIT'
3325	025074	104414				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3326	025076	100403				100403		; START AT ROM PC=3
3327	025100	104414				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3328	025102	103000				100000! <400*6>	JUMP TO	ROM PC OF 0
3329	025104	004737	035550			JSR	PC,RAMDAT	; R4=CRAM PC (LSB 8 BITS)
3330	025110	000000				0		; EXPECTED DATA
3331	025112	120504				CMPB	R5,R4	; IS ROM PC CORRECT?
3332	025114	001401				BEQ	4\$	; BR IF YES
3333	025116	104005				HLT	5	; ERROR, CRAM PC IS WRONG
3334	025120	104401			4\$:	SCOP1		; LOOP TO 3\$ IF SW09=1
3335	025122	012737	025130	001220		MOV	#5\$,LOCK	; NEW SCOP1
3336	025130				5\$:			
3337	025130	004737	035462			JSR	PC,SETBR4	; SET THE BR4 BIT'
3338	025134	104414				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3339	025136	100406				100406		; START AT ROM PC=6
3340	025140	104414				ROMCLK		; NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3341	025142	107125				104125! <400*6>	JUMP TO	ROM PC OF 525
3342	025144	004737	035550			JSR	PC,RAMDAT	; R4=CRAM PC (LSB 8 BITS)
3343	025150	000125				125		; EXPECTED DATA
3344	025152	120504				CMPB	R5,R4	; IS ROM PC CORRECT?
3345	025154	001401				BEQ	6\$	; BR IF YES
3346	025156	104005				HLT	5	; ERROR, CRAM PC IS WRONG
3347	025160	104401			6\$:	SCOP1		; LOOP TO 5\$ IF SW59=1
3348	025162	104400				SCOPE		; SCOPE THIS TEST

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***** TEST 41 *****
*CRAM TEST OF JUMP(1) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT,
*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
*THEN PORT4 WILL CONTAIN A 37
:*****

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025164 012737 000041 001226
025172 012737 025360 001216
025200 012737 025224 001220

TST41: MOV #41,TSTNO
MOV #TST42,NEXT
MOV #1\$,LOCK

MSTCLR
BIT #BIT15,STAT1
BEQ 6\$+2
JSR PC,MEMSET
1\$: JSR PC,SETBR7

; R1 CONTAINS BASE DMC11 ADDRESS
; MASTER CLEAR DMC11
; IS IT CRAM?
; SKIP TEST IF NO
; SET MEM AND RAM
; SET THE BR7 BIT'

E01

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PAGE: 0211

3374	025230	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3375	025232	100400			100400		;START AT ROM PC=0
3376	025234	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3377	025236	117777			114377! <400*7>		;JUMP TO ROM PC OF 1777
3379	025240	004737	035550		JSR	PC,RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3379	025244	000377			377		;EXPECTED DATA
3380	025246	120504			CMPB	R5,R4	;IS ROM PC CORRECT?
3381	025250	001401			BEQ	2\$	;BR IF YES
3382	025252	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3383	025254	104401			SCOP1		;LOOP TO 1\$ IF SW09=1
3384	025256	012737	025264	001220	MOV	#3\$,LOCK	;NEW SCOP1
3385	025264						
3386	025264	004737	035470		JSR	PC,SETBR7	;SET THE BR7 BIT
3387	025270	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3388	025272	100403			100403		;START AT ROM PC=3
3389	025274	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3390	025276	103400			100000! <400*7>	JUMP TO	ROM PC OF 0
3391	025300	004737	035550		JSR	PC,RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3392	025304	000000			0		;EXPECTED DATA
3393	025306	120504			CMPB	R5,R4	;IS ROM PC CORRECT?
3394	025310	001401			BEQ	4\$	;BR IF YES
3395	025312	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3396	025314	104401			SCOP1		;LOOP TO 3\$ IF SW09=1
3397	025316	012737	025324	001220	MOV	#5\$,LOCK	;NEW SCOP1
3398	025324						
3399	025324	004737	035470		JSR	PC,SETBR7	;SET THE BR7 BIT
3400	025330	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3401	025332	100406			100406		;START AT ROM PC=6
3402	025334	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3403	025336	107525			104125! <400*7>		;JUMP TO ROM PC OF 525
3404	025340	004737	035550		JSR	PC,RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3405	025344	000125			125		;EXPECTED DATA
3406	025346	120504			CMPB	R5,R4	;IS ROM PC CORRECT?
3407	025350	001401			BEQ	6\$	;BR IF YES
3408	025352	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3409	025354	104401			SCOP1		;LOOP TO 5\$ IF SW59=1
3410	025356	104400			SCOPE		;SCOPE THIS TEST

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***** TEST 42 *****
 ;*CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.
 ;*CLEAR THE C BIT, PERFORM THE JUMP INSTRUCTION,
 ;*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
 ;*IN THE LOCATION IT IS AT, THIS INSTRUCTION LOADS THE
 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
 ;*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
 ;*THEN PORT4 CONTAINS A 37
 ;*****

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025360	012737	000042	001226		TST42:	MOV	#42,TSTNO
025366	012737	025554	001216			MOV	#TST43,NEXT
025374	012737	025420	001220			MOV	#1\$,LOCK

;R1 CONTAINS BASE DMC11 ADDRESS

F01

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PAGE: 0212

3430	025402	104412			MSTCLR		;MASTER CLEAR DMC11
3431	025404	032737	100000	001366	BIT	#BIT15,STAT1	;IS IT CRAM?
3432	025412	001457			BEQ	6\$+2	;SKIP TEST IF NO
3433	025414	004737	035654		JSR	PC, MEMSET	;SET MEM AND RAM
3434	025420						
3435	025420	004737	035430		JSR	PC, CLRALL	;CLEAR ALL CONDITIONS
3436	025424	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3437	025426	100400			100400		;START AT ROM PC=0
3438	025430	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3439	025432	115377			114377! <400*2>		;JUMP TO ROM PC OF 1777
3440	025434	004737	035550		JSR	PC, RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3441	025440	000001			1		;EXPECTED DATA
3442	025442	120504			CMPB	R5, R4	;IS ROM PC CORRECT?
3443	025444	001401			BEQ	2\$	;BR IF YES
3444	025446	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3445	025450	104401			SCOP1		;LOOP TO 1\$ IF SW09=1
3446	025452	012737	025460	001220	MOV	#3\$, LOCK	;NEW SCOP1
3447	025460						
3448	025460	004737	035430		JSR	PC, CLRALL	;CLEAR ALL CONDITIONS
3449	025464	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3450	025466	100403			100403		;START AT ROM PC=3
3451	025470	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3452	025472	101000			100000! <400*2>		;JUMP TO ROM PC OF 0
3453	025474	004737	035550		JSR	PC, RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3454	025500	000004			4		;EXPECTED DATA
3455	025502	120504			CMPB	R5, R4	;IS ROM PC CORRECT?
3456	025504	001401			BEQ	4\$	;BR IF YES
3457	025506	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3458	025510	104401			SCOP1		;LOOP TO 3\$ IF SW09=1
3459	025512	012737	025520	001220	MOV	#5\$, LOCK	;NEW SCOP1
3460	025520						
3461	025520	004737	035430		JSR	PC, CLRALL	;CLEAR ALL CONDITIONS
3462	025524	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3463	025526	100406			100406		;START AT ROM PC=6
3464	025530	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3465	025532	105125			104125! <400*2>		;JUMP TO ROM PC OF 525
3466	025534	004737	035550		JSR	PC, RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3467	025540	000007			7		;EXPECTED DATA
3468	025542	120504			CMPB	R5, R4	;IS ROM PC CORRECT?
3469	025544	001401			BEQ	6\$	;BR IF YES
3470	025546	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3471	025550	104401			SCOP1		;LOOP TO 5\$ IF SW59=1
3472	025552	104400			SCOPE		;SCOPE THIS TEST

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***** TEST 43 *****
*CRAM TEST OF JUMP(1) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION,
*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
*THEN PORT4 CONTAINS A 37
*****

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3488 025554 012737 000043 001226
3489 025562 012737 025750 001216
3490 025570 012737 025614 001220
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3492 025576 104412
3493 025600 032737 100000 001366
3494 025606 001457
3495 025610 004737 035654
3496 025614
3497 025614 004737 035430
3498 025620 104414
3499 025622 100400
3500 025624 104414
3501 025626 115777
3502 025630 004737 035550
3503 025634 000001
3504 025636 120504
3505 025640 001401
3506 025642 104005
3507 025644 104401
3508 025646 012737 025654 001220
3509 025654
3510 025654 004737 035430
3511 025660 104414
3512 025662 100403
3513 025664 104414
3514 025666 101400
3515 025670 004737 035550
3516 025674 000004
3517 025676 120504
3518 025700 001401
3519 025702 104005
3520 025704 104401
3521 025706 012737 025714 001220
3522 025714
3523 025714 004737 035430
3524 025720 104414
3525 025722 100406
3526 025724 104414
3527 025726 105525
3528 025730 004737 035550
3529 025734 000007
3530 025736 120504
3531 025740 001401
3532 025742 104005
3533 025744 104401
3534 025746 104400
3535
3536
3537
3538
3539
3540
3541

```

```

; TEST 43
TST43: MOV #43,TSTNO
MOV #TST44,NEXT
MOV #1$,LOCK

MSTCLR
BIT #BIT15,STAT1
BEQ 6$+2
JSR PC,MEMSET

1$: JSR PC,CLRALL
ROMCLK
100400
ROMCLK
114377! <400*3>
JSR PC,RAMDAT
1
CMPB R5,R4
BEQ 2$
HLT 5

2$: SCOP1
MOV #3$,LOCK

3$: JSR PC,CLRALL
ROMCLK
100403
ROMCLK
100000! <400*3>
JSR PC,RAMDAT
4
CMPB R5,R4
BEQ 4$
HLT 5

4$: SCOP1
MOV #5$,LOCK

5$: JSR PC,CLRALL
ROMCLK
100406
ROMCLK
104125! <400*3>
JSR PC,RAMDAT
7
CMPB R5,R4
BEQ 6$
HLT 5

6$: SCOP1
SCOPE

```

```

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS IT CRAM?
;SKIP TEST IF NO
;SET MEM AND RAM

;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=0
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 1777
;R4=CRAM PC (LSB 8 BITS)
;EXPECTED DATA
;IS ROM PC CORRECT?
;BR IF YES
;ERROR, CRAM PC IS WRONG
;LOOP TO 1$ IF SW09=1
;NEW SCOP1

;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=3
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 0
;R4=CRAM PC (LSB 8 BITS)
;EXPECTED DATA
;IS ROM PC CORRECT?
;BR IF YES
;ERROR, CRAM PC IS WRONG
;LOOP TO 3$ IF SW09=1
;NEW SCOP1

;CLEAR ALL CONDITIONS
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;START AT ROM PC=6
;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;JUMP TO ROM PC OF 525
;R4=CRAM PC (LSB 8 BITS)
;EXPECTED DATA
;IS ROM PC CORRECT?
;BR IF YES
;ERROR, CRAM PC IS WRONG
;LOOP TO 5$ IF SW59=1
;SCOPE THIS TEST

```

```

***** TEST 44 *****
;*CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
;*CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION.
;*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE

```

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3542 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3543 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
3544 ;*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
3545 ;*THEN PORT4 CONTAINS A 37
3546 ;:*****
3547
3548 ; TEST 44
3549 ;-----
3550 025750 012737 000044 001226 TST44: MOV #44,TSTNO
3551 025756 012737 026144 001216 MOV #TST45,NEXT
3552 025764 012737 026010 001220 MOV #1$,LOCK
3553
3554 025772 104412 MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
3555 025774 032737 100000 001366 BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
3556 026002 001457 BEQ 6$+2 ;IS IT CRAM?
3557 026004 004737 035654 JSR PC,MEMSET ;SKIP TEST IF NO
3558 026010 004737 035430 1$: JSR PC,CLRALL ;SET MEM AND RAM
3559 026010 104414 ROMCLK ;CLEAR ALL CONDITIONS
3560 026016 100400 100400 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3561 026020 104414 ROMCLK ;START AT ROM PC=0
3562 026022 116377 114377!<400*4> ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3563 026024 004737 035550 JSR PC,RAMDAT ;JUMP TO ROM PC OF 1777
3564 026030 000001 1 CMPB R5,R4 ;R4=CRAM PC (LSB 8 BITS)
3565 026032 120504 BEQ 2$ ;EXPECTED DATA
3566 026034 001401 HLT 5 ;IS ROM PC CORRECT?
3567 026036 104005 2$: SCOP1 ;BR IF YES
3568 026040 104401 3$: MOV #3$,LOCK ;ERROR, CRAM PC IS WRONG
3569 026042 012737 026050 001220 ;LOOP TO 1$ IF SW09=1
3570 026050 004737 035430 4$: JSR PC,CLRALL ;NEW SCOP1
3571 026054 104414 ROMCLK ;CLEAR ALL CONDITIONS
3572 026056 100403 100403 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3573 026060 104414 ROMCLK ;START AT ROM PC=3
3574 026062 102000 100000!<400*4> ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3575 026064 004737 035550 JSR PC,RAMDAT ;JUMP TO ROM PC OF 0
3576 026070 000004 4 CMPB R5,R4 ;R4=CRAM PC (LSB 8 BITS)
3577 026072 120504 BEQ 4$ ;EXPECTED DATA
3578 026074 001401 HLT 5 ;IS ROM PC CORRECT?
3579 026076 104005 4$: SCOP1 ;BR IF YES
3580 026100 104401 5$: MOV #5$,LOCK ;ERROR, CRAM PC IS WRONG
3581 026102 012737 026110 001220 ;LOOP TO 3$ IF SW09=1
3582 026110 004737 035430 5$: JSR PC,CLRALL ;NEW SCOP1
3583 026114 104414 ROMCLK ;CLEAR ALL CONDITIONS
3584 026116 100406 100406 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3585 026120 104414 ROMCLK ;START AT ROM PC=6
3586 026122 106125 104125!<400*4> ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3587 026124 004737 035550 JSR PC,RAMDAT ;JUMP TO ROM PC OF 525
3588 026130 000007 7 CMPB R5,R4 ;R4=CRAM PC (LSB 8 BITS)
3589 026132 120504 BEQ 6$ ;EXPECTED DATA
3590 026134 001401 HLT 5 ;IS ROM PC CORRECT?
3591 026136 104005 6$: SCOP1 ;BR IF YES
3592 026140 104401 6$: SCOP1 ;ERROR, CRAM PC IS WRONG
3593 026142 104400 SCOPE ;LOOP TO 5$ IF SW59=1
3594 ;SCOPE THIS TEST
3595
3596
3597

```

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3598
3599
3600
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3603
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3606
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3608
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3610
3611
3612 026144 012737 000045 001226
3613 026152 012737 026340 001216
3614 026160 012737 026204 001220
3615
3616 026166 104412
3617 026170 032737 100000 001366
3618 026176 001457
3619 026200 004737 035654
3620 026204
3621 026204 004737 035430
3622 026210 104414
3623 026212 100400
3624 026214 104414
3625 026216 116777
3626 026220 004737 035550
3627 026224 000001
3628 026226 120504
3629 026230 001401
3630 026232 104005
3631 026234 104401
3632 026236 012737 026244 001220
3633 026244
3634 026244 004737 035430
3635 026250 104414
3636 026252 100403
3637 026254 104414
3638 026256 102400
3639 026260 004737 035550
3640 026264 000004
3641 026266 120504
3642 026270 001401
3643 026272 104005
3644 026274 104401
3645 026276 012737 026304 001220
3646 026304
3647 026304 004737 035430
3648 026310 104414
3649 026312 100406
3650 026314 104414
3651 026316 106525
3652 026320 004737 035550
3653 026324 000007

```

```

***** TEST 45 *****
*CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
*CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
*THEN PORT4 CONTAINS A 37
*****

```

; TEST 45

```

TST45: MOV #45,TSTNO
MOV #TST46,NEXT
MOV #1$,LOCK

MSTCLR ;R1 CONTAINS BASE DMC11 ADDRESS
BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
BEQ 6$+2 ;IS IT CRAM?
JSR PC,MEMSET ;SKIP TEST IF NO
;SET MEM AND RAM

1$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100400 ;START AT ROM PC=0
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
114377! <400*5> ;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
1 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 2$ ;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
2$: SCOP1 ;LOOP to 1$ IF SW09=1
MOV #3$,LOCK ;NEW SCOP1

3$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100403 ;START AT ROM PC=3
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100000! <400*5> ;JUMP TO ROM PC OF 0
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
4 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 4$ ;BR IF YES
HLT 5 ;ERROR, CRAM PC IS WRONG
4$: SCOP1 ;LOOP to 3$ IF SW09=1
MOV #5$,LOCK ;NEW SCOP1

5$: JSR PC,CLRALL ;CLEAR ALL CONDITIONS
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
100406 ;START AT ROM PC=6
ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
104125! <400*5> ;JUMP TO ROM PC OF 525
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
7 ;EXPECTED DATA

```

Address	Hex	Dec	Label	Instruction	Comment
3654	026326	120504		CMPB R5,R4	;IS ROM PC CORRECT?
3655	026330	001401		BEQ 6\$	;BR IF YES
3656	026332	104005		HLT 5	;ERROR, CRAM PC IS WRONG
3657	026334	104401	6\$:	SCOPI	;LOOP TO 5\$ IF SW59=1
3658	026336	104400		SCOPE	;SCOPE THIS TEST
3659					
3660					
3661					***** TEST 46 *****
3662					;*CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.
3663					;*CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION,
3664					;*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
3665					;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
3666					;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3667					;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
3668					;*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT,
3669					;*THEN FORT4 CONTAINS A 37
3670					*****
3671					
3672					
3673					; TEST 46
3674	026340	012737	000046	001226	TST46: MOV #46,TSTNO
3675	026346	012737	026534	001216	MOV #TST47,NEXT
3676	026354	012737	026400	001220	MOV #1\$,LOCK
3677					
3678	026362	104412			MSICLR ;R1 CONTAINS BASE DMC11 ADDRESS
3679	026364	032737	100000	001366	BIT #BIT15,STAT1 ;MASTER CLEAR DMC11
3680	026372	001457			BEQ 6\$+2 ;IS IT CRAM?
3681	026374	004737	035654		JSR PC,MEMSET ;SKIP TEST IF NO
3682	026400				1\$: ;SET MEM AND RAM
3683	026400	004737	035430		JSR PC,CLRALL ;CLEAR ALL CONDITIONS
3684	026404	104414			ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3685	026406	100400			100400 ;START AT ROM PC=0
3686	026410	104414			ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3687	026412	117377			114377! <400*6> ;JUMP TO ROM PC OF 1777
3688	026414	004737	035550		JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3689	026420	000001			1 ;EXPECTED DATA
3690	026422	120504			CMPB R5,R4 ;IS ROM PC CORRECT?
3691	026424	001401			BEQ 2\$;BR IF YES
3692	026426	104005			HLT 5 ;ERROR, CRAM PC IS WRONG
3693	026430	104401			2\$: SCOPI ;LOOP TO 1\$ IF SW09=1
3694	026432	012737	026440	001220	MOV #3\$,LOCK ;NEW SCOPI
3695	026440				3\$:
3696	026440	004737	035430		JSR PC,CLRALL ;CLEAR ALL CONDITIONS
3697	026444	104414			ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3698	026446	100403			100403 ;START AT ROM PC=3
3699	026450	104414			ROMCLK ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3700	026452	103000			100000! <400*6> ;JUMP TO ROM PC OF 0
3701	026454	004737	035550		JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
3702	026460	000004			4 ;EXPECTED DATA
3703	026462	120504			CMPB R5,R4 ;IS ROM PC CORRECT?
3704	026464	001401			BEQ 4\$;BR IF YES
3705	026466	104005			HLT 5 ;ERROR, CRAM PC IS WRONG
3706	026470	104401			4\$: SCOPI ;LOOP TO 3\$ IF SW09=1
3707	026472	012737	026500	001220	MOV #5\$,LOCK ;NEW SCOPI
3708	026500				5\$:
3709	026500	004737	035430		JSR PC,CLRALL ;CLEAR ALL CONDITIONS

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3710	026504	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3711	026506	100406			100406		;START AT ROM PC=6
3712	026510	104414			ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3713	026512	107125			104125! <400*6>		;JUMP TO ROM PC OF 525
3714	026514	004737	035550		JSR	PC,RAMDAT	;R4=CRAM PC (LSB 8 BITS)
3715	026520	000007			7		;EXPECTED DATA
3716	026522	120504			CMPB	R5,R4	;IS ROM PC CORRECT?
3717	026524	001401			BEQ	6\$	;BR IF YES
3718	026526	104005			HLT	5	;ERROR, CRAM PC IS WRONG
3719	026530	104401			SCOPI		;LOOP TO 5\$ IF SW59=1
3720	026532	104400			SCOPE		;SCOPE THIS TEST
3721							
3722							
3723							
3724							
3725							
3726							
3727							
3728							
3729							
3730							
3731							
3732							
3733							
3734							
3735							
3736	026534	012737	000047	001226	TST47:	MOV	#47,TSTNO
3737	026542	012737	026730	001216		MOV	#TST50,NEXT
3738	026550	012737	026574	001220		MOV	#1\$,LOCK
3739							
3740	026556	104412				MSTCLR	;R1 CONTAINS BASE DMC11 ADDRESS
3741	026560	032737	100000	001366		BIT	;MASTER CLEAR DMC11
3742	026566	001457				BEQ	;IS IT CRAM?
3743	026570	004737	035654			JSR	;SKIP TEST IF NO
3744	026574						;SET MEM AND RAM
3745	026574	004737	035430		1\$:	JSR	;CLEAR ALL CONDITIONS
3746	026600	104414				ROMCLK	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3747	026602	100400				100400	;START AT ROM PC=0
3748	026604	104414				ROMCLK	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3749	026606	117777				114377! <400*7>	;JUMP TO ROM PC OF 1777
3750	026610	004737	035550			JSR	;R4=CRAM PC (LSB 8 BITS)
3751	026614	000001				1	;EXPECTED DATA
3752	026616	120504				CMPB	;IS ROM PC CORRECT?
3753	026620	001401				BEQ	;BR IF YES
3754	026622	104005				HLT	;ERROR, CRAM PC IS WRONG
3755	026624	104401			2\$:	SCOPI	;LOOP TO 1\$ IF SW09=1
3756	026626	012737	026634	001220		MOV	;NEW SCOPI
3757	026634				3\$:		
3758	026634	004737	035430			JSR	;CLEAR ALL CONDITIONS
3759	026640	104414				ROMCLK	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3760	026642	100403				100403	;START AT ROM PC=3
3761	026644	104414				ROMCLK	;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3762	026646	103400				100000! <400*7>	;JUMP TO ROM PC OF 0
3763	026650	004737	035550			JSR	;R4=CRAM PC (LSB 8 BITS)
3764	026654	000004				4	;EXPECTED DATA
3765	026656	120504				CMPB	;IS ROM PC CORRECT?

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3766	026660	001401			BEQ	4\$		;BR IF YES
3767	026662	104005			HLT	5		;ERROR, CRAM PC IS WRONG
3768	026664	104401			SCOP1			;LOOP TO 3\$ IF SW09=1
3769	026666	012737	026674	001220	MOV	#5\$,LOCK		;NEW SCOP1
3770	026674							
3771	026674	004737	035430		JSR	PC,CLRALL		;CLEAR ALL CONDITIONS
3772	026700	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3773	026702	100406			100406			;START AT ROM PC=6
3774	026704	104414			ROMCLK			;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
3775	026706	107525			104125!<400*7>			;JUMP TO ROM PC OF 525
3776	026710	004737	035550		JSR	PC,RAMDAT		;R4=CRAM PC (LSB 8 BITS)
3777	026714	000007			7			;EXPECTED DATA
3778	026716	120504			CMPB	R5,R4		;IS ROM PC CORRECT?
3779	026720	001401			BEQ	6\$		;BR IF YES
3780	026722	104005			HLT	5		;ERROR, CRAM PC IS WRONG
3781	026724	104401			SCOP1			;LOOP TO 5\$ IF SW59=1
3782	026726	104400			SCOPE			;SCOPE THIS TEST
3783								
3784								
3785								
3786								
3787								
3788								
3789								
3790								
3791								
3792								
3793								
3794								
3795								
3796								
3797								
3798	026730	012737	000050	001226	TST50: MOV	#50,TSTNO		
3799	026736	012737	027742	001216	MOV	#TST51,NEXT		
3800								
3801	026744	104412			MSTCLR			;R1 CONTAINS BASE DMC11 ADDRESS
3802	026746	032737	100000	001366	BIT	#BIT15,STAT1		;MASTER CLEAR DMC11
3803	026754	001406			BEQ	+.16		;IS IT A DMC?
3804	026756	032737	000001	001372	BIT	#BIT0,STAT3		;BR IF YES
3805	026764	001002			BNE	+.6		;KMC WITH BIT0 SET?
3806	026766	000137	027740		JMP	14\$		;BR IF YES
3807	026772	032737	010000	001366	BIT	#BIT12,STAT1		;SKIP TEST
3808	027000	001372			BNE	.-12		;LU PRESENT?
3809	027002	004737	035602		JSR	PC,WROM		;BR IF NO
3810	027006	013700	034760		MOV	RCOUNT,R0		;WRITE MAP IN CRAM
3811	027012	062700	000002		ADD	#2,R0		;CLEAR RECEIVER BUFFER
3812	027016	012702	034762		MOV	#RBUF,R2		;CLEAR 2 MORE LOCATIONS
3813	027022	105022			CLRB	(R2)+		;CLEAR OUT RECEIVE BUFFER
3814	027024	005300			DEC	R0		;CLEAR BUFFER
3815	027026	001375			BNE	10\$		;DONE YET!
3816	027030	005037	034706		CLR	TFLAG		;NO
3817	027034	005037	034710		CLR	RFLAG		;SET TFLAG TO 0
3818	027040	012711	040000		MOV	#BIT14,(R1)		;SET RFLAG TO 0
3819	027044	032737	100000	001366	BIT	#BIT15,STAT1		;MASTER CLEAR
3820	027052	001402			BEQ	+.6		;CRAM?
3821	027054	012711	100000		MOV	#BIT15,(R1)		;BR IF NO
								;IF CRAM SET RUN

***** TEST 50 *****
 *FREE RUNNING FLAG MODE DATA TEST
 *TRANSMIT A MESSAGE AND VERIFY THE RECEIVED DATA
 *IF NO TURNAROUND CONNECTOR IS ON LINE UNIT LOOP IS SET.
 *ALL FOLLOWING TESTS ARE FREE RUNNING AND ARE PERFORMED
 *ONLY ON DMC'S WITH LINE UNITS. IF YOU WISH TO PERFORM
 *THESE FREE RUNNING TESTS ON A KMC (NORMALLY THE FREE RUNNING TESTS
 *WILL FAIL ON A KMC, THE TIMER IS TOO FAST) THEN YOU MUST
 *MANUALLY SET BIT0 OF STAT3 IN THE STATUS MAP.

 : TEST 50
 :-----
 TST50: MOV #50,TSTNO
 MOV #TST51,NEXT
 MSTCLR
 BIT #BIT15,STAT1
 BEQ .+16
 BIT #BIT0,STAT3
 BNE .+6
 JMP 14\$
 BIT #BIT12,STAT1
 BNE .-12
 JSR PC,WROM
 MOV RCOUNT,R0
 ADD #2,R0
 MOV #RBUF,R2
 CLRB (R2)+
 DEC R0
 BNE 10\$
 CLR TFLAG
 CLR RFLAG
 MOV #BIT14,(R1)
 BIT #BIT15,STAT1
 BEQ .+6
 MOV #BIT15,(R1)

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3822	027060	105227	000000		INCB	#0	;DELAY
3823	027064	001375			BNE	-4	;DELAY
3824	027066	005037	001416		CLR	TEMP	;GET SET TO DELAY
3825	027072	005711		1\$:	TST	(R1)	;RUN SET?
3826	027074	100405			BMI	+14	;BR IF YES
3827	027076	005237	001416		INC	TEMP	;INC DELAY
3828	027102	001373			BNE	1\$	;BR IF NOT DONE
3829	027104	104014			HLT	14	;ERROR RUN NOT SET
3830	027106	000771			BR	1\$	;TRY AGAIN
3831	027110	032737	040000	001366	BIT	#BIT14,STAT1	;TURNAROUND CONNECTOR?
3832	027116	001002			BNE	+6	;BR IF YES
3833	027120	052711	004000		BIS	#BIT11,(R1)	;SET LINE UNIT LOOP
3834	027124	152711	000043		BISB#43,(R1)		;BASE I
3835	027130	005037	001416		CLR	TEMP	;GET SET TO DELAY
3836	027134	105711		2\$:	TSTB	(R1)	;RDI SET?
3837	027136	100404			BMI	+12	;BR IF YES
3838	027140	005237	001416		INC	TEMP	;INC DELAY
3839	027144	001373			BNE	2\$	;BR IF NOT DONE
3840	027146	104014			HLT	14	;ERROR RDI NOT SET
3841	027150	012761	035030	000004	MOV	#BASE,4(R1)	;SET UP BASE ADDRESS
3842	027156	005061	000006		CLR	6(R1)	;CLEAR COUNT
3843	027162	142711	000040		BICB	#40,(R1)	;CLEAR RQI
3844	027166	005037	001416		CLR	TEMP	;GET SET TO DELAY
3845	027172	105711		3\$:	TSTB	(R1)	;IS RDI GONE?
3846	027174	100020			BPL	8\$	;BR IF YES
3847	027176	005237	001416		INC	TEMP	;INC DELAY
3848	027202	001373			BNE	3\$	;BR IF NOT DONE
3849	027204	105761	000002		TSTB	2(R1)	;IS THERE A CNTL 0 ERROR
3850	027210	100011			BPL	18\$	;BR IF NO
3851	027212	016137	000004	001252	MOV	4(R1),TEMP3	;SAVE SEL4 FOR TYPEOUT
3852	027220	016137	000006	001254	MOV	6(R1),TEMP4	;SAVE SEL6 FOR TYPEOUT
3853	027226	104016			HLT	16	;CNTL 0 ERROR
3854	027230	000137	027740		JMP	14\$	;FATAL ERROR STOP
3855	027234	104014		18\$:	HLT	14	;ERROR RDI STILL SET
3856	027236			8\$:			
3857	027236	152711	000041		BISB	#41,(R1)	;ASK FOR CNTL I
3858	027242	105711		64\$:	TSTB	(R1)	;WAIT FOR RDI
3859	027244	100376			BPL	64\$	;BR IF NOT SETY
3860	027246	005061	000006		CLR	6(R1)	;SET FULL DUPLEX
3861	027252	142711	000040		BICB	#40,(R1)	;CLEAR RQI
3862	027256	105711		65\$:	TSTB	(R1)	;RDI UP?
3863	027260	100776			BMI	65\$	;BR IF YES
3864	027262	152711	000044		BISB	#44,(R1)	;REC BA/CC
3865	027266	005037	001416		CLR	TEMP	;GET SET TO DELAY
3866	027272	105711		4\$:	TSTB	(R1)	;IS RDI SET?
3867	027274	100404			BMI	+12	;BR IF YES
3868	027276	005237	001416		INC	TEMP	;INC DELAY
3869	027302	001373			BNE	4\$	;BR IF DELAY NOT DONE
3870	027304	104014			HLT	14	;ERROR RDI NOT SET
3871	027306	012761	034762	000004	MOV	#RBUF,4(R1)	;LOAD REC BA
3872	027314	013761	034760	000006	MOV	RCOUNT,6(R1)	;LOAD REC COUNT
3873	027322	142711	000040		BICB	#40,(R1)	;CLEAR RQI
3874	027326	005037	001416		CLR	TEMP	;GET SET TO DELAY
3875	027332	105711		5\$:	TSTB	(R1)	;RDI GONE?
3876	027334	100004			BPL	+12	;BR IF YES
3877	027336	005237	001416		INC	TEMP	;INC DELAY

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Address	Instruction	Comments
3878	027342 001373	
3879	027344 104014	
3880	027346 152711 000040	
3881	027352 005037 001416	
3882	027356 105711	6\$: TSTB (R1)
3883	027360 100404	BMI +12
3884	027362 005237 001416	INC TEMP
3885	027366 001373	BNE 6\$
3886	027370 104014	HLT 14
3887	027372 012761 034714 000004	MOV #TBUF,4(R1)
3888	027400 013761 034712 000006	MOV TCOUNT,6(R1)
3889	027406 142711 000040	BICB #40,(R1)
3890	027412 005037 001416	CLR TEMP
3891	027416 105711	7\$: TSTB (R1)
3892	027420 100004	BPL +12
3893	027422 005237 001416	INC TEMP
3894	027426 001373	BNE 7\$
3895	027430 104014	HLT 14
3896	027432 005037 001416	16\$: CLR TEMP
3897	027436 012737 000022 001246	MOV #22,TEMP1
3898	027444 105761 000002	11\$: TSTB 2(R1)
3899	027450 100407	BMI 17\$
3900	027452 005237 001416	INC TEMP
3901	027456 001372	BNE 11\$
3902	027460 005337 001246	DEC TEMP1
3903	027464 001367	BNE 11\$
3904	027466 104014	HLT 14
3905	027470 016137 000002 001250	17\$: MOV 2(R1),TEMP2
3906	027476 001001	BNE +4
3907	027500 104014	HLT 14
3908	027502 032761 000004 000002	BIT #BIT2,2(R1)
3909	027510 001032	BNE 13\$
3910	027512 005737 034706	12\$: TST TFLAG
3911	027516 001401	BEQ +4
3912	027520 104014	HLT 14
3913	027522 012737 177777 034706	MOV #-1,TFLAG
3914	027530 132761 000001 000002	BITB #BIT0,2(R1)
3915	027536 001401	BEQ +4
3916	027540 104014	HLT 14
3917	027542 022761 034714 000004	CMP #TBUF,4(R1)
3918	027550 001401	BEQ +4
3919	027552 104014	HLT 14
3920	027554 023761 034712 000006	CMP TCOUNT,6(R1)
3921	027562 001401	BEQ +4
3922	027564 104014	HLT 14
3923	027566 142761 000207 000002	BICB #207,2(R1)
3924	027574 000453	BR 15\$
3925	027576 005737 034710	13\$: TST RFLAG
3926	027602 001401	BEQ +4
3927	027604 104014	HLT 14
3928	027606 012737 177777 034710	MOV #-1,RFLAG
3929	027614 132761 000001 000002	BITB #BIT0,2(R1)
3930	027622 001401	BEQ +4
3931	027624 104014	HLT 14
3932	027626 022761 034762 000004	CMP #RBUF,4(R1)
3933	027634 001401	BEQ +4

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3934	027636	104014			HLT	14	;REC BA ERROR
3935	027640	023761	034760	000006	CMP	RCOUNT,6(R1)	;COUNT OK?
3936	027646	001401			BEQ	.+4	;BR IF YES
3937	027650	104014			HLT	14	;REC COUNT ERROR
3939	027652	013700	034760		MOV	RCOUNT,R0	;GET SET TO CHECK DATA
3939	027656	012702	034714		MOV	#TBUF,R2	;R2 POINTS TO GOOD DATA
3940	027662	012703	034762		MOV	#RBUF,R3	;R3 POINTS TO RECEIVE DATA
3941	027666	010337	001252		MOV	R3,TEMP3	;SAVE ADDRESS FOR TYPEOUT
3942	027672	112205			MOVB	(R2)+,R5	;R5 = XMIT DATA
3943	027674	112304			MOVB	(R3)+,R4	;R4 = RECEIVE DATA
3944	027676	120504			CMPB	R5,R4	;CHECK DATA
3945	027700	001401			BEQ	.+4	;BR IF OK
3946	027702	104013			HLT	13	;DATA ERROR
3947	027704	005300			DEC	R0	;DEC COUNT
3948	027706	001367			BNE	9\$	;BR IF NOT DONE
3949	027710	005713			TST	(R3)	;THIS SHOULD BE 0, ELSE
3950	027712	001401			BEQ	.+4	;IT RECEIVED TO MUCH!!
3951	027714	104014			HLT	14	;ERROR
3952	027716	142761	000207	000002	BICB	#207,2(R1)	;CLEAR RDO AND BITS 0-2
3953	027724	005737	034710		TST	RFLAG	;REC DONE?
3954	027730	001640			BEQ	16\$	;BR IF NO
3955	027732	005737	034706		TST	TFLAG	;XMIT DONE?
3956	027736	001635			BEQ	16\$	;BR IF NO
3957	027740	104400			SCOPE		;SCOPE THIS TEST

14\$:

***** TEST 51 *****
 ;*OVERUN TEST
 ;*IN FREE RUNNING MODE SEND MESSAGE WITH NO RECEIVE
 ;*BUFFER AVAILABLE, VERIFY THAT AN OVERRUN ERROR OCCURS
 ;*****

; TEST 51

3968	027742	012737	000051	001226
3969	027750	012737	030170	001216
3970				
3971	027756	104412		
3972	027760	032737	100000	001366
3973	027766	001406		
3974	027770	032737	000001	001372
3975	027776	001002		
3976	030000	000137	030152	
3977	030004	032737	010000	001366
3978	030012	001372		
3979	030014	004737	035602	
3980	030020	004737	036002	
3981	030024	004537	036272	
3982	030030	034714		
3983	030032	000044		
3984	030034	012700	000010	
3985	030040	012703	000010	
3986	030044	005037	001416	
3987	030050	105761	000002	
3988	030054	100407		
3989	030056	005237	001416	

TST51:

MOV #51,TSTNO
 MOV #TST52,NEXT

MSTCLR

BIT #BIT15,STAT1
 BEQ .+16
 BIT #BIT0,STAT3
 BNE .+6
 JMP 10\$
 BIT #BIT12,STAT1
 BNE .-12
 JSR PC,WROM
 JSR PC,BASELD
 JSR R5,XFRELD

;R1 CONTAINS BASE DMC11 ADDRESS
 ;MASTER CLEAR DMC11
 ;IS IT A DMC?
 ;BR IF YES
 ;KMC WITH BIT0 SET?
 ;BR IF YES
 ;SKIP TEST
 ;LU PRESENT?
 ;BR IF NO
 ;WRITE MICRO-CODE IN CRAM
 ;LOAD DMC BASE ADDRESS
 ;LOAD XMIT BA/CC
 ;BA
 ;CC
 ;R0 = RETRANSMISSION COUNT
 ;DELAY COUNT
 ;CLEAR DELAY COUNTER
 ;IS RDY 0 SET?
 ;BR IF SET
 ;INC DELAY COUNTER

1\$:

MOV #10,R0
 MOV #10,R3
 CLR TEMP
 TSTB 2(R1)
 BMI .+20
 INC TEMP

3990	030062	001372			BNE	1\$	;BR IF NOT DONE DELAY
3991	030064	005303			DEC	R3	;DEC DELAY COUNT
3992	030066	001370			BNE	1\$	;BR IF DELAY NOT DONE
3993	030070	104014			HLT	14	;ERROR, RDY 0 NOT SET
3994	030072	000427			BR	10\$	;GET OUT
3995	030074	132761	000001	000002	BITB	#BIT0,2(R1)	;IS IT CNTL 0?
3996	030102	001002			BNE	11\$	;BR IF YES
3997	030104	104014			HLT	14	;ERROR, NOT CNTL 0
3998	030106	000421			BR	10\$	;CONTINUE
3999	030110	012705	000004		MOV	#BIT2,R5	;PUT "EXPECTED" IN R5
4000	030114	016104	000006		MOV	6(R1),R4	;PUT "FOUND" IN R4
4001	030120	020504			CMP	R5,R4	;IS ORUN SET?
4002	030122	001404			BEQ	12\$	;BR IF YES
4003	030124	022704	000001		CMP	#1,R4	;DATA CK ERROR?
4004	030130	001411			BEQ	13\$	;BR IF YES
4005	030132	104015			HLT	15	;ERROR, ORUN NOT SET
4006	030134	042761	000207	000002	BIC	#207,2(R1)	;CLEAR RDO
4007	030142	005037	001416		CLR	TEMP	;RESET DELAY
4008	030146	005300			DEC	R0	;DEC RETRANS COUNT
4009	030150	001337			BNE	1\$	;CONTINUE
4010	030152	104400			SCOPE		;SCOPE THIS TEST
4011	030154	042761	000207	000002	BIC	#207,2(R1)	;IGNOR THIS ERROR
4012	030162	005037	001416		CLR	TEMP	;RESET DELAY
4013	030166	000730			BR	1\$	;CONTINUE

***** TEST 52 *****
 ;*LOST DATA TEST
 ;*IN FREE RUNNING MODE SEND A MESSAGE LONGER THAN THE RECEIVE
 ;*BUFFER, VERIFY THAT A LOST DATA ERROR OCCURS.
 ;*****

; TEST 52

4024	030170	012737	000052	001226	TST52:	MOV	#52,TSTNO	
4025	030176	012737	030362	001216		MOV	#TST53,NEXT	
4026								;R1 CONTAINS BASE DMC11 ADDRESS
4027	030204	104412			MSTCLR			;MASTER CLEAR DMC11
4028	030206	032737	100000	001366	BIT	#BIT15,STAT1		;IS IT A DMC?
4029	030214	001406			BEQ	+.16		;BR IF YES
4030	030216	032737	000001	001372	BIT	#BIT0,STAT3		;KMC WITH BIT0 SET?
4031	030224	001002			BNE	+.6		;BR IF YES
4032	030226	000137	030360		JMP	10\$		;SKIP TEST
4033	030232	032737	010000	001366	BIT	#BIT12,STAT1		;LU PRESENT?
4034	030240	001372			BNE	.-12		;BR IF NO
4035	030242	004737	035602		JSR	PC,WROM		;WRITE MICRO-CODE IN CRAM
4036	030246	004737	036002		JSR	PC,BASED		;LOAD DMC BASE ADDRESS
4037	030252	004537	036240		JSR	R5,RFRELD		;LOAD RECEIVE BA/CC
4038	030256	034762			RBUF			;BA
4039	030260	000020			20			;CC
4040	030262	004537	036272		JSR	R5,XFRELD		;LOAD XMIT BA/CC
4041	030266	034714			TBUF			;BA
4042	030270	000044			44			;CC
4043	030272	012703	000010		MOV	#10,R3		;DELAY COUNT
4044	030276	005037	001416		CLR	TEMP		;CLEAR DELAY COUNTER
4045	030302	105761	000002		1\$:	TSTB	2(R1)	;IS RDY 0 SET?

Address	Op Code	Op	Op 2	Op 3	Op 4	Op 5	Op 6	Op 7	Op 8	Op 9	Op 10	Op 11	Op 12	Op 13	Op 14	Op 15	Op 16	Op 17	Op 18	Op 19	Op 20	Op 21	Op 22	Op 23	Op 24	Op 25	Op 26	Op 27	Op 28	Op 29	Op 30	Op 31	Op 32	Op 33	Op 34	Op 35	Op 36	Op 37	Op 38	Op 39	Op 40	Op 41	Op 42	Op 43	Op 44	Op 45	Op 46	Op 47	Op 48	Op 49	Op 50	Op 51	Op 52	Op 53	Op 54	Op 55	Op 56	Op 57	Op 58	Op 59	Op 60	Op 61	Op 62	Op 63	Op 64	Op 65	Op 66	Op 67	Op 68	Op 69	Op 70	Op 71	Op 72	Op 73	Op 74	Op 75	Op 76	Op 77	Op 78	Op 79	Op 80	Op 81	Op 82	Op 83	Op 84	Op 85	Op 86	Op 87	Op 88	Op 89	Op 90	Op 91	Op 92	Op 93	Op 94	Op 95	Op 96	Op 97	Op 98	Op 99	Op 100	Op 101	Op 102	Op 103	Op 104	Op 105	Op 106	Op 107	Op 108	Op 109	Op 110	Op 111	Op 112	Op 113	Op 114	Op 115	Op 116	Op 117	Op 118	Op 119	Op 120	Op 121	Op 122	Op 123	Op 124	Op 125	Op 126	Op 127	Op 128	Op 129	Op 130	Op 131	Op 132	Op 133	Op 134	Op 135	Op 136	Op 137	Op 138	Op 139	Op 140	Op 141	Op 142	Op 143	Op 144	Op 145	Op 146	Op 147	Op 148	Op 149	Op 150	Op 151	Op 152	Op 153	Op 154	Op 155	Op 156	Op 157	Op 158	Op 159	Op 160	Op 161	Op 162	Op 163	Op 164	Op 165	Op 166	Op 167	Op 168	Op 169	Op 170	Op 171	Op 172	Op 173	Op 174	Op 175	Op 176	Op 177	Op 178	Op 179	Op 180	Op 181	Op 182	Op 183	Op 184	Op 185	Op 186	Op 187	Op 188	Op 189	Op 190	Op 191	Op 192	Op 193	Op 194	Op 195	Op 196	Op 197	Op 198	Op 199	Op 200	Op 201	Op 202	Op 203	Op 204	Op 205	Op 206	Op 207	Op 208	Op 209	Op 210	Op 211	Op 212	Op 213	Op 214	Op 215	Op 216	Op 217	Op 218	Op 219	Op 220	Op 221	Op 222	Op 223	Op 224	Op 225	Op 226	Op 227	Op 228	Op 229	Op 230	Op 231	Op 232	Op 233	Op 234	Op 235	Op 236	Op 237	Op 238	Op 239	Op 240	Op 241	Op 242	Op 243	Op 244	Op 245	Op 246	Op 247	Op 248	Op 249	Op 250	Op 251	Op 252	Op 253	Op 254	Op 255	Op 256	Op 257	Op 258	Op 259	Op 260	Op 261	Op 262	Op 263	Op 264	Op 265	Op 266	Op 267	Op 268	Op 269	Op 270	Op 271	Op 272	Op 273	Op 274	Op 275	Op 276	Op 277	Op 278	Op 279	Op 280	Op 281	Op 282	Op 283	Op 284	Op 285	Op 286	Op 287	Op 288	Op 289	Op 290	Op 291	Op 292	Op 293	Op 294	Op 295	Op 296	Op 297	Op 298	Op 299	Op 300	Op 301	Op 302	Op 303	Op 304	Op 305	Op 306	Op 307	Op 308	Op 309	Op 310	Op 311	Op 312	Op 313	Op 314	Op 315	Op 316	Op 317	Op 318	Op 319	Op 320	Op 321	Op 322	Op 323	Op 324	Op 325	Op 326	Op 327	Op 328	Op 329	Op 330	Op 331	Op 332	Op 333	Op 334	Op 335	Op 336	Op 337	Op 338	Op 339	Op 340	Op 341	Op 342	Op 343	Op 344	Op 345	Op 346	Op 347	Op 348	Op 349	Op 350	Op 351	Op 352	Op 353	Op 354	Op 355	Op 356	Op 357	Op 358	Op 359	Op 360	Op 361	Op 362	Op 363	Op 364	Op 365	Op 366	Op 367	Op 368	Op 369	Op 370	Op 371	Op 372	Op 373	Op 374	Op 375	Op 376	Op 377	Op 378	Op 379	Op 380
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```

BMI      +20      ;BR IF SET
INC      TEMP     ;INC DELAY COUNTER
BNE      1$       ;BR IF NOT DONE DELAY
DEC      R3        ;DEC DELAY COUNT
BNE      1$       ;BR IF DELAY NOT DONE
HLT      14       ;ERROR, RDY 0 NOT SET
BR       10$      ;GET OUT
BITB     #BIT0,2(R1) ;IS IT CNTL 0?
BNE      11$      ;BR IF YES
HLT      14       ;ERROR NOT CNTL 0
BR       10$      ;CONTINUE
MOV      #BIT4,R5  ;PUT "EXPECTED" IN R5
MOV      6(R1),R4  ;PUT "FOUND" IN R4
CMP      R5,R4     ;IS LOST DATA SET?
BEQ      10$      ;BR IF YES
HLT      15       ;ERROR, LOST DATA NOT SET
SCOPE
SCOPE THIS TEST

```

```

***** TEST 53 *****
*TRANSMIT NON-EXISTENT MEMORY TEST
*IN FREE RUNNING MODE, LOAD A TRANSMIT BA THAT WILL TIME OUT
*VERIFY THAT A NON-EXISTENT MEMORY ERROR OCCURS
*****

```

: TEST 53

```
TST53:  MOV     #53,TSTNO
         MOV     #TST54,NEXT
```

```

MSTCLR          ;R1 CONTAINS BASE DMC11 ADDRESS
BIT             ;MASTER CLEAR DMC11
BEG             ;IS IT A DMC?
BIT             ;BR IF YES
BNE             ;KMC WITH BIT0 SET?
JMP             ;BR IF YES
JMP             ;SKIP TEST
BIT             ;LU PRESENT?
BNE             ;BR IF NO
JSR             ;WRITE MICRO-CODE IN CRAM
JSR             ;LOAD DMC BASE ADDRESS
JSR             ;LOAD XMIT BA/CC
177320          ;BA
140044          ;CC
MOV             ;DELAY COUNT
CLR             ;CLEAR DELAY COUNTER
TSTB            ;IS RDY 0 SET?
BMI             ;BR IF SET
INC             ;INC DELAY COUNTER
BNE            1$ ;BR IF NOT DONE DELAY
DEC            1$ ;DEC DELAY COUNT
BNE            1$ ;BR IF DELAY NOT DONE
HLT            14 ;ERROR, RDY 0 NOT SET
BR             10$ ;GET OUT
BITB            ;IS IT CNTL 0?
BNE            11$ ;BR IF YES
HLT            14 ;ERROR, NOT CNTL 0

```

15:

E02

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4102	030522	000407			BR	10\$	:CONTINUE
4103	030524	012705	000400	11\$:	MOV	#BIT8,R5	:PUT "EXPECTED" IN R5
4104	030530	016104	000006		MOV	6(R1),R4	:PUT "FOUND" IN R4
4105	030534	020504			CMP	R5,R4	:IS NON-EX-MEM SET?
4106	030536	001401			BEQ	.+4	:BR IF YES
4107	030540	104015			HLT	15	:ERROR NON-EX-MEM NOT SET
4108	030542	104400		10\$:	SCOPE		:SCOPE THIS TEST
4109							
4110							
4111							:***** TEST 54 *****
4112							:*RECEIVE NON-EXISTENT MEMORY TEST
4113							:*IN FREE RUNNING MODE, LOAD A RECEIVE BA THAT WILL TIME OUT
4114							:*VERIFY THAT A NON-EXISTENT MEMORY ERROR OCCURS
4115							:*****
4116							
4117							: TEST 54
4118							
4119	030544	012737	000354	001226	TST54:	MOV	#54,TSTNO
4120	030552	012737	030736	001216		MOV	#TST55,NEXT
4121							:R1 CONTAINS BASE DMC11 ADDRESS
4122	030560	104412			MSTCLR		:MASTER CLEAR DMC11
4123	030562	032737	100000	001366	BIT	#BIT15,STAT1	:IS IT A DMC?
4124	030570	001406			BEQ	.+16	:BR IF YES
4125	030572	032737	000001	001372	BIT	#BIT0,STAT3	:KMC WITH BIT0 SET?
4126	030600	001002			BNE	.+6	:BR IF YES
4127	030602	000137	030734		JMP	10\$	:SKIP TEST
4128	030606	032737	010000	001366	BIT	#BIT12,STAT1	:LU PRESENT?
4129	030614	001372			BNE	.-12	:BR IF NO
4130	030616	004737	035602		JSR	PC,WROM	:WRITE MICRO-CODE IN CRAM
4131	030622	004737	036002		JSR	PC,BASED	:LOAD DMC BASE ADDRESS
4132	030626	004537	036240		JSR	R5,RFELD	:LOAD RECEIVE BA/CC
4133	030632	177320					:BA
4134	030634	140044					:CC
4135	030636	004537	036272		JSR	R5,XFELD	:LOAD XMIT BA/CC
4136	030642	034714			TBUF		:BA
4137	030644	000044			44		:CC
4138	030646	012703	000010		MOV	#10,R3	:DELAY COUNT
4139	030652	005037	001416		CLR	TEMP	:CLEAR DELAY COUNTER
4140	030656	105761	000002	1\$:	TSTB	2(R1)	:IS RDY 0 SET?
4141	030662	100407			BMI	.+20	:BR IF SET
4142	030664	005237	001416		INC	TEMP	:INC DELAY COUNTER
4143	030670	001372			BNE	1\$	:BR IF NOT DONE DELAY
4144	030672	005303			DEC	R3	:DEC DELAY COUNT
4145	030674	001370			BNE	1\$	:BR IF DELAY NOT DONE
4146	030676	104014			HLT	14	:ERROR, RDY 0 NOT SET
4147	030700	000415			BR	10\$	:GET OUT
4148	030702	132761	000001	000002	BITB	#BIT0,2(R1)	:IS IT CNTL 0?
4149	030710	001002			BNE	11\$	:BR IF YES
4150	030712	104014			HLT	14	:ERROR, NOT CNTL 0
4151	030714	000407			BR	10\$	:CONTINUE
4152	030716	012705	000400	11\$:	MOV	#BIT8,R5	:PUT "EXPECTED" IN R5
4153	030722	016104	000006		MOV	6(R1),R4	:PUT "FOUND" IN R4
4154	030726	020504			CMP	R5,R4	:IS NON-EX-MEM SET?
4155	030730	001401			BEQ	.+4	:BR IF YES
4156	030732	104015			HLT	15	:ERROR NON-EX-MEM NOT SET
4157	030734	104400		10\$:	SCOPE		:SCOPE THIS TEST

F02

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4168 030736 012737 000055 001226
4169 030744 012737 031114 001216
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4171 030752 104412
4172 030754 032737 100000 001366
4173 030762 001406
4174 030764 032737 000001 001372
4175 030772 001002
4176 030774 000137 031112
4177 031000 032737 010000 001366
4178 031006 001372
4179 031010 004737 035602
4180 031014 004737 036002
4181 031020 152711 000043
4182 031024 105711
4183 031026 100376
4184 031030 142711 000040
4185 031034 005037 001416
4186 031040 105761 000002
4187 031044 100405
4188 031046 005237 001416
4189 031052 001372
4190 031054 104014
4191 031056 000770
4192 031060 132761 000001 000002
4193 031066 001002
4194 031070 104014
4195 031072 000407
4196 031074 012705 001000
4197 031100 016104 000006
4198 031104 020504
4199 031106 001401
4200 031110 104015
4201 031112 104400
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4212 031114 012737 000056 001226
4213 031122 012737 031272 001216

;***** TEST 55 *****
;PROCESSOR ERROR TEST
;IN FREE RUNNING MODE, DO A BASE TRANSFER REQUEST AFTER A
;BASE HAS BEEN SET UP, VERIFY THAT A PROCESSOR ERROR OCCURS.
;*****
; TEST 55
;-----
TST55: MOV #55,TSTNO
MOV #TST56,NEXT
MSTCLR
BIT #BIT15,STAT1
BEQ .+16
BIT #BIT3,STAT3
BNE .+6
JMP 10$
BIT #BIT12,STAT1
BNE .-12
JSR PC,WROM
JSR PC,BASELD
12$: BISB #43,(R1)
TSTB (R1)
BPL .-2
BICB #40,(R1)
CLR TEMP
13$: TSTB 2(R1)
BMI 14$
INC TEMP
BNE 13$
HLT 14
BR 13$
14$: BITB #BIT0,2(R1)
BNE 11$
HLT 14
BR 10$
11$: MOV #BIT9,R5
MOV 6(R1),R4
CMP R5,R4
BEQ .+4
HLT 15
10$: SCOPE

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS IT A DMC?
;BR IF YES
;KMC WITH BIT0 SET?
;BR IF YES
;SKIP TEST
;LU PRESENT?
;BR IF NO
;WRITE MICRO-CODE IN CRAM
;LOAD BASE ADDRESS
;2ND BASE REQUEST
;RDI SET?
;BR IF NO
;CLEAR RQI
;GET SET TO DELAY
;RDO SET?
;BR IF YES
;INC DELAY
;BR IF NOT DONE DELAY
;ERROR, RDO NOT SET
;TRY AGAIN
;IS IS CNTL 0?
;BR IF YES
;ERROR NOT CNTL 0
;CONTINUE
;PUT "EXPECTED" IN R5
;PUT "FOUND" IN R4
;IS PROC ERROR SET?
;BR IF YES
;ERROR, PROC ERROR NOT SET
;SCOPE THIS TEST

;***** TEST 56 *****
;PROCESSOR ERROR TEST
;IN FREE RUNNING MODE DO A RQI WITH AN ILLEGAL IO CODE
;VERIFY THAT A PROCESSOR ERROR OCCURS
;*****
; TEST 56
;-----
TST56: MOV #56,TSTNO
MOV #TST57,NEXT

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4214					MSTCLR		;R1 CONTAINS BASE DMC11 ADDRESS
4215	031130	104412			BIT	#BIT15,STAT1	;MASTER CLEAR DMC11
4216	031132	032737	100000	001366	BEQ	.+16	;IS IT A DMC?
4217	031140	001406			BIT	#BIT0,STAT3	;BR IF YES
4218	031142	032737	000001	001372	BNE	.+6	;KMC WITH BIT0 SET?
4219	031150	001002			JMP	10\$	;BR IF YES
4220	031152	000137	031270		BIT	#BIT12,STAT1	;SKIP TEST
4221	031156	032737	010000	001366	BNE	.-12	;LU PRESENT?
4222	031164	001372			JSR	PC,WROM	;BR IF NO
4223	031166	004737	035602		JSR	PC,BASELD	;WRITE MICRO-CODE IN CRAM
4224	031172	004737	036002		BISB	#46,(R1)	;LOAD DMC BASE ADDRESS
4225	031176	152711	000046		TSTB	(R1)	;RQI AND ILLEGAL CODE
4226	031202	105711			BPL	.-2	;WAIT FOR RDI
4227	031204	100376			BICB	#40,(R1)	;BR IF NO RDI
4228	031206	142711	000040		CLR	TEMP	;CLEAR RQI
4229	031212	005037	001416		1\$:	TSTB	;CLEAR COUNTER
4230	031216	105761	000002		BMI	.+14	;RDY 0 SET?
4231	031222	100405			INC	TEMP	;BR IF YES
4232	031224	005237	001416		BNE	1\$	;BUMP COUNTER DELAY
4233	031230	001372			HLT	14	;BR IF NOT DONE
4234	031232	104014			BR	1\$	;ERROR NO RDY 0
4235	031234	000770			BITB	#BIT0,2(R1)	;TRY AGAIN
4236	031236	132761	000001	000002	BNE	11\$	;IS IT CNTL 0
4237	031244	001002			HLT	14	;BR IF YES
4238	031246	104014			BR	10\$	;ERROR, NOT CNTL 0
4239	031250	000407			11\$:	MOV	;CONTINUE
4240	031252	012705	001000		MOV	#BIT9,R5	;PUT "EXPECTED" IN R5
4241	031256	016104	000006		CMP	6(R1),R4	;PUT "FOUND" IN R4
4242	031262	020504			BEQ	.+4	;IS PROC ERROR SET?
4243	031264	001401			HLT	15	;BR IF YES
4244	031266	104015			10\$:	SCOPE	;ERROR PROC ERROR NOT SET
4245	031270	104400					;SCOPE THIS TEST

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***** TEST 57 *****
 ;HALF DUPLEX TEST
 ;IN FREE RUNNING MODE, SET HALF DUPLEX AND L U LOOP
 ;SEND A MESSAGE AND VERIFY THAT THERE ARE NO DONES
 ;*****

: TEST 57

TST57: MOV #57,TSTNO
 MOV #TST60,NEXT

4256	031272	012737	000057	001226			
4257	031300	012737	031432	001216			
4258							
4259	031306	104412			MSTCLR		;R1 CONTAINS BASE DMC11 ADDRESS
4260	031310	032737	100000	001366	BIT	#BIT15,STAT1	;MASTER CLEAR DMC11
4261	031316	001406			BEQ	.+16	;IS IT A DMC?
4262	031320	032737	000001	001372	BIT	#BIT0,STAT3	;BR IF YES
4263	031326	001002			BNE	.+6	;KMC WITH BIT0 SET?
4264	031330	000137	031424		JMP	10\$	;BR IF YES
4265	031334	032737	010000	001366	BIT	#BIT12,STAT1	;SKIP TEST
4266	031342	001372			BNE	.-12	;LU PRESENT?
4267	031344	004737	035602		JSR	PC,WROM	;BR IF NO
4268	031350	004737	036120		JSR	PC,BASELH	;WRITE MICRO-CODE
4269	031354	004537	036240		JSR	R5,RFELD	;LOAD BASE AND HALF DUPLEX
							;LOAD RECEIVE BUFFER

4270	031360	034762		
4271	031362	000044		
4272	031364	004537	036272	
4273	031370	034714		
4274	031372	000044		
4275	031374	012703	000003	
4276	031400	005037	001416	
4277	031404	105761	000002	
4278	031410	100406		
4279	031412	005237	001416	
4280	031416	001372		
4281	031420	005303		
4282	031422	001370		
4283	031424	104400		
4284	031426	104014		
4285	031430	000775		
4286				
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4298				
4299	031432	012737	000060	001226
4300	031440	012737	003274	001216
4301				
4302	031446	104412		
4303	031450	032737	100000	001366
4304	031456	001406		
4305	031460	032737	000001	001372
4306	031466	001000		
4307	031470	000137	032434	
4308	031474	032737	010000	001366
4309	031502	001372		
4310	031504	004737	035602	
4311	031510	012737	000340	177776
4312	031516	013700	001366	
4313	031522	006200		
4314	031524	006200		
4315	031526	006200		
4316	031530	006200		
4317	031532	042700	177437	
4318	031536	012777	032534	147630
4319	031544	010077	147626	
4320	031550	012777	033040	147622
4321	031556	010077	147620	
4322				
4323				
4324				
4325	031562	012737	000104	034706

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RBUF                                ;BA
44                                  ;CC
JSR      RS,XFREL0                 ;LOAD TRANSMIT BUFFER
TBUF                                ;BA
44                                  ;CC
MOV      #3,R3                     ;LOAD DELAY COUNT
CLR      TEMP                      ;CLEAR DELAY
4$:      TSTB      2(R1)            ;IS DONE SET?
        BMI       5$               ;BR IF YES (ERROR)
        INC       TEMP             ;INC DELAY
        BNE       4$               ;BR IF DELAY NOT DONE
        DEC       R3               ;DEC DELAY COUNT
        BNE       4$               ;BR IF DELAY NOT DONE
10$:     SCOPE                     ;SCOPE THIS TEST
5$:      HLT      14                ;ERROR DONE WITH HALF-DUPLEX
        BR        10$              ;GET OUT

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;***** TEST 60 *****
;*FREE RUNNING DATA TEST (INTERRUPT DRIVEN EXERCISER)
;*THIS TEST REPEATEDLY QUEUES UP 7 RECEIVE BUFFERS AND
;*7 TRANSMIT BUFFERS AND CHECKS DATA WHEN ALL 7 BUFFERS
;*ARE RECEIVED. TRANSMIT COUNTS RANGE FROM 1 TO 104, ALSO
;*ODD AND EVEN TRANSMIT AND RECEIVE BA'S ARE USED. DATA
;*IS A BINARY COUNT PATTERN. THE RESUME FUNCTION IS CHECKED IN THIS TEST
;*****

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: TEST 60
-----
TST60:  MOV      #60,TSTNO
        MOV      #.EOP,NEXT

        MSTCLR
        BIT      #BIT15,STAT1
        BEQ      .+16
        BIT      #BIT0,STAT3
        BNE      .+6
        JMP      ENDEX1
        BIT      #BIT12,STAT1
        BNE      .-12
        JSR      PC,WROM
        MOV      #340,PS
        MOV      STAT1,RO
        ASR      RO
        ASR      RO
        ASR      RO
        ASR      RO
        BIC      #177437,RO
        MOV      #IISR,@DMRVEC
        MOV      RO,@DMRLVL
        MOV      #OISR,@DMTVEC
        MOV      RO,@DMTLVL

;R1 CONTAINS BASE DMC11 ADDRESS
;MASTER CLEAR DMC11
;IS IT A DMC?
;BR IF YES
;KMC WITH BIT0 SET?
;BR IF YES
;SKIP TEST
;LU PRESENT?
;BR IF NO
;WRITE MICR-CODE
;LOCK OUT INTERRUPTS
;GET BR LEVEL
;SHIFT RIGHT 4 TIMES

;PUT BR LEVEL IN RO
;LOAD INPUT VECTOR
;LOAD LEVEL
;LOAD OUTPUT VECTOR
;LOAD LEVEL

;INITIALIZE ALL BUFFER LISTS AND COUNT LISTS

MOV      #104,TFLAG      ;TFLAG CONTAINS COUNT

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4326	031570	012700	033454		MOV	#XMITBA+2,R0	;R0 POINTS TO BA LIST
4327	031574	012703	033746		MOV	#RBUF,R3	;R3 CONTAINS BUFFER ADDRESS
4328	031600	010320		1\$:	MOV	R3,(R0)+	;LOAD BA LIST WITH REC BA
4329	031602	062703	000104		ADD	#104,R3	;UPDATE BUFFER ADDRESS
4330	031606	022700	033472		CMP	#XMITBA+20,R0	;END OF REC BUFFERS?
4331	031612	001372			BNE	1\$	;NO LOAD NEXT ONE
4332	031614	012720	033510	2\$:	MOV	#TBUF,(R0)+	;LOAD BA LIST WITH XMIT BA
4333	031620	022700	033510		CMP	#XMITBA+36,R0	;END OF XMIT BUFFERS?
4334	031624	001373			BNE	2\$	;NO LOAD NEXT BUFFER
4335	031626	012700	033622		MOV	#RCNTAB+2,R0	;R0 POINTS TO COUNT LIST
4336	031632	013720	034706	3\$:	MOV	TFLAG,(R0)+	;LOAD COUNT OF 104
4337	031636	022700	033640		CMP	#RCNTAB+20,R0	;END OF REC COUNT LIST?
4338	031642	001373			BNE	3\$	;BR IF NO
4339	031644	012737	000006	034704	MOV	#6,FLAG ;LOOP COUNT	
4340	031652	012711	040000		MOV	#BIT14,(R1)	;SET MASTER CLEAR
4341	031656	032737	100000	CO:366	BIT	#BIT15,STAT1	;IOP?
4342	031664	001402			BEQ	.+6	;BR IF NO
4343	031666	012711	100000		MOV	#BIT15,(R1)	;SET RUN ON IOP
4344	031672	012700	177777		MOV	#-1,R0	;R0 IS INPUT DONE COUNTER
4345	031676	005037	033450	CLRTAB:	CLR	RESUME	;CLEAR RESUME FLAG
4346	031702	012705	033656		MOV	#RDNTAB,R5	;GET READY TO CLEAR ALL RECEIVE
4347	031706	005025		2\$:	CLR	(R5)+	;BUFFERS
4348	031710	022705	034702		CMP	#RBUFE,R5	;END OF BUFFER?
4349	031714	001374			BNE	2\$	;BR IF NO
4350	031716	005737	034704		TST	FLAG	;VARIABLE COUNTS?
4351	031722	100407			BMI	5\$	;BR IF YES(DON'T CHANGE THEM)
4352	031724	012704	033640		MOV	#XCNTAB,R4	;R4 POINTS TO XMIT COUNT LIST
4353	031730	013724	034706	4\$:	MOV	TFLAG,(R4)+	;LOAD XMIT CHAR COUNT
4354	031734	022704	033656		CMP	#XCNTAB+16,R4	;DONE?
4355	031740	001373			BNE	4\$	;BR IF NO
4356	031742	005002		5\$:	CLR	R2	;R2 IS OUTPUT DONE COUNTER
4357	031744	005004			CLR	R4	;R4 IS USED AS INDEX IN OISR
4358	031746	005711			TST	(R1)	;IS RUN SET?
4359	031750	100376			BPL	.-2	;WAIT FOR RUN
4360	031752	152761	000100	000002	BISB	#BIT6,2(R1)	;SET IEO
4361	031760	022737	000006	034704	CMP	#6,FLAG ;FIRST TIME?	
4362	031766	001003			BNE	1\$	;BR IF NOT
4363	031770	052711	004143		BIS	#4143,(R1)	;SET LU LOOP, IEI,RQI,BASE I
4364	031774	000402			BR	3\$	;CONTINUE
4365	031776	052711	004144	1\$:	BIS	#4144,(R1)	;SET LU LOOP, IEI, RQI, REC BA'CC
4366	032002	005037	001416	3\$:	CLR	TEMP	;SET UP FOR DELAY COUNT
4367	032006	012737	000022	001250	MOV	#22,TEMP2	;GET SET FOR DELAY
4368	032014	005037	177776		CLR	PS	;ALLOW INTERRUPTS
4369	032020	022737	000001	034704	SCAN:	CMP	#1,FLAG
4370	032026	001002			BNE	1\$	;1 BYTE MESS?
4371	032030	000137	032472		JMP	ENDEX3	;BR IF NO
4372	032034	022700	000020	1\$:	CMP	#20,R0	;BR IF YES
4373	032040	001402			BEQ	SCAN2	;INPUT DONE?
4374	032042	000137	032504		JMP	SCAN1	;BR IF YES
4375	032046	022702	000034	SCAN2:	CMP	#34,R2	;BR IF NO
4376	032052	001402			BEQ	8\$	;XMIT DONE FOR ALL MESSAGES?
4377	032054	000137	032504		JMP	SCAN1	;BR IF YES
4378	032060	022704	000034	8\$:	CMP	#34,R4	;BR IF NO
4379	032064	001402			BEQ	9\$	;REC DONE FOR ALL MESSAGES?
4380	032066	000137	032504		JMP	SCAN1	;BR IF YES
4381	032072			9\$:			;BR IF NO

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4382	032072	012700	033656		MOV	#RDNTAB,R0	:GET FIRST REC BUFFER
4383	032076	012002		5\$:	MOV	(R0)+,R2	:R2 POINTS TO BUFFER
4384	032100	005005			CLR	R5	:R5=EXPECTED
4385	032102	005003			CLR	R3	:R3 = COUNT
4386	032104	005737	034704		TST	FLAG	:CHECK FOR ODD XMIT BA'S
4387	032110	100012			BPL	6\$	:ONLY FOR VARIABLE COUNTS
4388	032112	022710	000027		CMP	#27,(R0)	:IF 27 BUMP DATA BY 1 (ODD XMIT BA)
4389	032116	001406			BEQ	7\$	:BR IF YES
4390	032120	022710	000042		CMP	#42,(R0)	:IF 42 THEN ODD XMIT BA ALSO
4391	032124	001403			BEQ	7\$	:BR IF YES
4392	032126	022710	000103		CMP	#103,(R0)	:IF 103 THEN ODD XMIT BA ALSO
4393	032132	001001			BNE	6\$	:SKIP IF NOT
4394	032134	005205		7\$:	INC	R5	:START DATA AT 1 FOR ODD XMIT BA'S
4395	032136	010237	001252	6\$:	MOV	R2,TEMP3	:SAVE ADDRESS FOR TYPECUT
4396	032142	112204			MOVB	(R2)+,R4	:GET RECEIVE DATA
4397	032144	120504			CMPB	R5,R4	:IS 1. CORRECT?
4398	032146	001401			BEQ	.+4	:BR IF YES
4399	032150	104013			HLT	13	:DATA ERROR
4400	032152	005205			INC	R5	:NEXT CHARACTER
4401	032154	005203			INC	R3	:INC COUNT
4402	032156	021003			CMP	(R0),R3	:DONE YET?
4403	032160	001366			BNE	6\$	:BR IF NO
4404	032162	062700	000002		ADD	#2,R0	:GET NEXT REC BUFFER
4405	032166	022700	033712		CMP	#RDNTAB+34,R0	:DONE YET?
4406	032172	001341			BNE	5\$	:BR IF NO
4407	032174	012700	000001		MOV	#1,R0	:SET R0 TO 1
4408	032200	005737	034704		TST	FLAG	:VARIABLE COUNTS?
4409	032204	100004			BPL	4\$	:BR IF NO
4410	032206	005237	034704		INC	FLAG	:FLAG IS NEGATIVE
4411	032212	001231			BNE	CLRTAB	:BR IF NOT DONE
4412	032214	000447			BR	ENDEX	:ALL DONE
4413	032216	032737	000001	034704	4\$:	BIT	#BIT0,FLAG
4414	032224	001003			BNE	1\$	:CHANGE CHAR COUNT FOR NEXT LOOP
4415	032226	005337	034706		DEC	TFLAG	:BR TO SUB 40
4416	032232	000403			BR	2\$	:DEC BY ONE
4417	032234	162737	000040	034706	1\$:	SUB	#40,TFLAG
4418	032242	005337	034704		2\$:	DEC	FLAG
4419	032246	001213			BNE	CLRTAB	:GO DO IT AGAIN
4420	032250	005004			CLR	R4	:R4 CONTAINS OFFSET
4421	032252	012702	033642		MOV	#XCNTAB+2,R2	:R2 POINTS TO XMIT COUNT LIST
4422	032256	062704	000013		3\$:	ADD	#13,R4
4423	032262	060422			ADD	R4,(R2)+	:INCREASE R4 BY 13
4424	032264	022702	033656		CMP	#XCNTAB+16,R2	:MAKE COUNTS VARIABLE
4425	032270	001372			BNE	3\$	:DONE ALL 7?
4426	032272	012702	033464		MOV	#RECBA+12,R2	:BR IF NO
4427	032276	005222			INC	(R2)+	:R2 POINTS TO REC BA LIST
4428	032300	005222			INC	(R2)+	:MAKE THIS REC BA ODD
4429	032302	005222			INC	(R2)+	:MAKE THIS REC BA ODD
4430	032304	062702	000004		ADD	#4,R2	:MAKE THIS REC BA ODD
4431	032310	005222			INC	(R2)+	:SKIP TO XMIT BA LIST
4432	032312	005222			INC	(R2)+	:MAKE THIS XMIT BA ODD
4433	032314	062702	000004		ADD	#4,R2	:MAKE THIS XMIT BA ODD
4434	032320	005222			INC	(R2)+	:SKIP TO NEXT ODD BA
4435	032322	012737	177772	034704	MOV	#-6,FLAG	:MAKE FLAG NEGATIVE
4436	032330	000137	031676		JMP	CLRTAB	:LOOP WITH VARIABLE COUNTS
4437	032334	152711	000146		ENDEX:	BISB	#146,(R1)

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4438	032340	005737	034704	1\$:	TST	FLAG	;HAS INTERRUPT OCCURED?
4439	032344	001775			BEQ	1\$	;BR IF NO
4440	032346	012700	000003		MOV	#3,RO	;BASE ADDRESS OFFSET
4441	032352	105760	035030	2\$:	TSTB	BASE(RO)	;CHECK ERROR COUNT
4442	032356	001027			BNE	ENDEX2	;BR IF ERROR
4443	032360	005200			INC	RO	;BUMB INDEX
4444	032362	022700	000005		CMP	#5,RO	;5 = NAKS BAD CRC
4445	032366	001006			BNE	3\$	;BR IF NOT 5
4446	032370	122760	000013 035030		CMPB	#13,BASE(RO)	;SHOULD BE 13 ERRORS
4447	032376	001017			BNE	ENDEX2	;BECAUSE OF RESUME
4448	032400	005200			INC	RO	;BUMP INDEX
4449	032402	000763			BR	2\$	;BR
4450	032404	022700	000011	3\$:	CMP	#11,RO	;DONE ALL ERROR COUNTERS YET?
4451	032410	001360			BNE	2\$	;BR IF NO
4452	032412	122760	000013 035030		CMPB	#13,BASE(RO)	;13 ERRORS BECAUSE OF RESUME
4453	032420	001006			BNE	ENDEX2	;BR IF NOT OK
4454	032422	005200			INC	RO	;NEXT BASE TABLE LOCATION
4455	032424	122760	000013 035030		CMPB	#13,BASE(RO)	;13 ERRORS BECAUSE OF RESUME
4456	032432	001001			BNE	ENDEX2	;BR IF NOT OK
4457	032434	104400		ENDEX1:	SCOPE		;SCOPE THIS TEST
4458	032436	113737	035033 001250	ENDEX2:	MOVB	BASE+3,TEMP2	;SAVE ALL ODD ADDRESSES
4459	032444	113737	035035 001252		MOVB	BASE+5,TEMP3	;FOR TYPEOUT
4460	032452	113737	035037 001254		MOVB	BASE+7,TEMP4	
4461	032460	113737	035041 001256		MOVB	BASE+11,TEMP5	
4462	032466	104017			HLT	17	;NON ZERO ERROR COUNT
4463	032470	000761			BR	ENDEX1	;GET OUT
4464	032472	022700	000017	ENDEX3:	CMP	#17,RO	;ALL DONE INPUT?
4465	032476	001002			BNE	SCAN1	;BR IF NO
4466	032500	000137	032046		JMP	SCAN2	;BR IF YES
4467	032504	005337	001416	SCAN1:	DEC	TEMP	;DECREMENT DELAY COUNTER
4468	032510	001402			BEQ	1\$	;BR IF ZERO
4469	032512	000137	032020		JMP	SCAN	;BR IF NOT DONE DELAY
4470	032516	005337	001250	1\$:	DEC	TEMP2	;DEC DELAY COUNT
4471	032522	001402			BEQ	2\$	;BR IF DONE DELAY
4472	032524	000137	032020		JMP	SCAN	;BR IF NOT DONE
4473	032530	104014		2\$:	HLT	14	;ERROR HUNG
4474	032532	000740			BR	ENDEX1	;GET OUT
4475							
4476							
4477							
4478	032534	022700	000017	IISR:	CMP	#17,RO	;PROC. ERROR DONE?
4479	032540	001421			BEQ	12\$	;BR IF YES
4480	032542	005737	033450		TST	RESUME	;IS THIS A RESUME INTERRUPT
4481	032546	001432			BEQ	8\$	;BR IF NO
4482	032550	032711	000002		BIT	#BIT1,(R1)	;CNTL OR BASE?
4483	032554	001407			BEQ	13\$	;BR IF CNTL I
4484	032556	012761	035030 000004		MOV	#BASE,4(R1)	;LOAD BASE ADDRESS
4485	032564	012761	010000 000006		MOV	#BIT12,6(R1)	;WITH RESUME BIT SET
4486	032572	000404			BR	12\$	;CONTINUE
4487	032574	005061	000006	13\$:	CLR	6(R1)	;SELECT FULL DUPLEX
4488	032600	005037	033450		CLR	RESUME	;CLEAR RESUME FLAG
4489	032604	142711	000040	12\$:	BICB	#40,(R1)	;CLEAR RQI
4490	032610	105711			TSTB	(R1)	;IS RDI GONE?
4491	032612	100776			BMI	-2	;BR IF NO
4492	032614	005737	033450		TST	RESUME	;BASE OR CNTL I?
4493	032620	001403			BEQ	14\$	;BR IF IT WAS CNTL I

;INPUT INTERRUPT SERVICE ROUTINE

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4494	032622	152711	000041		BISB	#41,(R1)	:ASK FOR CNTL I
4495	032626	000002			RTI		:RETURN
4496	032630	105011		14\$:	CLRB	(R1)	:CLEAR BSEL 0
4497	032632	000002			RTI		:RETURN
4499	032634	005700		8\$:	TST	RO	:FIRST TIME HERE?
4499	032636	100006			BPL	7\$	:LOAD BASE IF MINUS
4500	032640	012761	035030	000004	MOV	#BASE,4(R1)	:SET UP BASE ADDRESS
4501	032646	005061	000006		CLR	6(R1)	:CLEAR COUNT
4502	032652	000434			BR	3\$	:CONTINUE
4503	032654	001003		7\$:	BNE	1\$	:CNTL I FULL DUPLEX IF 0
4504	032656	005061	000006		CLR	6(R1)	:SELECT FULL DUPLEX
4505	032662	000430			BR	3\$	:CONTINUE
4506	032664	032700	000010	1\$:	BIT	#BIT3,RO	:XMIT?
4507	032670	001013			BNE	2\$	:BR IF YES
4508	032672	000241			CLC		:CLEAR CARRY
4509	032674	006100			ROL	RO	:MAKE RO EVEN
4510	032676	016061	033452	000004	MOV	RECBA(RO),4(R1)	:LOAD REC BUFFER
4511	032704	016061	033620	000006	MOV	RCNTAB(RO),6(R1)	:LOAD COUNT
4512	032712	000241			CLC		:CLEAR CARRY
4513	032714	006000			ROR	RO	:GET RO BACK
4514	032716	000412			BR	3\$	:CONTINUE
4515	032720	000241		2\$:	CLC		:CLEAR CARRY
4516	032722	006100			ROL	RO	:MAKE IT EVEN
4517	032724	016061	033452	000004	MOV	XMITBA(RO),4(R1)	:LOAD XMIT BUFFER
4518	032732	016061	033620	000006	MOV	RCNTAB(RO),6(R1)	:LOAD COUNT
4519	032740	000241			CLC		:CLEAR CARRY
4520	032742	006000			ROR	RO	:PUT IT BACK
4521	032744	142711	000040	3\$:	BICB	#40,(R1)	:CLEAR RQI
4522	032750	105711			TSTB	(R1)	:WAIT FOR
4523	032752	100776			BMI	-2	:RDI TO GO AWAY
4524	032754	005200			INC	RO	:INC COUNT
4525	032756	001003			BNE	6\$	:IF 0 ASK FOR CNTL I
4526	032760	152711	000041		BISB	#41,(R1)	:ASK FOR CNTL I
4527	032764	000002			RTI		:RETURN
4528	032766	022700	000017	6\$:	CMP	#17,RO	:DONE YET?
4529	032772	001411			BEQ	4\$	:BR IF YES
4530	032774	032700	000010		BIT	#BIT3,RO	:XMIT?
4531	033000	001003			BNE	5\$	:BR IF YES
4532	033002	152711	000044		BISB	#44,(R1)	:ASK FOR REC BA/CC
4533	033006	000002			RTI		:RETURN
4534	033010	152711	000040	5\$:	BISB	#40,(R1)	:ASK FOR XMIT BA/CC
4535	033014	000002			RTI		:RETURN
4536	033016	022737	000001	034704	4\$:	CMP	#1 FLAG
4537	033024	001403			BEQ	15\$	:1 BYTE MESS?
4538	033026	152711	000046		BISB	#46,(R1)	:FORCE PROC. ERROR
4539	033032	000002			RTI		:RETURN
4540	033034	105011		15\$:	CLRB	(R1)	:CLR SEL0
4541	033036	000002			RTI		:RETURN
4542							
4543							
4544							
4545	033040	032761	000001	000002	0ISR:	BIT	#BIT0,2(R1)
4546	033046	001461			BEQ	1\$	:IS THIS AN ERROR?
4547	033050	005737	034704		TST	FLAG	:BR IF NO
4548	033054	001006			BNE	9\$	:IS THIS SHUT DOWN INTERRUPT?
4549	033056	005237	034704		INC	FLAG	:BR IF NO
							:YES MAKE FLAG NON-ZERO

;OUTPUT INTERRUPT SERVICE ROUTINE

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4550	033062	022761	001000	000006		CMP	#BIT9,6(R1)	;SHUT DOWN BIT SET?
4551	033070	001516				BEQ	10\$	;YES ALL IS OK
4552	033072	022700	000017		9\$:	CMP	#17,R0	;RESUME INTERRUPT?
4553	033076	001033				BNE	11\$	;BR IF NO
4554	033100	022761	001000	000006		CMP	#BIT9,6(R1)	;PROC. ERROR BIT SET?
4555	033106	001027				BNE	11\$	;BR IF NO
4556	033110	005200				INC	R0	;BUMP COUNTER (TO 20)
4557	033112	012711	040000			MOV	#BIT14,(R1)	;MASTER CLEAR DEVICE
4558	033116	032737	100000	001366		BIT	#BIT15,STAT1	;DMC OR KMC?
4559	033124	001405				BEQ	.+14	;BR IF DMC
4560	033126	012711	100000			MOV	#BIT15,(R1)	;SET RUN ON KMC
4561	033132	105227	000000			INCB	#0	;DELAY ON KMC
4562	033136	001375				BNE	.-4	
4563	033140	012737	177777	033450		MOV	#-1,RESUME	;SET RESUME FLAG
4564	033146	005711				TST	(R1)	;RUN SET?
4565	033150	100376				BPL	.-2	;BR IF NO
4566	033152	012761	000100	000002		MOV	#BIT6,2(R1)	;SET IEO
4567	033160	052711	004143			BIS	#4143,(R1)	;ASK FOR PORT(BASE REQ)
4568	033164	000002				RTI		;RETURN
4569	033166	016137	000004	001252	11\$:	MOV	4(R1),TEMP3	;SAVE FOR ERROR TYPEOUT
4570	033174	016137	000006	001254		MOV	6(R1),TEMP4	;SAVE FOR ERROR TYPEOUT
4571	033202	104016				HLT	16	;CNTL 0 ERROR
4572	033204	022626				CMP	(SP)+,(SP)+	;ADJUST STACK
4573	033206	000137	032434			JMP	ENDEX1	;GET OUT
4574	033212	032761	000004	000002	1\$:	BIT	#BIT2,2(R1)	;RECEIVE?
4575	033220	001046				BNE	2\$	;BR IF YES
4576	033222	022761	033511	000004		CMP	#TBUF+1,4(R1)	;XMIT BA CORRECT?
4577	033230	001405				BEQ	4\$	;BR IF OK
4578	033232	022761	033510	000004		CMP	#TBUF,4(R1)	;XMIT BA CORRECT?
4579	033240	001401				BEQ	4\$	;BR IF YES
4580	033242	104014				HLT	14	;XMIT BA ERROR
4581	033244	005005			4\$:	CLR	R5	;R5 IS INDEX REG
4582	033246	026561	033640	000006	5\$:	CMP	XCNTAB(R5),6(R1)	;IS CHAR COUNT OK?
4583	033254	001406				BEQ	6\$	;BR IF YES
4584	033256	062705	000002			ADD	#2,R5	;INC INDEX
4585	033262	022705	000016			CMP	#16,R5	;DONE LIST YET?
4586	033266	001367				BNE	5\$	;BR IF NO
4587	033270	104014				HLT	14	;XMIT COUNT ERROR
4588	033272	016162	000004	033712	6\$:	MOV	4(R1),XDNTAB(R2)	;STORE XMIT DONE BA
4589	033300	062702	000002			ADD	#2,R2	;INC INDEX
4590	033304	016162	000006	033712		MOV	6(R1),XDNTAB(R2)	;STORE XMIT DONE CC
4591	033312	062702	000002			ADD	#2,R2	;INC INDEX
4592	033316	142761	000207	000002		BICB	#207,2(R1)	;CLEAR RDO
4593	033324	000002				RTI		;RETURN
4594	033326	105011			10\$:	CLRB	(R1)	;CLEAR SEL0
4595	033330	105061	000002			CLRB	2(R1)	;CLEAR SEL2
4596	033334	000002				RTI		;RETURN
4597	033336	012705	000002		2\$:	MOV	#2,R5	;SET UP R5 AS INDEX
4598	033342	026561	033452	000004		CMP	RECBA(R5),4(R1)	;COMPARE WITH LIST OF CORRECT BA'S
4599	033350	001406				BEQ	3\$	;BR IF OK?
4600	033352	062705	000002			ADD	#2,R5	;INCREMENT R5
4601	033356	022705	000020			CMP	#20,R5	;END OF LIST?
4602	033362	001367				BNE	2\$+4	;BR IF NO
4603	033364	104014				HLT	14	;REC BA ERROR
4604	033366	005005			3\$:	CLR	R5	;R5 IS INDEX
4605	033370	026561	033640	000006	7\$:	CMP	XCNTAB(R5),6(R1)	;CHECK FOR CORRECT REC COUNT

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4606	033376	001406			BEG	8\$	;BR IF YES
4607	033400	062705	000002		ADD	#2,R5	;INCREMENT R5
4608	033404	022705	000016		CMP	#16,R5	;END OF LIST?
4609	033410	001367			BNE	7\$	;BR IF NOT
4610	033412	104014			HLL	14	;REC COUNT ERROR
4611	033414	016164	000004	033656	MOV	4(R1),RDNTAB(R4)	;STORE REC BA
4612	033422	062704	000002		ADD	#2,R4	;INC INDEX
4613	033426	016164	000006	033656	MOV	6(R1),RDNTAB(R4)	;STORE REC DONE CC
4614	033434	062704	000002		ADD	#2,R4	;INC INDEX
4615	033440	142761	000207	000002	BICB	#207,2(R1)	;CLEAR RDO
4616	033446	000002			RTI		;RETURN
4617							
4618							
4619							
4620							
4621	033450	000000			RESUME:	0	
4622	033452				RECB:		
4623	033452	000017			XMITBA:	.BLKW 17	;REC & XMIT BA LIST
4624							
4625	033510				TBUFF:		;TRANSMIT DATA
4626	033510	000	001	002	.BYTE	0,1,2,3,4,5,6,7	
4627	033513	003	004	005			
4628	033516	006	007				
4629	033520	010	011	012	.BYTE	10,11,12,13,14,15,16,17	
4630	033523	013	014	015			
4631	033526	016	017				
4632	033530	020	021	022	.BYTE	20,21,22,23,24,25,26,27	
4633	033533	023	024	025			
4634	033536	026	027				
4635	033540	030	031	032	.BYTE	30,31,32,33,34,35,36,37	
4636	033543	033	034	035			
4637	033546	036	037				
4638	033550	040	041	042	.BYTE	40,41,42,43,44,45,46,47	
4639	033553	043	044	045			
4640	033556	046	047				
4641	033560	050	051	052	.BYTE	50,51,52,53,54,55,56,57	
4642	033563	053	054	055			
4643	033566	056	057				
4644	033570	060	061	062	.BYTE	60,61,62,63,64,65,66,67	
4645	033573	063	064	065			
4646	033576	066	067				
4647	033600	070	071	072	.BYTE	70,71,72,73,74,75,76,77	
4648	033603	073	074	075			
4649	033606	076	077				
4650	033610	100	101	102	.BYTE	100,101,102,103,104,105,106,107	
4651	033613	103	104	105			
4652	033616	106	107				
4653							
4654	033620	000010			RCNTAB:	.BLKW 10	;RECEIVE COUNT TABLE
4655	033640	000007			XCNTAB:	.BLKW 7	;TRANSMIT COUNT TABLE
4656							
4657	033656	000016			RDNTAB:	.BLKW 16	;RECEIVE DONE TABLE (BA/CC)
4658	033712	000016			XDNTAB:	.BLKW 16	;XMIT DONE TABLE (BA/CC)
4659							
4660	033746				RBUFF:		;RECEIVER BUFFERS
4661	033746	000104			RBUFF1:	.BLKB 104	

4662	034052	000104			RBUFF2:	.BLKB	104	
4663	034156	000104			RBUFF3:	.BLKB	104	
4664	034262	000104			RBUFF4:	.BLKB	104	
4665	034366	000104			RBUFF5:	.BLKB	104	
4666	034472	000104			RBUFF6:	.BLKB	104	
4667	034576	000104			RBUFF7:	.BLKB	104	
4668	034702	000000			RBUFE:	0		;END OF RECEIVER BUFFERS
4669			06900					
4670			07000					
4671			07100					
4672			07200					
4673			07300					
4674			07400					
4675	034704	000000	07500		FLAG:	0		
4676	034706	000000	07600		TFLAG:	0		
4677	034710	000000	07700		RFLAG:	0		
4678	034712	000044	07800		TCOUNT:	44		
4679	034714	041101	07900		TBUF:	.ASCII/ABCDEFGHIJKLMNOPQRSTUVWXYZ0123456789/		
4680	034722	044107		042103				
4681	034730	047115		043105				
4682	034736	052123		045111				
4683	034744	055131		050117				
4684	034752	032464		053125				
4685				054127				
4686	034760	000044		030460				
4687	034762	035030		033466				
4688			08000					
4689	035030	035430	08100		.EVEN			
4690			08200		RCOUNT:	44		
4691			08300		RBUF:	.=.+46		
4692			08400		.EVEN			
4693			00300		BASE:	.=.+256.		
4694			00400					
4695	035430		00500					
4696			00600					
4697			00700					
4698	035430	104414	00800					
4699	035432	000400	00900					
4700	035434	104414	01000					
4701	035436	063220						
4702	035440	104414						
4703	035442	060400						
4704	035444	000207						
4705								
4706								
4707	035446							
4708								
4709								
4710	035446	104414						
4711	035450	000401						
4712	035452	000207						
4713								
4714								
4715	035454							
4716								
4717								


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;BUFFER AREA
;-----
FLAG: 0
TFLAG: 0
RFLAG: 0
TCOUNT: 44
TBUF: .ASCII/ABCDEFGHIJKLMNOPQRSTUVWXYZ0123456789/

.EVEN
RCOUNT: 44
RBUF: .=.+46
.EVEN
BASE: .=.+256.

;SUBROUTINES
;-----
CLRALL:
;THIS SUBROUTINE CLEARS THE C&Z BITS AND THE BR
ROMCLK
000400 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR+0
ROMCLK
063220 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;SP(0)+BR
ROMCLK
060400 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR+SP(0)+BR
RTS PC

SETBRO:
;THIS SUBROUTINE SETS BRO BIT
ROMCLK
000401 ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
;BR+001
RTS PC

SETBR1:
;THIS SUBROUTINE SETS BR1 BIT

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PAGE: 0235

4718	035454	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4719	035456	000402	03200	000402		;BR+002
4720	035460	000207	03300	RTS	PC	
4721			03400			
4722			03500			
4723	035462		03600	SETBR4:		
4724			03700			;THIS SUBROUTINE SETS BR4 BIT
4725			03800			
4726	035462	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4727	035464	000420	04000	000420		;BR+020
4728	035466	000207	04100	RTS	PC	
4729			04200			
4730			04300			
4731	035470		04400	SETBR7:		
4732			04500			;THIS SUBROUTINE SETS BR7 BIT
4733			04600			
4734	035470	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4735	035472	000600	04800	000600		;BR+200
4736	035474	000207	04900	RTS	PC	
4737			05000			
4738			05100			
4739	035476		05200	SETC:		
4740			05300			;THIS SUBROUTINE SETS THE C BIT
4741			05400			
4742	035476	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4743	035500	000777	05600	000777		;BR+377
4744	035502	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4745	035504	063220	05800	063220		;SP(0)+BR
4746	035506	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4747	035510	060400	06000	060400		;BR+SP(0)+BR
4748	035512	000207	06100	RTS	PC	
4749			06200			
4750			06300			
4751	035514		06400	SETZ:		
4752			06500			;THIS SUBROUTINE SETS THE Z BIT
4753			06600			
4754	035514	104414		ROMCLK		;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
4755	035516	000777	06800	000777		;BR+377
4756	035520	000207	06900	RTS	PC	
4757			07000			
4758			07100			
4759	035522		07200	ROMDAT:		
4760			07300			;THIS SUBROUTINE LOADS R5 WITH EXPECTED ROM CONTENTS
4761			07400			;AND LOADS R4 WITH ACTUAL ROM CONTENTS
4762			07500			
4763	035522	017600	07600	MOV	2(SP),R0	;INDEX FOR COMPARE
4764	035526	062716	07700	ADD	#2,(SP)	;ADJUST STACK
4765	035532	012711	07800	MOV	#BIT10,(R1)	;SET ROMO
4766	035536	016005	07900	MOV	ROMMAP(R0),R5	;PUT "EXPECTED" IN R5
4767	035542	016104	08000	MOV	6(R1),R4	;PUT "FOUND" IN R4
4768	035546	000207	08100	RTS	PC	;RETURN
4769			08200			
4770	035550		08300	RAMDAT:		
4771			08400			;THIS SUBROUTINE LOADS R4 WITH THE LOWEST
4772			08500			;8 BITS OF THE CROM PC.
4773			08600			

4774	035550	017605	000000	08700
4775	035554	062716	000002	08800
4776	035560	005011		08900
4777	035562	052711	000400	09000
4779				09100
4779	035566	005011		09200
4780	035570	1044.4		
4781	035572	061225		09400
4782	035574	116104	000005	09500
4783	035600	000207		09600
4784				09700
4785	035602			09800
4786				09900
4787				10000
4788	035602	032737	100000 001366	10100
4789	035610	001420		10200
4790	035612	005000		10300
4791	035614	012702	011766	10400
4792	035620	012711	002000	10500
4793	035624	010061	000004	10600
4794	035630	012261	000006	10700
4795	035634	052711	020000	10800
4796	035640	005200		10900
4797	035642	022700	002000	11000
4798	035646	001364		11100
4799	035650	005011		11200
4800	035652	000207		11300
4801				11400
4802				11500
4803	035654			11600
4804				11700
4805				11800
4806				11900
4807				12000
4808				12100
4809				12200
4810				12300
4811	035654	005000		12400
4812	035656	012711	002000	12500
4813	035662	010061	000004	12600
4814	035666	012761	000437 000006	12700
4815	035674	052711	020000	12800
4816	035700	005200		12900
4817	035702	022700	002000	13000
4818	035706	001363		13100
4819	035710	005000		13200
4820	035712	012711	002000	13300
4821	035716	016061	035752 000004	13400
4822	035724	016061	035766 000006	13500
4823	035732	052711	020000	13600
4824	035736	005720		13700
4825	035740	022700	000014	13800
4826	035744	001362		13900
4827	035746	005011		14000
4828	035750	000207		14100
4829				14200

WROM:

```

MOV    2(SP),R5      ;GOOD DATA
ADD    #2,(SP)       ;ADJUST STACK
CLR    (R1)          ;CLEAR BIT10
BIS    #BIT8,(R1)    ;CLOCK INSTRUCTION IN CRAM THAT WAS
                        ;JUMPED TO, IT LOADS BR WITH ROM PC
CLR    (R1)          ;CLR BIT8
ROMCLK 061225        ;NEXT WORD IS INSTRUCTION, ROMCLK PC=5304
MOV    5(R1),R4      ;MOV BR TO PORT 5
RTS    PC             ;PUT "FOUND" IN R4
                        ;RETURN

```

;THIS SUBROUTINE WRITES THE ROMMAP INTO THE CRAM

```

BIT    #BIT15,STAT1  ;BE SURE DMC HAS CRAM
BEQ    2$             ;SKIP IF NO CRAM
CLR    R0             ;R0=CRAM ADDRESS
MOV    #ROMMAP,R2     ;R2 POINTS TO ROMMAP
1$:    MOV    #BIT10,(R1) ;SET ROMO
        MOV    R0,4(R1)  ;LOAD CRAM ADDRESS
        MOV    (R2)+,6(R1) ;LOAD WORD TO BE WRITTEN
        BIS    #BIT13,(R1) ;WRITE IT!
        INC    R0        ;NEXT ADDRESS
        CMP    #2000,R0  ;DONE YET?
        BNE    1$        ;BR IF NO
        CLR    (R1)      ;CLEAR SEL0
2$:    RTS    PC         ;RETURN

```

MEMSET:

```

;THIS SUBROUTINE LOADS CRAM WITH SPECIAL INSTRUCTIONS
;FOR THE CRAM JUMP TEST. ALL CRAM LOCATIONS ARE LOADED
;WITH INSTRUCTIONS THAT MOVE A 37 TO THE BR, EXCEPT THE
;FOLLOWING CRAM ADDRESSES: 0,1,4,7,525,1777. THESE LOCATIONS
;CONTAIN INSTRUCTIONS WHICH LOAD THE BR WITH THE LOWEST
;8 BITS OF THAT CRAM ADDRESS.

```

```

CLR    R0             ;R0 = CRAM ADDRESS
1$:    MOV    #BIT10,(R1) ;SET ROMO
        MOV    R0,4(R1)  ;LOAD CRAM ADDRESS
        MOV    #437,6(R1) ;LOAD INSTRUCTION
        BIS    #BIT13,(R1) ;WRITE INSTRUCTION IN CRAM
        INC    R0        ;NEXT ADDRESS
        CMP    #2000,R0  ;DONE YET?
        BNE    1$        ;BR IF NO
        CLR    R0        ;INDEX REGISTER
2$:    MOV    #BIT10,(R1) ;SET ROMO
        MOV    CRAMA(R0),4(R1) ;LOAD CRAM ADDRESS IN SEL4
        MOV    INSTU(R0),6(R1) ;LOAD INSTRUCTION TO BE WRITTEN
        BIS    #BIT13,(R1) ;WRITE CRAM!
        TST    (R0)+     ;NEXT
        CMP    #14,R0    ;DONE YET?
        BNE    2$        ;BR IF NO
        CLR    (R1)      ;CLEAR ALL BITS
        RTS    PC        ;RETURN

```

4830	035752	000000	000001	000004	14300	CRAMA:	.WORD	0,1,4,7,1777,525
4831	035760	000007	001777	000525				
4832	035766	000400			14400	INSTU:	000400	;BR+0
4833	035770	000401			14500		000401	;BR+1
4834	035772	000404			14600		000404	;BR+4
4835	035774	000407			14700		000407	;BR+7
4836	035776	000777			14800		000777	;BR+377
4837	036000	000525			14900		000525	;BR+125
4838					15000			
4839					15100			
4840	036002				15200	BASELD:		
4841					15300			;THIS SUBROUTINE LOADS THE DMC WITH A BASE ADDRESS
4842					15400			;AND PUTS DMC INTO FULL-DUPLEX MODE
4843					15500			
4844	036002	012711	040000		15600		MOV	#BIT14,(R1)
4845	036006	032737	100000	001366	15700		BIT	#BIT15,STAT1
4846	036014	001402			15800		BEG	.+6
4847	036016	012711	100000		15900		MOV	#BIT15,(R1)
4848	036022	105227	000000		16000		INCB	#0
4849	036026	001375			16100		BNE	.-4
4850	036030	005711			16200	1\$:	TST	(R1)
4851	036032	100376			16300		BPL	1\$
4852	036034	052711	004000		16400		BIS	#BIT11,(R1)
4853	036040	152711	000043		16500		BISB	#43,(R1)
4854	036044	105711			16600	2\$:	TSTB	(R1)
4855	036046	100376			16700		BPL	2\$
4856	036050	012761	035030	000004	16800		MOV	#BASE,4(R1)
4857	036056	005061	000006		16900		CLR	6(R1)
4858	036062	142711	000040		17000		BICB	#40,(R1)
4859	036066	105711			17100	3\$:	TSTB	(R1)
4860	036070	100776			17200		BMI	3\$
4861	036072	152711	000041				BISB	#41,(R1)
4862	036076	105711				64\$:	TSTB	(R1)
4863	036100	100376					BPL	64\$
4864	036102	005061	000006				CLR	6(R1)
4865	036106	142711	000040				BICB	#40,(R1)
4866	036112	105711				65\$:	TSTB	(R1)
4867	036114	100776					BMI	65\$
4868	036116	000207			17400		RTS	PC
4869					17500			;RETURN
4870	036120				17600	BASELH:		
4871					17700			;THIS SUBROUTINE LOADS THE DMC WITH A BASE ADDRESS
4872					17800			;AND PUTS DMC INTO HALF-DUPLEX MODE
4873					17900			
4874	036120	012711	040000		18000		MOV	#BIT14,(R1)
4875	036124	032737	100000	001366	18100		BIT	#BIT15,STAT1
4876	036132	001402			18200		BEG	.+6
4877	036134	012711	100000		18300		MOV	#BIT15,(R1)
4878	036140	105227	000000		18400		INCB	#0
4879	036144	001375			18500		BNE	.-4
4880	036146	005711			18600	1\$:	TST	(R1)
4881	036150	100376			18700		BPL	1\$
4882	036152	052711	004000		18800		BIS	#BIT11,(R1)
4883	036156	152711	000043		18900		BISB	#43,(R1)
4884	036162	105711			19000	2\$:	TSTB	(R1)
4885	036164	100376			19100		BPL	2\$

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4886	036166	012761	035030	000004	19200	MOV	#BASE,4(R1)	;LOAD BASE ADDRESS
4887	036174	005061	000006		19300	CLR	6(R1)	;CLEAR CC
4888	036200	142711	000040		19400	BICB	#40,(R1)	;CLEAR RQI
4889	036204	105711			19500	TSTB	(R1)	;RDY I CLEAR?
4890	036206	100776			19600	BMI	3\$	;BR IF NO
4891	036210	152711	000041			BISB	#41,(R1)	;ASK FOR CNTL I
4892	036214	105711				TSTB	(R1)	;WAIT FOR RDI
4893	036216	100376				BPL	64\$	;BR IF NOT SETY
4894	036220	012761	002000	000006		MOV	#BIT10,6(R1)	;SET HALF DUPLEX
4895	036226	142711	000040			BICB	#40,(R1)	;CLEAR RQI
4896	036232	105711				TSTB	(R1)	;RDI UP?
4897	036234	100776				BMI	65\$	;BR IF YES
4898	036236	000207			19800	RTS	PC	;RETURN
4899					19900			
4900	036240				20000	RFRELD:		;THIS SUBROUTINE LOADS THE DMC WITH A RECEIVE BA/CC
4901					20100			
4902					20200			
4903	036240	152711	000044		20300	BISB	#44,(R1)	;REC BA/CC REQUEST
4904	036244	105711			20400	TSTB	(R1)	;RDY I SET?
4905	036246	100376			20500	BPL	1\$	;BR IF NO
4906	036250	012561	000004		20600	MOV	(R5)+,4(R1)	;LOAD REC BA
4907	036254	012561	000006		20700	MOV	(R5)+,6(R1)	;LOAD REC CC
4908	036260	142711	000040		20800	BICB	#40,(R1)	;CLEAR RQI
4909	036264	105711			20900	TSTB	(R1)	;IS RDY I CLEAR
4910	036266	100776			21000	BMI	2\$	;BR IF NO
4911	036270	000205			21100	RTS	R5	;RETURN
4912					21200			
4913	036272				21300	XFRELD:		;THIS SUBROUTINE LOADS THE DMC WITH A TRANSMIT BA/CC
4914					21400			
4915					21500			
4916	036272	152711	000040		21600	BISB	#40,(R1)	;XMIT BA/CC REQUEST
4917	036276	105711			21700	TSTB	(R1)	;RDY I SET?
4918	036300	100376			21800	BPL	1\$	;BR IF NO
4919	036302	012561	000004		21900	MOV	(R5)+,4(R1)	;LOAD XMIT BA
4920	036306	012561	000006		22000	MOV	(R5)+,6(R1)	;LOAD XMIT CC
4921	036312	142711	000040		22100	BICB	#40,(R1)	;CLEAR RQI
4922	036316	105711			22200	TSTB	(R1)	;IS RDY I CLEAR
4923	036320	100776			22300	BMI	2\$	;BR IF NO
4924	036322	000205			22400	RTS	R5	;RETURN
4925					00300			
	036324	041777	040522	020115	00400	EM1:	.ASCIZ	<377>/CRAM DATA ERROR/
	036345	377	051103	046501	00500	EM2:	.ASCIZ	<377>/CRAM DUAL ADDRESSING ERROR/
	036401	377	051103	046517	00600	EM3:	.ASCIZ	<377>/CROM DATA ERROR/
	036422	045377	046525	020120	00700	EM4:	.ASCIZ	<377>/JUMP ERROR/
	036436	047777	052104	042440	00800	EM5:	.ASCIZ	<377>/ODT ERROR IN IBUS* REGIO/
	036470	044777	050117	046440	00900	EM6:	.ASCIZ	<377>/IOP MAIN MEMORY TEST/
	036516	044777	050117	046440	01000	EM7:	.ASCIZ	<377>/IOP MAR TEST/
	036534	041377	020122	044522	01100	EM10:	.ASCIZ	<377>/BR RIGHT SHIFT TEST/
	036561	377	042522	042503	01200	EM11:	.ASCIZ	<377>/RECEIVE DATA ERROR/
	036605	377	051106	042505	01300	EM12:	.ASCIZ	<377>/FREE RUNNING ERROR/
	036631	377	047503	052116	01400	EM13:	.ASCIZ	<377>/CONTROL OUT ERROR/
	036654	044777	052116	051105	01500	EM14:	.ASCIZ	<377>/INTERNAL DDCMP ERROR COUNTS NON ZERO/
					01600			
	036722	042777	050130	041505	01700	DH1:	.ASCIZ	<377>/EXPECTED FOUND ADDRESS/
	036754	042777	050130	041505	01800	DH2:	.ASCIZ	<377>/EXPECTED FOUND/
	036775	377	051440	046105	01900	DH3:	.ASCIZ	<377>/SEL4 SEL6/

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037016	041377	051501	025505	02000	DH4:	.ASCIZ	'377' / BASE+3 THRU BASE+12 /
				02100		.EVEN	
				02200			
037044	000003			02300	DT1:	3	
037046	006	004		02400		.BYTE	6,4
037050	001264			02500		SAVR2	
037052	006	004		02600		.BYTE	6,4
037054	001270			02700		SAVR4	
037056	004	002		02800		.BYTE	4,2
037060	001260			02900		SAVR0	
037062	000003			03000	DT2:	3	
037064	006	004		03100		.BYTE	6,4
037066	001272			03200		SAVR5	
037070	006	004		03300		.BYTE	6,4
037072	001270			03400		SAVR4	
037074	004	002		03500		.BYTE	4,2
037076	001264			03600		SAVR2	
037100	000003			03700	DT3:	3	
037102	006	004		03800		.BYTE	6,4
037104	001272			03900		SAVR5	
037106	006	004		04000		.BYTE	6,4
037110	001270			04100		SAVR4	
037112	004	002		04200		.BYTE	4,2
037114	001252			04300		TEMP3	
037116	000002			04400	DT4:	2	
037120	003	007		04500		.BYTE	3,7
037122	001272			04600		SAVR5	
037124	003	002		04700		.BYTE	3,2
037126	001270			04800		SAVR4	
037130	000002			04900	DT5:	2	
037132	006	004		05000		.BYTE	6,4
037134	001272			05100		SAVR5	
037136	006	002		05200		.BYTE	6,2
037140	001270			05300		SAVR4	
037142	000003			05400	DT6:	3	
037144	003	010		05500		.BYTE	3,10
037146	001272			05600		SAVR5	
037150	003	004		05700		.BYTE	3,4
037152	001270			05800		SAVR4	
037154	004	002		05900		.BYTE	4,2
037156	034704			06000		FLAG	
037160	000003			06100	DT7:	3	
037162	003	010		06200		.BYTE	3,10
037164	001272			06300		SAVR5	
037166	003	004		06400		.BYTE	3,4
037170	001270			06500		SAVR4	
037172	004	002		06600		.BYTE	4,2
037174	001264			06700		SAVR2	
037176	000003			06800	DT10:	3	
037200	003	007		06900		.BYTE	3,7
037202	001272			07000		SAVR5	
037204	003	004		07100		.BYTE	3,4
037206	001270			07200		SAVR4	
037210	006	002		07300		.BYTE	6,2
037212	001252			07400		TEMP3	
037214	000002			07500	DT11:	2	

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037216	006	004	07600	.BYTE	6.4
037220	001252		07700	TEMP3	
037222	006	002	07800	.BYTE	6.2
037224	001254		07900	TEMP4	
037226	000010		08000	DT12:	10
037230	003	002	08100	.BYTE	3.2
037232	001250		08200	TEMP2	
037234	003	002	08300	.BYTE	3.2
037236	035034		08400	BASE+4	
037240	003	002	08500	.BYTE	3.2
037242	001252		08600	TEMP3	
037244	003	002	08700	.BYTE	3.2
037246	035036		08800	BASE+6	
037250	003	002	08900	.BYTE	3.2
037252	001254		09000	TEMP4	
037254	003	002	09100	.BYTE	3.2
037256	035040		09200	BASE+10	
037260	003	002	09300	.BYTE	3.2
037262	001256		09400	TEMP5	
037264	003	002	09500	.BYTE	3.2
037266	035042		09600	BASE+12	
			09700		
037270			09800	.ERRTAB:	
037270	000000		09900	0	
037272	000000		10000	0	
037274	000000		10100	0	
037276	036324		10200	EM1	
037300	036722		10300	DH1	:HLT 1
037302	037044		10400	DT1	
037304	036345		10500	EM2	
037306	036722		10600	DH1	:HLT 2
037310	037044		10700	DT1	
037312	036324		10800	EM1	
037314	036722		10900	DH1	:HLT 3
037316	037062		11000	DT2	
037320	036401		11100	EM3	
037322	036722		11200	DH1	:HLT 4
037324	037100		11300	DT3	
037326	036422		11400	EM4	
037330	036754		11500	DH2	:HLT 5
037332	037116		11600	DT4	
037334	036422		11700	EM4	
037336	036754		11800	DH2	:HLT 6
037340	037130		11900	DT5	
037342	036436		12000	EM5	
037344	036754		12100	DH2	:HLT 7
037346	037116		12200	DT4	
037350	036470		12300	EM6	
037352	036722		12400	DH1	:HLT 10
037354	037142		12500	DT6	
037356	036516		12600	EM7	
037360	036722		12700	DH1	:HLT 11
037362	037160		12800	DT7	
037364	036534		12900	EM10	
037366	036754		13000	DH2	:HLT 12
037370	037116		13100	DT4	

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PAGE: 0241

037372	036561	13200	EM11		
037374	036722	13300	DH1	:HLT	13
037376	037176	13400	DT10		
037400	036605	13500	EM12		
037402	000000	13600	0	:HLT	14
037404	000000	13700	0		
037406	036605	13800	EM12		
037410	036754	13900	DH2	:HLT	15
037412	037130	14000	DT5		
037414	036631	14100	EM13		
037416	036775	14200	DH3	:HLT	16
037420	037214	14300	DT11		
037422	036654	14400	EM14		
037424	037016	14500	DH4	:HLT	17
037426	037226	14600	DT12		
		14700			
		14800			
037430		14900	CORMAX:		
	000001	15400	.END		

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ADRCNT=	004301	858*	894*	903#										
AJDONE	002734	566	639#											
AUSTRY	002446	565#	596	643										
AUTO.S	010252	528	1343#											
BASE	035030	3841	4441	4446	4452	4455	4458	4459	4460	4461	4484	4500	4689#	4856,
		4986	4925											
BASELD	036002	3980	4036	4085	4131	4180	4224	4840#						
BASELH	036120	4268	4870#											
BINWRD	004622	944*	947*	948	985#									
BIT0 =	000001	95#	1133	1134	3804	3914	3929	3974	3995	4030	4053	4079	4099	4125
		4148	4174	4192	4218	4236	4262	4305	4413	4545				
BIT1 =	000002	94#	533	1127	1133	1134	1503	4482						
BIT10 =	002000	85#	1475	1486	1682	1718	1754	1770	1804	2108	4765	4732	4812	4820
		4894												
BIT11 =	004000	84#	3833	4852	4882									
BIT12 =	010000	83#	1427	1501	3807	3977	4033	4082	4128	4177	4221	4265	4308	4485
BIT13 =	020000	82#	1430	1478	1505	1685	1721	1757	4795	4815	4823			
BIT14 =	040000	81#	761	1441	1443	1505	1516	3818	3831	4340	4557	4844	4874	
BIT15 =	100000	80#	487	569	572	1414	1481	1677	1712	1750	1797	1832	1878	1927
		1994	2036	2097	2146	2202	2255	2311	2367	2423	2479	2535	2592	2649
		2706	2763	2820	2877	2938	3000	3059	3121	3183	3245	3307	3369	3431
		3493	3555	3617	3679	3741	3802	3819	3821	3972	4028	4077	4123	4172
		4216	4260	4303	4341	4343	4558	4560	4788	4845	4847	4875	4877	
BIT2 =	000004	93#	533	692	1134	3908	3999	4574						
BIT3 =	000010	92#	1507	1514	4506	4530								
BIT4 =	000020	91#	1117	1140	1142	4057								
BIT5 =	000040	90#	1618	2047										
BIT6 =	000100	89#	1122	1123	1509	2062	4360	4566						
BIT7 =	000200	88#	1123	1240	1618									
BIT8 =	000400	87#	1465	1496	1498	1511	1513	1519	1522	1579	2045	4103	4152	4777
BIT9 =	001000	86#	1483	1485	1493	1519	1522	1577	1579	4196	4240	4550	4554	
BM	006756	1165#	1455											
BRLVL	011720	1574	1584	1592	1604#									
BRW	003640	698	784#											
BRX	003642	699	785#											
CHRCNT	004620	942*	945	949	965*	983#	984							
CKSWR	007362	514	759	790	1005	1190#								
CKSWR1	007426	1200#	1212											
CKSWR2	007440	1203#			</									

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[illegible]

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DMS114	001642	341#
DMS115	001652	346#
DMS116	001662	351#
DMS117	001672	356#
DMS200	001504	282#
DMS201	001514	287#
DMS202	001524	292#
DMS203	001534	297#
DMS204	001544	302#
DMS205	001554	307#
DMS206	001564	312#
DMS207	001574	317#
DMS210	001604	322#
DMS211	001614	327#
DMS212	001624	332#
DMS213	001634	337#
DMS214	001644	342#
DMS215	001654	347#
DMS216	001664	352#
DMS217	001674	357#
DMS300	001506	283#
DMS301	001516	288#
DMS302	001526	293#
DMS303	001536	298#
DMS304	001546	303#
DMS305	001556	308#
DMS306	001566	313#
DMS307	001576	318#
DMS310	001606	323#
DMS311	001616	328#
DMS312	001626	333#
DMS313	001636	338#
DMS314	001646	343#
DMS315	001656	348#
DMS316	001666	353#
DMS317	001676	358#
DMTLVL	001402	262#
DMTVEC	001400	261#
DM.END	001700	360#
DM.MAP	001500	195
DT1	037044	4925#
DT10	037176	4925#
DT11	037214	4925#
DT12	037226	4925#
DT2	037062	4925#
DT3	037100	4925#
DT4	037116	4925#
DT5	037130	4925#
DT6	037142	4925#
DT7	037160	4925#
EM1	036324	4925#
EM10	036534	4925#
EM11	036561	4925#
EM12	036605	4925#
EM13	036631	4925#
EM14	036654	4925#

1295*	1296*	4321*							
1293*	1294*	1295	4320*						
1347									
279*	485	538	548	642	1265	1267	1345	1350	1562

M03

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PAGE: 0245

EM2	036345	4925#																		
EM3	036401	4925#																		
EM4	036422	4925#																		
EM5	036436	4925#																		
EM6	036470	4925#																		
EM7	036516	4925#																		
ENDEX	032334	4412	4437#																	
ENDEX1	032434	4307	4457#	4463	4474	4573														
ENDEX2	032436	4442	4447	4453	4456	4458#														
ENDEX3	032472	4371	4464#																	
ERCT00	001704	367#																		
ERCT01	001710	370#																		
ERCT02	001714	373#																		
ERCT03	001720	376#																		
ERCT04	001724	379#																		
ERCT05	001730	382#																		
ERCT06	001734	385#																		
ERCT07	001740	388#																		
ERCT10	001744	391#																		
ERCT11	001750	394#																		
ERCT12	001754	397#																		
ERCT13	001760	400#																		
ERCT14	001764	403#																		
ERCT15	001770	406#																		
ERCT16	001774	409#																		
ERCT17	002000	412#																		
ERR	002612	589	599#	603																
ERRCNT	001232	163#	727	754	1066*	1280*														
ERRFLG	001325	202#	483#	713*	775*	1016*	1029	1043*	1101*											
ERRMSG	005100	1026*	1044	1047#																
ERRPC	002702	605	621#																	
ERTAB0	005224	1041	1075#																	
EXIT =	000205	96#																		
EXITER	005160	1061	1056#																	
FLAG	034704	1834*	1838	1839	1860*	1861	1880*	1885	1886	1908*	1909	1929*	1930	1933						
		1934	1952*	1953	1956*	1957	1960	1961	1976*	1977	4339*	4350	4361	4369						
		4386	4408	4410*	4413	4418*	4435*	4438	4536	4547	4549*	4675#	4925							
FLOAT	002536	582#	588																	
FY	002562	590#	594																	
HALTS	005130	1012	1058#																	
HILIM	004274	855*	882	900#																
ICOUNT	001222	159#	773	778*																
IISR	032534	4318	4478#																	
INBUF	007256	825	861	1180#																
INCHAR	007560	1206	1234#																	
INIFLG	001324	201#	509	529	536*															
INSTER=	104404	223#	876																	
INSTR =	104403	221#	1304	1356	1369	1378	1445	1454												
INSTR2	004074	832	844#																	
INSTU	035766	4822	4832#																	
INTTY	011734	1389	1406	1417	1433	1612#														
KMCM	007220	618	1165#																	
LIMITS	004222	871	882#																	
LINE	006720	1165#	1446																	
LOBITS	004300	857*	886	902#	903															
LOCK	001220	158#	777*	793	795	1035	1675*	1709*	1747*	1768*	1794*	1829*	1875*	1924*						

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PAGE: 024E

		1955*	2033*	2059*	2094*	2143*	2160*	2173*	2199*	2215*	2227*	2252*	2269*	2292*
		2308*	2325*	2338*	2364*	2381*	2394*	2420*	2437*	2450*	2476*	2493*	2506*	2532*
		2549*	2562*	2589*	2606*	2619*	2646*	2663*	2676*	2703*	2720*	2733*	2760*	2777*
		2790*	2817*	2834*	2847*	2874*	2891*	2904*	2935*	2953*	2966*	2997*	3014*	3026*
		3056*	3074*	3087*	3118*	3136*	3149*	3180*	3198*	3211*	3242*	3260*	3273*	3304*
		3322*	3335*	3366*	3384*	3397*	3428*	3446*	3459*	3490*	3508*	3521*	3552*	3570*
		3583*	3614*	3632*	3645*	3676*	3694*	3707*	3738*	3756*	3769*			
LOKFLG	001326	203*												
LOLIM	004272	854*	884	899*										
LPCNT	001224	160*	772*	773	776*									
LSTERR	001234	164*	492*	712*	1013	1015*	1102*							
MASKX	001244	172*												
MASTEK	006044	1037	1165*											
MCRLF	005574	810	933	1033	1034	1042	1165*	1303	1365					
MCSRX	005774	717	1165*											
MDATA	007320	963	973	1182*										
MEMLIM	001304	188*	680*											
MEMSET	035654	2940	3002	3061	3123	3185	3247	3309	3371	3433	3495	3557	3619	3681
		3743	4803*											
MEPASS	005635	716	1165*											
MERRPC	006121	1040	1165*											
MERRX	006021	723	1165*											
MERR2	005662	1165*	1547											
MERR3	005707	653	1165*											
MILK	001322	196*	486*	725	1263*	1268*	1272							
MLOCK	005745	694	1165*											
MNEW	006046	648	1165*											
MDOU	006606	1165*	1416											
MPASSX	006010	721	1165*											
MPFAIL	005577	1099	1165*											
MQM	005570	840	1165*	1327	1402	1412	1425	1439						
MR	005657	703	1165*	1321										
MRESET=	004000	96*												
MSTCLR=	104412	235*	1104	1637	1711	1749	1796	1831	1877	1926	1993	2035	2096	2145
		2201	2254	2310	2366	2422	2478	2534	2591	2648	2705	2762	2819	2876
		2937	2999	3058	3120	3182	3244	3306	3368	3430	3492	3554	3616	3678
		3740	3801	3971	4027	4076	4122	4171	4215	4259	4302			
MTITLE	001000	136*	513											
MTSTN	006032	1038	1165*	1305										
MTSTPC	005733	1165*												
MVECX	006002	719	1165*											
NEXT	001216	157*	779	1071	1635*	1674*	1708*	1746*	1793*	1828*	1874*	1923*	1991*	2032*
		2093*	2142*	2198*	2251*	2307*	2363*	2419*	2475*	2531*	2588*	2645*	2702*	2759*
		2816*	2873*	2934*	2996*	3055*	3117*	3179*	3241*	3303*	3365*	3427*	3489*	3551*
		3613*	3675*	3737*	3799*	3969*	4025*	4074*	4120*	4169*	4213*	4257*	4300*	
NOACT	007056	525	1165*	1257										
NODEV	002606	574	597*											
NUM	006352	1165*	1357											
OISR	033040	4320	4545*											
OK	002600	570	573	592	595*	620								
ONE	001302	187*												
FACT00	001702	366*												
FACT01	001706	369*												
FACT02	001712	372*												
FACT03	001716	375*												
FACT04	001722	378*												

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PAGE: 0247

PACT05	001726	381#																		
PACT06	001732	384#																		
PACT07	001736	387#																		
PACT10	001742	390#																		
PACT11	001746	393#																		
PACT12	001752	396#																		
PACT13	001756	399#																		
PACT14	001762	402#																		
PACT15	001766	405#																		
PACT16	001772	408#																		
PACT17	001776	411#																		
PARAM =	104405	225#	1306	1358	1371	1380	1447	1456												
PARAM1	004142	860#	877																	
PARBIT=	040000	96#																		
PARERR	004216	863	865	867	876#	883	885	887												
PASCNT	001230	162#	714*	715	726	751	1279*													
PERFOR=	004537	96#																		
PFTAB	005332	1100	1106#																	
POPRO =	012600	72#	1065																	
POP1SP=	005726	70#																		
POP2SP=	022626	74#	781																	
PRI0	006451	1165#	1388																	
PS =	177776	63#	478*	691*	1574*	1594*	4311*	4368*												
PUSHRO=	010046	71#	1062																	
PUSH1S=	005746	69#																		
PUSH2S=	024646	73#																		
QV.FLG	001327	204#	484*	730*	770															
RAMDAT	035550	2947	2960	2973	3008	3020	3032	3068	3081	3094	3130	3143	3156	3192						
		3205	3218	3254	3267	3280	3316	3329	3342	3376	3391	3404	3440	3453						
		3466	3502	3515	3528	3564	3577	3590	3626	3639	3652	3688	3701	3714						
		3750	3763	3776	4770#															
RBUF	034762	3812	3871	3932	3940	4038	4270	4687#												
RBUFF	033746	4327	4660#																	
RBUFFE	034702	4348	4668#																	
RBUFF1	033746	4661#																		
RBUFF2	034052	4662#																		
RBUFF3	034156	4663#																		
RBUFF4	034262	4664#																		
RBUFF5	034366	4665#																		
RBUFF6	034472	4666#																		
RBUFF7	034576	4667#																		
RCNTAB	033620	4335	4337	4511	4518	4654#														
RCOUNT	034760	3810	3872	3935	3938	4686#														
RDNTAB	033656	4346	4382	4405	4611*	4613*	4657*													
RECBA	033452	4426	4510	4598	4622#															
RESREG	005126	1054	1057#																	
RESTAR	005252	1086	1092#																	
RESTR1	003444	729	733	741#																
RESUME	033450	4345*	4480	4488*	4492	4563*	4621*													
RES05 =	104407	229#	1057																	
RETJRN	001214	156#	494*	700*	704	741*	779*	783	1071*	1073	1105	1320*	1330*	1332						
RFLAG	034710	3817*	3925	3928*	3953	4677#														
RFRELD	036240	4037	4132	4269	4900#															
ROMCLK=	104414	239#	1112	1115	1152	1157	1642	1644	1646	1654	1656	1840	1842	1845						
		1847	1849	1887	1889	1892	1894	1896	1935	1937	1940	1942	1944	1962						
		1964	1966	1968	1997	2000	2006	2009	2039	2042	2054	2060	2068	2070						

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CROSS REFERENCE TABLE -- USER SYMBOLS

		2072	2106	2150	2152	2163	2165	2176	2178	2205	2207	2217	2219	2229
		2231	2259	2261	2272	2274	2285	2287	2315	2317	2328	2330	2341	2342
		2371	2373	2384	2386	2397	2399	2427	2429	2440	2442	2453	2455	2483
		2485	2496	2498	2509	2511	2539	2541	2552	2554	2565	2567	2596	2598
		2609	2611	2622	2624	2653	2655	2666	2668	2679	2681	2710	2712	2723
		2725	2736	2738	2767	2769	2780	2782	2793	2795	2824	2826	2837	2839
		2850	2852	2881	2883	2894	2896	2907	2909	2943	2945	2956	2958	2969
		2971	3004	3006	3016	3018	3028	3030	3064	3066	3077	3079	3090	3092
		3126	3128	3139	3141	3152	3154	3188	3190	3201	3203	3214	3216	3250
		3252	3263	3265	3276	3278	3312	3314	3325	3327	3338	3340	3374	3376
		3387	3389	3400	3402	3436	3438	3449	3451	3462	3464	3498	3500	3511
		3513	3524	3526	3560	3562	3573	3575	3586	3588	3622	3624	3635	3637
		3648	3650	3684	3686	3697	3699	3710	3712	3746	3748	3759	3761	3772
		3774	4698	4700	4702	4710	4718	4726	4734	4742	4744	4746	4754	4780
ROMDAT	035522	2154	2167	2180	2209	2221	2233	2263	2276	2289	2319	2332	2345	2375
		2388	2401	2431	2444	2457	2487	2500	2513	2543	2556	2569	2600	2613
		2626	2657	2670	2683	2714	2727	2740	2771	2784	2797	2828	2841	2854
		2885	2898	2911	4759*									
ROMMAP	011766	1622*	1801	2100	4766	4791								
RUN	001316	193*	487*	1261*	1262*	1269								
SAVACT	001312	191*	651	1545*										
SAVNUM	001314	192*	481*	728*	731*	1538*								
SAVPC	001276	185*	603*	623	908*	1077								
SAVRO	001260	178*	917*	922	4925									
SAVR1	001262	179*	609*	626	916*	923								
SAVR2	001264	180*	915*	924	4925									
SAVR3	001266	181*	914*	925										
SAVR4	001270	182*	913*	926	4925									
SAVR5	001272	183*	912*	927	4925									
SAVSP	001274	184*												
SAVOS =	104406	227*	1017											
SCAN	032020	4369*	4469	4472										
SCAN1	032504	4374	4377	4380	4465	4467*								
SCAN2	032046	4373	4375*	4466										
SCOPE =	104400	215*	1663	1697	1734	1780	1817	1863	1911	1979	2019	2080	2129	2186
		2239	2295	2351	2407	2463	2519	2575	2632	2689	2746	2803	2860	2917
		2979	3038	3100	3162	3224	3286	3348	3410	3472	3534	3596	3658	3720
		3782	3957	4010	4062	4108	4157	4201	4245	4283	4457			
SCOP1 =	104401	217*	1690	1726	1763	1776	1812	1856	1903	1951	1975	2053	2120	2159
		2172	2185	2214	2226	2238	2268	2281	2294	2324	2337	2350	2380	2393
		2406	2436	2449	2462	2492	2505	2518	2548	2561	2574	2605	2618	2631
		2662	2675	2688	2719	2732	2745	2776	2789	2802	2833	2846	2859	2890
		2903	2916	2952	2965	2978	3013	3025	3037	3073	3086	3099	3135	3148
		3161	3197	3210	3223	3259	3272	3285	3321	3334	3347	3383	3396	3409
		3445	3458	3471	3507	3520	3533	3569	3582	3595	3631	3644	3657	3693
		3706	3719	3755	3768	3781								
SETBRO	035446	2370	2383	2396	3187	3200	3213	4707*						
SETBR1	035454	2426	2439	2452	3249	3262	3275	4715*						
SETBR4	035462	2482	2495	2508	3311	3324	3337	4723*						
SETBR7	035470	2538	2551	2564	3373	3386	3399	4731*						
SETC	035476	2258	2271	2284	3063	3076	3089	4739*						
SETZ	035514	2314	2327	2340	3125	3138	3151	4751*						
SOFTSW	007612	1204	1243*											
SPACNT=	004621	943*	967	970*	984*									
STACK =	001200	64*	479	670	1072	1094								
STAT	001240	170*												

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PAGE: 0249

STAT1	001366	252*	1276*	1677	1712	1750	1797	1832	1878	1927	1994	2036	2097	2146
		2202	2255	2311	2367	2423	2479	2535	2592	2649	2706	2763	2820	2877
		2938	3000	3059	3121	3183	3245	3307	3369	3431	3493	3555	3617	3679
		3741	3802	3807	3819	3831	3972	3977	4028	4033	4077	4082	4123	4128
		4172	4177	4216	4221	4260	4265	4303	4308	4312	4341	4558	4788	4845
		4875												
STAT2	001370	253*	1277*											
STAT3	001372	254*	1278*	3804	3974	4030	4079	4125	4174	4218	4262	4305		
STRTSW	001236	169*	515*	518*	519	521	531	533	646	692	701	1298	1322*	1352
		1558												
SV05	004310	912*												
SWFLG	007556	482*	804	1199*	1226*	1232*								
SWMES	007107	1155*	1202											
SWMES1	007117	1165*	1205											
SWR	001202	143*	499*	501	505*	515	651	656	761	768	791	806	1006	1011
		1060	1067	1069	1130	1190	1225*							
SWREG	000176	129*	505	1190	1245									
SW00	= 000001	45*	519	1352	1558									
SW01	= 000002	44*	701	1298	1322									
SW02	= 000004	43*												
SW03	= 000010	42*	646											
SW04	= 000020	41*												
SW05	= 000040	40*												
SW06	= 000100	39*	1130											
SW07	= 000200	38*												
SW08	= 000400	37*	1067											
SW09	= 001000	36*	791											
SW10	= 002000	35*	1069											
SW11	= 004000	34*	768											
SW12	= 010000	33*	806	1006										
SW13	= 020000	32*	1011											
SW14	= 040000	31*												
SW15	= 100000	30*												
TBUF	034714	3887	3917	3939	3982	4041	4136	4273	4679*					
TBUFF	033510	4332	4576	4578	4625*									
TCOUNT	034712	3888	3920	4678*										
TEMP	001416	272*	950	1096*	1097*	1138*	1143*	1149*	1161*	3824*	3827*	3835*	3838*	3944*
		3847*	3865*	3868*	3874*	3877*	3881*	3884*	3890*	3893*	3896*	3900*	3985*	3999*
		4007*	4012*	4044*	4047*	4090*	4093*	4139*	4142*	4185*	4188*	4229*	4232*	4276*
		4279*	4366*	4467*										
TEMP1	001246	173*	539*	1167	1570*	1571*	3897*	3902*						
TEMP2	001250	174*	540*	1169	3905*	4367*	4458*	4470*	4925					
TEMP3	001252	175*	542*	563*	599	608*	1171	1361	1364	1464*	2113*	2115*	2116*	2117*
		2118*	3851*	3941*	4395*	4459*	4569*	4925						
TEMP4	001254	176*	543*	1173	1374	1377	1383	1386	1450	1453	1459	1462	3852*	4450*
		4570*	4925											
TEMP5	001256	177*	544*	1175	1355*	1368*	1556	4461*	4925					
TFLAG	034706	3816*	3910	3913*	3955	4325*	4336	4353	4415*	4417*	4676*			
TIMER	= 104416	243*												
TKCSR	001204	148*	764	827	1234	1612								
TKOBR	001206	149*	766	829	835	1192	1194	1236	1614					
TLAST	= 031432	1325	4690*											
TPCSR	001210	150*	811	833	1008	1237	1615							
TPOBR	001212	151*	813*	835*	1010*	1239*	1617*							
TRPOK	004636	996*												
TSTNO	001226	161*	493*	1080	1108	1309	1316	1319	1634*	1673*	1707*	1745*	1792*	1827*

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CROSS REFERENCE TABLE -- USER SYMBOLS

		1873*	1922*	1990*	2031*	2092*	2141*	2197*	2250*	2306*	2362*	2418*	2474*	2530*
		2587*	2644*	2701*	2758*	2815*	2872*	2933*	2995*	3054*	3116*	3178*	3240*	3302*
		3364*	3426*	3488*	3550*	3612*	3674*	3736*	3798*	3968*	4024*	4073*	4119*	4168*
		4212*	4256*	4299*										
TST1	015766	1312	1330	1634*										
TST10	017216	1874	1922*											
TST11	017516	1923	1990*											
TST12	017632	1991	2031*											
TST13	020040	2032	2092*											
TST14	020230	2093	2141*											
TST15	020420	2142	2197*											
TST16	020574	2198	2250*											
TST17	020764	2251	2306*											
TST2	016100	1635	1673*											
TST20	021154	2307	2362*											
TST21	021344	2363	2418*											
TST22	021534	2419	2474*											
TST23	021724	2475	2530*											
TST24	022114	2531	2587*											
TST25	022304	2588	2644*											
TST26	022474	2645	2701*											
TST27	022664	2702	2758*											
TST3	016214	1674	1707*											
TST30	023054	2759	2815*											
TST31	023244	2816	2872*											
TST32	023434	2873	2933*											
TST33	023630	2934	2995*											
TST34	024010	2996	3054*											
TST35	024204	3055	3116*											
TST36	024400	3117	3178*											
TST37	024574	3179	3240*											
TST4	016336	1708	1745*											
TST40	024770	3241	3302*											
TST41	025164	3303	3364*											
TST42	025360	3365	3426*											
TST43	025554	3427	3488*											
TST44	025750	3489	3550*											
TST45	026144	3551	3612*											
TST46	026340	3613	3674*											
TST47	026534	3675	3736*											
TST5	016516	1746	1792*											
TST50	026730	3737	3798*											
TST51	027742	3799	3968*											
TST52	030170	3969	4024*											
TST53	030362	4025	4073*											
TST54	030544	4074	4119*											
TST55	030736	4120	4168*											
TST56	031114	4169	4212*											
TST57	031272	4213	4256*											
TST6	016636	1793	1827*											
TST60	031432	4257	4299*	4690										
TST7	017024	1828	1873*											
T*ST	003522	695*	696*	698*	699*	762*								
T*WCSYN=	010000	96*												
TYPDAT	005114	1032	1050	1053*										
TYPE =	104402	219*	513	525	537	601	606	614	617	648	653	694	703	716

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CROSS REFERENCE TABLE -- USER SYMBOLS

	717	719	721	723	810	823	840	933	973	1033	1034	1037	1038
TYPMSG 005014	1040	1042	1046	1051	1099	1202	1205	1257	1303	1321	1327	1365	1387
VEC 006430	1401	1404	1411	1415	1424	1431	1438	1547					
VECMAP 011456	1030	1033*											
WHICH 011450	1165*	1379											
WRDCNT 004616	1546	1558*											
WRKO.F 005102	1367	1554*	982*										
WROM 035602	941*	974*											
XBX 004706	1045	1048*											
XCNTAB 033640	1800	3809	3979	4035	4094	4130	4179	4223	4267	4310	4785*		
XCSR 003456	1007	1009	1011*										
XDNTAB 033712	4352	4354	4421	4424	4582	4605	4655*						
XERR 003500	718	743*											
XFRELD 036272	4588*	4590*	4658*										
XHEAD 006126	724	752*											
XMITBA 033452	3981	4040	4086	4135	4272	4913*							
XPASS 003472	537	1165*											
XSTATQ 007230	4326	4330	4333	4517	4623*								
XTSTN 005232	722	749*											
XVEC 003464	546	1165*											
X0 = 000110	1039	1078*											
X1 = 000101	720	746*											
X2 = 000102	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*	4653*			
X3 = 000103	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*				
X4 = 000104	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*				
X5 = 000105	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*				
X6 = 000106	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*				
X7 = 000107	4626*	4629*	4632*	4635*	4638*	4641*	4644*	4647*	4650*				
ZERG 001300	186*												
\$COD = ***** U	1												
\$CRAP = 177777	1*	1624*	1627	1630*	1664*	1667	1669*	1698*	1701	1703*	1735*	1738	1741*
	1781*	1784	1788*	1818*	1821	1823*	1864*	1867	1869*	1912*	1915	1919*	1980*
	1983	1986*	2020*	2023	2027*	2081*	2084	2088*	2130*	2133	2137*	2187*	2190
	2193*	2240*	2243	2246*	2296*	2299	2302*	2352*	2355	2358*	2408*	2411	2414*
	2464*	2467	2470*	2520*	2523	2526*	2576*	2579	2583*	2633*	2636	2640*	2690*
	2693	2697*	2747*	2750	2754*	2804*	2807	2811*	2861*	2864	2868*	2919*	2921
	2929*	2980*	2983	2991*	3039*	3042	3050*	3101*	3104	3112*	3163*	3166	3174*
	3225*	3228	3236*	3287*	3290	3298*	3349*	3352	3360*	3411*	3414	3422*	3473*
	3476	3484*	3535*	3538	3546*	3597*	3600	3608*	3659*	3662	3670*	3721*	3724
	3732*	3783*	3786	3794*	3958*	3961	3964*	4014*	4017	4020*	4063*	4066	4069*
	4109*	4112	4115*	4158*	4161	4164*	4202*	4205	4208*	4246*	4249	4252*	4286*
	4289	4295*											
\$ENDAD 003432	123	511	735*	1058									
\$Y = 000060	1*	1624	1630	1632	1637*	1664	1669	1671	1677*	1698	1703	1705	1711
	1712*	1735	1741	1743	1749	1750*	1791	1788	1790	1796	1797*	1819	1823
	1825	1831	1832*	1864	1869	1871	1877	1878*	1912	1918	1920	1926	1927*
	1980	1986	1988	1993	1994*	2020	2027	2029	2035	2036*	2081	2088	2090
	2096	2097*	2130	2137	2139	2145	2146*	2187	2193	2195	2201	2202*	2240
	2246	2248	2254	2255*	2296	2302	2304	2310	2311*	2352	2358	2360	2366
	2367*	2408	2414	2416	2422	2423*	2464	2470	2472	2478	2479*	2520	2526
	2528	2534	2535*	2576	2583	2585	2591	2592*	2633	2640	2642	2648	2649*
	2690	2697	2699	2705	2706*	2747	2754	2756	2762	2763*	2804	2811	2813
	2819	2820*	2861	2868	2870	2876	2877*	2918	2929	2931	2937	2938*	2980
	2991	2993	2999	3000*	3039	3050	3052	3058	3059*	3101	3112	3114	3120

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CROSS REFERENCE TABLE -- USER SYMBOLS

		3121#	3163	3174	3176	3182	3183#	3225	3236	3238	3244	3245#	3287	3298
		3300	3306	3307#	3349	3360	3362	3368	3369#	3411	3422	3424	3430	3431#
		3473	3484	3486	3492	3493#	3535	3546	3548	3554	3555#	3597	3608	3610
		3616	3617#	3659	3670	3672	3678	3679#	3721	3732	3734	3740	3741#	3793
		3794	3796	3801	3802#	3958	3964	3966	3971	3972#	4014	4020	4022	4027
		4028#	4063	4069	4071	4076	4077#	4109	4115	4117	4122	4123#	4158	4164
		4166	4171	4172#	4202	4208	4210	4215	4216#	4246	4252	4254	4259	4260#
		4286	4295	4297	4302	4303#	4690#							
\$S	= 000062	1#	1635	1637#	1674	1677#	1708	1712#	1746	1750#	1793	1797#	1828	1832#
		1874	1878#	1923	1927#	1991	1994#	2032	2036#	2093	2097#	2142	2146#	2198
		2202#	2251	2255#	2307	2311#	2363	2367#	2419	2423#	2475	2479#	2531	2535#
		2588	2592#	2645	2649#	2702	2706#	2759	2763#	2816	2820#	2873	2877#	2934
		2938#	2996	3000#	3055	3059#	3117	3121#	3179	3183#	3241	3245#	3303	3307#
		3365	3369#	3427	3431#	3489	3493#	3551	3555#	3613	3617#	3675	3679#	3737
		3741#	3799	3802#	3969	3972#	4025	4028#	4074	4077#	4120	4123#	4169	4172#
		4213	4216#	4257	4260#	4303#								
\$Y	= 000017	1#	207#	215	217#	219#	221#	223#	225#	227#	229#	231#	233#	235#
.	= 037430	237#	239#	241#	243#	245#								
		108#	109	112#	119#	124#	127#	131#	135#	137#	189#	190#	191#	192#
		273#	278#	280#	281#	282#	283#	285#	286#	287#	288#	290#	291#	292#
		293#	295#	296#	297#	298#	300#	301#	302#	303#	305#	306#	307#	308#
		310#	311#	312#	313#	315#	316#	317#	318#	320#	321#	322#	323#	325#
		326#	327#	328#	330#	331#	332#	333#	335#	336#	337#	338#	340#	341#
		342#	343#	345#	346#	347#	348#	350#	351#	352#	353#	355#	356#	357#
		358#	517	527	638#	655	1088	1099	1146#	1181#	1183#	1235	1238	1259
		1353	1397	1500	1504	1550	1581	1613	1616	2046	2051	2066	2078	3803
		3805	3808	3820	3823	3826	3832	3837	3867	3876	3883	3892	3906	3911
		3915	3918	3921	3926	3930	3933	3936	3945	3950	3973	3975	3978	3988
		4029	4031	4034	4046	4078	4080	4083	4092	4106	4124	4126	4129	4141
		4155	4173	4175	4178	4183	4199	4217	4219	4222	4227	4231	4243	4261
		4263	4266	4304	4306	4309	4342	4359	4398	4491	4523	4559	4562	4565
		4623#	4654#	4655#	4657#	4658#	4661#	4662#	4663#	4664#	4665#	4666#	4667#	4687#
		4689#	4846	4849	4876	4879								
		670#												
.BEGIN	003062													
.CNVRT	004400	234	934#											
.CONVR	004374	232	933#											
.DATAC	005454	242	1137#											
.DELAY	005340	238	1110#											
.EOP	003274	711#	4300											
.ERRTA	037270	1025	4925#											
.HLT	004656	115	1005#											
.INSIE	004062	224	840#											
.INSTR	003756	222	819#											
.INST1	003776	823#	843											
.MSG	004000	821#	824#											
.MSTCL	005370	236	1121#											
.PARAM	004102	226	851#											
.PFAIL	005240	113	480											
.RES05	004342	230	922#											
.ROMCL	005406	240	1126#											
.SAV05	004302	228	908#											
.SCOPE	003506	216	759#											
.SCOP1	003644	213	790#											
.START	002002	132	478#											
.TIMER	005520	244	1148#											
.TRPSR	004624	117	993#											

1085# 1093 -

494 1222

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.TRPTA	001330	214*	999
.TYPE	003674	220	801*

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 DZDMH.P11 09-DEC-76 14:59 CROSS REFERENCE TABLE -- MACRO NAMES

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DMEND	1#	705													
DMFRNT	1#														
HLT	75#	1652	1662	1689	1725	1762	1775	1809	1855	1902	1950	1974	2015	2052	2067
	2079	2119	2158	2171	2184	2213	2225	2237	2267	2280	2293	2323	2336	2349	2379
	2392	2405	2435	2448	2461	2491	2504	2517	2547	2560	2573	2604	2617	2630	2661
	2674	2687	2718	2731	2744	2775	2788	2801	2832	2845	2858	2889	2902	2915	2951
	2964	2977	3012	3024	3036	3072	3085	3098	3134	3147	3160	3196	3209	3222	3258
	3271	3284	3320	3333	3346	3382	3395	3408	3444	3457	3470	3506	3519	3532	3568
	3581	3594	3630	3643	3656	3692	3705	3718	3754	3767	3780	3829	3840	3853	3855
	3870	3879	3886	3895	3904	3907	3912	3916	3919	3922	3927	3931	3934	3937	3946
	3951	3993	3997	4005	4051	4055	4061	4097	4101	4107	4146	4150	4156	4190	4194
	4200	4234	4238	4244	4284	4399	4462	4473	4571	4580	4587	4603	4610		
\$AJTO	1#	543													
\$BRRSH	1#	1624													
\$BJFFE	1#	1177													
\$BYTE	1#	4626	4629	4632	4635	4638	4641	4644	4647	4650					
\$CKDAT	1#	4392													
\$COMP	1#														
\$GRAM	1#	1664	1698												
\$GRAMD	1#	1735													
\$CYCLE	1#	1246													
\$DATAF	1#	3783													
\$EOP	1#	705													
\$EXER	1#	4286													
\$FD	1#	3857	4861												
\$FINI	1#	4690													
\$GETPA	1#														
\$HALF	1#	4246													
\$HD	1#	4891													
\$HEADE	1#														
\$IOPOD	1#	2020													
\$JUMP	1#	2130	2187	2240	2296	2352	2408	2464	2520	2576	2633	2690	2747	2804	2861
	2918	2980	3039	3101	3163	3225	3287	3349	3411	3473	3535	3597	3659	3721	
\$LSTDA	1#	4014													
\$MARHI	1#														
\$MEMFL	1#	1932	1978												
\$MEMD	1#	1864													
\$MEM1	1#	1818													
\$MEM2	1#	1912													
\$MEM3	1#	1980													
\$MOCK	1#														
\$MSG	1#	1165													
\$NONEX	1#	4063	4109												
\$ORUN	1#	3958													
\$PFAIL	1#	1081													
\$PROC	1#	4158													
\$PROC1	1#	4202													
\$QUEST	1#	1356	1369	1378	1445	1454									
\$RAMCL	1#	1109													
\$RCLK	1#	1112	1115	1152	1157	1642	1644	1646	1653	1656	1940	1842	1845	1847	1849
	1887	1889	1892	1894	1896	1935	1937	1940	1942	1944	1962	1964	1966	1968	1997
	2000	2006	2009	2039	2042	2054	2060	2068	2070	2072	2106	2150	2152	2163	2165
	2176	2178	2205	2207	2217	2219	2229	2231	2259	2261	2272	2274	2285	2297	2315
	2317	2328	2330	2341	2343	2371	2373	2384	2386	2397	2399	2427	2429	2440	2442
	2453	2455	2483	2485	2496	2498	2509	2511	2539	2541	2552	2554	2565	2567	2596
	2598	2609	2611	2622	2624	2653	2655	2666	2668	2679	2691	2710	2712	2723	2725

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CROSS REFERENCE TABLE -- MACRO NAMES

	2736	2738	2767	2769	2780	2782	2793	2795	2824	2826	2837	2839	2850	2852	2881
	2883	2894	2896	2907	2909	2943	2945	2956	2958	2969	2971	3004	3006	3016	3018
	3028	3030	3064	3066	3077	3079	3090	3092	3126	3128	3139	3141	3152	3154	3188
	3190	3201	3203	3214	3216	3250	3252	3263	3265	3276	3278	3312	3314	3325	3327
	3338	3340	3374	3376	3387	3389	3400	3402	3436	3438	3449	3451	3462	3464	3498
	3500	3511	3513	3524	3526	3560	3562	3573	3575	3586	3588	3622	3624	3635	3637
	3648	3650	3684	3686	3697	3699	3710	3712	3746	3748	3759	3761	3772	3774	4698
	4700	4702	4710	4718	4726	4734	4742	4744	4746	4754	4780				
\$RDROM	1#	1781													
\$ROMRD	1#	2081													
\$SCOPE	1#	755													
\$SETUP	1#	3972	4028	4077	4123										
\$SIMBC	1#														
\$SKIPT	1#	3802	3972	4028	4077	4123	4172	4216	4260	4303					
\$SOFTC	1#	1185													
\$TRPDE	1#	215	217	219	221	223	225	227	229	231	233	235	237	239	241
	243														
\$TSTN	1#	1632	1671	1705	1743	1790	1825	1871	1920	1988	2029	2090	2139	2195	2248
	2304	2360	2416	2472	2528	2585	2642	2699	2756	2813	2870	2931	2993	3052	3114
	3176	3238	3300	3362	3424	3486	3548	3610	3672	3734	3796	3966	4022	4071	4117
	4166	4210	4254	4297											
\$VARIA	1#	134													
\$XZ	1#	1624	1630	1664	1669	1698	1703	1735	1741	1781	1798	1818	1823	1864	1869
	1912	1918	1980	1986	2020	2027	2081	2088	2130	2137	2187	2193	2240	2246	2296
	2302	2352	2358	2408	2414	2464	2470	2520	2526	2576	2583	2633	2640	2690	2697
	2747	2754	2804	2811	2861	2868	2918	2929	2980	2991	3039	3050	3101	3112	3163
	3174	3225	3236	3287	3298	3349	3360	3411	3422	3473	3484	3535	3546	3597	3608
	3659	3670	3721	3732	3783	3794	3958	3964	4014	4020	4063	4069	4109	4115	4158
	4164	4202	4208	4246	4252	4286	4295								

. ABS. 037430 000

ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

DZDMH, DZDMH/SOL/CRF+IPLUTL, DZDMH
 RUN-TIME: 51.72 5 SECONDS
 RUN-TIME RATIO: 259/130=1.9
 CORE USED: 29K (57 PAGES)