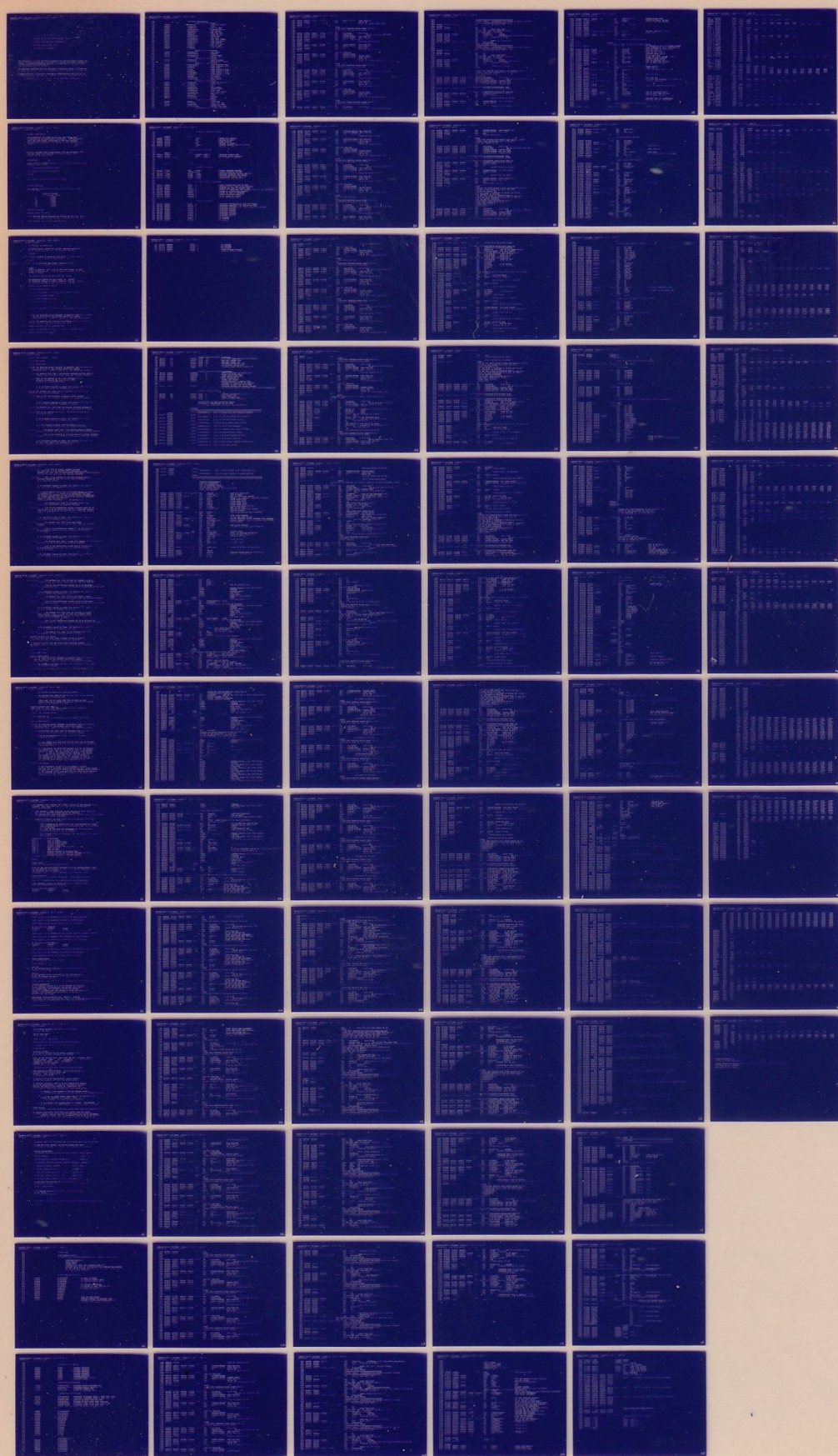


DU11

OFFLINE LOGI TESTS
MD-11-DZDUA-D

EP DZDUA D DL
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I D E N T I F I C A T I O N

PRODUCT NAME: D11 OFFLINE LOGIC TESTS

PRODUCT CODE: MAINDEC-11-DZDUA-D D

RELEASE DATE: 21 AUG 1976

MAINTAINER : DIAGNOSTICS

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GENERAL DESCRIPTION

THIS DIAGNOSTIC CAN CHAIN 16 DUI1'S. THIS MEANS THAT 16 DEVICES CAN BE SEQUENTIALLY EXERCISED. THE DIAGNOSTIC MAKES ONE PASS BEFORE PROCEEDING TO THE NEXT DEVICE, AND CONTINUES EXERCISING ALL DEVICES IN THIS FASHION UNTIL HALTED.

1. THE DUI1 OFFLINE LOGIC TESTS VERIFY THAT ALL REGISTERS EXIST ,AND ALL RESPECTIVE BITS CAN BE MASTER CLEARED, READ, WRITTEN AND/OR READ/WITTEN

2. REQUIREMENTS

PDP-11 FAMILY STANDARD COMPUTER WITH OR WITHOUT HARDWARE SWITCH REGISTER (LOC. 177570)

DUI1 SYNCHRONOUS/ISOCRONOUS OPTION

ONE CONSOLE TELETYPE OR EQUIVALENT

- 2.2 STORAGE

THE PROGRAM LOADS AND RUNS IN 8K OF MEMORY.

3. LOADING PROCEDURE

THE STANDARD PROCEDURE FOR LOADING ABSOLUTE BINARY TAPES IS TO BE USED.

	STARTING ADDRESS FOR ABSOLUTE LOADER
4K	017500
8K	037500
12K	057500
16K	077500
20K	117500
24K	137500
28K	157500

4. STARTING PROCEDURE

- 4.1 CONTROL SWITCH SETTINGS

NOTE: SOFTWARE SWITCH REGISTER IS DEFINED AS LOC. 176, WHILE THE SOFTWARE DISPLAY REGISTER IS DEFINED AS LOC. 174.

- 4.1.1 AFTER PROGRAM LOAD (INITIAL PROGRAM START)

ALL CONSOLE SWITCHES DOWN

- 4.1.2 TO MODIFY DEVICE VECTOR AND CONTROL REGISTER ADDRESSES
AFTER PROGRAM RESTART OR TO RUN MULTIPLE DEVICES

SW00=1

- 4.1.3 TO START PROGRAM AT SELECTED TEST AFTER A PROGRAM RESTART
(ONLY IN SINGLE DEVICE TESTS)

SW01=1

- 4.1.4 TO LOCK ON SELECTED TEST AFTER A PROGRAM RESTART
(ONLY IN SINGLE DEVICE TESTS)

SW02=1

NOTE1: IN GENERAL SW01 WILL BE USED WHEN SW02=1 IS USED

NOTE2: WITHOUT SW01=1 "LOCK ON TEST" WILL DEFAULT TO TEST 1
STARTING ADDRESS

- 4.2

THE STARTING ADDRESS FOR ALL TESTS IS 000200

THE RETARTING ADDRESS FOR ALL TESTS IS 000200

THE STARTING ADDRESS TO ENTER A SELECTED TEST IS 000200

THE STARTING ADDRESS TO LOCK ON TEST IS 000200

- 4.3 PROGRAM AND/OR OPERATOR ACTION

- 4.3.1 INITIAL PROGRAM START

4.3.1.1 LOAD PROGRAM INTO MEMORY WITH ABSOLUTE LOADER

4.3.1.2 LOAD ADDRESS 000200

4.3.1.3 CLEAR CONSOLE SWITCHES

4.3.1.4 PRESS START

4.3.1.5 THE PROGRAM WILL TYPE "D111 DZDUA-D TAPE A" (ONCE ONLY)

NOTE: IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:

SWR=XXXXXX NFW= (REFER TO SECTION 5. FOR OPERATOR'S OPTION)

4.3.1.7 THE PROGRAM WILL TYPE "P" TO INDICATE THAT IT IS ABOUT
TO START TESTING ,AND THEN TESTING WILL BEGIN

- 4.3.2 PROGRAM RESTART WITH ALL SWITCHES DOWN

4.3.2.1 THE PROGRAM WILL TYPE "R" AND WILL COMMENCE TESTING

- 4.3.3 PROGRAM RESTART WITH SW00=1

4.3.3.1 LOAD ADDRESS 000200

4.3.3.2 SET SW00=1

4.3.3.3 PRESS START

NOTE: IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:
SWP=XXXXXX NEW (REFER TO SECTION 5, FOR OPERATOR'S OPTION)

4.3.3.4 THE PROGRAM WILL TYPE "1ST DEVICE: RECEIVER CONTROL REGISTER
ADDRESS" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.5 TYPE IN THE ADDRESS OF THE FIRST RECEIVER CONTROL
REGISTER ADDRESS OF THE DU11 TO BE TESTED
FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.4

4.3.3.6 THE PROGRAM WILL TYPE "VECTOR ADDRESS-" AND WAIT FOR AN
INPUT FROM THE TELETYPE KEYBOARD

4.3.3.7 TYPE IN THE BASE RECEIVER INTERRUPT VECTOR ADDRESS
FOR THE DU11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ADDRESS IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.6

4.3.3.8 THE PROGRAM WILL TYPE "ARE YOU RUNNING MULTIPLE DEVICES ?"
(Y OR N)-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.9 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A
<CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS GIVEN, THE PROGRAM WILL TYPE "?"
AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.8

IF A "NO" ANSWER IS GIVEN: JUMP TO SECTION 4.3.3.12
IF A "YES" ANSWER IS GIVEN: THE NEXT QUESTION IS ASKED

4.3.3.10 THE PROGRAM WILL TYPE "LAST DEVICE: RECEIVER CONTROL
REGISTER ADDRESS-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.11 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL REGISTER
ADDRESS OF THE DU11 TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL THEN REPEAT THE MESSAGE OF 4.3.3.10
NOTE: ALL ADDRESSES SHALL BE CONTIGUOUS

4.3.3.11.1 IF AN "OUT OF RANGE" ADDRESS IS TYPED
IE, MORE THAN 16 (10) DEVICES AWAY (UPWARDS).....THE
PROGRAM WILL TYPE "OUT OF RANGE;RETYPE LAST DEVICE RXCSR ADDRESS-"
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.11.2 TYPE IN THE ADDRESS OF THE LAST RECEIVER CONTROL
REGISTER ADDRESS OF THE DU11 TO BE TESTED FOLLOWED
BY A <CARRIAGE RETURN>

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.11.1

IF A DEVICE ADDRESS LOWER THAN 1ST DEVICE ADDRESS IS TYPED.....
.....SCHOOLS OUT.....THERE IS NO PROTECTION FOR THIS.
THE PROGRAM WILL DEFAULT TO TWO DEVICES ACTIVE (UPWARDS FROM
1ST DEVICE ADDRESS).THE SAME APPLIES TO IDENTICAL ADDRESSES
TYPED FOR FIRST AND LAST DEVICE.
OBSERVE LOCATION # ACTRFG; SEE SECTION 7.2

4.3.3.12 THE PROGRAM WILL TYPE "DU PRIORITY LEVEL-" AND
WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.13 TYPE IN THE APPROPRIATE DEVICE PRIORITY LEVEL OF THE
DU11 OR DU11'S TO BE TESTED FOLLOWED BY A <CARRIAGE RETURN>
(NOTE THAT ALL MULTIPLE DEVICES MUST BE AT THE SAME PRIORITY
LEVEL). IE "5"

IF AN INCORRECT LEVEL IS TYPED ,THE PROGRAM WILL TYPE "?"
AND REPEAT THE MESSAGE OF 4.3.3.12

4.3.3.14 THE PROGRAM WILL TYPE "8 OF SYNC CHARS
SELECTED (1 OR 2)-" AND WAIT FOR AN INPUT FROM THE TELETYPE
KEYBOARD

4.3.3.15 TYPE IN THE APPROPRIATE ANSWER "1" OR "2" FOLLOWED
BY A <CARRIAGE RETURN>.(NOTE:ALL MULTIPLE DEVICES MUST
BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.14

4.3.3.16 THE PROGRAM WILL TYPE " IS SEC XMIT JUMPER #6 IN ? (Y OR N)-"
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.17 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED
BY A <CARRIAGE RETURN>.(NOTE THAT ALL MULTIPLE DEVICES
MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.16

4.3.3.18 THE PROGRAM WILL TYPE "IS SEC RFC JUMPER # 5 IN ?
(Y OR N)=-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.19 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED
BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.18

4.3.3.20 THE PROGRAM WILL TYPE "IS OPT CLR ENABLE JUMPER
4 IN ? (Y OR N)=-" AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.3.21 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED
BY A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.20

4.3.3.22 THE PROGRAM WILL TYPE "ARE YOU RUNNING IN MAINT.
MODE EXTERNAL ? AND DO YOU HAVE THE EXTERNAL MODEM
BYPASS JUMPER CONNECTOR ON ? (Y OR N)=-" AND WAIT FOR AN
INPUT FROM THE TELETYPE KEYBOARD

4.3.3.23 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY
A <CARRIAGE RETURN>. (NOTE: ALL MULTIPLE DEVICES MUST BE THE SAME)

IF AN INCORRECT ANSWER IS TYPED ,THE PROGRAM WILL TYPE "?"
AND WILL REPEAT THE MESSAGE OF 4.3.3.22

4.3.3.24 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT
HAS STARTED AND WILL COMMENCE TESTING AT TEST 1

4.3.4 PROGRAM RESTART WITH SW01=1
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED
,,,IT WILL NOT WORK IF MULTIPLE DEVICES ARE SELECTED

IF MULTIPLE DEVICES WERE PREVIOUSLY SELECTED,LOAD 000200,
AND SELECT SW00=1 AND ANSWER "NO" TO THE MULTIPLE DEVICE QUESTION
SFE 4.3.3

4.3.4.1 LOAD 000200

4.3.4.2 SET SW01=1

4.3.4.3 PRESS START
NOTE: IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:
SWR=XXXXXX NEW# (REFER TO SECTION 5, FOR OPERATOR'S OPTION)

4.3.4.4 THE PROGRAM WILL TYPE "TEST PC=-" AND WAIT FOR AN INPUT FROM
THE TELETYPE KEYBOARD

4.3.4.5 TYPE IN THE ADDRESS OF THE TEST AT WHICH THE PROGRAM IS TO

BE STARTED FOLLOWED BY A <CARRIAGE RETURN>

4.3.4.6 THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED TESTING AT THE SELECTED TEST

NOTE: CAPE MUST BE TAKEN WHEN THIS FEATURE IS USED
,SINCE THERE IS NO PROTECTION AGAINST SELECTING AN ADDRESS THAT IS IN THE MIDDLE OF A TEST

4.3.5 PROGRAM RESTART WITH SW02 =1
NOTE: THIS WILL ONLY WORK WHEN A SINGLE DEVICE IS SELECTED
SEE NOTE IN 4.3.4 FOR MORE DETAILS

4.3.5.1 LOAD ADDRESS 000200

4.3.5.2 SFT SW02 =1
NOTE: IT MAY BE ADVANTAGEOUS TO SET SW01=1 (OPTIONAL)

4.3.5.3 PRESS START

NOTE: IF THE SOFTWARE SWITCH REGISTER IS SELECTED THEN THE FOLLOWING
WILL BE TYPED AFTER THE PROGRAM IDENTIFIES ITSELF:
SWR=XXXXXX NEW (REFER TO SECTION 5, FOR OPERATOR'S OPTION)

4.3.5.4 THE PROGRAM WILL TYPE "LOCK ON SELECTED TEST ? (Y OR N)=-"
AND WAIT FOR AN INPUT FROM THE TELETYPE KEYBOARD

4.3.5.5 TYPE IN THE APPROPRIATE ANSWER YES OR NO FOLLOWED BY A
<CARRIAGE RETURN>

IF A NO ANSWER IS GIVEN: THIS LOCK ON TEST WILL BE IGNORED
AND THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED
TESTING AT TEST 1

4.3.5.6 IF A YES ANSWER WAS GIVEN: THE PROGRAM WILL ACT AS FOLLOWS...
THE PROGRAM WILL TYPE "R" TO INDICATE THAT IT HAS STARTED
TESTING AT TEST 1 AND WILL REMAIN IN TEST 1 UNTIL HALTED
OR IF ANY KEY IS STRUCK ON THE TELETYPE, THE PROGRAM
WILL FREEZE ON THE NEXT TEST UNTIL A KEY IS STRUCK ON
THE TELETYPE AND SO FORTH THRU THE PROGRAM. IF SW01 =1 IT
WILL PERFORM AS IN SECTION 4.3.4 ALLOWING ONE TO FREEZE
ON A SELECTED TEST RATHER THAN DEFAULTING TO TEST 1

5. OPERATING PROCEDURE

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
REGISTER (LOC. 176) IS USED.

CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY DOING THE FOLLOWING:

- 1) TYPE CONTROL G <"G"> THIS WILL ALLOW THE TTY TO ENTER DATA INTO LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THEN THE OPERATOR CAN DO ONE OF THE FOLLOWING AT THE TTY:
 - A) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A <CR>. (ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS WILL BE ALLOWED)
IF A <CR> IS THE FIRST KEY DEPRESSSED THE SOFTWARE SWITCH REGISTER CONTENTS WILL NOT BE CHANGED.
 - B) IF A CONTROL U <"U"> IS DEPRESSSED THEN THE PROGRAM WILL SEND YOU BACK TO STEP 2.

5.1 OPERATIONAL SWITCH SETTINGS

SW15 =1	HALT ON ERROR
SW14 =1	LOOP ON CURRENT TEST
SW13 =1	INHIBIT ERROR TYPEOUT
SW11 =1	INHIBIT ITERATIONS
SW10 =1	ESCAPE TO NEXT TEST ON ERROR
SW09 =1	LOOP ON ERROR
SW02 =1	LOCK ON TEST
SW01 =1	RESTART PROGRAM AT SELECTED TEST
SW00 =1	RESELECT VECTOR AND CONTROL REGISTER ADDRESSES
	6 PARAMETERS AFTER A PROGRAM RESTART

TO INHIBIT "END OF PASS" TYPEOUT - TURN TELETYPE OFF

6. EPROPS

6.1 ERROR HALTS
THERE ARE FOUR DISTINCT ERROR TYPEOUTS

NOTE: IF THE SOFTWARE SWITCH REGISTER IS TO BE CHANGED AFTER A HALT THE OPERATOR IS REQUIRED TO TYPE A <"G"> BEFORE DEPRESSING CONTINUE. THE FOLLOWING WILL BE TYPED:
SWR=XXXXXX NEW= (REFER TO SECTION 5. FOR OPERATOR OPTION)

6.1.1 PC+2 = ERROR PC
WHERE PC +2 IS THE ADDRESS OF THE CALL TO THE ERROR HANDLER +2

REFER TO THE ABOVE "HLT" IN DIAGNOSTIC FOR ERROR DESCRIPTION

CHECK ADDRESS 0 RXCSR: TO LOCATE THE DEVICE PRESENTLY UNDER TEST WHEN RUNNING MULTIPLE DEVICES

6.1.2 PC +2 = REGISTER ERROR PC

REGISTER	EXPECTED	ACTUAL
16XXXX	YYYYYY	ZZZZZZ

WHERE 16XXXX IS THE ADDRESS OF THE FAILING DEVICE REGISTER

WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER

6.1.3 PC +2 = RECEIVER ERROR PC
REGISTER EXPECTED ACTUAL
16XXXX YYYYYY ZZZZZZ

WHERE 16XXXX IS THE ADDRESS OF THE FAILING RECEIVER (RXDRUF) REGISTER

WHERE YYYYYY IS THE EXPECTED DATA CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL DATA CONTENTS OF THAT REGISTER

6.1.4 PC +2 = TRANSMITTER ERROR PC
REGISTER EXPECTED ACTUAL
16XXXX YYYYYY ZZZZZZ

WHERE 16XXXX IS THE ADDRESS OF THE FAILING TRANSMITTER (TXCSR) REGISTER

WHERE YYYYYY IS THE EXPECTED CONTENTS OF THAT REGISTER

WHERE ZZZZZZ IS THE ACTUAL CONTENTS OF THAT REGISTER

6.1.5 ERROR DESCRIPTIONS
SEE LISTINGS FOR DETAILS OF ERRORS

6.2 ERROR RECOVERY

6.2.1 SW15 =0
IF THE PROGRAM IS RUN WITH SW15 =0 ,NO OPERATOR ACTION IS
REQUIRED TO CONTINUE TESTING

6.2.2 SW15 =1
IF THE PROGRAM IS RUN WITH SW15 =1 ,TO CONTINUE TESTING
AFTER THE PROGRAM HAS HALTED ,PRESS THE PROCESSOR
CONSOLE "CONTINUE SWITCH"

NOTE: THE PC + 2 OF THE "HLT" WILL BE DISPLAYED IN THE DATA LIGHTS

6.2.3 ILLEGAL INTERRUPTS
IF AN INTERRUPT OCCURS TO A VECTOR ADDRESS NOT SELECTED
DURING PROGRAM INITIALIZATION, THE PROGRAM WILL HALT IN
THE TRAPCATCHER. THE ADDRESS AT WHICH THE PROGRAM
HALTS IS 2 GREATER THAN THE ADDRESS TO WHICH THE INTERRUPT
OCCURED. THE PROGRAM MUST BE RESTARTED AT 000200 TO
RECOVER FROM THIS ERROR.

6.2.4 ADDITIONAL TROUBLESHOOTING AIDS EPPCNT; & PASCNT;
CHECK THESE TWO TAG LOCATIONS FOR TOTAL # OF ERRORS AND PASSES RESPECTIVELY.
LOADING 000200 AND RESTARTING WILL CLEAR THESE LOCATIONS.

6.3 END OF PASS ROUTINE

THIS TYPEOUT IS MENTIONED HERE FOR CONVENIENCE
IT IS IN THE FORM:

END OF PASS TAPE Y
16XXXX = DEVICE

WHERE Y IS THE TAPE LOADED

WHERE 16XXXX IS THE DEVICE'S BASE REGISTER ADDRESS

TO INHIBIT THIS TYPEOUT - TURN TELETYPE OFF

7. RESTRICTIONS

7.1 MULTIPLE DEVICES

UP TO 16(10) DEVICES MAY BE TESTED, HOWEVER, THEY
MUST HAVE CONTIGUOUS ADDRESSES AND VECTORS

NOTE: IF ALL DEVICES UNDER TEST HAVE THE SAME INTERRUPT VECTOR
YOU CAN CHANGE "ZERO: ADD 010,BASEIV ;NEXT BLOCK
(VECTORS)" TO "ZERO: ADD 00,BASEIV";
THEREBY THE VECTOP ADDRESSES WILL NOT BE
UPDATED AFTER EACH PASS.

7.2 DISQUALIFYING DEVICES WHEN RUNNING MULTIPLE DEVICES

WHEN RUNNING MULTIPLE DEVICES AN ACTIVE BIT IS SET
FOR EACH DEVICE RUNNING UNDER TEST IE, BIT 0 FOR
DEVICE 0 ,BIT 15 FOR DEVICE 15
TO DISQUALIFY DEVICES:

7.2.1 IF DEVICE 0 IS TO BE DISQUALIFIED ,SIMPLY RESTART PROGRAM WITH SW00 01 AND OMIT THE FIRST DEVICE.

7.2.2 IF HOWEVER, DEVICES 1 THRU 15 OR ANY COMBINATION THEREOF ARE TO BE DISQUALIFIED,...LOAD THE LOCATION OF ACTRFG; OBSERVE THE ACTIVE BITS (ACTIVE 01, NONACTIVE 00) AND DEPOSIT 0 WHERE THOSE DEVICES ARE TO BE DISQUALIFIED

7.2.2.1 TO RESTART...LOAD 000200 IN SWR AND DEPRESS START....
THE PROGRAM WILL CONTINUE WITH THE DEVICE IT WAS IN BEFORE HALTING.

7.2.2.2 OF LOAD 000200 WITH SW00 01 AND DEPRESS START....
ANSWER THE QUESTION 11ST DEVICE 1 ETC.....
.....THE PROGRAM WILL CONTINUE WITH DEVICE 0

7.2.2.3 IF ALL DEVICES ARE DISQUALIFIED BY MISTAKE THE PROGRAM
WILL TYPEOUT AN ERROR MESSAGE.....LOAD & START AT 000200

7.3 CABLE DELAYS

NOTE: EXTERNAL LOOP BACK TESTS ONLY (MODEM CABLE WITH H315 CONNECTOR ON)

7.3.1 TO PROVIDE SUFFICIENT DELAY FOR CLOCK SIGNAL OVER THE CABLE, LOCATION "HOLD:" MUST BE MODIFIED TO ACCOMODATE FOR FASTER MACHINES. PRESENTLY "HOLD:" 020 IS SUFFICIENT TIME ON AN 11/20 MACHINE, IF RUNNING ON AN 11/40 OR AN 11/45 "HOLD:" MUST BE PATCHED TO 40 .

BASICALLY DON'T TRY TO EXCEED 10K TO 12K RATE USING THE EIA DRIVERS

7.4 TO USE THE "XOR" TESTER ,THE BRANCH AROUND THE "XOR"
CODE MUST BE PATCHED TO A "NOP", (SEE LISTINGS FOR DETAILS)

8. DEFAULT PARAMETERS:
1ST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- RXCSR: 160040
VECTOR ADDRESS- DURIV: 770
ARE YOU RUNNING MULTIPLE DEVICES ?- NO MULTD: 0
LAST DEVICE: RECEIVER CONTROL REGISTER ADDRESS- LASTADD: 0
DU PRIORITY LEVEL- LEVEL 5 DUPRT: LEVEL 5
OF SYNC CHARS SELECTED - 2 SYNCNO: 377
IS SEC XMIT JUMPER # 6 IN ?- YES SEXMIT: 377
IS SEC REC JUMPER # 5 IN ?- YES SERFC: 377
IS OPT CLR ENABLE JUMPER # 4 IN ?- YES OPTCLP: 377
DO YOU HAVE THE EXTERNAL MODEM BYPASS JUMPER
CONNECTOR ON (W315)- YES JMRY: 377

9. PROGRAM DESCRIPTION

9.1 THIS PROGRAM PERFORMS THE OFFLINE LOGIC BIT RANGING
OF THE DEVICE
SEE LISTING FOR DETAILS

10. FLOW CHARTS: RECEIVER FLOW,TRANSMITTER FLOW,TRANSMITTER & RECEIVER FLOW

11. LISTINGS

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587      .ENABLE ABS
588
589      ;DU11 DZDUA-D TAPE A
590      ;COPYRIGHT 1973, DIGITAL EQUIPMENT CORP., MAYNARD, MASS. 01754
591
592      ;STARTING PROCEDURE
593      ;LOAD PROGRAM
594      ;PRESS START
595      ;PROGRAM WILL TYPE "DU11 DZDUA-D TAPE A "
596      ;PROGRAM WILL TYPE "R" TO INDICATE THAT TESTING HAS STARTED
597      ;AT THE END OF A PASS, PROGRAM WILL TYPE "END OF PASS TAPE A"
598      ;AND THEN RESUME TESTING
599
600
601      ;SWITCH REGISTER OPTIONS
602
603      100000      SW15=100000      ;=1,HALT ON ERROR
604      040000      SW14=400000      ;=1,LOOP ON CURRENT TEST
605      020000      SW13=200000      ;=1,INHIBIT ERROR TYPEOUT
606      010000      SW12=100000
607      004000      SW11=400000      ;=1,INHIBIT ITERATIONS
608      002000      SW10=200000      ;=1,ESCAPE TO NEXT TEST ON ERROR
609      001000      SW09=100000      ;=1,LOOP WITH CURRENT DATA
610      000400      SW08=400000      ;=1,LOOP ON ERROR
611      000100      SW06=100000
612      000040      SW05=400000
613      000020      SW04=200000
614      000010      SW03=100000
615      000004      SW02=400000      ;LOCK ON TEST SELECT
616      000002      SW01=200000      ;RESTART PROGRAM AT SELECTED TEST
617      000001      SW00=100000      ;PESELECT VECTOR AND CONTROL REGISTER
618                                      ;ADDRESS AFTER PROGRAM RESTART
619

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620
621      ;REGISTER DEFINITIONS
622
623      000000      R0=00      ;GENERAL REGISTER
624      000001      R1=01      ;GENERAL REGISTER
625      000002      R2=02      ;GENERAL REGISTER
626      000003      R3=03      ;GENERAL REGISTER
627      000004      R4=04      ;GENERAL REGISTER
628      000005      R5=05      ;GENERAL REGISTER
629      000006      SP=06      ;PROCESSOR STACK POINTER
630      000007      PC=07      ;PROGRAM COUNTER
631
632      ;LOCATION EQUIVALENCES
633
634      177570      DSWR=177570      ;HARDWARE SWITCH REGISTER LOC.
635      177570      DLIGHTS=177570      ;HARDWARE DISPLAY REGISTER LOC.
636      177776      PS=177776      ;PROCESSOR STATUS WORD
637      001100      STACK=1100      ;START OF PROCESSOR STACK
638
639      ;INSTRUCTION DEFINITIONS
640
641      025746      PUSH1SP=5746      ;DECREMENT PROCESSOR STACK 1 WORD =TST -(SP)
642      025726      POP1SP=5726      ;INCREMENT PROCESSOR STACK 1 WORD =TST (SP)+
643      010046      PUSHRO=10046      ;SAVE R0 ON STACK =MOV R0,-(SP)
644      012600      POPRO=12600      ;RESTORE R0 FROM STACK =MOV (SP)+,R0
645      024646      PUSH2SP=24646      ;DECREMENT STACK TWICE =CMP -(SP),-(SP)
646      022626      POP2SP=22626      ;INCREMENT STACK TWICE =CMP (SP)+,(SP)+
647      .FQUIV FMT,HLT ;BASIC DEFINITION OF ERROR CALL
648
649
650      100000      BIT15=100000
651      040000      BIT14=400000
652      020000      BIT13=200000
653      010000      BIT12=100000
654      004000      BIT11=400000
655      002000      BIT10=200000
656      001000      BIT9=100000
657      000400      BIT8=400000
658      000200      BIT7=200000
659      000100      BIT6=100000
660      000040      BIT5=400000
661      000020      BIT4=200000
662      000010      BIT3=100000
663      000004      BIT2=400000
664      000002      BIT1=200000
665      000001      BIT0=100000
666
667      ;PROCESSOR LEVELS
668      000340      LFVEL7=340
669      000300      LEVEL6=300
670      000240      LFVEL5=240
671      000200      LEVEL4=200
672      000140      LFVEL3=140
673      000100      LFVEL2=100
674      000040      LEVEL1=040
675      000000      LFVEL0=000

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676      ;REGISTER DEFINITIONS
677      ;RXCSR BIT DEFINITIONS
678      10000000  DSC=BIT15      ;DATA SET CHANGE
679      04000000  RING=BIT14     ;RING
680      02000000  CTS=BIT13      ;CLP TO SEND
681      01000000  CARDET=BIT12   ;CARRIER DETECT
682      00400000  RECACT=BIT11   ;REC ACTIVE
683      00200000  SRD=BIT10      ;SEC REC DATA
684      00100000  DSP=BIT9       ;DATA SFT RDY
685      00040000  STPSYN=BIT8     ;STRIP SYNC
686      00020000  RXDONE=BIT7    ;REC DONE
687      00010000  RINTEN=BIT6    ;REC INTR ENABLE
688      00004000  DSINTE=BIT5    ;DSC INTR ENABLE
689      00002000  SYN SCH=BIT4    ;SYNC SEARCH
690      00001000  STD=BIT3       ;SEC XMIT DATA
691      00000400  RTS=BIT2       ;PFO TO SEND
692      00000200  DTR=BIT1      ;DATA TERM RDY
693      00000100  VOID=BIT0
694      ;RXDBUF BIT DEFINITIONS
695      10000000  RXERR=BIT15     ;REC ERROR
696      04000000  OVPRUN=BIT14    ;OVERRUN
697      02000000  FRMERR=BIT13    ;FRAME ERROR
698      01000000  PAPER=BIT12     ;PARITY ERROR
699      ;PAPCSR BIT DEFINITIONS
700      00100000  PAREN=BIT9      ;PARITY ENABLE
701      00040000  EVPAR=BIT8     ;EVEN PARITY SENSE
702      ;PARCSR WRD DEFINITIONS
703      03000000  SYNINT=3000000  ;SYNC EXTERNAL MODE
704      02000000  SYNEXT=2000000  ;SYNC INTERNAL MODE
705      00000000  ISYMOD=0        ;ISOC MODE
706      00000000  FIVE=0         ;WORD LENGTH 5 BITS
707      00200000  SIX=2000000    ;WORD LENGTH 6 BITS
708      00400000  SEVEN=4000000  ;WORD LENGTH 7 BITS
709      00600000  EIGHT=6000000  ;WORD LENGTH 8 BITS
710      00000000  NOPAR=0        ;NO PARITY
711      00100000  ODDPAR=1000000 ;ODD PARITY
712      00140000  EVLPAR=1400000 ;EVEN PARITY
713      ;TXCSR BIT DEFINITIONS
714      10000000  DNA=BIT15       ;DATA NOT AVAILABLE
715      04000000  MTDATA=BIT14    ;MAINT DATA
716      02000000  CLK=BIT13       ;CLK
717      00200000  BITW=BIT10      ;BIT WINDOW
718      00040000  MRESET=BIT8     ;MASTER RESET
719      00020000  TXDONE=BIT7     ;XMIT DONE
720      00010000  TXINTE=BIT6     ;XMIT INTR ENABLE
721      00004000  DNAINTF=BIT5    ;DNA INTR ENAB
722      00002000  SEND=BIT4       ;SEND
723      00001000  HDXFN=BIT3      ;HDX/FDX
724      00000100  BPFAR=BIT2     ;BREAK
725      ;TXCSR WRD DEFINITIONS
726      00000000  USER=0         ;USER MODE
727      00400000  MINT=4000000   ;MAINT INT MODE
728      01000000  NEXTE=1000000  ;MAINT EXT MODE
729      01400000  SYSTST=1400000 ;SYSTEM TEST MODE
730      ;TRAPCATCHER FOR ILLEGAL INTERRUPTS

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731                                ;STANDARD INTERRUPT VECTORS
732
733
734                                .B24
735      000024 015152                .PFAIL                ;POWER FAIL HANDLER
736      000026 000340                340                ;SERVICE AT LEVEL 7
737      000030 014702                .HLT                 ;ERROR HANDLER
738      000032 000340                340                ;SERVICE AT LEVEL 7
739      000034 014650                .TRPSRV              ;GENERAL HANDLER DISPATCH SERVICE
740      000036 000340                340                ;SERVICE AT LEVEL 7
741
742                                ;SOFTWARE SWITCH REGISTER
743
744                                .B174
745      000174 000000                DISPREG: .WORD 0      ;SOFTWARE DISPLAY REG.
746      000176 000000                SWREG:  .WORD 0      ;SOFTWARE SWITCH REGISTER
747      000200 000167 001054                JMP      .START ;GO TO START OF PROGRAM
748
749
750
751                                .B1100
752
753                                ;INDIRECT POINTERS
754
755      001100 177570                SWR:      177570      ;SWITCH REGISTER POINTER
756      001102 177570                LIGHTS: 177570      ;DISPLAY REGISTER POINTER
757      001104 177560                TKCSP:   177560      ;TELETYPE KEYBOARD CONTROL REGISTER
758      001106 177562                TKDBR:   177562      ;TELETYPE KEYBOARD DATA BUFFER
759      001110 177564                TPCSR:   177564      ;TELEPRINTER CONTROL REGISTER
760      001112 177566                TPDBR:   177566      ;TELEPRINTER DATA BUFFER
761
762                                ;PROGRAM CONTROL PARAMETERS
763
764      001114 000000                RTPN:    0           ;SCOPE ADDRESS FOR LOOP ON TEST
765      001116 000000                NFXT:    0           ;ADDRESS OF NFXT TEST TO BE EXECUTED
766      001120 000000                LOCK:    0           ;ADDRESS FOR LOCK ON CURRENT DATA
767      001122 000000                ICOUNT:  0           ;NUMBER OF ITERATIONS THAT CURRENT TEST WILL BE EXECUTED
768      001124 000000                LPCNT:   0           ;NUMBER OF ITERATIONS COMPLETED
769      001126 000000                TSTNO:   0           ;NUMBER OF TEST IN PROGRESS
770      001130 000000                PASCNT:  0           ;NUMBER OF PASSES COMPLETED
771      001132 000000                ERRCNT:  0           ;TOTAL NUMBER OF ERRORS
772      001134 000000                LSTEP:   0           ;PC OF LAST ERROR CALL
773
774                                ;PROGRAM VARIABLES
775
776      001136 000020                HOLD:    20          ;TEMPORARY STORAGE=DELAY TIME FOR CABLES
777      001140 000000                SHIFT:   0           ;TEMPORARY STORAGE= # OF SHIFTS PER CHAR
778      001142 000000                COUNT:   0           ;TEMPORARY STORAGE= # OF TIMES A CHAR WILL BE SENT
779      001144 000000                TFMP1:   0           ;TEMPORARY STORAGE
780      001146 000000                TFMP2:   0           ;TEMPORARY STORAGE
781      001150 000000                TFMP3:   0           ;TEMPORARY STORAGE
782      001152 000000                TEMP4:   0           ;TEMPORARY STORAGE
783      001154 000000                TEMP5:   0           ;TEMPORARY STORAGE
784      001156 000000                SAVPR:   0           ;R0 STORAGE
785      001160 000000                SAVR1:   0           ;R1 STORAGE
786      001162 000000                SAVR2:   0           ;R2 STORAGE

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DZDUAD,P11 24-AUG-76 00:00

787 001164 000000
788 001166 000000
789 001170 000000
790 001172 000000
791 001174 000000

SAVR3: 0
SAVR4: 0
SAVR5: 0
SAVSP: 0
SAVPC: 0

;R3 STORAGE
;R4 STORAGE
;R5 STORAGE
;STACK POINTER STORAGE
;PROGRAM COUNTER STORAGE

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792                                     ;PROGRAM CONVEPSATIONAL PARAMETERS
793 001176 377 SYNCNO: .BYTE 377 ;# OF SYNC CHARS REQ'D FOR SYNC'ZATION
794 001177 377 SEXMIT: .BYTE 377 ;SEC XMIT JUMPER "IN"
795 001200 377 SEPEC: .BYTE 377 ;SEC PEC JUMPER "IN"
796 001201 377 OPTCLR: .BYTE 377 ;OPTIONAL JUMPER CLR "IN"
797 001202 000 MULTD: .BYTE 0 ;NO MULTIPLE DEVICE FLAG
798 001203 377 JHPRY: .BYTE 377 ;EXTERNAL MODEM BYPASS JUMPER "IN"
799 .EVEN
800
801                                     ;PROGRAM MULTIPLE DEVICE PARAMETERS
802 001204 000000 BASEADD: 0 ;PROG CONTROLLED 1ST DEVICE ADDR
803 001206 000000 KFEPADD: 0 ;SAVED 1ST DEVICE ADDR
804 001210 000000 LASTADD: 0 ;LAST DEVICE RXCSR ADDR
805 001212 000000 BASFIV: 0 ;PROG CONTROLLED IV
806 001214 000000 KEEPIV: 0 ;SAVED INTR VECTOR
807 001216 000000 ACTHEG: 0 ;ACTIVE REGISTER,,,MODIFY THIS
808 ;LOCATION TO DISQUALIFY OR QUALIFY
809 ;DEVICES (1= RUN,,,0= DON'T RUN)
810 001220 000000 ROTADD: 0 ;ROTATING POINTER FOR ACTREG,,POINTS
811 ;TO DEVICE PRESENTLY UNDER TEST WHEN RUNNING MULTIPLE DE
812
813                                     ;PROGRAM CONTROL FLAGS
814
815 001222 000 INIFLG: .BYTE 0 ;PROGRAM INITIALIZATION FLAG
816 001223 000 STFLG: .BYTE 0 ;TEST START FLAG
817 001224 000 ERPLG: .BYTE 0 ;ERROR OCCURED FLAG
818 001225 000 LOKFLG: .BYTE 0 ;LOCK ON CURRENT TEST FLAG
819
820                                     ;DEFINITIONS FOR TRAP SUBROUTINE CALLS
821 ;POINTERS TO SUBROUTINES CAN BE FOUND
822 ;IN THE TABLE IMMEDIATLY FOLLOWING THE DEFINITIONS
823
824 001226 .TRPTAB:
825 ;.....
826 ;.....
827 104400 SCOPE=TRAP+0 ;CALL TO SCOPE LOOP AND ITERATION HANDLER
828 001226 013434 .SCOPE
829 104401 SCOP1=TRAP+1 ;CALL TO LOOP ON CURRENT DATA HANDLER
830 001230 013620 .SCOP1
831 104402 TYPE=TRAP+2 ;CALL TO TELETYPE OUTPUT ROUTINE
832 001232 013640 .TYPE
833 104403 INSTR=TRAP+3 ;CALL TO ASCII STRING INPUT ROUTINE
834 001234 013700 .INSTR
835 104404 INSTRP=TRAP+4 ;CALL TO INPUT ERROR HANDLER
836 001236 014016 .INSTRP
837 104405 PARAM=TRAP+5 ;CALL TO NUMERICAL DATA INPUT ROUTINE
838 001240 014050 .PARAM
839 104406 SAV05=TRAP+6 ;CALL TO REGISTER SAVE ROUTINE
840 001242 014264 .SAV05
841 104407 RES05=TRAP+7 ;CALL TO REGISTER RESTORE ROUTINE
842 001244 014324 .RES05
843 104410 CONVRT=TRAP+10 ;CALL TO DATA OUTPUT ROUTINE
844 001246 014356 .CONVRT
845 104411 CNVPT=TRAP+11 ;CALL TO DATA OUTPUT ROUTINE WITHOUT CR/LF
846 001250 014362 .CNVRT
847 104412 SETFLG=TRAP+12 ;CALL TO FLAG SET ROUTINE

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048	001252	014602			.SETFLG			
049		104413				CHKSWR=TPAP+13	;CALL TO ALLOW SWREG TO BE LOADED FROM TTY	
050	001254	015316			.CKSWP			
051		104414				CNTLU=TPAP+14	;CALL TO ALLOW LOADING OF SWREG FROM TTY	
052	001256	015372			.CNTLU			
053						;	;	
054						;	;	
055								
056						;PROGRAM INITIALIZATION		
057						;LOCK OUT INTERRUPTS		
058						;SET UP PROCESSOR STACK		
059						;SET UP POWER FAIL VECTOR		
060						;CLEAR PROGRAM CONTROL FLAGS AND COUNTS		
061						;TYPE TITLE MESSAGE		
062								
063	001260	012767	000340	176510	.START:	MOV	0340,PS	;LOCK OUT INTERRUPTS
064	001266	012706	001100			MOV	0STACK,SP	;SET UP STACK
065	001272	012737	015152	000024		MOV	0.PFAIL,0024	;SET UP POWER FAIL VECTOR
066	001300	005067	177629			CLP	LPCNT	;CLEAR # OF ITERATION COMPLETED LOCATION
067	001304	105067	177713			CLRR	STFLG	;CLEAR START FLAG
068	001310	005067	177614			CLP	PASCNT	;CLEAR PASS COUNT
069	001314	105067	177704			CLRR	ERRFLG	;CLEAR ERROR FLAG
070	001320	005067	177606			CLP	ERRCNT	;CLEAR ERROR COUNT
071	001324	005067	177604			CLP	LSTERR	;CLEAR LAST ERROR POINTER
072	001330	012767	000001	177570		MOV	01,TSTNO	;SET UP FOR TEST 1
073	001336	012767	001260	177550		MOV	0,START,RTPN	;SET UP FOR POWER FAIL BEFORE
074								;TESTING STARTS
075	001344	125767	177652			TSTR	INIFLG	;HAS INITIALIZATION BEEN PERFORMED
076	001350	001004				BNE	ONCE	
077	001352	104402	015472			TYPE	,MTITLE	;TYPE TITLE MESSAGE
078	001356	105167	177640			COMB	INIFLG	;IF NOT SET FLAG AND DO
079	001362	012767	177570	177510	ONCE:	MOV	0DSWP,SWP	;RELOAD HARDWARE SWITCH REGISTER INTO POINTER
080	001370	012767	177570	177504		MOV	0DLIGHTS,LIGHTS	;RELOAD HARDWARE DISPLAY REGISTER INTO POINTER
081	001376	013746	000006			MOV	006,-(SP)	;SAVE VECTORS
082	001402	013746	000004			MOV	004,-(SP)	
083	001406	012737	001426	000004		MOV	0648,004	;SET UP FOR TIMEOUT
084	001414	022777	177777	177456		CMP	0-1,0SWR	;REFERENCE HARDWARE SWITCH REGISTER
085	001422	001402				HEQ	658	
086	001424	000407				RR	668	
087	001426	022626			648:	CMP	(SP)+,(SP)+	;ADJUST STACK
088	001430	012767	000176	177442	658:	MOV	0SWPEG,SWR	;POINT TO SOFTWARE SWITCH REG
089	001436	012767	000174	177436		MOV	0DISPEG,LIGHTS	;POINT TO SOFT DISPLAY REG
090	001444	012637	000004		668:	MOV	(SP)+,004	;RESTORE VECTORS
091	001450	012637	000006			MOV	(SP)+,006	
092	001454	005737	000042			TST	0042	;UNDER MONITOR
093	001460	001005				BNE	678	
094	001462	022767	000176	177410		CMP	0SWREG,SWR	;IS SWREG USED
095	001470	001001				BNE	678	
096	001472	104414				CNTLU		
097	001474	032777	000001	177376	678:	BIT	0SW00,0SWR	;PESELECT VECTOR & CONTROL REG?
098	001502	001002				BNE	18	
099	001504	000167	000446			JMP	,BEGIN	
900	001510	012702	000300		18:	MOV	0300,R0	;RESTORE VECTOR AREA TO TRAPCATCHER
901	001514	012701	000302			MOV	0302,R1	;START AT LOCATION 300
902	001520	012702	000004			MOV	04,R2	
903	001524	010110			28:	MOV	R1,(R0)	

904	001526	005011			CLR	(R1)	
905	001530	060200			ADD	R2,R0	
906	001532	060201			AND	R2,R1	
907	001534	022701	001000		CMP	01000,R1	;END AT LOCATION 776
908	001540	002771			BLT	28	
909	001542	104403			INSTR		;OUTPUT MESSAGE & GET INPUT STRING
910	001544	015546			MREGAD		;MESSAGE
911	001546	104405			PARAM		;CONVERT STRING
912	001550	160000			160000		;LOW LIMIT
913	001552	167776			167776		;HIGH LIMIT
914	001554	017402			DUBASE		;STORE AT THIS LOCATION
915	001556	001			.PYTE	1	;MASK
916	001557	001			.PYTE	1	;HOW MANY TIMES + 2
917	001560	016767	015616	177420	MOV	DUBASE,KEPPADD	;SAVE
918	001566	004767	015456		JSR	PC,DUADDR	
919	001572	016767	177410	177404	MOV	KEPPADD,BASFADD	;RESTORE FOR ROTATION
920	001600	104403			INSTR		;OUTPUT MESSAGE & GET INPUT STRING
921	001602	015524			MVECTO		;MESSAGE
922	001604	104405			PARAM		;CONVERT STRING
923	001606	000300			300		;LOW LIMIT
924	001610	000776			776		;HIGH LIMIT
925	001612	017724			DURIV		;STORE AT THIS LOCATION
926	001614	001			.PYTE	1	;MASK
927	001615	004			.PYTE	4	;HOW MANY TIMES + 2
928	001616	016767	016102	177370	MOV	DURIV,KEEPIV	;SAVE
929	001624	016767	016074	177360	MOV	DURIV,BASEIV	;SET UP FOR ROTATION
930	001632	104403			INSTR		;OUTPUT MESSAGE & GET INPUT STRING
931	001634	015627			MMULT		;MESSAGE
932	001636	104412			SFTFLG		;SET FLAG BASED UPON INPUT STRING
933	001640	001202			MULTD		;THIS FLAG
934	001642	105767	177334		TSTR	MULTD	;ARE THERE MULTIPLE DEVICES
935							;ON THE SYSTEM ?
936	001646	100406			BMI	RBB	;YES,ASK NEXT QUESTION
937	001650	005067	177342		CLR	ACTREG	
938	001654	005067	177340		CLR	ROTADD	
939	001660	000167	000140		JMP	OUTMUL	;JUMP AROUND NEXT QUESTION
940	001664				RBB:		
941	001664	104403			INSTR		;OUTPUT MESSAGE & GET INPUT STRING
942	001666	015706			MLASTD		;MESSAGE
943	001670	104405			PARAM		;CONVERT STRING
944	001672	160000			160000		;LOW LIMIT
945	001674	167776			167776		;HIGH LIMIT
946	001676	001210			LASTADD		;STORE AT THIS LOCATION
947	001700	001			.PYTE	1	;MASK
948	001701	001			.PYTE	1	;HOW MANY TIMES + 2
949							
950	001702	012767	000001	177310	18:	MOV	01,ROTADD ;SET UP POINTER
951	001710	005067	177302		CLR	ACTREG	;CLR ACTIVE REGISTER
952	001714	0056767	177300	177274	28:	RIS	ROTADD,ACTREG ;MAKE THIS DEVICE ACTIVE
953	001722	000241			CLC		
954	001724	006167	177270		ROL	ROTADD	;SET UP POINTER
955	001730	103421			RCS	38	;ARE YOU OUT OF RANGE ?
956	001732	002767	000010	177244	ADD	010,BASEADD	;SET UP BASE ADDRESS
957	001740	002767	177244	177236	CMP	LASTADD,BASEADD	;IS THIS THE LAST DEVICE ?
958	001746	101362			RHI	28	;NO DO IT AGAIN
959	001750	0056767	177244	177240	RIS	ROTADD,ACTREG	;THIS ASSUMES THAT THERE ARE AT

960										;LEAST TWO DEVICES WHEN YOU ANSWER YES TO
961										;MULTIPLE DEVICE QUESTION
962	001756	012767	000001	177234	48:	MOV				01,ROTADD ;SET UP FOR LATER USE IN END OF PASS ROUTINE
963	001764	016767	177216	177212		MOV				KEEPADD,BASEADD ;DITTO
964	001772	000414				BP				OUTMUL ;CONTINUE QUESTIONS
965	001774	016767	177206	177202	38:	MOV				KFEPADD,BASEADD ;RESTORE
966	002002	104403				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
967	002004	016471				MFRNGE				;MESSAGE
968	002006	104425				PARAM				;CONVERT STRING
969	002010	103000				160000				;LOW LIMIT
970	002012	107776				167776				;HIGH LIMIT
971	002014	001210				LASTADD				;STORE AT THIS LOCATION
972	002016	001			.BYTE	1				;MASK
973	002017	001			.BYTE	1				;HOW MANY TIMES + 2
974	002020	000167	177656			JMP	18			;DO IT AGAIN
975	002024				OUTMUL;					
976	002024	104423				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
977	002026	016355				MFLVEL				;MESSAGE
978	002030	104405				PARAM				;CONVERT STRING
979	002032	000004				4				;LOW LIMIT
980	002034	000007				7				;HIGH LIMIT
981	002036	017244				DUPRT				;STORE AT THIS LOCATION
982	002040	001			.BYTE	0				;MASK
983	002041	001			.BYTE	1				;HOW MANY TIMES + 2
984	002042	004767	015126			JSP	PC,DULEV			
985										;COMPARE THE FIRST CHARACTER IN THE TELETYPE INPUT
986										;BUFFER TO THE CHARACTERS "1" AND "2".
987										;IF THE CHARACTER IS "1" CLEAR THE FLAG
988										;IF THE CHARACTER IS "2" SET THE FLAG
989	002046				AAA:					
990	002046	104423				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
991	002050	016472				MSYNC				;MESSAGE
992	002052	122767	000001	014754	38:	CMPR	0'1,INBUF			;IS IT "1" ?
993	002060	001003				BNE	18			
994	002062	105267	177110			CLRB	SYNCR0			;NOO
995	002066	000412				HR	48			
996	002070	122767	000062	014736	18:	CMPR	0'2,INBUF			;IS IT "2" ?
997	002076	001004				RNE	28			
998	002100	112767	177777	177070		MOVR	0-1,SYNCR0			;377
999	002106	000402				RR	48			
1000	002110	104404			78:	INSTR				;RETRY
1001	002112	000757				HK	38			
1002	002114	000240			48:	NOP				
1003	002116	104403				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
1004	002120	016450				MWIRE6				;MESSAGE
1005	002122	104412				SETFLG				;SET FLAG BASED UPON INPUT STRING
1006	002124	001177				SFXMIT				;THIS FLAG
1007	002126	104403				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
1008	002130	016516				MWIRE5				;MESSAGE
1009	002132	104412				SETFLG				;SET FLAG BASED UPON INPUT STRING
1010	002134	001200				SFREC				;THIS FLAG
1011	002136	104403				INSTR				;OUTPUT MESSAGE & GET INPUT STRING
1012	002140	016563				MWIRE4				;MESSAGE
1013	002142	104412		</						

H2

1072	002420	012737	000006	000004	658:	MOV	06,004	;RESTORE TRAPCATCHER
1073	002426	012737	000000	000006		MOV	00,006	;
1074	002434	104400				SCOPE		
1075						;;THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS		
1076						;;		
1077	002436	012767	000002	176462	TST2:	MOV	02,TSTNO	;SAVE THIS
1078	002444	012767	002524	176444		MOV	0TST3,NEXT	;GO TO THIS TEST WHEN THRU
1079	002452	012737	017642	000004		MOV	0TRPREG,004	;SETUP TRAPCATCHER
1080	002460	012737	000340	000006		MOV	0LEVEL7,006	;
1081	002466	105277	015217			INCB	0PXDRUF	;TEST THIS REG
1082	002472	000401				BR	648	;IF OK JMP AROUND HLT
1083	002474	104000				HLT		;CHECK DEVICE REG ADDRESSES
1084	002476	105277	015204		648:	INCB	0HXRDBUF	;TEST UPPER BYTE THIS REGISTER
1085	002502	000401				BR	658	;IF OK JMP AROUND HLT
1086	002504	104000				HLT		;CHECK DEVICE REG ADDRESSES
1087	002506	012737	000006	000004	656:	MOV	06,004	;RESTORE TRAPCATCHER
1088	002514	012737	000000	000006		MOV	00,006	;
1089	002522	104400				SCOPE		
1090						;;THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS		
1091						;;		
1092	002524	012767	000003	176374	TST3:	MOV	03,TSTNO	;SAVE THIS
1093	002532	012767	002612	176356		MOV	0TST4,NEXT	;GO TO THIS TEST WHEN THRU
1094	002540	012737	017642	000004		MOV	0TRPREG,004	;SETUP TRAPCATCHER
1095	002546	012737	000340	000006		MOV	0LEVEL7,006	;
1096	002554	105277	015130			INCB	0PAPCSR	;TEST THIS REG
1097	002560	000401				BR	648	;IF OK JMP AROUND HLT
1098	002562	104000				HLT		;CHECK DEVICE REG ADDRESSES
1099	002564	105277	015122		648:	INCB	0HPARCSR	;TEST UPPER BYTE THIS REGISTER
1100	002570	000401				BR	658	;IF OK JMP AROUND HLT
1101	002572	104000				HLT		;CHECK DEVICE REG ADDRESSES
1102	002574	012737	000006	000004	658:	MOV	06,004	;RESTORE TRAPCATCHER
1103	002602	012737	000000	000006		MOV	00,006	;
1104	002610	104400				SCOPE		
1105						;;THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS		
1106						;;		
1107	002612	012767	000004	176306	TST4:	MOV	04,TSTNO	;SAVE THIS
1108	002620	012767	002700	176270		MOV	0TST5,NEXT	;GO TO THIS TEST WHEN THRU
1109	002626	012737	017642	000004		MOV	0TRPREG,004	;SETUP TRAPCATCHER
1110	002634	012737	000340	000006		MOV	0LEVEL7,006	;
1111	002642	105277	015046			INCB	0TXCSR	;TEST THIS REG
1112	002646	000401				BR	648	;IF OK JMP AROUND HLT
1113	002650	104000				HLT		;CHECK DEVICE REG ADDRESSES
1114	002652	105277	015040		648:	INCB	0HTXCSR	;TEST UPPER BYTE THIS REGISTER
1115	002656	000401				BR	658	;IF OK JMP AROUND HLT
1116	002660	104000				HLT		;CHECK DEVICE REG ADDRESSES
1117	002662	012737	000006	000004	658:	MOV	06,004	;RESTORE TRAPCATCHER
1118	002670	012737	000000	000006		MOV	00,006	;
1119	002676	104400				SCOPE		
1120						;;THIS TEST PROVES EXISTANCE OF DEVICE REGISTERS		
1121						;;		
1122	002700	012767	000005	176220	TST5:	MOV	05,TSTNO	;SAVE THIS
1123	002706	012767	002706	176202		MOV	0TST6,NEXT	;GO TO THIS TEST WHEN THRU
1124	002714	012737	017642	000004		MOV	0TRPREG,004	;SETUP TRAPCATCHER
1125	002722	012737	000340	000006		MOV	0LEVEL7,006	;
1126	002730	105277	014764			INCB	0TXDBUF	;TEST THIS REG
1127	002734	000401				BR	648	;IF OK JMP AROUND HLT

1120	002736	104000				HLT			;CHECK DEVICE REG ADDRESSES
1129	002740	105277	014756		648:	INCR	0HTXDRUF		;TEST UPPER BYTE THIS REGISTER
1130	002744	000401				RR	658		;IF OF JMP AROUND HLT
1131	002746	104000				HLT			;CHECK DEVICE REG ADDRESSES
1132	002750	012737	000006	000004	658:	MOV	06,004		;RESTORE TRAPCATCHER
1133	002756	012737	000000	000006		MOV	00,006		
1134	002764	104000				SCOPE			
1135						;;BUS DRIVER TEST			
1136						;;			
1137	002766	012767	000006	176132	TST6:	MOV	06,TSTNO		;SAVE THIS
1138	002774	012767	003016	176114		MOV	0TST7,NEXT		;GO TO THIS TEST WHEN THRU
1139	003002	022777	177777	014710		CMP	0177777,0TXDBUF		
1140	003010	001401				BEQ	004		
1141	003012	104000				HLT			;READING TXDBUF SHOULD BE ALL 1'S
1142	003014	104000				SCOPE			
1143						;;THIS TEST PERFORMS MASTER RESET TESTING &			
1144						;;TESTING OF READ/WRITE BIT DTR			
1145						;;			
1146	003016	012767	000007	176102	TST7:	MOV	07,TSTNO		;SAVE THIS
1147	003024	012767	003146	176064		MOV	0TST8,NEXT		;GO TO THIS TEST WHEN THRU
1148	003032	052777	000002	014600		BIS	0DTR,0PXCSP		;SET THIS BIT
1149	003040	032777	000002	014632		BIT	0DTR,0PXCSP		;TEST THIS BIT
1150	003046	001001				BVE	648		;BR IF "1"
1151	003050	104000				HLT			;THIS BIT SHOULD BE SET
1152	003052				648:				
1153	003052	042777	000002	014620		RIC	0DTR,0PXCSP		;CLR THIS BIT
1154	003060	032777	000002	014612		BIT	0DTR,0PXCSP		;TEST THIS BIT
1155	003066	001401				BEQ	658		;BR IF "0"
1156	003070	104000				HLT			;THIS BIT SHOULD BE CLR
1157	003072				658:				
1158						;;NOW SET THIS BIT			
1159	003072	052777	000002	014600		RIS	0DTR,0PXCSP		
1160	003100	052777	000400	014606		RIS	0MWFRT,0TXCSR		;MASTER RESET
1161						;;CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER			
1162						;;			
1163	003106	105767	176067			TSTP	0PTCLR		;TEST FLAG
1164	003112	100006				RPL	18		;OPTIONAL CLR JUMPER IS NOT IN
1165	003114	032777	000002	014556		BIT	0DTR,0PXCSP		;TEST THIS BIT
1166	003122	001401				BEQ	668		;BR IF "0"
1167	003124	104000				HLT			;CHECK OUT MASTER RESET LOGIC
1168	003126				668:				
1169	003126	000405				RR	28		;JMP AROUND
1170	003130	032777	000002	014542	18:	BIT	0DTR,0PXCSP		;TEST THIS BIT
1171	003136	001001				RNE	678		;BR IF "1"
1172	003140	104000				HLT			;CHECK OUT OPTIONAL CLR JUMPER
1173	003142				678:				
1174	003142	000240			28:	NOP			
1175	003144	104000				SCOPE			
1176						;;THIS TEST PERFORMS MASTER RESET TESTING &			
1177						;;TESTING OF READ/WRITE BIT RTS			
1178						;;			
1179	003146	012767	000010	175752	TST8:	MOV	08,TSTNO		;SAVE THIS
1180	003154	012767	003276	175734		MOV	0TST9,NEXT		;GO TO THIS TEST WHEN THRU
1181	003162	052777	000004	014510		BIS	0RTS,0PXCSP		;SET THIS BIT
1182	003170	032777	000004	014502		BIT	0RTS,0PXCSP		;TEST THIS BIT
1183	003176	001001				BVE	648		;BR IF "1"

1104	003200	104000				HLT		;THIS BIT SHOULD BE SET
1105	003202				648:			
1106	003202	042777	000004	014470		BIC	0PTS,0RXCSR	;CLR THIS BIT
1107	003210	032777	000004	014462		BIT	0PTS,0RXCSR	;TEST THIS BIT
1108	003216	001401				BEQ	658	;BR IF "0"
1109	003220	104000				HLT		;THIS BIT SHOULD BE CLR
1190	003222				658:			
1191								;NOW SET THIS BIT
1192	003222	052777	000004	014450		BIS	0PTS,0RXCSR	
1193	003230	052777	000400	014456		BIS	0MRESET,0TXCSR	;MASTER RESET
1194								;CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
1195								;;
1196	003236	105767	175737			TSTB	OPTCLR	;TEST FLAG
1197	003242	100006				BPL	18	;OPTIONAL CLR JUMPER IS NOT IN
1198	003244	032777	000004	014426		BIT	0PTS,0RXCSR	;TEST THIS BIT
1199	003252	001401				BEQ	668	;BR IF "0"
1200	003254	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1201	003256				668:			
1202	003256	000405				BR	28	;JMP AROUND
1203	003260	032777	000004	014412	18:	BIT	0PTS,0RXCSR	;TEST THIS BIT
1204	003266	001001				BNE	678	;BR IF "1"
1205	003270	104000				HLT		;CHECK OUT OPTIONAL CLR JUMPER
1206	003272				678:			
1207	003272	000240			28:			
1208	003274	104400						
1209								NOF
1210								SCOPE
1211								;THIS TEST PERFORMS MASTER RESET TESTING &
1212								;TESTING OF READ/WRITE BIT STD
1213								;;
1214	003276	012767	000011	175622	TST9:	MOV	09,TSTNO	;SAVE THIS
1215	003304	012767	003426	175604		MOV	0TST10,NEXT	;GO TO THIS TEST WHEN THRU
1216	003312	052777	000010	014360		BIS	0STD,0RXCSR	;SET THIS BIT
1217	003320	032777	000010	014352		BIT	0STD,0RXCSR	;TEST THIS BIT
1218	003326	001001				BNE	648	;BR IF "1"
1219	003330	104000				HLT		;THIS BIT SHOULD BE SET
1220	003332				648:			
1221	003332	042777	000010	014340		BIC	0STD,0RXCSR	;CLR THIS BIT
1222	003340	032777	000010	014332		BIT	0STD,0RXCSR	;TEST THIS BIT
1223	003346	001401				BEQ	658	;BR IF "0"
1224	003350	104000				HLT		;THIS BIT SHOULD BE CLR
1225	003352				658:			
1226	003352	052777	000010	014320				;NOW SET THIS BIT
1227	003360	052777	000400	014326		BIS	0STD,0RXCSR	
1228						BIS	0MRESET,0TXCSR	;MASTER RESET
1229								;CHECK EXISTANCE OF OPTIONAL CLEAR JUMPER
1230								;;
1231	003366	105767	175627			TSTR	OPTCLR	;TEST FLAG
1232	003372	100006				HPL	18	;OPTIONAL CLR JUMPER IS NOT IN
1233	003374	032777	000010	014276		BIT	0STD,0RXCSR	;TEST THIS BIT
1234	003402	001401				BEQ	668	;BR IF "0"
1235	003404	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1236	003406				668:			
1237	003406	000405				BR	28	;JMP AROUND
1238	003410	032777	000010	014262	18:	BIT	0STD,0RXCSR	;TEST THIS BIT
1239	003416	001001				BNE	678	;BR IF "1"
1240	003420	104000				HLT		;CHECK OUT OPTIONAL CLR JUMPER
1241	003422				678:			

1240	003422	000240			28:	NOP		
1241	003424	104400				SCOPE		
1242						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1243						;;TESTING OF READ/WRITE BIT SYNSCH		
1244						;;		
1245	003426	012767	000012	175472	TST10:	MOV	010,TSTNO	;SAVE THIS
1246	003434	012767	003532	175454		MOV	0TST11,NEXT	;GO TO THIS TEST WHEN THRU
1247	003442	052777	000020	014230		BIS	0SYNSCH,0PXCSP	;SET THIS BIT
1248	003450	032777	000020	014222		HIT	0SYNSCH,0PXCSP	;TEST THIS BIT
1249	003456	001001				RNE	048	;BR IF "1"
1250	003460	104000				HLT		;THIS BIT SHOULD BE SET
1251	003462				648:			
1252	003462	042777	000020	014210		RIC	0SYNSCH,0PXCSP	;CLR THIS BIT
1253	003470	032777	000020	014202		BIT	0SYNSCH,0PXCSP	;TEST THIS BIT
1254	003476	001001				BEQ	058	;BR IF "0"
1255	003500	104000				HLT		;THIS BIT SHOULD BE CLR
1256	003502				658:			
1257						;;NOW SET THIS BIT		
1258	003502	052777	000020	014170		BIS	0SYNSCH,0PXCSP	
1259	003510	052777	000040	014176		MIS	0MPSET,0TXCSP	;MASTER RESET
1260	003516	032777	000020	014154		HIT	0SYNSCH,0PXCSP	;TEST THIS BIT
1261	003524	001001				BEQ	068	;BR IF "0"
1262	003526	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1263	003530				668:			
1264	003530	104400				SCOPE		
1265						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1266						;;TESTING OF READ/WRITE BIT DSINTE		
1267						;;		
1268	003532	012767	000013	175366	TST11:	MOV	011,TSTNO	;SAVE THIS
1269	003540	012767	003636	175350		MOV	0TST12,NEXT	;GO TO THIS TEST WHEN THRU
1270	003546	052777	000040	014124		BIS	0DSINTE,0PXCSP	;SET THIS BIT
1271	003554	032777	000040	014116		HIT	0DSINTE,0PXCSP	;TEST THIS BIT
1272	003562	001001				RNE	048	;BR IF "1"
1273	003564	104000				HLT		;THIS BIT SHOULD BE SET
1274	003566				648:			
1275	003566	042777	000040	014104		RIC	0DSINTE,0PXCSP	;CLR THIS BIT
1276	003574	032777	000040	014076		BIT	0DSINTE,0PXCSP	;TEST THIS BIT
1277	003602	001001				BEQ	058	;BR IF "0"
1278	003604	104000				HLT		;THIS BIT SHOULD BE CLR
1279	003606				658:			
1280						;;NOW SET THIS BIT		
1281	003606	052777	000040	014064		BIS	0DSINTE,0PXCSP	
1282	003614	052777	000040	014072		MIS	0MPSET,0TXCSP	;MASTER RESET
1283	003622	032777	000040	014050		HIT	0DSINTE,0PXCSP	;TEST THIS BIT
1284	003630	001001				BEQ	068	;BR IF "0"
1285	003632	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1286	003634				668:			
1287	003634	104400				SCOPE		
1288						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1289						;;TESTING OF READ/WRITE BIT RINTEN		
1290						;;		
1291	003636	012767	000014	175262	TST12:	MOV	012,TSTNO	;SAVE THIS
1292	003644	012767	003742	175244		MOV	0TST13,NEXT	;GO TO THIS TEST WHEN THRU
1293	003652	052777	000100	014020		BIS	0RINTEN,0PXCSP	;SET THIS BIT
1294	003660	032777	000100	014012		HIT	0RINTEN,0PXCSP	;TEST THIS BIT
1295	003666	001001				RNE	048	;BR IF "1"

1296	003670	104000			HLT		;THIS BIT SHOULD BE SFT
1297	003672						
1298	003672	042777	000100	014000	640:	BIC	0RINTEN,0RXCSP ;CLR THIS BIT
1299	003700	032777	000100	013772		BIT	0RINTEN,0RXCSP ;TEST THIS BIT
1300	003706	001401				BEO	650 ;BR IF "0"
1301	003710	104000				HLT	;THIS BIT SHOULD BE CLR
1302	003712				650:		
1303							
1304	003712	052777	000100	013760			;NOW SFT THIS BIT
1305	003720	052777	000400	013766		BIS	0RINTEN,0RXCSP
1306	003726	032777	000100	013744		RIS	0RRESET,0TXCSP ;MASTER RESET
1307	003734	001401				BIT	0RINTEN,0RXCSP ;TEST THIS BIT
1308	003736	104000				BEO	640 ;BR IF "0"
1309	003740					HLT	;CHECK OUT MASTER RESFT LOGIC
1310	003740	104400			660:		
1311							SCOPE
1312							;THIS TEST PERFORMS MASTER RESET TESTING &
1313							;TESTING OF READ/WRITE BIT STPSYN
1314	003742	012767	000015	175156	TST13:	MOV	013,TSTNO ;SAVE THIS
1315	003750	012767	000406	175140		MOV	0TST14,NEXT ;GO TO THIS TEST WHEN THRU
1316	003756	052777	000400	013714		BIS	0STPSYN,0RXCSP ;SET THIS BIT
1317	003764	032777	000400	013706		BIT	0STPSYN,0RXCSP ;TEST THIS BIT
1318	003772	001401				BNE	640 ;BR IF "1"
1319	003774	104000				HLT	;THIS BIT SHOULD BE SET
1320	003776				640:		
1321	003776	042777	000400	013674		BIC	0STPSYN,0RXCSP ;CLR THIS BIT
1322	004004	032777	000400	013666		BIT	0STPSYN,0RXCSP ;TEST THIS BIT
1323	004012	001401				BEO	650 ;BR IF "0"
1324	004014	104000				HLT	;THIS BIT SHOULD BE CLR
1325	004016				650:		
1326							
1327	004016	052777	000400	013654			;NOW SET THIS BIT
1328	004024	052777	000400	013662		RIS	0STPSYN,0RXCSP
1329	004032	032777	000400	013640		BIS	0RRESET,0TXCSP ;MASTER RESFT
1330	004040	001401				BIT	0STPSYN,0RXCSP ;TEST THIS BIT
1331	004042	104000				BEO	660 ;BR IF "0"
1332	004044					HLT	;CHECK OUT MASTER RESFT LOGIC
1333	004044	104400			660:		
1334							SCOPE
1335							;THIS TEST PERFORMS MASTER RESET TESTING &
1336							;TESTING OF READ/WRITE BIT BREAK
1337	004046	012767	000016	175052	TST14:	MOV	014,TSTNO ;SAVE THIS
1338	004054	012767	000152	175034		MOV	0TST15,NEXT ;GO TO THIS TEST WHEN THRU
1339	004062	052777	000001	013624		RIS	0RREAR,0TXCSP ;SET THIS BIT
1340	004070	032777	000001	013616		BIT	0RREAR,0TXCSP ;TEST THIS BIT
1341	004076	001401				BNE	640 ;BR IF "1"
1342	004100	104000				HLT	;THIS BIT SHOULD BE SET
1343	004102				640:		
1344	004102	042777	000001	013604		BIC	0BREAK,0TXCSP ;CLR THIS BIT
1345	004110	032777	000001	013576		BIT	0BREAK,0TXCSP ;TEST THIS BIT
1346	004116	001401				BEO	650 ;BR IF "0"
1347	004120	104000				HLT	;THIS BIT SHOULD BE CLR
1348	004122				650:		
1349							
1350	004122	052777	000001	013564			;NOW SET THIS BIT
1351	004130	052777	000400	013556		RIS	0RREAR,0TXCSP
						BIS	0RRESET,0TXCSP ;MASTER RESET

1352	004136	032777	000001	013550		RIT	00BREAK,0TXCSR	;TEST THIS BIT
1353	004144	001401				BFO	668	;BR IF "0"
1354	004146	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1355	004150				668:			
1356	004150	104400						
1357						SCOPE		
1358						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1359						;;TESTING OF READ/WRITE BIT HDXEN		
1360	004152	012767	000017	174746	TST15:	MOV	015,TSTNO	;SAVE THIS
1361	004160	012767	004256	174730		MOV	0TST16,NEXT	;GO TO THIS TEST WHEN THRU
1362	004166	052777	000010	013520		BIS	0HDXEN,0TXCSR	;SET THIS BIT
1363	004174	032777	000010	013512		BIT	0HDXEN,0TXCSR	;TEST THIS BIT
1364	004202	001001				RNE	648	;BR IF "1"
1365	004204	104000				HLT		;THIS BIT SHOULD BE SET
1366	004206				648:			
1367	004206	042777	000010	013500		BIC	0HDXEN,0TXCSR	;CLR THIS BIT
1368	004214	032777	000010	013472		BIT	0HDXEN,0TXCSR	;TEST THIS BIT
1369	004222	001401				BFO	658	;BR IF "0"
1370	004224	104000				HLT		;THIS BIT SHOULD BE CLR
1371	004226				658:			
1372						;NOW SET THIS BIT		
1373	004226	052777	000010	013460		BIS	0HDXEN,0TXCSR	
1374	004234	052777	000000	013452		RIS	0MPFSET,0TXCSR	;MASTER RESET
1375	004242	032777	000010	013444		BIT	0HDXEN,0TXCSR	;TEST THIS BIT
1376	004250	001401				BFO	668	;BR IF "0"
1377	004252	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1378	004254				668:			
1379	004254	104100				SCOPE		
1380						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1381						;;TESTING OF READ/WRITE BIT SEND		
1382						;;		
1383	004256	012767	000020	174642	TST16:	MOV	016,TSTNO	;SAVE THIS
1384	004264	012767	004362	174624		MOV	0TST17,NEXT	;GO TO THIS TEST WHEN THRU
1385	004272	052777	000020	013414		BIS	0SEND,0TXCSR	;SET THIS BIT
1386	004300	032777	000020	013406		BIT	0SEND,0TXCSR	;TEST THIS BIT
1387	004306	001001				RNE	648	;BR IF "1"
1388	004310	104000				HLT		;THIS BIT SHOULD BE SET
1389	004312				648:			
1390	004312	042777	000020	013374		BIC	0SEND,0TXCSR	;CLR THIS BIT
1391	004320	032777	000020	013366		BIT	0SEND,0TXCSR	;TEST THIS BIT
1392	004326	001401				BFO	658	;BR IF "0"
1393	004330	104000				HLT		;THIS BIT SHOULD BE CLR
1394	004332				658:			
1395						;NOW SET THIS BIT		
1396	004332	052777	000020	013354		RIS	0SEND,0TXCSR	
1397	004340	052777	000000	013346		BIS	0MPFSET,0TXCSR	;MASTER RESET
1398	004346	032777	000020	013340		RIT	0SEND,0TXCSR	;TEST THIS BIT
1399	004354	001401				BFO	668	;BR IF "0"
1400	004356	104000				HLT		;CHECK OUT MASTER RESET LOGIC
1401	004360				668:			
1402	004360	104400				SCOPE		
1403						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1404						;;TESTING OF READ/WRITE BIT DWRITE		
1405						;;		
1406	004362	012767	000021	174536	TST17:	MOV	017,TSTNO	;SAVE THIS
1407	004370	012767	004466	174520		MOV	0TST18,NEXT	;GO TO THIS TEST WHEN THRU

1400	004376	052777	000040	013310		BIS	0DNAINTE,0TXCSR	;SET THIS BIT
1409	004404	032777	000040	013302		BIT	0DNAINTE,0TXCSR	;TEST THIS BIT
1410	004412	001001				BNE	648	;BR IF "1"
1411	004414	104000				HLT		;THIS BIT SHOULD BE SET
1412	004416				648:			
1413	004416	042777	000040	013270		BIC	0DNAINTE,0TXCSR	;CLR THIS BIT
1414	004424	032777	000040	013267		BIT	0DNAINTE,0TXCSR	;TEST THIS BIT
1415	004432	001401				RFO	658	;BR IF "0"
1416	004434	104000				HLT		;THIS BIT SHOULD BE CLR
1417	004436				658:			
1418								
1419	004436	052777	000040	013250				;NOW SET THIS BIT
1420	004444	052777	000040	013247		BIS	0DNAINTE,0TXCSR	
1421	004452	032777	000040	013234		BIS	0MPFSET,0TXCSR	;MASTER RESET
1422	004460	001101				RIT	0DNAINTE,0TXCSR	;TEST THIS BIT
1423	004462	104000				REQ	668	;BR IF "0"
1424	004464					HLT		;CHECK OUT MASTER RESET LOGIC
1425	004464	104400			668:			
1426								
1427								
1428								
1429	004466	012767	000022	174432	TST18:	MOV	018,TSTNO	;SAVE THIS
1430	004474	012767	004572	174414		MOV	0TST19,NEXT	;GO TO THIS TEST WHEN THRU
1431	004502	052777	000100	013204		BIS	0TXINTE,0TXCSR	;SET THIS BIT
1432	004510	032777	000100	013176		BIT	0TXINTE,0TXCSR	;TEST THIS BIT
1433	004516	001001				RVE	648	;BR IF "1"
1434	004520	104000				HLT		;THIS BIT SHOULD BE SET
1435	004522				648:			
1436	004522	042777	000100	013164		RIC	0TXINTE,0TXCSR	;CLR THIS BIT
1437	004530	032777	000100	013156		BIT	0TXINTE,0TXCSR	;TEST THIS BIT
1438	004536	001101				RFO	658	;BR IF "0"
1439	004540	104000				HLT		;THIS BIT SHOULD BE CLR
1440	004542				658:			
1441								
1442	004542	052777	000100	013144				;NOW SET THIS BIT
1443	004550	052777	000040	013136		BIS	0TXINTE,0TXCSR	
1444	004556	032777	000100	013130		RIS	0MPFSET,0TXCSR	;MASTER RESET
1445	004564	001401				RIT	0TXINTE,0TXCSR	;TEST THIS BIT
1446	004566	104000				REQ	668	;BR IF "0"
1447	004570					HLT		;CHECK OUT MASTER RESET LOGIC
1448	004570	104400			668:			
1449								
1450								
1451								
1452								
1453								
1454	004572	012767	000022	174326	TST19:	MOV	019,TSTNO	;SAVE THIS
1455	004600	012767	004676	174310		MOV	0TST20,NEXT	;GO TO THIS TEST WHEN THRU
1456	004606	052777	000040	013100		RIS	0BIT11,0TXCSR	;SET THIS BIT
1457	004614	032777	000040	013072		RIT	0BIT11,0TXCSR	;TEST THIS BIT
1458	004622	001101				BNE	648	;BR IF "1"
1459	004624	104000				HLT		;THIS BIT SHOULD BE SET
1460	004626				648:			
1461	004626	042777	000040	013060		RIC	0BIT11,0TXCSR	;CLR THIS BIT
1462	004634	032777	000040	013052		BIT	0BIT11,0TXCSR	;TEST THIS BIT
1463	004642	001401				RFO	658	;BR IF "0"

1464	004644	104000			HLT		;THIS BIT SHOULD BE CLR
1465	004646				658:		
1466						;NOW SET THIS BIT	
1467	004646	052777	004000	013040	BIS	%BIT11,%TXCSR	
1468	004654	052777	000400	013032	BIS	%MRESET,%TXCSR	;MASTER RESET
1469	004662	032777	004000	013024	BIT	%BIT11,%TXCSR	;TEST THIS BIT
1470	004670	001001			BEO	668	;BR IF "0"
1471	004672	104000			HLT		;CHECK OUT MASTER RESET LOGIC
1472	004674				668:		
1473	004674	104400				SCOPE	
1474						;TEST MAINT MODE BIT 1	
1475						;;	
1476						;THIS TEST PERFORMS MASTER RESET TESTING &	
1477						;TESTING OF READ/WRITE BIT BIT12	
1478						;;	
1479	004676	012767	000024	174222	TST20:	MOV	%20,%TSTNO ;SAVE THIS
1480	004704	012767	005002	174204		MOV	%TST21,%NEXT ;GO TO THIS TEST WHEN THRU
1481	004712	052777	010000	012774		BIS	%BIT12,%TXCSR ;SET THIS BIT
1482	004720	032777	010000	012766		BIT	%BIT12,%TXCSR ;TEST THIS BIT
1483	004726	001001				BNE	648 ;BR IF "1"
1484	004730	104000				HLT	;THIS BIT SHOULD BE SFT
1485	004732				648:		
1486	004732	042777	010000	012754		BIC	%BIT12,%TXCSR ;CLR THIS BIT
1487	004740	032777	010000	012746		BIT	%BIT12,%TXCSR ;TEST THIS BIT
1488	004746	001001				BEO	658 ;BR IF "0"
1489	004750	104000				HLT	;THIS BIT SHOULD BE CLR
1490	004752				658:		
1491						;NOW SET THIS BIT	
1492	004752	052777	010000	012734		BIS	%BIT12,%TXCSR
1493	004760	052777	000400	012726		BIS	%MRESET,%TXCSR ;MASTER RESET
1494	004766	032777	010000	012720		BIT	%BIT12,%TXCSR ;TEST THIS BIT
1495	004774	001001				BEO	668 ;BR IF "0"
1496	004776	104000				HLT	;CHECK OUT MASTER RESET LOGIC
1497	005000				668:		
1498	005000	104400				SCOPE	
1499						;THIS TEST PERFORMS MASTER RESET TESTING &	
1500						;TESTING OF READ/WRITE BIT CLK	
1501						;;	
1502	005002	012767	000025	174116	TST21:	MOV	%21,%TSTNO ;SAVE THIS
1503	005010	012767	005106	174100		MOV	%TST22,%NEXT ;GO TO THIS TEST WHEN THRU
1504	005016	052777	020000	012670		BIS	%CLK,%TXCSR ;SET THIS BIT
1505	005024	032777	020000	012662		BIT	%CLK,%TXCSR ;TEST THIS BIT
1506	005032	001001				BNE	648 ;BR IF "1"
1507	005034	104000				HLT	;THIS BIT SHOULD BE SFT
1508	005036				648:		
1509	005036	042777	020000	012650		BIC	%CLK,%TXCSR ;CLR THIS BIT
1510	005044	032777	020000	012642		BIT	%CLK,%TXCSR ;TEST THIS BIT
1511	005052	001001				BEO	658 ;BR IF "0"
1512	005054	104000				HLT	;THIS BIT SHOULD BE CLR
1513	005056				658:		
1514						;NOW SET THIS BIT	
1515	005056	052777	020000	012630		BIS	%CLK,%TXCSR
1516	005064	052777	000400	012622		BIS	%MRESET,%TXCSR ;MASTER RESET
1517	005072	032777	020000	012614		BIT	%CLK,%TXCSR ;TEST THIS BIT
1518	005100	001001				BEO	668 ;BR IF "0"
1519	005102	104000				HLT	;CHECK OUT MASTER RESET LOGIC

1520	005104				668:		
1521	005104	104400				SCOPE	
1522						;;THIS TEST PERFORMS MASTER RESET TESTING &	
1523						;;TESTING OF READ/WRITE BIT MTDATA	
1524						;;	
1525	005106	012767	000026	174012	TST22:	MOV	022,TSTNO ;SAVE THIS
1526	005114	012767	005212	173774		MOV	0TST23,NEXT ;GO TO THIS TEST WHEN THRU
1527	005122	052777	040000	012564		BIS	0MTDATA,0TXCSR ;SET THIS BIT
1528	005130	032777	040000	012556		BIT	0MTDATA,0TXCSR ;TEST THIS BIT
1529	005136	001001				BNE	648 ;BR IF "1"
1530	005140	104000				HLT	;THIS BIT SHOULD BE SET
1531	005142				648:		
1532	005142	042777	040000	012544		BIC	0MTDATA,0TXCSR ;CLR THIS BIT
1533	005150	032777	040000	012536		BIT	0MTDATA,0TXCSR ;TEST THIS BIT
1534	005156	001001				BNE	658 ;BR IF "0"
1535	005160	104000				HLT	;THIS BIT SHOULD BE CLR
1536	005162				658:		
1537						;;NOW SET THIS BIT	
1538	005162	052777	040000	012524		BIS	0MTDATA,0TXCSR
1539	005170	052777	000400	012516		BIS	0MRESET,0TXCSR ;MASTER RESET
1540	005176	032777	040000	012510		BIT	0MTDATA,0TXCSR ;TEST THIS BIT
1541	005204	001001				BNE	668 ;BR IF "0"
1542	005206	104000				HLT	;CHECK OUT MASTER RESET LOGIC
1543	005210				668:		
1544	005210	104400				SCOPE	
1545						;;THIS TEST VERIFYS THAT INIT (RESET) CLEARS BITS IN THE	
1546						;;0TXCSR & 1TXCSR	
1547						;;	
1548	005212	012767	000027	173706	TST23:	MOV	023,TSTNO ;SAVE THIS
1549	005220	012767	005322	173670		MOV	0TST24,NEXT ;GO TO THIS TEST WHEN THRU
1550	005226	012777	177777	012444		MOV	0177777,0RXCSR ;SET ALL POSSIBLE BITS
1551	005234	012777	177777	012452		MOV	0177777,0TXCSR ;DITTO
1552	005242	000005				RESET	
1553	005244	012767	000040	172524		MOV	0LEVEL7,PS ;RESTORE NON INTERRUPT STATUS
1554	005252	017701	012422			MOV	00TXCSR,P1 ;SAVE
1555	005256	017702	012432			MOV	0TXCSR,P2 ;SAVE
1556	005262	105767	173713			TST	0OPTCLR ;IS THE OPTIONAL CLR JUMPER ON ?
1557	005266	100002				BMI	18 ;YES
1558	005270	042701	000016			BIC	016,P1 ;CLR THE NON RESETTABLE BITS
1559	005274	042701	073000		18:	BIC	0073000,P1 ;CLR ALL NON-CLEARABLE BITS
1560	005300	005701				TST	P1 ;ARE THEY ALL 0 ?
1561	005302	001001				BNE	04
1562	005304	104000				HLT	;ALL SPECIFIED BITS SHOULD BE CLEAR
1563	005306	042702	002200			BIC	0002200,P2 ;CLEAR ALL NON-CLEARABLE BITS
1564	005312	005702				TST	P2 ;ARE THEY ALL 0 ?
1565	005314	001001				BNE	04
1566	005316	104000				HLT	;ALL SPECIFIED BITS SHOULD BE CLEAR
1567	005320	104400				SCOPE	
1568						;;THIS TEST PERFORMS MASTER RESET TESTING &	
1569						;;TESTING OF WRITE ONLY BIT MRESET	
1570						;;	
1571	005322	012767	000030	173576	TST24:	MOV	024,TSTNO ;SAVE THIS
1572	005330	012767	005400	173560		MOV	0TST25,NEXT ;GO TO THIS TEST WHEN THRU
1573	005336	052777	000400	012350		BIS	0MRESET,0TXCSR ;TRY TO SET THIS BIT
1574	005344	032777	000400	012342		BIT	0MRESET,0TXCSR ;TEST THIS BIT
1575	005352	001001				BNE	648 ;BR IF "0"

1576	005354	104400			HLT		;THIS BIT SHOULD NOT BE SET
1577	005356						
1578	005356	052777	000400	012330	648:	RIS	0MPRESET,0TXCSR ;MASTER RESET
1579	005364	032777	000400	012322		BIT	0MPRESET,0TXCSR ;TEST THIS BIT
1580	005372	001401				REQ	650 ;BR IF "0"
1581	005374	104400				HIT	;THIS BIT SHOULD NOT BE SET
1582	005376				658:		
1583							;CHECK MASTER RESET LOGIC
1584	005376	104400					
1585						SCOPE	
1586							;THIS TEST VERIFYS THAT THE RXCSR & TXCSR CAN BE BYTE ADDRESSED (DATOB)
1587	005400	012767	000031	173520	TST25:	MOV	025,TSTNO ;SAVE THIS
1588	005406	012767	005566	173502		MOV	0TST26,NEXT ;GO TO THIS TEST WHEN THRU
1589	005414	052777	000400	012272		RIS	0MPRESET,0TXCSR ;MASTER RESET
1590	005422	105767	173553			TSTR	OPTCLR ;IS THE OPTIONAL CLR JUMPER ON ?
1591	005426	100405				AMI	10 ;YES
1592	005430	012777	000000	012242		MOV	00,0RXCSR ;CLR OUT NON RESETABLE BITS
1593	005436	005777	012236			TST	0RXCSR ;CLR OUT DSC BY READING RXCSR
1594	005442	152777	000001	012232	18:	RISR	0BITW,0HRXCSR ;SET STRIP SYNC UPPER BYTE
1595	005450	017701	012224			MOV	0RXCSR,R1 ;SAVE RXCSR
1596	005454	022701	000400			CMP	0400,R1 ;TEST RXCSR
1597	005460	001401				REQ	0+4
1598	005462	104000				HLT	;ONLY STRIP SYNC SHOULD BE SET
1599	005464	105077	012210			CLRR	0RXCSR ;CLR LOWER BYTE
1600	005470	017701	012204			MOV	0RXCSR,R1 ;SAVE RXCSR
1601	005474	022701	000400			CMP	0400,R1 ;TEST RXCSR
1602	005500	001401				REQ	0+4
1603	005502	104000				HLT	;ONLY STRIP SYNC SHOULD BE SET
1604	005504	052777	000400	012202		BIS	0MPRESET,0TXCSR ;MASTER RESET
1605	005512	152777	000000	012176		RISR	0BITS,0HTXCSR ;SET MAINT CLK UPPER BYTE
1606	005520	017701	012170			MOV	0TXCSR,R1 ;SAVE TXCSR
1607	005524	042701	002000			RIC	0BITW,R1 ;CLR BIT WINDOW (DEPENDENT
1608							ON H315 CONNECTOR EXISTANCE)
1609	005530	022701	020700			CMP	020200,R1 ;TEST TXCSR
1610	005534	001401				REQ	0+4
1611	005536	104000				HLT	;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET
1612	005540	105077	012150			CLRR	0TXCSR ;CLR LOWER BYTE
1613	005544	017701	012144			MOV	0TXCSR,R1 ;SAVE TXCSR
1614	005550	042701	002000			RIC	0BITW,R1 ;CLR BIT WINDOW (DITTO)
1615	005554	022701	020200			CMP	020200,R1 ;TEST TXCSR
1616	005560	001401				REQ	0+4
1617	005562	104000				HLT	;ONLY MAINT CLK BIT & TXDONE SHOULD BE SET
1618	005564	104400				SCOPE	
1619							;THIS TEST PERFORMS MASTER RESET TESTING &
1620							;TESTING OF READ ONLY BIT BITW
1621							;MAINT INTERNAL
1622							
1623	005566	012767	000032	173332	TST26:	MOV	026,TSTNO ;SAVE THIS
1624	005574	012767	005720	173314		MOV	0TST27,NEXT ;GO TO THIS TEST WHEN THRU
1625	005602	012777	044001	012104		MOV	0MINTIMDATAIBREAK,0TXCSR ;SET MAINT INT.,BREAK,
1626							0MNTDATA
1627	005610	032777	002000	012076		BIT	0BITW,0TXCSR ;TEST BITW
1628	005616	001401				RNE	0+4
1629	005620	104000				HLT	;BIT WINDOW SHOULD BE SET
1630	005622	042777	040000	012064		BIC	0MNTDATA,0TXCSR
1631	005630	013702	001136			MOV	00HOLD,R2

1632	005634	005302		181	DEC	R2	
1633	005636	001376			RNE	10	
1634	005640	032777	002000	P12046	BIT	0BITW,0TXCSR	
1635	005646	001401			REQ	.+4	
1636	005650	104000			HLT		;BIT SHOULD BE CLR
1637							;NOW SET THE MTDATA
1638	005652	052777	040000	012034	BIS	0MTDATA,0TXCSR	
1639	005660	052777	000400	012026	RIS	0MRESET,0TXCSR	;MASTER RESET
1640	005666	052777	004001	012020	RIS	0MINTIBREAK,0TXCSR	
1641	005674	013702	001136		MOV	00HOLD,R2	
1642	005700	005302		281	DFC	R2	
1643	005702	001376			RNE	20	
1644	005704	032777	002000	012002	RIT	0BITW,0TXCSR	
1645	005712	001401			REQ	.+4	
1646	005714	104000			HLT		;BITW SHOULD BE CLR BY MASTER RESET
1647	005716	104000					SCOPE
1648							;THIS TEST PERFORMS MASTER RESET TESTING &
1649							;TESTING OF READ ONLY RIT BITW
1650							;MAINT EXTERNAL
1651							;;
1652	005720	012767	000033	173200	TST271	MOV	027,TSTNO ;SAVE THIS
1653	005726	012767	006060	173162		MOV	0TST20,NEXT ;GO TO THIS TEST WHEN THRU
1654							;TEST TO SEE IF EXTERNAL MODEM BYPASS CONNECTOR
1655							;IS ON (H315)....IF "NO" JUMP AROUND TEST
1656	005734	105767	173243			TSTR	JMRBY
1657	005740	100046				BPL	10 ;IT IS NOT ON
1658	005742	012777	050001	011744		MOV	0NEXT,MTDATA;BREAK,0TXCSR ;SET MAINT EXT.,BREAK,
1659							;0MTDATA
1660	005750	032777	002000	011736		BIT	0BITW,0TXCSR ;TEST BITW
1661	005756	001001				RNE	.+4
1662	005760	104000				HLT	;BIT WINDOW SHOULD BE SFT
1663	005762	042777	040000	011724		BIC	0MTDATA,0TXCSR
1664	005770	013702	001136			MOV	00HOLD,R2
1665	005774	005302		281		DEC	R2
1666	005776	001376				RNE	20
1667	006000	032777	002000	011706		RIT	0BITW,0TXCSR
1668	006006	001401				BEO	.+4
1669	006010	104000				HLT	;BIT SHOULD BE CLR
1670							;NOW SET THE MTDATA
1671	006012	052777	040000	011674		BIS	0MTDATA,0TXCSR
1672	006020	052777	000400	011666		RIS	0MRESET,0TXCSR ;MASTER RESET
1673	006026	052777	010001	011660		RIS	0NEXTIBREAK,0TXCSR
1674	006034	013702	001136			MOV	00HOLD,R2
1675	006040	005302		381		DEC	R2
1676	006042	001376				RNE	30
1677	006044	032777	002000	011642		RIT	0BITW,0TXCSR
1678	006052	001401				REQ	.+4
1679	006054	104000				HLT	;BITW SHOULD BE CLR BY MASTER RESET
1680	006056	104000		181			SCOPE
1681							
1682							
1683							;THIS TEST PERFORMS MASTER RESET TESTING &
1684							;TESTING OF READ ONLY RIT RXDONE
1685							;;
1686	006060	012767	000034	173040	TST281	MOV	028,TSTNO ;SAVE THIS
1687	006066	012767	006116	173022		MOV	0TST29,NEXT ;GO TO THIS TEST WHEN THRU

1688	006074	052777	000400	011612		BIS	0MRESET,0TXCSR	;MASTER RESET
1689	006102	032777	000200	011570		BIT	0RXDONE,0RXCSR	;TEST THIS BIT
1690	006110	001401				BEQ	648	;BR IF "0"
1691	006112	104000				HLT		;CHECK MASTER RESET LOGIC
1692	006114				648:			
1693								;OR SHORT ON THIS BIT
1694	006114	104400				SCOPE		
1695						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1696						;;TESTING OF READ ONLY BIT REACT		
1697						;;		
1698	006116	012767	000035	173002	TST29:	MOV	029,TSTNO	;SAVE THIS
1699	006124	012767	006154	172764		MOV	0TST30,NEXT	;GO TO THIS TEST WHEN THRU
1700	006132	052777	000400	011554		BIS	0MPESET,0TXCSR	;MASTER RESET
1701	006140	032777	004000	011532		BIT	0REACT,0PXCSP	;TEST THIS BIT
1702	006146	001401				BEQ	648	;BR IF "0"
1703	006150	104000				HLT		;CHECK MASTER RESET LOGIC
1704	006152				648:			
1705								;OR SHORT ON THIS BIT
1706	006152	104400				SCOPE		
1707						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1708						;;TESTING OF READ ONLY BIT DSC		
1709						;;		
1710	006154	012767	000036	172744	TST30:	MOV	030,TSTNO	;SAVE THIS
1711	006162	012767	006212	172726		MOV	0TST31,NEXT	;GO TO THIS TEST WHEN THRU
1712	006170	052777	000400	011516		BIS	0MPESET,0TXCSR	;MASTER RESET
1713	006176	032777	100000	011474		BIT	0DSC,0RXCSR	;TEST THIS BIT
1714	006204	001401				BEQ	648	;BR IF "0"
1715	006206	104000				HLT		;CHECK MASTER RESET LOGIC
1716	006210				648:			
1717								;OR SHORT ON THIS BIT
1718	006210	104400				SCOPE		
1719						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1720						;;TESTING OF READ ONLY BIT TXDONE		
1721						;;		
1722	006212	012767	000037	172706	TST31:	MOV	031,TSTNO	;SAVE THIS
1723	006220	012767	006250	172670		MOV	0TST32,NEXT	;GO TO THIS TEST WHEN THRU
1724	006226	052777	000400	011460		BIS	0MRESET,0TXCSR	;MASTER RESET
1725	006234	032777	000200	011452		BIT	0TXDONE,0TXCSR	;TEST THIS BIT
1726	006242	001401				BNE	+4	;BR IF "1"
1727	006244	104000				HLT		;CHECK MASTER RESET LOGIC
1728								;OR SHORT ON THIS BIT
1729	006246	104400				SCOPE		
1730						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1731						;;TESTING OF READ ONLY BIT DNA		
1732						;;		
1733	006250	012767	000040	172650	TST32:	MOV	032,TSTNO	;SAVE THIS
1734	006256	012767	006300	172632		MOV	0TST33,NEXT	;GO TO THIS TEST WHEN THRU
1735	006264	052777	000400	011422		BIS	0MRESET,0TXCSR	;MASTER RESET
1736	006272	032777	100000	011414		BIT	0DNA,0TXCSR	;TEST THIS BIT
1737	006300	001401				BEQ	648	;BR IF "0"
1738	006302	104000				HLT		;CHECK MASTER RESET LOGIC
1739	006304				648:			
1740								;OR SHORT ON THIS BIT
1741	006304	104400				SCOPE		
1742						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1743						;;TESTING OF READ ONLY WORD RECEIVE DATA		

1744						11		
1745	006306	012767	000041	172612	TST33:	MOV	033,TSTNO	;SAVE THIS
1746	006314	012767	006354	172574		MOV	0TST34,NEXT	;GO TO THIS TEST WHEN THRU
1747	006322	052777	000400	011364		BIS	0MRESET,0TXCSR	;MASTER RESET
1748	006330	016703	011350			MOV	0RXDBUF,R3	;FOR ERROR MESSAGE
1749	006334	012700	000377			MOV	0377,R0	;EXPECTED
1750	006340	017701	011340			MOV	0RXDBUF,R1	;ACTUAL
1751	006344	120001				CMPR	R0,R1	
1752	006346	001401				BEQ	,+4	;BR IF "0"
1753	006350	104002				HLT	2	;REC DATA SHOULD BE ALL 1'S
1754	006352	104400				SCOPE		
1755						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1756						;;TESTING OF READ ONLY BIT PAPER		
1757						11		
1758	006354	012767	000042	172544	TST34:	MOV	034,TSTNO	;SAVE THIS
1759	006362	012767	006412	172526		MOV	0TST35,NEXT	;GO TO THIS TEST WHEN THRU
1760	006370	052777	000400	011316		BIS	0MRESET,0TXCSR	;MASTER RESET
1761	006376	032777	010000	011300		BIT	0PAPER,0RXDBUF	;TEST THIS BIT
1762	006404	001401				REQ	648	;BR IF "0"
1763	006406	104000				HLT		;CHECK MASTER RESET LOGIC
1764	006410				648:			
1765								;OR SHORT ON THIS BIT
1766	006410	104400				SCOPE		
1767						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1768						;;TESTING OF READ ONLY BIT FRMEPR		
1769						11		
1770	006412	012767	000043	172506	TST35:	MOV	035,TSTNO	;SAVE THIS
1771	006420	012767	006450	172470		MOV	0TST36,NEXT	;GO TO THIS TEST WHEN THRU
1772	006426	052777	000400	011260		BIS	0MRESET,0TXCSR	;MASTER RESET
1773	006434	032777	020000	011242		BIT	0FRMEPR,0RXDBUF	;TEST THIS BIT
1774	006442	001401				REQ	648	;BR IF "0"
1775	006444	104000				HLT		;CHECK MASTER RESET LOGIC
1776	006446				648:			
1777								;OR SHORT ON THIS BIT
1778	006446	104400				SCOPE		
1779						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1780						;;TESTING OF READ ONLY BIT OVRPRN		
1781						11		
1782	006450	012767	000044	172450	TST36:	MOV	036,TSTNO	;SAVE THIS
1783	006456	012767	006506	172432		MOV	0TST37,NEXT	;GO TO THIS TEST WHEN THRU
1784	006464	052777	000400	011222		BIS	0MRESET,0TXCSR	;MASTER RESET
1785	006472	032777	040000	011204		BIT	0OVRPRN,0RXDBUF	;TEST THIS BIT
1786	006500	001401				REQ	648	;BR IF "0"
1787	006502	104000				HLT		;CHECK MASTER RESET LOGIC
1788	006504				648:			
1789								;OR SHORT ON THIS BIT
1790	006504	104400				SCOPE		
1791						;;THIS TEST PERFORMS MASTER RESET TESTING &		
1792						;;TESTING OF READ ONLY BIT RXERR		
1793						11		
1794	006506	012767	000045	172412	TST37:	MOV	037,TSTNO	;SAVE THIS
1795	006514	012767	006544	172374		MOV	0TST38,NEXT	;GO TO THIS TEST WHEN THRU
1796	006522	052777	000400	011164		BIS	0MRESET,0TXCSR	;MASTER RESET
1797	006530	032777	100000	011146		BIT	0RXERR,0RXDBUF	;TEST THIS BIT
1798	006536	001401				REQ	648	;BR IF "0"
1799	006540	104000				HLT		;CHECK MASTER RESET LOGIC

1000	006542				648:	
1001						
1002	006542	104400				
1003						
1004						
1005	006544	012767	000046	172354	TST38:	MOV 038,TSTNO ;SAVE THIS
1006	006552	012767	006652	172336		MOV 0TST39,NEXT ;GO TO THIS TEST WHEN THRU
1007	006560	012777	177777	011112		MOV 0177777,0TXCSR ;SET ALL POSSIBLE BITS
1008	006566	052777	000400	011120		BIS 0MRESET,0TXCSR ;MASTER RESET
1009	006574	016703	011100			MOV 0TXCSR,R3 ;FOR ERROR MESSAGE
1010	006600	017701	011070			MOV 00TXCSR,R1 ;SAVE ACTUAL
1011	006604	105767	172371			TSTB OPTCLR ;TEST THE OPT CLR JUMPER FLAG
1012	006610	100010				BPL 18 ;NO,ITS NOT IN
1013	006612	042701	173000			BIC 0173000,R1 ;CLR NON-MASTER RESETTABLE
1014						;BITS(SINCE THESE ARE DEPENDENT ON H315 CONNECTORS EXISTANCE)
1015	006616	012700	000000			MOV 00,R0 ;EXPECTED
1016	006622	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
1017	006624	001401				BEQ .+4
1018	006626	104001				HLT 1 ;ALL MASTER RESETTABLE BITS SHOULD BE CLR
1019	006630	000407				BP 28 ;JUMP AROUND
1020	006632	042701	073000		18:	BIC 073000,R1 ;CLR NON-MASTER RESETTABLE
1021						;BITS(SINCE THESE ARE DEPENDENT ON H315 CONNECTORS EXISTANCE)
1022	006636	012700	000016			MOV 016,R0 ;EXPECTED
1023	006642	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
1024	006644	001401				BEQ .+4
1025	006646	104001				HLT 1 ;ONLY STD,PTS,DTP BITS SHOULD BE SET
1026						;NOTE THAT STD IS READ =1 INDEPENDENT OF
1027						;SFC XMIT 06 STRAP
1028	006650	104400			28:	SCOPE
1029						
1030						
1031						
1032						
1033	006652	012767	000047	172246	TST39:	MOV 039,TSTNO ;SAVE THIS
1034	006660	012767	006726	172230		MOV 0TST40,NEXT ;GO TO THIS TEST WHEN THRU
1035	006666	012777	177777	011020		MOV 0177777,0TXCSR ;SET ALL POSSIBLE BITS
1036	006674	052777	000400	011012		BIS 0MRESET,0TXCSR ;MASTER RESET
1037	006702	016703	011000			MOV 0TXCSR,R3 ;FOR ERROR MESSAGE
1038	006706	017701	011002			MOV 00TXCSR,R1 ;SAVE ACTUAL
1039	006712	012700	000200			MOV 0200,R0 ;EXPECTED
1040	006716	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
1041	006720	001401				BEQ .+4
1042	006722	104001				HLT 1 ;ONLY TXDONE SHOULD BE SET
1043	006724	104400				SCOPE
1044						
1045						
1046						
1047						
1048	006726	012767	000050	172172	TST40:	MOV 040,TSTNO ;SAVE THIS
1049	006734	012767	006774	172154		MOV 0TST41,NEXT ;GO TO THIS TEST WHEN THRU
1050	006742	052777	000400	010744		BIS 0MRESET,0TXCSR ;MASTER RESET
1051	006750	016703	010730			MOV 0RXDHUF,R3 ;FOR ERROR MESSAGE
1052	006754	017701	010724			MOV 00RXDHUF,R1 ;SAVE
1053	006760	012700	000377			MOV 0377,R0 ;EXPECTED
1054	006764	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
1055	006766	001401				BEQ .+4

1056	006770	104302		
1057	006772	104400		
1058				
1059				
1060				
1061				
1062				
1063				
1064	006774	012767	000051	172124 TST411
1065	007002	012767	007710	172106
1066	007010	005077	010604	
1067	007014	052777	000400	010672
1068				
1069				
1070				
1071				
1072	007022	105767		172155
1073	007026	100402		
1074				
1075	007030	000167	000652	
1076				
1077	007034	016703	010640	
1078	007040	017701	010634	
1079	007044	005000		
1080	007046	005701		
1081	007050	001401		
1082	007052	104001		
1083	007054	052777	000002	010616
1084				
1085				
1086				
1087				
1088	007062	016702		172050
1089	007066			
1090	007066	005302		
1091	007070	001376		
1092				
1093				
1094	007072	017701	010602	
1095	007076	012700	130002	
1096	007102	020001		
1097	007104	001401		
1098	007106	104001		
1099	007110	017701	010564	
1000	007114	012700	030002	
1001	007120	020001		
1002	007122	001401		
1003	007124	104001		
1004				
1005	007126	052777	000004	010544
1006				
1007				
1008				
1009				
1010	007134	016702		171776
1011	007140			

```

HLT      2          ;ONLY REC DATA BITS SHOULD BE SET
SCOPE
;THIS TEST VERIFYS BITS RING,CTS,CARDET,SRD,DSR
;ALSO DSC IS GENERATED WHEN ANY OF THESE BITS ARE SET
;FOR CLFARD.....IT ALSO CHECKS THE MODEM BYPASS
;JUMPER AND THAT THESE BITS CAN BE READ
;NOTE: THE MODEM BYPASS JUMPER MUST BE ON (H315)
;
MOV      041,TSTNO      ;SAVE THIS
MOV      0TST42,NEXT      ;GO TO THIS TEST WHEN THRU
CLR      0RXCSR      ;TO GET RID OF STD ,RTS,DTR IF OPTCLR JUMPER 04 IS NOT ON
BIS      0MRESET,0TXCSR ;MASTER RESET
;TEST THAT A "YES" ANSWER WAS GIVEN TO QUESTION IN
;THE MONITOR OR BY DEFAULT
;THIS TEST WILL BE BYPASSED IF THE EXTERNAL BYPASS
;JUMPER IS NOT INSTALLED
TSTR     JMBRY
BMT      .+6          ;THE ANSWER WAS YES.....
;PERFORM THIS TEST
JMP      OUT1          ;JUMP AROUND THIS TEST IF THE ANSWER
;WAS NO
MOV      RXCSR,H3      ;SET UP FOR ERROR MESSAGE
MOV      0RXCSR,R1      ;ACTUAL
CLR      R0          ;EXPECTED
TST      R1          ;IS IT = 0 ?
BEQ      .+4
HLT      1          ;RXCSR SHOULD BE CLR
BIS      0DTP,0RXCSR      ;SET DTP
;WAIT FOR CABLE DELAYS
;*****
;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
;*****
MOV      HOLD,R2 ;SET DELAY TIME

648:
DFC      P2
BNE      648          ;WAIT THIS TIME
;OK NOW FALL THRU AND CONTINUE TESTING.....
;EXIT STAGE LEFT....CHINNGI
MOV      0RXCSR,R1      ;ACTUAL
MOV      0130002,R0      ;DSC,CTS,CARDFT,DTR
CMP      R0,R1      ;EXPECTED VS ACTUAL
BEQ      .+4
HLT      1          ;CHECK BYPASS CONNECTOR
MOV      0RXCSR,R1      ;ACTUAL
MOV      030002,R0      ;CTS,CARDET,DTR
CMP      R0,R1      ;EXPECTED VS ACTUAL
BEQ      .+4
HLT      1          ;PREVIOUS READING OF RXCSR SHOULD
;HAVE CLEARED DSC
BIS      0RTS,0RXCSR
;WAIT FOR CABLE DELAYS
;*****
;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
;*****
MOV      HOLD,R2 ;SET DELAY TIME

```

658:

1912	007140	005302		DEC	R2	
1913	007142	001376		BNE	650	;WAIT THIS TIME
1914						;OK NOW FALL THRU AND CONTINUE TESTING.....
1915						;EXIT STAGE LEFT....CHINNGI
1916	007144	017701	010530	MOV	0RXCSR,R1	
1917	007150	012700	170006	MOV	0170006,R0	;DSC,RING,CTS,CARDET,RTS,DTR
1918	007154	020001		CMP	R0,R1	;EXPECTED VS ACTUAL
1919	007156	001401		BEQ	,+4	
1920	007160	104001		HLT	1	;CHECK BYPASS CONNECTOR
1921	007162	017701	010512	MOV	0RXCSR,R1	
1922	007166	012700	070006	MOV	070006,R0	;RING,CTS,CARDET,RTS,DTR
1923	007172	020001		CMP	R0,R1	;EXPECTED VS ACTUAL
1924	007174	001401		BEQ	,+4	
1925	007176	104001		HLT	1	;PREVIOUS READING OF RXCSR SHOULD
1926						;HAVE CLEARED DSC
1927	007200	105767	171773	TSTB	SEXMIT	;IS SEC XMIT JUMPER IN ?
1928	007204	100112		BPL	OUT2	;NO
1929	007206	105767	171766	TSTB	SEPEC	;IS SEC REC JUMPER IN ?
1930	007212	100163		BPL	OUT3	;NO
1931	007214	052777	000010 010456	BIS	0STD,0RXCSR	
1932						;WAIT FOR CABLE DELAYS
1933						;*****
1934						;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
1935						;*****
1936	007222	016702	171710	MOV	HOLD,R2	;SET DELAY TIME
1937	007226					
1938	007226	005302				
1939	007230	001376				
1940						
1941						
1942	007232	017701	010447			
1943	007236	012700	173016			
1944						
1945	007242	020001				
1946	007244	001401				
1947	007246	104001				
1948	007250	017701	010424			
1949	007254	012700	073016			
1950						
1951	007260	020001				
1952	007262	001401				
1953	007264	104001				
1954						
1955	007266	042777	000002 010404			
1956						
1957						
1958						
1959						
1960	007274	016702	171636			
1961	007300					
1962	007300	005302				
1963	007302	001376				
1964						
1965						
1966	007304	017701	010370			
1967	007310	012700	143014			

648:	DEC	R2	
	BNE	650	;WAIT THIS TIME
			;OK NOW FALL THRU AND CONTINUE TESTING.....
			;EXIT STAGE LEFT....CHINNGI
	MOV	0RXCSR,R1	
	MOV	0173016,R0	;DSC,RING,CTS,CARDET,SRD,DSR
			;STD,RTS,DTR
	CMP	R0,R1	;EXPECTED VS ACTUAL
	BEQ	,+4	
	HLT	1	;CHECK BYPASS CONNECTOR
	MOV	0RXCSR,R1	
MASK2:	MOV	073016,R0	;RING,CTS,CARDET,SRD,DSR,STD
			;RTS,DTR
	CMP	R0,R1	;EXPECTED VS ACTUAL
	BEQ	,+4	
	HLT	1	;PREVIOUS READING OF RXCSR SHOULD
			;HAVE CLEARED DSC
	RIC	0DTR,0RXCSR	
			;WAIT FOR CABLE DELAYS
			;*****
			;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
			;*****
	MOV	HOLD,R2	;SET DELAY TIME
648:	DEC	R2	
	BNE	648	;WAIT THIS TIME
			;OK NOW FALL THRU AND CONTINUE TESTING.....
			;EXIT STAGE LEFT....CHINNGI
	MOV	0RXCSR,R1	
	MOV	0143014,R0	;DSC,RING,SRD,DSR,STD,RTS

1968	007314	020001				CMP	R2,P1	;EXPECTED VS ACTUAL
1969	007316	001401				REQ	.+4	
1970	007320	104001				HLT	1	;DSC SHOULD BE SET
1971	007322	042777	000004	010350		BIC	0PTS,0RXCSR	
1972								;WAIT FOR CABLE DELAYS
1973								;.....
1974								;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
1975								;.....
1976	007330	016702	171602			MOV	HOLD,R2	;SET DELAY TIME
1977	007334				658:			
1978	007334	005302				DEC	R2	
1979	007336	001376				MNE	658	;WAIT THIS TIME
1980								;OK NOW FALL THRU AND CONTINUE TESTING.....
1981								;EXIT STAGE LEFT....CHINNGI
1982	007340	017701	010334			MOV	0RXCSR,R1	
1983	007344	012700	103010		MASK3:	MOV	0103010,R0	;DSC,SRD,DSR,STD
1984	007350	020001				CMP	R0,P1	;EXPECTED VS ACTUAL
1985	007352	001401				REQ	.+4	
1986	007354	104001				HLT	1	;DSC SHOULD BE SET
1987	007356	042777	000010	010314		BIC	0STD,0RXCSR	
1988								;WAIT FOR CABLE DELAYS
1989								;.....
1990								;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
1991								;.....
1992	007364	016702	171544			MOV	HOLD,R2	;SET DELAY TIME
1993	007370				648:			
1994	007374	005302				DEC	R2	
1995	007372	001376				MNE	648	;WAIT THIS TIME
1996								;OK NOW FALL THRU AND CONTINUE TESTING.....
1997								;EXIT STAGE LEFT....CHINNGI
1998	007374	017701	010300			MOV	0RXCSR,P1	
1999	007400	012700	100000			MOV	0100000,R0	;DSC
2000	007404	020001				CMP	R0,P1	;EXPECTED VS ACTUAL
2001	007406	001401				REQ	.+4	
2002	007410	104001				HLT	1	;DSC SHOULD BE SET
2003	007412	017701	010262			MOV	0RXCSR,P1	
2004	007416	005000				CLL	R0	;NONE
2005	007420	005701				TST	P1	
2006	007422	001401				BFO	.+4	
2007	007424	104001				HLT	1	;DSC SHOULD BE CLEARED FROM PREVIOUS
2008								;READING OF RXCSR
2009	007426	000167	000254			JMP	OUT1	;JUMP AROUND
2010								;THE FOLLOWING ROUTINE HANDLES THE SITUATION WHERE SEC XMIT
2011								;AND SEC REC JUMPERS ARE NOT ON
2012	007432	052777	000010	010240	OUT2:	BIS	0STD,0RXCSR	
2013								;WAIT FOR CABLE DELAYS
2014								;.....
2015								;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2016								;.....
2017	007440	016702	171472			MOV	HOLD,R2	;SET DELAY TIME
2018	007444				648:			
2019	007444	005302				DEC	R2	
2020	007446	001376				MNE	648	;WAIT THIS TIME
2021								;OK NOW FALL THRU AND CONTINUE TESTING.....
2022								;EXIT STAGE LEFT....CHINNGI
2023	007450	017701	010224			MOV	0RXCSR,P1	;ACTUAL

2024	007454	012700	070016		MOV	070016,R0	;EXPECTED: RING,CTS,CARDET,STD,RTS,DTR
2025	007460	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2026	007462	001401			BEQ	,+4	
2027	007464	104001			HLT	1	;CHECK SEC XMIT & SEC REC JUMPERS
2028	007466	042777	000004	010204	BIC	0PTS,0RXCSR	
2029							;WAIT FOR CABLE DELAYS
2030							;*****
2031							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2032							;*****
2033	007474	016702	171436		MOV	HOLD,R2	;SET DELAY TIME
2034	007500			6581			
2035	007500	005302			DEC	R2	
2036	007502	001376			BNE	658	;WAIT THIS TIME
2037							;OK NOW FALL THRU AND CONTINUE TESTING.....
2038							;EXIT STAGE LEFT....CHINNGI
2039	007504	017701	010170		MOV	0RXCSR,R1	;ACTUAL
2040	007510	012700	130012		MOV	0130012,R0	;DSC,CTS,CARDET,DTR,STD
2041							;NOTE THAT DSC STILL ASSERTS EVEN THO THE SEC XMIT JUMPER 0 6 IS NOT ON
2042	007514	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2043	007516	001401			BEQ	,+4	
2044	007520	104001			HLT	1	;CHECK BYPASS CONNECTOR
2045	007522	042777	000002	010150	BIC	0DTR,0RXCSR	
2046							;WAIT FOR CABLE DELAYS
2047							;*****
2048							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2049							;*****
2050	007530	016702	171402		MOV	HOLD,R2	;SET DELAY TIME
2051	007534			6681			
2052	007534	005302			DEC	R2	
2053	007536	001376			BNE	668	;WAIT THIS TIME
2054							;OK NOW FALL THRU AND CONTINUE TESTING.....
2055							;EXIT STAGE LEFT....CHINNGI
2056	007540	017701	010134		MOV	0RXCSR,R1	;ACTUAL
2057	007544	012700	100010		MOV	0100010,R0	;DSC,STD
2058	007550	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2059	007552	001401			BEQ	,+4	
2060	007554	104001			HLT	1	;ONLY DSC & STD SHOULD BE SET
2061	007556	000167	000174		JMP	00171	;JUMP AROUND
2062	007562	052777	000010	010110	BIS	0STD,0RXCSR	
2063				OUT31			;WAIT FOR CABLE DELAYS
2064							;*****
2065							;MODIFY "HOLD:" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2066							;*****
2067	007570	016702	171342		MOV	HOLD,R2	;SET DELAY TIME
2068	007574			6481			
2069	007574	005302			DEC	R2	
2070	007576	001376			BNE	648	;WAIT THIS TIME
2071							;OK NOW FALL THRU AND CONTINUE TESTING.....
2072							;EXIT STAGE LEFT....CHINNGI
2073	007600	017701	010074		MOV	0RXCSR,R1	;ACTUAL
2074	007604	012700	171016		MOV	0171016,R0	;EXPECTED: DSC,RING,CTS,CARDET,DTR,STD,RTS,DTR
2075	007610	020001			CMP	R0,R1	;EXPECTED VS ACTUAL
2076	007612	001401			BEQ	,+4	
2077	007614	104001			HLT	1	;CHECK SEC REC JUMPER
2078	007616	042777	000004	010054	BIC	0PTS,0RXCSR	
2079							;WAIT FOR CABLE DELAYS

Address	Hex Data	Hex Data	Hex Data	Hex Data	Hex Data	Assembly Code
2000						;*****
2001						;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2002						;*****
2003	007624	A16702	1713F6			MOV HOLD,R2 ;SET DELAY TIME
2004	007630				658:	
2005	007630	005302				DEC R2
2006	007632	001376				BNE 658 ;WAIT THIS TIME
2007						;OK NOW FALL THRU AND CONTINUE TESTING.....
2008						;EXIT STAGE LEFT,...CHINNGI
2009	007634	017701	010040			MOV @RXCSP,R1 ;ACTUAL
2010	007640	012700	131012			MOV @131012,R0 ;EXPECTED: DSC,CTS,CARDET,DSR,STD,DTR
2011	007644	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
2012	007646	001401				BEO .+4
2013	007650	104001				HLT 1 ;CHECK H315 CONNECTOR
2014	007652	042777	000002	010020		BIC @DTP,@RXCSP
2015						;WAIT FOR CABLE DELAYS
2016						;*****
2017						;MODIFY "HOLD;" ACCORDINGLY FOR FASTER OR SLOWER MACHINE
2018						;*****
2019	007660	016702	171252			MOV HOLD,R2 ;SET DELAY TIME
2100	007664				668:	
2101	007664	005302				DEC R2
2102	007666	001376				BNE 668 ;WAIT THIS TIME
2103						;OK NOW FALL THRU AND CONTINUE TESTING.....
2104						;EXIT STAGE LEFT,...CHINNGI
2105	007670	017701	010004			MOV @RXCSP,R1 ;ACTUAL
2106	007674	012700	101010			MOV @101010,R0 ;EXPECTED: DSC,DSR,STD
2107	007700	020001				CMP R0,R1 ;EXPECTED VS ACTUAL
2108	007702	001401				BFO .+4
2109	007704	104001				HLT 1 ;CHECK H315 CONNECTOR
2110	007706	104000			OUT1:	SCOPE
2111						
2112						;THIS TEST VERIFYS THAT RECACT (REC ACTIVE) ASSERTS
2113						;IMMED. WHEN SYNC EXTERNAL MODE IS SELECTED
2114						;AND SYNC SEARCH IS SET
2115						;;
2116	007710	012767	030052	171210	TST42:	MOV @42,TSTNO ;SAVE THIS
2117	007716	012767	010036	171172		MOV @TST43,NEXT ;GO TO THIS TEST WHEN THRU
2118	007724	052777	000000	007762		BIS @MPRESET,@TXCSP ;MASTER RESET
2119	007732	012777	020000	007750		MOV @SYNEXT,@PARCSP ;SET THE MODE
2120	007740	052777	000000	007746		BIS @MPRESET,@TXCSP ;MASTER RESET
2121						
2122						;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2123	007746	012777	064001	007740		MOV @MTDATA CLK INT BREAK,@TXCSP
2124						
2125						;SET MODE , & OF BITS,PARITY SENSE,&LOAD SYNC REG
2126	007754	012777	026026	007726		MOV @SYNEXT EIGHT NOPAR 26,@PARCSP
2127	007762	032777	004000	007710		RIT @RECACT,@RXCSP
2128	007770	001401				RFO 648
2129	007772	104000				HLT ;RECACT SHOULD NOT BE SET
2130	007774				648:	
2131	007774	052777	000020	007676		BIS @SYNBCH,@RXCSP ;SET SYNC SEARCH
2132	010002	032777	004000	007670		RIT @RECACT,@RXCSP
2133	010010	001001				BNE 658
2134	010012	104000				HLT ;RECACT DID NOT ASSERT
2135	010014				658:	

2136	010014	042777	000020	007656		BIC	%SYNSCH,%PRCSR	;DROP SEARCH SYNC
2137	010022	032777	004000	007650		BIT	%REACT,%PRCSR	;IS IT =0?
2138	010030	001401				BEG	668	
2139	010032	104000				HLT		;REACT SHOULD BE 0
2140	010034				668:			
2141	010034	104400						
2142							SCOPE	
2143							;;THIS TEST VERIFYS THAT REACT (REC ACTIVE) ASSERTS	
2144							;;IMMED. WHEN ISOCRONOUS MODE IS SELECTED	
2145							;;AND SYNC SEARCH IS SET	
2146	010036	012767	000053	171062	TST43:	MOV	%43,TSTNO	;SAVE THIS
2147	010044	012767	010164	171044		MOV	%TST44,NEXT	;GO TO THIS TEST WHEN THRU
2148	010052	052777	000400	007634		BIS	%MRESET,%TXCSR	;MASTER RESET
2149	010060	012777	000000	007622		MOV	%ISYMOD,%PARCSR	;SET THE MODE
2150	010066	052777	000400	007620		BIS	%MRESET,%TXCSR	;MASTER RESET
2151								
2152								;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2153	010074	012777	004001	007612		MOV	%MTDATA,CLK,MINT,BPFAK,%TXCSR	
2154								
2155								;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
2156	010102	012777	006026	007600		MOV	%ISYMOD,EIGHT,INOPAR,26,%PARCSR	
2157	010110	032777	004000	007502		BIT	%REACT,%PRCSR	
2158	010116	001401				BEG	648	
2159	010120	104000				HLT		;REACT SHOULD NOT BE SET
2160	010122				648:			
2161	010122	052777	000020	007550		BIS	%SYNSCH,%PRCSR	;SET SYNC SEARCH
2162	010130	032777	004000	007542		BIT	%REACT,%PRCSR	
2163	010136	001001				PNF	658	
2164	010140	104000				HLT		;REACT DID NOT ASSERT
2165	010142				658:			
2166	010142	042777	000020	007530		BIC	%SYNSCH,%PRCSR	;DROP SEARCH SYNC
2167	010150	032777	004000	007522		BIT	%REACT,%PRCSR	;IS IT =0?
2168	010156	001401				BEG	668	
2169	010160	104000				HLT		;REACT SHOULD BE 0
2170	010162				668:			
2171	010162	104400					SCOPE	
2172							;;VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING	
2173							;;IN TWO * SYNC CHARS THRU MAINT DATA BIT	
2174							;;WATCH THE REACT BIT	
2175							;;ON THE THIRD * CHARACTER IT SHOULD SET RXDONE	
2176							;;*1 DEPENDENT ON MONITOR.....	
2177							;;IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY	
2178							;;TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT	
2179							;;ON THE SECOND CHARACTER	
2180							;;ALSO CHECK THIS CHARACTER IN RXDBUF	
2181							;;AND CHECK OPERATION OF SYNSCH	
2182							;;MODE: SYNC INTERNAL	
2183							;;LENGTH:FIVE	
2184							;;	
2185	010164	012767	000054	170734	TST44:	MOV	%44,TSTNO	;SAVE THIS
2186	010172	012767	010506	170716		MOV	%TST45,NEXT	;GO TO THIS TEST WHEN THRU
2187	010200	052777	000400	007506		BIS	%MRESET,%TXCSR	;MASTER RESET
2188	010206	012777	000000	007474		MOV	%SYNINT,%PARCSR	;SET THE MODE
2189	010214	052777	000400	007472		BIS	%MRESET,%TXCSR	;MASTER RESET
2190								
2191								;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE

2192	010222	012777	064001	007464	MOV	0MTDATA CLK INT BREAK,0TXCSR	
2193							
2194							
2195	010230	012777	030026	007452			
2196	010236	016703	007442		MOV	0SYNINT FIVE NOPAR 26,0PARCSR	
2197	010242	052777	000020	007430	MOV	RXDRUF,R3	;SET UP FOR ERROR MESSAGE
2198					RIS	0SYNSCH,0RXCSR	;SET SYNC SEARCH
2199	010250	042777	020000	007436			
2200	010256	052777	020000	007430			
2201							
2202	010264	042777	020000	007427			
2203	010272	052777	020000	007414			
2204	010300	012767	000002	170634			
2205	010306	012767	000005	170624			
2206	010314	012767	000026	170622			
2207	010322	004767	007056				
2208	010326	005367	170610				
2209	010332	001403					
2210							
2211	010334	105767	170636				
2212	010340	100762					
2213	010342	105777	007332				
2214	010346	100001					
2215	010350	104000					
2216	010352						
2217	010352	032777	004000	007320			
2218	010360	001001					
2219	010362	104000					
2220	010364						
2221	010364	012767	000005	170546			
2222	010372	012767	000021	170544			
2223	010400	004767	007000				
2224	010404	105777	007270				
2225	010410	100401					
2226	010412	104000					
2227	010414						
2228	010414	032777	004000	007256			
2229	010422	001001					
2230	010424	104000					
2231	010426						
2232	010426	042777	000020	007244			
2233	010434	032777	004000	007236			
2234	010442	001401					
2235	010444	104000					
2236	010446						
2237	010446	105777	007226				
2238	010452	100401					
2239	010454	104000					
2240	010456						
2241	010456	012700	000021				
2242	010462	017701	007216				
2243	010466	020001					
2244	010470	001401					
2245	010472	104000					
2246	010474						
2247	010474	105777	007200				

2248	010500	100001			BPL	718	
2249	010502	104000			HLT		;RXDONE SHOULD BE CLR FROM
2250	010504			718:			
2251							;PREVIOUS READING OF RXDBUF
2252	010504	104400					SCOPE
2253							;VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
2254							;IN TWO * SYNC CHARS THRU MAINT DATA BIT
2255							;WATCH THE RECACT BIT
2256							;ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
2257							;: DEPENDENT ON MONITOR.....
2258							;IF ONE SYNC STAMP IS SELECTED THEN IT WILL ONLY
2259							;TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
2260							;ON THE SECOND CHARACTER
2261							;ALSO CHECK THIS CHARACTER IN RXDBUF
2262							;AND CHECK OPERATION OF SYNCH
2263							;MODE: SYNC INTERNAL
2264							;LENGTH: SIX
2265							;:
2266	010506	012767	000055	170412	TST45:	MOV	045, TSTNO ;SAVE THIS
2267	010514	012767	011030	170374		MOV	0TST46, NEXT ;GO TO THIS TEST WHEN THRU
2268	010522	052777	000400	007164		BIS	0MPESET, 0TXCSR ;MASTER RESET
2269	010530	012777	030000	007152		MOV	0SYNINT, 0PARCSR ;SET THE MODE
2270	010536	052777	000400	007150		BIS	0MPESET, 0TXCSR ;MASTER RESET
2271							
2272							;SET MAINT DATA, CLK, BREAK, & MAINTENANCE MODE
2273	010544	012777	064001	007142		MOV	0MTDATA, CLK, 0MINT, 0BREAK, 0TXCSR
2274							
2275							;SET MODE , 0 OF BITS, PARITY SENSE, & LOAD SYNC REG
2276	010552	012777	032026	007130		MOV	0SYNINT, 0SIX, 0NOPAR, 26, 0PARCSR
2277	010560	016703	007120			MOV	0RXDBUF, R3 ;SET UP FOR ERROR MESSAGE
2278	010564	052777	000020	007106		BIS	0SYNCH, 0RXCSR ;SET SYNC SEARCH
2279							;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION....
2280	010572	042777	020000	007114		BIC	0CLK, 0TXCSR ;POKE CLK DOWN
2281	010600	052777	020000	007106		BIS	0CLK, 0TXCSR ;POKE CLK UP
2282							;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION
2283	010606	042777	020000	007100		BIC	0CLK, 0TXCSR ;POKE CLK DOWN
2284	010614	052777	020000	007072		BIS	0CLK, 0TXCSR ;POKE CLK UP
2285	010622	012767	000002	170312		MOV	02, COUNT
2286	010630	012767	000006	170302	18:	MOV	06, SHIFT ;0 OF SHIFTS
2287	010636	012767	000020	170300		MOV	026, TEMP1 ;SYNC CHARACTER
2288	010644	004767	006534			JSR	PC, 0POKE
2289	010650	005367	170266			DEC	COUNT
2290	010654	001403				REQ	28
2291							;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
2292	010656	105767	170314			TSTR	0SYNCNO
2293	010662	100762				BMI	18 ;TWO SYNC CHARS
2294	010664	105777	007010		28:	TSTR	0RXCSR ;CHECK REC DONE BIT
2295	010670	100001				HPL	048
2296	010672	104000				HLT	;RXDONE SHOULD NOT BE ASSERTED
2297	010674				648:		
2298	010674	032777	004000	006776		BIT	0RECACT, 0RXCSR
2299	010702	001001				RNE	058
2300	010704	104000				HLT	;RECACT SHOULD BE ASSERTED
2301	010706				658:		
2302	010706	012767	000006	170224		MOV	06, SHIFT
2303	010714	012767	000021	170222		MOV	021, TEMP1 ;ANY CHARACTER

2304	010722	004767	006456		JSR	PC,PPOKE
2305	010726	105777	006746		TSTR	0RXCSR ;CHECK RXDONE
2306	010732	100401			BMI	668
2307	010734	104000			HLT	;RXDONE SHOULD BE ASSERTED
2308	010736			668:		
2309	010736	032777	004000	006734	RIT	0REACT,0RXCSR
2310	010744	001001			BNE	678
2311	010746	104000			HLT	;REACT SHOULD STILL BE ASSERTED
2312	010750			678:		
2313	010752	032777	000020	006722	BIC	0SYNSCH,0RXCSR ;CLR SYNC SEARCH
2314	010756	032777	004000	006714	RIT	0REACT,0RXCSR ;IT SHOULD DROP IMMEDIATELY
2315	010764	001401			REQ	688
2316	010766	104000			HLT	;REACT SHOULD BE CLR
2317	010770			688:		
2318	010770	105777	006704		TSTR	0RXCSR ;RXDONE
2319	010774	100401			BMI	698
2320	010776	104000			HLT	;RXDONE SHOULD STILL BE ASSERTED
2321	011000			698:		
2322	011000	012700	000021		MOV	021,R0 ;EXPECTED DATA
2323	011004	017701	006674		MOV	0RXDBUF,R1 ;ACTUAL DATA
2324	011010	020001			CMP	R0,R1 ;COMPARE EXP VS ACT
2325	011012	001401			BEQ	708
2326	011014	104002			HLT	;DATA CHARS SHOULD COMPARE
2327	011016			708:		
2328	011016	105777	006656		TSTR	0RXCSR ;CHECK RXDONE
2329	011022	100001			RPL	718
2330	011024	104000			HLT	;RXDONE SHOULD BE CLR FROM
2331	011026			718:		
2332						;PREVIOUS READING OF RXDBUF
2333	011026	104400				SCOPE
2334						;VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING
2335						;IN TWO * SYNC CHARS THRU MAINT DATA BIT
2336						;WATCH THE REACT BIT
2337						;ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
2338						;IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
2339						;TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
2340						;ON THE SECOND CHARACTER
2341						;ALSO CHECK THIS CHARACTER IN RXDBUF
2342						;AND CHECK OPERATION OF SYNSCH
2343						;MODE: SYNC INTERNAL
2344						;LENGTH:SEVEN
2345						
2346						
2347	011030	012767	000056	170070	TST46:	MOV 046,TSTNO ;SAVE THIS
2348	011036	012767	011352	170052		MOV 0TST47,NEXT ;GO TO THIS IFST WHEN THRU
2349	011044	052777	000000	006642	BIS	0MRESET,0TXCSR ;MASTER RESET
2350	011052	012777	030000	006630	MOV	0SYNINT,0PARCSR ;SET THE MODE
2351	011060	052777	000000	006626	BIS	0MRESET,0TXCSR ;MASTER RESET
2352						
2353						;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2354	011066	012777	064001	006620	MOV	0MTDATA,CLK,MINT,BREAK,0TXCSR
2355						
2356						;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
2357	011074	012777	034026	006606	MOV	0SYNINT,SEVEN;NOPARI26,0PARCSR
2358	011102	016703	006576		MOV	RXDBUF,R3 ;SET UP FOR ERROR MESSAGE
2359	011106	052777	000020	006564	BIS	0SYNSCH,0RXCSR ;SET SYNC SEARCH

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2360 ;POKE CLK TO GET RECEIVER INTO SYNCROIZATION....
2361 011114 042777 020000 006572 BIC 0CLK,0TXCSR ;POKE CLK DOWN
2362 011122 052777 020000 006564 BIS 0CLK,0TXCSR ;POKE CLK UP
2363 ;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
2364 011130 042777 020000 006556 BIC 0CLK,0TXCSR ;POKE CLK DOWN
2365 011136 052777 020000 006550 BIS 0CLK,0TXCSR ;POKE CLK UP
2366 011144 012767 000002 167770 MOV 02,COUNT
2367 011152 012767 000007 167760 18: MOV 07,SHIFT ;0 OF SHIFTS
2368 011160 012767 000026 167756 MOV 026,TEMP1 ;SYNC CHARACTER
2369 011166 004767 006212 JSR PC,PPOKE
2370 011172 005367 167744 DFC COUNT
2371 011176 001403 BEO 28
2372 ;TEST SYNCNO TO SEE HOW MANY SYNC CHAPS WERE SELECTED
2373 011200 105767 167772 TSTR SYNCNO
2374 011204 105762 BMI 18 ;TWO SYNC CHAPS
2375 011206 105777 006466 28: TSTR 00XCSR ;CHECK PEC DONE BIT
2376 011212 105701 BPL 648
2377 011214 104000 HLT ;RXDONE SHOULD NOT BE ASSERTED
2378 011216 032777 004000 006454 648: BIT 0REACT,00XCSR
2379 011224 001001 BNE 658
2380 011226 104000 HLT ;REACT SHOULD BE ASSERTED
2381 011230 012767 000007 167702 658: MOV 07,SHIFT
2382 011236 012767 000021 167700 MOV 021,TEMP1 ;ANY CHARACTER
2383 011244 004767 006134 JSR PC,PPOKE
2384 011250 105777 006424 TSTR 00XCSR ;CHECK RXDONE
2385 011254 104001 BMI 668
2386 011256 104000 HLT ;RXDONE SHOULD BE ASSERTED
2387 011260 032777 004000 006412 668: BIT 0REACT,00XCSR
2388 011266 001001 BNE 678
2389 011270 104000 HLT ;REACT SHOULD STILL BE ASSERTED
2390 011272 042777 000020 006400 678: BIC 0SYNSCH,00XCSR ;CLR SYNC SEARCH
2391 011300 032777 004000 006372 BIT 0REACT,00XCSR ;IT SHOULD DROP IMMEDIATELY
2392 011306 001401 BEQ 688
2393 011310 104000 HLT ;REACT SHOULD BE CLR
2394 011312 105777 006362 688: TSTR 00XCSR ;RXDONE
2395 011316 100401 BMI 698
2396 011320 104000 HLT ;RXDONE SHOULD STILL BE ASSERTED
2397 011322 012700 000021 698: MOV 021,R0 ;EXPECTED DATA
2398 011326 017701 006352 MOV 00XDBUF,R1 ;ACTUAL DATA
2399 011332 020001 CMP R0,R1 ;COMPARE EXP VS ACT
2400 011334 001401 BFO 708
2401 011336 104002 HLT 2 ;DATA CHARS SHOULD COMPARE
2402 011340 105777 006334 708: TSTR 00XCSR ;CHECK RXDONE
2403 011344 100001 BPL 718
2404 011346 104000 HLT ;RXDONE SHOULD BE CLR FROM
2405 011350 718: ;PREVIOUS READING OF RXDBUF
2406 011350 104000 SCOPE
2407 011350 104000 ;VERIFY THE MATCH DETECT & DATA RDY FLAGS BY PUMPING

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2416						;;IN TWO * SYNC CHARS THRU MAINT DATA BIT
2417						;;WATCH THE RECACT BIT
2418						;;ON THE THIRD * CHARACTER IT SHOULD SET RXDONE
2419						;;: DEPENDENT ON MONITOR.....
2420						;;IF ONE SYNC STRAP IS SELECTED THEN IT WILL ONLY
2421						;;TAKE ONE SYNC CHARACTER FOR RXDONE TO ASSERT
2422						;;ON THE SECOND CHARACTER
2423						;;ALSO CHECK THIS CHARACTER IN RXDBUF
2424						;;AND CHECK OPERATION OF SYN SCH
2425						;;MODE: SYNC INTERNAL
2426						;;LENGTH: EIGHT
2427						;;
2428	011352	012767	000057	167546	TST47:	MOV 047,TSTNO ;SAVE THIS
2429	011360	012767	011674	167530		MOV 0TST48,NEXT ;GO TO THIS TST WHEN THRU
2430	011366	052777	000400	006320		RIS 0MRESET,0TXCSR ;MASTER RESET
2431	011374	012777	030000	006306		MOV 0SYNINT,0PARCSR ;SET THE MODE
2432	011402	052777	000400	006304		BIS 0MRESET,0TXCSR ;MASTER RESET
2433						
2434						;;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2435	011410	012777	064001	006276		MOV 0MTDATA,CLK,MINT,BREAK,0TXCSR
2436						
2437						;;SET MODE ,0 OF BITS,PARITY SENSE,&LOAD SYNC REG
2438	011416	012777	036026	006264		MOV 0SYNINT,EIGHT,INOPAR,26,0PARCSR
2439	011424	016703	006254			MOV RXDBUF,R3 ;SET UP FOR ERROR MESSAGE
2440	011430	052777	000020	006242		RIS 0SYNSCH,0RXCSR ;SET SYNC SEARCH
2441						;;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION....
2442	011436	042777	020000	006250		RIC 0CLK,0TXCSR ;POKE CLK DOWN
2443	011444	052777	020000	006242		BIS 0CLK,0TXCSR ;POKE CLK UP
2444						;;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION
2445	011452	042777	020000	006234		BIC 0CLK,0TXCSR ;POKE CLK DOWN
2446	011460	052777	020000	006226		BIS 0CLK,0TXCSR ;POKE CLK UP
2447	011466	012767	000002	167446		MOV 02,COUNT
2448	011474	012767	000010	167436	18:	MOV 00,,SHIFT ;0 OF SHIFTS
2449	011502	012767	000020	167434		MOV 026,TEMP1 ;SYNC CHARACTER
2450	011510	004767	005670			JSR PC,PPOKE
2451	011514	005367	167422			DEC COUNT
2452	011520	001403				HFQ 28
2453						;;TEST SYNCNO TO SEE HOW MANY SYNC CHARS WERE SELECTED
2454	011522	105767	167450			TSTR SYNCNO
2455	011526	100762				RMI 18 ;TWO SYNC CHARS
2456	011530	165777	006144		28:	TSTR 0RXCSR ;CHECK REC DONE BIT
2457	011534	100001				BPL 648
2458	011536	104000				HLT ;RXDONE SHOULD NOT BE ASSERTED
2459	011540				648:	
2460	011540	032777	004000	006132		BIT 0RECACT,0RXCSR
2461	011546	001001				BNE 658
2462	011550	104000				HLT ;RECACT SHOULD BE ASSERTED
2463	011552				658:	
2464	011552	012767	000010	167360		MOV 00,,SHIFT
2465	011560	012767	000021	167356		MOV 021,TEMP1 ;ANY CHARACTER
2466	011566	004767	005612			JSR PC,PPOKE
2467	011572	105777	006102			TSTR 0RXCSR ;CHECK RXDONE
2468	011576	100001				RMI 668
2469	011600	104000				HLT ;RXDONE SHOULD BE ASSERTED
2470	011602				668:	
2471	011602	032777	004000	006070		BIT 0RECACT,0RXCSR

2472	011610	001001			BNE	678	
2473	011612	104000			HLT		;REACT SHOULD STILL BE ASSERTED
2474	011614			678:			
2475	011614	042777	000020	006056	BIC	0SYNSCH,0RXCSR	;CLR SYNC SEARCH
2476	011622	032777	004000	006050	BIT	0REACT,0RXCSR	;IT SHOULD DROP IMMEDIATELY
2477	011630	001401			BEQ	608	
2478	011632	104000			HLT		;REACT SHOULD BE CLR
2479	011634			608:			
2480	011634	105777	006040		TSTR	0RXCSR	;PXDONE
2481	011640	100401			BMI	698	
2482	011642	104000			HLT		;RXDONE SHOULD STILL BE ASSERTED
2483	011644			698:			
2484	011644	012700	000021		MOV	021,R0	;EXPECTED DATA
2485	011650	017701	006030		MOV	0RXDBUF,R1	;ACTUAL DATA
2486	011654	020001			CMP	R0,R1	;COMPARE EXP VS ACT
2487	011656	001401			RFQ	708	
2488	011660	104002			HLT	2	;DATA CHARS SHOULD COMPARE
2489	011662			708:			
2490	011662	105777	006012		TSTR	0RXCSR	;CHECK PXDONE
2491	011666	100001			BPL	718	
2492	011670	104000			HLT		;RXDONE SHOULD BE CLR FROM
2493	011672			718:			
2494							;PREVIOUS READING OF RXDBUF
2495	011672	104400					SCOPE
2496							;;THIS TEST VERIFYS WORD LENGTH SELECT OF THE
2497							;;RECEIVER SECTION,IT USES THE FRROP FLAGS
2498							;;TO DETERMINE THAT IT WAS SELECTED CORRECTLY
2499							;;(OVRRUN,RXERR)
2500							;;MODF:ISYMOD
2501							;;LENGTH:FIVE
2502							;;CHAR:25
2503							;;
2504	011674	012767	000060	167224	TST40:	MOV	040,TSTNO ;SAVE THIS
2505	011702	012767	012130	167206		MOV	0TST40,NEXT ;GO TO THIS TEST WHEN THRU
2506	011710	052777	000400	005776		BIS	0MRESET,0TXCSR ;MASTER RESET
2507	011716	012777	000000	005764		MOV	0ISYMOD,0PARCSR ;SET THE MODE
2508	011724	052777	000400	005762		BIS	0MRESET,0TXCSR ;MASTER RESET
2509							
2510							;SET MAINT DATA,CLK,BREAK,6MAINTENANCE MODE
2511	011732	012777	064001	005754		MOV	0MTDATA CLK INT BREAK,0TXCSR
2512							
2513							;SET MODE ,0 OF BITS,PARITY SENSE,6LOAD SYNC REG
2514	011740	012777	000000	005742		MOV	0ISYMOD FIVE NOPAR 0,0PARCSR
2515	011746	052777	000020	005724		BIS	0SYNSCH,0RXCSR ;SET SYNC SEARCH
2516							;POKE CLK TO GET RECEIVER INTO SYNCRIZATION....
2517	011754	042777	020000	005732		BIC	0CLK,0TXCSR ;POKE CLK DOWN
2518	011762	052777	020000	005724		BIS	0CLK,0TXCSR ;POKE CLK UP
2519							;POKE CLK TO GET LOGIC INTO SYNCRONIZATION
2520	011770	042777	020000	005716		BIC	0CLK,0TXCSR ;POKE CLK DOWN
2521	011776	052777	020000	005710		BIS	0CLK,0TXCSR ;POKE CLK UP
2522	012004	016703	005674			MOV	0RXDBUF,R3 ;SET UP FOR ERROR MESSAGE
2523	012010	012700	000025			MOV	025,R0 ;EXPECTED
2524	012014	012767	000007	167116		MOV	07,SHIFT ;0 OF SHIFTS
2525	012022	012767	000152	167114		MOV	0152,TEMP1 ;DATA CHAR
2526	012030	004707	005350			JSR	PC,RPOKE ;SHIFT IN THIS CHAR
2527	012034	105777	005640			TSTR	0RXCSR ;RXDONE ?

2528	012040	100401			BMI	648	
2529	012042	100000			HLT		;RXDONE SHOULD BE SET
2530	012044					648:	
2531	012044	017701	005634		MOV	0RXDBUF,R1	;ACTUAL
2532	012050	020001			CMP	R0,R1	;COMPARE EXPECTED VS. ACTUAL
2533	012052	001401			REQ	658	
2534	012054	104002			HLT	2	;RECEIVED DATA DID NOT MATCH ;EXPECTED DATA - CHECK MAINT DATA ;OR RECEIVER LOGIC
2535							
2536							
2537	012056					658:	
2538	012056	012767	000007	167054	MOV	07,SHIFT	;# OF SHIFTS
2539	012064	012767	000152	167052	MOV	0152,TEMP1	;DATA CHAR
2540	012072	004767	005306		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2541							;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
2542	012076	012767	000007	167034	MOV	07,SHIFT	;# OF SHIFTS
2543	012104	012767	000152	167032	MOV	0152,TEMP1	;DATA CHAR
2544	012112	004767	005206		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2545	012116	012700	100025		MOV	0140000125,R0	;EXPECTED DATA PLUS ;RXERR & OVPRUN
2546							
2547	012122	017701	005556		MOV	0RXDBUF,R1	;ACTUAL
2548	012126	020001			CMP	R0,R1	;COMPARE EXP VS. ACT
2549	012130	001401			REQ	668	
2550	012132	104002			HLT	2	;SPECIFICALLY LOOK AT RXERR & ;OVPRUN BITS...THEY BOTH SHOULD BE SET
2551							
2552	012134					668:	
2553	012134	104002					SCOPE
2554							;;THIS TEST VERIFYS WORD LENGTH SELECT OF THE
2555							;;RECEIVER SECTION,IT USES THE ERROR FLAGS
2556							;;TO DETERMINE THAT IT WAS SELECTED CORRECTLY
2557							;;(OVPRUN,RXERR)
2558							;;MODE;ISYMOD
2559							;;LENGTH;FIVE
2560							;;CHAR;12
2561							;;
2562	012136	012767	000001	166762	TST49:	MOV	049,ISTNO ;SAVE THIS
2563	012144	012767	012400	166744		MOV	0TST50,NEXT ;GO TO THIS TEST WHEN THRU
2564	012152	052777	000400	005534		BIS	0MPRESET,0TXCSR ;MASTER RESET
2565	012160	012777	000000	005522		MOV	0ISYMOD,0PARCSR ;SET THE MODE
2566	012166	052777	000400	005520		BIS	0MPRESET,0TXCSR ;MASTER RESET
2567							
2568							;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2569	012174	012777	004001	005512		MOV	0MTDATA;CLK;MINT;BREAK,0TXCSR
2570							
2571							;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
2572	012202	012777	000000	005500		MOV	0ISYMOD;FIVE;NOPAR;0,0PARCSR
2573	012210	052777	000020	005462		BIS	0SYNSCH,0RXCSR ;SET SYNC SEARCH
2574							;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION....
2575	012216	042777	020000	005470		BIC	0CLK,0TXCSR ;POKE CLK DOWN
2576	012224	052777	020000	005462		BIS	0CLK,0TXCSR ;POKE CLK UP
2577							;POKE CLK TO GET LOGIC INTO SYNCHRONIZATION
2578	012232	042777	020000	005454		BIC	0CLK,0TXCSR ;POKE CLK DOWN
2579	012240	052777	020000	005446		BIS	0CLK,0TXCSR ;POKE CLK UP
2580	012246	016703	005432			MOV	0RXDR'F,R3 ;SET UP FOR ERROR MESSAGE
2581	012252	012700	000012			MOV	012,R0 ;EXPECTED
2582	012256	012767	000007	166654		MOV	07,SHIFT ;# OF SHIFTS
2583	012264	012767	000124	166652		MOV	0124,TEMP1 ;DATA CHAR

2584	012272	004767	005106		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2585	012276	105777	005376		ISTB	0RXCSR	;RXDONE ?
2586	012302	100401			RMI	648	
2587	012304	104000			MLT		;RXDONE SHOULD BE SET
2588	012306			648:			
2589	012306	017701	005372		MOV	0RXDBUF,R1	;ACTUAL
2590	012312	020001			CMP	R0,R1	;COMPARE EXPECTED VS. ACTUAL
2591	012314	001401			BEQ	658	
2592	012316	104002			MLT	2	;RECEIVED DATA DID NOT MATCH
2593							;EXPECTED DATA - CHECK MAINT DATA
2594							;OR RECEIVER LOGIC
2595	012320			658:			
2596	012320	012767	000007	166612	MOV	07,SHIFT	;# OF SHIFTS
2597	012326	012767	000124	166610	MOV	0124,TEMP1	;DATA CHAR
2598	012334	004767	005044		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2599							;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
2600	012340	012767	000007	166572	MOV	07,SHIFT	;# OF SHIFTS
2601	012346	012767	000124	166570	MOV	0124,TEMP1	;DATA CHAR
2602	012354	004767	005024		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2603	012360	012767	140017		MOV	0140000112,R0	;EXPECTED DATA PLUS
2604							;RXERR & OVRUN
2605	01236	017701	005314		MOV	0RXDBUF,R1	;ACTUAL
2606	012370	020001			CMP	R0,R1	;COMPARE EXP VS. ACT
2607	012372	001401			BEQ	668	
2608	012374	104002			MLT	2	;SPECIFICALLY LOOK AT RXERR &
2609							;OVRUN BITS...THEY BOTH SHOULD BE SET
2610	012376			668:			
2611	012376	104400					SCOPE
2612							;;THIS TEST VERIFYS WORD LENGTH SELECT OF THE
2613							;;RECEIVER SECTION,IT USES THE ERROR FLAGS
2614							;;TO DETERMINE THAT IT WAS SELECTED CORRECTLY
2615							;;(OVRUN,RXERR)
2616							;;MODE:ISYMOD
2617							;;LENGTH:FIVE
2618							;;CHAR:37
2619							;;
2620	012400	012767	000002	166520	TST50:	MOV	050,TSTNO
2621	012406	012767	012642	166502		MOV	0TST51,NEXT
2622	012414	052777	000400	005272		BIS	0MPRESF,0TXCSR
2623	012422	012777	000000	005260		MOV	0ISYMOD,0PARCSR
2624	012430	052777	000400	005256		BIS	0MPRESF,0TXCSR
2625							;MASTER RESET
2626							;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2627	012436	012777	064001	005250		MOV	0MTDATA CLK MAINT BREAK,0TXCSR
2628							
2629							;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
2630	012444	012777	000000	005236		MOV	0ISYMOD FIVE NOPAR 0,0PARCSR
2631	012452	052777	000020	005220		BIS	0SYNSCH,0RXCSR
2632							;SET SYNC SEARCH
2633	012460	042777	020000	005226			;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION....
2634	012466	052777	020000	005220		BIC	0CLK,0TXCSR
2635							;POKE CLK DOWN
2636	012474	042777	020000	005212		BIS	0CLK,0TXCSR
2637	012502	052777	020000	005204			;POKE CLK UP
2638	012510	016703	005170			MOV	0RXDBUF,R3
2639	012514	012700	000037			MOV	037,R0
							;SET UP FOR ERROR MESSAGE
							;EXPECTED

2640	R12520	012767	000007	166412	MOV	07,SHIFT	;# OF SHIFTS
2641	012526	012767	000176	166410	MOV	0176,TEMP1	;DATA CHAR
2642	R12534	004767	004644		JSP	PC,RPOKE	;SHIFT IN THIS CHAR
2643	012540	105777	005134		TSTR	0RXCSR	;RXDONE ?
2644	012544	100401			BMI	648	
2645	012546	104000			HLT		;RXDONE SHOULD BE SET
2646	012550			648:			
2647	012550	017701	005130		MOV	0RXDBUF,R1	;ACTUAL
2648	012554	020001			CMP	R0,R1	;COMPARE EXPECTED VS. ACTUAL
2649	012556	001401			BLO	658	
2650	012560	104002			HLT	2	;RECEIVED DATA DID NOT MATCH ;EXPECTED DATA - CHECK MAINT DATA ;OR RECEIVER LOGIC
2651							
2652							
2653	012562			658:			
2654	012562	012767	000007	166350	MOV	07,SHIFT	;# OF SHIFTS
2655	012570	012767	000176	166346	MOV	0176,TEMP1	;DATA CHAR
2656	012576	004767	004602		JSR	PC,RPOKE	;SHIFT IN THIS CHAR
2657							;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
2658	012602	012767	000007	166330	MOV	07,SHIFT	;# OF SHIFTS
2659	012610	012767	000176	166326	MOV	0176,TEMP1	;DATA CHAR
2660	012616	004767	004502		JSP	PC,RPOKE	;SHIFT IN THIS CHAR
2661	012622	012700	140037		MOV	0140000137,R0	;EXPECTED DATA PLUS ;RXERR & OVRUN
2662							
2663	012626	017701	005052		MOV	0RXDBUF,R1	;ACTUAL
2664	012632	020001			CMP	R0,R1	;COMPARE EXP VS. ACT
2665	012634	001401			RFU	668	
2666	012636	104002			HLT	2	;SPECIFICALLY LOOK AT RXERR & ;OVRUN BITS...THEY BOTH SHOULD BE SET
2667							
2668	012640			668:			
2669	012640	104400					
2670							SCOPE
2671							;THIS TEST VERIFYS WORD LENGTH SELECT OF THE
2672							;RECEIVER SECTION,IT USES THE ERROR FLAGS
2673							;TO DETERMINE THAT IT WAS SELECTED CORRECTLY
2674							;((OVRUN,RXERR)
2675							;MODE:ISYMOD
2676							;LENGTH:FIVE
2677							;CHAR:0
2678	012642	012767	000003	166256	TST51:	MOV	051,TSTNO
2679	012650	012767	013104	166240		MOV	0,EOP,NEXT
2680	012656	052777	000400	005030		BIS	0MRFSET,0TXCSR
2681	012664	012777	000000	005016		MOV	0ISYMOD,0PARCSR
2682	012672	052777	000400	005014		BIS	0MRFSET,0TXCSR
2683							;MASTER RESET
2684							;SET MAINT DATA,CLK,BREAK,&MAINTENANCE MODE
2685	012700	012777	004001	005006		MOV	0MTDATA,CLK,MINT,BREAK,0TXCSR
2686							
2687							;SET MODE ,# OF BITS,PARITY SENSE,&LOAD SYNC REG
2688	012706	012777	000000	004774		MOV	0ISYMOD,FIVE,NO,0PARCSR
2689	012714	052777	000020	004756		BIS	0SYNSCH,0RXCSR
2690							;SET SYNC SEARCH
2691	012722	042777	020000	004764			;POKE CLK TO GET RECEIVER INTO SYNCHRONIZATION,...
2692	012730	052777	020000	004756		RJC	0CLK,0TXCSR
2693							;POKE CLK DOWN
2694	012736	042777	020000	004750		BIS	0CLK,0TXCSR
2695	012744	052777	020000	004742			;POKE CLK UP

2696	012752	016703	004726		MOV	RXDBUF,R3	;SET UP FOR ERROR MESSAGE
2697	012756	012704	000000		MOV	00,R0	;EXPECTED
2698	012762	012767	000007	166150	MOV	07,SHIFT	;0 OF SHIFTS
2699	012770	012767	000100	166146	MOV	0100,TEMP1	;DATA CHAP
2700	012776	004767	004402		JSR	PC,PPOKE	;SHIFT IN THIS CHAR
2701	013002	105777	004672		TSTB	0RXCSR	;PXDONE ?
2702	013006	100401			BMI	648	
2703	013010	104000			HLT		;PXDONE SHOULD BE SET
2704	013012			648:			
2705	013012	017701	004666		MOV	0RXDBUF,R1	;ACTUAL
2706	013016	020001			CMP	R0,R1	;COMPARE EXPECTED VS. ACTUAL
2707	013020	001001			BEO	650	
2708	013022	104002			HLT	2	;RECEIVED DATA DID NOT MATCH
2709							;EXPECTED DATA - CHECK MAINT DATA
2710							;OR RECEIVER LOGIC
2711	013024			650:			
2712	013024	012767	000007	166106	MOV	07,SHIFT	;0 OF SHIFTS
2713	013032	012767	000100	166104	MOV	0100,TEMP1	;DATA CHAP
2714	013040	004767	004340		JSR	PC,PPOKE	;SHIFT IN THIS CHAR
2715							;NOW SHIFT IN A SECOND CHARACTER WITHOUT READING RXDBUF
2716	013044	012767	000007	166066	MOV	07,SHIFT	;0 OF SHIFTS
2717	013052	012767	000100	166064	MOV	0100,TEMP1	;DATA CHAP
2718	013060	004767	004320		JSR	PC,PPOKE	;SHIFT IN THIS CHAR
2719	013064	012700	140000		MOV	014000010,R0	;EXPECTED DATA PLUS
2720							;RXERR & OVRUN
2721	013070	017701	004610		MOV	0RXDBUF,R1	;ACTUAL
2722	013074	020001			CMP	R0,R1	;COMPARE EXP VS. ACT
2723	013076	001001			BEO	668	
2724	013100	104002			HLT	2	;SPECIFICALLY LOOK AT RXERR &
2725							;OVRUN BITS...THEY BOTH SHOULD BE SET
2726	013102			668:			
2727	013102	104400			SCOPE		
2728							

[illegible]

2705	013364	016777	165540	165510	MOV	PASCNT,ALIGHTS	;DISPLAY PASS COUNT
2706	013372	013701	000042		MOV	0042,P1	;CHECK FOR ACT-11 OR DDP
2707	013376	001405			BFO	PESTRT	;IF NOT, CONTINUE TESTING
2708	013400	000005			RFSET		
2709	013402	004711			LOGICAL:	JSP PC,(R1)	
2790	013404	000240			NOP		
2791	013406	000240			NOP		
2792	013410	000240			NOP		
2793	013412	012767	000340	164356	RESTRT:	MOV 0340,PS	;PREVENT INTERRUPTS (PRIOR 7)
2794	013420	104413			CKSWR		;CHECK FOR "G
2795	013422	012767	002350	165464	MOV	0TST1,RTRN	
2796	013430	000167	160714		JMP	TST1	
2797							
2798							
2799							
2800	013434						
2801							
2802	013434	000424					
2803							
2804	013436	013746	000004		MOV	004,-(SP)	;IF RUNNING ON THE X OR TESTER CHANGE
2805	013442	012737	013462	000004	MOV	018,004	;THIS INSTRUCTION TO A "NOP"(NOP=240)
2806	013450	005737	177000		TST	00177060	;SAVE CONTENTS OF ERROR VECTOR
2807	013454	012637	000004		MOV	(SP)+,004	;SET FOR TIME OUT
2808	013460	000404			RR	28	;TIME OUT ON X OR ?
2809	013462	022626			RR	28	;RESTORE ERROR VECTOR
2810	013464	012637	000004		RR	28	;GO TO NEXT TEST
2811	013470	000403			RR	38	;CLEAR THE STACK AFTER A TIMEOUT
2812	013472	016767	165420	165414	RR	38	;RESTORE ERROR VECTOR
2813	013500	016716	165410		RR	38	;LOOP ON PRESENT TEST
2814	013504	000002			MOV	NEXT,RTRN	;SET UP NEXT TEST IN RTRN
2815	013506				MOV	RTRN,(SP)	;SET UP STACK FOR RTI
2816	013506	104413			RTI		
2817	013510	032777	040000	165362			
2818	013510	001407					
2819	013520	000432					
2820	013522	105777	165356				
2821	013526	100027					
2822	013530	017700	165352				
2823	013534	000412					
2824	013536	032777	004000	165334			
2825	013544	001006					
2826	013546	005267	165352				
2827	013552	026767	165346	165342			
2828	013560	101412					
2829	013562	105007	165436				
2830	013566	005067	165332				
2831	013572	012767	000004	165322			
2832	013600	016767	165312	165306			
2833	013606	016716	165302				
2834	013612	000002					
2835	013614	001407					
2836	013616	000432					
2837							
2838							
2839							
2840	013620	104413					

2041	013622	032777	001000	165250	BIT	0SW09,0SWR	
2042	013630	001402			REQ	10	
2043	013632	016716	165262		MOV	LOCK,(SP)	
2044	013636	000002		10:	RTI		
2045							
2046							
2047							
2048	013640	010546			.TYPE:	MOV	R5,-(SP)
2049	013642	017625	000002			MOV	02(SP),R5
2050	013646	062766	000002	000002		ADD	02,2(SP)
2051	013654	105715		10:	TSTB	(R5)	;LOOK FOR "0"
2052	013656	001406			BFC	30	
2053	013660	105777	165224	20:	TSTB	0TPCSR	;TEST DONE BIT
2054	013664	100375			HPL	20	
2055	013666	112577	165220		MOVB	(R5)+,0TPDBR	;TYPE CHAR
2056	013672	000770			RR	10	;DO IT AGAIN UNTIL "0" IS SEEN
2057	013674	012605		30:	MOV	(SP)+,R5	
2058	013676	000002			RTI		
2059							
2060							
2061							
2062	013700	010346			.INSTR:	MOV	R3,-(SP)
2063	013702	010146				MOV	R4,-(SP)
2064	013704	017667	000004	000010		MOV	04(SP),.MSG
2065	013712	062766	000002	000004		ADD	02,4(SP)
2066	013720	104402			.INST1:	TYPE	
2067	013722	000000			.MSG:	R	
2068	013724	012704	017034			MOV	0INRUF,R4
2069	013730	012703	000007			MOV	07,R3
2070	013734	105777	165144	10:	TSTB	0TKCSR	
2071	013740	100375			HPL	10	
2072	013742	117714	165140		MOVB	0TKDBR,(R4)	
2073	013746	142714	000200		BICR	0200,(R4)	
2074	013752	121427	000025		CMPS	(R4),025	;IS IT <"U">
2075	013756	001003			HNE	2000	
2076	013760	104402	016156			TYPE,MCRLF	
2077	013764	000755			BR	.INST1	
2078	013766	122427	000015	20001	CMPS	(R4)+,015	
2079	013772	001423			REQ	INSTR2	
2080	013774	117777	165106	165110	MOVB	0TKDBR,0TPDBR	
2081	014002	105777	165102	20:	TSTB	0TPCSR	
2082	014006	100375			BPL	20	
2083	014010	005303			DFC	R3	
2084	014012	001350			BNE	10	
2085	014014	000402			BR	.INSTG	
2086	014016	010346			.INSTE:	MOV	R3,-(SP)
2087	014020	010446				MOV	R4,-(SP)
2088	014022	104402			.INSTG:	TYPE	
2089	014024	016152			MOB		
2090	014026	005737	015314		TST	00RDSW	
2091	014032	001402			REQ	4000	
2092	014034	104402	016156			TYPE,MCRLF	
2093	014040	000727		40001	RR	.INST1	
2094	014042	012604			INSTR2:	MOV	(SP)+,R4
2095	014044	012603				MOV	(SP)+,R3
2096	014046	000002			RTI		

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2953 014260 000000 DFVADR: 0
2954 014262 000000 LOPITS: 0
2955 014263 000000 ADPCNT=LOPITS+1
2956
2957 ;SAVE PC OF TEST THAT FAILED AND R0-R5
2958
2959 014264 016667 000004 164702 .SAVR5: MOV 4(SP),SAVPC
2960
2961 ;SAVE R0-R5
2962
2963 014272 010567 164672 SVR5: MOV R5,SAVR5
2964 014276 010467 164664 MOV R4,SAVR4
2965 014302 010367 164656 MOV R3,SAVR3
2966 014306 010267 164650 MOV R2,SAVR2
2967 014312 010167 164642 MOV R1,SAVR1
2968 014316 010067 164634 MOV R0,SAVR0
2969 014322 000002 RTI
2970
2971 ;PSTORE R0-R5
2972
2973 014324 016700 164626 .RFS05: MOV SAVR0,R0
2974 014330 016701 164624 MOV SAVR1,R1
2975 014334 016702 164622 MOV SAVR2,R2
2976 014340 016703 164620 MOV SAVR3,R3
2977 014344 016704 164616 MOV SAVR4,R4
2978 014350 016705 164614 MOV SAVR5,R5
2979 014354 000002 RTI
2980
2981 ;CONVERT OCTAL NUMBER TO ASCII AND OUTPUT TO TELEPRINTER
2982
2983 014356 104402 .CONVP: TYPE
2984 014360 016156 MCRLF
2985 014362 010046 .CNVRT: MOV R0,-(SP)
2986 014364 010146 MOV R1,-(SP)
2987 014366 010346 MOV R3,-(SP)
2988 014370 010446 MOV R4,-(SP)
2989 014372 010546 MOV R5,-(SP)
2990 014374 017601 000012 MOV 012(SP),R1
2991 014400 016767 002470 164542 MOV TEMP,TEMP3
2992 014406 002766 000002 000012 ADD 02,12(SP)
2993 014414 012167 000154 MOV (R1)+,WRDCNT
2994 014420 112167 000152 18: MOVE (R1)+,CHRCNT
2995 014424 112167 000147 MOVE (R1)+,SPACNT
2996 014430 013167 000144 MOV 0(R1)+,BINWRD
2997 014434 016704 000140 26: MOV BINWRD,R4
2998 014440 116705 000132 MOVE CHRCNT,R5
2999 014444 012700 017074 MOV 0TEMP,R0
3000 014450 010403 38: MOV R4,R3
3001 014452 042703 177770 BIC 0177770,R3
3002 014456 062703 000260 ADD 0060,R3
3003 014462 110320 MOVE R3,(R0)+
3004 014464 006204 ASR R4
3005 014466 042704 100000 BIC 0100000,R4
3006 014472 006204 ASR R4
3007 014474 006204 ASR R4
3008 014476 005305 DEC R5

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;SHIFT FOR NEXT 0
;CLUGE TO STOP BIT 15 PROPAGATING.
;DITTO
;DITTO

3009	014500	001363			BNE	38	
3010	014502	012703	017134		MOV	00DATA,R3	
3011	014506	114023		48:	MOV	=(R0),(R3)+	
3012	014510	105367	000062		DECR	CHRCNT	
3013	014514	001374			BNE	48	
3014	014516	105767	000055		TSTB	SPACNT	
3015	014522	001405			REQ	68	
3016	014524	112723	000040	58:	MOV	0040,(R3)+	
3017	014530	105367	000043		DECR	SPACNT	
3018	014534	001373			BNE	58	
3019	014536	105013		68:	CLRB	(R3)	
3020	014540	104402			TYPE		
3021	014542	017134			MDATA		
3022	014544	005367	000024		DEC	WPDCNT	
3023	014550	001323			HNE	18	
3024	014552	016767	164372	WP2314	MOV	TFMP3,TEMP	
3025	014560	012605			MOV	(SP)+,R5	
3026	014562	012604			MOV	(SP)+,R4	
3027	014564	012603			MOV	(SP)+,R3	
3028	014566	012601			MOV	(SP)+,R1	
3029	014570	012600			MOV	(SP)+,R0	
3030	014572	000002			RTI		
3031	014574	000000			WPDCNT: 0		
3032	014576	000000			CHRCNT: 0		
3033		014577			SPACNT=CHRCNT+1		
3034	014600	000000			BINWRD: 0		
3035							
3036							
3037							
3038							
3039							
3040							
3041	014602	017605	000000		.SETFLG:MOV	0(SP),R5	
3042	014606	122767	000116	002220	CMPE	0'N,INBUF	;IS IT "N" ?
3043	014614	001002			BNE	18	
3044	014616	105015			CLRB	(R5)	;000
3045	014620	000406			HR	28	
3046	014622	122767	000131	002204	18:	CMPE	0'Y,INBUF ;IS IT "Y" ?
3047	014630	001005			HNE	38	
3048	014632	112715	177777		MOV	0-1,(R5)	;377
3049	014636	002716	000002		28:	ADD	02,(SP)
3050	014642	000002			RTI		
3051	014644	104404			38:	INSTR	;PTRY
3052	014646	000755			BR	.SETFLG	
3053							
3054							
3055							
3056							
3057							
3058	014650	011616			.TRPSP:MOV	(SP),-(SP)	;GET PC OF RETURN
3059	014652	162716	000002		SUB	02,(SP)	;PC OF TRAP
3060	014656	017616	000000		MOV	0(SP),(SP)	;GET TRP
3061	014662	000316			TPPOK:ASL	(SP)	;MULTIPLY TRAP ARG BY 2
3062	014664	002716	177001		RIC	017001,(SP)	;CLEAR UNWANTED BITS
3063	014670	002716	001226		ADD	0,TRPTAR,(SP)	;POINTER TO SUBROUTINE ADDRESS
3064	014674	017616	000000		MOV	0(SP),(SP)	;SUBROUTINE ADDRESS

3065	014700	000136			JMP	0(SP)+	;GO TO SUBROUTINE
3066							
3067							
3068							
3069	014702	104413			.HLT:	CKSWP	;CHECK FOR "G
3070	014704	032777	020000	164166		BIT	;INHIBIT ERROR TYPE OUT ?
3071	014712	001061				RNE	
3072	014714	021667	164214			CMP	(SP),LSTERR
3073	014720	001401				REQ	18
3074	014722	011667	164206			MOV	(SP),LSTERR
3075	014726	105067	164272			CLRB	ERRFLG
3076	014732	104426			18:	SAVES	
3077	014734	011665				MOV	(SP),R5
3078	014736	162705	000002			SUB	02,R5
3079	014742	011504				MOV	(R5),P4
3080	014744	006304				ASL	R4
3081	014746	061504				AND	(R5),P4
3082	014750	006304				ASL	R4
3083	014752	042704	177001			RIC	0177001,R4
3084	014756	062704	017650			ADD	0,ERRTAB,R4
3085	014762	012467	000004			MOV	(R4)+,ERRMSG
3086	014766	012467	000006			MOV	(R4)+,DATAHD
3087	014772	011467	000054			MOV	(R4),DATABP
3088	014776	105767	164222			TSTR	ERRFLG
3089	015002	001403				REQ	TYPMSG
3090	015004	005767	000002			TST	DATABP
3091	015010	001414				BNE	TYPDAT
3092	015012	104410				TYPMSG:	CONVRT
3093	015014	015144				ERTAB0	
3094	015016	112767	177777	164200		MOV	0-1,ERRFLG
3095	015024	104402				TYPE	
3096	015026	000000				ERRMSG:	0
3097	015030	005767	000004			TST	DATAHD
3098	015034	001402				REQ	TYPDAT
3099	015036	104402				TYPE	
3100	015040	000000				DATAHD:	0
3101	015042	005767	000004			TYPDAT:	TST
3102	015046	001402				REQ	DATABP
3103	015050	104410				CONVRT	RESPEC
3104	015052	000000				DATABP:	0
3105	015054	104407				RESPEC:	RES05
3106	015056	005777	164016			HALTS:	TST
3107	015062	100005					0SWP
3108	015064	010006					EXITER
3109	015066	016600	000002				
3110	015072	000000					
3111	015074	012600					
3112	015076	104413				EXITER:	CKSWP
3113	015100	005267	164226			INC	ERRCNT
3114	015104	032777	000400	163766		BIT	0SW00,0SWP
3115	015112	001007				RNE	18
3116	015114	032777	002000	163756		BIT	0SW10,0SWP
3117	015122	001407				REQ	28
3118	015124	016767	163766	163762		MOV	NEXT,RTRN
3119	015132	012706	001100			MOV	0STACK,SP
3120	015136	000177	163752			JMP	0RTPN

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3121 015142 000002      28: PTI
3122 015144 000001      EPTAB: 1
3123 015146 006      002      ,BYTE 6,2
3124 015150 001174      SAVPC
3125      ;FNTER HERE ON POWER FAILURE
3126
3127
3128 015152 P10046      .PFAIL: MOV R0,-(SP)      ;SAVE R0-R5 ON PROCESSOR STACK
3129 015154 010146      MOV R1,-(SP)
3130 015156 010246      MOV R2,-(SP)
3131 015160 010346      MOV R3,-(SP)
3132 015162 010446      MOV R4,-(SP)
3133 015164 010546      MOV R5,-(SP)
3134 015166 016746 162632      MOV 24,-(SP)
3135 015172 010667 163774      MOV SP,SAVSP      ;SAVE STACK POINTER
3136 015176 012767 015210 162620      MOV 0PESTANT,24      ;SET UP FOR POWER UP TRAP
3137 015204 000000      HALT      ;HALT ON POWER DOWN NORMAL
3138 015206 000777      18: RP 18
3139
3140      ;PROCESSOR WILL TRAP HERE WHEN POWER IS RESTORED
3141
3142 015210 016706 163756      RESTAP: MOV SAVSP,SP      ;RESTORE STACK POINTER
3143 015214 012605      MOV (SP)+,R5      ;RESTORE R0-R5
3144 015216 012604      MOV (SP)+,R4
3145 015220 012603      MOV (SP)+,R3
3146 015222 012602      MOV (SP)+,R2
3147 015224 012601      MOV (SP)+,R1
3148 015226 012600      MOV (SP)+,R0
3149 015230 012767 015152 162566      MOV 0,PFAIL,24      ;SET UP FOR POWER FAILURE
3150 015236 012767 000340 162532      MOV 0340,PS
3151 015244 012706 001100      MOV 0STACK,SP
3152 015250 005067 001620      CLR TEMP
3153 015254 005267 001614      18: INC TEMP
3154 015260 001375      RNE 18
3155 015262 104410      CONVRT
3156 015264 015306      PFTAB
3157 015266 104402      TYPE
3158 015270 016161      MPFAIL
3159 015272 005067 163726      CLR EPFLG
3160 015276 005067 163632      CLR LSTERR
3161 015302 000177 163606      JMP 0RTPN
3162 015306 000001      PFTAB: 1
3163 015310 006      002      ,BYTE 6,2
3164 015312 001114      RTN
3165
3166
3167      ;CHECK SWITCH REGISTER ROUTINE. CHECKS FOR "G" TO ALLOW CHANGING
3168      ;OF LOC.176.
3169      ;LOCATIONS USED:
3170 015314 000000      RDSW: ,WORD 0
3171
3172
3173 015316 005737 000042      .CKSWP: TST 0042
3174 015322 001042      BNE OUT
3175 015324 022767 000176 163546      CMP 0SWPFG,SWP      ;SOFTWARE SWITCH REGISTER PRESENT
3176 015332 001036      BNE OUT      ;NO, GET OUT

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;YES, WAIT FOR
;READY, GET CHARACTER
;AND STRIP OFF
;THE GARBAGE
;IS IT A <'G>

```

3233	015730	053111	051105	041440	
3234	015736	047117	051124	040117	
3235	015744	051040	043505	051511	
3236	015752	042524	020122	042101	
3237	015760	051104	051505	020523	
3238	015766	000			
3239	015767	075	042504	044526	DEVICE: .ASCIZ /#DEVICE /
3240	015774	042503	020040	000	
3241	016001	015	044012	053517	MCOW: .ASCIZ <15><12>/HOW NOW BROWN COW? ...SELECT SOMETHING TO RUN 0ACTREG/
3242	016006	047040	053517	041040	
3243	016014	047522	047127	041440	
3244	016022	053517	020077	027056	
3245	016030	051456	046105	041505	
3246	016036	020124	047523	042515	
3247	016044	044124	047111	020107	
3248	016052	047524	051040	047125	
3249	016060	040040	041501	051124	
3250	016066	043505	000		
3251	016071	015	047412	052125	MRANGE: .ASCIZ <15><12>/OUT OF RANGE:RFTYPE LAST DEVICE PXC8P ADDRESS-/
3252	016076	047440	020106	040522	
3253	016104	043516	035105	042522	
3254	016112	054524	042520	046040	
3255	016120	051501	020124	042504	
3256	016126	044526	042503	051040	
3257	016134	041530	051123	040440	
3258	016142	042104	042522	051523	
3259	016150	000055			
3260	016152	020040	000077		MON: .ASCIZ / ?/
3261	016156	005015	000		MCRLF: .ASCIZ <15><12>
3262	016161	040	050040	053517	MPFAIL: .ASCIZ / POWER FAILURE, PROGRAM RESTART AT TEST IN PROGRESS/
3263	016166	051105	043040	044501	
3264	016174	052514	042522	020054	
3265	016202	051120	043517	040522	
3266	016210	020115	042522	052123	
3267	016216	051101	020124	052101	
3268	016224	052040	051505	020124	
3269	016232	047111	050040	047522	
3270	016240	051107	051505	000123	
3271	016246	005015	047105	020104	MEPASS: .ASCIZ <15><12>/END OF PASS TAPE A/
3272	016254	043117	050040	051501	
3273	016262	020123	040524	042520	
3274	016270	040440	000		
3275	016273	015	051012	000	MR: .ASCIZ <15><12>/R/
3276	016277	015	052012	051505	MTSTPC: .ASCIZ <15><12>/TEST PC-/
3277	016304	020124	041520	000055	
3278	016312	005015	047514	045503	MLOCK: .ASCIZ <15><12>/LOCK ON SELECTED TEST? (Y OR N)-/
3279	016320	047440	020116	042523	
3280	016326	042514	052103	042105	
3281	016334	052040	051505	037524	
3282	016342	024040	020131	051117	
3283	016350	047040	020451	000	
3284	016355	015	042012	020125	MLEVEL: .ASCIZ <15><12>/DU PRIORITY LEVEL-/
3285	016362	051120	047511	044522	
3286	016370	054524	046040	053105	
3287	016376	046105	000055		
3288	016402	005015	020043	043117	MSYNC: .ASCIZ <15><12>/# OF SYNC CHARS SELECTED (1 OR 2)-/

3289	016410	051440	047131	020103	
3290	016416	044103	051101	020123	
3291	016424	042523	042514	052103	
3292	016432	042105	024040	030440	
3293	016440	047440	020122	024462	
3294	016446	000055			
3295	016450	005015	051511	051440	HWIRE6: .ASCIZ <15><12>/IS SEC XMIT JUMPER 06 IN? (Y OR N)-/
3296	016456	041505	054040	044515	
3297	016464	020124	052512	050115	
3298	016472	051105	021440	020066	
3299	016500	047111	020077	054450	
3300	016506	047440	020122	024516	
3301	016514	000055			
3302	016516	005015	051511	051440	HWIRE5: .ASCIZ <15><12>/IS SEC RFC JUMPER 05 IN? (Y OR N)-/
3303	016524	041505	051040	041505	
3304	016532	045040	046525	042520	
3305	016540	020122	032443	044440	
3306	016546	037516	024040	020131	
3307	016554	051117	047040	020451	
3308	016562	000			
3309	016563	015	044012	020123	HWIRE4: .ASCIZ <15><12>/IS OPT CLR ENABLF JUMPER 04 IN? (Y OR N)-/
3310	016570	050117	020124	040103	
3311	016576	020122	047105	041101	
3312	016604	042514	045040	040525	
3313	016612	042520	020122	032043	
3314	016620	044440	037514	024040	
3315	016626	020131	051117	047040	
3316	016634	026451	000		
3317	016637	015	040412	042522	MFXTJ: .ASCII <15><12>/ARE YOU RUNNING IN MAINT MODE EXTERNAL?/
3318	016644	054440	052517	051040	
3319	016652	047125	044516	043516	
3320	016660	044440	020116	040515	
3321	016666	047111	020124	047515	
3322	016674	042504	042440	052130	
3323	016702	051105	040516	037514	
3324	016710	005015	040401	042116	.ASCII <15><12><1>/AND DO YOU HAVE THE EXTERNAL MODEM BYPASS/
3325	016716	027040	027056	027056	
3326	016724	042040	020117	047531	
3327	016732	020125	040510	042526	
3328	016740	052040	042510	042440	
3329	016746	052130	051105	040516	
3330	016754	020114	047515	042504	
3331	016762	020115	054502	040520	
3332	016770	051523			
3333	016772	005015	045001	046525	.ASCIZ <15><12><1>/JUMPER CONNECTION ON ?(Y OR N)-/
3334	017000	042524	020122	047503	
3335	017006	047116	041505	047524	
3336	017014	020122	047117	037440	
3337	017022	054450	047440	020122	
3338	017030	024516	000055		
3339					.EVEN
3340					
3341					;BUFFERS FOR INPUT-OUTPUT
3342					
3343	017034	000040	INBUF: .ALKB	40	
3344	017074	000040	TEMP: .ALKB	40	

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3345 017134 000243          MDATA: ,BLKB 40
3346                          ;.....
3347                          ;UTILITIES
3348                          ;.....
3349
3350                          ;THIS UTILITY CALCULATES PRIORITY LEVEL
3351 017174 006367 000244  D'LFV:  ASL      D'PRT  ;SHIFT LEFT
3352 017200 006367 000240          ASL      D'PRT  ;
3353 017204 006367 000234          ASL      D'PRT  ;
3354 017210 006367 000230          ASL      D'PRT  ;
3355 017214 006367 000224          ASL      D'PRT  ;
3356 017220 016767 000220 000220  MOV      D'PRT,LESS1 ;MOVE THIS TO LESS1
3357 017226 162767 000216 000212  SUB      01,LESS1 ;CREATE LESS1
3358 017234 042767 000214 000210  RTC      037,LESS1 ;CLEAR TNZVC
3359 017242 000207          RTS      PC
3360 017244 000204          D'PRT:  LEVELS
3361 017246 000204          LESS1:  LEVEL4 ;LEVEL TO ALLOW INTERRUPTS
3362
3363                          ;NEW DU ADDRESSES
3364 017250 016767 000204 000202  D'ADDR: MOV      D'BASE,FXCSR ;XXX0
3365 017256 005267 000200          INC      D'BASE
3366 017262 016767 000196 000192  MOV      D'BASE,HPXCSR ;XXX1
3367 017270 005267 000194          INC      D'BASE
3368 017274 016767 000190 000186  MOV      D'BASE,RXDBIF ;XXX2
3369 017302 016767 000174 000170  MOV      D'BASE,PARCSR ;XXX2
3370 017310 005267 000170          INC      D'BASE
3371 017314 016767 000166 000162  MOV      D'BASE,HRXDRUF ;XXX3
3372 017322 016767 000164 000160  MOV      D'BASE,HPARCSR ;XXX3
3373 017330 005267 000160          INC      D'BASE
3374 017334 016767 000156 000152  MOV      D'BASE,FXCSR ;XXX4
3375 017342 005267 000154          INC      D'BASE
3376 017346 016767 000150 000146  MOV      D'BASE,HTXCSR ;XXX5
3377 017354 005267 000148          INC      D'BASE
3378 017360 016767 000144 000140  MOV      D'BASE,TXDRUF ;XXX6
3379 017366 005267 000142          INC      D'BASE
3380 017372 016767 000138 000134  MOV      D'BASE,HTXDRUF ;XXX7
3381 017400 000207          RTS      PC
3382 017402 000204          D'BASE:  0
3383
3384                          ;THIS UTILITY POKES THE MAINT DATA BASED UPON THE
3385                          ;INFORMATION CONTAINED IN TEMP1 AND IT IS
3386                          ;SHIFTED IN BY THE CONTENTS OF SHIFT
3387 017404 042777 040000 000302  WPOKE:  RIC      0MTDATA,0TXCSR
3388 017412 005267 161530          CLR      TEMP2
3389 017416 006067 161522          ROR      TEMP1 ;FORCE CARRY
3390 017422 006067 161520          POP      TEMP2 ;PICK UP CARRY IN BIT 15
3391 017426 006267 161514          ASH      TEMP2 ;SHIFT INTO BIT 14
3392 017432 042767 100000 161506  BIC      0BIT14,TEMP2 ;CLR BIT 15
3393 017440 056777 161502 000246  RIS      TEMP2,0TXCSR ;POKE MAINT DATA
3394 017446 042777 020000 000240  RIC      0CLK,0TXCSR ;POKE CLK
3395 017454 052777 020000 000232  BIS      0CLK,0TXCSR ;
3396 017462 005367 161452          DEC      SHIFT
3397 017466 001346          ENL      WPOKE
3398 017470 000207          RTS      PC
3399
3400                          ;THIS ROUTINE CALCULATES ODD PARITY FOR AN 8 BIT CHAR

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3401 017472 016767 161446 161446 0000: MOV    TFMP1,TEMP2    ;SAVE TEMP1
3402 017500 005267 161444      CLR    TEMP3
3403 017504 012727 000010      MOV    00,.(PC)+
3404 017510 000000      18:    0
3405 017512 006267 161430      28:    ROR    TEMP2
3406 017516 005567 161426      ADC    TEMP3
3407 017522 005367 177762      DEC    18
3408 017526 001371      HNE    28
3409 017530 006267 161414      ROP    TEMP3
3410 017534 103404      RCS    38
3411 017536 052767 000400 161400  HIS    0BIT0,TEMP1    ;SET ODD PARITY
3412 017544 000403      BR     48
3413 017546 042767 000400 161370 38:    HIC    0BIT0,TEMP1    ;CLR EVEN PARITY
3414      ;TEMP1 NOW HAS ODD PARITY CHARACTER
3415 017554 000207      48:    RTS    PC
3416
3417      ;THIS ROUTINE CALCULATES EVEN PARITY FOR AN 8 BIT CHARACTER
3418 017556 016767 161362 161362 EVEN0: MOV    TEMP1,TEMP2    ;SAVE TEMP1
3419 017564 005267 161360      CLR    TEMP3
3420 017570 012727 000010      MOV    00,.(PC)+
3421 017574 000000      18:    0
3422 017576 006267 161344      28:    ROR    TEMP2
3423 017602 005567 161342      ADC    TEMP3
3424 017606 005367 177762      DEC    18
3425 017612 001371      HNE    28
3426 017614 006267 161330      ROP    TEMP3
3427 017620 103404      BCC    38
3428 017622 052767 000400 161314  HIS    0BIT0,TEMP1    ;SET EVEN PARITY
3429 017630 000403      BR     48
3430 017632 042767 000400 161304 38:    HIC    0BIT0,TEMP1    ;CLR ODD PARITY
3431      ;TEMP1 NOW HAS EVEN PARITY CHARACTER
3432 017640 000207      48:    RTS    PC
3433 017642 062716 000007  TRPPEG: ADD    02,(SP) ;ALLOW IT TO "CRUNCH" INTO HLT BACK
3434      ;IN MAIN PART OF THE PROGRAM
3435 017646 000002      RTI
3436      ;FRROR HLT TABLE
3437 017650 017734      .FRPTAB:  E40    ;HLT 0  BIT ERROR (GENERAL)
3438 017652 000000      0
3439 017654 000000      0
3440 017656 017752      E41    ;HLT 1  REGISTER ERROR
3441 017660 020121      DH1
3442 017662 020142      DT1
3443 017664 020012      E42    ;HLT 2  RECEIVED FRROR
3444 017666 020121      DH1
3445 017670 020142      DT1
3446 017672 020054      E43    ;HLT 3  TRANSMITTER ERROR
3447 017674 020121      DH1
3448 017676 020142      DT1
3449      ;DEFAULT DU ADDRESSES
3450 017700 160000  PXCSR: 160000
3451 017702 160001  HPXCSR: 160001
3452 017704 160002  PXDHUF: 160002
3453 017706 160003  HPXDBUF: 160003
3454 017710 160002  PARCSP: 160002
3455 017712 160003  HPAPCSP: 160003
3456 017714 160004  TXCSR: 160004

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3457	017716	160045			MTXCSR: 160045
3458	017720	160046			TXDRUF: 160046
3459	017722	160047			MTXDBUF: 160047
3460					;DEFAULT DU VECTORS
3461	017724	000770			DIIRIV: 770 ;REC INTR VECTOR
3462	017726	000772			DIIRIS: 772 ;REC INTR STATUS
3463	017730	000774			DUTIV: 774 ;XMIT INTR VECTOR
3464	017732	000776			DUTIS: 776 ;XMIT INTR STATUS
3465					;FRPOP MESSAGES
3466	017734	036440	042440	051122	EM0: .ASCIZ / = ERROR PC/
3467	017742	051117	050040	000103	
3468	017750	036440	051040	043505	EM1: .ASCIZ / = REGISTER FRPOP PC/<15><12><1>/REGISTER /
3469	017756	051511	042524	020122	
3470	017764	051105	047522	020122	
3471	017772	041520	045015	051001	
3472	020000	043505	051511	042524	
3473	020006	020122	000040		
3474	020012	036440	051040	041505	EM2: .ASCIZ / = RECEIVER ERROR PC/<15><12><1>/REGISTER /
3475	020020	044505	042526	020122	
3476	020026	051105	047522	020122	
3477	020034	041520	045015	051001	
3478	020042	043505	051511	042524	
3479	020050	020122	000040		
3480	020054	036440	052040	040522	EM3: .ASCIZ / = TRANSMITTER ERROR PC/<15><12><1>/REGISTER /
3481	020062	051516	044515	052124	
3482	020070	051105	042440	051122	
3483	020076	051117	050040	040503	
3484	020101	000012	042522	044507	
3485	020112	052123	051105	020040	
3486	020120	000			
3487					;DATA HEADERS FOR ERROR MESSAGES
3488	020121	105	050130	041505	DH1: .ASCIZ /EXPECTED ACTUAL/
3489	020126	042524	020104	040440	
3490	020134	052103	040525	000114	
3491					.FVFN
3492					;DATA TABLES FOR FRPOP MESSAGES
3493	020142	000003			DT1: 3
3494	020144	000	004		.BYTE 6,4
3495	020146	001164			SAVR3 ;REGISTER
3496	020150	000	004		.BYTE 6,4
3497	020152	001156			SAVR0 ;EXPECTED DATA
3498	020154	000	002		.BYTE 6,2
3499	020156	001160			SAVR1 ;ACTUAL DATA
3500		000001			.FND

AAA	002046	9890												
ACTREG	001216	0370	9370	9510	9520	9590	2742	2745	2755					
ADPCNT	014263	29470	29460	29550										
BASEAD	001244	0420	9190	9560	957	9630	9650	27490	27610	2765				
BASEIV	001212	0050	9290	27500	27620	2767	27680	2769	27700	2771	27720	2773	27740	
BRB	001664	936	9600											
BINWRD	014620	29960	2997	30340										
BITW	002000	7170	1607	1614	1627	1634	1644	1660	1667	1677				
BITW	000001	0650	093	724	1594									
BIT1	000002	0640	092											
BIT10	002000	0550	083	717										
BIT11	004000	0540	082	1456	1457	1461	1462	1467	1469					
BIT12	010000	0530	081	090	1401	1402	1406	1407	1492	1494				
BIT13	000000	0520	080	097	710									
BIT14	000000	0510	079	096	715									
BIT15	100000	0500	078	095	714	3392								
BIT2	000000	0630	091	1032										
BIT3	000001	0620	090	723										
BIT4	000002	0610	089	722										
BIT5	000000	0600	088	721	1605									
BIT6	000000	0590	087	720										
BIT7	000200	0580	086	719										
BIT8	000400	0570	085	701	710	3411	3413	3420	3430					
BIT9	001000	0560	084	700										
BREAK	000001	7240	1330	1340	1344	1345	1350	1352	1625	1640	1650	1673	2123	2153
		2192	2273	2354	2435	2511	2569	2627	2605					
BRW	013614	1029	1043	20350										
BRX	013616	1030	1044	20360										
CARDCT	010000	0810												
CCC	013350	2741	2764	27010										
CHPCNT	014576	29940	2998	30120	30320	3033								
CKSWR	004413	0490	2794	2816	2840	3069	3112							
CLK	020000	7160	1504	1505	1509	1510	1515	1517	2123	2153	2192	2199	2200	2202
		2203	2273	2280	2281	2283	2284	2354	2361	2362	2364	2365	2435	2442
		2443	2445	2446	2511	2517	2518	2520	2521	2569	2575	2576	2578	2579
		2627	2633	2634	2636	2637	2605	2691	2692	2694	2695	3394	3395	
CNTLU	004414	0510	096											
CONVRT	004411	0450	3106											
CONVFT	004412	0430	2730	3002	3103	3155								
COUNT	001142	7700	22040	22000	22050	22090	23660	23700	24470	24510				
CTS	000000	0800												
DATABP	015052	30070	3000	3101	31040									
DATAHD	015040	30060	3007	31000										
DFVADP	014200	29050	2943	29530										
DFVICE	015767	2739	32390											
DHI	020121	3441	3444	3447	34000									
DISPPE	000174	7450	089											
DLIGHT	077570	0350	080											
DNA	000000	7140	1736											
DNAINT	000000	7210	1600	1609	1613	1614	1619	1621						
DSC	000000	0700	1713											
DSINTE	000000	0800	1270	1271	1275	1276	1281	1283						
DSR	001000	0940												
DSWR	077570	0340	079											
DTR	000002	0920	1140	1149	1153	1154	1159	1165	1170	1003	1955	2045	2094	
DTI	020142	3442	3445	3448	14930									

DUADDP	017250	910	2766	33640										
DUBASE	017402	914	917	27650	3364	33650	3366	33670	3368	3369	33700	3371	3372	33730
		3374	33750	3376	33770	3378	33790	3380	33820					
DULEV	017174	904	33510											
DUPRT	017244	901	33510	33520	33530	33540	33550	3356	33600					
DURIS	017726	27690	34620											
DUPIV	017724	925	920	929	27670	2774	34610							
DUTIS	017732	27730	34640											
DUTIV	017730	27710	34630											
EIGHT	0006000	7090	2176	2156	2430									
EMF	017734	3437	34660											
EM1	017750	3440	34600											
EM2	020012	3443	34740											
EM3	020054	3446	34800											
EPRCNT	001132	7710	0700	31130										
EPPFLG	001224	0170	0690	27030	20290	30750	3000	30940	31590					
EPPMSG	015026	30050	30060											
EPTABN	015144	3003	31220											
EVFN0	017556	34100												
EVERAR	001400	7120												
EVPAR	000400	7010												
EXITER	015076	3107	31120											
FIVE	000000	7060	2105	2514	2572	2630	2600							
FMERR	020000	6070	1773											
HALTS	015056	3071	31000											
HDXEN	000010	7230	1362	1363	1367	1368	1373	1375						
HILIM	014256	20040	2034	20520										
HOLD	001136	7760	1631	1641	1664	1674	1800	1910	1936	1960	1976	1992	2017	2033
		2050	2067	2003	2009									
HPARCS	017712	10090	33720	34550										
HPXCSP	017702	10690	15940	33660	34510									
HPXDBU	017706	10040	33710	34530										
HTXCSP	017716	11140	16050	33760	34570									
HTXDBU	017722	11290	33000	34590										
ICOUNT	001122	7470	2027	20310										
INBUF	017034	902	906	2060	2010	3042	3046	33430						
INIFLG	001222	0150	075	0700										
INSTER	104401	0350	1000	2029	3051									
TR	104403	0330	909	920	930	941	946	976	990	1003	1007	1011	1015	1034
		1047	3107											
INSTR2	014042	2079	20940											
ISYMOD	000000	7050	2149	2156	2507	2514	2565	2572	2623	2630	2601	2600		
JMPRY	001203	7000	1010	1656	1072									
KEEPAD	001206	0030	9170	919	963	965	2761							
KEEPIV	001214	0060	9280	2762										
LASTAD	001210	0040	946	957	971									
LFSS1	017246	33560	33570	33580	33610									
LEVEL0	000000	6750												
LEVEL1	000040	6740												
LEVEL2	000100	6730												
LEVEL3	000140	6720												
LEVEL4	000200	6710	3361											
LEVEL5	000240	6700	3360											
LEVEL6	000300	6690												
LEVEL7	000340	6680	1065	1000	1095	1110	1125	1553						
LIGHTS	001102	7560	0000	0000	27050									

C6

OUT2	007432	1920	20120											
OUT3	007562	1930	20520											
OVRRUN	040000	6960	1705											
PARAM	104405	0370	911	922	943	960	970	1049	3100					
PAPAM1	014110	20090	2930											
PARCSP	017710	10960	21190	21260	21490	21560	21000	21950	22690	22760	23500	23570	24310	24300
		25070	25140	25650	25720	26230	26300	26010	26000	33690	34540			
PAREN	001000	7000												
PARER	010000	6900	1761											
PAPEPP	014164	2012	2914	2916	29250	2935	2937	2939						
PARTI	014246	2920	29400											
PASCNT	001130	7700	0600	27040	2705									
PFTAB	015306	3156	31620											
POPR0	012600	6440	3111											
POP1SP	005726	6420												
POP2SP	022626	6460												
PS	177776	6360	0630	10220	15530	27930	31500							
PUSHR0	010016	6430	3100											
PUSH1S	005746	6410												
PUSH2S	024646	6450												
PDSW	015314	2090	2927	31700	31040	31940								
REACT0	004000	6020	1701	2127	2132	2137	2157	2162	2167	2217	2220	2233	2290	2309
		2314	2379	2300	2305	2460	2471	2476						
REPLAY	013246	2757	2743	27650										
RFSREG	015054	3102	31050											
RFSTAR	015210	3136	31420											
RESTR	013412	2750	2707	27030										
RES05	104407	0410	3105											
RING	000000	6790												
RINTFN	000100	6070	1293	1294	1290	1299	1304	1306						
ROTADD	001220	0100	9300	9500	952	9540	959	9620	27520	2755	27590			
RPOKE	017404	2207	2223	2200	2304	2360	2305	2450	2466	2526	2540	2544	2504	2590
		2602	2642	2656	2660	2700	2714	2710	33070	3397				
RTRN	001114	7640	0730	1052	10560	1050	27050	20120	2013	20320	2033	31100	3120	3161
		3164												
RTS	000000	6910	1101	1102	1106	1107	1192	1100	1203	1905	1971	2020	2070	
RUNA	000000	1	52	69	135	576								
RUNB	000000 U	20	57	69	130	501								
RUNC	000000 U	20	57	69	130	501								
RUND	000000 U	20	57	69	130	501								
RUNE	000000 U	20	57	72	130	501								
RUNF	000000 U	20	57	72	130	501								
RUNIT	013152	2743	27490	2756										
RXCSP	017700	10660	11400	1149	11530	1154	11590	1165	1170	11010	1102	11060	1107	11920
		1190	1203	1210	1215	12100	1220	12250	1231	1236	12470	1240	12520	1253
		12500	1260	12700	1271	12750	1276	12010	1203	12930	1294	12900	1299	13040
		1306	13160	1317	13210	1322	13270	1329	15500	1554	15920	1593	1595	15990
		1600	1609	1701	1713	10070	1009	1010	10660	1077	1070	10030	1094	1099
		10050	1016	1021	10310	1042	1040	10550	1066	10710	1002	10070	1090	2003
		20120	2023	20200	2039	20450	2056	20620	2073	20700	2009	20940	2105	2127
		21310	2132	21360	2137	2157	21610	2162	21660	2167	21970	2213	2217	2224
		2220	22320	2233	2237	2247	22700	2294	2290	2305	2309	23130	2314	2310
		2320	23590	2375	2379	2306	2390	23940	2395	2399	2409	24400	2456	2460
		2467	2471	24750	2476	2400	2490	25150	2527	25730	2505	26310	2643	26090
		2701	2770	33640	34500									
RXDBUF	017704	10010	1700	1750	1761	1773	1705	1797	1051	1052	2196	2242	2277	2323

	2358	2404	2439	2485	2522	2531	2547	2580	2589	2605	2638	2647	2663
	2696	2705	2721	3360	3452								
RXDONE = 000200	6060	1689											
RXERF = 100000	6050	1797											
SAVPC = 001174	7010	2059	3124										
SAVPA = 001156	7040	2060	2973	3497									
SAVR1 = 001164	7050	2067	2974	3499									
SAVR2 = 001167	7060	2060	2975										
SAVR3 = 001164	7070	2065	2976	3495									
SAVR4 = 001166	7080	2064	2977										
SAVR5 = 001170	7090	2063	2978										
SAVSP = 001172	7000	3135	3142										
SAVMS = 104426	8390	3076											
SCOPE = 104400	8270	1074	1089	1104	1119	1134	1142	1175	1200	1241	1264	1287	1310
	1333	1356	1379	1422	1425	1448	1473	1498	1521	1544	1567	1584	1610
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	1843	1857	2110	2141	2171	2252	2333	2414	2495	2553	2611	2669	2727
SCOPI = 104401	8290												
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SEREC = 001200	7050	1010	1029										
SFTFLG = 104412	8470	937	1005	1009	1013	1017	1036						
SEVEN = 004000	7080	2357											
SEXMIT = 001177	7040	1006	1027										
SHIFT = 001140	7770	2205	2221	2206	2302	2367	2303	2448	2464	2524	2538	2542	2582
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SIX = 002000	7070	2276											
SPACNT = 014577	2095	3014	3017	3033									
SPD = 002000	6030												
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SVMS = 014272	2063												
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SW00 = 000001	6170	097											
SW01 = 000002	6160	1045											
SW02 = 000004	6150												
SW03 = 000013	6140												
SW04 = 000020	6130												
SW05 = 000040	6120												
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SW07 = 000400	6100	3114											
SW08 = 001000	6090	2041											
SW09 = 002000	6080	3116											
SW10 = 004000	6070	2024											
SW12 = 010000	6060												
SW13 = 020000	6050	3070											
SW14 = 040000	6040	2017											
SW15 = 100000	6030												
SYNCH0 = 001176	7930	094	990	2211	2292	2373	2454						
SYNEXTE = 020000	7040	2119	2126										
SYNINT = 030000	7230	2100	2195	2269	2276	2350	2357	2431	2438				
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TEMP2	001146	7000	33000	33000	33910	33920	3393	34010	34050	34100	34220			
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TEMP4	001152	7020												
TEMP5	001154	7030												
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TST14	004046	1315	13370											
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TST17	004362	1394	14060											
TST18	004466	1407	14290											
TST19	004572	1430	14540											
TST2	0042436	1463	10770											
TST20	004676	1455	14790											
TST21	005002	1400	15020											
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TST29	006116	1697	16900											
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TXINTE	000100	7200	14310	14320	14360	14370	14420	14440						
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USER	0000000	7260												
VOID	0000001	6030												
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ZERO	013160	27500												
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BY	= 000015	0190	027	0290	0310	0330	0350	0370	0390	0410	0430	0450	0470	0490
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.CNVRT	014362	016	29050											
.CONVR	014356	044	29030											
.EOP	013104	2670	27360											
.ERRTA	017650	3094	34370											
.HLT	014702	737	30690											
.INSTE	014016	036	20060											
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.INSTR	013700	034	20620											
.INST1	013720	20660	2077	2003										
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.SAV05	014264	040	29590											
.SCOPE	013434	070	20000											
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.SETFL	014602	040	30410	3052										
.START	001260	717	0630	073	2740									
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.TRPTA	001226	0240	3063											
.TYPE	013640	032	20400											

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	1856	1882	1890	1903	1920	1925	1947	1953	1970	1986	2002	2007	2027	2044	2060
	2077	2093	2109	2129	2134	2139	2159	2164	2169	2215	2219	2226	2230	2235	2239
	2245	2249	2296	2300	2307	2311	2316	2320	2326	2330	2377	2381	2388	2392	2397
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PPGFRT	5070	500													
PUSYF	5070														
RSETUP	5070	2110	2140	2107	2260	2349	2430	2506	2564	2622	2600				
TSETUP	5070														
REGIN	5070	1019													
SBINAP	5070														
SBUFF	5070	3340													
SCABIE	5070	1004	1906	1932	1956	1972	1988	2013	2029	2046	2063	2079	2095		
SCATCH	5070	730													
SCLPVE	5070	079													
SCONVP	5070	2900													
SDNA	5070														
SEOP	5070	2729													
SGETFL	5070	930	1003	1007	1011	1015	1034								
SGETPA	5070	909	920	940	966	975	1047								
SGETSY	5070	905													
SHEADF	5070	500													
SHLT	5070	3066													
SINSTR	5070	2059													
SISOB	5070														
SMATCH	5070														
SMRR	5070	1603	1695	1707	1730	1755	1767	1779	1791						
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	1499	1522													
SMRW	5070	1560													
MSG	5070	3205													
SPARAM	5070	2097													
SPFAIL	5070	3125													
SPOKE	5070														
SPOKEP	5070	2201	2202	2363	2444	2519	2577	2635	2693						
SPCNET	5070														
SPCAC	5070	2172	2253	2334	2415										
SPREG	5070	2956													
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SRXACT	5070	2112	2142												
SCOPF	5070	2797													
SCOP1	5070	2037													
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SETVE	5070	731													
START	5070	055													
STRIP	5070														

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 DZDUAD.P11 04-AUG-76 00100 CROSS REFERENCE TABLE -- MACRO NAMES

SSYMB0	5070	600													
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STRPAR	5070														
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STYPL	5070	2045													
SUNTB0	5070	1060	1075	1090	1105	1120									
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ERRORS DETECTED: 0
 DEFAULT GLOBALS GENERATED: 0

DZDUAD,DZDUAD/CRF/CPU:20/SOL=HELLO,P11/EQ:RUNA,PAPA,P11,KEFT,P11,DZDUAD,P11
 RUN-TIME: 74 36 3 SECONDS
 RUN-TIME RATIO: 01/64=1.2
 CORE USED: 10K (36 PAGES)